64-Channel Serial to Parallel Converter with P-Channel Open Drain Controllable Output Current

Features

- HVCMOS® technology
- 5.0V CMOS Logic
- Output voltage up to -85V
- Output current source control
- 16MHz equivalent data rate
- Latched data outputs
- Forward and reverse shifting options (DIR pin)
- Diode to VDD allows efficient power recovery
- Hi-Rel processing available

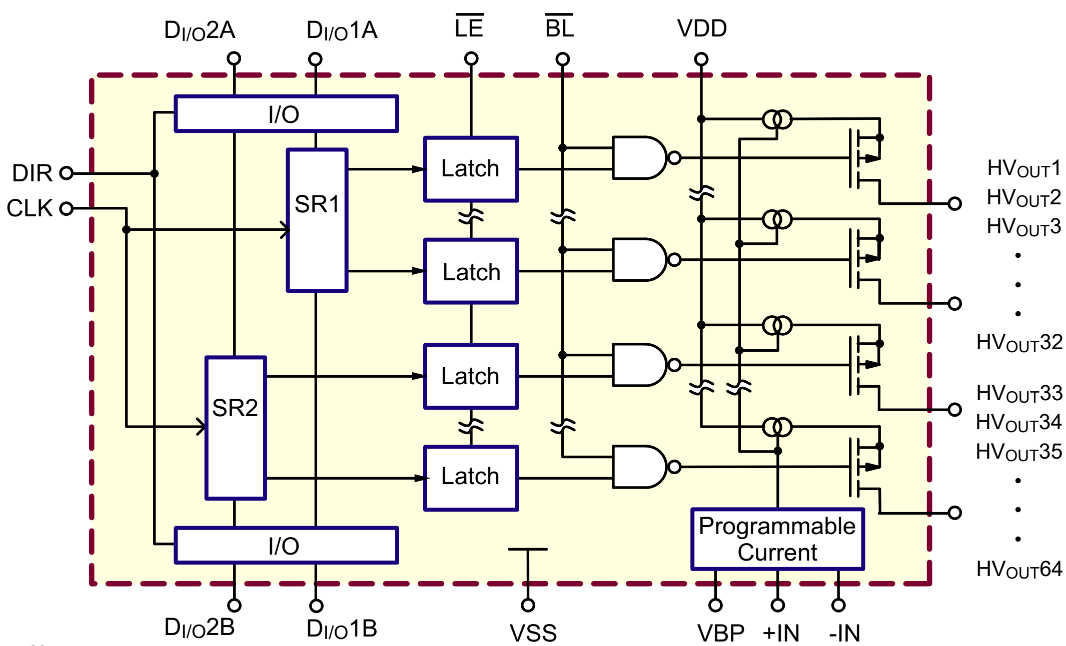
General Description

The HV57009 is a low-voltage serial to high-voltage parallel converter with P-channel open drain outputs. This device has been designed for use as a driver for plasma panels.

The device has two parallel 32-bit shift registers, permitting data rates twice the speed of one (they are clocked together). There are also 64 latches and control logic to perform the blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first shift register through the blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to VSS, and CW shifting when connected to VDD. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}64$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), or the $\overline{BL}$ (blanking) inputs. Transfer of data from the shift registers to latches occurs when the $\overline{LE}$ input is high. The data in the latches is stored when $\overline{LE}$ is low.

The HV570 has 64 channels of output constant current sourcing capability. They are adjustable from 0.1 to 2.0mA through one external resistor or a current source.

Functional Block Diagram



Note:
Each SR (shift register) provides 32 outputs. SR1 supplies outputs 1 to 32 and SR2 supplies outputs 33 to 64.

Ordering Information

Device	Package Options	
	80-Lead PQFP *20.00x14.00mm body* *3.4mm height (max)* *0.65mm pitch*	Die
HV57009	HV57009PG-G	HV57009X

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

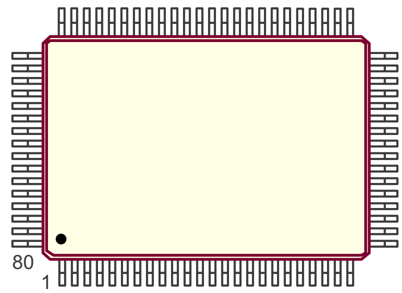
Parameter	Value
Supply voltage, V_{DD}[1]	-0.5V to +7.5V
Output voltage , V_{NN}[1]	V_{DD} + 0.5V to -95V
Logic input levels[1]	-0.3V to V_{DD} +0.3V
Ground current[2]	1.5A
Continuous total power dissipation[3]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature[4]	260°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Notes:

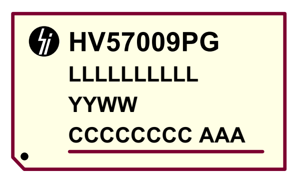
1. *All voltages are referenced to V_{SS}.*
2. *Duty cycle is limited by the total power dissipated in the package.*
3. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.*
4. *1.6mm (1/16inch) from case for 10 seconds*

Pin Configuration



80-Lead PQFP (PG)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
___ = "Green" Packaging

80-Lead PQFP (PG)

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
HV_{OUT}	HV output off voltage	-85	V_{DD}	V
V_{IH}	High-level input voltage	V_{DD} -1.2V	V_{DD}	V
V_{IL}	Low-level input voltage	0	1.2	V
f_{CLK}	Clock frequency per register	DC	8.0	MHz
			4.5	
T_A	Operating free-air temperature	-40	+85	°C

Notes:

Power-up sequence should be the following:

1. Connect ground
2. Apply V_{DD}
3. Set all inputs to a known state

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics *(All voltages are referenced to V_{SS}, V_{SS} = 0, T_A = 25°C)*

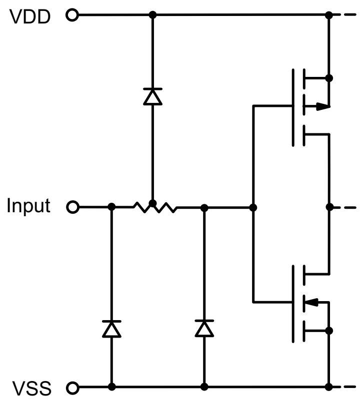
Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	15	mA	V_{DD} = V_{DD} max, f_{CLK} = 8.0MHz
I_{NN}	High voltage supply current		-	-10	µA	Outputs off, HV_{OUT} = -85V (total of all outputs)
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All inputs = V_{DD}, except +IN = V_{SS} = GND
V_{OH}	High level output	Data Out	V_{DD} -0.5V	-	V	I_O = -100µA
		HV_{OUT}	+1.0	V_{DD}	V	I_O = -2.0mA
V_{OL}	Low level output	Data Out	-	+0.5	V	I_O = 100µA
I_{IH}	High-level logic input current		-	1.0	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current		-	-1.0	µA	V_{IL} = 0V
I_{CS}	High output source current		-	-2.0	mA	V_{REF} = 2.0V, R_{EXT} = 1.0KΩ, see Figures 1a and 1b
			-0.1	-		V_{REF} = 0.1V, R_{EXT} = 1.0KΩ, see Figures 1a and 1b
ΔI_{CS}	HV output source current for I_{REF} = 2.0mA		-	10	%	V_{REF} = 2.0V, R_{EXT} = 1.0KΩ

Note:
Current going out of the chip is considered negative.

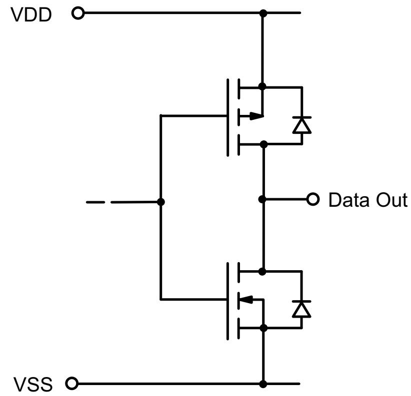
AC Electrical Characteristics *(Logic signal inputs and data inputs have t_r, t_f ≤ 5ns [10% and 90% points] for measurements)*

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	DC	8.0	MHz	Per register
			4.5		When cascading devices
t_{WL}, t_{WH}	Clock width high or low	62	-	ns	---
t_{SU}	Data set-up time before clock rises	20	-	ns	---
t_H	Data hold time after clock rises	15	-	ns	---
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}	-	500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low	-	150	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high	-	150	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	45	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	25	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0	-	ns	---
t_r, t_f	Max. allowable clock rise and fall time (10% and 90% points)	-	100	ns	---

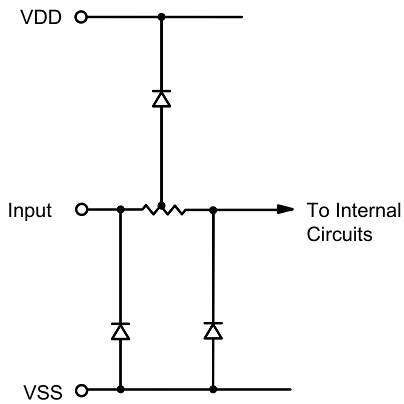
Input and Output Equivalent Circuits



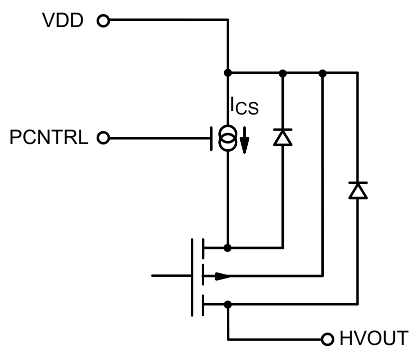
Logic Inputs



Logic Data Output

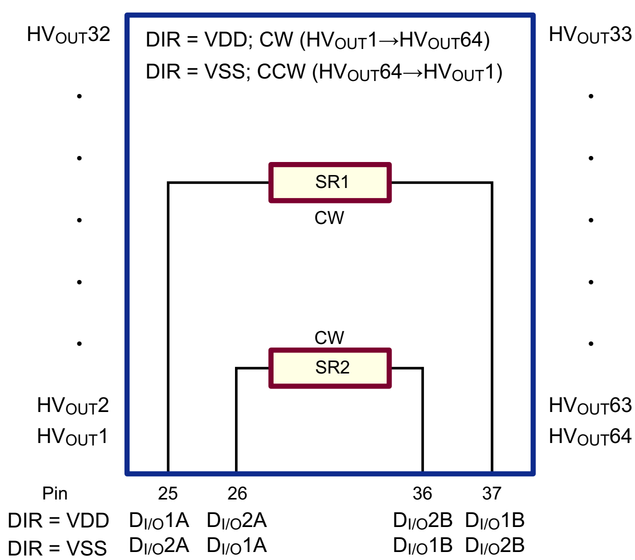


Analog Input

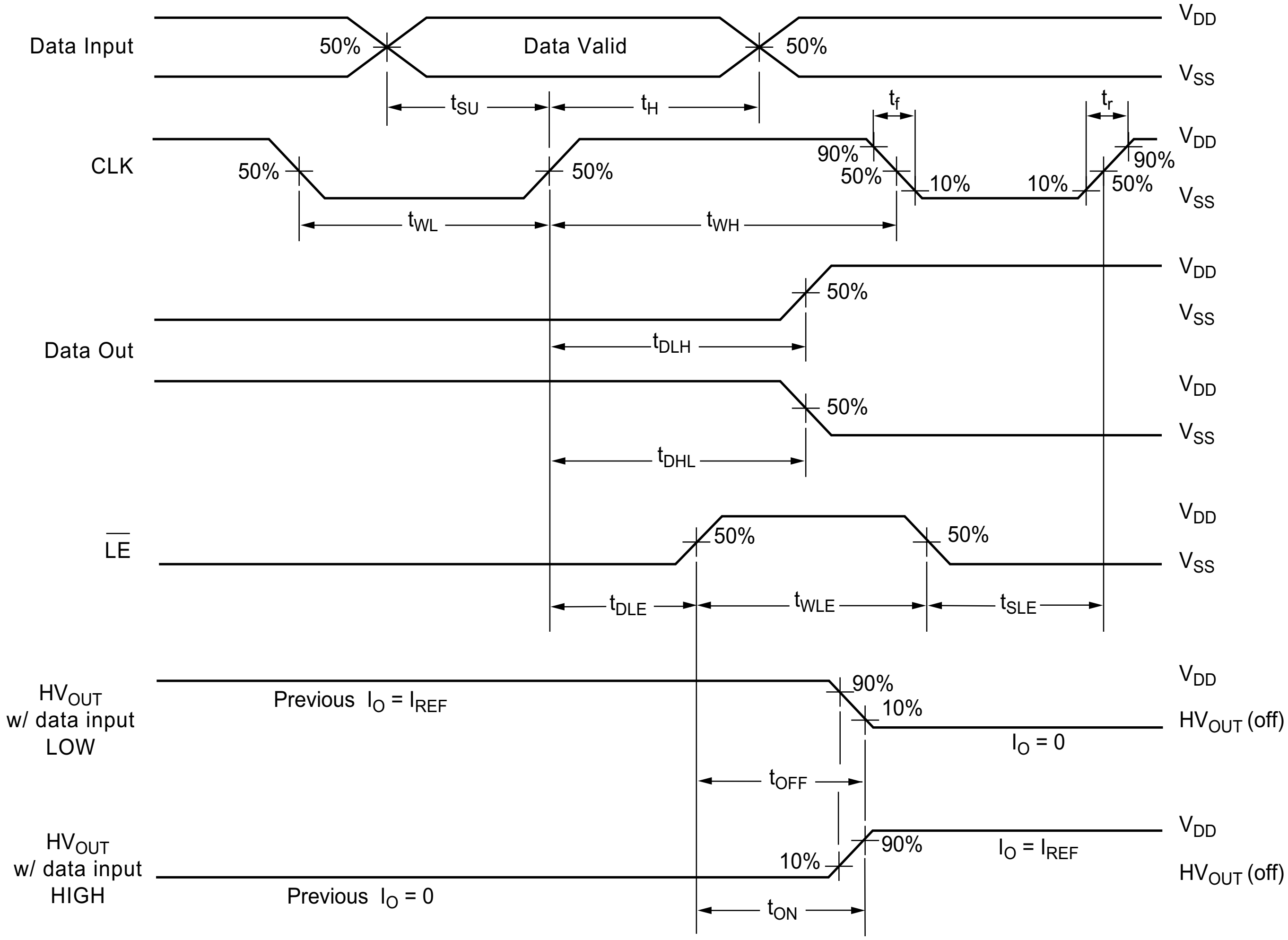


High Voltage Output

Shift Register Operation



Switching Waveforms



Function Table

Function	Inputs					Outputs		
	Data In	CLK	$\overline{LE}$	$\overline{BL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P high	X	X	X	L	X	*	ON	*
Data falls through (latches transparent)	L	_↑‾	H	H	X	L.....L	ON	L
	H	_↑‾	H	H	X	H.....H	OFF	H
Data stored in latches	X	X	L	H	X	*	Inversion of stored data	*
I/O relation	$D_{I/O}$1-2A	_↑‾	H	H	H	$Q_n \rightarrow Q_{n+1}$	New ON or OFF	$D_{I/O}$1-2B
	$D_{I/O}$1-2A	_↑‾	L	H	H	$Q_n \rightarrow Q_{n+1}$	Previous ON or OFF	$D_{I/O}$1-2B
	$D_{I/O}$1-2B	_↑‾	L	H	L	$Q_n \rightarrow Q_{n-1}$	Previous ON or OFF	$D_{I/O}$1-2A
	$D_{I/O}$1-2B	_↑‾	H	H	L	$Q_n \rightarrow Q_{n-1}$	New ON or OFF	$D_{I/O}$1-2A

Note:

** = dependent on previous stage's state. See Figure 7 for DIN and DOUT pin designation for CW and CCW shift.*
H = V_{DD} (Logic)/V_{NN} (HV Outputs)
L = V_{SS}

Typical Current Programing Circuits

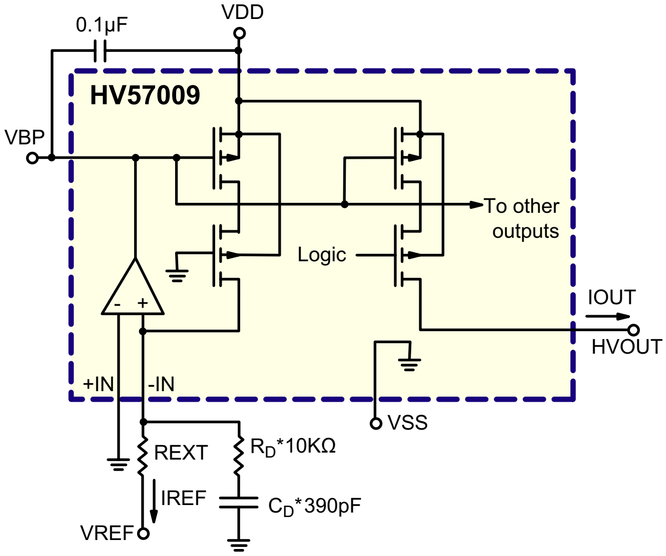


Figure 1a: Negative Control

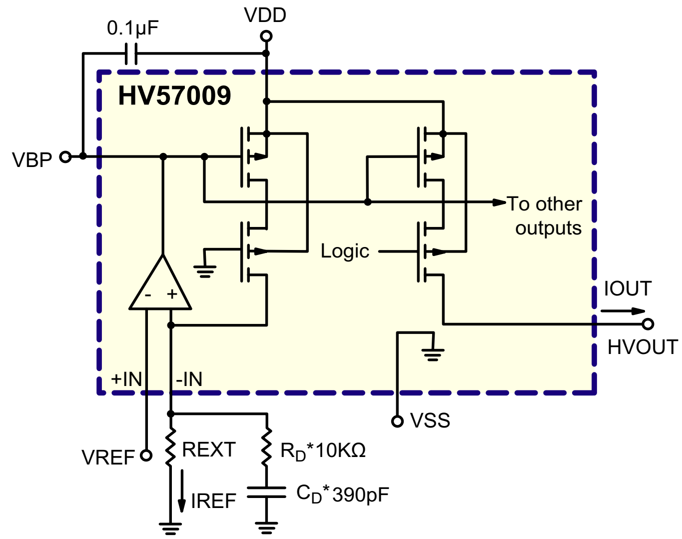


Figure 1b: Positive Control

**Required if R_{EXT} > 10KΩ or R_{EXT} is replaced by a constant current source.*

Since $I_{OUT} = I_{REF} = |V_{REF}| / R_{EXT}$

Therefore:

If I_{OUT} = 2.0mA and V_{REF} = -5.0V → R_{EXT} = 2.5KΩ.
If I_{OUT} = 1.0mA and R_{EXT} = 1.0KΩ → V_{REF} = -1.0V.

If R_{EXT} >10KΩ, add series network R_D and C_D to ground for stability as shown.

This control method behaves linearly as long as the operational amplifier is not saturated. However, it requires a negative power source and needs to provide a current $I_{REF} = I_{OUT}$ for each HV570 chip being controlled.

If HV_{OUT} ≥ +1.0V, the HV_{OUT} cascade may no longer operate as a perfect current source, and the output current will diminish. This effect depends on the magnitude of the output current.

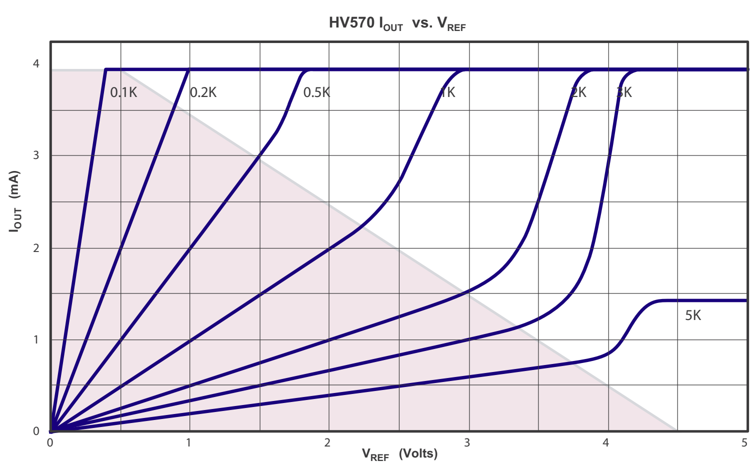
Given I_{OUT} and V_{REF}, the R_{EXT} can be calculated by using:

$R_{EXT} = V_{REF} / I_{REF} = V_{REF} / I_{OUT}$

The intersection of a set of I_{OUT} and V_{REF} values can be located in the graph shown below. The value picked for R_{EXT} must always be in the shaded area for linear operation. This control method has the advantage that V_{REF} is positive, and draws only leakage current. If R_{EXT} > 10KΩ, add series network R_D and C_D to ground for stability as shown.

Note:

Lower reference current I_{REF}, results in higher distortion, ΔI_{CS}, on the output.



Pin Function

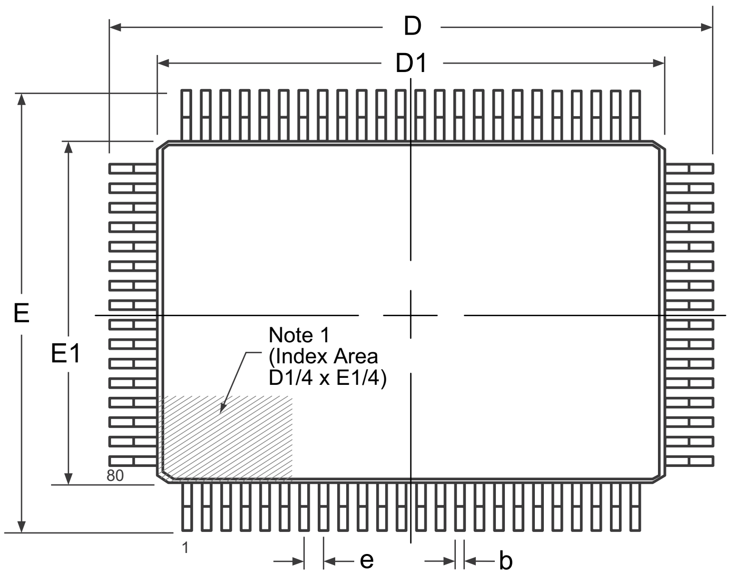
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	$HV_{OUT}24$	21	$HV_{OUT}4$	41	$HV_{OUT}64$	61	$HV_{OUT}44$
2	$HV_{OUT}23$	22	$HV_{OUT}3$	42	$HV_{OUT}63$	62	$HV_{OUT}43$
3	$HV_{OUT}22$	23	$HV_{OUT}2$	43	$HV_{OUT}62$	63	$HV_{OUT}42$
4	$HV_{OUT}21$	24	$HV_{OUT}1$	44	$HV_{OUT}61$	64	$HV_{OUT}41$
5	$HV_{OUT}20$	25	$D_{I/O}1A$	45	$HV_{OUT}60$	65	$HV_{OUT}40$
6	$HV_{OUT}19$	26	$D_{I/O}2A$	46	$HV_{OUT}59$	66	$HV_{OUT}39$
7	$HV_{OUT}18$	27	NC	47	$HV_{OUT}58$	67	$HV_{OUT}38$
8	$HV_{OUT}17$	28	NC	48	$HV_{OUT}57$	68	$HV_{OUT}37$
9	$HV_{OUT}16$	29	$\overline{LE}$	49	$HV_{OUT}56$	69	$HV_{OUT}36$
10	$HV_{OUT}15$	30	CLK	50	$HV_{OUT}55$	70	$HV_{OUT}35$
11	$HV_{OUT}14$	31	$\overline{BL}$	51	$HV_{OUT}54$	71	$HV_{OUT}34$
12	$HV_{OUT}13$	32	VSS	52	$HV_{OUT}53$	72	$HV_{OUT}33$
13	$HV_{OUT}12$	33	DIR	53	$HV_{OUT}52$	73	$HV_{OUT}32$
14	$HV_{OUT}11$	34	VDD	54	$HV_{OUT}51$	74	$HV_{OUT}31$
15	$HV_{OUT}10$	35	-IN	55	$HV_{OUT}50$	75	$HV_{OUT}30$
16	$HV_{OUT}9$	36	$D_{I/O}2B$	56	$HV_{OUT}49$	76	$HV_{OUT}29$
17	$HV_{OUT}8$	37	$D_{I/O}1B$	57	$HV_{OUT}48$	77	$HV_{OUT}28$
18	$HV_{OUT}7$	38	NC	58	$HV_{OUT}47$	78	$HV_{OUT}27$
19	$HV_{OUT}6$	39	+IN	59	$HV_{OUT}46$	79	$HV_{OUT}26$
20	$HV_{OUT}5$	40	VBP	60	$HV_{OUT}45$	80	$HV_{OUT}25$

Notes:

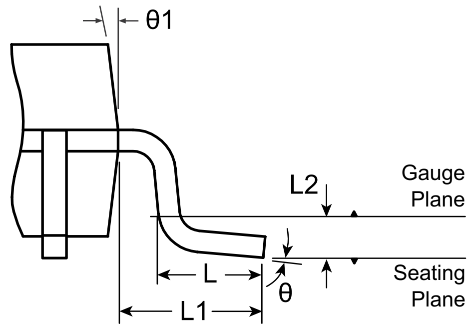
1. *Pin designation for DIR = VDD.*
2. *A 0.1µF capacitor is needed between VDD and VBP (pin 40) for better output current stability and to prevent transient cross-coupling between outputs. See Figures 1a and 1b.*

80-Lead PQFP Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



View B

Side View

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimen-sion (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept.1995.
** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-80PQFPPG, Version B101708.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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