

8-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs

Features

- ▶ HVCMOS® technology
- ▶ Operating output voltage of 250V
- ▶ Low power level shifting from 5.0 to 250V
- ▶ Shift register speed 8.0MHz @ $V_{DD} = 5.0V$
- ▶ 8 latch data outputs
- ▶ Output blanking
- ▶ Programmable POL latch
- ▶ CMOS compatible inputs

Applications

- ▶ Piezoelectric transducer driver
- ▶ Braille driver
- ▶ Weaving applications
- ▶ Printer drivers
- ▶ MEMs
- ▶ Displays

General Description

The HV514 is a low voltage serial to high voltage parallel converter with 8 high voltage push-pull outputs. This device has been designed to drive small capacitive loads such as piezoelectric transducers. It can also be used in any application requiring multiple high voltage outputs, medium current sourcing and sinking capabilities.

The device consists of an 8-bit shift register, dual 8-bit latches, and control logic to latch data, and control blanking of the outputs. Data is shifted through the shift register on the rising transition of the clock. A data output buffer is provided for cascading devices. Operation of the shift register is not affected by the \overline{LE} , \overline{SEL} , or the \overline{BL} inputs. Transfer of data from the shift register to the latch occurs when the \overline{LE} is high. Shift register data is shifted to the 8-bit Data Latch when \overline{SEL} is high; and shift register data is shifted to the 8-bit Polarity Latch when \overline{SEL} is low. The data is held in the output latches whenever \overline{LE} is low.

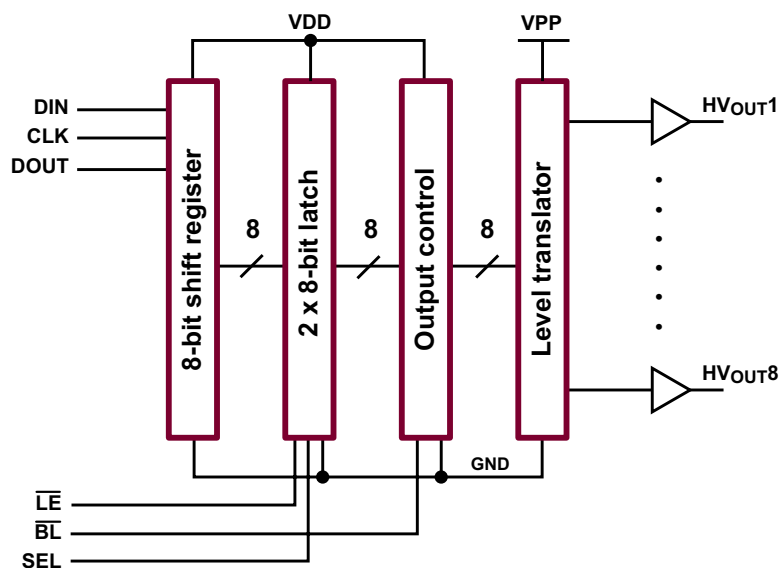
The high voltage output state is primarily dependent on the value in the polarity latch. If \overline{BL} is low, the output condition is the result of a 1 being exclusively-NOR'ed with the polarity latch value. If \overline{BL} is high, the output condition is the result of the data latch being exclusively-NOR'ed with the polarity latch.

All outputs with have a break-before-make circuitry to reduce cross-over current during output state changes.

Note:

1. \overline{LE} , \overline{SEL} , and \overline{BL} have internal 20k Ω pull-up resistors.

Block Diagram



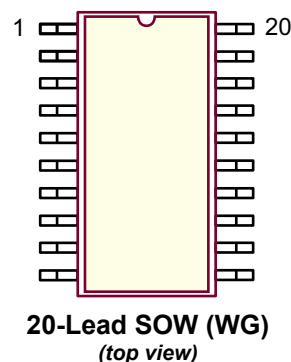
Ordering Information

| Device | Package Option |
|--------|---|
| | 20-Lead SOW 12.80x7.50mm body 2.65mm height (max) 1.27 pitch |
| HV514 | HV514WG-G |

-G indicates package is RoHS compliant ('Green')



Pin Configuration

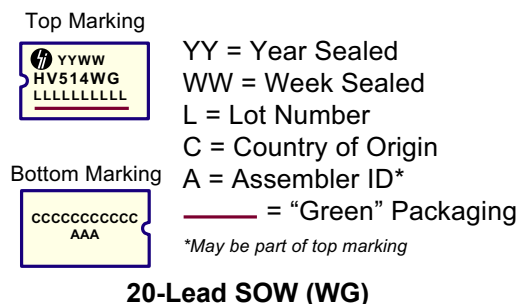


Absolute Maximum Ratings

| Parameter | Value |
|------------------------------------|--------------------------|
| Supply voltage, V_{DD} | -0.5V to 6.0V |
| Supply voltage, V_{PP} | 275V |
| Logic input levels | -0.5V to $V_{DD} + 0.5V$ |
| Ground current | 0.3A |
| High voltage supply current | 0.25A |
| Continuous total power dissipation | 750mW |
| Operating junction temperature | -40°C to +85°C |
| Storage temperature range | -65°C to +150°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking



Typical Operating Conditions

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--------------------------------|----------------|-----|----------|-------|------------|
| V_{DD} | Logic supply voltage | 4.5 | 5.0 | 5.5 | V | --- |
| V_{PP} | High voltage supply | 50 | - | 250 | V | Note 1 |
| V_{IH} | High-level input voltage | $V_{DD} - 0.9$ | - | V_{DD} | V | --- |
| V_{IL} | Low-level input voltage | 0 | - | 0.9 | V | --- |
| T_J | Operating junction temperature | -40 | - | +85 | °C | --- |

Notes:

- Below minimum V_{PP} the output may not switch.
- Power-up sequence should be the following:
 - Connect ground
 - Apply V_{DD}
 - Set all inputs (Data, CLK, Enable, etc.) to a known state
 - Apply V_{PP}

Power-down sequence should be the reverse of the above

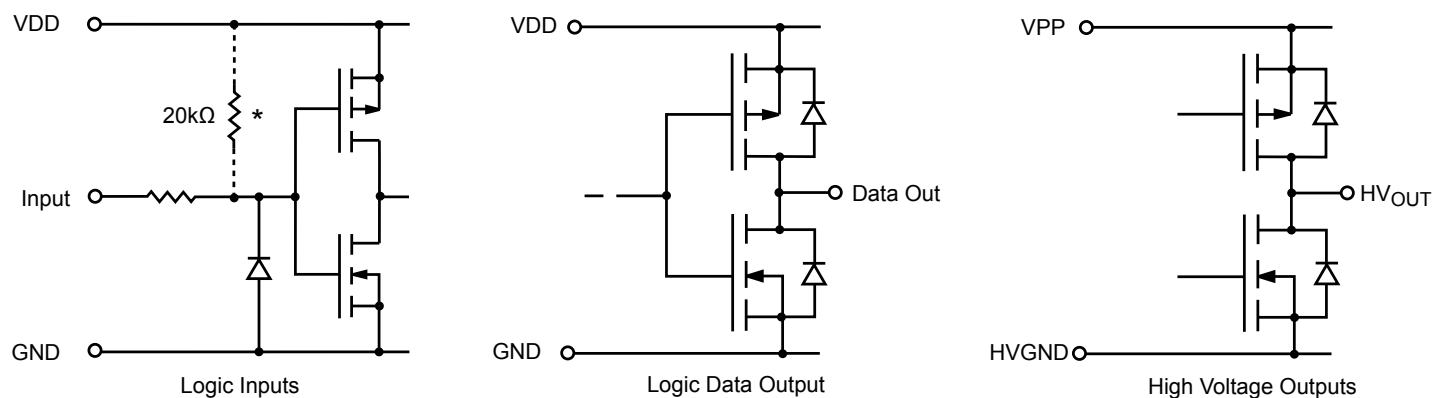
DC Electrical Characteristics (Over typical operating conditions unless otherwise specified, $T_J = 25^\circ\text{C}$)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|-----------------------------------|-------------------|------------------------|------|---------------|---|
| I_{DD} | V_{DD} supply current | - | - | 4.0 | mA | $f_{CLK} = 8.0\text{MHz}$, $\overline{LE} = \text{Low}$ |
| I_{DDQ} | Quiescent V_{DD} supply current | - | - | 0.1 | mA | All $V_{IN} = V_{DD}$ |
| | | - | - | 2.0 | | All $V_{IN} = 0\text{V}$ |
| I_{PP} | V_{PP} supply current | - | - | 100 | μA | $V_{PP} = 250\text{V}$, $f_{OUT} = 300\text{Hz}$, no load |
| I_{PPQ} | Quiescent V_{PP} supply current | - | - | 100 | μA | $V_{PP} = 240\text{V}$, outputs are static |
| I_{IH} | High-level logic input current | - | - | 10 | μA | $V_{IH} = V_{DD}$ |
| I_{IL} | Low-level logic input current | - | - | -10 | μA | $V_{IL} = 0\text{V}$ |
| | | - | - | -350 | | $V_{IL} = 0\text{V}$ for inputs w/pull-up resistors |
| I_{DPP} | Dynamic I_{PP} | - | - | 0.1 | mA | $f_{OUT} = 100\text{kHz}$, no load |
| V_{OH} | High level output | HV _{OUT} | 140 | - | V | $V_{PP} = 200\text{V}$, $I_{HVOUT} = -20\text{mA}$ |
| | | Data out | $V_{DD} - 1.0\text{V}$ | - | | $I_{DOUT} = -0.1\text{mA}$ |
| V_{OL} | Low level output | HV _{OUT} | - | - | V | $V_{DD} = 4.5\text{V}$, $I_{HVOUT} = 20\text{mA}$ |
| | | Data out | - | - | | $I_{DOUT} = 0.1\text{mA}$ |

AC Electrical Characteristics (Over typical operating conditions unless otherwise specified, $T_J = 25^\circ\text{C}$)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------------------|--|-----|-----|------|---------------|---|
| f_{CLK} | Clock frequency | 0 | - | 8.0 | MHz | --- |
| f_{OUT} | Output switching frequency (SOA limited) | - | 300 | - | Hz | $C_L = 50\text{nF}$, $V_{PP} = 200\text{V}$ |
| t_W | Clock width high and low | 62 | - | - | ns | --- |
| t_{SU} | Data setup time before clock rises | 15 | - | - | ns | --- |
| t_H | Data hold time after clock rises | 30 | - | - | ns | --- |
| t_{WLE} | Width of latch enable pulse | 80 | - | - | ns | --- |
| t_{DLE} | \overline{LE} delay time after rising edge of clock | 35 | - | - | ns | --- |
| t_{SLE} | \overline{LE} setup time before rising edge of clock | 40 | - | - | ns | --- |
| t_{OR}, t_{OF} | HV _{OUT} rise/fall time | - | - | 1000 | μs | $C_L = 100\text{nF}$, $V_{PP} = 200\text{V}$ |
| $t_{d\text{ ON/OFF}}$ | Delay time for output to start rise/fall | - | - | 500 | ns | --- |
| t_{DHL} | Delay time clock to D _{OUT} high to low | - | - | 110 | ns | $C_L = 15\text{pF}$ |
| t_{DLH} | Delay time clock to D _{OUT} low to high | - | - | 110 | ns | $C_L = 15\text{pF}$ |
| t_R, t_F | All logic inputs | - | - | 5.0 | ns | --- |

Input and Output Equivalent Circuits

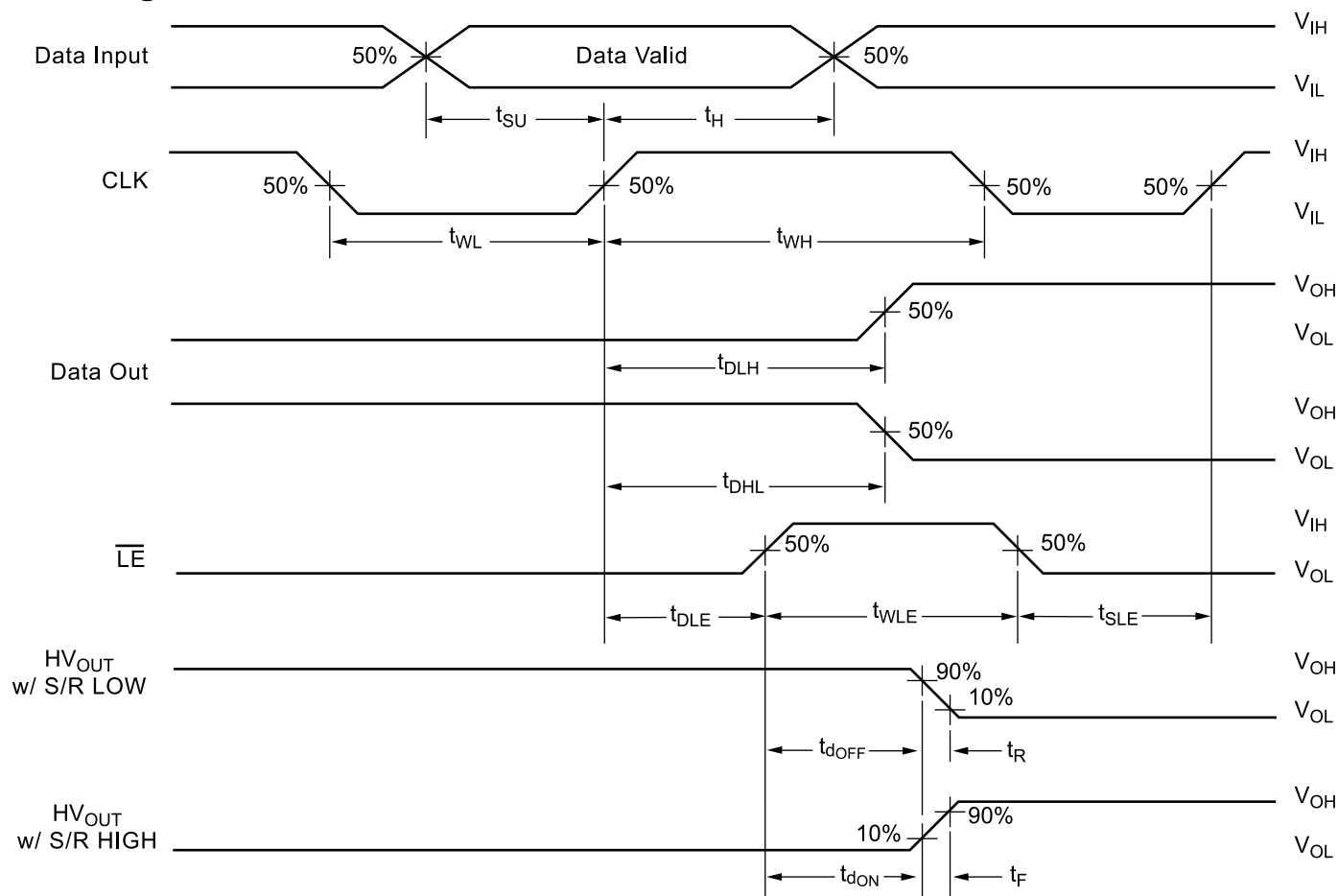


Notes:

There is an internal output resistor for the high voltage output pin for SOA protection.

* \overline{LE} , \overline{SEL} , \overline{SL}

Switching Waveforms



Note:

\overline{LE} , \overline{SEL} , and \overline{BL} have internal $20k\Omega$ pull-up resistors.

Function Table

| Function | Inputs | | | | | Outputs | | | |
|-----------------------|--------|-----|-----------------|-----|-----------------|----------------------|-------------|--------------------------------|-------------|
| | Data | CLK | \overline{LE} | SEL | \overline{BL} | Shift Reg 1 2...8 | Latch | HV Output Action 1 2...8 | Data Out |
| Load S/R | H OR L | - | - | - | - | H or L •...• | • •...• | • •...• | • |
| Transfer S/R to latch | X | X | H | H | - | H or L •...• | To data | • •...• | • |
| Invert mode | X | X | H | L | - | H or L •...• | To polarity | • •...• | • |
| Hold latch data | X | X | L | - | - | • •...• | • •...• | • •...• | • |
| Blank output | X | X | X | X | L | • •...• | • •...• | 1 (XNOR) POL | • |
| Active output | X | X | X | X | H | • •...• | • •...• | Data (XNOR) POL | • |

Notes:

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition

• = dependent on previous stage's state before the last CLK or last \overline{LE} high.

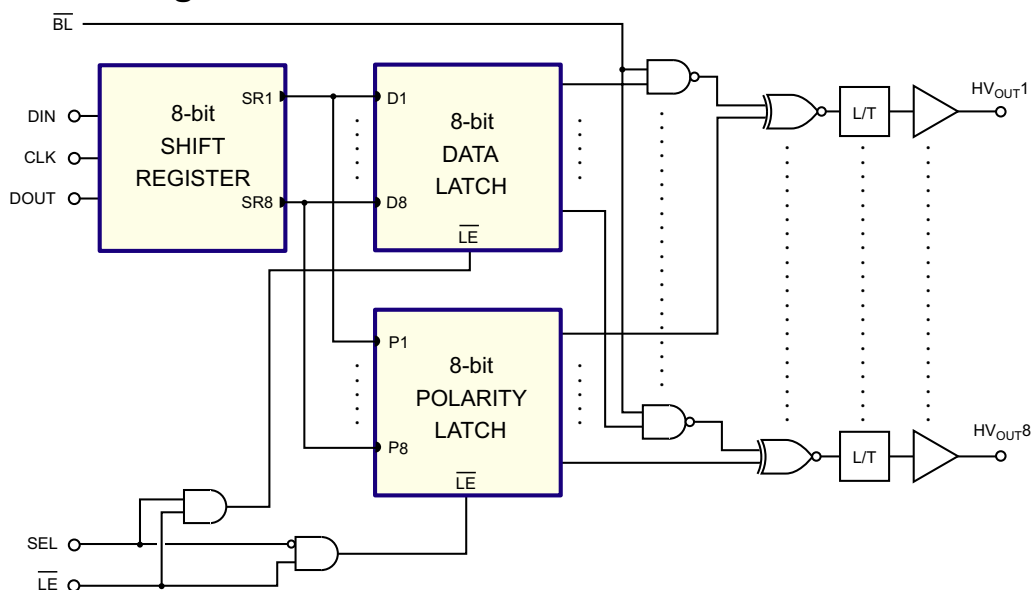
Blanking Function Table

| \overline{BL} | Latched Information | | HV Output |
|-----------------|---------------------|------------------|-----------|
| | Data | \overline{POL} | |
| L | X | L | L |
| L | X | H | H |
| H | L | L | L |
| H | H | L | H |
| H | L | H | L |
| H | H | H | H |

Note:

H = high level, L = low level

Functional Block Diagram



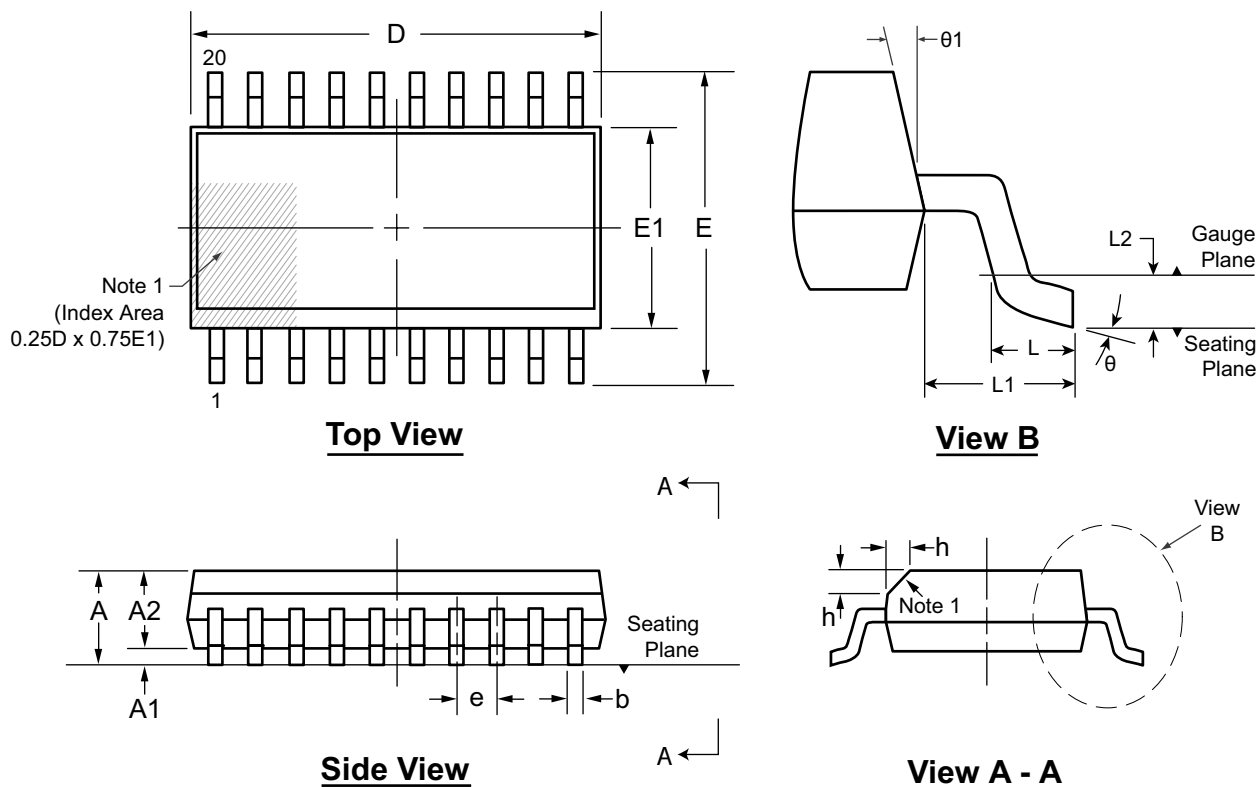
Note:
 \overline{BL} , \overline{LE} , and SEL have internal 20k Ω pull-up resistors.

Pin Description

| Pin # | Function | Description |
|-------|--------------------|---|
| 1 | CLK | Clock pin, shift registers shifts data on rising edge of input clock. |
| 2 | \overline{LE} | Latch enable bar input logic. |
| 3 | DIN | Data input. |
| 4 | LGND | Low voltage ground. |
| 5 | HVGND | High voltage ground. |
| 6 | | |
| 7 | HV _{OUT1} | High voltage push-pull output. |
| 8 | HV _{OUT2} | High voltage push-pull output. |
| 9 | HV _{OUT3} | High voltage push-pull output. |
| 10 | HV _{OUT4} | High voltage push-pull output. |
| 11 | HV _{OUT5} | High voltage push-pull output. |
| 12 | HV _{OUT6} | High voltage push-pull output. |
| 13 | HV _{OUT7} | High voltage push-pull output. |
| 14 | HV _{OUT8} | High voltage push-pull output. |
| 15 | VPP | High voltage power supply pin. |
| 16 | | |
| 17 | VDD | Logic supply voltage. |
| 18 | DOUT | Data output. |
| 19 | \overline{BL} | Blanking pin, logic input LOW sets all HV _{OUTS} low. See truth table. |
| 20 | SEL | Data select. |

20-Lead SOW (Wide Body) Package Outline (WG)

12.80x7.50mm body, 2.65mm height (max), 1.27mm pitch



Note:

1. This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | θ1 |
|-------------------|-----|-------|------|-------|------|--------|--------|-------|-------------|------|------|-------------|-------------|----|-----|
| Dimension (mm) | MIN | 2.15* | 0.10 | 2.05 | 0.31 | 12.60* | 9.97* | 7.40* | 1.27 BSC | 0.25 | 0.40 | 1.40 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 12.80 | 10.30 | 7.50 | | - | - | | | - | - |
| | MAX | 2.65 | 0.30 | 2.55* | 0.51 | 13.00* | 10.63* | 7.60* | | 0.75 | 1.27 | | | 8° | 15° |

JEDEC Registration MS-013, Variation AC, Issue E, Sep. 2005.

* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings are not to scale.

Supertex Doc. #: DSPD-20SOWWG, Version C090408.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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