



N-Channel Depletion-Mode Vertical DMOS FET

Features

- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Normally-on switches
- ▶ Solid state relays
- ▶ Converters
- ▶ Linear amplifiers
- ▶ Constant current sources
- ▶ Power supply circuits
- ▶ Telecom

General Description

These depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options		BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (max) (Ω)	I_{DSS} (min) (mA)
	TO-92	TO-243AA (SOT-89)			
DN3545	DN3545N3-G	DN3545N8-G	450	20	200

-G indicates package is RoHS compliant ("Green")



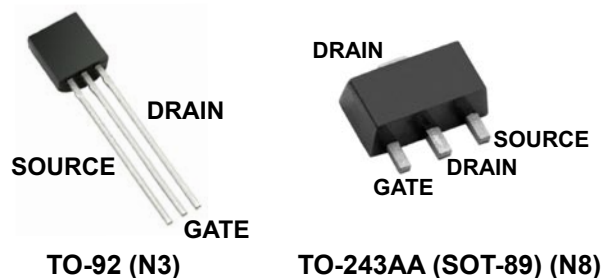
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSX}
Drain-to-gate voltage	BV_{DGX}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

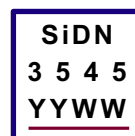
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configurations



Product Marking



YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)



W = Code for week sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-243AA (SOT-89) (N8)

Thermal Characteristics

Package	I_D (continuous) [†] (mA)	I_D (pulsed) (mA)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C/W}$)	θ_{ja} ($^\circ\text{C/W}$)	$I_{DR}^{\dagger}$ (mA)	I_{DRM} (mA)
T0-92	136	1600	0.74	125	170	136	1600
TO-243AA	200	300	1.6 [‡]	15	78 [‡]	200	300

Notes:

[†] I_D (continuous) is limited by max rated T_j .

[‡] Mounted on FR4 board, 25mm x 25mm x 1.57mm.

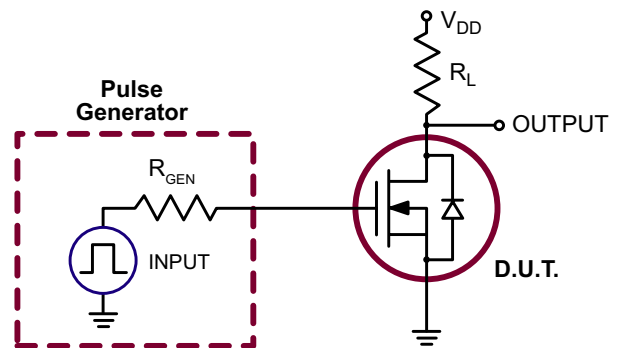
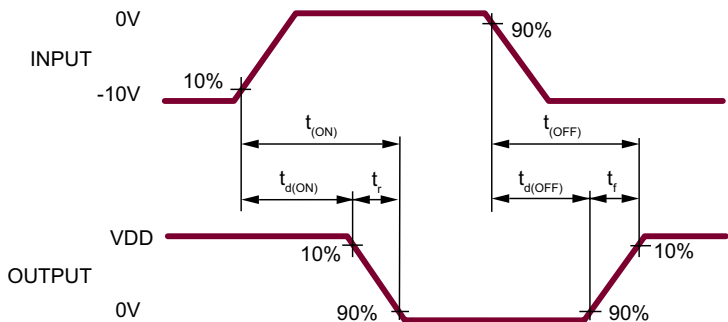
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSX}	Drain-to-source breakdown voltage	450	-	-	V	$V_{GS} = -5.0\text{V}$, $I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	-	-3.5	V	$V_{DS} = 25\text{V}$, $I_D = 10\mu\text{A}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	-4.5	mV/ $^\circ\text{C}$	$V_{DS} = 25\text{V}$, $I_D = 10\mu\text{A}$
I_{GSS}	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
$I_{D(OFF)}$	drain-to-source leakage current	-	-	1.0	μA	$V_{GS} = -5.0\text{V}$, $V_{DS} = \text{Max Rating}$
		-	-	1.0	mA	$V_{GS} = -5.0\text{V}$, $V_{DS} = 0.8\text{Max Rating}$ $T_A = 125^\circ\text{C}$
I_{DSS}	Saturated drain-to-source current	200	-	-	mA	$V_{GS} = 0\text{V}$, $V_{DS} = 15\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	20	Ω	$V_{GS} = 0\text{V}$, $I_D = 150\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/ $^\circ\text{C}$	$V_{GS} = 0\text{V}$, $I_D = 150\text{mA}$
G_{FS}	Forward transductance	150	-	-	mmho	$I_D = 100\text{mA}$, $V_{DS} = 10\text{V}$
C_{ISS}	Input capacitance	-	-	360	pF	$V_{GS} = -5.0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$
C_{OSS}	Common source output capacitance	-	-	40		
C_{RSS}	Reverse transfer capacitance	-	-	15		
$t_{d(ON)}$	Turn-on delay time	-	-	20	ns	$V_{DD} = 25\text{V}$, $I_D = 150\text{mA}$, $R_{GEN} = 25\Omega$, $V_{GS} = 0\text{V to } -10\text{V}$
t_r	Rise time	-	-	30		
$t_{d(OFF)}$	Turn-off delay time	-	-	30		
t_f	Fall time	-	-	40		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = -5.0\text{V}$, $I_{SD} = 150\text{mA}$
t_{rr}	Reverse recovery time	-	800	-	ns	$V_{GS} = -5.0\text{V}$, $I_{SD} = 150\text{mA}$

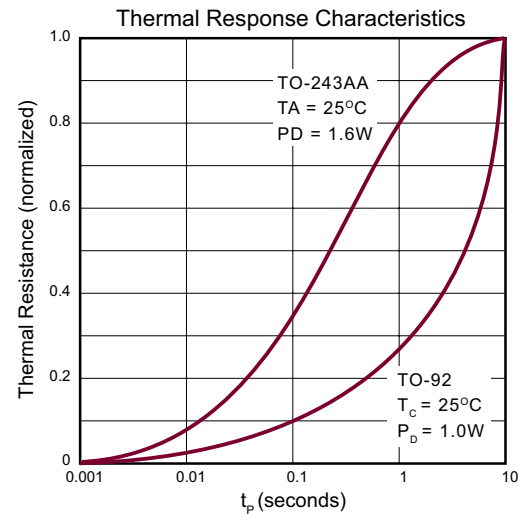
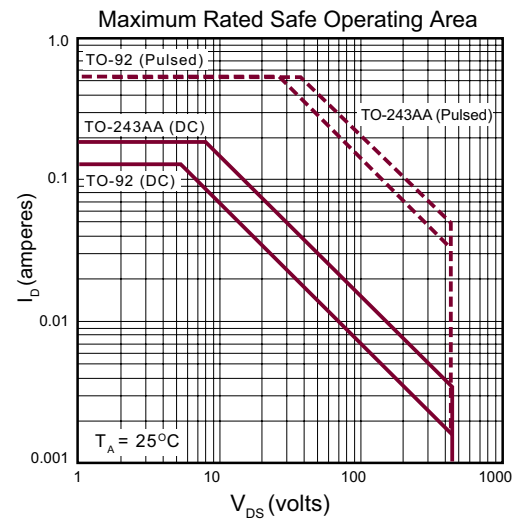
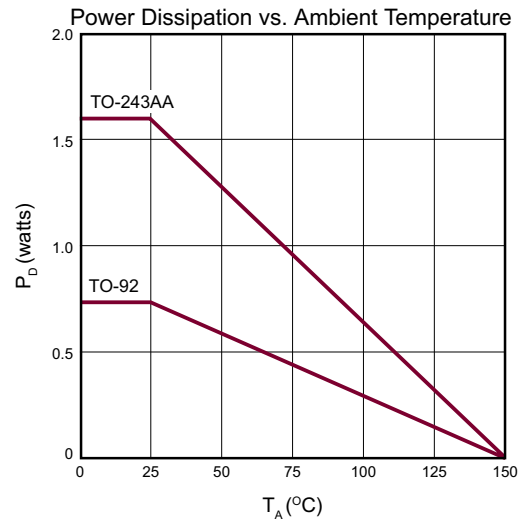
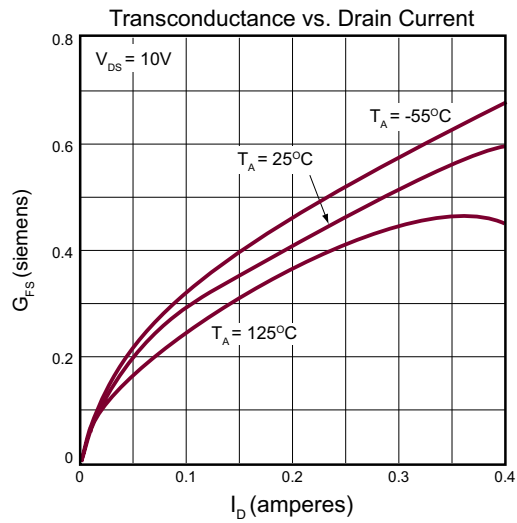
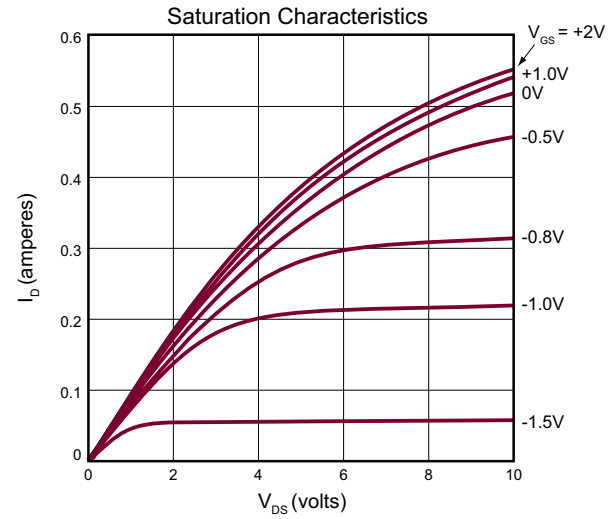
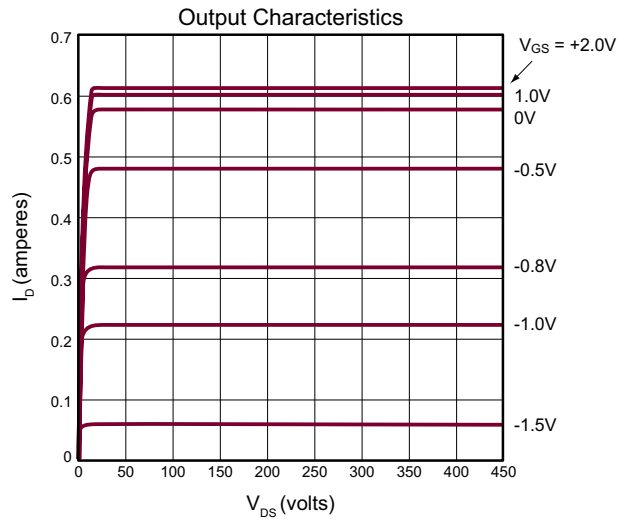
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

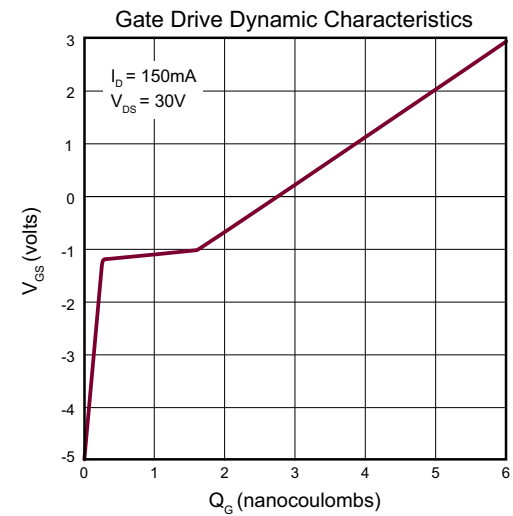
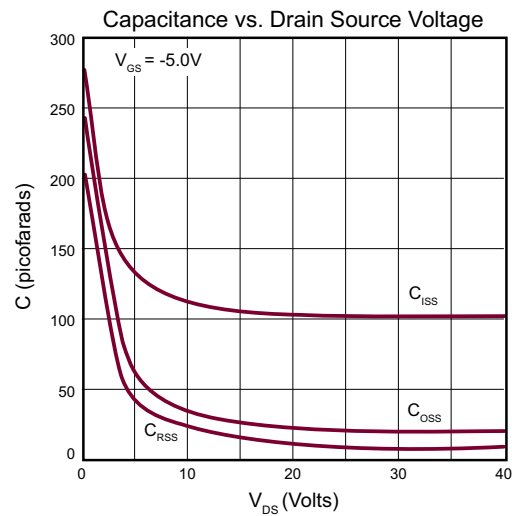
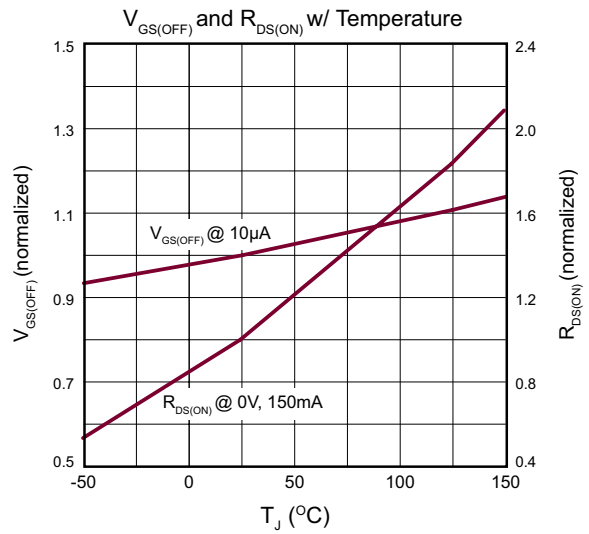
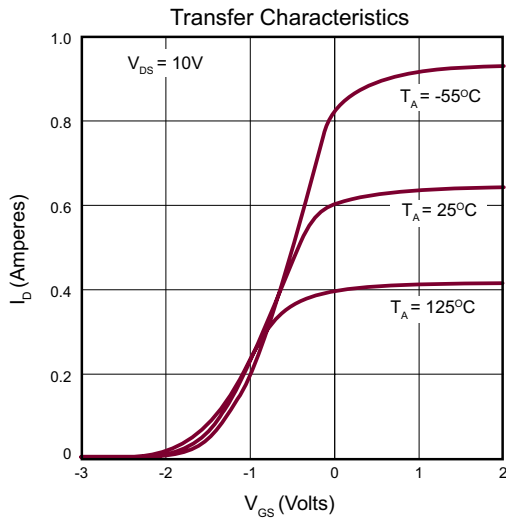
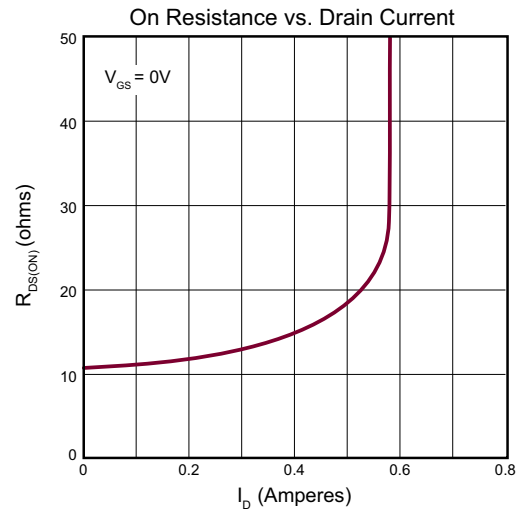
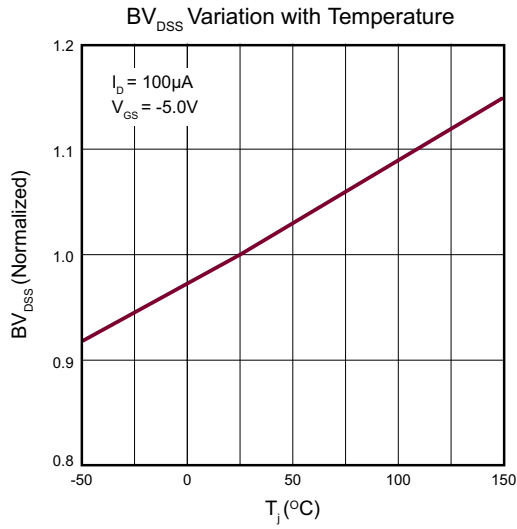
Switching Waveforms and Test Circuit



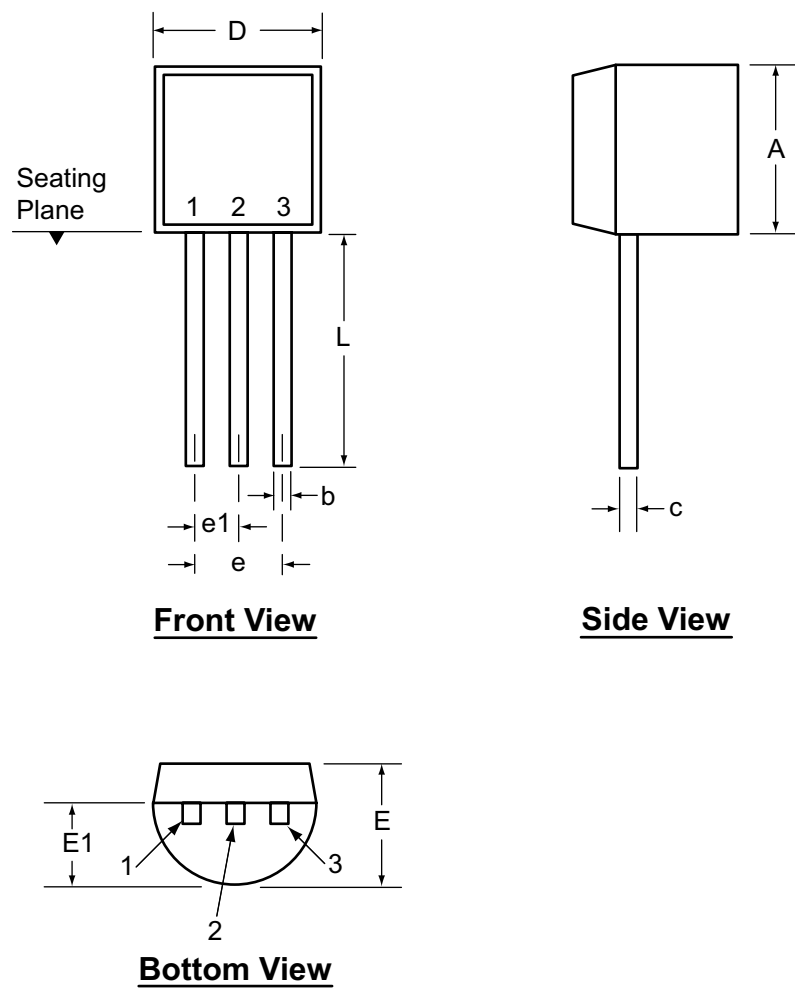
Typical Performance Curves



Typical Performance Curves (cont.)



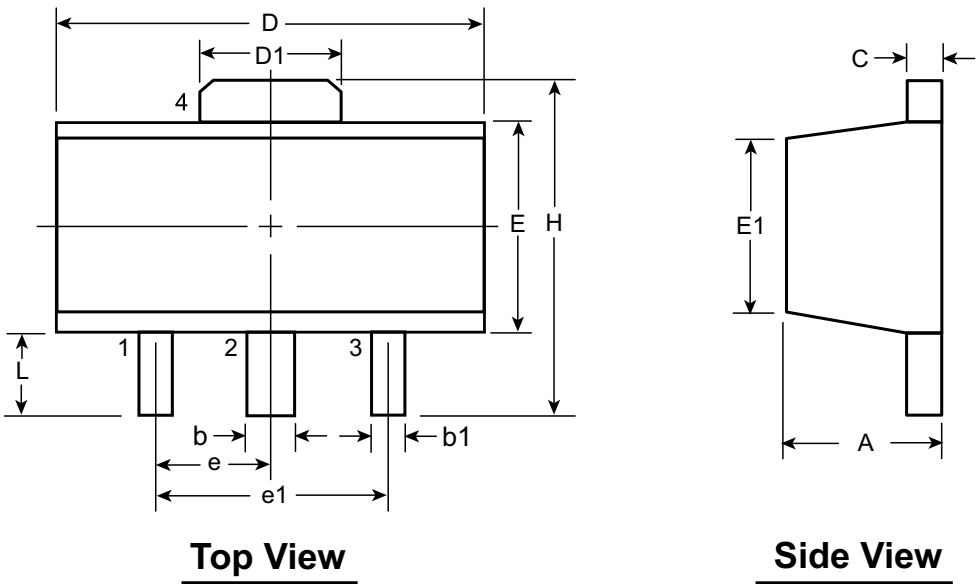
3-Lead TO-92 Package Outline (N3)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
* This dimension is not specified in the JEDEC drawing.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: DSPD-3TO92N3, Version E041009.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.89
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† This dimension differs from the JEDEC drawing
Drawings not to scale.
Supertex Doc. #: DSPD-3TO243AAN8, Version E051509.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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