

PM5369 TUPP 9953

Tributary Unit Payload Processor for 9953 Mbit/s

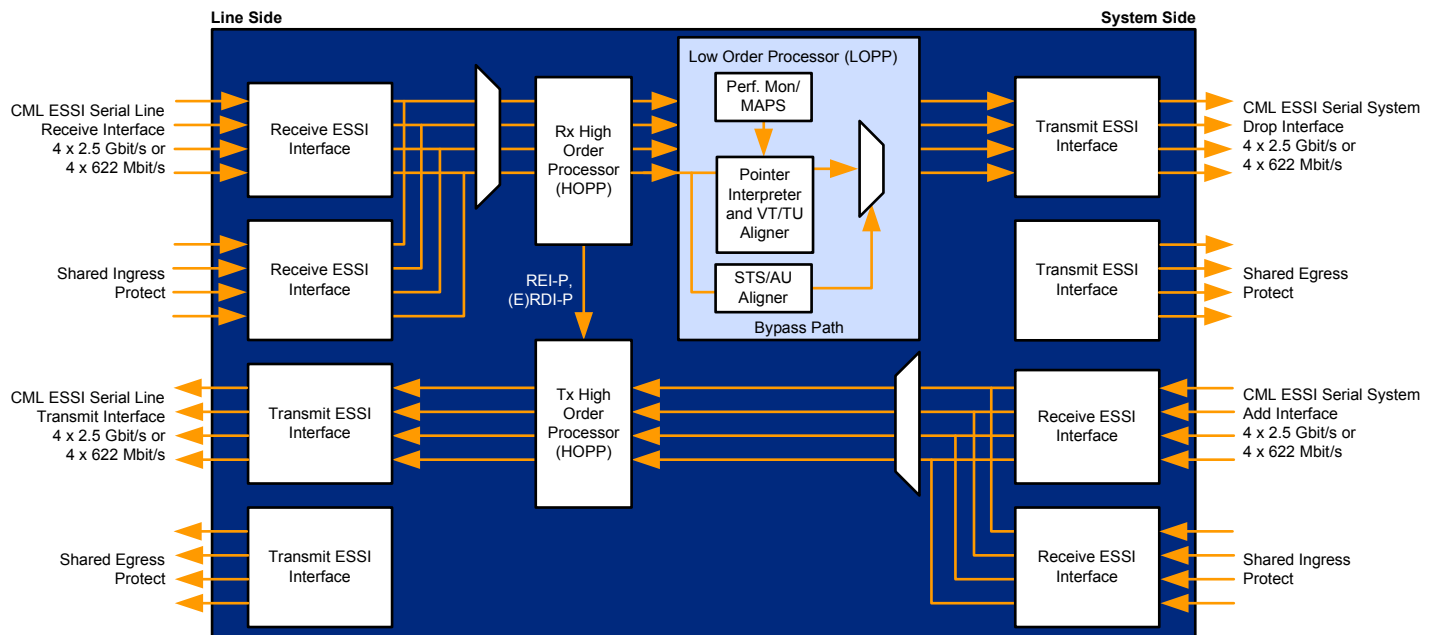
Released Product Brief



Product Highlights

- Configurable, multi-channel payload processor for aligning SONET virtual tributaries (VTs) or SDH tributary units (TUs) in an STS-192/STM-64 or STS-48/STM-16 data stream
- Supports High Order (STS/AU) pointer processing, payload processing, and path termination/monitoring
- Supports Low Order (VT/TU) pointer processing, payload processing, and path monitoring
- On the line side, provides working Serial Receive and Transmit ESSI (Extended SONET Serial Interface) CML links. Links are configurable as:
 - 4xSTS-48/STM-16 2488.32 Mbit/s SONET/SDH framed interfaces; or
 - 4xSTS-12/STM-4 622.08 Mbit/s SONET/SDH framed interfaces
- On the system side, provides working Add and Drop Serial ESSI links. Links are configurable as:
 - 4xSTS-48/STM-16 2488.32 Mbit/s SONET/SDH framed interfaces; or
 - 4xSTS-12/STM-4 622.08 Mbit/s SONET/SDH framed interfaces
- Independently configurable (2488.32 Mbit/s or 622.08 Mbit/s) Line and System Interfaces
- Provides a set of Ingress and Egress shared protection links
- Provides a per-link Space switch on egress interfaces
- Provides a steady-state latency of:
 - 21 ns from line Receive to system DROP for VT.1.5
 - 2.5 ns from system ADD to line TX
- Provides hardware based Message Assisted Protection Switching (MAPS) support to work with a centralized fabric (e.g., PM5370 WSE 40)
- Supports independent Line Receive and System Drop transport frame alignment for high-order traffic
- Supports independent transport, high-order payload and tributary multi-frame alignments for low-order traffic
- Supports independent Line Transmit and System Add transport frame alignments
- On the receive path, provides optional SDH payload conversion of:
 - AU4/VC4/TUG3/TU3/VC3/C3 to AU3/VC3/C3; or
 - AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3; or
 - AU4/VC4/TUG3/TUG2 to AU3/VC3/TUG2; or
 - AU3/VC3/TUG2 to AU4/VC4/TUG3/TUG2
- On the transmit path, provides optional SDH payload conversion of:
 - AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3; or
 - AU4/VC4/TUG3/TUG2 to AU3/VC3/TUG2; or
 - AU3/VC3/TUG2 to AU4/VC4/TUG3/TUG2
- Allows for low order (VT/TU) processing bypass
- Supports high-order ESSI transport overhead transparency
- Supports line and system diagnostic and facility loopbacks
- Provides optional PRBS generation and monitoring features for ESSI offline link verification
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring
- Provides a standard 5-signal IEEE 1149.1 JTAG test port for boundary scan test purposes

Block Diagram



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