PM8357

QuadPHY® XR

4 X 1.2-3.2 Gbit/s Quad, Full Duplex, XAUI Re-timer, 10 Gigabit Ethernet & Fibre Channel Device

Data Sheet

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Contacting PMC-Sierra

PMC-Sierra
100-2700 Production Way
Burnaby, BC Canada V5A 4X1

Tel: +1 (604) 415-6000
Fax: +1 (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

Revision History

Issue No.	Issue Date	Details of Change
1	January 2003	Advance Release
2	March 2003	Advance Release 2
3	January 2004	Preliminary Release
4	April 2004	Production Release
5	November 2005	Updated ordering information including RoHS-compliant device details.

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1 Definitions

The following table defines terms and abbreviations used in this document.

Table 1 Definitions

ANSI	American National Standards Institute
ASSP	Application Specific Standard Product
BER	Bit Error Rate
BIST	Built In Self Test
Channel	A group of 4 Lanes carrying 10GE or 10GFC 8b/10b encoded data.
CMOS	Complementary Metal Oxide Semiconductor
CRU	Clock Recovery Unit
DCRU	Data Clock and Recovery Unit
DTE	Data Termination Equipment
ESD	Electrostatic Discharge
FC-HSPI	Fibre Channel – High Speed Parallel Interface
FIFO	First-In First-Out
HSTL	High Speed Transceiver Logic – 1.5 V
IEEE	Institute of Electrical and Electronics Engineers
IPG	Inter-Packet Gap
JTAG	Joint Test Action Group
Lane	single 1.2Gbit/s to 3.2 Gbit/s CML differential pair or a single 8 or 10 bit internal data path in either RX or TX direction.
LVDS	Low Voltage Differential Signaling
MDIO	Management Data Input/Output
MMD	MDIO Manageable Device
NC	No Connect, indicates an unused pin
NCITS	American National Standard of Accredited Standards Committee.
PCS	Physical Coding Sublayer
PECL	Pseudo Emitter Coupled Logic
PHY	Physical Layer
PISO	Parallel-in-Serial-Out
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
Port	A pair of Channels forming a full duplex data stream.
PRBS	Pseudo-Random Binary Sequence
RDI	Remote Defect Indication
REFX	Receive 10G Ethernet/Fibre Channel Telecom System Block
SAW	Surface Acoustic Wave
SD	Signal Detect
SERDES	Serializer/De-Serializer

SIPO	Serial-in-Parallel-Out
TEFX	Transmit 10G Ethernet/Fibre Channel Telecom System Block
VCSO	Voltage Controlled SAW Oscillator
WAN	Wide Area Network
XAUI	10Gb Attachment Unit Interface
XGMII	10Gb Media Independent Interface
XGXS	XGMII Extender Sublayer

2 Features

2.1 General Features

- IEEE 802.3ae compliant fully redundant, full duplex, XAUI Re-timer, 10 Gigabit Ethernet (10GbE) device
- T11 NCITS 1413-D Rev 3.2 compliant fully redundant, full duplex, XAUI to XAUI, 10 Gigabit Fibre Channel (10GFC) device.
- Integrated serializer/de-serializer, clock recovery, clock synthesis, byte alignment, trunking, and 8B/10B encode/decode logic.
- Supports completely non-blocking cross-connect to enable flexible configuration in parallel loopback, XAUI re-timer or XAUI cross connect.
- Complete 8 lane x 10bit, non-blocking Cross-Connect with any lane to any lane switching capability enabling simpler board layouts. The device implements a smart switchover mechanism allowing connections to be changed during IPG and minimize packet fragmentation.
- Implements the PHY-XS constituent of the XGMII Extender Sublayer (XGXS) and the PMA/PMD and PCS MDIO Manageable Devices (MMDs) as defined in IEEE 802.3ae for 10GBASE-X family of physical layer implementations .
- Contains a per-link 16 byte receive FIFO that supports clock rate difference compensation to ± 100 ppm and performs lane-to-lane de-skew/alignment across the four lanes of a 10GbE or 10GFC data stream.
- Supports differential AC coupled PECL level *REFCLK*+/- at 60.00 MHz to 160 MHz for 1.2 Gbit/s to 3.2 Gbit/s operations respectively.
- Supports independent lane based operation each running at 1.2 Gbit/s to 3.2 Gbit/s Gbit/s with 8B/10B encoded data and 2.48832 Gbit/s for per-SERDES scrambled NRZ 8 bit data.
- Electrostatic Discharge tested to meet 2KV HBM and 500V CDM

2.2 High Speed Interface Features

- Allows full control and monitoring under the Management Interface of the high-speed ports.
- High-speed outputs with programmable pre-emphasis to counteract dielectric losses and allow maximum reach on printed circuit boards.
- High-speed inputs with programmable equalization to reduce Inter Symbol Interference (ISI) providing robust BER performance.
- Internal 100 ohms differential termination on transmit and receive high-speed signals for optimal signal integrity.

2.3 Test and Control Features

- Supports pin programmable configuration with software override. Needs no microprocessor interface for normal mode of operation.

- Supports a optional 2-pin serial management interface using IEEE 802.3ae Clause 45 MDC/MDIO management control for configuration and diagnostic access.
- Supports built in self-test (BIST) via internal packet generation and checking.
- Supports Metallic Line Loopback, Parallel Line Loopback, Serial Loopback, Parallel Diagnostic Loopback, Recovery Clock Loopback and System Loopback modes for each link/lane for rich debugging capability. Further control over data flow is also available on a per-lane basis.
- Internal CRPAT and CJPAT Packet generator as per IEEE 802.3ae for 10GbE and ANSI T11 NCITS working group for 10GFC.
- Provides automatic packet generation (PRBS 7, PRBS 23, Fixed pattern, Counting pattern) with selective self checking capabilities. All patterns can be framed or unframed, trunked or per-lane, and 8 or 10 bits.
- Supports packet monitoring by providing the total number of packets received and the number of errored packets received.
- Allows bit swizzle and invert of input/output serial data on per-lane basis across the Port A and Port B.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board purpose.

2.4 Physical

- Low power operation with power saving modes to disable unused channels and unused features.
- Power under maximum use configuration with 2 XAUI links is 1.6 Watts typical case.
- Power with only the single XAUI link active with loaded outputs yields only 1 Watt typical case.
- Implemented in 0.13 µm CMOS technology.
- Small footprint 15x15 mm, 196-pin BGA package with 1 mm ball pitch.

3 Applications

- 10 Gbits/s full duplex Ethernet or Fibre Channel XAUI retimers.
- 10 Gbits/s full duplex XAUI transponders.
- High-speed serial backplanes.
- Intra-system interconnects.
- 2.5 Gbits/s Infiniband transceivers.
- 2.125 Gbits/s Fibre Channel applications.
- 2.488 Gbit/s pure SERDES mode for NRZ data.
- 1.536 Gbit/s Open Base Station Architecture Initiative (OBSAI) standard.
- 1.2288 & 2.4576 Gbit/s Common Public Radio Interface (CPRI) standard.
- 1.485 Gbit/s SMPTE 292M HD-SDI for HDTV switch/routers.
- 1.25 Gbit/s, 2.5 Gbit/s and 3.125 Gbit/s Serial RapidIO transceivers.

4 References

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2. NCITS T11 project 1413-D Rev 3.5 Fibre Channel 10 Gigabit (10GFC).

3. IEEE 1149.1-1990 Standard Test Access Port and Boundary-Scan Architecture.

4. PMC-2010750, Signal Integrity for PMC-Sierra 3.125/2.488/1.25 Gbits/s Links Application Note.

5. PMC-2010793, High Frequency Simulation with HSPICE Application Note. PMC-Sierra.

6. Electronic Industries Association. *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*: EIA/JESD51. December 1995.

7. Electronic Industries Alliance 1999. *Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8*. October 1999.

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9. SEMI (Semiconductor Equipment and Materials International). SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages. 1988.

10. ITU-T G.958 “Digital line systems based on the synchronous digital hierarchy for use on optical fibre cables”, 1994.

11. PMC-2040363, Retimer Support for Serial RapidIO Applications, Issue 1, March 2004.

12. PMC-2030760, SERDES and Retimer Support for Infiniband Applications, Issue 1, February 2004.

5 Application Examples

The QuadPHY XR has numerous applications throughout data networking and storage applications.

Figure 1 QuadPHY XR in XENPAK 10GBASE-LX4 WWDM Optical Module

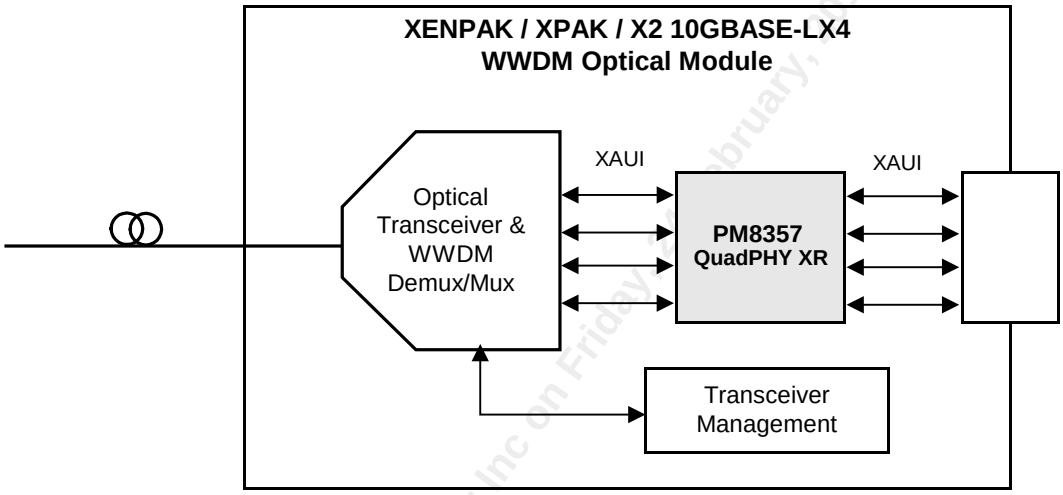


Figure 2 QuadPHY XR in 10 Gigabit Ethernet Line Card as a Backplane Extender

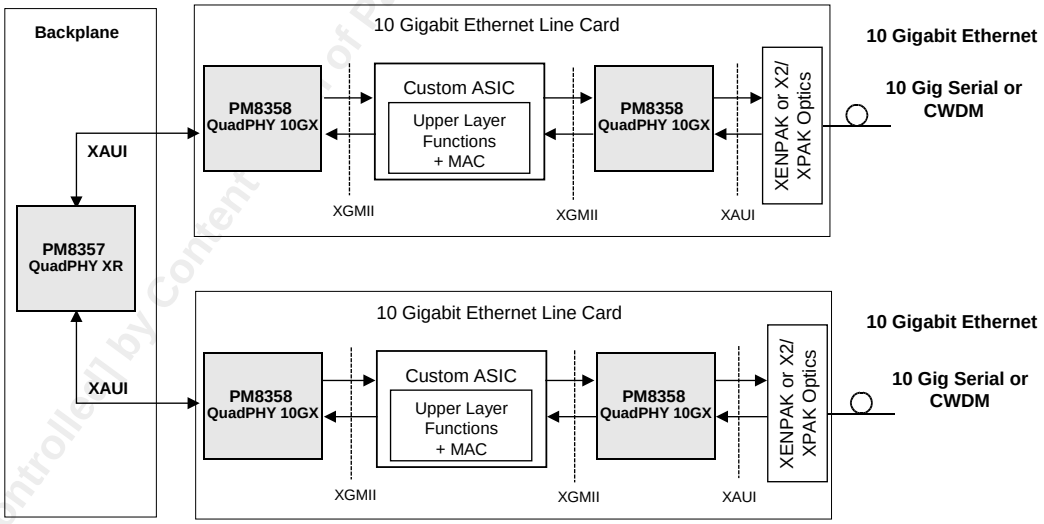
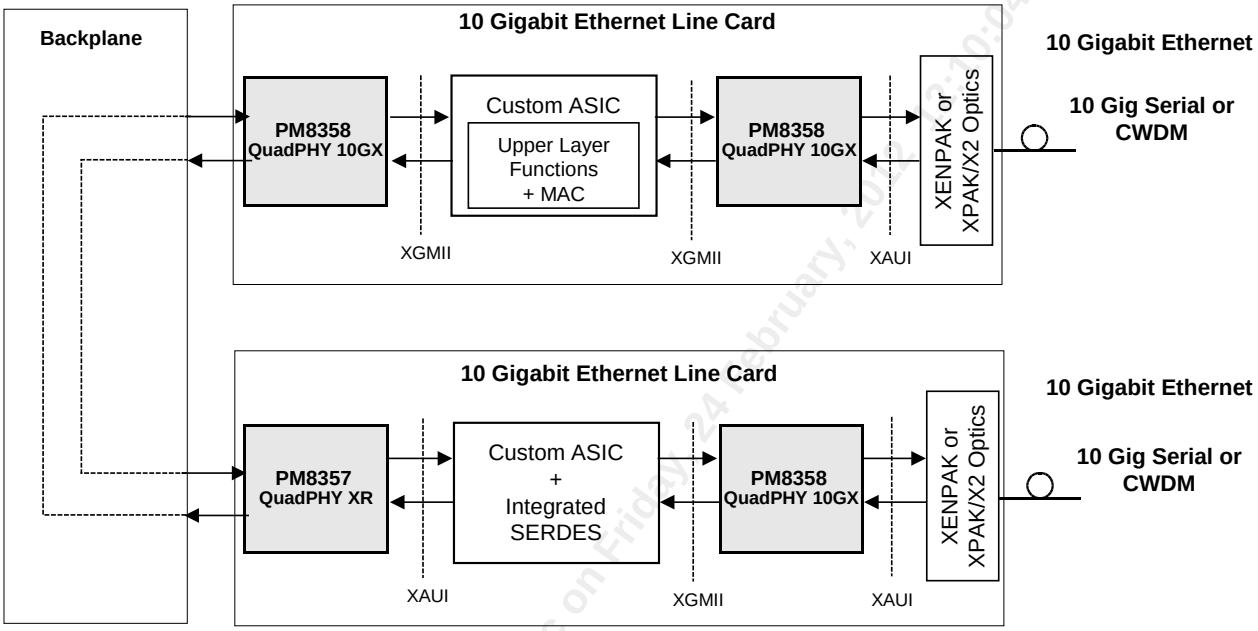


Figure 3 QuadPHY XR in 10 Gigabit Ethernet Line Card extending short-reach ASIC signals.



6 Block Diagram

Figure 4 Block Diagram

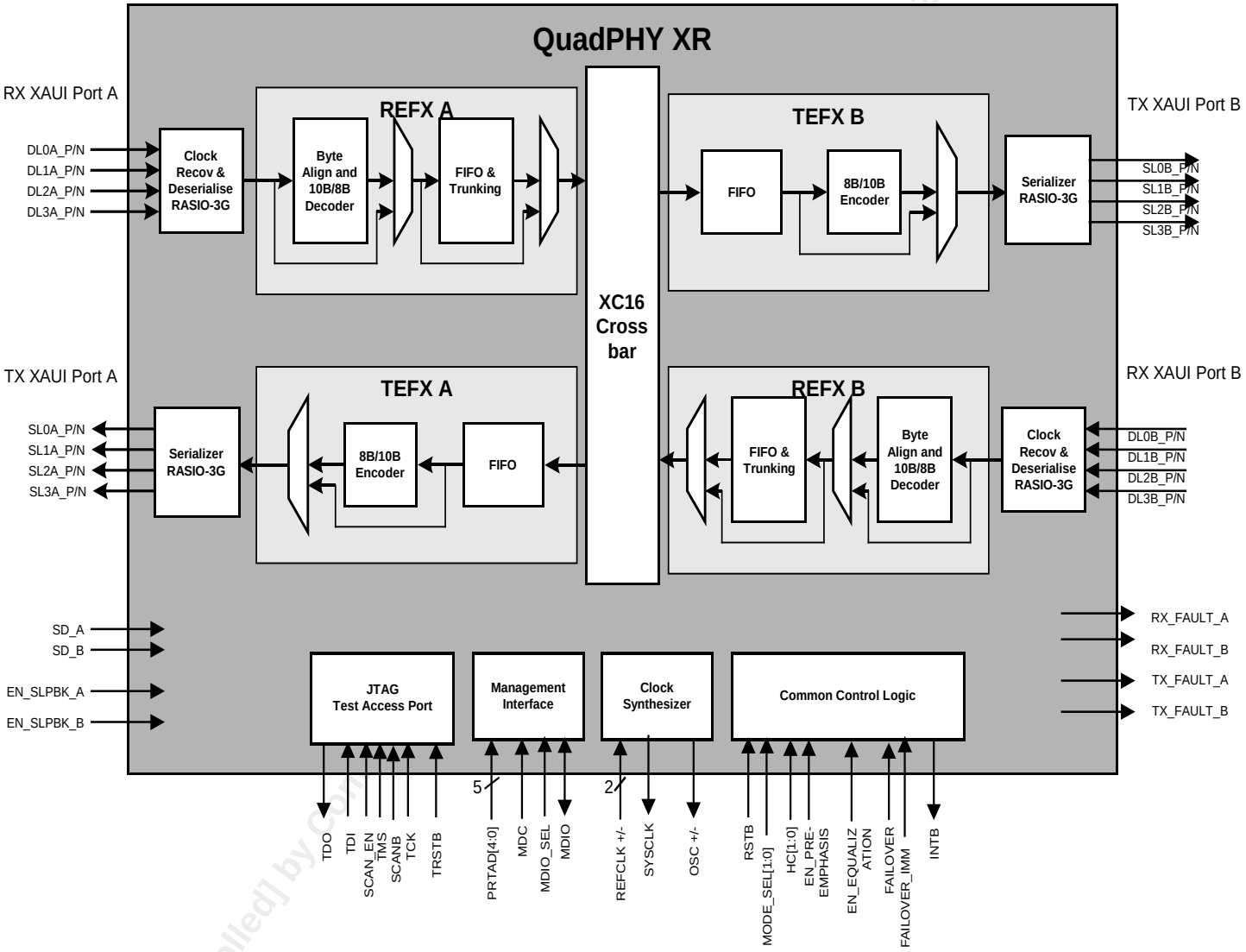


Figure 5 Block Diagram with Loopbacks

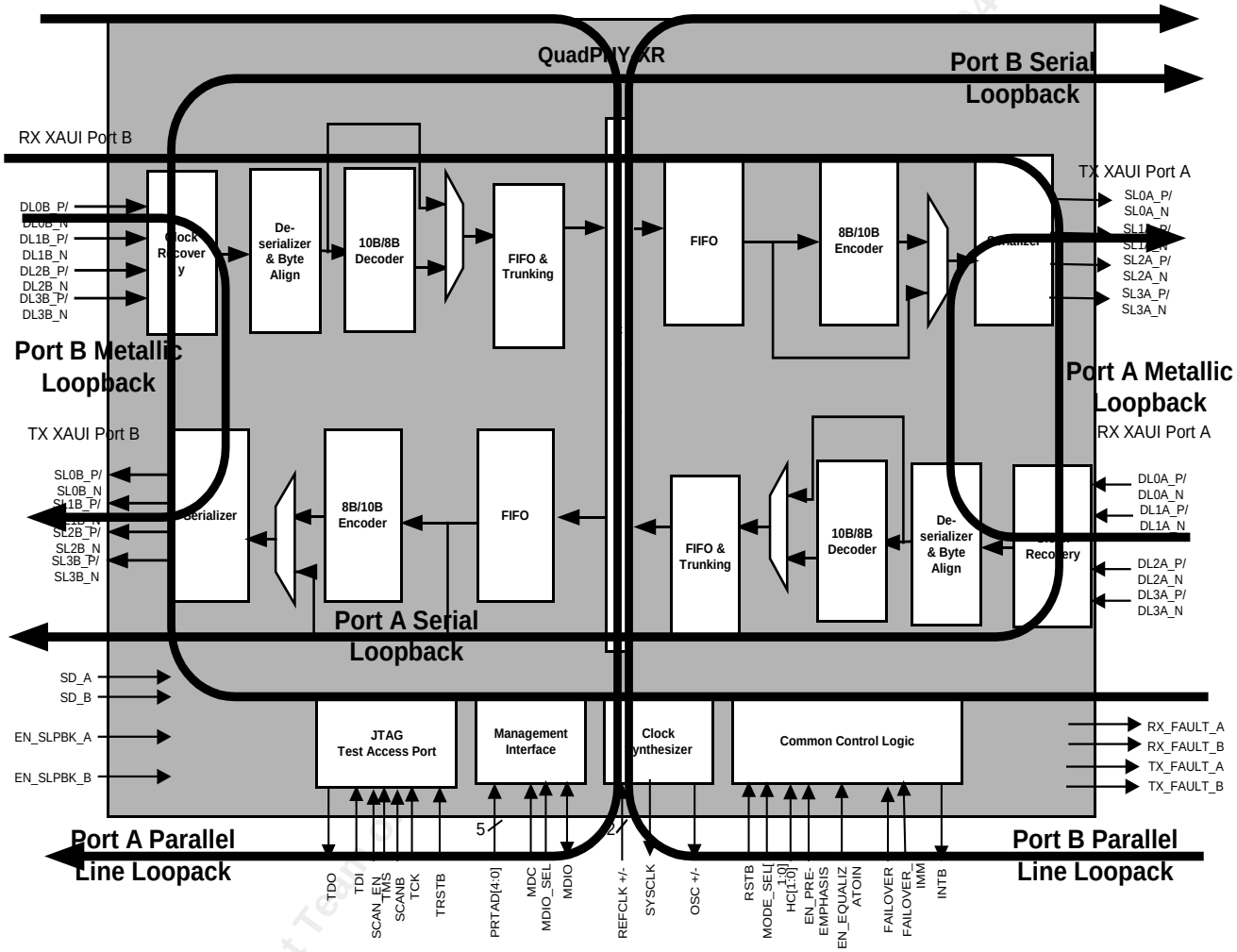
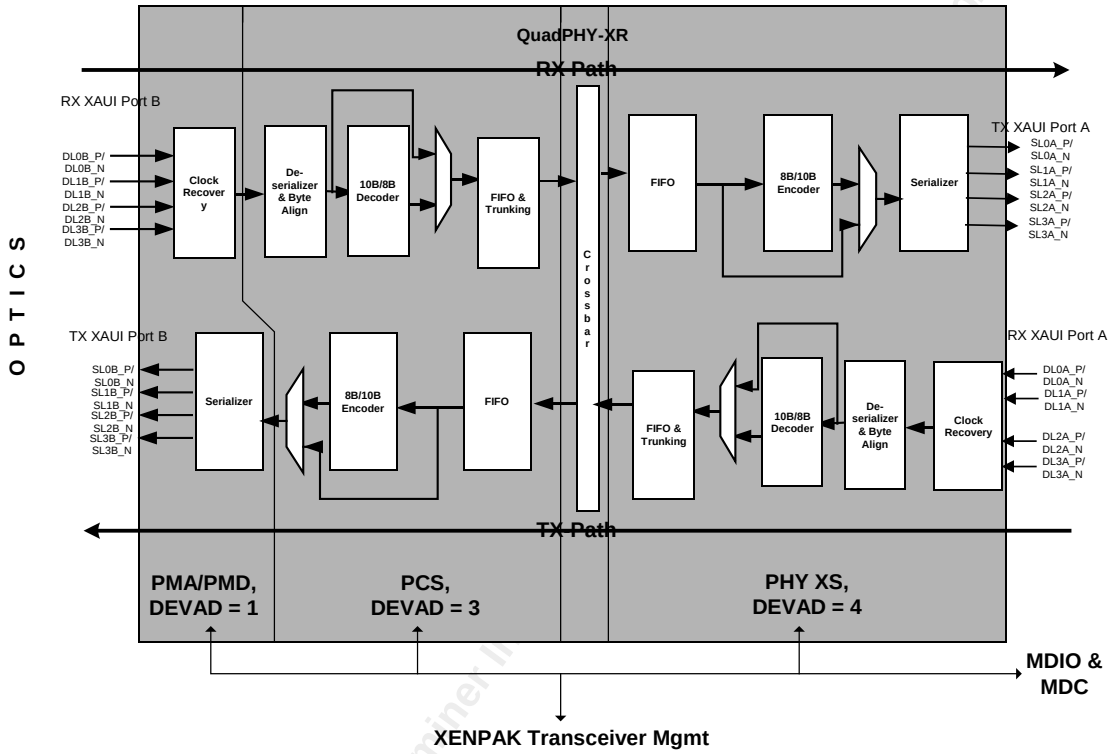


Figure 6 Block Diagram: MDIO MMD View



7 Description

The PM8357, QuadPHY XR is an IEEE 802.3ae and T11 compliant, fully redundant, full duplex, XAUI to XAUI 10 Gigabit Ethernet/Fibre Channel SERDES device. It includes integrated serializer/de-serializer, clock recovery, clock synthesis, byte alignment, trunking, and 8B/10B encode/decode logic for both ports. The QuadPHY XR also supports completely non-blocking cross-connect to enable flexible configuration in parallel loopback, XAUI re-timer and XAUI cross-connect. The QuadPHY XR non-blocking cross-connect includes a smart switchover mechanism allowing connections to be changed during IPG and minimize packet fragmentation. The device implements the PHY-XS constituent of the XGMII Extender Sublayer (XGXS) and the PMA/PMD and PCS MDIO Manageable Devices (MMDs) as defined in IEEE 802.3ae for 10GBASE-X family of physical layer implementations (10GBASE-LX4). The QuadPHY XR supports independent lane based operation for all 8 lanes each running at 1.2Gbit/s to 3.2 Gbit/s with 8B/10B encoded data and 2.488 Gbit/s for scrambled NRZ 8 bit data. In addition, the QuadPHY XR supports a differential PECL REFCLK up to 159.375 MHz.

The PM8357, QuadPHY XR device provides a bi-directional high-speed interface with integrated serializer/de-serializer, clock recovery, clock synthesis, byte alignment, and 8B/10B encode/decode logic. The high-speed outputs have programmable pre-emphasis to counteract dielectric losses and allow maximum reach on printed circuit boards. The high-speed inputs with programmable equalization to reduce Inter Symbol Interference (ISI) providing robust BER performance. The QuadPHY XR incorporates internal 100 Ω differential termination on transmit and receive high-speed interfaces for optimal signal integrity.

The QuadPHY XR device supports pin programmable configuration with a software override for all major modes of operation. For most of the targeted applications, pin configuration is adequate. This device also supports 2-pin serial management interface using an MDC/MDIO interface for configuration and diagnostic access.

The QuadPHY XR supports built in self-test (BIST) via internal packet generator and checker and various serial and parallel loopback modes for testing and debugging on a per-channel basis. The device provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan.

The QuadPHY XR has a low power operation and further power savings can be achieved by disabling unused links and unused features. Power for full mode of operation with loaded outputs is 1.6 Watts typical case with 2 XAUI links operating, and only 1 Watt typical case with a single XAUI link active.

The QuadPHY XR is packaged in small footprint 15x15 mm, 196-pin BGA package with 1 mm ball pitch.

8 Pin Diagram

The QuadPHY XR is packaged in a 196 BGA package having a body size of 15 mm by 15 mm and a pin pitch of 1.0 mm.

Figure 7 Pin Diagram (Ball View)

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	PRTAD3	TX_FAULT_B	NC	VSS	PRTAD1	TRSTB	TDO	TDI	TMS	RSTB	MDIO	HC[1]	AVDL	VSS	A
B	MODE_SEL1	EN_SLBK_A	EN_PRE_EMPHASIS	PRTAD0	PRTAD2	PRTAD4	NC	NC	TCK	MDC	HC[0]	VSS	SL1A_P	SL1A_N	B
C	VSS	MODE_SEL0	TX_FAULT_A	VSS	VSS	VSS	NC	VSS	VSS	VSS	VSS	SL0A_P	SL0A_N	VSS	C
D	MDIO_SEL	EN_SLBK_B	VSS	VSS	VSS	VSS	VDDI	VDDO	VDDI	VDDO	VSS	VSS	DL1A_P	DL1A_N	D
E	SYSCLK	SD_A	NC	VSS	VSS	VSS	VSS	VSS	VSS	VDDO	AVDL	DL0A_P	DL0A_N	VSS	E
F	VSS	FAILOVER	VSS	VDDI	VSS	VSS	VSS	VSS	VSS	AVDL	VSS	VSS	SL2A_P	SL2A_N	F
G	SD_B	FAILOVER_IMM	NC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDL	SL3A_P	SL3A_N	VSS	G
H	RX_FAULT_B	VSS	NC	VDDI	VSS	VSS	VSS	VSS	VSS	AVDL	VSS	VSS	DL2A_P	DL2A_N	H
J	RX_FAULT_A	VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDH	DL3A_P	DL3A_N	VSS	J
K	EN_EQUALIZATION	VSS	VDDO	VDDI	VDDO	AVDL	AVDL	AVDH	VSS	VSS	VSS	VSS	AVDL	VSS	K
L	INTB	NC	VSS	VSS	AVDL	VSS	VSS	AVDL	CAVDL0	CAVDL1	VSS	NC	QAVD	CAVDH0	L
M	VSS	DL3B_N	VSS	SL2B_N	VSS	DL0B_N	VSS	SL0B_N	VSS	VSS	AVDL	VSS	CAVDL2	NC	M
N	DL2B_N	DL3B_P	SL3B_N	SL2B_P	DL1B_N	DL0B_P	SL1B_N	SL0B_P	REFCLK_P	CAVDH1	NC	NC	NC	NC	N
P	DL2B_P	VSS	SL3B_P	VSS	DL1B_P	VSS	SL1B_P	VSS	REFCLK_N	VSS	NC	VSS	NC	VSS	P
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

9 Pin Description

Table 2 XAUI Receive High Speed Input Pin Descriptions

Pin Name	Type	Pin	Function
DL0A_P *DL0A_N*	Analog CML Input	*E3* *E2*	*Port A XAUI Differential Serial Data Input – lane 0* DL0A_P and DL0A_N are the 3.1875/3.125 Gbit/s differential inputs for lane 0 of port A XAUI port in 10GFC/10GE mode of operation. *DL0A_P* and *DL0A_N* are the 1.2 Gbit/s to 3.2 Gbit/s differential inputs for lane 0 of the primary serial receive port when configured to support Lane Based and SERDES operation. These differential inputs are internally terminated with a 100Ω differential resistor. These differential inputs are ignored when Serial Loopback is enabled. If a channel is enabled, active data must be provided to it, or the invalid data will be recovered. Do not use pull-up/pull-down resistors on the high-speed differential inputs. These inputs may be left unconnected when this channel is disabled.
DL0B_P *DL0B_N*	Analog CML Input	*N9* *M9*	*Port B XAUI Differential Serial Data Input – lane 0* DL0B_N and DL0B_N are /3.125 Gbit/s differential inputs for lane 0 of port B XAUI port when configured to support 10GFC/10GE mode. DL0B_N and DL0B_N are the 1.2 Gbit/s to 3.2 Gbit/s differential inputs for lane 0 of port B serial receive port when configured to support Lane Based and SERDES operation. These differential inputs are internally terminated with a 100Ω differential resistor. These differential inputs are ignored when Serial Loopback is enabled. If a channel is enabled, active data must be provided to it, or the invalid data will be recovered. Do not use pull-up/pull-down resistors on the high-speed differential inputs. These inputs may be left unconnected when this channel is disabled.
DL1A_P *DL1A_N*	Analog CML Input	*D2* *D1*	*Port A XAUI Differential Serial Data Input – lane 1* Equivalent to DL0A_P and DL0A_N for XAUI port lane 1.
DL1B_P *DL1B_N*	Analog CML Input	*P10* *N10*	*Port B XAUI Differential Serial Data Input – lane 1* Equivalent to DL0B_N and DL0B_N for XAUI port lane 1
DL2A_P *DL2A_N*	Analog CML Input	*H2* *H1*	*Port A XAUI Differential Serial Data Input – lane 2* Equivalent to DL0A_P and DL0A_N for XAUI port lane 2.
DL2B_P *DL2B_N*	Analog CML Input	*P14* *N14*	*Port B XAUI Differential Serial Data Input – lane 2* Equivalent to DL0B_N and DL0B_N for XAUI port lane 2.

Pin Name	Type	Pin	Function
DL3A_P *DL3A_N*	Analog CML Input	*J3* *J2*	*Port A XAUI Differential Serial Data Input – lane 3* Equivalent to DL0A_P and DL0A_N for XAUI port lane 3.
DL3B_P *DL3B_N*	Analog CML Input	*N13* *M13*	*Port B XAUI Differential Serial Data Input – lane 3* Equivalent to DL0B_N and DL0B_N for XAUI port lane 3.

Table 3 XAUI Transmit High Speed Output Pin Descriptions

Pin Name	Type	Pin	Function
SL0A_P *SL0A_N*	Analog CML Output	*C3* *C2*	*Port A XAUI Differential Serial Data Output – lane 0* SL0P_A and SL0N_A are the 3.1875/3.125 Gbit/s outputs for Port A XAUI port lane 0 when configured to support 10GFC/10GE mode. SL0P_A and SL0N_A are the 1.2 Gbit/s to 3.2 Gbit/s differential outputs for lane 0 of port A serial transmit port when configured to support Lane Based and SERDES operation. These differential outputs are internally terminated with a 100Ω differential resistor. When Serial, Parallel Diagnostic or System Loopback mode is selected, these outputs are optionally driven high. These outputs are tri-stated when disabled through management register control.
SL0B_P *SL0B_N*	Analog CML Output	*N7* *M7*	*Port B XAUI Differential Serial Data Output – lane 0* SL0P_B and SL0N_B are the 3.1875/3.125 Gbit/s outputs for Port A XAUI port lane 0 when configured for 10GFC/10GE operation. SL0P_B and SL0N_B are the 1.2 Gbit/s to 3.2 Gbit/s differential outputs for lane 0 of port B serial transmit port when configured to support Lane Based and SERDES operation. These differential outputs are internally terminated with a 100Ω differential resistor. When Serial, Parallel Diagnostic or System Loopback mode is selected, these outputs are optionally driven high. These outputs are tri-stated when disabled through management register control.
SL1A_P *SL1A_N*	Analog CML Output	*B2* *B1*	*Port A XAUI Differential Serial Data Output – lane 1* Equivalent to SL0P_A and SL0N_A for XAUI port lane 1.
SL1B_P *SL1B_N*	Analog CML Output	*P8* *N8*	*Port B XAUI Differential Serial Data Output – lane 1* Equivalent to SL0P_B and SL0N_B for XAUI port lane 1.
SL2A_P *SL2A_N*	Analog CML Output	*F2* *F1*	*Port A XAUI Differential Serial Data Output – lane 2* Equivalent to SL0P_A and SL0N_A for XAUI port lane 2.
SL2B_P *SL2B_N*	Analog CML Output	*N11* *M11*	*Port B XAUI Differential Serial Data Output – lane 2* Equivalent to SL0P_B and SL0N_B for XAUI port lane 2.

Pin Name	Type	Pin	Function
SL3A_P *SL3A_N*	Analog CML Output	*G3* *G2*	*Port A XAUI Differential Serial Data Output – lane 3* Equivalent to SL0P_A and SL0N_A for XAUI port lane 3.
SL3B_P *SL3B_N*	Analog CML Output	*P12* *N12*	*Port B XAUI Differential Serial Data Output – lane 3* Equivalent to SL0P_B and SL0N_B for XAUI port lane 3.
SD_A	Input with Pull-Up	*E13*	*Port A Signal Detect* The SD_A input is the signal detect indicators for port A link. When SD_A is a logical 0, it indicates that there is no meaningful signal on the Port A high speed receive interface. When SD_A is a logical 1, it indicates that there is valid data on port A high speed receive interface. The active state of this bit is configurable through management control. This signal should be an asserted if any of the 4 lanes within Port A receive channel become invalid external to the device. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
SD_B	Input with Pull-Up	*G14*	*Port B Signal Detect* The SD_A input is the signal detect indicators for port B link. When SD_B is a logical '0', it indicates that there is no meaningful signal on the Port high speed receive interface. When SD_B is a logical '1', it indicates that there is valid data on port A high speed receive interface. The active state of this bit is configurable through management control. This signal should be an asserted if any of the 4 lanes within Port B receive channel become invalid external to the device. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.

Table 4 Management Interface Pin Descriptions

Pin Name	Type	Pin	Function
PRTAD[4] *PRTAD[3]* *PRTAD[2]* *PRTAD[1]* *PRTAD[0]*	Input	*B9* *A14* *B10* *A10* *B11*	*Port Address* The PRTAD[4:0] is a 5-bit pin programmable port address. These Management Interface address terminals are used to assign a unique address to each QuadPHY XR. Note that the address is assigned to the entire chip, not to individual channels within the chip. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.

Pin Name	Type	Pin	Function
MDC	Input	*B5*	*Management Data Clock* This signal carries control and status information for the Management Data Interface. The MDIO pin is driven and sampled synchronously on the rising edge of the MDC signal. MDC can be aperiodic. This input pin operates at 1.2 V, 1.8V, 2.5V, 3.3V depending on the state of the *MDIO_SEL* input.
MDIO	Open Drain Bidirectional	*A4*	*Management Data Input/Output/Serial Data Line* The MDIO signal carries control and status information for the Management Data Interface. The MDIO is driven and sampled synchronously on the rising edge of the MDC signal. The MDIO is an open-drain bi-directional signal. It is expected that there is a sufficient external pull-up resistor to 1.2 V on the MDIO external to the device. This open drain pin operates at .2 V, 1.8V, 2.5V, 3.3V depending on the polarity of the *MDIO_SEL* input.
MDIO_SEL	Input	*D14*	*Management Interface Voltage Selection* The *MDIO_SEL* input selects the operating voltage of the *MDIO* and *MDC* inputs. When a logic 1, the *MDIO* and *MDC* inputs work at 1.2v MDIO mode, which is fully compliant with the IEEE 802.3ae standard. When *MDIO_SEL* is a logic 0, the pad is working at 1.8/2.5/3.3v hybrid mode for legacy compatibility. Please refer to the D.C. Electrical Characteristics section for details on these 2 modes. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
RX_FAULT_A	Output	*J14*	*XAUI Port A Receive Fault* This signal indicates if there is a fault condition on port A receive XAUI channel. Contributing factors to the assertion of this signal include digital transition detect failure, loss of receive synchronization, loss of receive alignment and the *SD_A* input pin. The dependency of *RX_FAULT_A* on the above conditions is programmable through register control. This is an asynchronous output.
RX_FAULT_B	Output	*H14*	*XAUI Port B Receive Fault* This signal indicates if there is a fault condition on port B receive XAUI channel. Contributing factors to the assertion of this signal include digital transition detect failure, loss of receive synchronization, loss of receive alignment and the *SD_B* input pin. The dependency of *RX_FAULT_B* on the above conditions is programmable through register control. This is an asynchronous output.

Pin Name	Type	Pin	Function
TX_FAULT_A	Output	*C12*	*XAUI Port A Transmit Fault* This signal indicates if there is a fault condition on port A transmit XAUI channel. This signal indicates an internal transmit FIFO error in the device or loss of PLL lock in the Clock Synthesis Unit. This is an asynchronous output.
TX_FAULT_B	Output	*A13*	*XAUI Port B Transmit Fault* This signal indicates if there is a fault condition on port B transmit XAUI channel. This signal indicates an internal transmit FIFO error in the device or loss of PLL lock in the Clock Synthesis Unit. This is an asynchronous output.

Table 5 Cross Bar Control

Pin Name	Type	Pin	Function
FAILOVER	Input with pull-up	*F13*	*FAILOVER* Assertion of this signal initiates a controlled switchover of the space switch cross-connect from the active to standby register settings. This functionality is shared with internal register bits via the management register control. This input is logically OR'ed with the register bit to achieve the desired operation. This is an asynchronous input. . This pin should not be asserted within 250 ns on an MDIO write to the STANDBY registers used for switching lanes. See Operations Section for details. For software control of the switchover via the corresponding register bits, the FAILOVER (FAILOVER_IMM) pin must be strapped to ground This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
FAILOVER_IMM	Input with pull-up	*G13*	*FAILOVER_IMM* Assertion of this signal initiates an immediate switchover of the space switch cross-connect from the active to standby register settings. This functionality is shared with internal register bits via the management register control. This input is logically OR'ed with the register bit to achieve the desired operation. This is an asynchronous input. This pin should not be asserted within 250 ns on an MDIO write to the STANDBY registers used for switching lanes. See Operations Section for details. For software control of the switchover via the corresponding register bits, the FAILOVER (FAILOVER_IMM) pin must be strapped to ground This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.

Table 6 Clock, Control and Status Pin Descriptions

Pin Name	Type	Pin	Function
REFCLK_P *REFCLK_N*	Analog PECL Input	*N6* *P6*	*Reference Clock* This input requires a low jitter reference clock operating at between 60 MHz ±100ppm to 160 MHz ±100ppm for 1.2 Gbit/s to 3.2 Gbit/s operation. Please refer to Table 10 for more details.The Reference Clock provides an internal 100 ohm differential termination. The Clock Synthesis PLL uses this clock to generate a phase locked internal clock for serialization and deserialization. These inputs must be externally AC coupled.
SYSCLK	Output	*E14*	*System Utility Clock* This output is derived from the internal PLL, and is provided for use by upstream devices. *SYSCLK* is frequency locked to *REFCLK* frequency.
HC[1] *HC[0]*	Input with Pull-up	*A3* *B4*	*High Current – Amplitude control for the high speed transmit drivers.* *HC[1:0]* – High speed transmit output levels With pre-emphasis off: 00 – min swing 01 – intermediate swing 10 - intermediate swing 11 – Max swing XAUI-compatible With pre-emphasis on: 00 – XAUI with 1/0.46(high/low) 01 – XAUI with 1/0.56(high/low) 10 – XAUI with 1/0.66(high/low) 11 – XAUI with 1/0.76(high/low) The *HC[1:0]* pins have internal pull-up resistors. This functionality is shared with internal register bits via the management register control. This input is logically XOR'ed with the register bit to achieve the desired operation. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
EN_PRE-EMPHASIS	Input with Pull-up	*B12*	*Enable Pre-Emphasis* (active high). This input signal is used to enable the pre-emphasis feature of the high-speed transmit interfaces. Pre-emphasis can only be enabled on high-speed ports that are in high swing or XAUI compatible swing mode. When *EN_PRE-EMPHASIS* is one, pre-emphasis is enabled on port A high speed differential signals, *SLnA_P* / *SLnA_N*, and Port B high speed differential signals, *SLnB_P* / *SLnB_N*. When *EN_PRE-EMPHASIS* is zero, pre-emphasis is disabled on port A high speed differential signals, *SLnA_P* / *SLnA_N*, and Port B high speed differential

Pin Name	Type	Pin	Function
			signals, *SLnB_P* / *SLnB_N*. Pre-emphasis can be further granulated using register control. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
EN_SLPBK_A	Input with Pull up	*B13*	*Enable Serial Data Loopback Port A (active high)* This input enables the loopback function for serial data. When logic 1, serial data is routed from the output of the serializer block to the input of the clock recovery block of Port A. The high speed transmit Port A differential signals, *SLnA_P* / *SLnA_N*, outputs also contains the data in the loopback path. The high speed receive Port A differential signals *DLnA_P*, *DLnA_N*, are ignored. This input should be held low for normal operation, or to relinquish serial loopback control to the management register control in the *MDIO* MMD pre-defined register space. The *EN_SLPBK_A* input pin will override the register only when it is a logic 1. This functionality is shared with an internal register bit via the management register control. This input is logically XOR'ed with the register bit to achieve the desired operation. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
EN_SLPBK_B	Input with Pull up	*D13*	*Enable Serial Data Loopback Port B (active high)* This input enables the loopback function for serial data. When logic 1, serial data is routed from the output of the serializer block to the input of the clock recovery block of Port A. The high speed transmit Port A differential signals, *SLnB_P* / *SLnB_N*, outputs also contains the data in the loopback path. The high speed receive Port A differential signals *DLnB_P*, *DLnB_N*, are ignored. This input should be held low for normal operation, or to relinquish serial loopback control to the management register control in the *MDIO* MMD pre-defined register space. The *EN_SLPBK_B* put pin will override the register only when it is a logic 1. This functionality is shared with an internal register bit via the management register control. This input is logically XOR'ed with the register bit to achieve the desired operation This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
EN_EQUALIZATION	Input with Pull up	*K14*	*Enable Equalization (active high)* The *EN_EQUALIZATION* input is used to enable the high speed analog receiver equalization. When *EN_EQUALIZATION* is a logic 1, equalization is set to high on port A channel high speed differential signals,

Pin Name	Type	Pin	Function
			DLnA_P / *DLnA_N*, and port B channel high speed differential signals, *DLnB_P* / *DLnB_N*. When *EN_EQUALIZATION* is logic 0, equalization is set to half on port A channel high speed differential signals, *DLnA_P* / *DLnA_N*, and port B channel high speed differential signals, *DLnB_P* / *DLnB_N*. Equalization can be further granulated using register control. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
MODE_SEL[1] MODE_SEL[0]	Input with Pull up	*B14* *C13*	*Mode Select* The mode select pins select modes of the device. MODE_SEL[1:0] – Description *00 – 10GE Operation* Device configured to operate as XAUI to XAUI retimer operating at 4 x 3.125 Gbit/s per port with **trunking and 8B/10B processing enabled** to support 10GE operation. *01 – 10GFC Operation* Device configured to operate as XAUI to XAUI retimer operating at 4 x 3.1875 Gbit/s per port with **trunking and 8B/10B processing enabled** to support 10GFC operation. *10 –Lane-Based Operation* Device configured to operate as a SERDES with **trunking disabled and 8B/10B processing enabled**. operating between 2.5 Gbits/s to 3.2 Gbits/s per link. *11 RESERVED* The functionality controlled by these pins is shared with various internal register bits via the management register control. The *MODE_SEL[1:0]* input is decoded then logically XOR'ed with the relevant register bit to achieve the desired operation. Out of reset, the *MODE_SEL[1:0]* pins are respected and further programmability can then be realized through register bits. This is an asynchronous input. This input operates at 2.5 V CMOS levels, and is 3.3 V tolerant.
RSTB	Input with pull up	*A5*	*System Reset* (Active low). This input resets the device to a known state. All registers go to default values, all state machines are reset, and all data path flip-flops are reset. . RSTB is a Schmidt triggered input with an integral pull-up resistor. RSTB should be held low for at least 500 nS when asserted.
INTB	Open Drain Output	*L14*	The active low interrupt (*INTB*) signal is set low when a QuadPHY XR enabled interrupt source is active. The QuadPHY XR may be enabled to report many alarms or events via interrupts.

Pin Name	Type	Pin	Function
			INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. *INTB* is an open drain output , and should be pulled high using an external 10K ohm resistor to a maximum of 3.3 volts. This is an asynchronous input.

Table 7 JTAG Test Pin Descriptions

Pin Name	Type	Pin	Function
TMS	Input with Pull-up	*A6*	*JTAG (IEEE 1149.1) Test Mode Select Input* This input controls the test operations that can be carried out using the IEEE 1149.1 test access port. This input has an internal 50K Ω pullup resistor.
TCK	Input	*B6*	*JTAG (IEEE 1149.1) Test Clock Input.* This signal provides timing for test operations that can be carried out using the IEEE 1149.1 test access port. This input has an internal 50K Ω pullup resistor.
TDI	Input with Pull-up	*A7*	*JTAG (IEEE 1149.1) Test Data Input* When the QuadPHY XR is configured for JTAG operation, this input carries test data into the device via the IEEE 1149.1 test access port. This input has an internal 50K Ω pullup resistor.
TDO	Output	*A8*	*JTAG (IEEE 1149.1) Test Data Output* This signal carries test data out of the QuadPHY XR via the IEEE 1149.1 test access port.
TRSTB	Input with Pull-up	*A9*	*JTAG (IEEE 1149.1) Test Reset Input* This signal provides an asynchronous reset to the 1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull-up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

Table 8 Supply and Reference Pin Descriptions

Pin Name	Type	Pin	Function
VDDI (6)	Power	*D6, D8, K11, J13, H11, F11*	*Digital Core Power Supply* 1.2V ± 5%
VDDO (5)	Power	*K12, K10, D7, D5, E5*	*Digital I/O supply* 2.5 V ± 5%.
AVDH (2)	Power	*J4, K7*	*Analog Power Supply* 2.5 V ± 5% analog supply

Pin Name	Type	Pin	Function
AVDL (11)	Power	*A2, E4, F5, G4, H5, K9, K8, K2, L10, L7, M4*	*Analog Power Supply* 1.2 V ± 5% analog supply
CAVDL0 *CAVDL1* *CAVDL2*	Power	*L6, L5, M2*	*Analog Power Supply* 1.2 V ± 5% analog supply
CAVDH0 *CAVDH1*	Power	*L1,N5*	*Analog Power Supply* 2.5 V ± 5% analog supply
QAVD	Power	*L2*	*Quite Analog Power* 2.5 V ± 5% analog supply
VSS (84)	Ground	*A1, A11 B3, C14, C11, C10, C9, C7, C6, C5, C4, C1, D12, D11, D10, D9, D4, D3, E11, E10, E9, E8, E7, E6, E1, F14, F12, F10, F9, F8, F7, F6, F4, F3, G11, G10, G9, G8, G7, G6, G5, G1, H13, H10, H9, H8, H7, H6, H4, H3, J12, J11, J10, J9, J8, J7, J6, J5, J1, K13, K6, K5, K4, K3, K1, L12, L11, L9, L8, L4, M14, M12, M10 ,M8, M6 ,M5, M3, P13, P11, P9, P7, P5, P3, P1*	*Digital Core and Noisy I/O Ground*

Pin Name	Type	Pin	Function
NC		*B7, B8, C8, E12, G12, H12, L3, L13, M1 , A12, N1, N2, P2, N3,P4, N4*	*No Connect. These balls should not be connected.*

9.1 Pad Summary

Table 9 Pad Summary

Interface	Analog Inputs	Analog Outputs	Digital Inputs	Digital Outputs	Digital Bidir	Pwr/ Gnd	Total
Serial Line Side Interface	16	16	2	0	0	0	**34**
System Side Interface	0	0	0	0	0	0	**0**
Microprocessor Interface	0	0	9	0	1	0	**10**
Control & Status	0	0	11	6	0	0	**17**
JTAG Test Access Port	0	0	4	1	0	0	**5**
Analog Misc.	6	2	0	0	0	0	**8**
Analog Power	0	0	0	0	0	19	**19**
Digital Power	0	0	0	0	0	11	**11**
Ground	0	0	0	0	0	84	**84**
Totals	**22**	**18**	**26**	**7**	**1**	**114**	**188**

Pin Description Notes:

1. All QuadPHY XR inputs and bi-directionals present minimum capacitive loading and operate at LVCMOS/LVTTL logic levels except: the *REFCLK_P/N* pins, which operate at AC coupled pseudo-ECL (PECL) logic levels; and *SLnA_P/N*, *SLnB_P/N*, which operate at CML logic levels.

   NOTE: Drive Capability: AC Drive is the transient output response of a circuit when the input is switched. The value describes both the time delay and the output load drive capability. For example, a circuit with an AC drive capability value of 4 normally has a shorter time delay and can drive larger capacitive loads than a circuit with an AC drive capability value of 3. The AC drive capability value is only a factor and should not be interpreted as an analog AC performance value. Please see the DC Characteristics Section for a complete electrical description of each pin.

2. It is mandatory that every ground pin (*VSS*) be connected to the printed circuit board ground plane to ensure reliable device operation.
3. It is mandatory that every analog power pin (*QAVD, AVDH, AVDL*) and every digital power pin (VDDI, VDDO) be connected to the printed circuit board power plane to ensure reliable device operation.
4. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to the Operations section.
5. Due to ESD protection structures in the pads, it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.
6. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operation section.

7. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.
8. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.
9. Ensure that all digital power is applied simultaneously, and applied simultaneously with or after the analog power. Refer to the Power Sequencing description in the Operation section.

10 Functional Description

The PM8357 QuadPHY XR consists of Common Control Logic and four main functional blocks: Clock Synthesizer, Transmit Data Path, Receive Data Path, and the Crossbar. The Common Control Logic includes the Management Interface, control registers, and test logic.

10.1 Clock Synthesizer

The Clock Synthesizer uses a PLL to synthesize a clock from the *REFCLK*+/- input. The QuadPHY XR operates from 1.2 Gbit/s to 3.1875 Gbit/s based on the *REFCLK*+/- input. The frequency of the PLL clock can be 16 or 20 times the frequency of *REFCLK*+/-, and a single synthesized clock is used to transmit serial data on all four transmit channels.

The PLL clock frequency can vary over a range of 1.2 GHz to 3.1875 GHz by changing the frequency of *REFCLK*+/-. Some application examples are as shown in Table 10.

Table 10 REFCLK+/- and PLL Clock Combinations

REFCLK+/- Frequency	Multiplier	PLL Clock Frequency	Transmit Data Rate	Application
122.88 MHz	10X1	1.2288 GHz	1.2288 Gbit/s	CPRI
61.44 MHz	20X	1.2288 GHz	1.2288 Gbit/s	CPRI
125 MHz	10X1	1.25 GHz	1.25 Gbit/s	GE
62.5 MHz	20X	1.25 GHz	1.25 Gbit/s	GE
148.5 MHz	10X1	1.485 GHz	1.485 Gbit/s	HDTV/Video Server
74.25 MHz	20X	1.485 GHz	1.485 Gbit/s	HDTV/Video Server
153.6 MHz	10X1	1.536 GHz	1.536 Gbit/s	OBSAI RP3
76.8 MHz	20X	1.536 GHz	1.536 Gbit/s	OBSAI RP3
106.25 MHz	20X	2.125 GHz	2.125 Gbit/s	2G Fibre Channel
122.88 MHz	20X	2.4576 GHz	2.4576 Gbit/s	CPRI
125 MHz	20X	2.5 GHz	2.5 Gbit/s	Infiniband
156.25 MHz	20X	3.125 GHz	3.125 Gbit/s	10GbE
159.375 MHz	20X	3.1875 GHz	3.1875 Gbit/s	10GFC
155.52 MHz	16X	2.488 GHz	2.488 Gbit/s	8-bit scrambled NRZ

Notes:

1. 10x REFCLK multiplier ratio is enabled by writing 0x0110h to register 0xD0B5h.

The PLL has a programmable integer multiplier for different line rate-to-reference rate ratios.

10.2 Transmit Data Path

The transmit data path consists of a Crossbar, Transmit FIFO, 8B/10B Encoder, Serializer and High-speed Output Driver.

The QuadPHY XR provides two independent transmit channels operating at data rates of 1.2 to 3.2 Gbs for use in applications such as 10 Gigabit Ethernet, 10 Gigabit Fibre Channel, SONET and serial backplanes. The 8 high speed serial transmit lanes are mapped to 4 Port A lanes and 4 Port B lanes, each lane is capable of driving a differential high-speed 100Ω differential transmission line. The internal 8x8 Cross-Connect block provides all combinations of possible data sources to each of the lanes.

10.2.1 Transmit FIFO

The QuadPHY XR has a transmit FIFO on each channel for phase compensation of the input data. The Transmit FIFO separates the clock domains of the serial receive and transmit interfaces.

10.2.2 8B/10B Encoder

The QuadPHY XR is capable of encoding data using 8B/10B block encoding. The 8B/10B encoding scheme ensures sufficient transition density so that a clock can be recovered from the encoded data at the far end.

When enabled, the encoder accepts an 8-bit data word and a bit K-bit character. The K-bit character defines whether the 8-bit word is a control character or a data character.

The encoder generates a running disparity by generating sub-blocks of 6- and 4-bit codes that limit the run length and maintain the DC balance of the serialized data stream. Negative running disparity is set on all four transmit channels upon initialization.

Alternatively, the user may disable the 8B/10B encoding logic and run pre encoded data through the device from Port A to Port B and vice versa.

10.2.3 Serializer

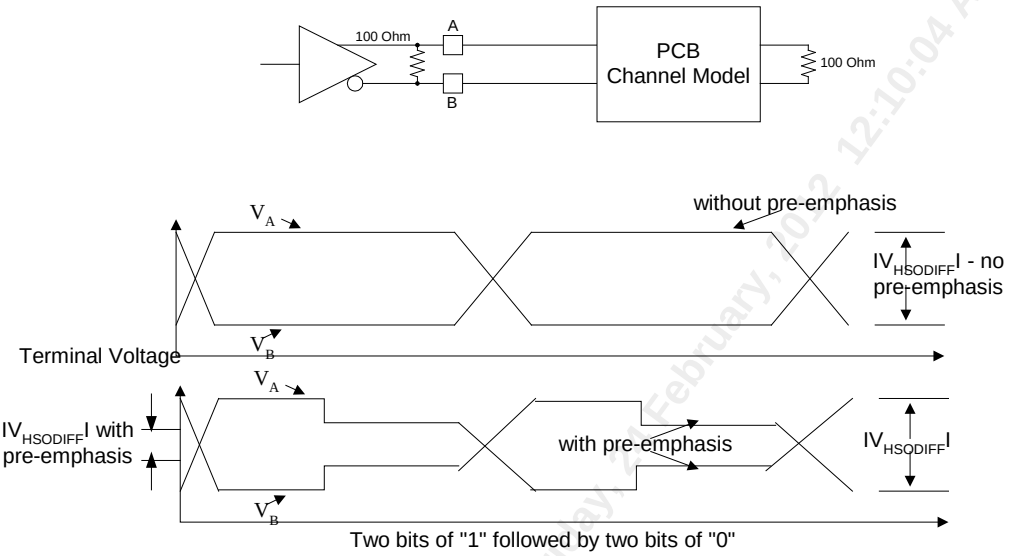
The serializer accepts 10-bit characters from the 8B/10B Encoder, or 8-bit bytes from an NRZ data stream, and converts the data into a serial bit stream running at 1.2 Gbit/s to 3.2 Gbit/s , depending on the reference clock frequency. The least significant bit is transmitted first.

10.2.4 High-Speed Output Driver

High-speed output data is driven differentially and may directly drive coaxial cable or PC-board interconnect. For backplanes implemented with FR4 or similar materials, significant dielectric losses occur at high frequencies that severely limit the achievable separation between transmitter and receiver.

To mitigate this problem, the QuadPHY XR supports programmable pre-emphasis on the high-speed transmit outputs. The pre-emphasis circuit accentuates high-frequency components. Pre-emphasis compensates for loss of high frequency components in the backplane material so that the signal received at the far end is much cleaner and has a wider eye than data transmitted with simple bi-level output buffers. Figure 8 shows the effect of pre-emphasis on the transmitted waveform.

Figure 8 Output Pre-Emphasis



10.3 Receive Data Path

The Receive Data Path consists of a Clock and Data Recovery Unit, Deserializer and Byte Alignment Logic, a 8B/10B Decoder, a Receive FIFO and Crossbar.

10.3.1 Clock and Data Recovery

The Clock and Data Recovery unit recovers the clock and data embedded in the incoming serial stream. The clock and data recovery is performed on each of the input lanes separately with the corresponding data and recovered clocks generated internally per lane. For trunked XAUI operation, the incoming four lanes need to be frequency locked to each other. For lane based operation each lane can have a frequency offset of ±100 ppm from the nominal frequency derived by multiplying *REFCLK+/-* frequency by 20.

The Clock and Data Recovery circuit will lock to a valid data stream accordance with Table 11. The data stream must be 8B/10B encoded to ensure sufficient transition density and the data rate must be within ±100 ppm of the nominal rate to guarantee proper lock. This allows a total skew budget of ±200 ppm from the transmitter's clock source to the receiver's clock reference.

Table 11 Lock time of CSU in bit periods

Transition Density	Data Contents	Frequency Tracking Loop Filter Co-efficient = 16	Frequency Tracking Loop Filter Co-efficient = 32	Frequency Tracking Loop Filter Co-efficient = 48
0.5	K28.5 Idle Character	384 BP	768 BP	1152 BP
0.6	Random 8B/10B endoded data	320 BP	640 BP	960 BP
0.8	K28.5, D21.4, D21.5 and D21.5 Idle Ordered Set	240 BP	480 BP	720 BP

The Clock and Data Recovery unit also performs various levels of Equalization to reduce the distortion on the data due to deterministic jitter arising from limited bandwidth of the transmission channel, or Inter Symbol Interference.

While receiving SONET scrambled data, the Clock and Data Recovery circuit will be able to correctly recover data with run lengths of up to 80 consecutive identical digits, as specified by ITU-T G.958.

10.3.2 Deserializer and Byte Alignment Logic

After clock recovery, the device deserializes and byte aligns the received data. The Byte Alignment Logic searches the coded incoming serial stream for a sequence defined in IEEE 802.3z as a "comma". A comma sequence is defined as “0011111xxx” or its complement, “1100000xxx.” The Byte Alignment Logic detects and aligns to both positive and negative commas of K28.1 and K28.5 code groups as per 10GE/10GFC standards. The comma K28.7 is reserved in the above standards and it is not supported by the QuadPHY XR for byte alignment. Upon detection of a comma sequence, the Byte Alignment Logic shifts the incoming data to properly align the received data. Alternately, byte Alignment logic can be bypassed.

Each channel performs comma detection independently and provides the byte aligned words to the 8B/10B Decoder. During byte alignment, up to (but not exceeding) four 10-bit code groups may be deleted or modified while aligning the code group to the edges of the receive clock.

The serial bit stream must be ordered "abcdeifghj" with "a" being the first bit received and "j" the last bit received by the QuadPHY XR.

10.3.3 8B/10B Decoder

The QuadPHY XR has 8B/10B decode logic to decode the 10-bit code-group-aligned data into 8-bit data and 1 bit K-control bit. The K-control bit indicates whether the corresponding word is a data word or a control word.

The 8B/10B Decoder checks for code violation and disparity errors in the received data stream, and based on software control, the QuadPHY XR can replace the incoming errored data with the 8B/10B Error Character, **/E/**. The **/E/** character is a K30.7 or 0xDFE after 8B/10B decoding.

10.3.4 Receive Trunking

The QuadPHY XR absorbs receive system clocking differences from the transmit source through a 16 byte FIFO. The QuadPHY XR supports clock rate difference compensation by inserting and deleting idle characters. A ± 200 ppm difference between clocks is tolerated for 16K byte trunked packets with 12 bytes minimum IPG across the four lanes.

In case of the lane based operation, the FIFO is used to perform the clock rate compensation. If no de-skewing operation is performed or necessary, a ± 200 ppm difference between clocks is tolerated for 16K byte lane-based packets with 20 bytes minimum IPG.

Trunking operation enables all four XAUI lanes to be treated as one 10GbE or 10GFC port.

In trunking mode, the QuadPHY XR utilizes the alignment character (/A/) to de-skew the 4 lanes comprising a trunk. De-skewing is performed automatically by the transmitters and receivers. Up to 60 bits of skew between any 2 lanes in the trunk can be zeroed out in the synchronous mode. Up to 41 bits of skew in the trunk can be zeroed out in the asynchronous mode where clock rate compensation is performed. The skew numbers include 21 bits of skew that is internally generated due to serialization and de-serialization functions.

The following diagram explains pictorially how the alignment is achieved across the four lanes.

Original Data:

-	-	-	D	D	D	D	D	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	S	P	D	D	-	-	-
-	-	-	D	D	D	D	D	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	P	P	D	D	-	-	-
-	-	-	D	D	D	D	T	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	P	P	D	D	-	-	-
-	-	-	D	D	D	D	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	P	P	D	D	-	-	-

D = data, T= end of packet, S = start of packet, P = preamble, R,K = IDLE,
A = alignment, I = IPG

At the transmitter generic IPG characters are replaced with /K/ and /R/ (or equivalently, /KB/ and /RB/) with alignment characters at pseudo-random intervals:

-	-	-	D	D	D	D	D	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	S	P	D	D	-	-	-
-	-	-	D	D	D	D	D	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-	-
-	-	-	D	D	D	D	T	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-	-
-	-	-	D	D	D	D	K	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-	-

Data gets serialized, transmitted across the channels, received and de-serialized by QuadPHY XR. The skew is introduces by the serialization, deserialization and byte alignment process as well as trace length differences and medium differences. The result is that four channels do not line up as a column, as shown below.

-	D	D	D	D	D	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	S	P	D	D	D	D	-	-	-
-	-	-	D	D	D	D	D	D	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-
-	-	-	D	D	D	D	T	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-	-
-	-	-	D	D	D	D	D	D	D	D	K	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D

QuadPHY XR receivers de-skew the incoming data such that the /A/s line up again:

-	-	-	D	D	D	D	D	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	S	P	D	D	-	-	-
-	-	-	D	D	D	D	D	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-	-
-	-	-	D	D	D	D	T	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-	-
-	-	-	D	D	D	D	K	K	R	K	R	R	K	K	A	K	K	R	K	R	K	K	R	K	R	K	P	P	D	D	-	-	-

10.3.5 Receive Transition Detect

The Data Transition Detector de-asserts its transition-detected output when no transition is detected for N consecutive bits. The value of N is determined by the TRANS_DET_THRES[3:0] bits, in granularity of 16 bits, in the Data Lock Detection Control register. In the QuadPHY XR, transition detect on a per-lane basis can optionally contribute to the *RX_FAULT_A* or *RX_FAULT_B* device outputs.

The Data Transition Detector examines the incoming 10-bit data word in sections of 10 bits. For each section, a flag is set if no transition is detected. A counter keeps track of the number of successive 10-bit sections that have a flag set. The count is compared with the programmed threshold after each section is examined and an error flag is set if the threshold is exceeded. The error flag is then checked every clock cycle and if the flag is set, the transition-detected output is de-asserted. The counter accumulates the count across 10-bit word boundaries and is reset to zero when a bit change is detected.

10.3.6 Packet Generator

The generator can generate several patterns such as prbs7, prbs23, fixed, counting, CJPAT and CRPAT. Each pattern will have its own generator but shares the control state machines. The CRPAT and CJPAT generators are responsible for generating the Jitter Patterns as per IEEE 802.3ae for 10GE and NCITS 10GFC for 10GFC. The patterns can be raw or framed (starting with programmable character and ending with a programmable character, with programmable number of idles and data bytes). The patterns can be 8 or 10 bits. The patterns can be generated independently per lane or trunked across the 4 lanes. Trunking is not supported in 10 bit mode.

Each lane will need a state machine and for each pattern type a generator. In trunked mode, only the state machine of lane 0 will be active and the generators in lane 0 will act as masters supplying the seed for the slave generators in the remaining lanes.

10.3.7 Packet Comparator

The comparator can detect several patterns such as prbs7, prbs23, fixed, counting. The patterns can be raw or framed (starting with a programmable /S/ and ending with a programmable /T/, with programmable number of data bytes). The patterns can be 8 or 10 bits. The patterns can be detected independently per lane or trunked across the 4 lanes. Trunking is not supported in 10 bit mode. Each lane has two state machines and for each pattern type a comparator. In trunked mode, only the state machines of lane 0 will be active and the comparators in lane 0 will act as masters supplying the seed for the slave comparators in the remaining lanes.

10.4 Crossbar

QuadPHY XR provides a non-blocking Crossbar switch and implements an intelligent switchover algorithm. The crossbar is a 8x8 static space switch. Mapping of inputs to outputs is controlled by a master-slave register set – StandbyInput_n and ActiveInput_n . The crossover is controlled by the *FAILOVER* and *FAILOVER_IMM* pins that control if the switchover is performed during IPG and minimize packet fragmentation or is performed immediately when requested.

The Crossbar is a 8x8 Lane 10GbE/FC Crossbar Space Switch. The Crossbar is capable of intelligent switching on packet boundaries in 10bit 8B/10B encoded data or 8 bit data plus k bit control signal. The Crossbar is also capable of switching arbitrary data up to the compatible Lane bus width of 10 bits.

The switch is capable of smart switching on packet boundaries to avoid breaking packets during a switch operation.

The Crossbar has 8 lanes. Each lane is identical to every other lane in the crossbar. A single clock is supplied to each lane. For a switch to be successful, both the active and standby lanes must carry synchronous data. The Crossbar does not perform any phase or rate compensation.

The Crossbar is a non-blocking switch; any of the 8 inputs maybe switched to any of the 8 outputs. Multicasting is supported to propagate a single input to multiple outputs. The data path is 10 bits wide to support 8B/10B encoded data.

Control of the Crossbar can be through fixed configuration pins or management control accesses. Limited switch control through external pins allows configuration without any management control accesses.

10.5 Management Interface

10.5.1 MDIO Description

The QuadPHY XR implements a Management Interface as defined in IEEE 802.3ae. This 2-wire interface consists of MDC (Management Data Clock) and MDIO (Management Data I/O) terminals. The QuadPHY XR supports indirect addressing, as proposed in *IEEE* 802.3ae.

Port Address is determined by the *PRTAD[4:0]* pins. These Management Interface address terminals are used to assign a unique address to each QuadPHY XR. Note that the address is assigned to the entire chip, not to individual channels within the chip. Upon reset, the QuadPHY XR is sensitive to all of the 32 device types offered by IEEE 802.3ae Section 45. It is expected that an initialization sequence will be performed, where the relevant register is programmed to the desired MMD response. However, the QuadPHY XR is intended for PHY-XS, PMA/PMD and PCS applications. The MDC/MDIO interface requires that a full 32 bit preamble be applied prior to the start of each transaction.

The MDIO serial protocol consists of two pins. One is a serial clock pin called MDC and the other is a bi-directional data pin called MDIO.The MDIO interface frame structure is shown in the table below. The order of bit transmission is from left to right.

Table 12 Management Frame Format for Indirect Access

Frame	PRE	ST	OP	PRTAD	DEVAD	TA	Address/Data	Idle
Address	1…1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1…1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1…1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read inc.	1…1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

There are two frames required for either a read or a write access to the registers. The first frame provides the address for the register to be accessed. The second frame contains data to be written to the register in a write operation, or the contents of the register read in a read operation.

Indirect Addressing supports a Post Read Increment operation where the register address needs to be provided only once. The Management Interface logic increments the internal pointer at the end of a read operation and provides data from the next register when a read operation is performed. Description of the management interface fields is in Table 13.

Table 13 Indirect Addressing Management Frame Descriptions

Name	Field	Description
PRE	Preamble	At the beginning of each read or write operation, the station management entity sends a pattern that the PHY can use to establish synchronization. The Preamble consists of 32 contiguous logic 1 bits

Name	Field	Description
		on MDIO with 32 corresponding cycles on MDC. The PHY must observe this sequence before it will respond to any transaction.
ST	Start of Frame	The <00> pattern indicates a Start-of-Frame.
OP	Op Code	The operation code for an address transaction is <00>, a read transaction is <11>, post read increment is <10> and a write transaction is <01>.
PRTAD	Port Address	The value on PRTAD has to match the pin strapping of the PRTVAD[4:0] pins in order for the device to respond.
DEVICE_ID	PHY Device Address	This field is programmable to enable the device to be sensitive to any or all of the following: PMA/PMD, PCS, PHY XS, DTE XS and vender specific MMDs. (note the device can respond to frames with the WIS device ID, however, the QuadPHY XR is not used as WIS device)
TA	Turn-around	The turnaround time is a 2-bit time spacing between the register address field and the data field of a management frame to avoid contention during a read transaction. During a read transaction, both the CPU and the QuadPHY XR remain in a high-impedance state for the first bit time of the turnaround, and the QuadPHY XR drives a logic 0 during the second bit time of the turnaround. During a write transaction, the CPU drives a logic 1 for the first bit time of the turnaround and a 0 bit for the second bit time of the turnaround.
DATA / ADDRESS	Data	The data / address field is sixteen bits. The first data bit transmitted and received is bit 15 of the register being addressed.
IDLE	Idle	The IDLE condition on *MDIO* is a high-impedance state. The 3-state driver is disabled.

10.6 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The QuadPHY XR identification code is 0x083570CD hexadecimal.

11 Register Memory Map

Table 14 Register Memory Map

	Address	Register Description
MMD	**0x0000 – 0x0019**	**PMA/PMD, PCS, PHY XS MDIO Manageable Device Register Space**
1	0x0000	QuadPHY XR PMA/PMD Control 1
1	0x0001	QuadPHY XR PMA/PMD Status 1
1	0x0002	QuadPHY XR PMA/PMD Device Identifier 1
1	0x0003	QuadPHY XR PMA/PMD Device Identifier 2
1	0x0004	QuadPHY XR PMA/PMD Speed Ability
1	0x0005	QuadPHY XR PMA/PMD Devices in Package 1
1	0x0006	QuadPHY XR PMA/PMD Devices in Package 2
1	0x0007	QuadPHY XR PMA/PMD control 2
1	0x0008	QuadPHY XR PMA/PMD status 2
1	0x0009	QuadPHY XR PMD transmit disable
1	0x000A	QuadPHY XR PMD signal detect
1	0x000E	QuadPHY XR PMA/PMD Package Identifier 1
1	0x000F	QuadPHY XR PMA/PMD Package Identifier 2
3	0x0000	QuadPHY XR PCS Control 1
3	0x0001	QuadPHY XR PCS Status 1
3	0x0002	QuadPHY XR PCS Device Identifier 1
3	0x0003	QuadPHY XR PCS Device Identifier 2
3	0x0004	QuadPHY XR PCS Speed Ability
3	0x0005	QuadPHY XR PCS Devices in Package 1
3	0x0006	QuadPHY XR PCS Devices in Package 2
3	0x0008	QuadPHY XR PCS status 2
3	0x000E	QuadPHY XR PCS Package Identifier 1
3	0x000F	QuadPHY XR PCS Package Identifier 2
3	0x0018	QuadPHY XR PCS lane status register
3	0x0019	QuadPHY XR PCS test control
4	0x0000	QuadPHY XR PHY XS Control 1
4	0x0001	QuadPHY XR PHY XS Status 1
4	0x0002	QuadPHY XR PHY XS Device Identifier 1
4	0x0003	QuadPHY XR PHY XS Device Identifier 2
4	0x0004	QuadPHY XR PHY XS Speed Ability
4	0x0005	QuadPHY XR PHY XS Devices in Package 1
4	0x0006	QuadPHY XR PHY XS Devices in Package 2
4	0x0008	QuadPHY XR PHY XS status 2
4	0x000A	QuadPHY XR PHY XS signal detect

	Address	Register Description
4	0x000E	QuadPHY XR PHY XS Package Identifier 1
4	0x000F	QuadPHY XR PHY XS Package Identifier 2
4	0x0018	QuadPHY XR PHY XS lane status register
4	0x0019	QuadPHY XR PHY XS test control

For MDIO register addresses at and above 0xD000, accesses can be made using any MMD for which the corresponding DEV_ID bit in registers 0xD009, 0xD00A is logic 1. By default, bits 1,3 and 4 of DEV_ID[31:0] are 1. Registers at addresses at and above 0xD000 can be accessed with any MMD, irrespective of the DEV_ID bits in registers 0xD009, 0xD00A.

0xD000 – 0xD00C	QuadPHY XR Master Register Space
0xD000	Master Identity, and Global Performance Monitor Update
0xD001	Master Reset, and Configuration 1
0xD002	Master Configuration 2
0xD003	Master Receive Fault Configuration
0xD004	Master Port A Receive Fault Configuration/Monitor
0xD005	Master Port B Receive Fault Configuration/Monitor
0xD006	Master Register Port Status
0xD007	Master Port A Receive Fault Status
0xD008	Master Port B Receive Fault Status
0xD009	Master MDIO Device ID 1
0xD00A	Master MDIO Device ID 2
0XD00C	Master Register Port Status
0xD020 –0xD03F 0xD040 – 0xD05F	Analog Transmit and Receive Register space
0xD020, 0xD028, 0xD030, 0xD038	Port A Channel Lanes 0-3 Analog Transmit Configuration/Monitor 1
0xD021, 0xD029, 0xD031, 0xD039	Port A Channel Lanes 0-3 Analog Transmit Configuration 2
0xD025, 0xD02D, 0xD035, 0xD03D	Port A Channel Lanes 0–3 Analog Receive Configuration 4
0xD040, 0xD048, 0xD050, 0xD058	Port B Channel Lanes 0-3 Analog Transmit Configuration/Monitor 1
0xD041, 0xD049, 0xD051, 0xD059	Port B Channel Lanes 0-3 Analog Transmit Configuration 2
0xD045, 0xD04D, 0xD055, 0xD05D	Port B Channel Lanes 0–3 Analog Receive Configuration 4
0xD057 top 0xD07F	Reserved
0xD080 – 0xC0A7	Cross Bar Register Space
0xD080	XC16 Control
0xD081	XC16 Switch Enable
0xD082	XC16 Busy
0xD083	XC16 IDLE Compare 0
0xD084	XC16 IDLE Compare 1

0xD085	XC16 IDLE Compare 2
0xD086	XC16 IDLE Compare 3
0xD087	XC16 IDLE TX
0xD088	XC16 Lane Reset
0xD089	XC16 Terminate Control Character 0
0xD08A	XC16 Terminate Control Character 1
0xD08B to 0xD093	Reserved
0xD094, 0xD095, 0xD096, 0xD097	XC16 Standby
0xD098, 0xD099, 0xD09A, 0xD09B, 0xD09C, 0xD09E, 0xD09F	Reserved
, 0xD0A4, 0xD0A5, 0xD0A6, 0xD0A7	XC16 Standby Active
0xD0A8, 0xD0A9, 0xD0AA, 0xD0AB, 0xD0AC, 0xD0AE, 0xD0AF	Reserved
0xD0B0 – 0xC0B7	**Analog Clock Synthesis Unit Register Space**
0xD0B0	CSU Configuration and Status Registers
0xD0B1	CSU Monitor and Interrupt Status Registers
0xD0B8 top 0xD0FF	Reserved
0xD100 – 0xD17C 0xD200 – 0xD27C	**Receive 10G Ethernet/Fibre Channel Register Space**
0xD100, 0xD200	REFX Port A/Port B Global Control
0xD101, 0xD201	REFX Port A/Port B Global Monitor
0xD102, 0xD202	REFX Port A/Port B PGC Threshold
0xD103, 0xD203	REFX Port A/Port B PGC Packet and Idle Length
0xD104, 0xD204	REFX Port A/Port B 8B/10B Code Error Threshold
0xD105, 0xD205	REFX Port A/Port B Packet Counter Control
0xD106, 0xD206	REFX Port A/Port B Trunked Inserted Column Count
0xD107, 0xD207	REFX Port A/Port B Trunked Deleted Column Count
0xD108, 0xD208	REFX Port A/Port B Interrupt Enable 1
0xD109, 0xD209	REFX Port A/Port B Interrupt Enable 2
0xD10A, 0xD20A	REFX Port A/Port B Interrupt Enable 3
0xD10B, 0xD20B	REFX Port A/Port B Interrupt Status 1
0xD10C, 0xD20C	REFX Port A/Port B Interrupt Status 2
0xD10D, 0xD20D	REFX Port A/Port B Interrupt Status 3
0xD10E, 0xD20E	REFX Port A/Port B Status 1
0xD10F, 0xD20F	REFX Port A/Port B Status 2
0xD110, 0xD210	REFX Port A/Port B Status 3
0xD119, 0xD219	REFX TIP Mask
0xD140, 0xD150,	REFX Port A Lanes 0-3 and Port B Lanes 0-3 Control

0xD160, 0xD170, 0xD240, 0xD250, 0xD260, 0xD270	
0xD141, 0xD151, 0xD161, 0xD171, 0xD241, 0xD251, 0xD261, 0xD271	REFX Port A Lanes 0-3 and Port B Lanes 0-3 Monitor
0xD142, 0xD152, 0xD162, 0xD172, 0xD242, 0xD252, 0xD262, 0xD272	REFX Port A Lanes 0-3 and Port B Lanes 0-3 PGC Control
0xD143, 0xD153, 0xD163, 0xD173, 0xD243, 0xD253, 0xD263, 0xD273	REFX Port A Lanes 0-3 and Port B Lanes 0-3 PGC Error Count
0xD144, 0xD154, 0xD164, 0xD174, 0xD2144, 0xD2154, 0xD2164, 0xD2174	REFX Port A Lanes 0-3 and Port B Lanes 0-3 8B/10B Error Count
0xD145, 0xD155, 0xD165, 0xD175, 0xD245, 0xD255, 0xD265, 0xD275	REFX Port A Lanes 0-3 and Port B Lanes 0-3 Packet Error Count
0xD146, 0xD156, 0xD166, 0xD176, 0xD246, 0xD256, 0xD266, 0xD276	REFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count MSW
0xD147, 0xD157, 0xD167, 0xD177, 0xD247, 0xD257, 0xD267, 0xD277	REFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count LSW
0xD300 – 0xD33F 0xD400 – 0xD43F	**Transmit 10G Ethernet/Fibre Channel Register Space**
0xD300, 0xD400	TEFX Port A/Port B Global Control
0xD301, 0xD401	TEFX Port A/Port B Global Diagnostic
0xD302, 0xD402	TEFX Port A/Port B Packet Counter Control
0xD303, 0xD403	TEFX Port A/Port B Interrupt Enable
0xD304, 0xD404	TEFX Port A/Port B Interrupt Status
0xD305, 0xD405	TEFX Port A/Port B Status
0xD320, 0xD328, 0xD330, 0xD338, 0xD420, 0xD428, 0xD430, 0xD438	TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Control
0xD321, 0xD329, 0xD331, 0xD339, 0xD421, 0xD429, 0xD431, 0xD439	TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Control and Diagnostic
0xD322, 0xD32A, 0xD332, 0xD33A, 0xD422, 0xD42A, 0xD432, 0xD43A	TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count LSW

0xD323, 0xD32B, 0xD333, 0xD33B, 0xD423, 0xD42B, 0xD433, 0xD43B	TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count MSW
0xD324, 0xD32C, 0xD334, 0xD33C, 0xD424, 0xD42C, 0xD434, 0xD43C	TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Error Packet Count

Notes on Register Memory Map:

1. Addresses that are not shown must be treated as Reserved.

12 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the QuadPHY XR. These registers are accessed by default through the standard PMA/PMD, PCS and PHY XS MMD numbers 1,3 and 4. For the following section, if the contents at a given address are dependent on the MMD access, the register at this address will be separately described for these different MMDs. If the register contents do not depend on the MMD access, the register is described once only.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the QuadPHY XR to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect QuadPHY XR operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with mega-cell functions that are unused in this application. To ensure that the QuadPHY XR operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Register 0x0000: PHY XS, PMA/PMD, PCS Control 1

Bit	Type	Function	Default
15	R/W	RESET	0
14	R/W	LOOPBACK	0
13	R	SPEED_SEL	1
12	R	Reserved	X
11	R/W	LOW_PWR	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	SPEED_SEL	1
5	R	SPEED_SEL	0
4	R	SPEED_SEL	0
3	R	SPEED_SEL	0
2	R	SPEED_SEL	0
1	R	Reserved	0
0	R/W	PMA_LOOPBACK	0

PMA_LOOPBACK

This bit is available via only PMA/PMD. The PMA_LOOPBACK bit enables a loopback of serial data that has been presented at PHY XS input ports back to PHY XS output ports. When the PMA_LOOPBACK bit is set to a one, data presented at *DLnA_P/N*. input pins is internally looped back and presented at *SLnA_P/N*. output pins. This internal loopback of serial encoded data occurs within the PMA/PMD . The output port *SLnB_P/N*. of the PMA/PMD is unaffected by the operation of this loopback. If the *EN_SLPBK_B* input pin is a logic 1, this loopback will be active and the PMA_LOOPBACK bit will be ignored.

SPEED_SEL

The Speed selection bits 13 and 6 must be written with a one. Any attempt to change these bits to an invalid setting will be ignored. These two bits are set to one in order to make them compatible with Clause 22 of the IEEE 802.3ae. Non-zero values for SPEED_SEL bits 5 through 2 are reserved, these bits must always be written with 0.

SPEED_SEL[3:0]	**Function**
1 x x x	Reserved
x 1 x x	Reserved
x x 1 x	Reserved

0 0 0 1	Reserved
0 0 0 0	10 Gbit/s

LOW_PWR

The QuadPHY XR will be placed into low power mode by setting LOW_PWR to a logic 1. In this mode, the digital and analog circuitry is disabled for this port, thus minimizing its power consumption. The MDIO interface will still be active while in low power mode. The low power mode is exited by resetting the device. No interface signals to the QuadPHY XR should be relied upon when this bit is active. A read of this bit will reflect the current state of the internal low power signal, and therefore may not reflect the last value written to this bit.

LOOPBACK

This bit is available via PCS or PHY XS accesses.

For PCS access, the LOOPBACK bit enables a loopback of serial data that has been presented at PHY XS input ports back to PHY XS output ports. When the LOOPBACK bit is set to a one, data presented at *DLnA_P/N*. input pins is internally looped back and presented at *SLnA_P/N*. output pins. This internal loopback of serial encoded data occurs within the PCS. The output port *SLnB_P/N*. of the PCS is unaffected by the operation of this loopback. If the *EN_SLPBK_B* input pin is a logic 1, this loopback will be active and the LOOPBACK bit will be ignored.

For PHY XS access, the LOOPBACK bit enables a loopback of serial data that has been presented at PMA/PMD input ports back to PMA/PMD output ports. When the LOOPBACK bit is set to a one, data presented at *DLnB_P/N* input pins is internally looped back and presented at *SLnB_P/N*. output pins. This internal loopback of serial encoded data occurs within the PHY XS . The output port *SLnA_P./N*. of the PHY XS is unaffected by the operation of this loopback. If the *EN_SLPBK_A* input pin is logic 1, the serial loopback will be active and the device will ignore the LOOPBACK bit.

RESET

Resetting the QuadPHY XR is accomplished by setting this bit to a one. This action sets all MMD registers to their default states. As a consequence, this action may change the internal state of the MMD and the state of the physical link. This bit is self-clearing and will return a logic 1 when a reset is in progress and a logic 0 otherwise. The QuadPHY XR will not accept a write transaction to any of its registers until the reset process is completed. The reset process will be completed within the 0.5s from the setting of the bit. During this reset, the QuadPHY XR will respond to reads from this register bit and register bits [15:14] in register 0x0008 or 0xC008. All other register accesses will be ignored. This operation may interrupt data communication.

Register 0x0001: PHY XS, PMA/PMD, PCS Status 1

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	FAULT	-
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
4	R	Reserved	0
2	R	LINK_STAT	-
1	R	LOW_PWR_ABILITY	1
0	R	Reserved	0

LOW_PWR_ABILITY

When read as a logic 1, LOW_PWR_ABILITY indicates that low power feature is supported, low power is unsupported otherwise. The low power feature is controlled using the LOW_PWR bit in register 0x0000.

LINK_STAT

When read logic 1, the LINK_STAT bit indicates that the MMD's receive link is aligned, the link is unaligned otherwise. This bit is a latching low version of the LANE_ALIGN_STAT bit in register 0x0018.

FAULT

When read as a logic 1, the device has detected a fault condition on either the transmit or receive paths as they apply to each of the devices, the device has not detected a fault condition otherwise. The FAULT bit is set to a logic 1 when either the TX_FAULT or RX_FAULT bits in Register 0x0008 is set to a logic 1.

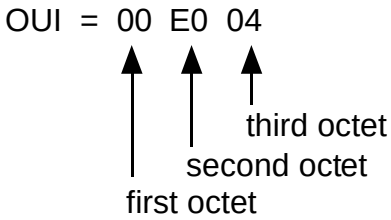
Register 0x0002: PHY XS, PMA/PMD, PCS Device Identifier 1

Bit	Type	Function	Default
15	R	CHIPID[31]	0
14	R	CHIPID[30]	0
13	R	CHIPID[29]	0
12	R	CHIPID[28]	0
11	R	CHIPID[27]	0
10	R	CHIPID[26]	0
9	R	CHIPID[25]	0
8	R	CHIPID[24]	0
7	R	CHIPID[23]	0
6	R	CHIPID[22]	0
5	R	CHIPID[21]	0
4	R	CHIPID[20]	1
3	R	CHIPID[19]	1
2	R	CHIPID[18]	1
1	R	CHIPID[17]	0
0	R	CHIPID[16]	0

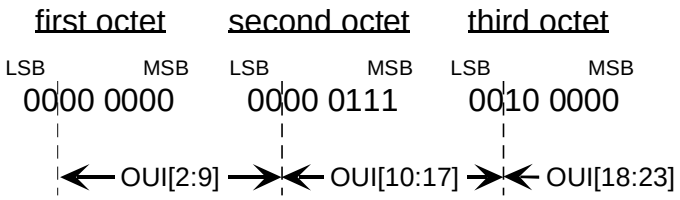
The Device Identifier 1 register contains bit 3 through 18 of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE. This PHY Identifier is intended to provide sufficient information to support the ResourceTypeID object as required in *IEEE* Standard 802.3, Section 30.1.2.

CHIPID[31:16]

The CHIPID[31:16] bits contain bits 3 through 18 of the Organizationally Unique Identifier (OUI). The bit 3 of the OUI is assigned to CHIPID[31], the 4th bit of the OUI is assigned to CHIPID[30], and so on. Bit CHIPID[16] contains the 18th bit of the OUI. The default setting for CHIPID[31:16] is 0x001Ch.



Each octet is represented as a conventional two digit hexadecimal numeral where the first (left-most) digit of the pair is the more significant. The mapping of the OUI to the GMII CHIPID registers of the QuadPHY-XR is described below.



CHIP Identifier1 [31:16]=OUI[2:17] = 001C

CHIP Identifier2 [15:10] = OUI[18:23] = 20

Register 0x0003: PHY XS, PMA/PMD, PCS Device Identifier 2

Bit	Type	Function	Default
15	R	CHIPID[15]	0
14	R	CHIPID[14]	0
13	R	CHIPID[13]	1
12	R	CHIPID[12]	0
11	R	CHIPID[11]	0
10	R	CHIPID[10]	0
9	R	CHIPID[9]	0
8	R	CHIPID[8]	0
7	R	CHIPID[7]	0
6	R	CHIPID[6]	1
5	R	CHIPID[5]	1
4	R	CHIPID[4]	1
3	R	CHIPID[3]	0
2	R	CHIPID[2]	0
1	R	CHIPID[1]	0
0	R	CHIPID[0]	0

The Device Identifier 2 register contains the 19th through 24th bits of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE, the 6 bit Manufacturing Model Number and the 4 bit Revision Number.

CHIPID[3:0]

CHIP[3:0] contain the 4 bit Revision Number of the QuadPHY XR. The default setting for these bits change with device revision. The revision number for Revision A of the QuadPHY XR is 0x00.

CHIPID[9:4]

CHIPID[9:4] contain the 6 bit Manufacturing Model Number. The default setting for these bits is 0x07

CHIPID[15:10]

CHIPID[15:10] contain the 19th through 24th bits of the Organizationally Unique Identifier (OUI). The default setting for these bits is 0x08.

Register 0x0004: PHY XS, PMA/PMD, PCS Speed Ability

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
3	R	Reserved	0
2	R	Reserved	0
1	R	Reserved	0
0	R	10G_CAPABLE	1

10G_CAPABLE

When read as a logic 1 the device is able to operate at a data rate of 10 Gbit/s, the device is not able to operate at this data rate otherwise.

Register 0x0005: PHY XS, PMA/PMD, PCS Devices in Package 2

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	DTE_XS_PRES	0
4	R	PHY_XS_PRES	1
3	R	PCS_PRES	1
2	R	WIS_PRES	0
1	R	PMA_PMD_PRES	1
0	R	Reserved	0

Note:

1. The QuadPHY XR will optionally respond to any of the 32 MMDs, as outlined in IEEE 802.3ae. The Devices in Package register reflects the default application of the QuadPHY XR.

PMA_PMD_PRES

When read as a 1, the PMA_PMD_PRES bit indicates that the PMA/PMD MMD is instantiated in the QuadPHY XR package. When read as a 0, the PMA_PMD_PRES bit indicates that the PMA/PMD is not is instantiated in the QuadPHY XR package

WIS_PRES

When read as a 1, the WIS_PRES bit indicates that the WIS MMD is instantiated in the QuadPHY XR package. When read as a 0, the WIS_PRES bit indicates that the WIS is not is instantiated in the QuadPHY XR package.

PCS_PRES

When read as a 1, the PCS_PRES bit indicates that the PCS MMD is instantiated in the QuadPHY XR package. When read as a 0, the PCS_PRES bit indicates that the PCS is not is instantiated in the QuadPHY XR package.

PHY_XS_PRES

When read as a 1, the PHY_XS_PRES bit indicates that the PHY_XS MMD is instantiated in the QuadPHY XR package. When read as a 0, the PHY_XS_PRES bit indicates that the PHY_XS is not is instantiated in the QuadPHY XR package.

DTE_XS_PRES

When read as a 1, the DTE_XS_PRES bit indicates that the DTE_XS MMD is instantiated in the QuadPHY XR package. When read as a 0, the DTE_XS_PRES bit indicates that the DTE_XS is not is instantiated in the QuadPHY XR package.

Register 0x0006: PHY XS, PMA/PMD, PCS Devices in Package 1

Bit	Type	Function	Default
15	R	VEN_SPECIFIC_2_PRES	0
14	R	VEN_SPECIFIC_1_PRES	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
3	R	Reserved	0
2	R	Reserved	0
1	R	Reserved	0
0	R	Reserved	0

VEN_SPECIFIC_1_PRES

When read as a logic 1, a vender specific device 1 MMD is instantiated in the QuadPHY XR package. When read as a logic 0, a vender specific device 1 MMD is not instantiated in the QuadPHY XR package.

VEN_SPECIFIC_2_PRES

When read as a logic 1, a vender specific device 2 MMD is instantiated in the QuadPHY XR package. When read as a logic 0, a vender specific device 2 MMD is not instantiated in the QuadPHY XR package.

Register 0x0007: PMA/PMD, PCS Control 2

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
3	R	Reserved	0
2	R/W	PMA_PMD_TYPE[2]	0
1	R/W	PMA_PMD_TYPE[1]/PCS_TYPE[1]	0
0	R/W	PMA_PMD_TYPE[0]/PCS_TYPE[1]	0/1

PMA_PMD_TYPE[2:0]

On PMA PMD accesses, reads of and writes to these bits will present and affect PMA PMD type selection as per IEEE P802.3 section 45. The default value for PMA PMD type selection is 0’b100, which selects for 10GBASE-LX4 PMA/PMD type.

PCS_TYPE[1:0]

On PCS accesses, reads of and writes to these bits will present and affect PCS type selection as per IEEE P802.3 section 45. The default value for PCS type selection is 0’b001, which selects for 10GBASE-X PCS type.

Register 0x0008: PHY XS, PMA/PMD, PCS Status 2

Bit	Type	Function	Default
15	R	DEV_PRES[1]	1
14	R	DEV_PRES[0]	0
13	R	PMA_TX_FAULT_ABILITY	-
12	R	PMA_RX_FAULT_ABILITY	-
11	R	TX_FAULT	-
10	R	RX_FAULT	-
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
3	R	Reserved	0
2	R	Reserved	0
1	R	PCS_10GBASE_X_CAPABLE	1
0	R	PMA_LOOBACK_ABILITY	-

PMA_LOOBACK_ABILITY

The QuadPHY XR supports PMA loopback, on PMA/PMD accesses this bit will read as logic 1, otherwise this bit will read as logic 0.

PCS_10GBASE_X_CAPABLE

The QuadPHY XR supports 10GBASE-X PCS type, on PCS accesses this bit will read as logic 1, otherwise this bit will read as logic 0.

RX_FAULT

The significance of this bit depends on whether this register is accessed as a PMA/PMD PCS device, or as a PHY XS device. For PMA/PMD or PCS accesses, RX_FAULT indicates that a fault condition has been detected on the RX path within the PMA/PMD or PCS devices. For PHY XS accesses RX_FAULT indicates a fault condition on the TX path within the PHY XS device. RX_FAULT is a logical OR of an internal receive FIFO error, loss of signal from the optics (as reflected in the *SD_A* or *SD_B* input pins), digital transition detect, and DRU loss of sync. Once active, RX_FAULT will remain so until this bit is read. Once such a read has occurred, the value of this bit will be based on the current state of the condition it monitors.

Since this bit is shared across all MMD space, a valid read of this bit from any type of MMD access may clear this bit.

TX_FAULT

The significance of this bit depends on whether this register is accessed as a PMA/PMD PCS device, or as a PHY XS device. For PMA/PMD or PCS accesses, TX_FAULT indicates that a fault condition has been detected on the TX path within the PMA/PMD or PCS devices. For PHY XS accesses TX_FAULT indicates a fault condition on the RX path within the PHY XS device. TX_FAULT is a logic OR of an internal transmit FIFO error or a loss of lock by the internal CSU block. Once active, TX_FAULT will remain so until this bit is read. Once such a read has occurred, the value of this bit will be based on the current state of the condition it monitors.

Since this bit is shared across all MMD space, a valid read of this bit from any type of MMD access may clear this bit.

DEV_PRES [1:0]

The DEV_PRES[1:0] bits indicates that this MMD of the QuadPHY XR device is not present at this register address or not functioning properly according to the following:

DEV_PRES[1:0]	**Device status**
10	Device responding at this address
11	No device responding at this address
01	No device responding at this address
00	No device responding at this address

Register 0x0009: PMD Transmit Disable

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	PMD TX1 DISABLE	0
3	R	PMD TX2 DISABLE	0
2	R	PMD TX3 DISABLE	0
1	R	PMD TX4 DISABLE	0
0	R	GLOBAL PMD TX DISABLE	0

PMD TXn DISABLE, GLOBAL_PMD_TX_DISABLE

These read only bits will always read as ‘0’. The QuadPHY GX does not support PMD transmit disable

Register 0x000A: PMD Receive Signal Detect

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	RX3 SIGNAL DETECT	-
3	R	RX2 SIGNAL DETECT	-
2	R	RX1 SIGNAL DETECT	-
1	R	RX0 SIGNAL DETECT	-
0	R	GLOBAL_RX SIGNAL DETECT	-

RXn SIGNAL_DETECT, GLOBAL_RX_SIGNAL_DETECT

By default, these read only bits reflects the value on either the *SD_B* or *SD_A* pins. If SD_INF_B or SD_INV_A bits of register 0xD003 are logical '1', then these read only bits reflect the logical inverse of the value on the *SD_B* or *SD_A* pin respectively. The *SD_B* pin is presented when this register is accessed as a PMA/PMD device. The *SD_A* pin is presented when this register is accessed as a PHY XS device.

Register 0x0000A is not a standard PHY XS device register but is provided for software visibility of the SD_A pin.

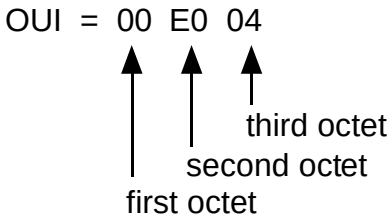
Register 0x000E: PHY XS, PMA/PMD, PCS Package Identifier 1

Bit	Type	Function	Default
15	R	PACK_ID[31]	0
14	R	PACK_ID[30]	0
13	R	PACK_ID[29]	0
12	R	PACK_ID[28]	0
11	R	PACK_ID[27]	0
10	R	PACK_ID[26]	0
9	R	PACK_ID[25]	0
8	R	PACK_ID[24]	0
7	R	PACK_ID[23]	0
6	R	PACK_ID[22]	0
5	R	PACK_ID[21]	0
4	R	PACK_ID[20]	1
3	R	PACK_ID[19]	1
2	R	PACK_ID[18]	1
1	R	PACK_ID[17]	0
0	R	PACK_ID[16]	0

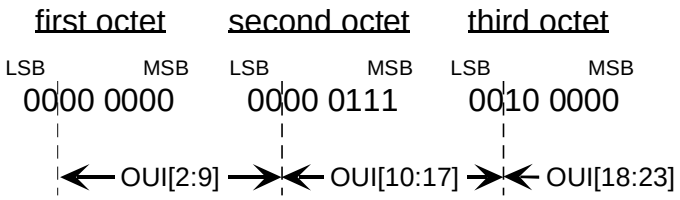
The PackageIdentifier 1 register contains bit 3 through 18 of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE. This PHY Identifier is intended to provide sufficient information to support the ResourceTypeID object as required in *IEEE* Standard 802.3, Section 30.1.2.

PACK_ID[31:16]

The PACK_ID[31:16] bits contain bits 3 through 18 of the Organizationally Unique Identifier (OUI). The bit 3 of the OUI is assigned to PACK_ID[31], the 4th bit of the OUI is assigned to PACK_ID[30], and so on. Bit PACK_ID[16] contains the 18th bit of the OUI. The default setting for PACK_ID[31:16] is 0x001Ch.



Each octet is represented as a conventional two digit hexadecimal numeral where the first (left-most) digit of the pair is the more significant. The mapping of the OUI to the GMII PACK_ID registers of the QuadPHY-XR is described below.



PACK Identifier1 [31:16]=OUI[2:17] = 001C

PACK Identifier2 [15:10] = OUI[18:23] = 20

Register 0x000F: PHY XS, PMA/PMD, PCS Package Identifier 2

Bit	Type	Function	Default
15	R	PACK_ID[15]	0
14	R	PACK_ID[14]	0
13	R	PACK_ID[13]	1
12	R	PACK_ID[12]	0
11	R	PACK_ID[11]	0
10	R	PACK_ID[10]	0
9	R	PACK_ID[9]	0
8	R	PACK_ID[8]	0
7	R	PACK_ID[7]	0
6	R	PACK_ID[6]	1
5	R	PACK_ID[5]	1
4	R	PACK_ID[4]	1
3	R	PACK_ID[3]	0
2	R	PACK_ID[2]	0
1	R	PACK_ID[1]	0
0	R	PACK_ID[0]	0

The Package Identifier 2 register contains the 19th through 24th bits of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE, the 6 bit Manufacturing Model Number and the 4 bit Revision Number.

PACK_ID[3:0]

PACK_ID[3:0] contain the 4 bit Revision Number of the QuadPHY XR. The default setting for these bits change with device revision. The revision number for Revision A of the QuadPHY XR is 0x00.

PACK_ID[9:4]

PACK_ID[9:4] contain the 6 bit Manufacturing Model Number. The default setting for these bits is 0x07

PACK_ID[15:10]

PACK_ID[15:10] contain the 19th through 24th bits of the Organizationally Unique Identifier (OUI). The default setting for these bits is 0x08.

Register 0x0018: PHY XS, PCS Lane Status Register

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	LANE_ALIGN_STAT	-
Bit 11	R	PATT_TEST_ABILITY	1
Bit 10	R	LOOPBACK_ABILITY	-
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	LANE_3_SYNC	-
Bit 2	R	LANE_2_SYNC	-
Bit 1	R	LANE_1_SYNC	-
Bit 0	R	LANE_0_SYNC	-

LANE_0_SYNC

For PMA/PMD or PCS accesses a logic 1 in this bit position signifies that comma detection has succeeded on the input lane *DL0B_P/N*, and hence synchronization has been achieved for this lane. Synchronization has not been achieved for this lane otherwise.

For PHY XS accesses a logic 1 in this bit position signifies that comma detection has succeeded on the input lane *DL0A_P/N*, and hence synchronization has been achieved for this lane. Synchronization has not been achieved for this lane otherwise.

LANE_1_SYNC

This bit behaves identically to LANE_0_SYNC but applies to lane 1.

LANE_2_SYNC

This bit behaves identically to LANE_0_SYNC but applies to lane 2.

LANE_3_SYNC

This bit behaves identically to LANE_0_SYNC but applies to lane 3.

LOOPBACK_ABILITY

As a PHY XS, PMA/PMD, or a PCS device, when LOOPBACK_TEST_ABILITY is read a logic 1, the device is able to generate the loopback functionality as specified in Register 0x0000. If this bit is read as a logic 0, it is not able to perform this loopback function.

PATT_TEST_ABILITY

When PATT_TEST_ABILITY is read as a logic 1, the device is able to generate test patterns as controlled in Register 0x0019. If this bit is read as a logic 0, is not able to generate test patterns.

LANE_ALIGN_STAT

For PMA/PMD or PCS accesses a logic 1 in this bit position signifies that lane to lane has been achieved across the input lanes DLnB_N/P. Alignment has not been achieved across these lanes otherwise.

For PHY XS accesses a logic 1 in this bit position signifies that lane to lane alignment has been acheived across the input lanes DLnA_N/P. Alignment has not been achieved across these lanes otherwise.

Register 0x0019: PHY XS, PCS Test Control

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
3	R	Reserved	0
2	R/W	TX_TEST_PATT_EN	0
1	R/W	TX_TEST_PATT_SEL[1]	0
0	R/W	TX_TEST_PATT_SEL[0]	0

TX_TEST_PATT_SEL[1:0]

For PMA/PMD or PCS accesses, these bits apply to the outputs *SLnB_P/N*. For PHY XS accesses these bits apply to the ouputs *SLnA_P/N*.

The test pattern select bits are used to select the type of test pattern transmitted. The description of the these bits are summarized in the following table.

TX_TEST_PATT_SEL[1:0]	Device status
11	Reserved
10	Mixed frequency test pattern
01	Low frequency test pattern
00	High frequency test pattern

Please refer to Annex 48A of the IEEE 802.3ae standard for definitions of these patterns.

TX_TEST_PATT_EN

For PMA/PMD or PCS accesses, this bit affects the outputs *SLnB_.P/N* For PHY XS accesses this bit affects to the outputs *SLnA_.P/N*

The transmit test pattern enable bit controls the insertion of test patterns on a high speed serial transmit interface. When TX_TEST_PATT_EN is a logic 1, test pattern transmission is enabled, test pattern transmission is disabled otherwise.

Register 0xD000: Master Identity and Global Performance Monitor Update

Bit	Type	Function	Default
15	/W	TIP	0
14		Unused	X
13		Unused	X
12	R/W	SW_CONFIG	0
11	R/W	ANALOG_CTRL	0
10	R	Reserved	0
9	R/W	SYSCLK_EN	0
8	R	TYPE[4]	0
7	R	TYPE[3]	0
6	R	TYPE[2]	0
5	R	TYPE[1]	0
4	R	TYPE[0]	1
3	R	REVCODE[3]	0
2	R	REVCODE[2]	0
1	R	REVCODE[1]	0
0	R	REVCODE[0]	0

This register allows the revision number of the QuadPHY XR to be read by software permitting graceful migration to newer, feature-enhanced versions of the QuadPHY XR.

REVCODE [3:0]

The REVCODE bits can be read to provide a binary QuadPHY XR revision number.

REVCODE [3:0]	Revision
0000	A
0001	B
0010	C

TYPE[4:0]

The TYPE bits can be read to distinguish the QuadPHY XR from the other members of the family of devices. The TYPE[4:0] register for the PM8357 is 0001.

SYSCLK_EN

Sysclk Enable. When SYSCLK_EN is a logic 1, the *SYSCLK* output pin carries the divided down CSU core clock for monitoring and retiming external devices. When SYSCLK_EN is a logic 0, the SYSCLK output is held in tri-state.

ANALOG_CTRL

The ANALOG_CTRL bit determines how equalization, pre-emphasis and output swing levels on the *DLnA_P, DLnA_N, DLnB_ P, DLnB_N, SLnA_P, SLnA_N, SLnB_P* and *SLnB_N* high speed serial data I/O are programmed

When ANALOG_CTRL is a logic 1, the configuration of these features is determined by the TX_MODE[4:0], PISO_MODE[3] and RX_MODE[1:0] register bits in the Analog Transmit and Receive Register space.

When ANALOG_CTRL is a logic 0, the configuration of these features is determined by the *EN_PRE-EMPHASIS, EN_EQUALIZATION* and *HC[1:0]* input configuration pins. The following vectors are set directly to the analog blocks :

EN_PRE-EMPHASIS	HC[1:0]	TX_MODE[4:0]	PISO_MODE[3]	Comments
0	00	01010	0	No pre-emphasis, min swing
0	01	01101	0	No pre-emphasis
0	10	10000	0	No pre-emphasis
0	11	10011	0	No pre-emphasis, max swing (XAUI compatible)
1	00	10000	1	XAUI with 1/0.46 (high/low) pre-emphasis
1	01	10010	1	XAUI with 1/0.56 (high/low) pre-emphasis
1	10	10100	1	XAUI with 1/0.66 (high/low) pre-emphasis
1	11	10110	1	XAUI with 1/0.76 (high/low) pre-emphasis

EN_EQUALIZATION	RX_MODE[1:0]	Comments
0	01	Half equalization
1	10	Full Equalization

SW_CONFIG

Software configuration. This bit is used to determine the method of configuration of device features.

When SW_CONFIG is logic 0, the device uses the hardware method for configuration. This method relies on device pins with XOR software override via the *_MON and *_SW register bits used throughout the device address space to configure the indented operation.

When SW_CONFIG is logic 1, the device uses the software method for configuration. This method ignores all device configuration pins, namely *FAILOVER, FAILOVER_IMM, , EN_SLPBK_A, EN_SLPBK_B, MODE_SEL[1:0], EN_PREEMPHASIS, HC[1:0] and EN_EQUALIZATION*. Global device configuration is achieved with *_SW bits directly in the Master Register Space. Per-lane XOR software override is achieved via the *_MON and *_SW register bits in the XC16 Register Space, REFX Register Space and TEFX register space. Both MUX_PRESET_TX_XAUI_A and MUX_PRESET_TX_XAUI_B register bits will have a default value of "00". Please refer to the Operations section for more information on software programmability.

TIP

The TIP bit is set to logic 1 when the performance meter registers are being loaded. Writing to this register, with the DRESET bit in register 0xD001 equal to logic 0, initiates an accumulation interval transfer and loads all the performance meter registers in the QuadPHY XR. TIP remains high while the transfer is in progress, and is set to logic 0 when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Register 0xD001: Master Reset and Configuration 1

Bit	Type	Function	Default
Bit 15	R/W	PLLE_A	0
Bit 14	R/W	MLLB_A	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	RCLE_A	0
Bit 11	R	FC_GEB_MODE_MON_A	-
Bit 10	R	TRNK_LNB_MODE_MON_A	-
Bit 9	R	8B10B_EN_MON_A	-
Bit 8	R/W	Reserved	0
Bit 7	R/W	FC_GEB_MODE_SW_A	0
Bit 6	R/W	TRNK_LNB_MODE_SW_A	0
Bit 5	R/W	8B10B_EN_SW_A	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	MREG_RESET	0
Bit 2	R/W	ARESET	0
Bit 1	R/W	DRESET	0
Bit 0	R/W	WCIMODE	0

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. In this mode of operation a logic 1 must be written to clear the active interrupt bit. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read. In this mode of operation the act of reading the active interrupt clears the bit. The WCIMODE bit effects the operation of all Interrupt Register Bits in the QuadPHY XR.

DRESET

The DRESET bit allows the digital circuitry in the QuadPHY XR to be reset under software control. If the DRESET bit is a logic 1, all the digital circuitry, except all the bits in the MMD, analog transmit and receive, and Master Registers, is held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the device out of reset. A hardware reset clears the DRESET bit, thus negating the digital software reset.

ARESET

The ARESET bit allows the analog circuitry in the QuadPHY XR to be reset under software control. If the ARESET bit is a logic 1, all the analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the device out of reset. A hardware reset clears the ARESET bit, thus negating the analog software reset.

MREG_RESET

The Master Register Reset. The MREG_RESET bit resets all master registers to their default values. If the MREG_RESET bit is a logic 1, all bits in the MMD, analog transmit and receive, and master register space except the MREG_RESET, ARESET, and DRESET of register 0xD001H are held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written in order to resume normal operation. A hardware reset clears the MREG_RESET bit, thus negating the digital software reset.

8B10B_EN_MON_A

Port A 8B/10B encoder/decoder enable monitor. The 8B10B_EN_MON_A bit reflects the internal state of the 8B10B encoder/decoder as realized by the *MODE_SEL[1:0]* input pins. A logic 1 on this bit indicates that the device is strapped for 8B10B encoding/decoding. A logic 0 on this bit indicates that the device is strapped for no 8B/10B processing. This bit is used in conjunction with the 8B10B_EN_SW_A bit to determine port A's behaviour. Further programmability in either the transmit or receive channel on a lane-by-lane basis within port A is available in the REFX and TEFX register space and will override the 8B10B_EN_MON_A and 8B10B_EN_SW_A register bits.

TRNK_LNB_MODE_MON _A

Port A Trunk/Lane based mode monitor. The TRNK_LNB_MODE_MON _A bit reflects the internal operation mode as realized by the *MODE_SEL[1:0]* input pins. A logic 1 on this bit indicates that the device is strapped for XAUI trunked mode of operation on port A. A logic 0 on this bit indicates that the device is strapped for lane-based mode of operation. This bit is used in conjunction with the TRNK_LNB_SW_A bit to determine port A's behaviour. Further programmability in either the transmit or receive channel within port A is available in the REFX and TEFX register space and will override the TRNK_LNB_MODE_MON _A and TRNK_LNB_MODE_SW _A register bits.

FC_GEB_MODE_MON _A

Port A 10GFC/10GbE mode monitor. The FC_GEB_MODE_MON _A bit reflects the internal operation mode as realized by the *MODE_SEL[1:0]* input pin pins. A logic 1 on this bit indicates that the device is strapped for 10 Gbit/s Fibre Channel mode of operation on port A. A logic 0 on this bit indicates that the device is strapped for 10 Gbit/s Ethernet of operation. This bit is used in conjunction with the FC_GEB_MODE_SW _A bit to determine port A's behaviour. Further programmability in either the transmit or receive channel within port A is available in the REFX and TEFX register space and will override the FC_GEB_MODE _MON _A and FC_GEB_MODE _SW _A register bits.

8B10B_EN_SW_A

Port A 8B/10B encoder/decoder enable software override. The 8B10B_EN_SW_A bit is used to program the 8B10B encoder/decoder. The value written to this bit is logically XOR'ed with the 8B10B_EN_MON_A to obtain the desired functionality. A logic 1 resulting from the XOR enables 8B10B encoding/decoding on port A. A logic 0 resulting from the XOR disables 8B/10B processing on port A. Further software programmability in either the transmit or receive channel on a lane-by-lane basis within port A is available in the REFX and TEFX register space and will override (8B10B_EN_MON_A) XOR (8B10B_EN_SW_A).

TRNK_LNB_MODE_SW_A

Port A Trunk/Lane based mode software override. The TRNK_LNB_MODE_SW _A bit is used to configure the operation of port A. The value written to this bit is logically XOR'ed with the TRNK_LNB_MODE_MON_A to obtain the desired functionality. A logic 1 resulting from the XOR configures the device for XAUI trunked mode of operation on port A. A logic 0 resulting from the XOR configures the device for lane-based mode of operation. Further programmability in either the transmit or receive channel within port A is available in the REFX and TEFX register space and will override (TRNK_LNB_MODE_MON _A) XOR (TRNK_LNB_MODE_SW _A).

FC_GEB_MODE_SW_A

Port A 10GFC/10GbE mode software override. The FC_GEB_MODE_SW _A bit is used to configure the operation of port A. The value written to this bit is logically XOR'ed with the FC_GEB_MODE _ MON_A to obtain the desired functionality. A logic 1 resulting from the XOR configures the device for 10 Gbit/s Fibre Channel mode of operation on port A. A logic 0 resulting from the XOR configures the device for 10 Gbit/s Ethernet of operation. Further programmability in either the transmit or receive channel within port A is available in the REFX and TEFX register space and will override (FC_GEB_MODE _MON _A) XOR (FC_GEB_MODE _SW _A).

RCLE_A

Port A Recovered Clock Loopback Enable. The RCLE_A bit is used to obtain the recovered clock derived from the high speed serial data path for each of the lanes in the device. When RCLE_A is logic 1, each of the *SLnA_P* and *SLnA_N* will transmit the locally derived clock from the associated *DLnA_P* and *DLnA_N* serial data inputs. When RCLE_A is a logic 0, the normal high speed transmit serial interface is preserved. Note that the RCLE_A bit is OR'ed with the 4 Channel RCLE_A bits in the Analog Transmit Configuration/Monitor 1 register to obtain the loopback for the 4 lanes in port A.

MLLB_A

Port A Metallic Line loopback. This bit is used to put the QuadPHY XR port A in a metallic loopback where the high speed serial receive data is immediately looped to the high speed transmit interface. When MLLB_A is logic 1, each of the *DLnA_P* and *DLnA_N* serial data inputs is presented on the *SLnA_P* and *SLnA_N* serial data outputs. When MLLB_A is a logic 0, the normal high speed transmit serial interface is preserved.

PLLE_A

Port A Parallel Line Loopback Enable. The PLLE_A bit is used to put the QuadPHY XR in parallel line loopback mode where the *DLnN_P* and *DLnA_P* serial data inputs are presented on the *SLnN_P* and *SLnA_P* serial data outputs at the system side of the digital core encompassing all of the digital functionality for port A. When PLLE_A is logic 1, the line loopback is enabled. When PLLE_A is logic 0, the QuadPHY XR operates normally. Note that in order for correct operation in this parallel loopback, the receive and transmit interfaces must be frequency locked.

Register 0xD002: Master Configuration 2

Bit	Type	Function	Default
Bit 15	R/W	PLLE_B	0
Bit 14	R/W	MLLB_B	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	RCLE_B	0
Bit 11	R	FC_GEB_MODE_MON_B	-
Bit 10	R	TRNK_LNB_MODE_MON_B	-
Bit 9	R	8B10B_EN_MON_B	-
Bit 8	R	Reserved	0
Bit 7	R/W	FC_GEB_MODE_SW_B	0
Bit 6	R/W	TRNK_LNB_MODE_SW_B	0
Bit 5	R/W	8B10B_EN_SW_R	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	1
Bit 1	R	SERDES_WIDTH_MON	-
Bit 0	R/W	SERDES_WIDTH_SW	0

SERDES_WIDTH_SW

SERDES Mode Data Path Width software override. When the QuadPHY XR device is not operating in trunked mode (can be accomplished by setting TRNK_LNB_MODE_SW appropriately through software override or strapping *MODE_SEL[1:0]* appropriately through device pins), the SERDES_WIDTH_SW is used by the internal PISO and SIPO blocks to perform serial-to-parallel and parallel-to-serial processing of data and it will drive the swizzle logic if it is enabled. The value written to this bit is logically XOR'ed with the SERDES_WIDTH _MON bit to obtain the desired functionality. A logic 0 resulting from the XOR, will configure all lanes in the device to 10-bit processing. A logic 1 resulting from the XOR, will configure all lanes in the device to 8-bit processing.

SERDES_WIDTH_MON

SERDES Mode Data Path Width monitor. The SERDES_WIDTH_MON bit reflects the internal data path width as realized by the *MODE_SEL[1:0]* input pin pins. A logic 1 on this bit indicates that the device is strapped for 8-bit processing. A logic 0 on this bit indicates that the device is strapped for 10-bit processing. This bit is used in conjunction with the SERDES_WIDTH_SW bit to determine port B and port A behavior.

8B10B_EN_MON_B

Port B 8B/10B encoder/decoder enable monitor. The 8B10B_EN_MON_B bit reflects the internal state of the 8B10B encoder/decoder as realized by the *MODE_SEL[1:0]* input pins. A logic 1 on this bit indicates that the device is strapped for 8B10B encoding/decoding. A logic 0 on this bit indicates that the device is strapped for no 8B/10B processing. This bit is used in conjunction with the 8B10B_EN_SW_B bit to determine port B's behavior. Further programmability in either the transmit or receive channel on a lane-by-lane basis within port B is available in the REFX and TEFX register space and will override the 8B10B_EN_MON_B and 8B10B_EN_SW_B register bits.

TRNK_LNB_MODE_MON _B

Port B Trunk/Lane based mode monitor. The TRNK_LNB_MODE_MON _B bit reflects the internal operation mode as realized by the *MODE_SEL[1:0]* input pin pins. A logic 1 on this bit indicates that the device is strapped for XAUI trunked mode of operation on port B. A logic 0 on this bit indicates that the device is strapped for lane-based mode of operation. This bit is used in conjunction with the TRNK_LNB_MODE_SW _B bit to determine port B's behaviour. Further programmability in either the transmit or receive channel within port B is available in the REFX and TEFX register space and will override the TRNK_LNB_MODE_MON _B and TRNK_LNB_MODE_SW _B register bits.

FC_GEB_MODE_MON _B

Port B 10GFC/10GbE mode monitor. The FC_GEB_MODE_MON _B bit reflects the internal operation mode as realized by the *MODE_SEL[1:0]* input pin pins. A logic 1 on this bit indicates that the device is strapped for 10 Gbit/s Fibre Channel mode of operation on port B. A logic 0 on this bit indicates that the device is strapped for 10 Gbit/s Ethernet of operation. This bit is used in conjunction with the FC_GEB_MODE_SW _B bit to determine port B's behaviour. Further programmability in either the transmit or receive channel within port B is available in the REFX and TEFX register space and will override the FC_GEB_MODE _MON _B and FC_GEB_MODE _SW _B register bits.

8B10B_EN_SW_B

Port B 8B/10B encoder/decoder enable software override. The 8B10B_EN_SW_B bit is used to program the 8B10B encoder/decoder. The value written to this bit is logically XOR'ed with the 8B10B_EN_MON_B to obtain the desired functionality. A logic 1 resulting from the XOR enables 8B10B encoding/decoding on port B. A logic 0 resulting from the XOR disables 8B/10B processing on port B. Further software programmability in either the transmit or receive channel on a lane-by-lane basis within port B is available in the REFX and TEFX register space and will override (8B10B_EN_MON_B) XOR (8B10B_EN_SW_B) .

TRNK_LNB_MODE_SW_B

Port B Trunk/Lane based mode software override. The TRNK_LNB_MODE_SW _B bit is used to configure the operation of port B. The value written to this bit is logically XOR'ed with the TRNK_LNB_MODE_MON_B to obtain the desired functionality. A logic 1 resulting from the XOR configures the device for XAUI trunked mode of operation on port B. A logic 0 resulting from the XOR configures the device for lane-based mode of operation. Further programmability in either the transmit or receive channel within port B is available in the REFX and TEFX register space and will override (TRNK_LNB_MODE_MON _B) XOR (TRNK_LNB_MODE_SW _B).

FC_GEB_MODE_SW _B

Port B 10GFC/10GbE mode software override. The FC_GEB_MODE_SW _B bit is used to configure the operation of port B. The value written to this bit is logically XOR'ed with the FC_GEB_MODE _ MON_B to obtain the desired functionality. A logic 1 resulting from the XOR configures the device for 10 Gbit/s Fibre Port mode of operation on port B. A logic 0 resulting from the XOR configures the device for 10 Gbit/s Ethernet mode of operation. Further programmability in either the transmit or receive channel within port B is available in the REFX and TEFX register space and will override (FC_GEB_MODE _MON _B) XOR (FC_GEB_MODE _SW _B).

RCLE_B

Port B Recovered Clock Loopback Enable. The RCLE_B bit is used to obtain the recovered clock derived from the high speed serial data path for each of the lanes in the device. When RCLE _B is logic 1, each of the *SLnB_N* and *SLnB_P* will transmit the locally derived clock from the associated *DLnB_N* and *DLnB_P* serial data inputs. When RCLE_B is a logic 0, the normal high speed transmit serial interface is preserved. Note that the RCLE_B bit is logically OR'ed with the 4 Port B Channel RCLE_B bits in the Analog Transmit Configuration/Monitor 1 register to obtain the loopback for the 4 lanes in port B channel.

MLLB_B

Port B Metallic Line loopback. This bit is used to put the QuadPHY XR port B in a metallic loopback where the high speed serial receive data is immediately looped to the high speed transmit interface. When MLLB_B is logic 1, each of the *DLnB_N* and *DLnB_P* serial data inputs is presented on the *SLnB_N* and *SLnB_P* serial data outputs. When MLLB_B is a logic 0, the normal high speed transmit serial interface is preserved.

PLLE_B

Port B Parallel Line Loopback Enable. The PLLE_B bit is used to put the QuadPHY XR in parallel line loopback mode where the *DLnB_N* and *DLnB_P* serial data inputs are presented on the *SLnB_N* and *SLnB_P* serial data outputs at the system side of the digital core encompassing almost all of the digital functionality. When PLLE_B is logic 1, the line loopback is enabled. When PLLE_B is logic 0, the QuadPHY XR operates normally. Note that in order for correct operation in this parallel loopback, the receive and transmit interfaces are frequency locked.

Register 0xD003: Master Receive Fault Configuration

Bit	Type	Function	Default
15	R/W	D_TRANS_DET_A_E	0
14	R/W	D_TRANS_DET_B_E	0
13	R/W	SD_A_E	0
12	R/W	SD_B_E	0
11	R	D_TRANS_DET_A_V	-
10	R	D_TRANS_DET_B_V	-
9	R	SD_A_V	-
8	R	SD_B_V	-
7	R/W	SD_INV_A	0
6	R/W	D_TRANS_INCL_A	1
5	R/W	SD_INCL_A	1
4	R/W	RX_SYNC_INCL_A	1
3	R/W	SD_INV_B	0
2	R/W	D_TRANS_INCL_B	1
1	R/W	SD_INCL_B	1
0	R/W	RX_SYNC_INCL_B	1

RX_SYNC_INCL_B

Port B Receive Synchronization Error Inclusion. When RX_SYNC_INCL_B is set to logic 1, LANE_0_SYNC, LANE_1_SYNC, LANE_2_SYNC, and LANE_3_SYNC of Register 0xC018 are included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When RX_SYNC_INCL_B is set to logic 0, port B receive channel synchronization does not contribute to *RX_FAULT_B.*

SD_INCL_B

Port B Signal Detect Inclusion. When SD_INCL_B is set to logic 1, the *SD_B* input pin is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When SD_INCL_B is set to logic 0, port B receive channel signal detect does not contribute to *RX_FAULT_B.*

D_TRANS_INCL_B

Port B Transition Detect Inclusion. When D_TRANS_INCL_B is set to logic 1, transition detect on the high speed *DLnB_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When D_TRANS_INCL_B is set to logic 0, port B receive channel signal transition detect does not contribute to *RX_FAULT_B.*

SD_INV_B

Port B Signal Detect Invert. When SD_INV_B is set to logic 1, the *SD_B* input pin is preconditioned with an inverter before processing. When SD_INV_B is a logic 0, the *SD_B* input pin is processed directly.

RX_SYNC_INCL_A

Port A Receive Synchronization Error Inclusion. When RX_SYNC_INCL_A is set to logic 1, LANE_0_SYNC, LANE_1_SYNC, LANE_2_SYNC, and LANE_3_SYNC of Register 0x0018 are included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When RX_SYNC_INCL_A is set to logic 0, port A receive channel synchronization does not contribute to *RX_FAULT_A*.

SD_INCL_A

Port A Signal Detect Inclusion. When SD_INCL_A is set to logic 1, the *SD_A* input pin is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When SD_INCL_A is set to logic 0, port A receive channel signal detect does not contribute to *RX_FAULT_A*.

D_TRANS_INCL_A

Port A Transition Detect Inclusion. When D_TRANS_INCL_A is set to logic 1, transition detect on the high speed *DLnA_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When D_TRANS_INCL_A is set to logic 0, port A receive channel signal transition detect does not contribute to *RX_FAULT_A*.

SD_INV_A

Port B Signal Detect Invert. When SD_INV_A is set to logic 1, the *SD_A* input pin is preconditioned with an inverter before processing. When SD_INV_A is a logic 0, the *SD_A* input pin is processed with no inverter in it's signal path.

SD_B_V

Port B Signal Detect Status. The SD_B_V bit follows the state of the *SD_B* input pin. The logic value of the state of the *SD_B* input pin is dependant on programmable inversion.

SD_A_V

Port A Signal Detect Status. The SD_A_V bit follows the state of the *SD_A* input pin. The logic value of the state of the *SD_A* input pin is dependant on programmable inversion

D_TRANS_DET_B_V

Port B Transition Detect Status. When D_TRANS_DET_B_V is logic 1, there is sufficient transition density on the *DLnB_P/N* port B high speed input. When D_TRANS_DET_B_V is logic 0, there is no meaningful data on *DLnB_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_A_V

Port A Transition Detect Status. When D_TRANS_DET_A_V is logic 1, there is sufficient transition density on the *DLnA_P/N* port A high speed input. When D_TRANS_DET_A_V is logic 0, there is no meaningful data on *DLnA_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

SD_B_E

Port B Signal Detect Enable. When SD_B_E is logic 1, a transition of logic 0 to logic 1 SD_B_I transition logic 0 to logic 1 on the SD_B_I bit will drive the assertion of the *INTB* output pin. When SD_B_E is logic 0, SD_B_I bit has no contribution to the *INTB* output pin.

SD_A_E

Port A Signal Detect Enable. When SD_A_E is logic 1, a transition of logic 0 to logic 1 on the SD_A_I bit will drive the assertion of the *INTB* output pin. When SD_A_E is logic 0, SD_A_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_B_E

Port B Signal Detect Enable. When D_TRANS_DET_B_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_B_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_B_E is logic 0, D_TRANS_DET_B_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_A_E

Port A Signal Detect Enable. When D_TRANS_DET_A_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_A_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_A_E is logic 0, D_TRANS_DET_A_I bit has no contribution to the *INTB* output pin.

Register 0xD004: Master Port A Receive Fault Configuration/Monitor

Bit	Type	Function	Default
15	R/W	D_TRANS_DET_A3_E	0
14	R/W	D_TRANS_DET_A2_E	0
13	R/W	D_TRANS_DET_A1_E	0
12	R/W	D_TRANS_DET_A0_E	0
11	R	D_TRANS_DET_A3_V	-
10	R	D_TRANS_DET_A2_V	-
9	R	D_TRANS_DET_A1_V	-
8	R	D_TRANS_DET_A0_V	-
7	R/W	D_TRANS_INCL_A3	1
6	RW	D_TRANS_INCL_A2	1
5	R/W	D_TRANS_INCL_A1	1
4	R/W	D_TRANS_INCL_A0	1
3	R/W	RX_SYNC_INCL_A3	1
2	R/W	RX_SYNC_INCL_A2	1
1	R/W	RX_SYNC_INCL_A1	1
0	R/W	RX_SYNC_INCL_A0	1

RX_SYNC_INCL_A0

Port A Lane 0 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_A0 is set to logic 1, LANE_0_SYNC of Register 0x0018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When RX_SYNC_INCL_A0 is set to logic 0, port A lane 0 receive synchronization does not contribute to *RX_FAULT_A.* RX_SYNC_INCL_A has priority over this bit.

RX_SYNC_INCL_A1

Port A Lane 1 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_A1 is set to logic 1, LANE_1_SYNC of Register 0x0018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When RX_SYNC_INCL_A1 is set to logic 0, port A lane 1 receive synchronization does not contribute to *RX_FAULT_A.* RX_SYNC_INCL_A has priority over this bit.

RX_SYNC_INCL_A2

Port A Lane 2 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_A2 is set to logic 1, LANE_2_SYNC of Register 0x0018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When RX_SYNC_INCL_A2 is set to logic 0, port A lane 2 receive synchronization does not contribute to *RX_FAULT_A.* RX_SYNC_INCL_A has priority over this bit.

RX_SYNC_INCL_A3

Port A Lane 3 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_A3 is set to logic 1, LANE_3_SYNC of Register 0x0018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When RX_SYNC_INCL_A3 is set to logic 0, port A lane 3 receive synchronization does not contribute to *RX_FAULT_A.* RX_SYNC_INCL_A has priority over this bit.

D_TRANS_INCL_A0

Port A Lane 0 Transition Detect Inclusion. When D_TRANS_INCL_A_A0 is set to logic 1, transition detect on the high speed *DL0A_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When D_TRANS_INCL_A0 is set to logic 0, port A receive lane 0 signal transition detect does not contribute to *RX_FAULT_A.*

D_TRANS_INCL_A1

Port A Lane 1 Transition Detect Inclusion. When D_TRANS_INCL_A_A1 is set to logic 1, transition detect on the high speed *DL1A_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When D_TRANS_INCL_A1 is set to logic 0, port A receive lane 1 signal transition detect does not contribute to *RX_FAULT_A.*

D_TRANS_INCL_A2

Port A Lane 2 Transition Detect Inclusion. When D_TRANS_INCL_A_A2 is set to logic 1, transition detect on the high speed *DL2A_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When D_TRANS_INCL_A2 is set to logic 0, port A receive lane 2 signal transition detect does not contribute to *RX_FAULT_A.*

D_TRANS_INCL_A3

Port A Lane 3 Transition Detect Inclusion. When D_TRANS_INCL_A_A3 is set to logic 1, transition detect on the high speed *DL3A_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_A* output pin. When D_TRANS_INCL_A3 is set to logic 0, port A receive lane 3 signal transition detect does not contribute to *RX_FAULT_A.*

D_TRANS_DET_A0_V

Port A Lane 0 Transition Detect Status. When D_TRANS_DET_A0_V is logic 1, there is sufficient transition density on the *DL0*R_A*/N* port A high speed input. When D_TRANS_DET_A0_V is logic 0, there is insufficient transition density *DL0A_P/N.*

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_A1_V

Port A Lane 1 Transition Detect Status. When D_TRANS_DET_A1_V is logic 1, there is sufficient transition density on the *DL1A_P/N* port A high speed input. When D_TRANS_DET_A1_V is logic 0, there is insufficient transition density *DL1A_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_A2_V

Port A Lane 2 Transition Detect Status. When D_TRANS_DET_A2_V is logic 1, there is sufficient transition density on the *DL2A_P/N* port A high speed input. When D_TRANS_DET_A2_V is logic 0, there is insufficient transition density *DL2A_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_A3_V

Port A Lane 3 Transition Detect Status. When D_TRANS_DET_A3_V is logic 1, there is sufficient transition density on the *DL3*R_A*/N* port A high speed input. When D_TRANS_DET_A3_V is logic 0, there is insufficient transition density *DL3A_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_A0_E

Port A Lane 0 Signal Detect Enable. When D_TRANS_DET_A0_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_A0_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_A0_E is logic 0, D_TRANS_DET_A0_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_A1_E

Port A Lane 1 Signal Detect Enable. When D_TRANS_DET_A1_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_A1_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_A1_E is logic 0, D_TRANS_DET_A1_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_A2_E

Port A Lane 2 Signal Detect Enable. When D_TRANS_DET_A2_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_A2_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_A2_E is logic 0, D_TRANS_DET_A2_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_A3_E

Port A Lane 3 Signal Detect Enable. When D_TRANS_DET_A3_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_A3_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_A3_E is logic 0, D_TRANS_DET_A3_I bit has no contribution to the *INTB* output pin.

Register 0xD005: Master Port B Receive Fault Configuration/Monitor

Bit	Type	Function	Default
15	R/W	D_TRANS_DET_B3_E	0
14	R/W	D_TRANS_DET_B2_E	0
13	R/W	D_TRANS_DET_B1_E	0
12	R/W	D_TRANS_DET_B0_E	0
11	R	D_TRANS_DET_B3_V	-
10	R	D_TRANS_DET_B2_V	-
9	R	D_TRANS_DET_B1_V	-
8	R	D_TRANS_DET_B0_V	-
7	R/W	D_TRANS_INCL_B3	1
6	R/W	D_TRANS_INCL_B2	1
5	R/W	D_TRANS_INCL_B1	1
4	R/W	D_TRANS_INCL_B0	1
3	R/W	RX_SYNC_INCL_B3	1
2	R/W	RX_SYNC_INCL_B2	1
1	R/W	RX_SYNC_INCL_B1	1
0	R/W	RX_SYNC_INCL_B0	1

RX_SYNC_INCL_B0

Port B Lane 0 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_B0 is set to logic 1, LANE_0_SYNC of Register 0xC018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When RX_SYNC_INCL_B0 is set to logic 0, port B lane 0 receive synchronization does not contribute to *RX_FAULT_B*. RX_SYNC_INCL_B has priority over this bit.

RX_SYNC_INCL_B1

Port B Lane 1 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_B1 is set to logic 1, LANE_1_SYNC of Register 0xC018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When RX_SYNC_INCL_B1 is set to logic 0, port B lane 1 receive channel synchronization does not contribute to *RX_FAULT_B*. RX_SYNC_INCL_B has priority over this bit.

RX_SYNC_INCL_B2

Port B Lane 2 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_B2 is set to logic 1, LANE_2_SYNC of Register 0xC018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When RX_SYNC_INCL_B2 is set to logic 0, port B lane 2 receive channel synchronization does not contribute to *RX_FAULT_B*. RX_SYNC_INCL_B has priority over this bit.

RX_SYNC_INCL_B3

Port B Lane 3 Receive Synchronization Error Inclusion. When RX_SYNC_INCL_B3 is set to logic 1, LANE_3_SYNC of Register 0xC018 is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT*_B output pin. When RX_SYNC_INCL_B3 is set to logic 0, port B lane 3 receive channel synchronization does not contribute to *RX_FAULT_B.* The RX_SYNC_INCL_B bit has priority over this bit.

D_TRANS_INCL_B0

Port B Lane 0 Transition Detect Inclusion. When D_TRANS_INCL_B_B0 is set to logic 1, transition detect on the high speed *DL0B_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When D_TRANS_INCL_B0 is set to logic 0, port B receive lane 0 signal transition detect does not contribute to *RX_FAULT_B.*

D_TRANS_INCL_B1

Port B Lane 1 Transition Detect Inclusion. When D_TRANS_INCL_B_B1 is set to logic 1, transition detect on the high speed *DL1B_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When D_TRANS_INCL_B1 is set to logic 0, port B lane 1 receive signal transition detect does not contribute to *RX_FAULT*_B.

D_TRANS_INCL_B2

Port B Lane 2 Transition Detect Inclusion. When D_TRANS_INCL_B_B2 is set to logic 1, transition detect on the high speed *DL2B_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When D_TRANS_INCL_B2 is set to logic 0, port B lane 2 receive signal transition detect does not contribute to *RX_FAULT*_B.

D_TRANS_INCL_B3

Port B Lane 3 Transition Detect Inclusion. When D_TRANS_INCL_B_B3 is set to logic 1, transition detect on the high speed *DL3B_P/N* input pins is included in the logical OR'ing of receive error conditions to generate the *RX_FAULT_B* output pin. When D_TRANS_INCL_B3 is set to logic 0, port B lane 3 receive signal transition detect does not contribute to *RX_FAULT_B.*

D_TRANS_DET_B0_V

Port B Lane 0 Transition Detect Status. When D_TRANS_DET_B0_V is logic 1 there is sufficient transition density on the *DL0B_P/N* port B high speed input. When D_TRANS_DET_A0_V is logic 0, there is insufficient transition density *DL0B_P/N.*

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_B1_V

Port B Lane 1 Transition Detect Status. When D_TRANS_DET_B1_V is logic 1, there is sufficient transition density on the *DL1B_P/N* port B high speed input. When D_TRANS_DET_B1_V is logic 0, there is insufficient transition density *DL1B_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_B2_V

Port B Lane 2 Transition Detect Status. When D_TRANS_DET_B0_V is logic 1 there is sufficient transition density on the *DL2B_P/N* port B high speed input. When D_TRANS_DET_B2_V is logic 0, there is insufficient transition density *DL2B_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_B3_V

Port B Lane 3 Transition Detect Status. When D_TRANS_DET_B3_V is logic 1, there is sufficient transition density on the DL3R_A/N port B high speed input. When D_TRANS_DET_B3_V is logic 0, there is insufficient transition density *DL3B_P/N*.

Transition detection is not supported in 8-bit SERDES mode.

D_TRANS_DET_B0_E

Port B Lane 0 Signal Detect Enable. When D_TRANS_DET_B0_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_B0_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_B0_E is logic 0, D_TRANS_DET_B0_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_B1_E

Port B Lane 1 Signal Detect Enable. When D_TRANS_DET_B1_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_B1_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_B1_E is logic 0, D_TRANS_DET_B1_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_B2_E

Port B Lane 2 Signal Detect Enable. When D_TRANS_DET_B2_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_B2_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_B2_E is logic 0, D_TRANS_DET_B2_I bit has no contribution to the *INTB* output pin.

D_TRANS_DET_B3_E

Port B Lane 3 Signal Detect Enable. When D_TRANS_DET_B3_E is logic 1, a transition of logic 0 to logic 1 on the D_TRANS_DET_B3_I bit will drive the assertion of the *INTB* output pin. When D_TRANS_DET_B3_E is logic 0, D_TRANS_DET_B3_I bit has no contribution to the *INTB* output pin

Register 0xD006: Master Register Port Status

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R	Reserved	-
8	R	Reserved	-
7	R	TX_CLK_MON	-
6		Unused	X
5		Unused	X
4		Unused	X
3	R	D_TRANS_DET_A_I	-
2	R	SD_A_I	-
1	R	D_TRANS_DET_B_I	-
0	R	SD_B_I	-

SD_B_I

Port B Signal Detect Interrupt. When SD_B_I is logic 1, the SD_B_V bit has transitioned from a logic 0 to a logic 1 reflecting the a active transition of the *SD_B* input pin. When SD_B_I is logic 0, an active transition on the SD_B input pin has not occurred since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_B_I

Port B Transition Detect Interrupt. When D_TRANS_DET_B_I is logic 1, the D_TRANS_DET_B_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DLnB_P/N* port B high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

SD_A_I

Port A Signal Detect Interrupt. When SD_A_I is logic 1, the SD_A_V bit has transitioned from a logic 0 to a logic 1 reflecting the a active transition of the *SD_A* input pin. . When SD_A_I is logic 0, an active transition on the SD_A input pin has not occurred since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_A_I

Port A Transition Detect Interrupt. When D_TRANS_DET_A_I is logic 1, the D_TRANS_DET_A_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DLnA_P/N* port A high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

TX_CLK_MON:

The transmit clock monitor bit (TX_CLK_MON) is used to verify that the transmit clock is toggling. When TX_CLK_MON is logic 0, the transmit clock has not toggled since this bit was last read. When TX_CLK_MON is logic 1, the Transmit clock has toggled since this bit was last read.

Register 0xD007: Master Port A Receive Fault Status

Bit	Type	Function	Default
15	R	TX_DATA_MON_A3	-
14	R	TX_DATA_MON_A2	-
13	R	TX_DATA_MON_A1	-
12	R	TX_DATA_MON_A0	-
11	R	Reserved	-
10	R	Reserved	-
9	R	Reserved	-
8	R	Reserved	-
7	R	Reserved	-
6	R	Reserved	-
5	R	Reserved	-
4	R	Reserved	-
3	R	D_TRANS_DET_A3_I	-
2	R	D_TRANS_DET_A2_I	-
1	R	D_TRANS_DET_A1_I	-
0	R	D_TRANS_DET_A0_I	-

D_TRANS_DET_A0_I

Port A Lane 0 Transition Detect Interrupt. When D_TRANS_DET_A0_I is logic 1, the D_TRANS_DET_A0_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL0A_P/N* port A high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_A1_I

Port A Lane 1 Transition Detect Interrupt. When D_TRANS_DET_A1_I is logic 1, the D_TRANS_DET_A1_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL1A_P/N* port A high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_A2_I

Port A Lane 2 Transition Detect Interrupt. When D_TRANS_DET_A2_I is logic 1, the D_TRANS_DET_A2_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL2A_P/N* port A high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_A3_I

Port A Lane 3 Transition Detect Interrupt. When D_TRANS_DET_A3_I is logic 1, the D_TRANS_DET_A3_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL3A_P/N* port A high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

TX_DATA_MON_A0

Port A lane 0 transmit data monitor bit is used to verify the transmit data is toggling for the corresponding lane. When TX_DATA_MON_A0 is logic 0, none of the bits in port A lane 0 parallel transmit data path have toggled since TX_DATA_MON_A0 was last read. When TX_DATA_MON_A0 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_A0 was last read.

TX_DATA_MON_A1

Port A lane 1 transmit data monitor bit is used to verify that the transmit data is toggling for the corresponding lane. When TX_DATA_MON_A1 is logic 0, none of the bits in port A lane 1 parallel transmit data path have toggled since TX_DATA_MON_A1 was last read. When TX_DATA_MON_A1 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_A1 was last read.

TX_DATA_MON_A2

Port A lane 2 transmit data monitor bit is used to verify that the transmit data is toggling for the corresponding lane. When TX_DATA_MON_A2 is logic 0, none of the bits in port A lane 2 parallel transmit data path have toggled since TX_DATA_MON_A2 was last read. When TX_DATA_MON_A2 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_A2 was last read.

TX_DATA_MON_A3

Port A lane 3 transmit data monitor bit is used to verify that the transmit data is toggling for the corresponding lane. When TX_DATA_MON_A3 is logic 0, none of the bits in port A lane 3 parallel transmit data path have toggled since TX_DATA_MON_A3 was last read. When TX_DATA_MON_A3 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_A3 was last read.

Registers 0xD008: Master Port B Receive Fault Status

Bit	Type	Function	Default
15	R	TX_DATA_MON_B3	-
14	R	TX_DATA_MON_B2	-
13	R	TX_DATA_MON_B1	-
12	R	TX_DATA_MON_B0	-
11	R	Reserved	-
10	R	Reserved	-
9	R	Reserved	-
8	R	Reserved	-
7	R	Reserved	-
6	R	Reserved	-
5	R	Reserved	-
4	R	Reserved	-
3	R	D_TRANS_DET_B3_I	-
2	R	D_TRANS_DET_B2_I	-
1	R	D_TRANS_DET_B1_I	-
0	R	D_TRANS_DET_B0_I	-

D_TRANS_DET_B0_I

Port B Lane 0 Transition Detect Interrupt. When D_TRANS_DET_B0_I is logic 1, the D_TRANS_DET_B0_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL0B_P/N* port B high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_B1_I

Port B Lane 1 Transition Detect Interrupt. When D_TRANS_DET_B1_I is logic 1, the D_TRANS_DET_B1_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL1B_P/N* port B high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_B2_I

Port B Lane 2 Transition Detect Interrupt. When D_TRANS_DET_B2_I is logic 1, the D_TRANS_DET_B2_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL2B_P/N* port B high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

D_TRANS_DET_B3_I

Port B Lane 3 Transition Detect Interrupt. When D_TRANS_DET_B3_I is logic 1, the D_TRANS_DET_B3_V bit has transitioned from a logic 1 to a logic 0 indicating that there is insufficient transition density detected on the *DL3B_P/N* port B high speed input since this bit was last cleared. When the WCIMODE register bit is a logic 1, this bit is written to clear. When the WCIMODE register bit is a logic 0, this bit is read to clear.

TX_DATA_MON_B0

Port B lane 0 transmit data monitor bit is used to verify the transmit data is toggling for the corresponding lane. When TX_DATA_MON_B0 is logic 0, none of the bits in port B lane 0 parallel transmit data path have toggled since TX_DATA_MON_B0 was last read. When TX_DATA_MON_B0 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_B0 was last read.

TX_DATA_MON_B1

Port B lane 1 transmit data monitor bit is used to verify that the transmit data is toggling for the corresponding lane. When TX_DATA_MON_B1 is logic 0, none of the bits in port B lane 0 parallel transmit data path have toggled since TX_DATA_MON_B1 was last read. When TX_DATA_MON_B1 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_B1 was last read.

TX_DATA_MON_B2

Port B lane 0 transmit data monitor bit is used to verify that the transmit data is toggling for the corresponding lane. When TX_DATA_MON_B2 is logic 0, none of the bits in port B lane 0 parallel transmit data path have toggled since TX_DATA_MON_B2 was last read. When TX_DATA_MON_B2 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_B2 was last read.

TX_DATA_MON_B3

Port B lane 3 transmit data monitor bit is used to verify that the transmit data is toggling for the corresponding lane. When TX_DATA_MON_B3 is logic 0, none of the bits in port B lane 0 parallel transmit data path have toggled since TX_DATA_MON_B3 was last read. When TX_DATA_MON_B3 is logic 1, at least one of the bits in the this lane have toggled since TX_DATA_MON_B3 was last read.

Register 0xD009: MDIO Device ID 1

Bit	Type	Function	Default
15	R/W	DEV_ID[31]	0
14	R/W	DEV_ID[30]	0
13	R/W	DEV_ID[29]	0
12	R/W	DEV_ID[28]	0
11	R/W	DEV_ID[27]	0
10	R/W	DEV_ID[26]	0
9	R/W	DEV_ID[25]	0
8	R/W	DEV_ID[24]	0
7	R/W	DEV_ID[23]	0
6	R/W	DEV_ID[22]	0
5	R/W	DEV_ID[21]	0
4	R/W	DEV_ID[20]	0
3	R/W	DEV_ID[19]	0
2	R/W	DEV_ID[18]	0
1	R/W	DEV_ID[17]	0
0	R/W	DEV_ID[16]	0

DEV_ID[31:16]

The DEV_ID[31:16] Device ID bits comprise the most significant word of all possible MDIO Manageable Device Addresses. If DEV_ID[*n*] is a logic 1, the QuadPHY XR will be sensitive to all register addresses on the MDIO/MDC interface for which the MMD device address is equal to *n* . If DEV_ID[*n*] is a logic 0, the QuadPHY XR will not be sensitive to any register addresses on the MDIO/MDC interface for which the MMD device address is equal to *n*. Refer to IEEE P802.3ae - "45. Management Data Input/Output (MDIO) Interface" for further information on the MDIO Device types

Register 0xD00A: MDIO Device ID 2

Bit	Type	Function	Default
15	R/W	DEV_ID[15]	0
14	R/W	DEV_ID[14]	0
13	R/W	DEV_ID[13]	0
12	R/W	DEV_ID[12]	0
11	R/W	DEV_ID[11]	0
10	R/W	DEV_ID[10]	0
9	R/W	DEV_ID[9]	0
8	R/W	DEV_ID[8]	0
7	R/W	DEV_ID[7]	0
6	R/W	DEV_ID[6]	0
5	R/W	DEV_ID[5]	0
4	R/W	DEV_ID[4]	1
3	R/W	DEV_ID[3]	1
2	R/W	DEV_ID[2]	0
1	R/W	DEV_ID[1]	1
0	R/W	DEV_ID[0]	0

DEV_ID[15:0]

The DEV_ID[15:0] Device ID bits comprise the least significant word of all possible MDIO Manageable Device Addresses. If DEV_ID[*n*] is a logic 1, the QuadPHY XR will be sensitive to all register addresses on the MDIO/MDC interface for which the MMD device address is equal to *n*. If DEV_ID[*n*] is a logic 0, the QuadPHY XR will not be sensitive to any register addresses on the MDIO/MDC interface for which the MMD device address is equal to *n*. Refer to IEEE P802.3ae - "45. Management Data Input/Output (MDIO) Interface" for further information on the MDIO Device types. For non-supported applications, registers 0xD009 and 0xD00A should be reprogrammed to the desired MMD device address during initialization after reset. Before and after reprogramming, this register will remain accessable at any device address for which DEV_ID[n] is a logic 1. If DEV_ID bits 1,3 or 4 are written with logic 0, PMA/PMD, PCS or PHY XS register sets will become unaccessable.

Register 0xD00C: Master Register Port Status

Bit	Type	Function	Default
15	R/W	TRANS_DET_THRES[3]	1
14	R/W	TRANS_DET_THRES[2]	0
13	R/W	TRANS_DET_THRES[1]	0
12	R/W	TRANS_DET_THRES[0]	0
11	R	Reserved	0
10	R	Reserved	0
9		Unused	X
8		Unused	X
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3		Unused	X
2		Unused	X
1		Unused	X
0		Unused	X

TRANS_DET_THRES[3:0]

Transition Detect Threshold bus. This value determines the integration period of the transition detect logic in multiples of 10 bits. A value of '0001' on TRANS_DET_THRES[3:0] will cause the transition detect lane or port interrupt bits to become active if there is one or more transitions detected within a 10-bit window on a given lane. A value of '1111' on TRANS_DET_THRES[3:0] will cause the TRANS_DET interrupt bits to become active if there is one or more transitions detected within a 160-bit window on a given lane

Registers 0xD020, 0xD028, 0xD030, 0xD038: Port A Channel Lanes 0-3 Analog Transmit Configuration/Monitor 1

Bit	Type	Function	Default
15	R/W	TX_ENB	0
14	R/W	Reserved	1
13	R/W	Reserved	1
12	R/W	Reserved	1
11	R/W	Reserved	0
10		Unused	X
9		Unused	X
8		Unused	X
7	R/W	RCLE	0
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1		Unused	X
0		Unused	X

RCLE

Recovered Clock Loopback Enable. The RCLE bit is used to obtain the recovered clock derived from the high speed serial data path for this lane in the device. When RCLE is logic 1, the *SLnA_P* and *SLnA_N* will transmit the locally derived clock from the associated *DLnA_P* and *DLnA_N* serial data inputs. When RCLE is a logic 0, the normal high speed transmit serial interface is preserved. Note that the RCLE bit is OR'ed with the RCLE_A bit in the Master Reset and Configuration1 register to obtain the loopback for this lane.

TX_ENB

Transmit active low enable.

TX_ENB when driven to logic 1 in channel 1-3 (0xD028, 0xD030, 0xD038), the corresponding lane is disabled, the circuitry will be put into low-power mode and the corresponding serial differential output pins are held static.

TX_ENB when driven to logic 1 in channel 0 (0xD020), all 4 channels are disabled, and all the Port A serial differential output pins are held static. TX_ENB for channel 1-3 should be set to logic 1 in conjunction with channel 0 to put all Port A TX circuitry into low-power mode.

Registers 0xD021, 0xD029, 0xD031, 0xD039: Port A Channel Lanes 0-3 Analog Transmit Configuration 2

Bit	Type	Function	Default
15	R/W	TX_MODE[7]	0
14	R/W	TX_MODE[6]	0
13	R/W	TX_MODE[5]	0
12	R/W	TX_MODE[4]	1
11	R/W	TX_MODE[3]	0
10	R/W	TX_MODE[2]	0
9	R/W	TX_MODE[1]	1
8	R/W	TX_MODE[0]	1
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R/W	PISO_MODE[3]	0
2	R/W	PISO_MODE[2]	0
1	R	PISO_MODE[1]	-0
0	R	PISO_MODE[0]	-

PISO_MODE[3:0]

Parallel-In-Serial-Out Mode. The PISO_MODE bits determine the various modes in which the link can be configured specifically for different input bus-widths to the PISO, pre-emphasis and some test-pattern generation. The operation of these bits is detailed below:

PISO_MODE	FUNCTION	COMMENTS
[1:0] VALID INPUT BUS WIDHT		
[00]	-	Reserved
[01]	8-bit	Internal bus width set to 8 bits
[10]	10-bit	Internal bus width set to 10 bits
[11]	-	Reserved
[2] TEST-PATTERN MODE		
[1]	-	Reserved
[3] . PRE-EMPHAISIS MODE Thisbit enables transmitter pre-emphasis. Refer to the Operations section for recommended use of the TXCML pre-emphasis feature.		
[1]	High enables the pre-emphasis for i-th PISO and i-th transmitter analog circuit. Pre-emphasis is enabled only when both TX and	Also pre-emphasis is not valid for either JTAG or loop-back modes. This bit has the least priority over all other test and functional modes for the link.

	PISO of the i-th link are enabled.	
[0]	Disabled	Pre-Emphasis is not activated.
For details on pre-emphasis, the usage and configuration guide-lines and different swing levels on **SLnP/R_N/P** in this mode, please refer to Operations Section .		
note: PSIO_MODE[0] is controlled by top level register bit SERDES_WIDTH_SW or by configuration pins		

TX_MODE[7:0]

The transmitter mode bits select the differential swing levels of a TXCML differential output pair. With pre-emphasis disabled, the TX_MODE[4:0] bits control the differential swing from 285 mV to 645 mV in 13 steps. With pre-emphasis enabled, the TX_MODE[4:3] bits control the high swing level while the TX_MODE[2:0] bits control the low swing level. The common mode output voltage with pre-emphasis enabled is defined by the TRANSMIT_MODE[4:0] bits. Refer to the Electrical Characteristics section for the swing levels with pre-emphasis disabled/enabled and for the common mode output voltage

Registers 0xD025, 0xD02D, 0xD035, 0xD03D: Port A Channel Lanes 0–3 Analog Receive Configuration 4

Bit	Type	Function	Default
15	R/W	RX_MODE[7]	1
14	R/W	RX_MODE[6]	0
13	R/W	RX_MODE[5]	0
12	R/W	RX_MODE[4]	0
11	R/W	RX_MODE[3]	0
10	R/W	RX_MODE[2]	0
9	R/W	RX_MODE[1]	0
8	R/W	RX_MODE[0]	1
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R	Reserved	-
0	R	Reserved	-

RX_MODE[7:0]

Receiver Mode. This bus is used to set the modes of the Receiver of the corresponding lane such as equalization and internal termination schemes. The bit definitions are outlined below.

Mode inputs for the equalizer of the appropriate receiver lane. The mode inputs perform the following functions:	
RX_MODE[7:0]	**OPERATION**
[7]	1: 50 ohms to 1.2V termination 0: 100 ohms floating termination This bit configures the input termination of the RXCML for either floating termination when set to a logic 0 or termination to 1.2V when set to a logic 1. Refer to Figure 18 for a schematic of the two termination modes. Termination to the 1.2V supply is recommended when interfacing to drivers that require a common mode current, such as the CML transmit links of the device, or when AC coupling using an external AC coupling capacitor. Floating termination is suitable for interfacing to drivers that do not require common mode current.
[6:2]	RESERVED and defaulted to 0

[1:0]	00 : no equalization 01 : half equalization 10 : full equalization 11 : reserved Equalization is controlled by EN_EQUALIZATION primary input pin when ANALOG_CTRL register bit (0xD000 bit 11) is set to logic 0. RX_MODE[1:0] bits are only effective when ANALOG_CTRL register bit is set to logic 1.

Registers 0xD040, 0xD048, 0xD050, 0xD058: Port B Channel Lanes 0-3 Analog Transmit Configuration/Monitor 1

Bit	Type	Function	Default
15	R/W	TX_ENB	0
14	R/W	Reserved	1
13	R/W	Reserved	1
12	R/W	Reserved	1
11	R/W	Reserved	0
10		Unused	X
9		Unused	X
8		Unused	X
7	R/W	RCLE	0
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1		Unused	X
0		Unused	X

RCLE

Recovered Clock Loopback Enable. The RCLE bit is used to obtain the recovered clock derived from the high speed serial data path for this lane in the device. When RCLE is logic 1, the *SLnA_P* and *SLnA_N* will transmit the locally derived clock from the associated *DLnA_P* and *DLnA_N* serial data inputs. When RCLE is a logic 0, the normal high speed transmit serial interface is preserved. Note that the RCLE bit is OR'ed with the RCLE_B bit in the Master Reset and Configuration 2 register to obtain the loopback for this lane.

TX_ENB

Transmit active low enable.

TX_ENB when driven to logic 1 in channel 1-3 (0xD048, 0xD050, 0xD058), the corresponding lane is disabled, the circuitry will be put into low-power mode and the corresponding serial differential output pins are held static.

TX_ENB when driven to logic 1 in channel 0 (0xD040), all 4 channels are disabled, and all the Port B serial differential output pins are held static. TX_ENB for channel 1-3 should be set to logic 1 in conjunction with channel 0 to put all Port B TX circuitry into low-power mode.

Registers 0xD041, 0xD049, 0xD051, 0xD059: Port B Channel Lanes 0-3 Analog Transmit Configuration 2

Bit	Type	Function	Default
15	R/W	TX_MODE[7]	0
14	R/W	TX_MODE[6]	0
13	R/W	TX_MODE[5]	0
12	R/W	TX_MODE[4]	1
11	R/W	TX_MODE[3]	0
10	R/W	TX_MODE[2]	0
9	R/W	TX_MODE[1]	1
8	R/W	TX_MODE[0]	1
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R/W	PISO_MODE[3]	0
2	R/W	PISO_MODE[2]	0
1	R	PISO_MODE[1]	-
0	R	PISO_MODE[0]	-

PISO_MODE[3:0]

Parallel-In-Serial-Out Mode. The PISO_MODE determines the various modes in which the link can be configured specifically for different input bus-widths to the PISO, pre-emphasis and some test-pattern generation. The operation of these bits is detailed below:

PISO_MODE	FUNCTION	COMMENTS
[1:0] VALID INPUT BUS WIDHT		
[00]		Reserved
[01]	8-bit	Internal bus width set to 8 bits
[10]	10-bit	Internal bus width set to 10 bits
[11]		Reserved
[2] TEST-PATTERN MODE		
[1]	-	Reserved
[3] . PRE-EMPHAISIS MODE This bit enables transmitter pre-emphasis. Refer to the Operations section for recommended use of the TXCML pre-emphasis feature.		

[1]	High enables the pre-emphasis for i-th PISO and i-th transmitter analog circuit. Pre-emphasis is enabled only when both TX and PISO of the i-th link are enabled.	Also pre-emphasis is not valid for either JTAG or loop-back modes. This bit has the least priority over all other test and functional modes for the link.
[0]	Disabled	Pre-Emphasis is not activated.
For details on pre-emphasis, the usage and configuration guide-lines and different swing levels on *SLnP/R_N/P* in this mode, please refer to Operations Section .		
note PSIO_MODE[0] is controlled by the SERDES_WIDTH_SW top level register bit or device configuration pins		

TX_MODE[7:0]

The transmitter mode bits select the differential swing levels of a TXCML differential output pair. With pre-emphasis disabled, the TX_MODE[4:0] bits control the differential swing from 285 mV to 645 mV in 13 steps. With pre-emphasis enabled, the TX_MODE[4:3] bits control the high swing level while the TX_MODE[2:0] bits control the low swing level. The common mode output voltage with pre-emphasis enabled is defined by the TX_MODE[4:0] bits. Refer to the Electrical Characteristics section for the swing levels with pre-emphasis disabled/enabled and for the common mode output voltage

Registers 0xD045, 0xD04D, 0xD055, 0xD05D: Port B Channel Lanes 0–3 Analog Receive Configuration 4

Bit	Type	Function	Default
15	R/W	RX_MODE[7]	1
14	R/W	RX_MODE[6]	0
13	R/W	RX_MODE[5]	0
12	R/W	RX_MODE[4]	0
11	R/W	RX_MODE[3]	0
10	R/W	RX_MODE[2]	0
9	R/W	RX_MODE[1]	0
8	R/W	RX_MODE[0]	1
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R	Reserved	0
0	R	Reserved	-

RX_MODE[7:0]

Receiver Mode. This bus is used to set the modes of the Receiver of the corresponding lane such as equalization and internal termination schemes. The bit definitions are outlined below.

Mode inputs for the equalizer of receiver Ri. The mode inputs perform the following functions:	
RX_MODE[7:0]	**OPERATION**
[7]	1: 50 ohms to 1.2V termination 0: 100 ohms floating termination This bit configures the input termination of the RXCML for either floating termination when set to a logic 0 or termination to 1.2V when set to a logic 1. Refer to Figure 18 for a schematic of the two termination modes. Termination to the 1.2V supply is recommended when interfacing to drivers that require a common mode current, such as the CML transmit links of the device, or when AC coupling using an external AC coupling capacitor. Floating termination is suitable for interfacing to drivers that do not require common mode current.
[6:2]	RESERVED and defaulted to 0 presently

[1:0]	00 : no equalization 01 : half equalization 10 : full equalization 11 : reserved For usage notes on programming the equalization, please refer to Application Note PMC-2021098

Registers 0xD080: XC16 Control

Bit	Type	Function	Default
15	R	MUX_PRESET TX_XAUI_B[1]	-
14	R	MUX_PRESET TX_XAUI_B[0]	-
13	R	MUX_PRESET TX_XAUI_A[1]	-
12	R	MUX_PRESET TX_XAUI_A[0]	-
11		Unused	X
10	R	Unused	1
9	R	Reserved	0
8	R	Reserved	1
7	R/W	TRUNKEN_TX_XAUI_B	0
6	R/W	TRUNKEN_TX_XAUI_A	0
5	R	Reserved	0
4	R	Reserved	0
3		Unused	X
2	R/W	FAILOVER	0
1	R/W	FAILOVER_IMM	0
0	R/W	IPG_SWITCHEN	0

IPG_SWITCHEN

IPG_SWITCHEN enables the IPG switch feature of the XC16 when set to logic 1. A transition from logic 0 to logic 1 on the FAILOVER input pin will switch all lanes. When IPG_SWITCHEN is set to logic 0, , a transition from logic 0 to logic 1 on the FAILOVER input pin is ignored by all lanes.

FAILOVER_IMM

When FAILOVER_IMM is toggled from logic 0 to logic 1, the XC16 will execute an immediate switch operation. All lanes with SWITCHEN*[n]* set to logic 1 will have their respective ACTIVELN registers updated with the STDBYLN register setting. This register bit is OR'ed with the FAILOVER_IMM pin For register control, the FAILOVER_IMM pin should be logic '0'. An attempt to write a logic '0' to this bit will have no effect. Refer to the Operation Section for details on the FAILOVER_IMM functionality.

FAILOVER

When FAILOVER is toggled from logic 0 to logic 1, the XC16 will perform the IPG switching sequence on lanes for which SWITCHEN*[n]* set to logic 1, if IPG_SWITCHEN is a logic 1. Lanes for which SWITCHEN is a logic 0 will not be switched, nor will a switch operation occur if IPG_SWITCHEN is a logic 0. This register bit is OR'ed with the FAILOVER pin. For register control, the FAILOVER pin should be logic '0'. An attempt to write a logic '0' to this bit will have no effect. Refer to the Operation Section for details on the FAILOVER functionality.

TRUNKEN_TX_XAUI_A:

TRUNKEN_TX_XAUI_A controls trunk data switching for port A transmit XAUI channel. When TRUNKEN_TX_XAUI_A is set to logic 1, the T_CHAR registers are used to detect terminate columns in order to synchronize lane switching across all output lanes within the port A transmit XAUI channel.

TRUNKEN_TX_XAUI_B:

TRUNKEN_TX_XAUI_B controls trunk data switching for port B transmit XAUI channel. When TRUNKEN_TX_XAUI_B is set to logic 1, the T_CHAR registers are used to detect terminate columns in order to synchronize lane switching across all output lanes within the for port B transmit XAUI channel.

MUX_PRESET TX_XAUI_A[1:0]

The MUX_PRESET TX_XAUI_A[1:0] bits reflects the internal state of the crossbar realized by the *MODE_SEL[1:0]* input pins and/or enabled loopbacks as it applies to port A transmit XAUI output port. This 2-bit pair is XOR'ed with the 2 MSBs of the ACTIVELNA[3:0] and ACTIVELNB[3:0] bus' in registers 0xD0A4 and 0xD0A5 to determine it's data path through the internal cross connect. Refer to the Operation Section for details on how to configure the crossbar

MUX_PRESET TX_XAUI_B[1:0]

The MUX_PRESET TX_XAUI_B[1:0] bits reflects the internal state of the crossbar realized by the *MODE_SEL[1:0]* input pins and/or enabled loopbacks as it applies to port A transmit XAUI output port. This 2-bit pair is XOR'ed with the 2 MSBs of the ACTIVELNA[3:0] and ACTIVELNB[3:0] bus' in registers , 0xD0A6 and 0xD0A7 to determine it's data path through the internal cross connect. Refer to the Operation Section for details on how to configure the crossbar

Registers 0xD081: XC16 Switch Enable

Bit	Type	Function	Default
15	R/W	TX_XAUI_B_LANE_SWTCHEN [3]	0
14	R/W	TX_XAUI_B_LANE_SWTCHEN [2]	0
13	R/W	TX_XAUI_B_LANE_SWTCHEN [1]	0
12	R/W	TX_XAUI_B_LANE_SWTCHEN [0]	0
11	R/W	TX_XAUI_ P_LANE_SWTCHEN [3]	0
10	R/W	TX_XAUI_ P_LANE_SWTCHEN [2]	0
9	R/W	TX_XAUI_ P_LANE_SWTCHEN [1]	0
8	R/W	TX_XAUI_ P_LANE_SWTCHEN [0]	0
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

TX_XAUI_A_LANE _SWTCHEN[3:0]

This bit enables per-lane switching on the next rising edge of FAILOVER_IMM or FAILOVER pin or register bit if the IPG_SWITCH bit is active. When the TX_XAUI_ P_LANE _SWTCHEN[*n*] bit corresponding to the lane is set to logic 1, that lane will switch from its current ACTIVELN[*n*] setting to the setting stored in STDBYLN[*n*] at the appropriate time.

TX_XAUI_B_LANE _SWTCHEN[3:0]

This bit enables per-lane switching on the next rising edge of FAILOVER_IMM or FAILOVER pin or register bit if the IPG_SWITCH bit is active. When the TX_XAUI_ R_LANE _SWTCHEN[*n*] bit corresponding to the lane is set to logic 1, that lane will switch from its current ACTIVELN[*n*] setting to the setting stored in STDBYLN[*n*] at the appropriate time.

Registers 0xD082: XC16 Busy

Bit	Type	Function	Default
15	R	TX_XAUI_B_LANE_BUSY[3]	0
14	R	TX_XAUI_B_LANE_BUSY[2]	0
13	R	TX_XAUI_B_LANE_BUSY[1]	0
12	R	TX_XAUI_B_LANE_BUSY[0]	0
11	R	TX_XAUI_A_LANE_BUSY[3]	0
10	R	TX_XAUI_A_LANE_BUSY[2]	0
9	R	TX_XAUI_A_LANE_BUSY[1]	0
8	R	TX_XAUI_A_LANE_BUSY[0]	0
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R	Reserved	0
2	R	Reserved	0
1	R	Reserved	0
0	R	Reserved	0

TX_XAUI_A_LANE_BUSY[3:0]

These bits indicate per lane switch status of port A Transmit XAUI data path when IPG Switching is enabled for the corresponding lane. When this bit is high, the lane is currently switching the lane or searching for an IPG. The XC16 will wait indefinitely attempting to match patterns and does not implement any timeout function. In such a condition, this bit will remain at logic 1 until the device is configured out of this condition either via FAILOVER_IMM, reset, or de-asserting the IPG_SWITCHEN bit.

TX_XAUI_B_LANE_BUSY[3:0]

These bits indicate per lane switch status of port B Transmit XAUI data path when IPG Switching is enabled for the corresponding lane. When this bit is high, the lane is currently switching the lane or searching for an IPG. The XC16 will wait indefinitely attempting to match patterns and does not implement any timeout function. In such a condition, this bit will remain at logic 1 until the device is configured out of this condition either via FAILOVER_IMM, reset, or de-asserting the IPG_SWITCHEN bit.

Registers 0xD083: XC16 IDLE Compare 0

Bit	Type	Function	Default
15	R/W	IDLE0_ENABLE	1
14	R/W	IDLE0_MASK9	1
13	R/W	IDLE0_MASK8	0
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	IDLE0[9]	0
8	R/W	IDLE0[8]	1
7	R/W	IDLE0[7]	0
6	R/W	IDLE0[6]	0
5	R/W	IDLE0[5]	0
4	R/W	IDLE0[4]	0
3	R/W	IDLE0[3]	0
2	R/W	IDLE0[2]	1
1	R/W	IDLE0[1]	1
0	R/W	IDLE0[0]	1

IDLE0[9:0]:

The IDLE0 register contains one of four possible IDLE values to be used for IPG detection during IPG switching. IDLE0 defaults to 0x107, the decoded idle column value for 10GE. IDLE0 register can be programmed with a different value if non-Ethernet data stream is being transported through XC16.

IDLE0_MASK8:

When IDLE0_MASK8 register bit is set to logic 1, bit 8 of IDLE0 pattern will be disregarded in the IPG detection . When set to logic 0, bit 8 of IDLE0 pattern will be taken into account in the IPG detection.

IDLE0_MASK9:

When IDLE0_MASK9 register bit is set to logic 1, bit 9 of IDLE0 pattern will be disregarded in the IPG detection. When set to logic 0, bit 9 of IDLE0 pattern will be taken into account in the IPG detection.

IDLE0_ENABLE:

When set to logic 1, the IDLE pattern defined in this register will be used in IPG detection during IPG switch. When set to logic 0, the idle pattern defined in this register will not be used in IPG detection.

Registers 0xD084: XC16 IDLE Compare 1

Bit	Type	Function	Default
15	R/W	IDLE1_ENABLE	0
14	R/W	IDLE1_MASK9	0
13	R/W	IDLE1_MASK8	0
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	IDLE1[9]	0
8	R/W	IDLE1[8]	0
7	R/W	IDLE1[7]	0
6	R/W	IDLE1[6]	0
5	R/W	IDLE1[5]	0
4	R/W	IDLE1[4]	0
3	R/W	IDLE1[3]	0
2	R/W	IDLE1[2]	0
1	R/W	IDLE1[1]	0
0	R/W	IDLE1[0]	0

IDLE1[9:0]:

The IDLE1 register contains one of four possible IDLE values to be used for IPG detection during IPG switching. IDLE1 register defaults to 0x000. It should be programmed with valid idle pattern when IDLE1 register is in use.

IDLE1_MASK8:

When IDLE1_MASK8 register bit is set to logic 1, bit 8 of IDLE1 pattern will be disregarded in the IPG detection. When set to logic 0, bit 8 of IDLE1 pattern will be taken into account in the IPG detection.

IDLE1_MASK9:

When IDLE1_MASK9 register bit is set to logic 1, bit 9 of IDLE1 pattern will be disregarded in the IPG detection. When set to logic 1, bit 9 of IDLE1 pattern will be taken into account in the IPG detection.

IDLE1_ENABLE:

When set to logic 1, the IDLE pattern defined in this register will be used in IPG detection during IPG switch. When set to logic 0, the idle pattern defined in this register will not be used in IPG detection.

Registers 0xD085: XC16 IDLE Compare 2

Bit	Type	Function	Default
15	R/W	IDLE2_ENABLE	0
14	R/W	IDLE2_MASK9	0
13	R/W	IDLE2_MASK8	0
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	IDLE2[9]	0
8	R/W	IDLE2[8]	0
7	R/W	IDLE2[7]	0
6	R/W	IDLE2[6]	0
5	R/W	IDLE2[5]	0
4	R/W	IDLE2[4]	0
3	R/W	IDLE2[3]	0
2	R/W	IDLE2[2]	0
1	R/W	IDLE2[1]	0
0	R/W	IDLE2[0]	0

IDLE2[9:0]:

The IDLE2 register contains one of four possible IDLE values to be used for IPG detection during IPG switching. IDLE2 register defaults to 0x000. It should be programmed with valid idle pattern when IDLE2 register is in use.

IDLE2_MASK8:

When IDLE2_MASK8 register bit is set to logic 1, bit 8 of IDLE2 pattern will be disregarded in the IPG detection. When set to logic 0, bit 8 of IDLE2 pattern will be taken into account in the IPG detection.

IDLE2_MASK9:

When IDLE2_MASK9 register bit is set to logic 1, bit 9 of IDLE2 pattern will be disregarded in the IPG detection. When set to logic 0, bit 9 of IDLE2 pattern will be taken into account in the IPG detection.

IDLE2_ENABLE:

When set to logic 1, the IDLE pattern defined in this register will be used in IPG detection during IPG switch. When set to logic 0, the idle pattern defined in this register will not be used in IPG detection.

Registers 0xD086: XC16 IDLE Compare 3

Bit	Type	Function	Default
15	R/W	IDLE3_ENABLE	0
14	R/W	IDLE3_MASK9	0
13	R/W	IDLE3_MASK8	0
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	IDLE3[9]	0
8	R/W	IDLE3[8]	0
7	R/W	IDLE3[7]	0
6	R/W	IDLE3[6]	0
5	R/W	IDLE3[5]	0
4	R/W	IDLE3[4]	0
3	R/W	IDLE3[3]	0
2	R/W	IDLE3[2]	0
1	R/W	IDLE3[1]	0
0	R/W	IDLE3[0]	0

IDLE3[9:0]:

The IDLE3 register contains one of four possible IDLE values to be used for IPG detection during IPG switching. IDLE3 register defaults to 0x000. It should be programmed with valid idle pattern when IDLE3 register is in use.

IDLE3_MASK8:

When IDLE3_MASK8 register bit is set to logic 1, bit 8 of IDLE3 pattern will be disregarded in the IPG detection. When set to logic 0, bit 8 of IDLE3 pattern will be taken into account in the IPG detection.

IDLE3_MASK9:

When IDLE3_MASK9 register bit is set to logic 1, bit 9 of IDLE3 pattern will be disregarded in the IPG detection. When set to logic 0, bit 9 of IDLE3 pattern will be taken into account in the IPG detection.

IDLE3_ENABLE:

When set to logic 1, the IDLE pattern defined in this register will be used in IPG detection during IPG switch. When set to logic 0, the idle pattern defined in this register will not be used in IPG detection.

Registers 0xD087: XC16 IDLE TX

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	IDLETX[9]	0
8	R/W	IDLETX[8]	1
7	R/W	IDLETX[7]	0
6	R/W	IDLETX[6]	0
5	R/W	IDLETX[5]	0
4	R/W	IDLETX[4]	0
3	R/W	IDLETX[3]	0
2	R/W	IDLETX[2]	1
1	R/W	IDLETX[1]	1
0	R/W	IDLETX[0]	1

IDLETX[9:0]:

The IDLETX register contains the IDLE word to be transmitted by the XC16 during an IPG switch interval. When a connection is broken on the active input lane during IPG switch, the XC16 will transmit the IDLETX word until an IPG is detected on the standby input lane, at which point the XC16 completes the new connection. This register defaults to 0x107, the decoded idle character for 10GE. This register can be programmed with a different value if non-Ethernet data stream is being transported through XC16.

Registers 0xD088: XC16 Lane Reset

Bit	Type	Function	Default
15	R/W	TX_XAUI_B_LANE RST[3]	0
14	R/W	TX_XAUI_B_LANE RST[2]	0
13	R/W	TX_XAUI_B_LANE RST[1]	0
12	R/W	TX_XAUI_B_LANE RST[0]	0
11	R/W	TX_XAUI_A_LANE RST[3]	0
10	R/W	TX_XAUI_A_LANE RST[2]	0
9	R/W	TX_XAUI_A_LANE RST[1]	0
8	R/W	TX_XAUI_A_LANE RST[0]	0
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

TX_XAUI_A_LANE_RST [3:0]

The reset bit is active high and is not self- clearing. When TX_XAUI_A_LANE_RST [*n*] is set to logic 0, output lane n operates normally. When TX_XAUI_A_LANE_RST [*n*] is set to logic 1, output lane n will be put into reset. Any switching session will be aborted. While in reset, the default value for ACTIVELN register will be restored on the output lane n. The actual input lane selected is still determined by the XOR'ing of ACTIVELN register and MUX_PRESET bits. While in reset, output lane n will be silenced. Lane that is under reset shall have no effect on other lanes unless the reset lane is configured to be part of trunk IPG operation. In that case, other lanes within the same trunk channel may be affected as well.

TX_XAUI_B LANE_RST [3:0]

The reset bit is active high and is not self- clearing. When TX_XAUI_B_LANE_RST [n] is set to logic 0, output lane n operates normally. When TX_XAUI_B_LANE_RST [n] is set to logic 1, output lane n will be put into reset. Any switching session will be aborted. While in reset, the default value for ACTIVELN register will be restored on the output lane n. The actual input lane selected is still determined by the XOR'ing of ACTIVELN register and MUX_PRESET bits. While in reset, output lane n will be silenced. Lane that is under reset shall have no effect on other lanes unless the reset lane is configured to be part of trunk IPG operation. In that case, other lanes within the same trunk channel may be affected as well.

Register 0xD089: XC16 Terminate Control Character 0

Bit	Type	Function	Default
15	R/W	T_CHAR0_ENABLE	1
14	R/W	T_CHAR0_MASK9	1
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	T_CHAR0[9]	0
8	R/W	T_CHAR0[8]	1
7	R/W	T_CHAR0[7]	1
6	R/W	T_CHAR0[6]	1
5	R/W	T_CHAR0[5]	1
4	R/W	T_CHAR0[4]	1
3	R/W	T_CHAR0[3]	1
2	R/W	T_CHAR0[2]	1
1	R/W	T_CHAR0[1]	0
0	R/W	T_CHAR0[0]	1

T_CHAR0[9:0]:

The Terminate character defined in this register is used for terminate column detection in trunk Ethernet data stream. Without this ability, trunk IPG switch may be started off prematurely corrupting trunk Ethernet data stream. This register must be programmed with a valid terminate character when switching trunkted Ethernet data. stream. T_CHAR0 defaults to 0x1FD, the decoded terminate character for 10GE. See Operations Section for operation details.

T_CHAR0_MASK9:

When set to logic 1, bit 9 of terminate character 0 pattern will be disregarded in terminate character matching. . When set to logic 0, bit 9 of terminate character 0 is used in terminate character matching.

T_CHAR0_ENABLE:

When set to logic 1, the terminate character 0 pattern will be included in terminate character matching to identify the terminate column. When set to logic 0, the register will be excluded from terminate character matching.

Register 0xD08A: XC16 Terminate Control Character 1

Bit	Type	Function	Default
15	R/W	T_CHAR1_ENABLE	0
14	R/W	T_CHAR1_MASK9	0
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9	R/W	T_CHAR1[9]	0
8	R/W	T_CHAR1[8]	0
7	R/W	T_CHAR1[7]	0
6	R/W	T_CHAR1[6]	0
5	R/W	T_CHAR1[5]	0
4	R/W	T_CHAR1[4]	0
3	R/W	T_CHAR1[3]	0
2	R/W	T_CHAR1[2]	0
1	R/W	T_CHAR1[1]	0
0	R/W	T_CHAR1[0]	0

T_CHAR1[9:0]:

The Terminate character defined in this register is used for terminate column detection in trunk Ethernet data stream. Without this ability, trunk IPG switch may be started off prematurely corrupting trunk Ethernet data stream. This register must be programmed with a valid terminate character when switching trunk Ethernet data. stream. T_CHAR1 defaults to 0x000. This register must programmed with valid terminate character when in use. See Operations Section for operation details.

T_CHAR0_MASK9:

When set to logic 1, bit 9 of terminate character 1 pattern will be disregarded in terminate character matching. . When set to logic 0, bit 9 of terminate character 1 is used in terminate character matching.

T_CHAR1_ENABLE:

When set to logic 1, the terminate character 1 pattern will be included in terminate character matching to identify the terminate column. When set to logic 0, the register will be excluded from terminate character matching.

Registers 0xD094, 0xD095, 0xD096, 0xD097: XC16 Standby

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R/W	STDBYLNB[3]	-
10	R/W	STDBYLNB[2]	-
9	R/W	STDBYLNB[1]	-
8	R/W	STDBYLNB[0]	-
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R/W	STDBYLNA[3]	-
2	R/W	STDBYLNA[2]	-
1	R/W	STDBYLNA[1]	-
0	R/W	STDBYLNA[0]	-

STDBYLNA[3:0]

The standby input select for the port A transmit XAUI lanes 0 and 2, and port B transmit XAUI lanes 0 and 2 in Standby Registers 0xD094, 0xD095, 0xD096, 0xD097 respectively. This value will become the active input for the lane if corresponding SWITCHEN in register 0xD081 is set. The assertion of FAILOVER_IMM will cause this latching to occur immediately, and the assertion of FAILOVER will cause this latching to occur during an Inter-Packet Gap (IPG), when FAILOVER is asserted. Refer to the Operation Section for details on this bit's functionality.

STDBYLNB[3:0]

The standby input select for the port A transmit XAUI lanes 1 and 3, and port B transmit XAUI lanes 1 and 3 in Standby Registers 0xD094, 0xD095, 0xD096, 0xD097 respectively. This value will become the active input for the lane if corresponding SWITCHEN bit in register 0xD081 is set. The assertion of FAILOVER_IMM will cause this latching to occur immediately, and the assertion of FAILOVER will cause this latching to occur during an Inter-Packet Gap (IPG). Please Refer to the Operation Section for details on this bit's functionality.

The following details the 4-bit vector assigned to each of the 2 data path inputs to the internal cross connect. Note that for a given lane to achieve the desired data source, 4-bit vectors below are the result of XOR'ing bits [3:2] of ACTIVELNA[3:0] or ACTIVELNB[3:0] with the MUX_PRESET TX_XAUI_A[1:0] or MUX_PRESET TX_XAUI_B[1:0] of register 0xD080 respectively.

Data Source	Lane 3 [3:0]	Lane 2 [3:0]	Lane 1 [3:0]	Lane 0 [3:0]
Port A Receive XAUI	0011	0010	0001	0000
Port B Receive XAUI	0111	0110	0101	0100

Registers 0xD0A4, 0xD0A5, 0xD0A6, 0xD0A7: XC16 Standby Active

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R	ACTIVELNB[3]	-
10	R	ACTIVELNB[2]	-
9	R	ACTIVELNB[1]	-
8	R	ACTIVELNB[0]	-
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3	R	ACTIVELNA[3]	-
2	R	ACTIVELNA[2]	-
1	R	ACTIVELNA[1]	-
0	R	ACTIVELNA[0]	-

ACTIVELNA[3:0]

This value is the current data path source for the port A transmit XAUI lanes 0 and 2, and port B transmit XAUI lanes 0 and 2 in Active Registers 0xD0A4, 0xD0A5, 0xD0A6, 0xD0A7 respectively. This value is updated with the value in STDBYLNA[3:0] on a successful switch operation. Refer to the Operation Section for details on this bit's functionality.

ACTIVELNB[3:0]

This value is the current data path source for the port A transmit XAUI lanes 1 and 3, and port B transmit XAUI lanes 1 and 3 in Active Registers 0xD0A4, 0xD0A5, 0xD0A6, 0xD0A7 respectively. . This value is updated with the value in STDBYLNB[3:0] on a successful switch operation. Refer to the Operation Section for details on this bit's functionality

The following details the 4-bit vector assigned to each of the 3 data path sources to the internal cross connect. Note that for a given lane to achieve the desired data source, 4-bit vectors below are the result of XOR'ing bits [3:2] of ACTIVELNA[3:0] or ACTIVELNB[3:0] with the MUX_PRESET TX_XAUI_A[1:0] or MUX_PRESET TX_XAUI_B[1:0] of register 0xD080 respectively.

Data Source	Lane 3 [3:0]	Lane 2 [3:0]	Lane 1 [3:0]	Lane 0 [3:0]
Port A Receive XAUI	0011	0010	0001	0000
Port B Receive XAUI	0111	0110	0101	0100

Registers 0xD0B0: CSU Configuration and Status Registers

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2	R/W	Reserved	0
1	R	LOCKV	-
0	R/W	LOCKE	-

LOCKE

The CSU Lock Interrupt Enable (LOCKE) bit controls the assertion of the CSU lock state interrupts by the CSU. When LOCKE is high, an interrupt is generated on the interrupt output (INTB) when the CSU lock state changes. Interrupts due to changes in the CSU lock state are masked when LOCKE is set low. Note: LOCKE only affects the *INTB* output. The LOCKI bit remains valid at all times.

LOCKV

The CSU Lock status bit (LOCKV) indicates whether the clock synthesis unit is currently locked with the reference clock, *REFCLK+/-*. LOCKV is set low when the CSU is not successfully locked with the reference clock, *REFCLK+/-*. LOCKV is set high when the CSU is locked with the reference clock.

Registers 0xD0B1: CSU Monitor and Interrupt Status Registers

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	R	Reserved	X
0	R	LOCKI	0

LOCKI

The CSU Lock Interrupt (LOCKI) status bit responds to changes in the CSU lock state. Interrupts are to be generated as the CSU achieves lock with the reference clock or loses lock to the reference clock. As a result, the LOCKI register bit is set high when any of these changes occur. The LOCKI bit is cleared according to the value of WCIMODE. If WCIMODE is "0", the LOCKI register bit is cleared the next time the LOCKI bit is read. If WCIMODE is "1", the LOCKI bit is cleared when a '1' is written to the LOCKI bit. When LOCKE is set high, LOCKI is used to produce the interrupt output (*INTB*). Whether or not the interrupt is masked by the LOCKE bit, the LOCKI bit remains valid and may be polled to detect change of lock status events.

Registers 0xD100, 0xD200: REFX Port A/Port B Global Control

Bit	Type	Function	Default
Bit 15	R	Unused	X
Bit 14	R/W	RESET_SW	0
Bit 13	R/W	FC_GEB_MODE_SW	0
Bit 12	R/W	TRUNK_LANEB_MODE_SW	0
Bit 11	R/W	IDLEDATA_ALIGN_SW	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	A_REPLACE_EN_SW	0
Bit 7	R/W	FAULT_REPLACE_EN_SW	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FIFO_DEPTH[3]	1
Bit 2	R/W	FIFO_DEPTH[2]	0
Bit 1	R/W	FIFO_DEPTH[1]	0
Bit 0	R/W	FIFO_DEPTH[0]	0

FIFO_DEPTH [3:0]

FIFO_DEPTH[3:0] programs the separation distance between the read and write pointers. Varying FIFO_DEPTH[3:0] varies the separation between the read and write pointers and thus would enable the RXFIFO to perform more clock compensation. Setting FIOF_DEPTH[3:0] to a value lower than the default value (08H) would result in the RXFIFO performing more deletion, while setting it to a value higher than the default value would result in the RXFIFO performing more insertion. The verified and allowable values for FIFO_DEPTH are 06H, 07H and 08H for Trunking mode and between 04H and 0CH for Lane based mode. This feature is useful for forcing rate compensation for validation purposes.

FAULT_REPLACE_EN_SW

Active high. When asserted, the in-band local fault and remote fault sequence ordered sets is replaced with the R_IDLE character /R/. If addtionally, EN_IDLE_REPLACE is also set the local and remote fault will be replaced with the XGMII idle character /I/.

This bit is XOR'ed with the FAULT_REPLACE_EN_MON bit to achieve the desired functionality

A_REPLACE_EN_SW

Active high. When asserted, the /A/ characters are replaced with the XGMII idle character /I/.

This bit is XOR'ed with the A_REPLACE_EN MON bit to achieve the desired functionality. .

IDLE_DATA_ALIGN_SW

Active high. When asserted, if in trunked mode, , results in de-skewing (alignment) using idle to data transition boundary rather than /A/ characters.

This bit is XOR'ed with the IDLE_DATA_ALIGN_MON bit to achieve the desired functionality

TRUNK_LANEB_MODE_SW

Active high. When asserted, the incoming data on the 4 lanes is trunked together and de-skewed (aligned). This is used for the incoming trunked data de-skewing. The four incoming lanes need to be frequency locked to each other however, can have a phase offset. The packet comparator and generator (PGC) and packet counter (PC) will also operate in trunked mode.

This bit is XOR'ed with the TRUNK_LANEB_MODE_MON bit to achieve the desired functionality

FC_GEB_MODE_SW

Fibre Channel operation mode that controls the block to be operated in 10GbE mode or 10GFC mode. When asserted, the mode of operation is 10GFC. When de-asserted, the mode of operation is 10GbE.

This bit is XOR'ed with the FC_GEB_MODE_MON bit to achieve the desired functionality.

RESET_SW

Global, active high software rest bit. When logic 1 the REFX is held in reset (excluding the software registers). This bit is not self clearing and must be written to logic 0 to take REFX out of reset. This bit is reset only by the *RSTB* pin.

Registers 0xD101, 0xD201: REFX Port A/Port B Global Monitor

Bit	Type	Function	Default
15	R/W	Reserved	0
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4	R	FC_GEB_MODE_MON	X
3	R	TRUNK_LANEB_MODE_MON	X
2	R	IDLEDATA_ALIGN_MON	X
1	R	A_REPLACE_EN_MON	X
0	R	FAULT_REPLACE_EN_MON	X

FAULT_REPLACE_EN_MON

FAULT_REPLACE_EN_MON is used in conjunction with the FAULT_REPLACE_EN_SW register bit to determine the desired configuration. See the FAULT_REPLACE_EN_SW register bit description for details.

A_REPLACE_EN_MON

A_REPLACE_EN_MON is used in conjunction with the A_REPLACE_EN_SW register bit to determine the desired configuration. See the A_REPLACE_EN_SW register bit description for details.

IDLEDATA_ALIGN_MON

IDLEDATA_ALIGN_MON is used in conjunction with the IDLEDATA_ALIGN_SW register bit to determine the desired configuration. See the IDLEDATA_ALIGN_SW register bit description for details.

TRUNK_LANEB_MODE_MON

TRUNK_LANEB_MODE_MON is used in conjunction with the TRUNK_LANEB_MODE_SW register bit to determine the desired configuration. See the TRUNK_LANEB_MODE_SW register bit description for details

FC_GEB_MODE_MON

FC_GEB_MODE_MON is used in conjunction with the FC_GEB_MODE_SW register bit to determine the desired configuration. See the FC_GEB_MODE_SW register bit description for details.

Registers 0xD102, 0xD202: REFX Port A/Port B PGC Threshold

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5	R/W	SYNC_THR[2]	1
4	R/W	SYNC _THR[1]	0
3	R/W	SYNC _THR[0]	0
2	R/W	LOSS_THR[2]	1
1	R/W	LOSS _THR[1]	0
0	R/W	LOSS _THR[0]	0

LOSS_THR[2:0]

The comparator will lose pattern synchronization if more than LOSS_THR + 1 consecutive error columns in trunk mode and consecutive error bytes in lane-based mode are detected.

SYNC_THR[2:0]

The comparator is guaranteed to gain pattern synchronization if SYNC_THR + 7 or more consecutive matching columns/bytes (trunk mode/lane-based mode) are detected. The comparator is guaranteed not to gain pattern synchronization if less than SYNC_THR + 1 consecutive matching columns/bytes (trunk mode/lane-based mode) are detected.

The match count includes matching the data loaded from the input data stream (which is 3 bytes in prbs23 lane mode and 1 byte in all other modes). Because of the above, SYNC_THR has to be more than 2.

Registers 0xD103, 0xD203: REFX Port A/Port B PGC Packet and Idle Length

Bit	Type	Function	Default
15	R/W	IDLE_LEN[3]	0
14	R/W	IDLE_LEN[2]	1
13	R/W	IDLE_LEN[1]	0
12	R/W	IDLE_LEN[0]	0
11	R/W	PACKET_LEN[11]	0
10	R/W	PACKET_LEN[10]	0
9	R/W	PACKET_LEN[9]	0
8	R/W	PACKET_LEN[8]	1
7	R/W	PACKET_LEN[7]	0
6	R/W	PACKET_LEN[6]	0
5	R/W	PACKET_LEN[5]	0
4	R/W	PACKET_LEN[4]	0
3	R/W	PACKET_LEN[3]	0
2	R/W	PACKET_LEN[2]	0
1	R/W	PACKET_LEN[1]	0
0	R/W	PACKET_LEN[0]	0

PACKET_LEN[11:0]

PACKET_LEN is the length of the packet -1 (in bytes for lane based mode and in columns for trunked mode and excluding ||S|| and ||T||) used when the generator or comparator is in framed mode.

IDLE_LEN[3:0]

IDLE_LEN is the length of the inter-packet-gap -1 (in bytes for lane based mode and in columns for trunked mode and excluding ||T||) used when the generator or comparator is in framed mode. It is ignored when PGC is in raw mode (unframed).

Registers 0xD104, 0xD204: REFX Port A/Port B 8B/10B Code Error Threshold

Bit	Type	Function	Default
15	R/W	CODE_ER_THR[15]	1
14	R/W	CODE_ER_THR[14]	1
13	R/W	CODE_ER_THR[13]	1
12	R/W	CODE_ER_THR[12]	1
11	R/W	CODE_ER_THR[11]	1
10	R/W	CODE_ER_THR[10]	1
9	R/W	CODE_ER_THR[9]	1
8	R/W	CODE_ER_THR[8]	1
7	R/W	CODE_ER_THR[7]	1
6	R/W	CODE_ER_THR[6]	1
5	R/W	CODE_ER_THR[5]	1
4	R/W	CODE_ER_THR[4]	1
3	R/W	CODE_ER_THR[3]	1
2	R/W	CODE_ER_THR[2]	1
1	R/W	CODE_ER_THR[1]	1
0	R/W	CODE_ER_THR[0]	1

CODE_ERR_THR[15:0]

This register holds the threshold value for 8B/10B disparity and code violations. When this value is either equaled or exceeded the HICERI interrupt bit for the corresponding lane is set.

Registers 0xD105, 0xD205: REFX Port A/Port B Packet Counter Control

Bit	Type	Function	Default
15	R/W	MUST_I	1
14	R/W	ALLOW_CNTRL	1
13	R/W	PKT_MIN_LEN [5]	1
12	R/W	PKT_MIN_LEN [4]	1
11	R/W	PKT_MIN_LEN [3]	1
10	R/W	PKT_MIN_LEN [2]	1
9	R/W	PKT_MIN_LEN [1]	1
8	R/W	PKT_MIN_LEN[0]	1
7	R/W	CNTRL[7]	1
6	R/W	CNTRL [6]	1
5	R/W	CNTRL [5]	1
4	R/W	CNTRL [4]	1
3	R/W	CNTRL [3]	1
2	R/W	CNTRL [2]	1
1	R/W	CNTRL [1]	1
0	R/W	CNTRL [0]	0

CNTRL [7:0]

CNTRL indicates the in-band control character optionally allowed by the packet counter.

PKT_MIN_LEN[5:0]

This is the minimum data packet size expected by the packet counter block. This refers to number of bytes in lane based mode and to the number of columns in trunked mode. Packet smaller then this size are counted as errored packets.

ALLOW_CNTRL

ALLOW_CNTRL indicates whether the packet counter counts the occurrence of the control character specified in CNTRL inside the data frame as an error or not. When ALLOW_CNTRL is logic 0, the packet counter will consider any control character (including CNTRL) inside a data packet as an error. When ALLOW_CNTRL is logic 1, the packet counter will consider any control character excluding CNTRL inside a data packet as an error.

MUST_I

When set to logic 1, the packet counter block expects at least one idle character (I_CHAR) – or column in trunked mode - between frames.

Registers 0xD106, 0xD206: REFX Port A/Port B Trunked Inserted Column Count

Bit	Type	Function	Default
15	R	INSERTED_COL[15]	X
14	R	INSERTED_COL[14]	X
13	R	INSERTED_COL[13]	X
12	R	INSERTED_COL[12]	X
11	R	INSERTED_COL[11]	X
10	R	INSERTED_COL[10]	X
9	R	INSERTED_COL[9]	X
8	R	INSERTED_COL[8]	X
7	R	INSERTED_COL[7]	X
6	R	INSERTED_COL[6]	X
5	R	INSERTED_COL[5]	X
4	R	INSERTED_COL[4]	X
3	R	INSERTED_COL[3]	X
2	R	INSERTED_COL[2]	X
1	R	INSERTED_COL[1]	X
0	R	INSERTED_COL[0]	X

INSERTED_COL[15:0]

INSERTED_COL[15:0] bits store the number of idle columns inserted across all four lanes in trunked mode. On a global monitor update, the value of the internal counter is transferred to this holding register, and the counter resets to 0x0000. This counter saturates at 0xFFFF. This register is applicable only in trunked mode.

Optionally, a write to this register will transfer all local REFX performance monitoring counter values (including this one) to their corresponding holding registers.

Registers 0xD107H, 0xD207H: REFX Port A/Port B Trunked Deleted Column Count

Bit	Type	Function	Default
Bit 15	R	DELETED_COL[15]	X
Bit 14	R	DELETED_COL[14]	X
Bit 13	R	DELETED_COL[13]	X
Bit 12	R	DELETED_COL[12]	X
Bit 11	R	DELETED_COL[11]	X
Bit 10	R	DELETED_COL[10]	X
Bit 9	R	DELETED_COL[9]	X
Bit 8	R	DELETED_COL[8]	X
Bit 7	R	DELETED_COL[7]	X
Bit 6	R	DELETED_COL[6]	X
Bit 5	R	DELETED_COL[5]	X
Bit 4	R	DELETED_COL[4]	X
Bit 3	R	DELETED_COL[3]	X
Bit 2	R	DELETED_COL[2]	X
Bit 1	R	DELETED_COL[1]	X
Bit 0	R	DELETED_COL[0]	X

DELETED_COL[15:0]

DELETED_COL[15:0]counter stores the number of idle columns deleted across all four lanes in trunked mode. This counter saturates at 0FFFF. On a global monitor update, the value of the counter is transferred to this holding register, and the counter resets to 0x0000. This register is applicable only in trunked mode.

Registers 0xD108, 0xD208: REFX Port A/Port B Interrupt Enable 1

Bit	Type	Function	Default
15		Unused	X
14	R/W	RF_DETE	0
13	R/W	LF_DETE	0
12	R/W	ALIGN_ERRE	0
11	R/W	HICERE[3]	0
10	R/W	HICERE[2]	0
9	R/W	HICERE[1]	0
8	R/W	HICERE[0]	0
7	R/W	SDE[3]	0
6	R/W	SDE[2]	0
5	R/W	SDE[1]	0
4	R/W	SDE[0]	0
3	R/W	SYNC_ERRE[3]	0
2	R/W	SYNC_ERRE[2]	0
1	R/W	SYNC_ERRE[1]	0
0	R/W	SYNC_ERRE[0]	0

SYNC_ERRE[3:0]

When SYNC_ERRE for the corresponding lane is set to logic 1, the assertion of SYNC_ERRI for that lane will cause the INTB output signal to be asserted. When SYNC_ERRE for the corresponding is set to logic 0, the assertion of SYNC_ERRI for that lane will not cause the *INTB* output to be asserted. These bits have no effect on SYNC_ERRI.

SDE[3:0]

When SDE for the corresponding lane is set to logic 1, the assertion of SDI for that lane will cause the *INTB* output signal to be asserted. When SDE for the corresponding lane is set to logic 0, the assertion of SDI for that lane will not cause the *INTB* output to be asserted. These bits have no effect on SDI.

HICERE[3:0]

When HICERE for the corresponding lane is set to logic 1, the assertion of HICERI for that lane will cause the *INTB* output signal to be asserted. When HICERE for the corresponding lane is set to logic 0, the assertion of HICERI for that lane will not cause the *INTB* output to be asserted. These bits have no effect on HICERI.

ALIGN_ERRE

When ALIGN_ERRE is set to logic 1, the assertion of ALIGN_ERRI will cause the *INTB* output signal to be asserted. When ALIGN_ERRE is set to logic 0, the assertion of ALIGN_ERRI will not cause the *INTB* output to be asserted. This bit has no effect on ALIGN_ERRI.

LF_DETE

When LF_DETE is set to logic 1, the assertion of LF_DETI will cause the *INTB* output signal to be asserted. When LF_DETE is set to logic 0, the assertion of LF_DETI will not cause the *INTB* output to be asserted. This bit has no affect on LF_DETI.

RF_DETE

When RF_DETE is set to logic 1, the assertion of RF_DETI will cause the *INTB* output signal to be asserted. When RF_DETE is set to logic 0, the assertion of RF_DETI will not cause the *INTB* output to be asserted. This bit has no effect on RF_DETI.

Registers 0xD109, 0xD209: REFX Port A/Port B Interrupt Enable 2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R/W	OVERRUNE[3]	0
6	R/W	OVERRUNE[2]	0
5	R/W	OVERRUNE[1]	0
4	R/W	OVERRUNE[0]	0
3	R/W	UNDERRUNE[3]	0
2	R/W	UNDERRUNE[2]	0
1	R/W	UNDERRUNE[1]	0
0	R/W	UNDERRUNE[0]	0

UNDERRUNE[3:0]

When UNDERRUNE for the corresponding lane is set to logic 1, the assertion of UNDERRUNI for that lane will cause the *INTB* output signal to be asserted. When UNDERRUNE for the corresponding lane is set to logic 0, the assertion of UNDERRUNI for that lane will not cause the *INTB* output to be asserted. These bits have no effect on UNDERRUNI.

OVERRUNE[3:0]

When OVERRUNE for the corresponding lane is set to logic 1, the assertion of OVERRUNI for that lane will cause the *INTB* output signal to be asserted. When OVERRUNE for the corresponding lane is set to logic 0, the assertion of OVERRUNI for that lane will not cause the *INTB* output to be asserted. These bits have no effect on OVERRUNI.

Registers 0xD10A, 0xD20A: REFX Port A/Port B Interrupt Enable 3

Bit	Type	Function	Default
15	R/W	PC_ERRE[3]	0
14	R/W	PC_ERRE[2]	0
13	R/W	PC_ERRE[1]	0
12	R/W	PC_ERRE[0]	0
11	R/W	PGC_ERRE[3]	0
10	R/W	PGC_ERRE[2]	0
9	R/W	PGC_ERRE[1]	0
8	R/W	PGC_ERRE[0]	0
7	R/W	PGC_SYNCE[3]	0
6	R/W	PGC_SYNCE[2]	0
5	R/W	PGC_SYNCE[1]	0
4	R/W	PGC_SYNCE[0]	0
3	R/W	PGC_FRAME_SYNCE[3]	0
2	R/W	PGC_FRAME_SYNCE[2]	0
1	R/W	PGC_FRAME_SYNCE[1]	0
0	R/W	PGC_FRAME_SYNCE[0]	0

PGC_FRAME_SYNCE[3:0]

PGC_FRAME_SYNCE allows changes in PGC_FRAME_SYNCI for the corresponding lane to cause an interrupt on the *INTB* pin. These bits have no effect on PGC_FRAME_SYNCI.

PGC_SYNCE[3:0]

PGC_SYNCE allows changes in PGC_SYNCI for the corresponding lane to cause an interrupt on the *INTB* pin. These bits have no effect on PGC_SYNCI.

PGC_ERRE[3:0]

PGC_ERRE allows changes in PGC_ERRI for the corresponding lane to cause an interrupt on the *INTB* pin. These bits have no effect on PGC_ERRI.

PC_ERRE[3:0]

PC_ERRE allows changes in PC_ERREI for the corresponding lane to cause an interrupt on the *INTB* pin. These bits have no effect on PGC_ERRI.

Registers 0xD10B, 0xD20B: REFX Port A/Port B Interrupt Status 1

Bit	Type	Function	Default
15		unused	X
14	R	RF_DETI	X
13	R	LF_DETI	X
12	R	ALIGN_ERRI	X
11	R	HICERI[3]	X
10	R	HICERI[2]	X
9	R	HICERI[1]	X
8	R	HICERI[0]	X
7	R	SDI[3]	X
6	R	SDI[2]	X
5	R	SDI[1]	X
4	R	SDI[0]	X
3	R	SYNC_ERRI[3]	X
2	R	SYNC_ERRI[2]	X
1	R	SYNC_ERRI[1]	X
0	R	SYNC_ERRI[0]	X

SYNC_ERRI[3:0]

When set to logic 1, indicates the transition of byte alignment for the corresponding lane from aligned to the word boundary to unaligned. SYNC_ERRI is set to logic 0 when this register is read (WCIMODE = 0) or a 1 is written to it (WCIMODE= 1).

SDI[3:0]

The Signal Detect interrupt event indication (SDI) transitions to logic 1 when the corresponding lane transitions into the loss of signal state. The loss of signal state on a lane is declared when the corresponding signal detect transitions from a logic 1 to a logic 0 value. SDI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1).

HICERI[3:0]

When set to logic 1, indicates that the number of 8B/10B code errors received on respective lane has exceeded or equaled the value programmed in the CODE_ERR_THRESHOLD Register. HICERI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1).

ALIGN_ERRI

When set to logic 1, indicates the transition of word alignment state across the four lanes for trunked modes from aligned to unaligned. ALIGN_ERRI is set to logic 0 when this register is read (WCIMODE = 0) or a 1 is written to it (WCIMODE= 1).

LF_DETI

When LF_DETI is set to logic 1, indicates the detection of a local fault in the trunked data stream. LF_DETI is set to logic 0 when this register is read (WCIMODE = 0) or a 1 is written to it (WCIMODE= 1).

RF_DETI

When RF_DETI is set to logic 1, indicates the detection of a remote fault in the trunked data stream. RF_DETI is set to logic 0 when this register is read (WCIMODE = 0) or a 1 is written to it (WCIMODE= 1).

Registers 0xD10C, 0xD20C: REFX Port A/Port B Interrupt Status 2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R	OVERRUNI[3]	X
6	R	OVERRUNI[2]	X
5	R	OVERRUNI[1]	X
4	R	OVERRUNI[0]	X
3	R	UNDERRUNI[3]	X
2	R	UNDERRUNI[2]	X
1	R	UNDERRUNI[1]	X
0	R	UNDERRUNI[0]	X

UNDERRUNI[3:0]

When set to logic 1, indicates that the receive FIFO within corresponding lane had an underrun condition (read pointer 1 position before write pointer) occur. UNDERRUNI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1). In lane based mode, any FIFO that underruns will be reset. In trunked mode, any FIFO that underruns will cause all the FIFOs to be reset.

OVERRUNI[3:0]

When set to logic 1, indicates that the receive FIFO within corresponding lane had an overrun condition (read pointer 1 position after write pointer) occur. OVERRUNI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1). In lane based mode, any FIFO that overrruns will be reset. In trunked mode, any FIFO that overruns will cause all the FIFOs to be reset.

Registers 0xD10D, 0xD20D: REFX Port A/Port B Interrupt Status 3

Bit	Type	Function	Default
15	R	PC_ERRI[3]	X
14	R	PC_ERRI[2]	X
13	R	PC_ERRI[1]	X
12	R	PC_ERRI[0]	X
11	R	PGC_ERRI[3]	X
10	R	PGC_ERRI[2]	X
9	R	PGC_ERRI[1]	X
8	R	PGC_ERRI[0]	X
7	R	PGC_SYNCI[3]	X
6	R	PGC_SYNCI[2]	X
5	R	PGC_SYNCI[1]	X
4	R	PGC_SYNCI[0]	X
3	R	PGC_FRAME_SYNCI[3]	X
2	R	PGC_FRAME_SYNCI[2]	X
1	R	PGC_FRAME_SYNCI[1]	X
0	R	PGC_FRAME_SYNCI[0]	X

PGC_FRAME_SYNCI[3:0]

PGC_FRAME_SYNCI indicates that PGC_FRAME_SYNCV has changed. When set to logic 1, indicates that the PGC for the corresponding lane has gained or lost frame synchronization. In trunked mode, only lane 0 bit is valid. PGC_FRAME_SYNCI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1).

PGC_SYNCI[3:0]

PGC_SYNCI indicates that PGC_SYNCV has changed. When set to logic 1, indicates that the PGC for the corresponding lane has gained or lost pattern synchronization. In trunked mode, only lane 0 bit is valid. PGC_SYNCI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1).

PGC_ERRI[3:0]

PGC_ERRI is asserted every time the PGC for the corresponding lane detects an error in the received pattern. In trunked mode, only lane 0 bit is valid. PGC_ERRI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1).

PC_ERRI[3:0]

PC_ERRI is asserted every time the packet counter for the corresponding lane detects an errored packet. In trunked mode, only lane 0 bit is valid. PC_ERRI is set to logic 0 when this register is read (WCIMODE = 0) or a logic 1 is written to it (WCIMODE = 1).

Registers 0xD10E, 0xD20E: REFX Port A/Port B Status 1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R	RF_DETV	X
Bit 13	R	LF_DETV	X
Bit 12	R	ALIGN_ERRV	X
Bit 11	R	HICERV[3]	X
Bit 10	R	HICERV[2]	X
Bit 9	R	HICERV[1]	X
Bit 8	R	HICERV[0]	X
Bit 7	R	SDV[3]	X
Bit 6	R	SDV[2]	X
Bit 5	R	SDV[1]	X
Bit 4	R	SDV[0]	X
Bit 3	R	SYNC_ERRV[3]	X
Bit 2	R	SYNC_ERRV[2]	X
Bit 1	R	SYNC_ERRV[1]	X
Bit 0	R	SYNC_ERRV[0]	X

SYNC_ERRV[3:0]

When logic 1, indicates that byte alignment for trunked mode within respective lane has been lost. When set to logic 0, indicates that byte alignment within respective lane has been acquired or disabled.

SDV[3:0]

The Signal Detect status signal (SDV) reflects the current value of respective lane signal detect input.

HICERV[3:0]

When logic 1, indicates that the current number of 8B/10B code errors received on respective lane is greater than or equal to the value programmed in the CODE_ERR_THRESHOLD register. When logic 0, indicates that the current number of 8B/10B code errors received on respective lane is less than the value programmed in the CODE_ERR_THRESHOLD register

ALIGN_ERRV

When logic 1, indicates that word alignment (de-skew) across the four lanes for trunked mode has been lost. When logic 0, indicates that word alignment has been acquired or disabled.

LF_DETV

This signal reflects the current value of LF_DET output. When logic 1, indicates a local fault is currently present on the output data irrespective of idle replacement. When logic 0, indicates a local fault is not currently present of the output. This bit is only applicable in trunked mode.

RF_DETV

This signal reflects the current value of RF_DET output. When logic 1, indicates a local fault is currently present on the output data irrespective of idle replacement. When logic 0, indicates a local fault is not currently present of the output. This bit is only applicable in trunked mode.

Registers 0xD10F, 0xD20F: REFX Port A/Port B Status 2

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	R	OVERRUNV[3]	X
6	R	OVERRUNV[2]	X
5	R	OVERRUNV[1]	X
4	R	OVERRUNV[0]	X
3	R	UNDERRUNV[3]	X
2	R	UNDERRUNV[2]	X
1	R	UNDERRUNV[1]	X
0	R	UNDERRUNV[0]	X

UNDERRUNV[3:0]

When logic 1, indicates the FIFO in the respective lane is currently experiencing an underrun (read pointer one position before the write pointer). When logic 0, indicates the FIFO in the respective lane is not currently experiencing an underrun. In lane based mode, any FIFO that underruns will be reset. In trunked mode, any FIFO that underruns will cause all the FIFOs to be reset.

OVERRUNV[3:0]

When logic 1, indicates the FIFO in the respective lane is currently experiencing an overrun (read pointer one position after the write pointer). When logic 0, indicates the FIFO in the respective lane is not currently experiencing an overrun. In lane based mode, any FIFO that overruns will be reset. In trunked mode, any FIFO that overruns will cause all the FIFOs to be reset.

Registers 0xD110, 0xD210: REFX Port A/Port B Status 3

Bit	Type	Function	Default
15	R	PC_ERRV[3]	X
14	R	PC_ERRV[2]	X
13	R	PC_ERRV[1]	X
12	R	PC_ERRV[0]	X
11	R	PGC_ERRV[3]	X
10	R	PGC_ERRV[2]	X
9	R	PGC_ERRV[1]	X
8	R	PGC_ERRV[0]	X
7	R	PGC_SYNCV[3]	X
6	R	PGC_SYNCV[2]	X
5	R	PGC_SYNCV[1]	X
4	R	PGC_SYNCV[0]	X
3	R	PGC_FRAME_SYNCV[3]	X
2	R	PGC_FRAME_SYNCV[2]	X
1	R	PGC_FRAME_SYNCV[1]	X
0	R	PGC_FRAME_SYNCV[0]	X

PGC_FRAME_SYNCV[3:0]

When logic 1, indicates the associated lane comparator is currently frame synchronized. When logic 0, indicates the associated comparator is not currently frame synchronized. . PGC detector will declare frame synchronization after one packet of the required size with PGC_S (Start) and PGC_T (Terminate) columns is received. The PGC detector will declare loss of frame synchronization after one packet with an incorrect size, PGC_S or PGC_T columns is received. Only lane 0 bit is applicable in trunked mode.

PGC_SYNCV[3:0]

When logic 1, indicates the associated lane comparator is currently pattern synchronized. When logic 0, indicates the associated comparator is not currently pattern synchronized. The PGC detector will declare pattern synchronization after frame synchronization is gained and SYNC_THR consecutive matching data columns are detected. The PGC detector will declare loss of pattern synchronization if frame synchronization is lost or SYNC_LOSS consecutive data column mismatches are detected. Only lane 0 bit is applicable in trunked mode.

PGC_ERRV[3:0]

When logic 1, indicates the current byte being processed by the associated lane comparator did not match the expected pattern value. When logic 0, indicates the current byte being processed by the associated lane comparator matched the expected pattern value. When PGC for a lane is out of frame or pattern sync, PGC_ERRV for that lane is set to 0. In trunked mode, only lane 0 bit is valid.

PC_ERRV[3:0]

When logic 1, indicates the current packet being processed by the associated lane packet counter violated at least one of the rules in Section 14.4.5. When logic 0, indicates the current packet being processed by the associated packet counter did not violate any of the rules in the operations section. In trunked mode, only lane 0 bit is valid.

Register 0xD119, 0xD219: REFX TIP Mask

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7	RW	WRCLK_MASKB[3]	1
6	RW	WRCLK_MASKB[2]	1
5	RW	WRCLK_MASKB[1]	1
4	RW	WRCLK_MASKB[0]	1
3	RW	RDCLK_MASKB[3]	1
2	RW	RDCLK_MASKB[2]	1
1	RW	RDCLK_MASKB[1]	1
0	RW	RDCLK_MASKB[0]	1

RDCLK_MASKB[3:0]

Active low read clock tip mask. If the READ_CLK of lane n is not toggling, then RDCLK_MASKB[n] must be set to logic 0 to avoid freezing the TIP output and performance counters. Otherwise RDCLK_MASKB[n] must be set to logic 1 for correct operation of the TIP output and correct updating of the performance counters.

WRCLK_MASKB[3:0]

Active low write clock tip mask. If the WRITE_CLK of lane n is not toggling, then WRCLK_MASKB[n] must be set to logic 0 to avoid freezing the TIP output and performance counters. Otherwise WRCLK_MASKB[n] must be set to logic 1 for correct operation of the TIP output and correct updating of the performance counters.

Registers 0xD140, 0xD150, 0xD160, 0xD170, 0xD240, 0xD250, 0xD260, 0xD270: REFX Port A Lanes 0-3 and Port B Lanes 0-3 Control

Bit	Type	Function	Default
15	R/W	PKT_GEN_EN	0
14	R/W	PKT_COMP_EN	0
13		Unused	X
12		Unused	X
11	R/W	Reserved	0
10		Unused	X
9	R/W	PACKET_COUNTER_EN	0
8	R/W	INV_SW	0
7	R/W	SWIZZLE_SW	0
6	R/W	SERDES_8BIT_EN_SW	0
5	R/W	IDLE_REPLACE_EN_SW	0
4	R/W	INVLD_REPLACE_EN_SW	0
3	R/W	Reserved	0
2	R/W	DECODE_EN_SW	0
1	R/W	BYTE_ALIGN_EN_SW	0
0	R/W	RATE_COMP_EN_SW	0

RATE_COMP_EN_SW

Active high. When asserted, the clock rate compensation through idle insert and delete is enabled. REFX is able to handle up to ±200 ppm offset between write clock and read clock.

The bit for each lane is XOR'ed with it's RATE_COMP_EN_MON bit to achieve the desired functionality.

BYTE_ALIGN_EN_SW

Active high. When asserted, byte alignment is enabled on the corresponding lane. Byte alignment is done on 8B/10B encoded comma sequences.

The bit for each lane is XOR'ed with it's BYTE_ALIGN_EN_MON bit to achieve the desired functionality.

DECODE_EN_SW

Active high. When asserted, data for the corresponding lane, in lane-based mode, is decoded. When de-asserted, , data for the corresponding lane, is not decoded.

The bit for each lane is XOR'ed with it's DECODE_EN_MON bit to achieve the desired functionality.

INVLD_REPLACE_EN_SW

Active high. When asserted, if the code violation or disparity error is detected, the corresponding character on the corresponding lane is replaced by the XGMII error character K30.7.

The bit for each lane is XOR'ed with it's INVLD_REPLACE_EN_MON bit to achieve the desired functionality.

IDLE_REPLACE_EN_SW

Active high. When asserted, the idle characters /K/ and /R/ are replaced with the XGMII idle character /I/.

The bit for each lane is XOR'ed with its IDLE_REPLACE_EN_MON bit to achieve the desired functionality.

SERDES_8BIT_EN_SW

SERDES_8BIT_EN_SW[n] specifies an 8 bit swizzling of the bit order on a given lane. When SERDES_8BIT_EN_SW [n] is logic 1, lane n is configured for an 8 bit swizzle (bits 10 and 9 are ignored) when the XOR'ed result of SWIZZLE_MON and SWIZZLE_SW[n] is logic 1. When SERDES_8BIT_EN_SW [n] is logic 0, lane n is configured for a 10 bit swizzle, when the XOR'ed result of SWIZZLE_MON and SWIZZLE[n] is logic 1.

This bit is XOR'ed with it's SERDES_8BIT_EN_MON bit to achieve the desired functionality

SWIZZLE_SW

SWIZZLE_SW[n] enables the swizzling of the bit order on a given lane. When SWIZZLE_SW[n] is logic 1, lane n has its bit order reversed as specified by SERDES_8BIT_EN_SW[n].

The bit for each lane is XOR'ed with the SWIZZLE_MON bit to achieve the desired functionality

INV_SW

INV_SW enables the inversion of the input data on a given lane. When INV_SW[n] is logic 1, lane n has its data inverted.

The bit for each lane is XOR'ed with the INV_MON bit to achieve the desired functionality

PACKET_COUNTER_EN

When PACKET_COUNTER _EN is logic 1, the packet counter is enabled to count total and errored packets.

For Trunked Mode operation, lane 0's PACKET_COUNTER_EN is sufficient for control across all 4 lanes of the trunked link.

PKT_COMP_EN

PKT_COMP_EN when set to logic 1, the comparator block will be enabled. Payload errors are counted only after frame and pattern synchronization are achieved. The number of errored bytes is recorded in the 8 bit error counter for that channel. These counters count from 00H to FFH where upon they saturate until reset or until the positive edge of the TIP register bit. No checking of the idle stream is done. The packet comparator logic is disabled when PKT_COMP_EN is set to logic 0. In trunked mode, only lane 0 bits are relevant.

For Trunked Mode operation, lane 0's PKT_COMP_EN is sufficient for control across all 4 lanes of the trunked link

PKT_GEN_EN

PKT_GEN_EN will enable the packet generator logic when set to a logic 1. The pattern generated when PKT_GEN_EN is set to a logic 1 is controlled by the PATT[3:0] bits. The packet generator logic is disabled when PKT_GEN_EN is set to a logic 0.

Each bit is XOR'ed with corresponding TEST_PATT_EN input pin. TEST_PATT_EN should be de-asserted if the mode is register controlled. In trunked mode, only lane 0 bit is relevant.

For Trunked Mode operation, lane 0, lane 1, lane2,and lane 3's assoicated PKT_GEN_EN bits must be configured to the common desired value for expected operation. It is not sufficient to program only lane0's PKT_GEN_EN for operation in trunked mode

Registers 0xD141, 0xD151H, 0xD161, 0xD171, 0xD241, 0xD251, 0xD261, 0xD271: REFX Port A Lanes 0-3 and Port B Lanes 0-3 Monitor

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8	R	SWIZZLE_MON	-
7	R	INV_MON	-
6	R	SERDES_8BIT_EN_MON	-
5	R	IDLE_REPLACE_EN_MON	-
4	R	INVLD_REPLACE_EN_MON	-
3	R	Reserved	-
2	R	DECODE_EN_MON	-
1	R	BYTE_ALIGN_EN_MON	-
0	R	RATE_COMP_EN_MON	-

RATE_COMP_EN_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. RATE_COMP_EN_MON is used in conjunction with the RATE_COMP_EN_SW register bit to determine the desired configuration. See the RATE_COMP_EN_SW register bit description for details.

BYTE_ALIGN_EN_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. BYTE_ALIGN_EN_MON is used in conjunction with the BYTE_ALIGN_EN_SW register bit to determine the desired configuration. See the BYTE_ALIGN_EN_SW register bit description for details.

DECODE_EN_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. DECODE_EN_MON is used in conjunction with the DECODE_EN _SW register bit to determine the desired configuration. See the DECODE _EN_SW register bit description for details

INVLD_REPLACE_EN_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. INVLD_REPLACE_EN_MON is used in conjunction with the INVLD_REPLACE_EN_SW register bit to determine the desired configuration. See the INVLD_REPLACE_EN_SW register bit description for details

IDLE_REPLACE_EN_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. IDLE_REPLACE_EN_MON is used in conjunction with the IDLE_REPLACE_EN_SW register bit to determine the desired configuration. See the IDLE_REPLACE_EN_SW register bit description for details

SERDES_8BIT_EN_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. SERDES_8BIT_EN_MON is used in conjunction with the SERDES_8BIT_EN_SW register bit to determine the desired configuration. See the SERDES_8BIT_EN_SW register bit description for details

INV_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. INV_MON is used in conjunction with the INV_SW register bit to determine the desired configuration. See the INV_SW register bit description for details.

SWIZZLE_MON

The state of this bit reflects the configuration of the device as determined by device pins or top level registers. SWIZZLE_MON is used in conjunction with the SWIZZLE_SW register bit to determine the desired configuration. See the SWIZZLE_SW register bit description for details

Registers 0xD142, 0xD152, 0xD162, 0xD172, 0xD242, 0xD252, 0xD262, 0xD272: REFX Port A Lanes 0-3 and Port B Lanes 0-3 PGC Control

Bit	Type	Function	Default
15	R/W	FIXED_PATT[9]	0
14	R/W	FIXED_PATT[8]	0
13	R/W	FIXED_PATT[7]	0
12	R/W	FIXED_PATT[6]	0
11	R/W	FIXED_PATT[5]	0
10	R/W	FIXED_PATT[4]	0
9	R/W	FIXED_PATT[3]	0
8	R/W	FIXED_PATT[2]	0
7	R/W	FIXED_PATT[1]	0
6	R/W	FIXED_PATT[0]	0
5	R/W	FRAMED_MODE	0
4	R/W	PATT[3]	0
3	R/W	PATT[2]	0
2	R/W	PATT[1]	0
1	R/W	PATT[0]	0
0	R/W	FRC_ERR	0

FRC_ERR

FRC_ERR enables the forcing of a single byte error on the corresponding lane when set to logic 1. The FRC_ERR bit is internally positive edge-detected and is not self-clearing. Hence logic 0 has to be written into this register location before logic 1 is written into it for forcing an error. FRC_ERR is ignored when PKT_GEN_EN is set to logic 0. Note that FRC_ERR will also be ignored if PATT[1:0] = "0100" (CRPAT repeated) or PATT[1:0]="0101"(CJPAT repeated).

PATT[3:0]

PATT[3:0] determines the pattern that the Packet Generator transmits and what the Pattern comparator compares against. Please refer to the table below for details. The comparator can only compare against raw or framed counting, fixed (framed only) and PRBS patterns. The generator can generate all the patterns below.

Table 15 PATT Register Bits Decode

PATT[3]	PATT[2]	PATT[1]	PATT[0]	Pattern
0	0	0	0	/D21.5/ (0B5) repeated (high frequency pattern)
0	0	0	1	/K28.7/ (1FC) repeated (low frequency pattern)

0	0	1	0	/K28.5/ (1BC) repeated (mixed frequency pattern)
0	0	1	1	Counting Pattern
0	1	0	0	CRPAT repeated
0	1	0	1	CJPAT repeated
0	1	1	0	PRBS 7
0	1	1	1	PRBS 23 (inverted)
1	0	0	0	Fixed Pattern

PATT[1:0] are XOR'ed with TX_TEST_PATT_SEL[1:0]] in register 0x0019 or 0xC0019. In trunked mode, only lane 0 bits are relevant.

FRAMED_MODE

FRAMED_MODE will enable the packet generator and comparator to operate in framed mode. The pattern generated and comparator will operate in framed mode when FRAMED_MODE is set to a logic 1. The pattern generated and comparator will operate in raw mode when FRAMED_MODE is set to a logic 0. Framed mode is only applicable to counting, fixed and PRBS patterns. If 8b10b coding is not used in raw mode then the comparator can only detect prbs patterns (prbs is self aligning but all the other patterns are not). In trunked mode the FRAMED_MODE register bits for all the lanes must be asserted.

FIXED_PATT[9:0]

FIXED_PATT[9:0] is the pattern used when the PATT[3:0] bits are 1000. In lane base mode FIXED_PATT[8] must be set to 0. In trunk mode, FIXED_PATT[9:8] must be set to 0.

Registers 0xD143, 0xD153, 0xD163, 0xD173, 0xD243, 0xD253, 0xD263, 0xD273: REFX Port A Lanes 0-3 and Port B Lanes 0-3 PGC Error Count

Bit	Type	Function	Default
15	R	Unused	X
14	R	Unused	X
13	R	Unused	X
12	R	Unused	X
11	R	Unused	X
10	R	Unused	X
9	R	Unused	X
8	R	Unused	X
7	R	PGC_ERR_COUNT [7]	X
6	R	PGC_ERR_COUNT[6]	X
5	R	PGC_ERR_COUNT[5]	X
4	R	PGC_ERR_COUNT[4]	X
3	R	PGC_ERR_COUNT[3]	X
2	R	PGC_ERR_COUNT[2]	X
1	R	PGC_ERR_COUNT[1]	X
0	R	PGC_ERR_COUNT[0]	X

PGC_ERR_COUNT[7:0]

The PGC_ERR_COUNT[7:0] forms an 8-bit counter that records the number of errored bytes received on respective lane when the Packet Comparator is enabled. When the counter hits 0xFF, it saturates and will only clear on reset, or on a global monitor update. Errors are not accumulated when the packet detector is out of frame or pattern synchronization. In trunked mode, only lane 0 register is applicable and it indicates the column count instead of the byte count.

Registers 0xD144, 0xD154, 0xD164, 0xD174, 0xD244, 0xD254, 0xD264, 0xD274: REFX Port A Lanes 0-3 and Port B Lanes 0-3 8B/10B Error Count

Bit	Type	Function	Default
15	R	CODE_ERR[15]	X
14	R	CODE_ERR[14]	X
13	R	CODE_ERR[13]	X
12	R	CODE_ERR[12]	X
11	R	CODE_ERR[11]	X
10	R	CODE_ERR[10]	X
9	R	CODE_ERR[9]	X
8	R	CODE_ERR[8]	X
7	R	CODE_ERR[7]	X
6	R	CODE_ERR[6]	X
5	R	CODE_ERR[5]	X
4	R	CODE_ERR[4]	X
3	R	CODE_ERR[3]	X
2	R	CODE_ERR[2]	X
1	R	CODE_ERR[1]	X
0	R	CODE_ERR[0]	X

CODE_ERR[15:0]

CODE_ERR[15:0] counter stores the 8B/10B code and disparity violations found for respective lane. This counter saturates at 0xFFFF. On a global monitor update, the value of the counter is transferred to this holding register, and the counter resets to 0x00. This register must be polled every second to avoid saturation in a 10^{-3} bit error rate environment.

Registers 0xD145, 0xD155, 0xD165, 0xD175, 0xD245, 0xD255, 0xD265, 0xD275: REFX Port A Lanes 0-3 and Port B Lanes 0-3 Packet Error Count

Bit	Type	Function	Default
15	R	ERROR_PKT_CNT[15]	X
14	R	ERROR_PKT_CNT[14]	X
13	R	ERROR_PKT_CNT[13]	X
12	R	ERROR_PKT_CNT[12]	X
11	R	ERROR_PKT_CNT[11]	X
10	R	ERROR_PKT_CNT[10]	X
9	R	ERROR_PKT_CNT[9]	X
8	R	ERROR_PKT_CNT[8]	X
7	R	ERROR_PKT_CNT[7]	X
6	R	ERROR_PKT_CNT[6]	X
5	R	ERROR_PKT_CNT[5]	X
4	R	ERROR_PKT_CNT[4]	X
3	R	ERROR_PKT_CNT[3]	X
2	R	ERROR_PKT_CNT[2]	X
1	R	ERROR_PKT_CNT[1]	X
0	R	ERROR_PKT_CNT[0]	X

ERROR_PKT_CNT[15:0]

Error[15:0] is the number of errored packets (packets that violate the rules in the Operations section) received on respective lane. ERROR_PKT_CNT saturates at 0xFFFF and is updated on a global monitor update. In trunked mode, only lane 0 register is applicable.

Registers 0xD146, 0xD156, 0xD166, 0xD176, 0xD246, 0xD256, 0xD266, 0xD276: REFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count MSW

Bit	Type	Function	Default
15	R	TOTAL_PKT_CNT[31]	X
14	R	TOTAL_PKT_CNT[30]	X
13	R	TOTAL_PKT_CNT[29]	X
12	R	TOTAL_PKT_CNT[28]	X
11	R	TOTAL_PKT_CNT[27]	X
10	R	TOTAL_PKT_CNT[26]	X
9	R	TOTAL_PKT_CNT[25]	X
8	R	TOTAL_PKT_CNT[24]	X
7	R	TOTAL_PKT_CNT[23]	X
6	R	TOTAL_PKT_CNT[22]	X
5	R	TOTAL_PKT_CNT[21]	X
4	R	TOTAL_PKT_CNT[20]	X
3	R	TOTAL_PKT_CNT[19]	X
2	R	TOTAL_PKT_CNT[18]	X
1	R	TOTAL_PKT_CNT[17]	X
0	R	TOTAL_PKT_CNT[16]	X

TOTAL_PKT_CNT[31:16]

TOTAL_PKT_CNT[31:16] is the most significant 16 bits of the total number of complete packets received on respective lane. In trunked mode, only lane 0 register is applicable.

Registers 0xD147, 0xD157, 0xD167, 0xD177, 0xD247, 0xD257, 0xD267, 0xD277: REFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count LSW

Bit	Type	Function	Default
15	R	TOTAL_PKT_CNT[15]	X
14	R	TOTAL_PKT_CNT[14]	X
13	R	TOTAL_PKT_CNT[13]	X
12	R	TOTAL_PKT_CNT[12]	X
11	R	TOTAL_PKT_CNT[11]	X
10	R	TOTAL_PKT_CNT[10]	X
9	R	TOTAL_PKT_CNT[9]	X
8	R	TOTAL_PKT_CNT[8]	X
7	R	TOTAL_PKT_CNT[7]	X
6	R	TOTAL_PKT_CNT[6]	X
5	R	TOTAL_PKT_CNT[5]	X
4	R	TOTAL_PKT_CNT[4]	X
3	R	TOTAL_PKT_CNT[3]	X
2	R	TOTAL_PKT_CNT[2]	X
1	R	TOTAL_PKT_CNT[1]	X
0	R	TOTAL_PKT_CNT[0]	X

TOTAL_PKT_CNT[15:0]

TOTAL_PKT_CNT[15:0] is the least significant 16 bits of the total number of complete packets received on respective lane. TOTAL_PKT_CNT saturates at 0xFFFFFFFF and is updated on a global monitor update. In trunked mode, only lane 0 register is applicable. This counter should be polled every second to avoid saturation.

Registers 0xD300, 0xD400: TEFX Port A and Port B Global Control

Bit	Type	Function	Default
15	R/W	RESET	0
14	R/W	I2K_CTRL_MODE	1
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5	R	Q_DET_DIS_MON	0
4	R/W	Q_DET_DIS_SW	0
3	R	TRUNK_LANEB_MODE_MON	0
2	R/W	TRUNK_LANEB_MODE_SW	0
1	R	FC_GEB_MODE_MON	0
0	R/W	FC_GEB_MODE_SW	0

FC_GEB_MODE_SW

When FC_GEB_MODE_MON bit indicates logic 0, this function is controlled by register bit only. In this case, when this register bit is set to logic 0, 10GE mode is enabled. When this register bit is set to logic 1, 10GFC mode is enabled.

When FC_GEB_MODE_MON bit indicates logic 1. This register bit is XOR'ed FC_GEB_MODE_MON register bit to obtain the configuration. This register bit is ignored when configured for lane based operation. The value of this register bit is used in trunk mode only.

FC_GEB_MODE_MON

The FC_GEB_MODE_MON register bit reflects the polarity of the FC_GEB_MODE internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When FC_GEB_MODE internal signal is set to logic 0, the FC_GEB-_MODE_MON register bit is set to logic 0. When FC_GEB_MODE internal signal is set to logic 1, the FC_GEB_MODE_MON register bit is set to logic 1.

TRUNK_LANEB_MODE_SW

When its corresponding MON bit indicates logic 0, this function is controlled by register bit only. In this case, when this register bit is set to logic 0, each lane transmits one traffic stream. , When this register bit is set to logic 1, all four lanes are grouped together to form and transmit single traffic stream.

When its corresponding MON bit indicates logic 1. This register bit is XOR'ed with it's corresponding MON bit to obtain the configuration.

TRUNK_LANEB_MODE_MON

The TRUNK_LANEB_MODE_MON register bit reflects the polarity of the TRUNK_LANEB_MODE internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When TRUNK_LANEB_MODE internal signal is set to logic 0, the TRUNK_LANEB_MODE_MON register bit is set to logic 0. When TRUNK_LANEB_MODE internal signal is set to logic 1, the TRUNK_LANEB_MODE_MON register bit is set to logic 1.

Q_DET_DIS_SW

The Q_DET_DIS_SW bit allows the control of in-band primitive sequence detection logic. When its corresponding MON bit indicates logic 0, this function is controlled by register bit only. In this case, when this register bit is set to logic 1, in-band primitive sequence detection is disabled. Primitive sequence column will be treated as data column. When this register bit is set to logic 0, in-band primitive sequence detection is enabled. Detected in-band primitive sequence will be retained, and be transmitted at an appropriate time by Q detect state machine logic when enabled. If previous in-band primitive sequence has not yet been sent, and a new one has been detected, the previously retained value will be replaced with the new one. Because, primitive sequence has only been defined in trunk mode, this register bit has no effect in lane operation.

When its corresponding MON bit indicates logic 1. This register bit is XOR'ed with it's corresponding MON bit to obtain the configuration.

Q_DET_DIS_MON

The Q_DET_DIS_MON register bit reflects the polarity of the Q_DET_DIS internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When Q_DET_DIS internal signal is set to logic 0, the Q_DET_DIS_MON register bit is set to logic 0. When Q_DET_DIS internal signal is set to logic 1, the Q_DET_DIS_MON register bit is set to logic 1.

I2K_CTRL_MODE

When set to logic 0, all XGMII idle character (k107) will blindly be replaced with /k/ character (k1BC) when idle_replace_en[*n*] is also enabled on the corresponding lane *n* and the IPG randomizer is OFF. When the IPG randomizer is ON, only the misplaced idle character (k107) will be replaced by /k/.

When set to logic 1, all XGMII idle character (k107) will be replaced with /e/ character (k1FE) when idle_replace_en[*n*] is also enabled on the corresponding lane n and the IPG randomizer is OFF. When the IPG randomizer is ON, only the misplaced idle character (k107) will be replaced by /e/.

This register bit has effect in 10GE mode only. In 10GFC mode, all XGMII idle will blindly be replaced with /e/ character when idle_replace_en[*n*] is also enabled on the corresponding lane *n* and the IPG randomizer is OFF. When the IPG randomizer is ON, only the misplaced idle character (k107) will be replaced by /e/.

RESET

The RESET bit allows the TEFX to be reset under software control. If the RESET bit is a logic 1, the entire TEFX is held under reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the TEFX out-of -reset. Holding the TEFX in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating software reset. A hardware reset reverts all bits to their default values. A software reset reverts all but RESET bit to their default values. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Registers 0xD301, 0xD401: TEFX Port A and Port B Global Diagnostic

Bit	Type	Function	Default
15	R	Reserved	0
14	R	WR_SM[1]	0
13	R	WR_SM[0]	0
12	R	Reserved	0
11	R	RD_SM[1]	0
10	R	RD_SM[0]	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Q_DET_SM_RESET	0
6	R/W	FORCE_FIFO_RESYNC	0
5		Unused	X
4		Unused	X
3	R	Reserved	0
2	R/W	FORCE_RF_SW	0
1	R	Reserved	0
0	R/W	FORCE_LF_SW	0

FORCE_LF_SW

When this register bit is set to logic 1, Local Fault (LF) primitive sequence will be inserted into the transmit output stream according to the rules of the Random Idles State Machine, and that any in-band primitive sequences and out-of-band RF primitive sequence will be discarded. When this register bit set to logic 0, the transmit output stream is unaltered. This register bit is only applicable while configured in trunk based mode.

When its corresponding MON bit indicates logic 1. This register bit is XOR'ed with it's corresponding MON bit to obtain the configuration.

FORCE_RF_SW

When this register bit is set to logic 1, Remote Fault (RF) primitive sequence will be inserted into the transmit output stream according to the rules of the Random Idles State Machine, and that any in-band primitive sequences will be discarded. When this register bit is set to logic 0, the transmit output stream is unaltered. This register bit is only applicable while configured in trunk based mode.

When its corresponding MON bit indicates logic 1. This register bit is XOR'ed with its corresponding MON bit to obtain the configuration.

FORCE_FIFO_RESYNC

When FORCE_FIFO_RESYNC is set to logic 1, the Read State Machine for the transmit FIFO is forced into the WAIT state. TEFX remains in this state until FORCE_FIFO_RESYNC is set to logic 0.

Q_DET_SM_RESET

When Q_DET_SM_RESET is set to logic 1, the primitive sequence detect state machine is forced into the reset state. TEFX remains in this state until Q_DET_SM_RESET is set to logic 0.

Registers 0xD302, 0xD402: TEFX Port A and Port B Packet Counter Control

Bit	Type	Function	Default
15	R/W	MUST_IDLE	1
14	R/W	ALLOW_CTRL	1
13	R/W	MIN_PKT_LEN[5]	1
12	R/W	MIN_PKT_LEN[4]	1
11	R/W	MIN_PKT_LEN[3]	1
10	R/W	MIN_PKT_LEN[2]	1
9	R/W	MIN_PKT_LEN[1]	1
8	R/W	MIN_PKT_LEN[0]	1
7	R/W	CTRL_CHAR [7]	1
6	R/W	CTRL_CHAR [6]	1
5	R/W	CTRL_CHAR [5]	1
4	R/W	CTRL_CHAR [4]	1
3	R/W	CTRL_CHAR [3]	1
2	R/W	CTRL_CHAR [2]	1
1	R/W	CTRL_CHAR [1]	1
0	R/W	CTRL_CHAR [0]	0

CTRL_CHAR [7:0]

The CTRL_CHAR [7:0] register bits let user to define one control character. The CTRL_CHAR[7:0] register bits are used in conjunction with the ALLOW_CTRL register bit to allow a data packet to contain this user-defined control character and not to be accounted as an error.

MIN_PKT_LEN[5:0]

When configured in lane mode, minimum packet length (MIN_PKT_LEN[5:0]) bits are used to set the minimum packet length in number of bytes to be expected by the counter block.

When configured in trunk mode, minimum packet length (MIN_PKT_LEN[5:0]) bits are used to set the minimum packet length in number of columns to be expected by the counter block.

ALLOW_CTRL

Normally, control characters (i.e., when txdatain*[8]=1) should not be inserted inside a data packet. If that happens, it will be accounted as an error. The ALLOW_CTRL register bit allows one control character defined in CTRL_CHAR[7:0] to be inserted inside a data packet, and yet it will not be counted as an error by the performance monitor. When ALLOW_CTRL is set to logic 0, the performance monitor will account any control character inside a data packet as an error. When ALLOW_CTRL is set to logic 1, the performance monitor will account any control character except the one defined in CTRL_CHAR[7:0] inside a data packet as an error.

MUST_IDLE

In lane based mode, when set to logic 1, the minimum inter-packet gap, expected by the performance monitor is one idle character. Therefore, error packet count will be incremented if there is no inter-packet gap. When set to logic 0, any natural number inter-packet gap will not be counted as error.

In trunk mode, when set to logic 1, the minimum inter-packet gap, expected by the performance monitor is one idle column. Therefore, error packet count will be incremented if there is no inter-packet gap. When set to logic 0, any natural number inter-packet gap will not be counted as error.

Idle character can be redefined in idle control character register.

Registers 0xD303, 0xD403: TEFX Port A and Port B Interrupt Enable

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	EN	Q_DET_INT_E	0
0	EN	LOST_SYNC_E	0

LOST_SYNC_E

When LOST_SYNC_E is set to logic 1, it enables the state of the interrupt event bit LOST_SYNC_I to drive the *INTB* output pin.

When LOST_SYNC_E is set to logic 0, the state of the interrupt event bit LOST_SYNC_I has no effect on the *INTB* output pin.

Q_DET_INT_E

When Q_DET_INT_E is set to logic 1, it enables the state of the interrupt event bit Q_DET_INT_I to drive the *INTB* output pin.

When Q_DET_INT_E is set to logic 0, the state of the interrupt event bit Q_DET_INT_I has no effect on the *INTB* output pin.

Registers 0xD304, 0xD404: TEFX Port A and Port B Interrupt Status

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	IC	Q_DET_INT_I	0
0	IC	LOST_SYNC_I	0

LOST_SYNC_I

LOST_SYNC_I register bit is set to logic 1 when entering and exiting the LOST_SYNC condition. It is cleared on read when WCIMODE = 0, or cleared on write when WCIMODE = 1.

Q_DET_INT_I

Q_DET_INT_I register bit is set to logic 1 when detecting the transitions of presence to absence and absence to presence of Primitive Sequences on XGMII interface. It is cleared on read when WCIMODE = 0, or cleared on write when WCIMODE = 1.

Registers 0xD305, 0xD405: TEFX Port A and Port B Status

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	R	Q_DET_INT_V	0
0	R	LOST_SYNC_V	0

LOST_SYNC_V

Reflects the current LOST_SYNC state of the FIFO. When set to logic 1, this indicates the Read State Machine is in a re-sync condition. When set to logic 0, the Read State Machine is operating normally.

Q_DET_INT_V

When set to logic 1, this indicates that Primitive Sequences are currently detected on the incoming XGMII interface. When set to logic 0, this indicates that Primitive Sequences are not present on the incoming XGMII interface.

Registers 0xD320, 0xD328, 0xD330, 0xD338, 0xD420, 0xD428, 0xD430, 0xD438: TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Control

Bit	Type	Function	Default
15		Unused	X
14		Unused	X
13		Unused	X
12		Unused	X
11	R	T_DET_DIS_MON	0
10	R/W	T_DET_DIS_SW	0
9	R	ENCODER_EN_MON	0
8	R/W	ENCODER_EN_SW	0
7	R	RSVD_REPLACE_EN_MON	0
6	R/W	RSVD_REPLACE_EN_SW	0
5	R	INVALID_REPLACE_EN_MON	0
4	R/W	INVALID_REPLACE_EN_SW	0
3	R	IDLE_REPLACE_EN_MON	0
2	R/W	IDLE_REPLACE_EN_SW	0
1	R	RAND_IPG_EN_MON	0
0	R/W	RAND_IPG_EN_SW	0

RAND_IPG_EN_SW

When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when RAND_IPG_EN_SW[*n*] is set to logic 0, IPG randomizer is disabled for the corresponding lane *n*. When RAND_IPG_EN_SW[*n*] is set to logic 1, IPG randomizer is enabled for the corresponding lane *n*. In trunk mode, only RAND_IPG_EN_SW[0] is used.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

RAND_IPG_EN_MON

The RAND_IPG_EN_MON[n] register bit reflects the polarity of the RAND_IPG_EN[n] internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When RAND_IPG_EN[n] internal signal is set to logic 0, the RAND_IPG_EN_MON[n] register bit is set to logic 0. When RAND_IPG_EN[n] internal signal is set to logic 1, the RAND_IPG_EN_MON[n] register bit is set to logic 1.

IDLE_REPLACE_EN_SW

When IDLE_REPLACE_EN_SW[n] is set to logic 0, idle character replacement logic is enabled. When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when IDLE_REPLACE_EN_SW[*n*] is set to logic 0, idle character replacement logic is disabled for the corresponding lane *n*. When IDLE_REPLACE_EN_SW[*n*] is set to logic 1, idle character replacement logic is enabled for the corresponding lane *n*. Idle character will be replaced depending on the value of I2K_CTRL_MODE register bit (see I2K_CTRL_MODE bit description for more details). When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

IDLE_REPLACE_EN_MON

The IDLE_REPLACE_EN_MON[n] register bit reflects the polarity of the IDLE_REPLACE_EN[n] internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When IDLE_REPLACE_EN[n] internal signal is set to logic 0, the IDLE_REPLACE_EN_MON[n] register bit is set to logic 0. When IDLE_REPLACE_EN[n] internal signal is set to logic 1, the IDLE_REPLACE_EN_MON[n] register bit is set to logic 1.

INVALID_REPLACE_EN_SW

When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when INVALID_REPLACE_EN_SW[*n*] is set to logic 0, invalid character replacement logic is disabled for the corresponding lane *n*. When INVALID_REPLACE_EN_SW[*n*] is set to logic 1, invalid character replacement logic is enabled for the corresponding lane *n*. In both 10GE and 10GFC modes, invalid character is replaced with character defined in error control character register. Any 10GE and 10GFC valid or invalid characters that are defined in any of control character registers would be regarded as part of valid character set, and therefore exempted from invalid character replacement. In order to claim compliance with 10GE or 10GFC standards, the preprogrammed default values in all control character registers should not be altered.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

INVALID_REPLACE_EN_MON

The INVALID_REPLACE_EN_MON[n] register bit reflects the polarity of the INVALID_REPLACE_EN[n] internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When INVALID_REPLACE_EN[*n*] internal signal is set to logic 0, the INVALID_REPLACE_EN_MON[n] register bit is set to logic 0. When INVALID_REPLACE_EN[n] internal signal is set to logic 1, the INVALID_REPLACE_EN_MON[n] register bit is set to logic 1.

RSVD_REPLACE_EN_SW

When RSVD_REPLACE_EN_SW[*n*] is set to logic 0, reserved character replacement logic is disabled for the corresponding lane n. When RSVD_REPLACE_EN_SW[n] is set to logic 1, reserved character replacement logic is enabled. In both 10GbE and 10GFC modes, reserved character defined in reserved control character register is replaced with character defined in error control character register when enabled.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

RSVD_REPLACE_EN_MON

The RSVD_REPLACE_EN_MON[n] register bit reflects the polarity of the RSVD_REPLACE_EN[*n*] internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When RSVD_REPLACE_EN[n] internal signal is set to logic 0, the RSVD_REPLACE_EN_MON[n] register bit is set to logic 0. When RSVD_REPLACE_EN[n] internal signal is set to logic 1, the RSVD_REPLACE_EN_MON[n] register bit is set to logic 1.

ENCODER_EN_SW

When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when ENCODER_EN_SW[*n*] is set to logic 0, 8B/10B encoder is disabled for the corresponding lane *n*. When ENCODER_EN_SW[*n*] is set to logic 1, 8B/10B encoder is enabled. Feeding invalid control characters into the 8B/10B encoder may cause non-existing 10-bit code to be encoded on the output. Or it may cause alias 10-bit code to be encoded on the output.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

ENCODER_EN_MON

The ENCODER_EN_MON[n] register bit reflects the polarity of the ENCODER_EN[n] internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When ENCODER_EN[n] internal signal is set to logic 0, the ENCODER_EN_MON[n] register bit is set to logic 0. When ENCODER_EN[n] internal signal is set to logic 1, the ENCODER_EN_MON[n] register bit is set to logic 1.

T_DET_DIS_SW

When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when T_DET_DIS_SW[*n*] is set to logic 1,terminate detection logic is disabled for the corresponding lane *n*. When T_DET_DIS_SW[n] is set to logic 0, terminate detection logic is enabled for the corresponding lane *n*. Terminate character can be re-defined in terminate control character register.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

T_DET_DIS_MON

The T_DET_DIS_MON[*n*] register bit reflects the polarity of the T_DET_DIS[*n*] internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When T_DET_DIS[*n*] internal signal is set to logic 0, the T_DET_DIS_MON[*n*] register bit is set to logic 0. When T_DET_DIS[*n*] internal signal is set to logic 1, the T_DET_DIS_MON[n] register bit is set to logic 1.

Registers 0xD321, 0xD329, 0xD331, 0xD339, 0xD421, 0xD429, 0xD431, 0xD439: TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Control and Diagnostic

Bit	Type	Function	Default
15		Unused	X
14	R/W	PACKET_COUNTER_EN	0
13	R/W	IDLE_SM_RESET	0
12	R/W	FORCE_DP_ERR	0
11		Unused	X
10		Unused	X
9		Unused	X
8		Unused	X
7		Unused	X
6		Unused	X
5	R	DATA_BIT_SWIZZLE_MON	0
4	R/W	DATA_BIT_SWIZZLE_SW	0
3	R	DATA_BIT_INV_MON	0
2	R/W	DATA_BIT_INV_SW	0
1	R	SERDES_8BIT_EN_MON	0
0	R/W	SERDES_8BIT_EN_SW	0

SERDES_8BIT_EN_SW

When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when SERDES_8BIT_EN_SW[*n*] is set to logic 0, swizzle will be performed on the 10-bit output bus for the corresponding lane *n*. When SERDES_8NBIT_EN_SW[*n*] is set to logic 1, swizzle will be performed on the lower 8-bit output bus for the corresponding lane *n*. The bit swizzling is not performed until DATA_BIT_SWIZZLE[*n*] register bit is enabled for the corresponding lane *n*.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

SERDES_8BIT_EN_MON

The SERDES_8BIT_EN_MON[*n*] register bit reflects the polarity of the SERDES_8BIT_EN[n] internal signal as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When SERDES_8BIT_EN[*n*] internal signal is set to logic 0, the SERDES_8BIT_EN_MON[*n*] register bit is set to logic 0. When SERDES_8BIT_EN[n] internal signal is set to logic 1, the SERDES_8BIT_EN_MON[*n*] register bit is set to logic 1.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

DATA BIT_INV_SW

When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when DATA_BIT_INV_SW[*n*] is set to logic 0,all bits are transmitted unmodified onto the TEFX output data bus *n*. When DATA_BIT_INV_SW[*n*] is set to logic 1, all bits are transmitted negated before transmitting onto the TEFX output data bus *n*.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

DATA_BIT_INV _MON

The DATA_BIT_ INV _MON[*n*] register bit reflects the polarity of the DATA_BIT_ INV[*n*] input pin as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When DATA_BIT_ INV[*n*] input pin is set to logic 0, the DATA_BIT_ INV _MON[*n*] register bit is set to logic 0. When DATA_BIT_ INV[*n*] input pin is set to logic 1, the DATA_BIT_ INV _MON[*n*] register bit is set to logic 1.

DATA_BIT_SWIZZLE_SW

When its corresponding MON[*n*] bit indicates logic 0, this function is controlled by register bit only. In this case, when DATA_BIT_SWIZZLE_SW[*n*] is set to logic 0, output bus *n* is transmitted normally. When DATA_BIT_SWIZZLE_SW[*n*] is set to logic 1, output bus *n* is swizzled. If the expected output bus is 8 bit wide as controlled by SERDES_8BIT_EN[*n*] register bit , 8 bits are swizzled for lane *n*. If the expected output bus is 10-bit wide as controlled by SERDES_8BIT_EN[*n*] register bit, 10 bits are swizzled for lane *n*.

When its corresponding MON[*n*] bit indicates logic 1. This register bit is XOR'ed with its corresponding MON[*n*] bit to obtain the configuration.

Function of this register bit is also summarized in the following table.

Table 16 Data Swizzle Functionality

Original DATA bit position		DATA bit position when DATA_ BIT_SWIZZLE=0		DATA bit position when DATA_ BIT_SWIZZLE=1	
10 bits	8 bits	10 bits	8 bits	10 bits	8 bits
9	x	9	x	0	x
8	x	8	x	1	x
7	7	7	7	2	0
6	6	6	6	3	1
5	5	5	5	4	2
4	4	4	4	5	3
3	3	3	3	6	4

2	2	2	2	7	5
1	1	1	1	8	6
0	0	0	0	9	7

DATA_BIT_SWIZZLE _MON

The DATA_BIT_SWIZZLE _MON[*n*] register bit reflects the polarity of the DATA_BIT_SWIZZLE[*n*] input pin as dictated by the *MODE_SEL[1:0]* device inputs and/or relevant Master Register bits. When DATA_BIT_SWIZZLE[*n*] input pin is set to logic 0, the DATA_BIT_SWIZZLE _MON[*n*] register bit is set to logic 0. When DATA_BIT_SWIZZLE[*n*] input pin is set to logic 1, the DATA_BIT_SWIZZLE _MON[*n*] register bit is set to logic 1.

FORCE_DP_ERR

When FORCE_DP_ERR [*n*] is set to logic 1, the current running disparity will be inverted for the corresponding lane *n*. The current disparity will be inverted once for each FORCE_DP_ERR[*n*] assertion because this register bit is self-clearing. When FORCE_DP_ERR [*n*] is set to logic 0, the current running disparity is not modified for the corresponding lane *n*.

IDLE_SM_RESET

During lane based operation, when IDLE_SM_RESET[*n*] is set to logic 1, the lane based random idle state machine is forced into the reset state on lane *n*. TEFX lane *n* remains in reset until IDLE_SM_RESET[*n*] returns to logic 0.

During trunk based operation, when IDLE_SM_RESET[0] is set to logic 1, the trunk based idle state machine is forced into the reset state. TEFX remains in reset until IDLE_SM_RESET[0] returns to logic 0. In trunk mode, only the IDLE_SM_RESET[0] register bit is used.

PACKET_COUNTER_EN

The PACKET_COUNTER_EN[*n*] is set to logic 0, the number of good and errored packets going through the TEFX will not be counted on lane *n*. When set to logic 1, the number of good and errored packets going through the TEFX will be counted on lane *n*. In trunk mode, only PACKET_COUNTER_EN[0] is used.

Registers 0xD322, 0xD32A, 0xD332, 0xD33A, 0xD422, 0xD42A, 0xD432, 0xD43A: TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count LSW

Bit	Type	Function	Default
15	R	TOTAL_PKT_CNT[15]	0
14	R	TOTAL_PKT_CNT[14]	0
13	R	TOTAL_PKT_CNT[13]	0
12	R	TOTAL_PKT_CNT[12]	0
11	R	TOTAL_PKT_CNT[11]	0
10	R	TOTAL_PKT_CNT[10]	0
9	R	TOTAL_PKT_CNT[9]	0
8	R	TOTAL_PKT_CNT[8]	0
7	R	TOTAL_PKT_CNT[7]	0
6	R	TOTAL_PKT_CNT[6]	0
5	R	TOTAL_PKT_CNT[5]	0
4	R	TOTAL_PKT_CNT[4]	0
3	R	TOTAL_PKT_CNT[3]	0
2	R	TOTAL_PKT_CNT[2]	0
1	R	TOTAL_PKT_CNT[1]	0
0	R	TOTAL_PKT_CNT[0]	0

TOTAL_PKT_CNT[15:0]

The TOTAL_PKT_CNT[15:0] bits indicate Least Significant Word (LSW) of the 32 bit counter. This counter tracks the total number of frames (not including errored frames) transmitted to the TEFX FIFO during the last accumulation interval for the corresponding lane. In trunk mode, only lane 0 counter is valid.

The 32-bit counter saturates at its maximum count value of 0xFFFFFFFF.

A performance update request loads the register with the current counter value and resets the internal counter to zero.

Registers 0xD323, 0xD32B, 0xD333, 0xD33B, 0xD423, 0xD42B, 0xD433, 0xD43B: TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Total Packet Count MSW

Bit	Type	Function	Default
15	R	TOTAL_PKT_CNT[31]	0
14	R	TOTAL_PKT_CNT[30]	0
13	R	TOTAL_PKT_CNT[29]	0
12	R	TOTAL_PKT_CNT[28]	0
11	R	TOTAL_PKT_CNT[27]	0
10	R	TOTAL_PKT_CNT[26]	0
9	R	TOTAL_PKT_CNT[25]	0
8	R	TOTAL_PKT_CNT[24]	0
7	R	TOTAL_PKT_CNT[23]	0
6	R	TOTAL_PKT_CNT[22]	0
5	R	TOTAL_PKT_CNT[21]	0
4	R	TOTAL_PKT_CNT[20]	0
3	R	TOTAL_PKT_CNT[19]	0
2	R	TOTAL_PKT_CNT[18]	0
1	R	TOTAL_PKT_CNT[17]	0
0	R	TOTAL_PKT_CNT[16]	0

TOTAL_PKT_CNT[31:16]

The TOTAL_PKT_CNT[31:16] bits indicate Most Significant Word (MSW) of the 32 bit counter. This counter tracks the total number of complete frames being transmitted to the TEFX FIFO during the last accumulation interval for the corresponding lane. In trunk mode, only lane 0 counter is valid.

The 32-bit counter saturates at its maximum count value of 0xFFFFFFFF.

A performance update request loads the register with the current counter value and resets the internal counter to zero.

Registers 0xD324, 0xD32C, 0xD334, 0xD33C, 0xD424, 0xD42C, 0xD434, 0xD43C: TEFX Port A Lanes 0-3 and Port B Lanes 0-3 Error Packet Count

Bit	Type	Function	Default
15	R	ERROR_PKT_CNT[15]	0
14	R	ERROR_PKT_CNT[14]	0
13	R	ERROR_PKT_CNT[13]	0
12	R	ERROR_PKT_CNT[12]	0
11	R	ERROR_PKT_CNT[11]	0
10	R	ERROR_PKT_CNT[10]	0
9	R	ERROR_PKT_CNT[9]	0
8	R	ERROR_PKT_CNT[8]	0
7	R	ERROR_PKT_CNT[7]	0
6	R	ERROR_PKT_CNT[6]	0
5	R	ERROR_PKT_CNT[5]	0
4	R	ERROR_PKT_CNT[4]	0
3	R	ERROR_PKT_CNT[3]	0
2	R	ERROR_PKT_CNT[2]	0
1	R	ERROR_PKT_CNT[1]	0
0	R	ERROR_PKT_CNT[0]	0

ERROR_PKT_CNT[15:0]

The ERROR_PKT_CNT[15:0] bits indicate a 16 bit counter. This counter tracks the total number of errored frames being transmitted to the TEFX FIFO during the last accumulation interval for the corresponding lane. In trunk mode, only lane 0 counter is valid.

The 16-bit counter saturates at its maximum count value of 0xFFFF.

A performance update request loads the register with the current counter value and resets the internal counter to zero.

13 Test Features Description

13.1 JTAG Test Port

The QuadPHY XR TAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 17 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 18 Identification Register

Length	32 bits
Version Number	01H
Part Number	8357H
Manufacturer's Identification Code	0x083570CD H
Device Identification	0x083570CD H

Table 19 Boundary Scan Register

Name	Register Bit	Cell Type	Device ID
PM8357	15 - 0	IN_CELL	0x083570CD

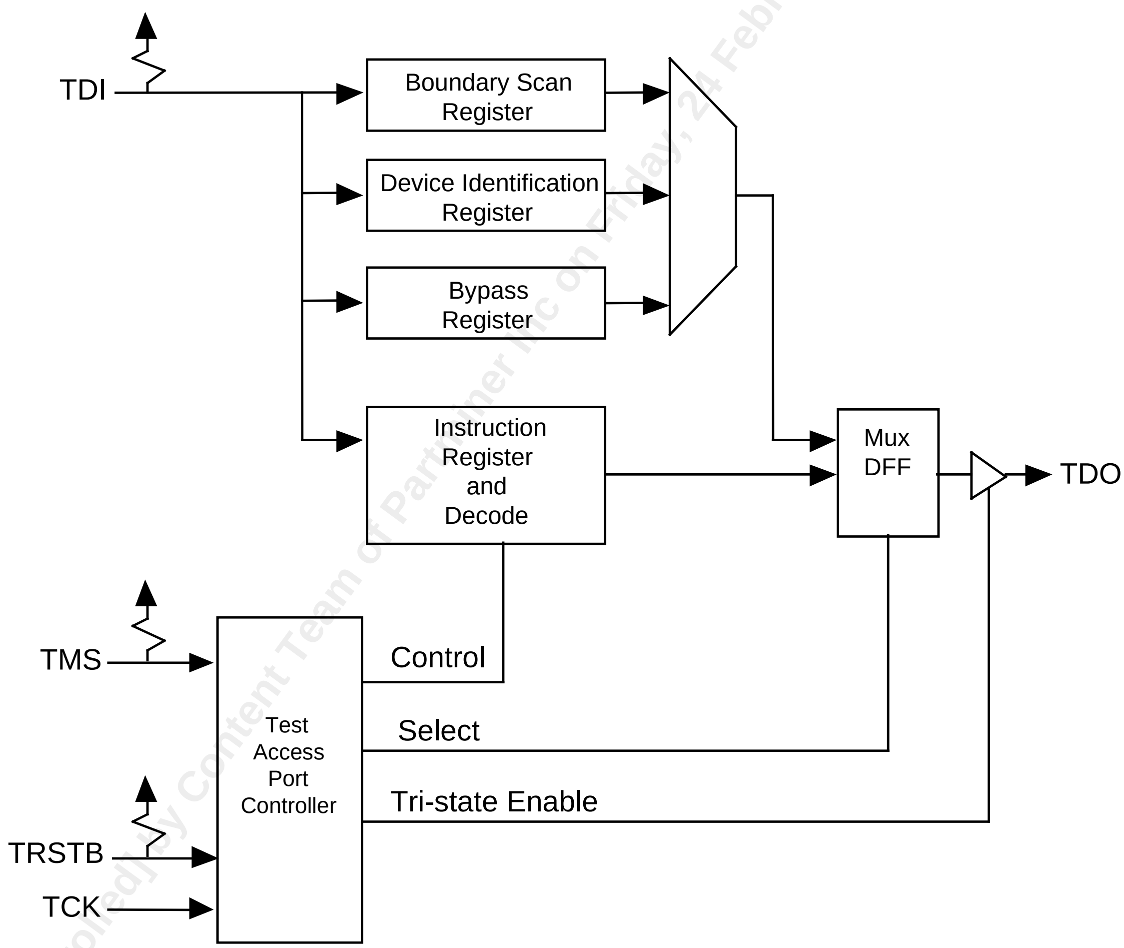
Note:

1. When set high, INTB will be set to high impedance.
2. Each output cell has its own output enable (OEB_*)

13.2 JTAG Control

The QuadPHY XR supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TRSTB should be tied to RSTB if the JTAG interface is not used. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 9 Boundary Scan Architecture



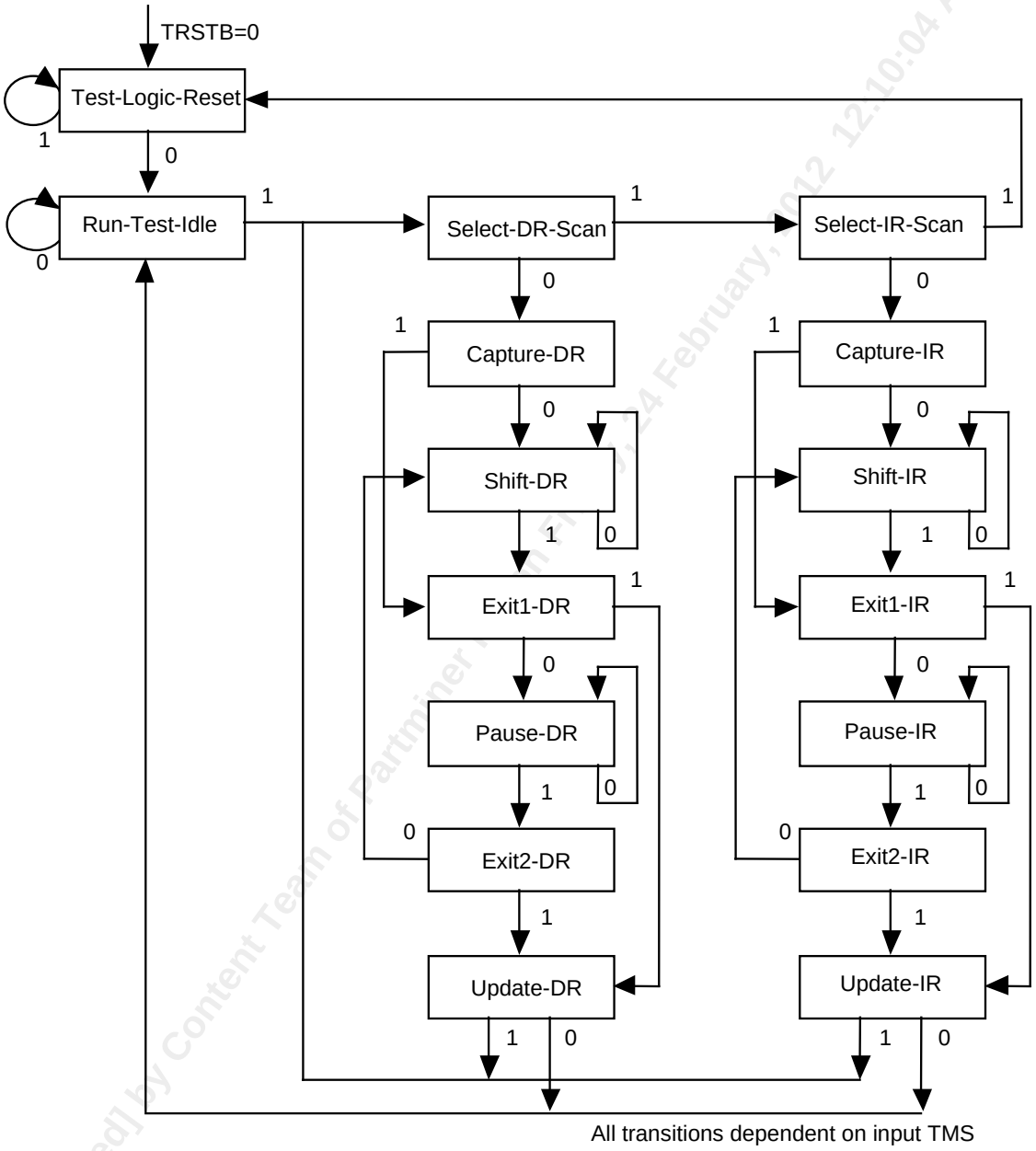
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.2.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 10 TAP Controller Finite State Machine



13.2.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

13.2.3 Instructions

Bypass

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

Extest

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

Sample

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCode

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTest

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

14 Operation

14.1 Modes of Operation

14.1.1 10 Gigabit Ethernet (10GE) Mode

When configured for 10 Gigabit Ethernet Mode operation, the QuadPHY XR operates as a XAUI to XAUI retimer.

The four lanes of traffic on each port will be 8B/10B decoded, aligned, and converted to the local clock domain. After the signals pass through the internal crosspoint switch, they will be 8B/10B encoded prior to re-transmission.

For 10GBase-X optical module applications, Port A is connected to the XGXS interface and Port B of the QuadPHY XR is connected to the optical module PMA/PMD electrical interface. This port assignment is required so that the register definitions for MMD1 and MMD4 will reflect the correct interface. For backplane retiming applications, a specific port assignment is not required, as both ports provide identical functionality.

In order for the XAUI alignment logic to function properly, all incoming high-speed signal applied to a particular port (A or B) must operate at exactly the same bit rate. Signals applied to either port may be asynchronous to each other, and with respect to the local Reference Clock. Although this mode is intended for 10GE applications operating at 3.125 Gbit/s, this mode supports operation from 1.2 Gbit/s to 3.2 Gbit/s.

This mode is selected by setting the MODE_SEL[1:0] pins to "00".

14.1.2 10 Gigabit Fibre Channel (10GFC) Mode

When configured for 10 Gigabit Ethernet Mode operation, the QuadPHY XR operates as a XAUI to XAUI retimer. The four lanes of traffic on each port will be 8B/10B decoded, aligned, and converted to the local clock domain. After the signals pass through the internal crosspoint switch, they will be 8B/10B encoded prior to re-transmission.

While very similar to 10GE mode, the 10GFC mode provides additional processing of primitive sequences specific to Fibre Channel applications.

All incoming high-speed signal applied to a particular port (A or B) must operate at exactly the same bit rate. Signals applied to either port may be asynchronous to each other, and with respect to the local Reference Clock. This mode is intended for 10GFC applications operating at 3.1875 Gbit/s, this mode supports operation from 1.2 Gbit/s to 3.2 Gbit/s.

This mode is selected by setting the MODE_SEL[1:0] pins to "01".

14.1.3 Lane-Based Mode

When configured for Lane-Based Mode operation, the QuadPHY XR operates as a retimer for each individual high-speed input. Traffic on each of the eight high-speed inputs will be 8B/10B decoded, and converted to the local clock domain. After the signals pass through the internal crosspoint switch, they will be 8B/10B encoded prior to re-transmission.

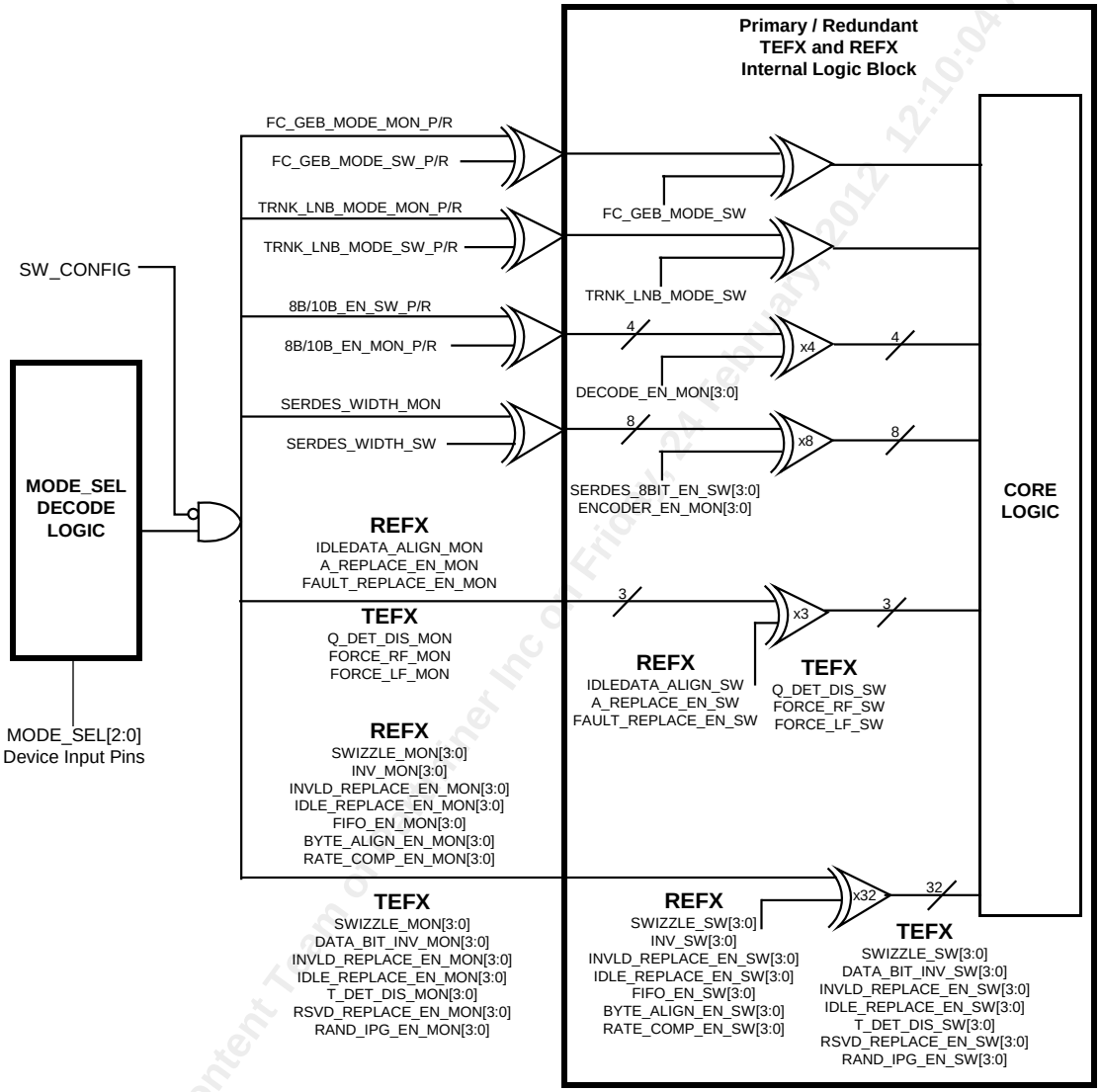
All incoming bit streams applied to a particular port (A or B) may operater from independent clocks source, provided that the data rate is +/-100 ppm from the nominal rate. Signals applied to either port may be asynchronous to each other, and with respect to the local Reference Clock. This mode supports operation from 1.2 Gbit/s to 3.2 Gbit/s.

This mode is selected by setting the MODE_SEL[1:0] pins to "10".

14.2 Logical XOR Programmability

The QuadPHY XR was designed to operate on pin-driven configuration. At the same time, it offers an extensive software override capability via stages of XOR'ing at the device level and at the block level. Figure 11 below summarizes how this is implemented in the QuadPHY XR.

Figure 11 QuadPHY XR Logical XOR Tree



Note that this configuration scheme is intended to be used out of device reset. Once software override has been invoked via master register bit, or block level register bit, write access, a post-reset change in the *MODE_SEL[1:0]* primary inputs will not yield the configurations outlined in the Pin Description of the *MODE_SEL[1:0]* bits. With such activity, the core logic configuration would be realized by the XOR tree in Figure 11.

14.3 XC16 Cross Bar Operation

14.3.1 Initialization

Out of reset, if the *MODE_SEL[1:0]* pins have been tied appropriately, each output lane is automatically defaulted to source traffic from its own input lane. For example, output lane 0 sources traffic from its input lane 0; output lane n sources traffic from its input lane n. At the same time, each output lane's active lane register reflects the current input lane selection accordingly. If the aforementioned setup is the desired operation, no additional configuration is required. Otherwise, additional configuration steps are required. These steps may include input lane selection, idle and terminate characters redefinition and immediate or IPG switching mode selection.

14.3.2 Input Lane Selection

Pin Configuration

The input lane for each output lane can be selected via *MODE_SEL[1:0]* pins and / or XC16 Standby registers.; In order to obtain the resultant input lane selection for a particular output lane, its corresponding MUX_PRESET register value is XOR'ed with the two most significant bits of its corresponding ACTIVELN register value as shown in the following figure . This will allow a group of four logically adjacent output lanes to select any other group of four logically adjacent input lanes as their inputs via MUX_PRESET register value as dictated by the *MODE_SEL[1:0]* pins only. Because XC16 has 8 input and 8 output lanes, there are 2 input and output groups respectively. Each input or output group consists of four logically adjacent input or output lanes respectively.

Figure 12 gives an example of this setup as it applies to a single lane of the Transmit XAUI Port A Output of the Cross Connect.

Figure 12 MUX_PRESET XOR Diagram

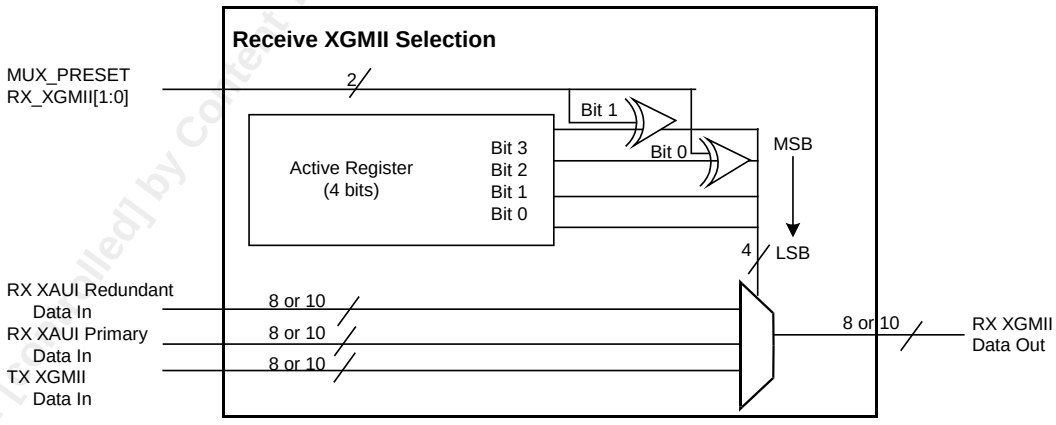


Figure 12 shows the implementation for one lane of the TX XAUI Port A data output, which appears on the QuadPHY XR as one of the *SLnA_P/N* differential sets of device outputs.

It should be noted that the toggling of *MODE_SEL[1:0]* pins intentional or not will cause an abrupt and immediate update to crossbar's cross-connect configuration. Transiting traffic may be corrupted. If graceful switching is desired, XC16 IPG switch feature may be used. More information on IPG switch will be detailed later.

ECBI Configuration

Via the MDIO interface, each output lane can be configured to source traffic from any one of 8 input lanes. Therefore, cross-connect granularity is increased. In addition, the host control software can utilize the XOR function of *MODE_SEL[1:0]* pins and ACTIVELN registers to achieve more complex functions such as redundant switching, IPG switching, multicasting and loopback.

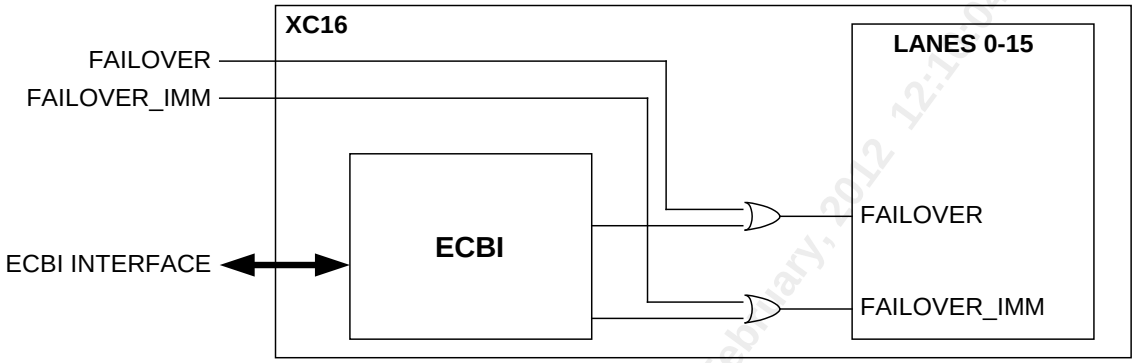
The host control software can access XC16 output lane's active input lane selection configuration via its MUX_PRESET register and its corresponding ACTIVELN register. The read only MUX_PRESET register reflects *MODE_SEL[1:0]* pins' current value while the read only ACTIVELN register reflects the actively programmed input lane for the corresponding output lane. The XOR'ing of these 2 pieces of information will provide the final active input lane selection for the corresponding output lane. To select a different input lane for a particular output lane, the corresponding XC16 Standby register must be appropriately programmed. The XOR'ing of the current padded MUX_PRESET value and the desired standby input lane value gives the appropriate programmed value for those XC16 Standby register. The padded MUX_PRESET value is actually the 2-bit MUX_PRESET value for the corresponding output lane padded with 2 0's to the right. For example, if you desire to source traffic from input lane 5 on output lane 0, and let us assume the MUX_PRESET[1:0] value is 3, the padded MUX_PRESET value in binary format will be 1100. The desired input lane in binary format will be 0101. Then the programmed value in output lane 0's XC16 Standby register shall be given by 1100 XOR 0101 (i.e. 1001). It should be noted that XC16 Standby register value would not be updated into XC16 Active register until pending switch request is successful completed. More details will be given later.

14.3.3 Switch Mode

XC16 supports 2 switching modes. They are immediate switching and IPG switching. Immediate switching can be activated via XC16 FAILOVER_IMM pin or register while IPG switching can be activated via FAILOVER pin or register if IPG_SWITCHEN also set to logic 1.

It should be noted that the FAILOVER_IMM and FAILOVER have both pin and register bit controls that are ORed together to create a rising edge signal to activate the switch. Figure 13 shows the wiring for FAILOVER pin and its register bit as well as FAILOVER_IMM pin and its register bit.

Figure 13 FAILOVER and FAILOVER_IMM's pin and register OR function



14.3.4 Switch Configurations Concept

The basic steps in performing either switch operation require accesses to STDBYLN, SWITCHEN and CONTROL registers.

STDBYLN register contains the standby input lane to be switched to on a FAILOVER_IMM or FAILOVER trigger event. The value written into this register has no immediate effect on the output lane. It can be written and rewritten as many times as required, but will only be sampled on a FAILOVER_IMM or FAILOVER trigger event. The value programmed in STDBYLN register does not change unless user overwrites it.

The FAILOVER_IMM and FAILOVER control signals affect all lanes at the same time. To enable either switching on output lane n, SWITCHEN[n] must be set to logic 1. To disable either switching on output lane n, SWITCHEN[n] must be set to logic 0. Failing to disable SWITCHEN on lanes, that do not wish switch operation, may result in unnecessary traffic disruption for those lanes. SWITCHEN is not self-clearing after a switch is completed. It therefore must be explicitly cleared by writing a logic 0 to it if no future switch action is required.

Finally, toggling FAILOVER_IMM or FAILOVER control signals from logic 0 to logic 1 to activate immediate switching or IPG switching respectively.

Immediate Switching Setup

The toggling of FAILOVER_IMM from logic 0 to logic 1 will cause output lane n whose SWITCHEN[n] set to logic 1 to immediately be switched to the standby lane defined in its own STDBYLN register n. The switch operation is abrupt. No attempt is made to cleanly break the active data stream or cleanly reconnect the standby data stream using this switch mechanism.

IPG Switching Setup for Lane-based Traffic

The entire IPG switching operation is slightly more complex Before such switch operation can take place, these additional registers other than the ones mentioned previously have to be setup as well: IDLE0-3, IDLETX, and CONTROL.

IDLE0-3 contain the definitions of IPG pattern. Each IDLE[n] has its own enable and mask bits to define how its own IPG pattern matching logic should operate. If no IDLE[n] matching logic is enabled, or if the IPG pattern used never occurs in the data stream, the IPG switch will appear to hang while waiting for the occurrence of these IPG patterns. When waiting for these IPG patterns to occur, the output lane's BUSY bit will be set to logic 1. Polling this register will give the output lane's IPG switch status.

Toggling FAILOVER_IMM from logic 0 to logic 1 will force an immediate switch of a hung output lane to the standby input lane. Deasserting IPG_SWITCHEN during IPG switch operation will cause output lane to switch to the standby input lane through a rapid transversal of its MUX control state machine logic. In a sense, a submitted IPG switch request can never be aborted. Output lane will always end up in switching to the standby input lane gracefully or not.

IDLETX must be set with a valid idle character IDLETX value is transmitted by the XC16 after the active connection is broken . IDLETX continues to be transmitted until an IPG is detected on the standby input data stream, at which point new connection is established.

The CONTROL register contains the IPG_SWITCHEN bit, which must be set to logic 1 to enable IPG switching. When IPG_SWITCHEN is set to logic 0, toggling FAILOVER will have no effect. The CONTROL register also has the register versions of FAILOVER_IMM and FAILOVER. These bits are ORed with their corresponding input pins to allow configuration flexibility. These bits are not self-clearing.

IPG Switch Setup for Decoded Trunk Traffic

Four lanes can be used together to for trunk data stream. The XC16 supports switching on decoded trunk data. In XC16, these input lanes 0-3, 4-7, 8-11, and 12-15 are grouped into input trunk groups 0, 1, 2 and 3 respectively. These output lanes 0-3, 4-7, 8-11, and 12-15 are grouped into output trunk groups 0, 1, 2 and 3 respectively. Each output trunk group can source traffic from any input lane.

IPG switching of trunk data stream requires extra setup steps in addition to the ones mentioned in the previous sections. Because a trunk data packet (such as 10GE packet) can terminate on any lane within the output trunk group, the TERMINATE character must be defined to identify the trunk data packet's terminate column. In the case of 10GE decoded character set, this TERMINATE character is 0x1FD. If set incorrectly, the XC16 may start IPG switching on the terminate column prematurely on certain output lanes corrupting trunk data packets even when IPG switching feature is used.

Registers T_CHAR0 and T_CHAR1 are the programmable terminate pattern registers. By default, T_CHAR0 is programmed with 0x1FD. If IPG switching of encoded trunk data character set is desired, these registers can be programmed with both disparity versions of encoded terminate character . See the register description for exact details.

Each output trunk group n has a corresponding TRUNKEN[n] bit in the CONTROL register. This bit enables the Terminate column detection for the output trunk group n. This allows certain output trunk groups to switch on trunk data stream while others output trunk groups to switch on lane based data stream at the same time. If the crossbar switches trunk data stream exclusively, all TRUNKEN bits should be set to logic 1.

In summary, switching of trunk data stream requires the terminate column of a packet to be identified to allow the crossbar to properly switch the trunk data packet. This is accomplished by programming T_CHAR0 or TRUNK1 or both with valid terminate characters that mark the terminate column of the trunk data packet. The TRUNKEN[n] bits of the output trunk group n trunk must be set to enable Terminate column detection circuitry.

Once all the required registers are setup, toggling FAILOVER from logic 0 to logic 1 will activate a trunk IPG switch operation. The BUSY bit for the output lane under switch request is set at the 1^{st} wait state and remains set until the switch operation is completed. If the switch stalls at any point, FAILOVER_IMM can be toggled from logic 0 to logic 1 to force an immediate switch operation. Deasserting IPG_SWITCHEN during IPG switch operation will cause output lane to switch to the standby input lane through a rapid transversal of its MUX control state machine logic.

IPG Switch Setup for Encoded Trunk Traffic

The XC16 supports switching on encoded trunk data to certain extent. Instead of programming the decoded version of IPG character and Terminate character into IDLE, IDLETX and T_CHAR register, the encoded version of IPG character and Terminate character must be programmed. The extra IDLE and T_CHAR registers that have not been used in IPG switching of decoded trunk traffic must be enabled to accommodate both the positive and the negative disparity copy of encoded IPG character and encoded Terminate character. For IDLETX register, only one disparity copy of encoded IPG character can be programmed. Other than that, the IPG switching setup of encoded trunk traffic is identical to the IPG setup of decoded trunk traffic.

It should be noted that in 10GE and 10GFC traffic system, IPG column is supposed to randomize, and the disparity of the transmitting traffic is supposed to alternate from word to word. By transmitting constant disparity, constant valued 10-bit word in 10GE and 10GFC traffic system, this standard practice would have been violated causing a system wide failure. At one stage of IPG switching, XC16 will transmit IDLETX word constantly thereby violating the standard practiced in 10GE and 10GFC. In summary, XC16 is not well designed for IPG switching of encoded trunk traffic especially in 10GE and 10GFC modes.

Special Notes for IPG Switch Setup

XC16 has the ability to program the IPG Idle detection and the IDLETX generation for IPG switching. For seamless IPG switching in a real working and protect application environment, IDLETX must be programmed to the same value as the IPG Idle. This will allow the QuadPHY XR to generate the same IPG Idle as the receive traffic for the downstream device until the switchover occurs.

14.4 REFX Operation

14.4.1 10GE Mode Configuration

In this mode all the lanes operate together as a single link. REFX will initially declare alignment (deskew) loss and synchronization (byte alignment) loss. REFX will indicate synchronization loss by asserting the SYNC_ERRV status register bits for all lanes. REFX will indicate alignment loss by asserting the ALIGN_ERRV status register bit. Synchronization is declared after 4 /K/ characters are received by de-asserting the SYNC_ERRV status register bits for all lanes. Alignment is declared when 4 ||A|| columns are received after synchronization is gained by de-asserting the ALIGN_ERRV status register bit.

After synchronization is gained and one ||A|| is received to set the initial alignment, rate compensation (idle column insertion and deletion) is allowed to keep the FIFO centered during the presence of ± 200 ppm frequency difference between the write and read clock domains. An ||R|| column is inserted in all lanes during an IPG if the FIFO depth in any of the lanes is less than FIFO_DEPTH -2. An Idle column (||A||, ||K|| and ||R||) or ||Q|| column is deleted when the FIFO depth is more than FIFO_DEPTH + 2. An idle column is allowed to be deleted provided it is preceded by an idle or ||Q|| column to guarantee that at the IPG is at least 1 column in size. A ||Q|| column is allowed to be deleted provided it is preceded by an identical ||Q|| column to guarantee that only duplicated ||Q|| columns are deleted. An ||R|| column can be inserted anywhere in an IPG. Once an insertion or deletion is performed, further deletions or insertions are prevented for 7 cycles to allow the FIFO to stabilize. ||Q|| column deletion can be disabled by asserting the DIAG_DISABLE_QDEL register bit since it is not explicitly indicated in draft 5 of IEEE 802.3ae standard; however allowing duplicate ||Q|| deletion allows backward compatibility with previous drafts of the same standard.

While alignment is lost, ||LF|| (local fault) columns are continuously driven on the output data path. When alignment is gained, ||A||, ||K|| and ||R|| columns are replaced by ||I|| columns. Also, /K/ characters in ||T|| columns are replaced by /I/ characters. The output stream will be 8B10B decoded and /E/ characters will replace any byte that contained a code violation or disparity error. /E/ characters will also be propagated into any byte of the packet adjacent to an IPG byte that is not an / A/ or /K/ - this is the check end functionality.

14.4.2 10GFC Configuration

The 10GFC configuration is identical to the 10GE configuration above except that the device is boot straped for 10GFC operation or FC_GEB_MODE_SW software register bit is asserted.

The 10GFC behavior is identical to the 10GE configuration above except that there are a 2 more rules for rate compensation. The two idles preceding and following a ||Ps|| (clock synchronization primitive) column cannot be deleted; this is to prevent the idles in the IIPsPsPsII sequence from being deleted. Also an ||R|| cannot be inserted after a ||Ps|| columns; this is to prevent the PsPsPs sequence from being broken by an inserted idle column.

14.4.3 Lane Mode Configuration

In this mode all lanes operate independently. This mode can be configured via pins or software registers. REFX will initially declare synchronization loss by asserting the SYNC_ERRV status register bits for all lanes. Alignment loss is not declared since it is not applicable in this mode. Synchronization is declared on a given lane after 4 /K/ characters are received by de-asserting the SYNC_ERRV status register bit for that lane.

When 1 /K/ character is received to set the initial synchronization rate compensation (idle character insertion and deletion) is allowed to keep the FIFO centered during the presence of ± 200 ppm frequency difference between the write and read clock domains. An /R/ character is inserted in a given lane during an IPG if that lane's FIFO depth is less than FIFO_DEPTH -2. An Idle character (/K/ and /R/) is deleted from a lane's IPG when that lane's FIFO depth is more than FIFO_DEPTH + 2. An idle character is allowed to be deleted provided it is preceded by an idle character to guarantee that at the IPG is at least 1 character in size. An /R/ character can be inserted anywhere in an IPG. Once an insertion or deletion is performed in a lane, further deletions or insertions in that lane are prevented for 3 cycles to allow that lane's FIFO to stabilize. If desired, rate compensation for a given lane can be disabled by de-asserting the RATE_COMP_EN_SW software register bit for that given lane.

The output stream will be 8B10B decoded and /E/ characters will replace any byte that contained a code violation or disparity error. /K/ and /R/ idle characters will also be replaced by /I/ characters. If desired, 8B10B error replacement with /E/ for a given lane can be disabled by de-asserting the INVLD_REPLACE_EN_SW register bit for that lane. If desired, /K/ and /R/ character replacement by /I/ for a given lane can be disabled by de-asserting the IDLE_REPLACE_EN_SW register bit for that lane.

14.4.4 Serdes Mode Configuration

8B10B Mode

In this mode the data stream is 8B10B encoded not scrambled. Also, all lanes are independent and rate compensation is not allowed. Byte alignment, 8B10B decoding, phase compensation and idle replacement are optionally allowed. This mode can be configured via pins or software registers. REFX has all functions disabled and the input data is passed through transparently. Alignment loss is not declared by REFX in this mode since they are not applicable.

If desired, byte alignment for a given lane can be enabled by BYTE_ALIGN_EN_SW register bit for that lane. If byte alignment is enabled, synchronization loss will be initially declared by asserting the SYNC_ERRV status register bits for all lanes. Synchronization is declared on a given lane after 4 /K/ characters are received by de-asserting the SYNC_ERRV status register bit for that lane. If byte alignment is not enabled, synchronization loss will not be declared since it is not applicable.

If desired, the 8B10B decoder can be enabled for a given lane by asserting the DECODE_EN_SW register bit for that lane. If desired, 8B10B errors can be replaced by /E/ character for a given lane by asserting the INVLD_REPLACE_EN_SW register bit for that lane. If desired, /K/ and /R/ idle characters can be replaced by /I/ characters for a given lane by asserting the REPLACE_EN_SW register bit for that lane.

The output stream on RXOUT will be on the write clock domain. If the write and read clock domain for a given lane are locked, the data stream can be passed through that lane's FIFO so the data stream on RXOUT is on the read clock domain. This is achieved by asserting the FIFO_EN_SW register bit for that lane. The FIFO will perform only phase compensation not rate compensation (i.e. no ppm difference between the write and read clock domains).

14.4.5 Packet Counter Configuration

Trunk Mode

Configure REFX in trunk mode. In trunk mode, the packet counter is additionally in 10GFC mode when the FC_GEB_MODE_SW register bit is asserted; otherwise it is in 10GE mode. In this mode the packet counter is enabled by asserting the PC_EN register bit for lane 0. When enabled, the packet counter will count the number of good trunked packets and the number of errors. After a performance counter update the count values will be stored in the REFX Primary Lane 0-3 and Redundant Lanes 0-3 Total Packet Count MSW/LSW and Packet Error Count software register for lane 0.

The TEFX packet counter can be configured the same way as the REFX packet counter.

Trunked packets are considered good if they confirm to the rules below. A trunked packet starts with an /S/ character on lane 0 and end with a ||T|| column. In 10GE mode, the /T/ character can be on any column and must be followed by Idle characters (/A/, /K/, /R/ or /I/). In 10GFC mode, the /T/ must be on lane 3. When the ALLOW_CNTRL register bit is de-asserted no control characters are allowed in side the packet with the exception of the /S/ and /T/ characters. When the ALLOW_CNTRL register bit is asserted the control character defined in the CNTRL software register is also allowed inside the packet. When the MUST_I register bit is asserted, the packet must be preceded by an IPG (||A||, ||K||, ||R|| or ||I|| columns) with a minimum size of 1 column. When the MUST_I register bit is de-asserted, there are no restrictions on the IPG preceding the packet (i.e. there can be no IPG and the packets could be back to back). The packet size (excluding the ||S|| and ||T|| columns) must be greater than the number of columns in the PKT_MIN_LEN software register.

Lane Mode

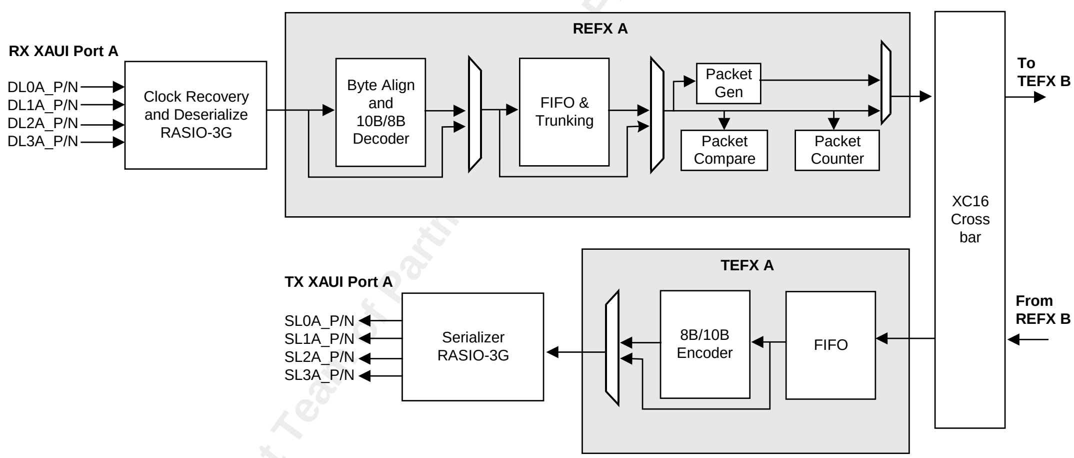
Configure REFX in lane mode In this mode the packet counter for each lane is independent and is enabled by asserting the PC_EN register bit for that lane. When enabled, the packet counter for a given lane will count the number of good packets and the number of errors on that lane. After a performance counter update the count values will be stored in the REFX Primary Lane 0-3 and Redundant Lanes 0-3 Total Packet Count MSW/LSW and Packet Error Count software register for that lane.

Packets are considered good if they confirm to the rules below. A packet starts with an /S/ character and ends with a /T/ character. When the ALLOW_CNTRL register bit is de-asserted no control characters are allowed in side the packet with the exception of the /S/ and /T/ characters. When the ALLOW_CNTRL register bit is asserted the control character defined in the CNTRL software register is also allowed inside the packet. When the MUST_I register bit is asserted, the packet must be preceded by an IPG (/A/, /K/, /R/ or /I/ characters) with a minimum size of 1 character. When the MUST_I register bit is de-asserted, there are no restrictions on the IPG preceding the packet (i.e. there can be no IPG and the packets could be back to back). The packet size (excluding the /S/ and /T/ characters) must be greater than the number of columns in the PKT_MIN_LEN software register.

14.4.6 PGC Configuration

Figure 14 shows the location of the packet generator and packet comparator in the device. Both of them are located after the receive FIFO in the REFX block. Refer to Figure 5 for the complete Quadphy XR diagram and all the loopback options of the device.

Figure 14 PGC in the device



Trunk Mode Generation and Detection

Configure REFX in trunk mode. The generator and detector can be independently enabled but they share a common configuration. The PGC generator is enabled by asserting the PKT_GEN_EN software register bits for all lanes. The PGC detector is enabled by asserting the PKT_COMP_EN software register bits for lane 0.

The FRAMED_MODE register bit in each lane must be asserted. The trunked packet generated or detected will start with a PGC_S column and end with a PGC_T column. The PGC_S column is defined by the REFX PGC Start Control Character Register for each lane. The PGC_T column is defined by the REFX PGC Terminate Control Character Register for each lane. The number of columns in the trunked packet (excluding the PGC_S and PGC_T columns) is set by the PACKET_LEN register bits. The number of columns of IPG between the trunked packets is set by the IDLE_LEN register bits. The data inside the trunked packet can be PRBS 7 , PRBS 23 , incrementing mod 256 or fixed as controlled by the XOR of the PATT register bits for all the lanes and the TX_TEST_PATT_SEL register bits. If the fixed pattern is chosen, the pattern value used is what is defined in FIXED_PAT register bits. FIXED_PAT[9:8] must be set to 0 if a fixed pattern is being generated in trunk mode.

The PGC generator will generate packets even if REFX has lost alignment or byte synchronization. Writing a rising edge (0 followed by 1) to the FRC_ERR register bit of a given lane will cause a bit error on that lane inside the trunked packet. The FRC_ERR register bit must be written back to 0 before another bit error insertion can be performed since this bit is not self clearing.

The PGC detector will declare frame synchronization after one packet of the required size, PGC_S and PGC_T columns is received. The PGC detector will declare loss of frame synchronization after one packet of the wrong size, wrong PGC_S or wrong PGC_T columns is received. Frame synchronization is declared by asserting the PGC_FRAME_SYNCV status register bit for lane 0. The PGC detector will declare pattern synchronization after frame synchronization is gained and SYNC_THR consecutive data column matches. The PGC detector will declare loss of pattern synchronization if frame synchronization is lost or SYNC_LOSS consecutive data column mismatches (bit errors) occur. Pattern synchronization is declared by asserting the PGC_SYNCV status register bits for lane 0. The PGC detector will count bit errors only while it has pattern synchronization. The number of bit errors will be loaded in PGC_ERR_CNT register bits of lane 0 after a performance counters update.

Lane Mode Generation and Detection

Configure REFX in lane mode. The generator and detector for each lane can be independently enabled but they share a common configuration. The PGC generator for a given lane is enabled by asserting the TX_TEST_PATT_EN register bit or PKT_GEN_EN software register bit for that lane. The PGC detector for a given is enabled by asserting the PKT_COMP_EN software register bit for that lane.

The FRAMED_MODE register bit for each lane with an active PGC generator or detector must be asserted. The lane packet generated or detected on a given lane will start with that lane's PGC_S character and end with that lane's PGC_T character. Each lane's PGC_S character is defined by the corresponding REFX PGC Start Control Character Register for that lane. Each lane's PGC_T character is defined by the corresponding REFX PGC Terminate Control Character Register for that lane. The number of bytes in the lane packet (excluding the PGC_S and PGC_T characters) is set by the PACKET_LEN register bits. The number of bytes of IPG between the lane packets is set by the IDLE_LEN register bits. The data inside a lane packet for a given lane can be PRBS 7, PRBS 23, incrementing mod 256 or fixed as controlled the XOR of the PATT register bits for that lane and the TX_TEST_PATT_SEL register bits. If the fixed pattern is chosen on a given lane, the pattern value used is what is defined in FIXED_PAT register bits for that lane. A given lane's FIXED_PAT[9:8] must be set to 0 if a fixed pattern is being generated on that lane.

The PGC generator will generate packets even if REFX has lost byte synchronization. Writing a rising edge (0 followed by 1) to the FRC_ERR register bit of a given lane will cause a bit error on that lane inside the lane packet. The FRC_ERR register bit must be written back to 0 before another bit error insertion can be performed since this bit is not self clearing.

The PGC detector for a given lane will declare frame synchronization after one packet of the required size, PGC_S and PGC_T characters is received on that lane. The PGC detector for a given lane will declare loss of frame synchronization after one packet of the wrong size, wrong PGC_S or wrong PGC_T characters is received on that lane. Frame synchronization for a given lane is declared by asserting the PGC_FRAME_SYNCV status register bit for that lane. The PGC detector for a given lane will declare pattern synchronization after frame synchronization is gained and SYNC_THR consecutive data byte matches are detected on that lane. The PGC detector for a given lane will declare loss of pattern synchronization if frame synchronization is lost or SYNC_LOSS consecutive data column mismatches (bit errors) occur on that lane. Pattern synchronization for a given lane is declared by asserting the PGC_SYNCV status register bits for that lane. The PGC detector for a given lane will count bit errors only while it has pattern synchronization. The number of bit errors for a given lane will be loaded in PGC_ERR_CNT register bits of that lane after a performance counters update.

CJPAT and CRPAT Generation

The REFX can generate CJPAT or CRPAT in any mode (trunk, lane or serdes). Either of the TX_TEST_PATT_EN register bits or PKT_GEN_EN register bits for all the lanes must be asserted. Either of the PATT register bits for all the lane or the TX_TEST_PATT_SEL register bits must be set to 0x5 or 0x4 for CJPAT and CRPAT patterns respectively.

The PGC detector does not detect CJPAT or CRPAT patterns.

Low, Mixed and High Frequency Pattern Generation

The REFX can generate low, mixed or high frequency patterns on any given lane in lane or serdes mode. Either of the TX_TEST_PATT_EN register bits or PKT_GEN_EN register bits for the required lane must be asserted. Either of the PATT register bits for the required lane or the TX_TEST_PATT_SEL register bits must be set to 0x1, 0x2 or 0x0 for low, mixed and high frequency patterns respectively.

The PGC detector does not detect low, mixed or high frequency patterns.

Performance Counters Updating

An update of the performance counters can be requested when TIP is not asserted. An update will load all the performance counters with the current count value and reset their corresponding internal counters. A performance counters update can be initiated locally or globally:A write to the REFX Trunked Inserted Column Count register (0xD106 / 0xD206) will update all the counters (including all the performance counters) of the corresponding REFX.

A write to any TEFX counter registers will update all the counters (including all the performance counters) of the corresponding TEFX.

A write to the TIP bit in 0xD000 will update all the counters in TEFX and REFX. If any of the receive channel is disabled for power savings, then the corresponding WRCLK_MASKB and RDCLK_MASKB register bits in the REFX TIP Mask Register must be set to logic 0 to avoid freezing the performance counters when an update is requested.

14.5 Latency

The following table describe the latency of each block that is shown in Table 20.

Table 20 Block Latency

Block	Maximum Latency (bytes / words)
Deserializer	2
REFX	29
Crossbar	3
Serializer	2
TEFX	9 (8B/10B encoder disabled) / 11 (8B/10B encoder enabled)

14.6 Power-up

The QuadPHY XR operating in either 10GE or 10GFCcan all configured without using the microprocessor interface for normal operations in most applications. However, the microprocessor interface may still be required for testing, debugging and for configuring the device in various loopback modes as well as packet generation and recovering statistics. .

14.7 Interrupt Service Routine

The QuadPHY XR will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Find the register address of the corresponding block which caused the interrupt and read its Interrupt Status registers.

2. Service the interrupt(s).

3. If the *INTB* pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of *INTB*.

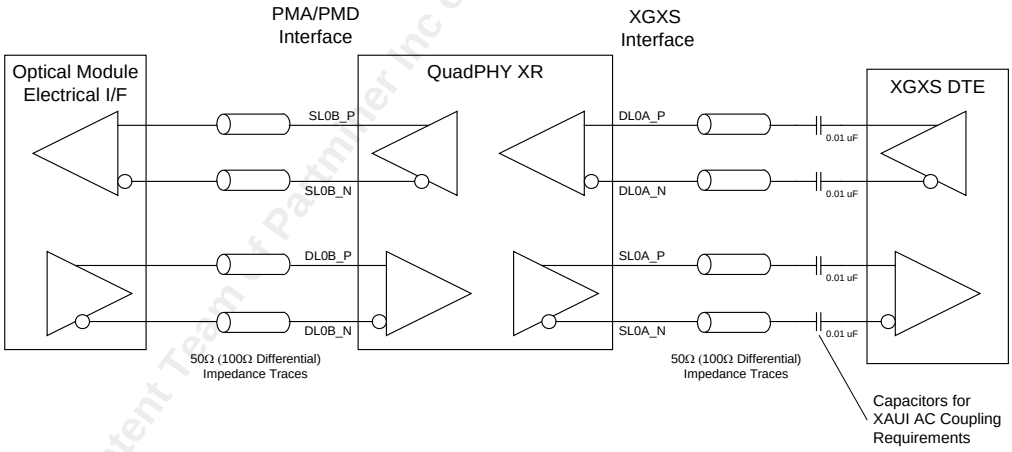
14.8 Board Design Recommendations

Please reference PMC-2030148, QuadPHY Evaluation Kit Design Document, Issue 1 for specific Board Design Issues with the QuadPHY XR.

14.9 High-Speed Serial Interface

As shown in Figure 15, the high-speed serial interface is a set of differential drivers and receivers operating over 50Ω transmission lines. The serial transmit outputs are internally terminated, complementary current-sourcing drivers. The serial receive inputs are differential receivers with internal 100Ω differential terminations.

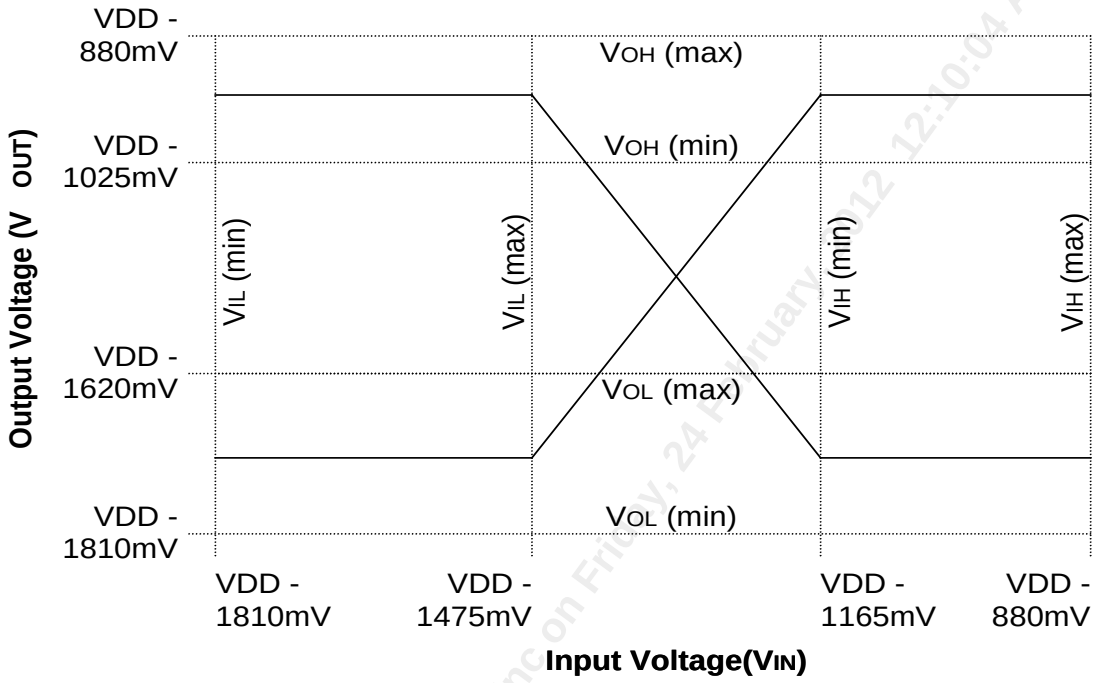
Figure 15 Serial Receive and Transmit Interface



14.10 PECL and CML Input and Output Levels

The following details 100K ECL/PECL and CML compatible input and output level characteristics. The figure below shows DC ECL/PECL output levels and their limits. We see that output levels are referenced to a positive power supply, VDD (VDD=0V for ECL and is typically 2.5V, 3.3V or 5V for PECL). Therefore, regardless of the value of VDD, the typical value of VOH is required to be 952.5 mV below VDD and the typical value of VOL is required to be an additional 762.5 mV below that.

Figure 16 PECL Levels (100K Characteristics).



CML signal are between 250 mV pp and 400 mV pp whose common mode is half the swing value from Vdd. The lower pulse amplitudes lead to lower crosstalk, EMI and noise transients. Thus each device that claims CML compatibly must be looked at carefully to insure interoperability with other devices.

14.11 High Speed Interface Considerations

14.11.1 Transmitter Interface Configuration

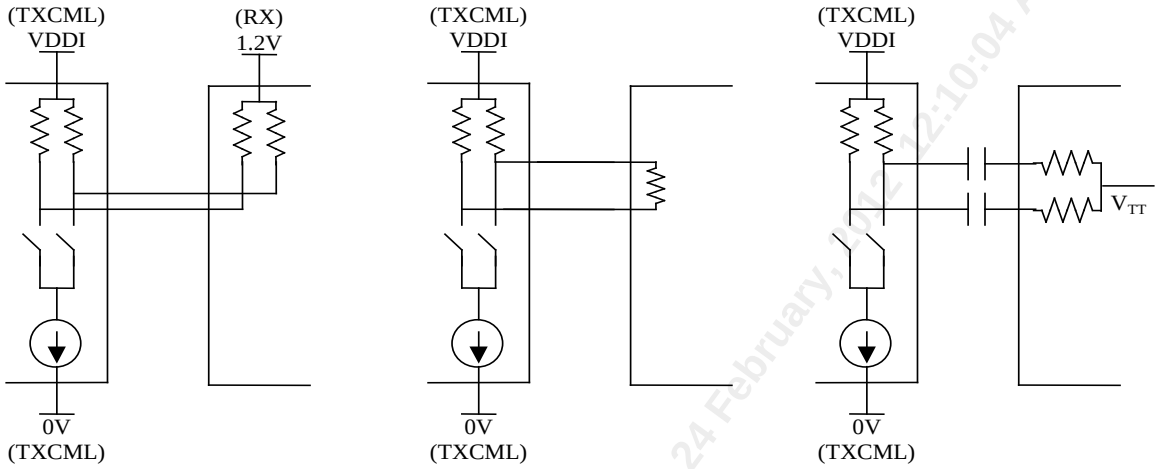
The CML (current-mode logic) transmitter includes an on-chip termination. The CML transmitter is capable of driving the following types of receiver terminations:

50Ω to 1.2Volt (Figure 17a)

100Ω floating (Figure 17b)

100Ω AC-coupled XAUI Standard (Figure 17c)

Figure 17 Transmitter Interface Configurations

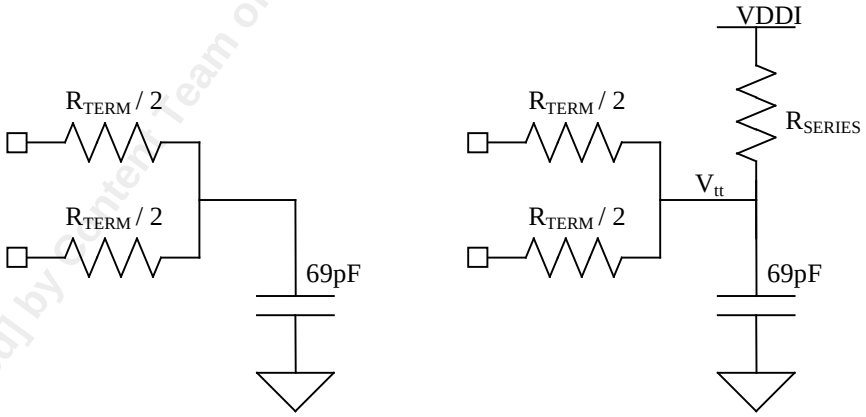


a) 50Ω to 1.2V b) 100Ω floating c) 100Ω AC coupled

14.11.2 Receiver Termination

The receiver termination can be configured to be either floating or to be connected to the 1.2V VDDI supply. This can be controlled by the RX_TERM register bit as shown inFigure 18.

Figure 18 Receiver Termination Modes



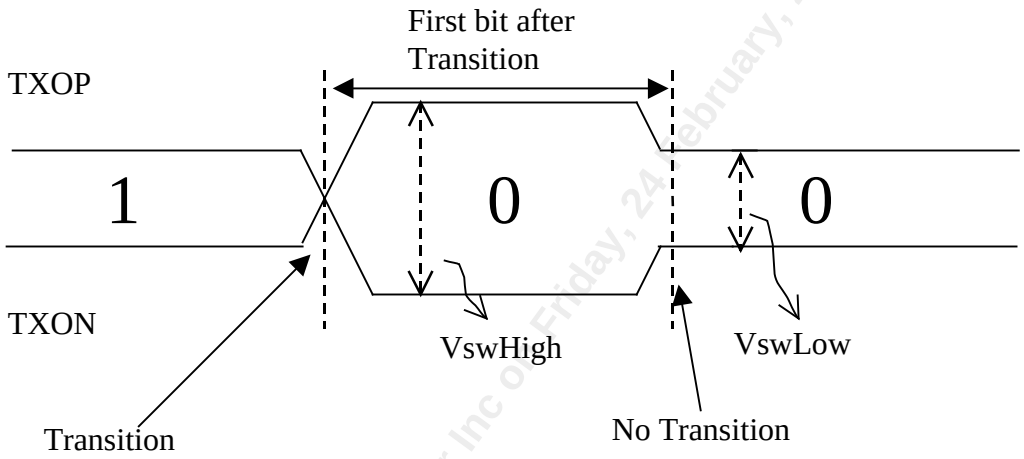
RX_TERM = 0
Floating Termination
(DC coupled, no CM current)

RX_TERM = 1
Termination to 1.2V
(for AC coupling or CML drivers, allows CM current)

14.11.3 Pre-emphasis

When using transmit pre-emphasis, the first bit that follows a transition from 1 to 0 or from 0 to 1 is output with a greater amplitude than bits that do not follow transitions. This is illustrated in Figure 19.

Figure 19 Output Waveform using Pre-emphasis



This increased amplitude of bits following transitions helps to counteract frequency dependent attenuation incurred with transmission over PCB traces and cables. The high speed CML transmitter provide programmable ratios of VswHigh to VswLow to provide optimal performance over a wide range of trace lengths.

For guidance on the usage of pre-emphasis, refer to Application Note PMC-2021098.

14.11.4 Receive Equalization

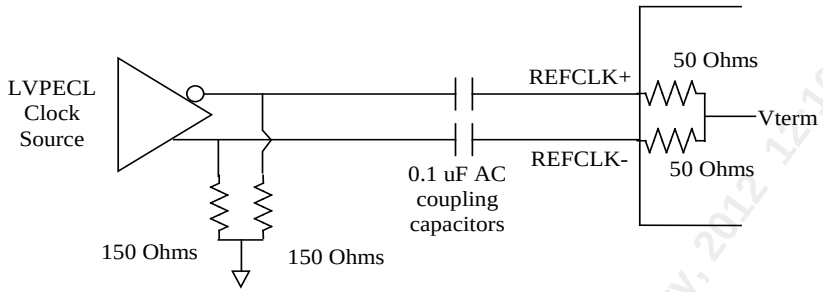
Receive equalization boosts the high frequency content of received signals, counteracting some of the high frequency attenuation incurred with transmission over PCB traces and cables. The high speed CML I/O provides 3 levels for equalization – no equalization, low equalization, and high equalization level.

For guidance on the usage of receive equalization, refer to Application Note PMC-2021098.

14.11.5 LVPECL REFCLK Inputs

The LVPECL REFCLK inputs require AC coupling capacitors between the inputs and the clock source as shown in Figure 20. The LVPECL REFCLK inputs are internally biased and have internal termination resistors therefore no external biasing or terminating resistors for the receiver are required. Resistors are still required to bias the outputs of the LVPECL clock source.

Figure 20 AC coupling for LVPECL Clock Signal to REFCLK inputs



15 Functional Timing

15.1 MDIO Functional Timing

Figure 21 MDIO I/O Functional Timing (MDIO Mode)

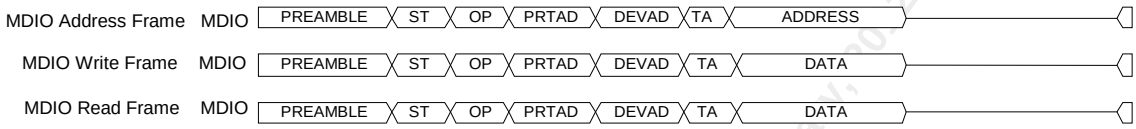


Figure 21 shows the 3 basic types of MDIO transfers on the MDIO primary bi-directional pin. The MDC clock is not shown for simplicity. . For a complete specification of the MDIO protocol please refer to Clause 45 of the IEEE P802ae Specification,

16 Absolute Maximum Ratings

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 21 Absolute Maximum Ratings

Storage Temperature	-40 °C to +125 °C
1.2V Supply Voltage (AVDL, CAVDH0, CAVDH1, VDDI)	-0.5 V to +1.8 V
2.5V Supply Voltage (AVDH, CAVDH0, CAVDH1, QAVD, VDDO)	-0.5 V to +3.6 V
Input pad tolerance	-2 V < Vpin < VDDO +2 V for 10 ns, 100 mA max
Output pad overshoot limits	-2 V < Vpin < VDDO +2 V for 10 ns, 100 mA max
Voltage on Any Digital Pin	-0.3 V to VDDO+0.3 V
Static Discharge Voltage	±2000 V (HBM) ±500 V (CDM)
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead/Ball Temperature	225 +0 –5 °C
Absolute Maximum Junction Temperature	+150 °C

Notes:

1. Most output pins require termination circuitry.
2. Overshoot duration is 10ns at 100 mA Max.

17 Normal Operating Conditions

Table 22 Normal Operating Voltages

	Operating Range[1]			Reference (approx.)
Supply Voltages	**Minimum (V)**	**Typical (V)**	**Maximum (V)**	
1.2V Core Supply Voltage (VDDi)	1.14	1.20	1.26	+/- 5%
1.2V Analog Supply Voltage (AVDLi)	1.14	1.20	1.26	+/- 5%
2.5V Analog Supply Voltage (AVDHi)	2.38	2.50	2.62	+/- 5%
2.5V Analog Supply Voltage (QAVD)	2.38	2.50	2.62	+/- 5%
2.5V I/O Supply Voltage (VDDO)	2.38	2.50	2.62	+/- 5%

Notes:

1. Power supply, D.C. characteristics, and A.C. timing are characterized across these operating ranges, unless otherwise stated
2. Where typical measurements are given, these parameter values will be used, unless otherwise stated

18 Power Information

18.1 Power Supplies

1. Use a single plane for both digital and analog grounds.

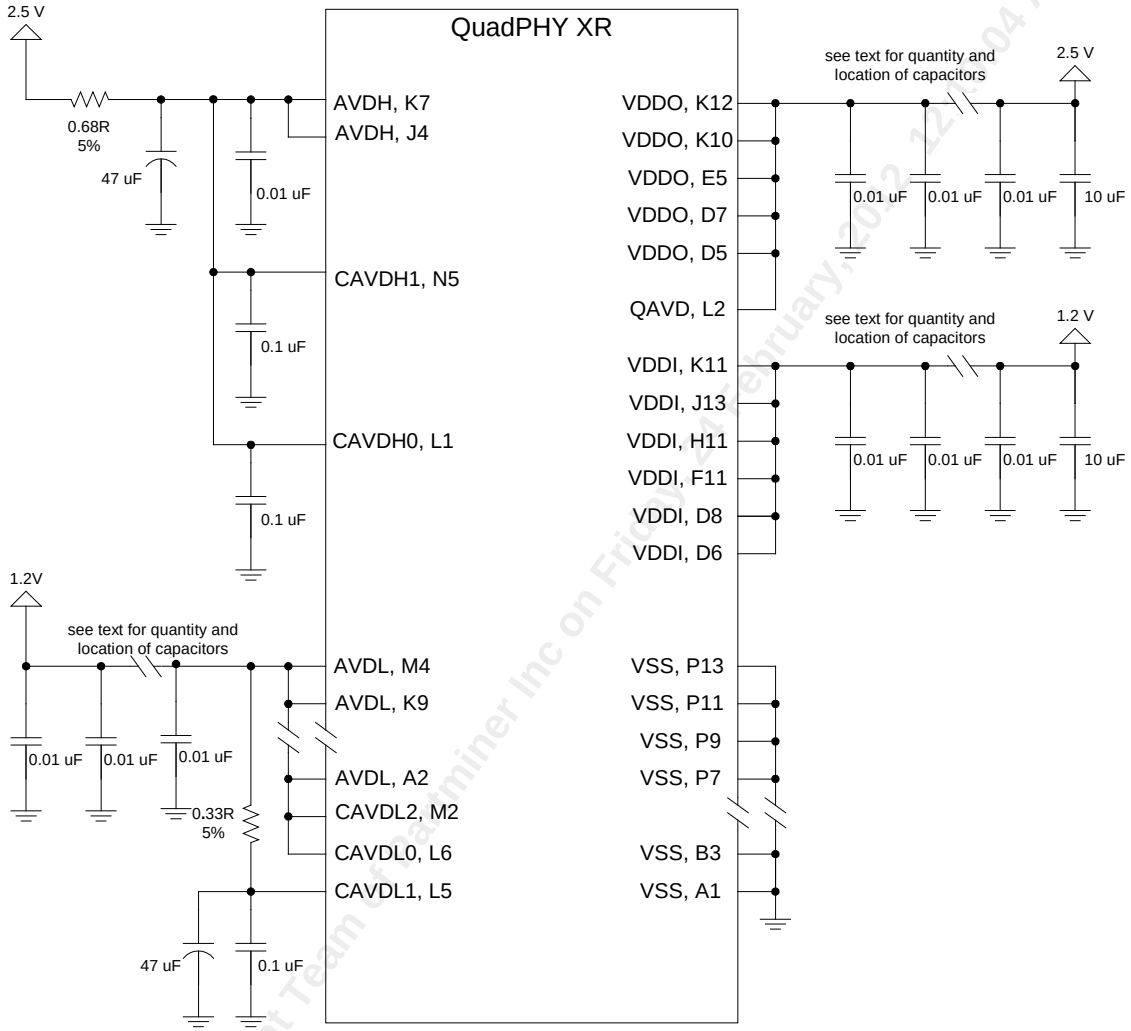
2. Provide separate analog transmit, analog receive, and digital supplies, but otherwise connect the supply voltages together at one point close to the connector where the voltage is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

18.2 Power Supply Decoupling

Figure 22 illustrates the scheme required for power supply conditioning. This conditioning scheme is suitable for boards with power supply noise up to 50 mV peak-to-peak on the 1.2Volt and 100 mV peak to peak on the 2.5 Volt power supplies. For boards with higher noise levels, additional filtering measures could be necessary.

Figure 22 Power Supply Decoupling



The 10uF Ceramic caps are X5R (X7R) type, and not Tantalum or Y5V, for best frequency response and lowest ESR. Two suggested capacitor types are:

- Taiyo Yuden PN # LMK325BJ106MN or
- Panasonic PN # ECJ-3YB0J106K

Boards that meet the following criteria may use a distributed decoupling scheme, with 0.1 uF capacitors placed on a one-inch grid.

- VDDI and VDDO pins are connected to large power planes with a minimum area of 20 square inches (~ 130 cm2) adjacent to a ground plane.
- Board stack-up has a maximum power plane to ground plane spacing of 0.006 inches

(~ 0.15 mm)

A distributed decoupling capacitor placement offers significant improvements compared to grouped placement of capacitors. This is described further in the Digital Power Supply Bypass Guidelines Application Note [References, Item 12].

On boards that do not meet these criteria, one capacitor should be used for every two VDDI (or every two VDDO) pins. The 0.1 uF capacitors should be placed as close as possible to each power pin and to ground layer. The traces from the capacitors to the QuadPHY-XR power pins and to the ground plane should be as short as possible to limit series inductance.

18.3 Power Requirements

Table 23 Power Requirements

Conditions	Parameter	Typ[1]	Pwr for Thermal Calc[1]	Max Current[1]	Units
Full duplex operation with loaded outputs	IDDOP (1.2V) Vddi	0.333	-	0.760	A
	IDDOP (2.5 V) Vddo	0.0002	-	0.0002	A
	IDDOP (2.5 V) AVDH	0.036	-	0.045	A
	IDDOP (1.2 V) AVDL	0.914	-	1.184	A
	Total Power	1.6	2	-	W

Notes on Power Information:

Outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity.

1. Power values are calculated using the formula:

   $$\text{Power} = \sum i(VDD \times IDD)$$

   Where i denotes all the various power supplies on the device, VDD is the voltage for supply i, and IDD is the current for supply i

18.4 Power Sequencing

There are no power sequencing requirement on this device. The power rails servicing the QuadPHY XR may be powered up in any order. However, there is a requirement on the input voltage on the high-speed CML receiver input when the device is powered down:

The CML receiver inputs should NOT be driven above 1.45V when the receiver is powered down.

19 D.C. Characteristics

T_A = -40 °C to T_J = 125°C , V_{DD} = $VDD_{typical}$ ± 5%
(Typical Conditions: T_J = 70 °C, V_{VDDI} = 1.2 V, V_{AVDH} = 2.5V +/- 5% only, V_{AVDL} = 1.2 V +/- 5% only, V_{QAVD} = 2.5 V +/- 5% only)

Table 24 D.C. Characteristics (CMOS/TTL)[1]

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDDI	Power Supply	1.14	1.2	1.26	Volts	
VDDO	Power Supply	2.38	2.5	2.62	Volts	
VAVDH	Power Supply	2.38	2.5	2.62	Volts	
VAVDL	Power Supply	1.14	1.2	1.26	Volts	
QAVD	Power Supply	2.38	2.5	2.62	Volts	
VIL	Input Low Voltage	-0.5	—	0.7	Volts	Guaranteed Input LOW Voltage
VIH	Input High Voltage	1.7	—	VDDo+0.5	Volts	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	—	0.1	0.4	Volts	VDDo = min, IOL = 4 mA
VOH	Output or Bidirectional High Voltage	1.8	2.2	—	Volts	VDDo = min, IOH = 4 mA
VT+	Reset Input High Voltage	2.0			Volts	Applies to RSTB and TRSTB only.
VT-	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
VTH	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB and TRSTB only.
IILPU	Input Low Current	+20	+83	+200	µA	VIL = GND. Notes 4 and 6.
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 4 and 6.
IIL	Input Low Current	-10	0	+10	µA	VIL = GND. Notes 5 and 6.
IIH	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 5 and 6.
|ΔVODM|	Change in |VODM| between “0” and “1”			25	mV	RLOAD=100Ω ±1%
ΔVOCM	Change in VOCM between “0” and “1”			25	mV	RLOAD=100Ω ±1%
$V_{IA, PECL}$	PECL Input Amplitude	0.4		2.0	Vppd	Differential Peak-to-Peak Voltage (Rx)
CIN	Input Capacitance		5		pF	tA=25°C, f = 1 MHz
COUT	Output Capacitance		5		pF	tA=25°C, f = 1 MHz
CIO	Bi-directional Capacitance		5		pF	tA=25°C, f = 1 MHz

Notes on D.C. Characteristics:

1. This table defines the thresholds that allow CMOS input pads to be compatible for the TTL input thresholds of the input only pad. See notes (2) and (3)
2. The threshold of logic low is specified as the CMOS's V_{IL} max that is compatible with the TTL's V_{IL} or 0.8 V in all cases of V_{DD}.
3. The threshold of logic high is specified as the minimum TTL's V_{IH} or 2 V that insure the compatibility with all CMOS's V_{IH} in all cases of V_{DD}.
4. Input pin or bi-directional pin with internal pull-up resistor.
5. Input pin or bi-directional pin without internal pull-up resistor
6. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

20 A.C Characteristics

Unless otherwise stated, the following parameters are provided given the following conditions:

Ta = -40C to Tj = 125C, V_{AVDH} = 2.5 V ±5%, V_{AVDL} = 1.2 V ±5%, V_{QAVD} = 2.5 V ±5%. V_{VDDO} = 2.5 V ±5% V_{VDDI} = 1.2 V ±5%

20.1 MDIO Interface Characteristics

Table 25 Electrical Characteristics of MDIO and MDC Inputs

Symbol	Parameter	1.2v MDIO mode (MDIO_SEL pin = "high")		1.8v/2.5v/3.3vv Hybrid mode (MDIO_SEL pin = "low")		
		Min	Max	Min	Typ	Max
V_{IH}	Input high voltage	0.84 V	1.5 V	1.1 V		3.6 V
V_{IL}	Input low voltage	-0.3 V	0.36 V	-0.3 V		0.7 V
V_{OH}	Output high voltage	1.0 V	1.5 V	1.35 V/1.8 V/2.4 V		2.0 V/2.7 V/3.6 V
V_{OL}	Output low voltage	-0.3 V	0.2 V	-0.3 V		0.4 V
I_{OL}	Output low current	+4 mA (V_I=0.2 V)			5.64 mA / 7.20 mA / 9.66 mA[1]	
C_i	Input capacitance		10 pF			10 pF
C_L	Bus loading		470 pF			470 pF

Notes:

1. These are based on average measured results with an external resistance of 170/300/300 ohms in series and an external load of 470pF in parallel.

Table 26 CPU Interface Section

Symbol	Parameter	Min	Typ.	Max	Unit
MDC_Per	MDC period	100		-	ns
$t_{MDCHIGH}$	MDC high pulse width	45		-	ns
t_{MDCLOW}	MDC low pulse width	45		-	ns
t_{MDS}	MDIO setup time	10		-	ns
t_{MDH}	MDIO hold time	10		-	ns
t_{MDR}, t_{MDF}	Rise/fall time of MDC and MDIO signal[1]	5		-	ns
t_{Delay}	MDC to MDIO delay	0		300[2]	ns

Notes:

1. MDC or MDIO rise times and fall times are measure from 10% to 90%.
2. The load is 470 pF.

Figure 23 Behavior of MDIO During Turnaround Time of a Read Transaction

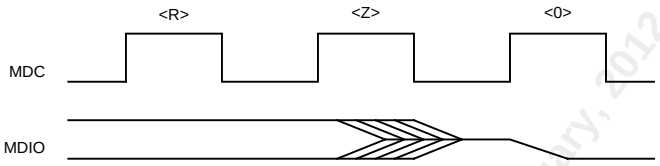


Figure 24 MDIO Sourced by STA

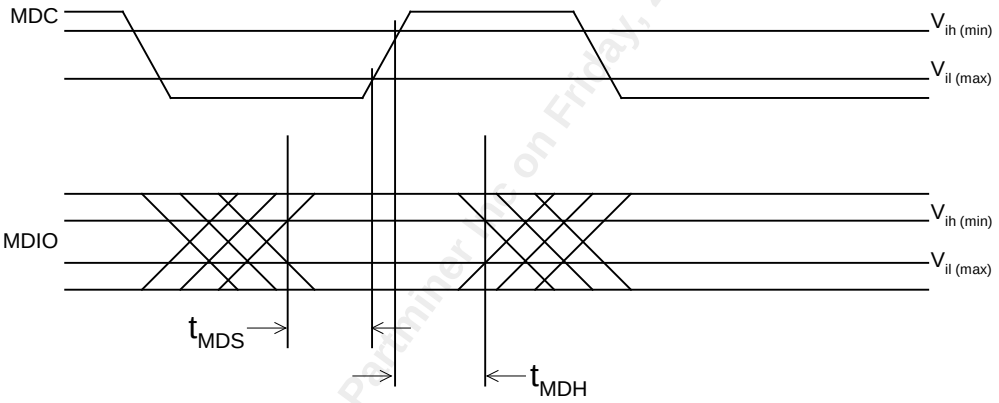
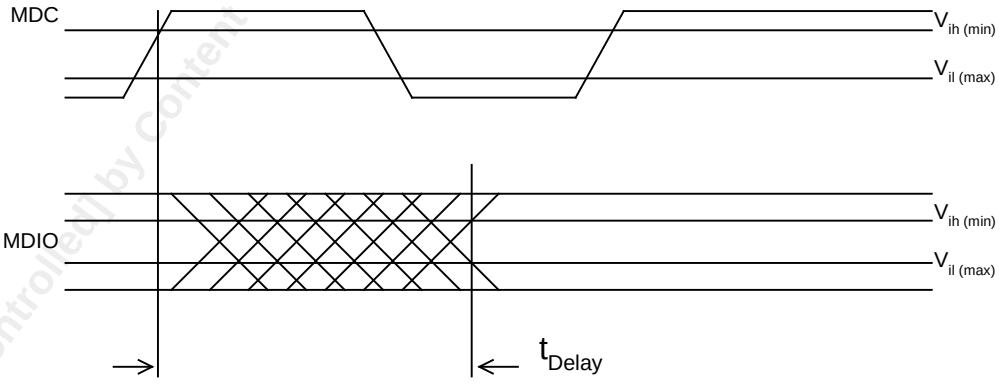


Figure 25 MDIO Sourced by PHY



20.2 High Speed Output Characteristics

Table 27 High-speed Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T_{DRF}	Differential rise/fall time, 20%-80%.	--	80	--	ps	
Z_D	Differential Impedance	85	100	115	ohm	
DJod	Output Data Deterministic Jitter 2	--	--	0.17	UI	
TJod	Total Output Data Jitter	--	--	0.35	UI	
UI	Unit Interval	313		833	ps	1.2 to 3.2 Gbit/s

Note:

1. Transmit_Mode [4:0] bus is set to 10010 under all measurement conditions.
2. The unit interval (UI) is the reciprocal of symbol rate. At 2.488Gbit/s, 1UI = 402ps.
3. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
4. Jitter values are measured with each LVDS output AC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
5. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
6. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.

Table 28 Differential Peak to Peak Output Amplitude, No Pre-emphasis

(See Figure 26 for Signal definition)

Output Level Control		100Ω Floating / 100Ω AC-coupled [1] (mV ppd) [2,3]		
Register Control Transmit Mode [4:0]	Pin Control HC [1:0]	Min.	Typical	Max.
01000		458	568	688
01001		508	630	762
01010	00	556	690	832
01011		606	750	902
01100		656	810	970
01101	01	704	866	1038
01110		752	922	1102
01111		800	976	1164
10000	10	844	1030	1222
10001		888	1080	1276
10010		930	1126	1324
10011	11	970	1170	1366
10100		1000	1210	1404
11111		1100	1400	1600

Notes:

1. The receiver termination is assumed to have a tolerance of ± 5%
2. High Speed output peak-peak differential voltages are measured with 100 ohm external differential termination at the pin of the device.

Figure 26 Signal Level with No Pre-emphasis

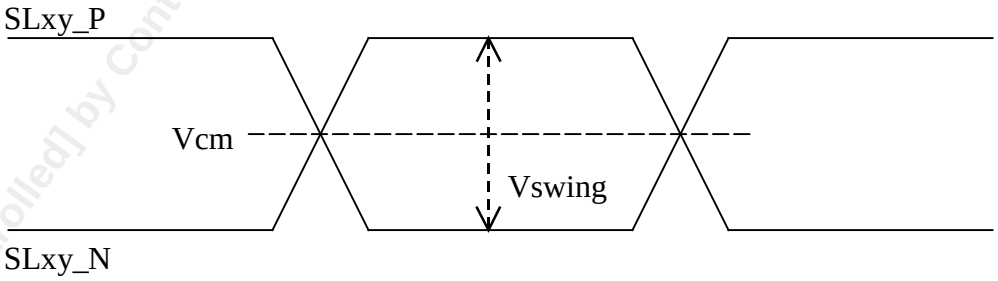


Table 29 Differential Peak to Peak Output Amplitude, Pre-emphasis Enabled, Register Control

(See Figure 27 for Signal definition)

Output Level Control		100Ω Floating / 100Ω AC-coupled [1] (mV ppd) [2]		
Register Control Transmit_Mode [4:0]		Min	Typical	Max
Bit Amplitude, first bit after transition, set by Transmit_Mode[4:3]				
00 XXX		888	1080	1276
01 XXX		930	1126	1324
10 XXX		970	1170	1366
11 XXX		1000	1210	1404
Bit Amplitude, for consecutive identical bits, set by Transmit_Mode[2:0]				
XX **000**		458	568	688
XX **001**		508	630	762
XX **010**		556	690	832
XX **011**		606	750	902
XX **100**		656	810	970
XX **101**		704	866	1038
XX **110**		752	922	1102
XX **111**		800	976	1164

Notes:

1. The receiver termination is assumed to have a tolerance of ± 5%
2. High Speed output peak-peak differential voltages are measured with 100 ohm external differential termination at the pin of the device.

Figure 27 Signal Level with Pre-emphasis

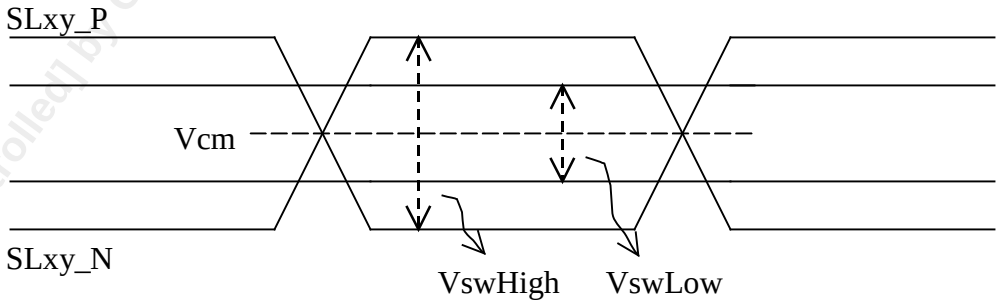


Table 30 Differential Peak to Peak Output Amplitude, Pre-emphasis Enabled, Pin Control

(See Figure 27 for Signal definition)

Output Level Control		100Ω Floating / 100Ω AC-coupled [1] (mV ppd) [2]		
	Pin Control HC [1:0]	Min	Typical	Max
Pre-emphasis Settings, set by HC[1:0] pins				
	HC[1:0] = 00 **Pre-emphasis = 1/0.46**	970	1170	1366
		458	568	688
	HC[1:0] = 01 **Pre-emphasis = 1/0.56**	970	1170	1366
		556	690	832
	HC[1:0] = 10 **Pre-emphasis = 1/0.66**	970	1170	1366
		656	810	970
	HC[1:0] = 11 **Pre-emphasis = 1/0.76**	970	1170	1366
		752	922	1102

Notes:

1. The receiver termination is assumed to have a tolerance of ±5%
2. High Speed output peak-peak differential voltages are measured with 100 ohm external differential termination at the pin of the device.

20.3 High Speed Input Characteristics

Table 31 High-speed Input Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DJid	Deterministic Jitter Tolerance	--	--	0.37	UI	peak-to-peak value
TJid	Total Jitter Tolerance	--	--	0.65	UI	peak-to-peak value
V_{tt}	Termination Voltage	1.1	1.2	1.26	V	
L_{DR}	Differential Return Loss	10		--	dB	From 100 MHz to 2.5 GHz
L_{CR}	Common Mode Return Loss	6		--	dB	From 100 MHz to 2.5 GHz
V_{Rsense}	Differential Input Sensitivity	150	--	--	mVpp	Peak-to-Peak Differential
V_{Rmax}	Max Differential Input Voltage	--	--	2.2	Vpp	Peak-to-Peak Differential
T_{Reye}	Receiver Eye Opening	0.26	--	--	UI	<= 2.5 Gbit/s
		0.35	--	--	UI	> 2.5 Gbit/s
V_{RCM}	Common Mode Range	0.2	--	1.6	V	If AC-coupled, $V_{RCM} = V_{tt}$
R_{TERM}	Differential Termination resistance (see **Figure 18**)	85	100	115	Ω	
R_{SERIES}	Series resistance (see Figure 4)	--	--	2	Ω	

Notes:

3. The unit interval (UI) is the reciprocal of symbol rate. At 2.488Gbit/s, 1UI = 402ps.
4. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
5. Jitter values are measured with each high-speed input AC coupled into a 50 Ohm impedance.
6. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
7. Jitter tolerance and, Differential Input Sensitivity and Receiver Eye Opening parameters are guaranteed when Full Rx Equalization is enabled.

Figure 28 XAUI Sinusoidal Jitter Tolerance Mask

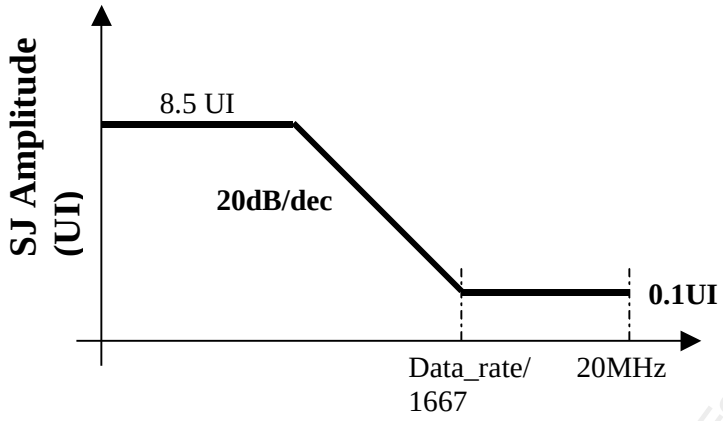


Table 32 Reference Clock Input Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DCref	REFCLK Duty Cycle	45	--	55	%	
TJref	Wideband Peak to peak jitter on REFCLK (10 Hz-20MHz) (RMS jitter is peak to peak jitter divided by 7) Narrowband peak to peak jitter on REFCLK (12kHz-20 MHz)	--	--	50 28	pS	See Note 1
tRFref	REFCLK Rise / Fall Times (20% to 80%)			1	ns	
V_{Rsense}	Differential Input Sensitivity	175	--	--	mVpp	Peak-to-Peak Differential
V_{Rmax}	Max Differential Input Voltage	--	--	2.2	Vpp	Peak-to-Peak Differential
R_{TERM}	Differential Termination resistance (see **Figure 18**)	80	100	120	Ω	

Notes:

1. Total jitter includes both deterministic jitter and random jitter but it is assumed the majority of the jitter is random.
2. Reference Clock inputs must be AC-coupled.

20.4 Reset Timing

Table 33 System Miscellaneous Timing

Symbol	Description	Min	Type	Max	Units
tV_{RSTB}	RSTB input pulse width	100			ns

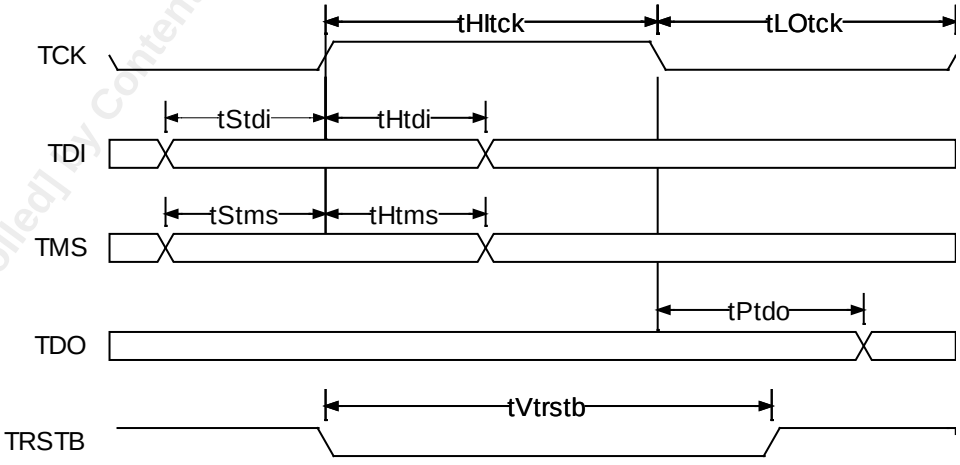
Figure 29 Reset Timing

Table 22 JTAG Port Interface

Symbol	Description	Min	Max	Units
fTCK	TCK Frequency		4	MHz
tHITck	TCK HI Pulse Width	100		ns
tHITck	TCK LO Pulse Width	100		ns
tSTMS	TMS Set-up time to TCK	25		ns
tHTMS	TMS Hold time to TCK	25		ns
tSTDI	TDI Set-up time to TCK	25		ns
tHTDI	TDI Hold time to TCK	25		ns
tPTDO	TCK Low t TDO Valid	2	25	ns
tVTRSTB	TRSTB Pulse Width	100		ns

20.5 JTAG Timing

Figure 30 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

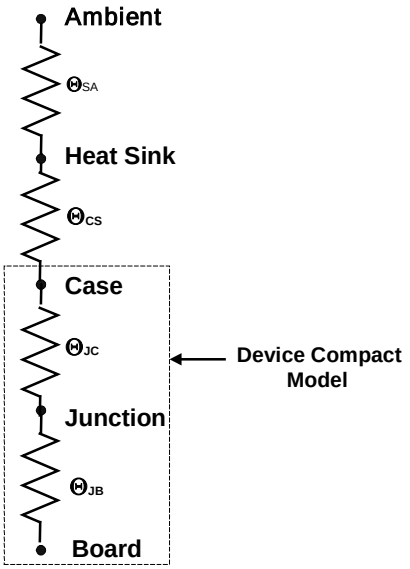
2. Maximum output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

21 Ordering, Thermal and Reliability Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for commercial applications such as central office equipment[1].

Maximum long-term operating junction temperature to ensure adequate long-term life	105 ^{0}C
Maximum junction temperature for short-term excursions with guaranteed continued functional performance.[2]	125 ^{0}C
Minimum ambient temperature	-40 ^{0}C

Device Compact Model[3]	
Θ_{JC} (^{0}C/W)	7.5
Θ_{JB} (^{0}C/W)	20.04



Thermal Resistance vs. Air Flow[4]			
Airflow	Natural Convection	200 LFM	400 LFM
θ_{JA} (°C/W)	28.52	25.3	23.99

To obtain power information for thermal calculations, refer to values in Table 23

Heat Sink Requirements	
θ_{SA}+ θ_{CS}[5]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: [(105 - T_A) / P_D] - θ_{JC}] °C/W where: T_A is the ambient temperature at the heatsink location P_D is the operating power dissipated in the package
θ_{SA} and θ_{CS} are required for long-term operation[6]	

Table 34 Ordering Information

Part No.	Description
PM8357-NI	196-Pin CABGA, 15x15 mm; 1mm BP
PM8357-NGI	196-Pin CABGA; 15 x 15 mm; 1.0 mm BP (RoHS-compliant)

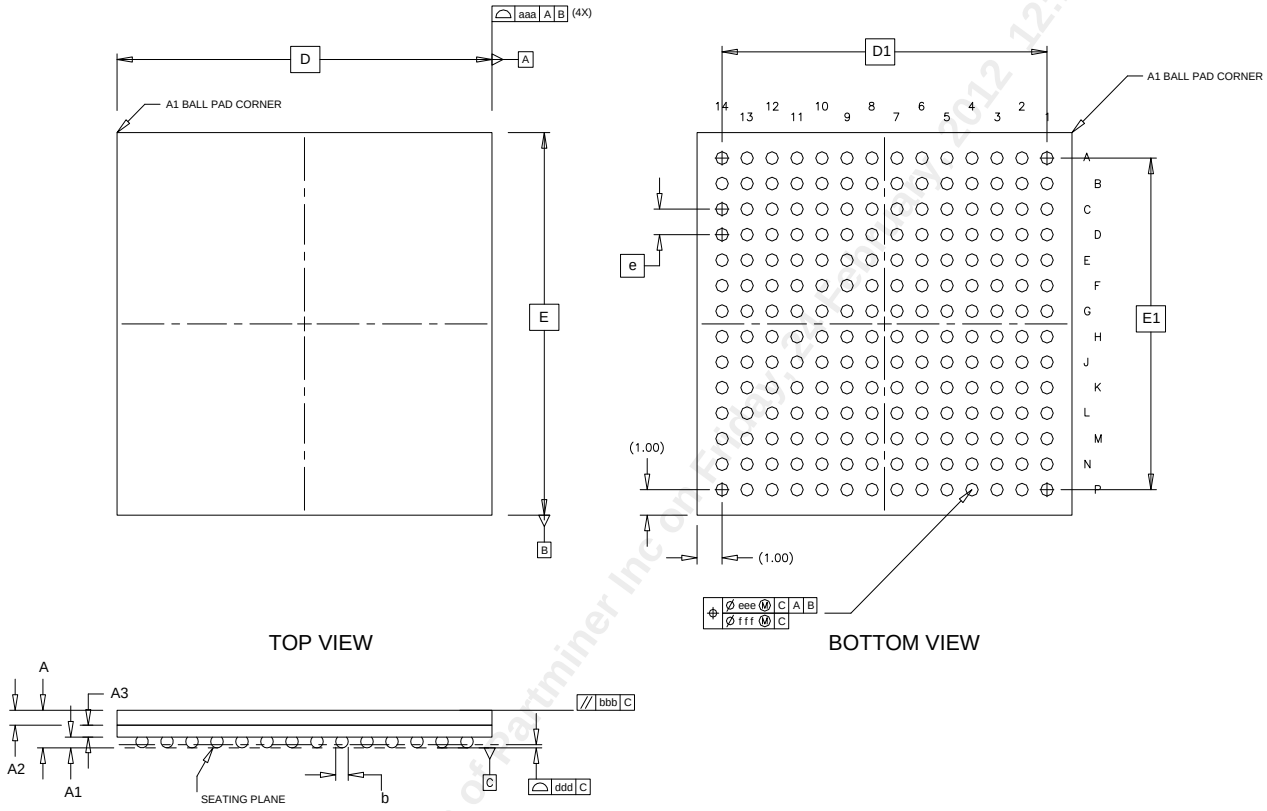
Notes:

1. The minimum ambient temperature for Central Office Equipment approximates the minimum ambient temperature requirement for Commercial Equipment.
2. Short-term is understood as the definition stated in Bellcore Generic Requirements GR-63-Core.
3. Θ_{JC}, the junction-to-case thermal resistance is a measured nominal value +2 sigma. Θ_{JB}, the junction-to-board thermal resistance is obtained by simulating conditions described in JEDEC Standard, JESD 51-8.
4. θ_{JA} is the total junction to ambient thermal resistance as measured according to JEDEC Standard JESD51 (2S2P).

5. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material.
6. The actual θ_{SA} required may vary according to the air speed at the location of the device in the system with all the components in place.

22 Mechanical Information

Figure 31 Mechanical Drawing 196 PIN BGA - 15x15 MM BODY – (N SUFFIX) (preliminary)



NOTES: 1) ALL DIMENSIONS IN MILLIMETERS
2) DIMENSION aaa DENOTES PACKAGE PROFILE
3) DIMENSION bbb DENOTES PARALLELISM
4) DIMENSION ddd DENOTES COPLANARITY
5) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MO-192 VARIATION DAE-1 WITH THE EXCEPTION OF BALL SIZE

PACKAGE TYPE: 196 CHIP ARRAY BALL GRID ARRAY (2 LAYER) – CABGA															
BODY SIZE: 15 x 15 x 1.40mm															
Dim.	A	A1	A2	A3	D	D1	E	E1	e	b	aaa	bbb	ddd	eee	f f f
Min.	1.30	0.31	0.65	-	-	-	-	-	-	-	-	-	-	-	-
Nom.	1.40	0.36	0.70	0.34	15.00 BSC	13.00 BSC	15.00 BSC	13.00 BSC	1.00 BSC	0.46	-	-	-	-	-
Max.	1.50	0.41	0.75	-	-	-	-	-	-	-	0.10	0.10	0.12	0.15	0.08

Notes

Mouser Electronics

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Microchip:
PM8357-NI