PM7348

S/UNI IMA 4

S/UNI Inverse Multiplexing for ATM, 4 Links

Datasheet

Proprietary and Confidential

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Patents

Granted

The technology discussed in this document is protected by one or more of the following patent grants:

U.S. Patent No. 5,875,192; 6,584,521; 6,680,954; 6,671,758; 6,774,693

Canadian patent 2,209,388.

Other relevant patent applications may also exist.

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Revision History

Issue No.	Issue Date	Details of Change
3	March 2008	Changes include: • Added the ADJ_DELAY_TOGGLE bit to bit 31 of word 1 of the RDAT IMA Group Context record (MEM_SELECT=9). • Updated LSEL field of Register 0x350. • Added register 0x354. • Added the ICP_INIT_DONE bit to bit 8 of word 0 of the RDAT Link Context Memory (MEM_SELECT=4). • Added Group_Tag and TRL fields to the indirect data register 0x352 for LSEL = b'01. • Added the DHCSADD bit to Register.0x072. • Updated the sections titled "Delay Compensation Buffers", "Group Start-up and Differential Delay" and "Link Addition and Differential Delay" to indicate that DIFF_DELAY_INT will occur if link addition fails. • Updated the RX_IMA_ID field description in the RIPP Group Context Record Structure. • Corrected the description of RX_FE_INFO_VALID in the RIPP Group Context Record Structure. • Corrected the Data field name of RIPP RX Link Configuration Record Structure Word 0 Bit 1. • Corrected the description for RX_IMA_ID_CFG_EN in the RIPP RX Link Configuration Structure. • Updated the RESET bit description of Register 0x000. • Added timeout period details for Register 0x210. • Added the register name to the Register Memory Map for Register 0x208 • Updated the register name in the Register Memory Map for Register 0x336. • Updated the section "Configuring a Link for IMA" within the "Configuring For IMA Operations". • Updated the Command Register Encoding parameters for Start_LASR and Delete_link in Table 16. • Corrected the information regarding the results of an overrun for Register 0x328-0x332 Transmit Link FIFO Overrun Interrupt Register. • Updated the Pinout Diagram to the correct version. • Updated the pin counts for the SDRAM I/F, Clk/Data, and General to the correct number of signals. • Changed the pins identified as "Reserved" in the General Pin Description section to "NC". • Updated RA_UTOP_MODE bit description for register 0x024 Receive. • Updated the Patent subsection to include the relevant patents.

Issue No.	Issue Date	Details of Change
		• Added Register 0x354 to the Register Memory Map. • Updated register name in Register 0x352 in the Register Memory Map.
2	May 2002	CBA[2:0] and VDDI Pins corrected
1	July 2002	Original release

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1 Definitions

Table 1 Terminology

Term	Definition
Any-PHY	Interoperable version of UTOPIA and UTOPIA L2, with inband addressing.
ATM	Asynchronous Transfer Mode
CDV	Cell Delay Variation
CTC	Common Transmit Clock
DLL	Delay Locked Loop
ECBI	Enhanced Common Bus Interface (asynchronous register bus and interface)
FIFO	First-In-First-Out
Framed	Framing information available – may be channelized or unchannelized.
HEC	Header Error Check
HCS	Header Check Sequence
ICP	IMA Control Protocol Cell
IDCC	IMA Data Cell Clock
IDCR	IMA Data Cell Rate
IFSN	IMA Frame Sequence Number
IMA	Inverse Multiplexing for ATM
ITC	Independent Transmit Clock
LCD	Loss of Cell Delineation
LID	Link ID
LSI	Link Stuff Indication
MIB	Management Information Base
MCFD	Multi-Channel Cell Based FIFO
OAM	Operation, Administration and Maintenance
OCD	Out of Cell Delineation
PISO	Parallel in Serial Out
PM	Plane Management (Microprocessor)
RCAS	Receive Channel Assigner
RDAT	RX IMA Data Processor
RIPP	RX IMA Protocol Processor
RMTS	RX Master TX Slave
SIPO	Serial in Parallel Out
TC	Transmission Convergence
TCAS	Transmit Channel Assigner
TDM	Time Division Multiplexing
TRL	Timing Reference Link
TRLCR	TRL Cell Rate

Term	Definition
TSB	Telecom Systems Block
TC	Transmission Convergence
TIMA	TX IMA Processor
Unframed	No framing information available
UTOPIA	Universal Test & Operations PHY Interface for ATM

2 Features

The PM7348 S/UNI IMA 4 device is a monolithic integrated circuit that implements the ATM Forum Inverse Multiplexing for ATM (IMA 1.1) protocol with backward compatibility to IMA 1.0 and the Transmission Convergence (TC) layer function.

The S/UNI IMA 4 device supports 4 independent T1, E1 or unchannelized physical links via a clock/data interface. Each link is dynamically configurable to support IMA 1.1, backward compatible IMA 1.0, or ATM HEC cell delineation. ATM over fractional T1/E1 is also supported. Unchannelized links may be used to support applications such as G.SHDSL or ADSL.

Standards Supported

- ATM Forum Inverse Multiplexing for ATM Specification Version 1.1, March 1999.
- ATM Forum Inverse Multiplexing for ATM Specification Version 1.0 – supports the method of reporting Rx cell information as in Appendix C.8 of the ATM Forum Inverse Multiplexing for ATM Specification Version 1.1 for symmetrical configurations.
- I.432-1 B-ISDN user network interface – Physical Layer specification: General characteristics.
- I.432-3 B-ISDN user network interface – Physical Layer specification: 1544 kbps and 2048 kbps operation.
- ATM on Fractional E1/T1, af-phy-0130.00 October, 1999.

IMA Features

- IMA 1.1 protocol including group and link state machines implemented by on-chip hardware.
  - The S/UNI IMA device performs all ICP cell processing internally with no requirement for microprocessor intervention; however, ICP cells are made available for diagnostic purposes.
- Supports up to four simultaneous IMA groups.
- Each IMA group can support any number of supported links.
- Each link can be programmed for either IMA processing or cell delineation.
- Supports all IMA Group Symmetry modes:
  - Symmetrical configuration with symmetrical operation.
  - Symmetrical configuration with asymmetrical operation.
  - Asymmetrical configuration with asymmetrical operation.
- Performs IMA differential delay calculation and synchronization.

- Provides programmable limit on differential delay tolerance and minimum number of links per group.

- Supports up to 282 ms (for T1 links) and 226 ms (for E1 links) link-differential delay among links in an IMA group.
- Performs ICP and stuff-cell insertion and removal.
- Supports both Common Transmit Clock (CTC) and Independent Transmit Clock (ITC) transmit ICP stuffing modes.
- Supports IMA frame lengths (M) equal to 32, 64, 128, or 256.
- Optionally supports the IMA 1.0 method of reporting Rx cell information as defined in appendix C.8 of the ATM Forum Inverse Multiplexing for ATM Specification Version 1.1 for symmetrical configurations; also optionally supports the IMA 1.1 method of reporting Rx cell information when sending and receiving the IMA 1.0 OAM Label.
- Provides IMA layer statistic counts and alarms for support of IMA Performance and Failure Alarm Monitoring and MIB support.
- Provides per link counters for statistics and performance monitoring:
  - ICP Violations.
  - OIF anomalies.
  - Rx Link stuff events.
  - Tx Link stuff events.
  - User cells.
  - Filler cells.
- Provides per group counters for statistics and performance monitoring:
  - User cells received.
  - Filler cells received.
  - User cells transmitted.
  - Filler cells transmitted.

TC Features

- Performs cell delineation on all links.
- Performs receive cell Header Error Check (HEC) checking and transmit cell HEC generation.
- Optionally supports receive cell payload unscrambling and transmit cell payload scrambling.
- Provides TC layer statistics counts and alarms for MIB support.

Interface Support

- Clock/Data Interface:

- Supports four individual serial (T1 or E1 or unchannelized rates up to 8 Mbps) links via a two-pin line interface.
- Supports ATM over fractional T1/E1 by providing the capability to select any DS0 timeslots that are active in a link.
- Serial link interface supports both independent transmit clock (ITC) and common transmit clock (CTC) options.

- Interfaces to a 1M x 16 SDRAM (16 Mbits of storage for 282 msec of T1, 226 msec of E1 differential delay tolerance) through a 16-bit SDRAM interface. Note that other larger SDRAM sizes can also be supported to support future market availability.
- Provides a 16-bit microprocessor bus interface for configuration and Link and Unit Management.
- ATM receive interface supports 8- and 16-bit UTOPIA L2 or Any-PHY cell interfaces at clock rates up to 52 MHz.
  - Any-PHY receive slave appears as single device. The PHY-ID of each cell is identified in the in-band address.
  - UTOPIA L2 receive slave appears as a 4 port multi-PHY.
  - UTOPIA L2 receive slave can also appear as a single port with the logical port provided as a prepend or in the HEC/UDF field.
- ATM transmit interface supports 8- and 16-bit UTOPIA L2 and Any-PHY cell interfaces at clock rates up to 52 MHz.
  - Each link configured for cell delineation or each IMA group appears as a PHY port on the Any-PHY and UTOPIA L2 bus.
  - Any-PHY transmit slave appears as a 4-port multi-PHY. The PHY-ID of each cell is identified in the in-band address.
  - UTOPIA L2 transmit slave appears as a 4-port multi-PHY.

Loopback and Diagnostic Features

- Supports UTOPIA L2 / Any-PHY Loopback (global loopback– where all cells received on the UTOPIA L2 / Any-PHY interface are looped back out).
- Supports Line Side Loopback (global loopback– where all data received on the line side is looped back out).
- Supports the capability to trace ICP cells for any group.

Software

The S/UNI IMA device driver, written in ANSI C, provides a well-defined Application Programming Interface (API) for use by application software. Low level utility functions are also provided for diagnostics and debugging purposes. Software wrappers are used for RTOS-related functions making the S/UNI IMA device driver portable to any Real Time Operating System (RTOS) and hardware environment. The S/UNI IMA device driver is compatible across the S/UNI IMA family of devices.

Packaging

- Implemented in low power, 0.18 micron, 1.8V CMOS technology with TTL compatible inputs and outputs
- Provides a standard 5-pin P1149 JTAG port
- 324 ball PBGA, 23mm x 23mm

Applications

- Integrated Access Device (IAD)
- Digital Subscriber Loop Access Multiplexers (DSLAMs)
- Wireless Base Transceiver Stations
- Customer Premises Equipment (CPE)

3 References

1. AF-PHY-0086.001, *Inverse Multiplexing for ATM (IMA) Specification Version 1.1*, March 1999.

2. I.432-1 B-ISDN, *User Network Interface – Physical Layer specification: General characteristics*.

3. I.432-3 B-ISDN, *User Network Interface – Physical Layer specification: 1544 kbps and 2048 kbps operation*.

4. G.804, *ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)*.

5. AF-PHY-0016.000, *ATM Forum DS1 Physical Layer Specification*.

6. AF-PHY-0064.000, *ATM Forum E1 Physical Interface*.

7. ATM Forum, *UTOPIA, an ATM-PHY Layer Specification*, Level 2, V. 1.0, Foster City, CA USA, June 1995.

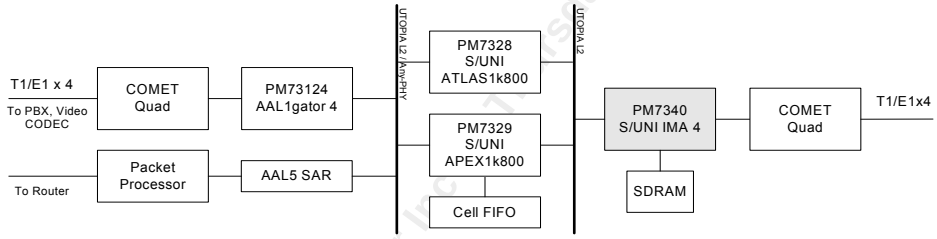
8. PMC-1990712, *VORTEX Chip Set Introduction*, 1999, Issue 1.

4 Application Examples

4.1 Integrated Access Device (IAD)

Multiservice access equipment such as Integrated Access Devices (IADs) and Access Concentrators consolidate voice, data, Internet, and video wide-area network services over ATM unifying the functions of many different types of equipment including CSUs, DSUs, multiplexers and FRADs. Figure 1 is an example of a multiservice access box using IMA over multiple T1/E1 lines or IMA over G.shdsl for WAN access.

Figure 1 Multiservice Access – IADs and Access Concentrators

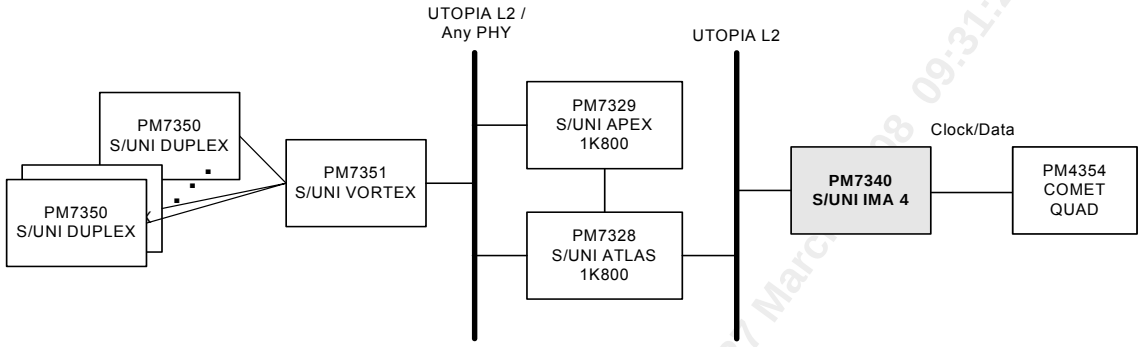


On the network side, the S/UNI IMA 4 device interfaces seamlessly to standard T1/E1 framers such as the PM4354 COMET QUAD T1/E1 Framer Plus LIU and to any device with a clear-channel clock and data interface. Alternately, the S/UNI IMA 4 interfaces seamlessly with G.shdsl Modems via the PCM interfaces to allow multiple DSL links multiplexed into a single higher bandwidth channel. An external low-cost standard 1Mx16 SDRAM must buffer data for tolerating up to a maximum of 282 msec (T1) / 226 msec (E1) of differential delay across the serial clock and data links.

4.2 Remote DSLAM WAN Uplink

Coupled with ATM, remote DSLAMs enable service providers to use the bandwidth of the T1/E1 infrastructure for delivering integrated services such as high-speed Internet access and real-time voice and video. ATM over T1/E1 is a suitable remote DSLAM WAN uplink technology and IMA, due to its benefits of higher bandwidth, statistical gain and fault tolerance, is even more suitable. Figure 2 shows an example of the S/UNI IMA 4 device in a remote DSLAM WAN uplink application.

Figure 2 Remote DSLAM WAN Uplink



The design shown in Figure 2 is built on the Vortex Chipset, which comprises the PM7351 S/UNI VORTEX, PM7350 S/UNI DUPLEX, PM7329 S/UNI APEX-1K800 and PM7328 S/UNI ATLAS-1K800 devices. Each S/UNI VORTEX aggregates traffic from up to eight S/UNI DUPLEXs which, in turn, aggregate traffic from multiple DSL MODEMs and/or COMET QUAD Framer plus LIUs. The S/UNI APEX-1K800 is an ATM/Packet Traffic Manager and Switch device which aggregates, shapes and switches traffic from the S/UNI VORTEX. The S/UNI ATLAS-1K800 performs OAM, policing and address translation functions (see document PMC-1990712, “VORTEX Chip Set Introduction” for details).

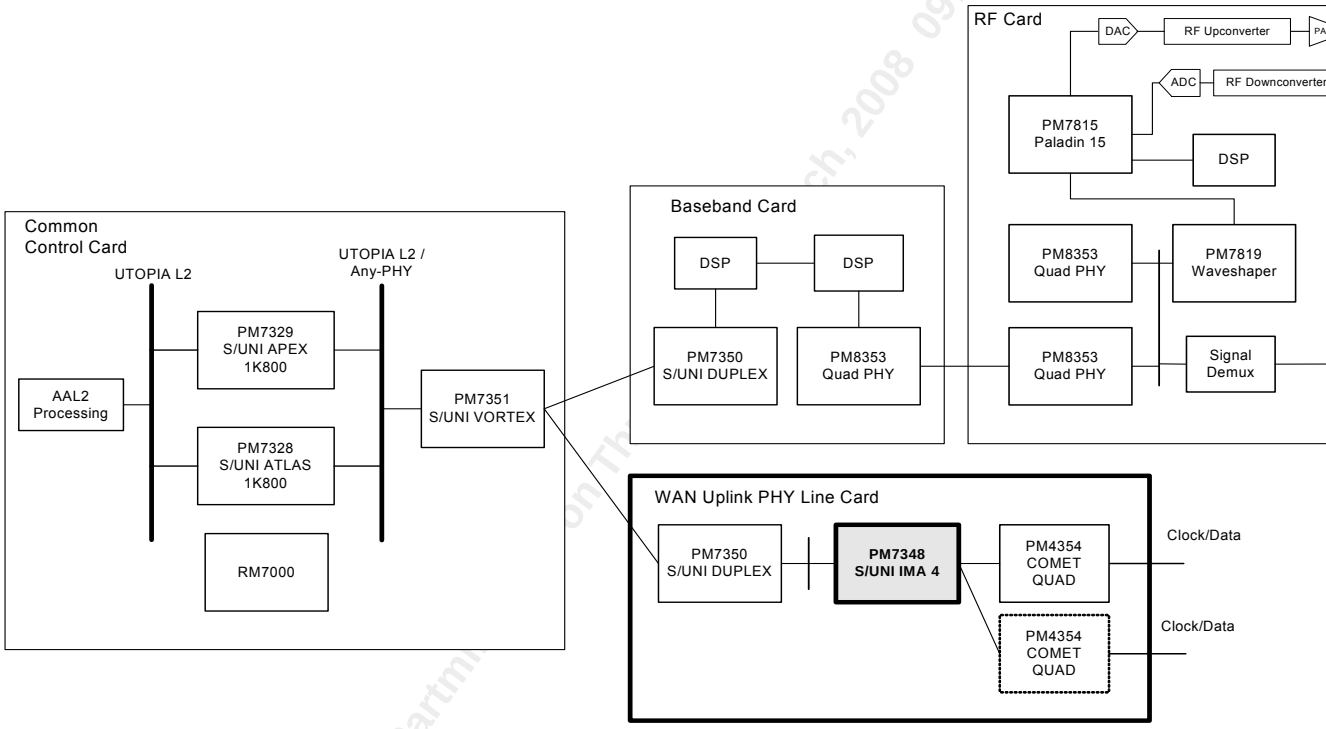
The S/UNI IMA 4 seamlessly interfaces to the Vortex Chipset over a standard UTOPIA Level 2/ Any-PHY bus and the COMET QUAD over a clock and data interface.

4.3 3G Wireless WAN Uplink PHY Line Card

The S/UNI IMA 4 device supports 4 T1/E1 links providing IMA, ATM over T1/E1, and ATM over fractional T1/E1 functionality ideal for 3G Wireless applications as shown in Figure 3. The pin compatible and software compatible S/UNI IMA 8 can upgrade the existing S/UNI IMA 4 to allow a single design to support current and future scalability. Similar to the Remote DSLAM WAN Uplink application, this design is based on the Vortex Chipset used to aggregate the traffic, perform buffering, switching, scheduling, addressing, policing, and OAM functions at OC-3 traffic rates.

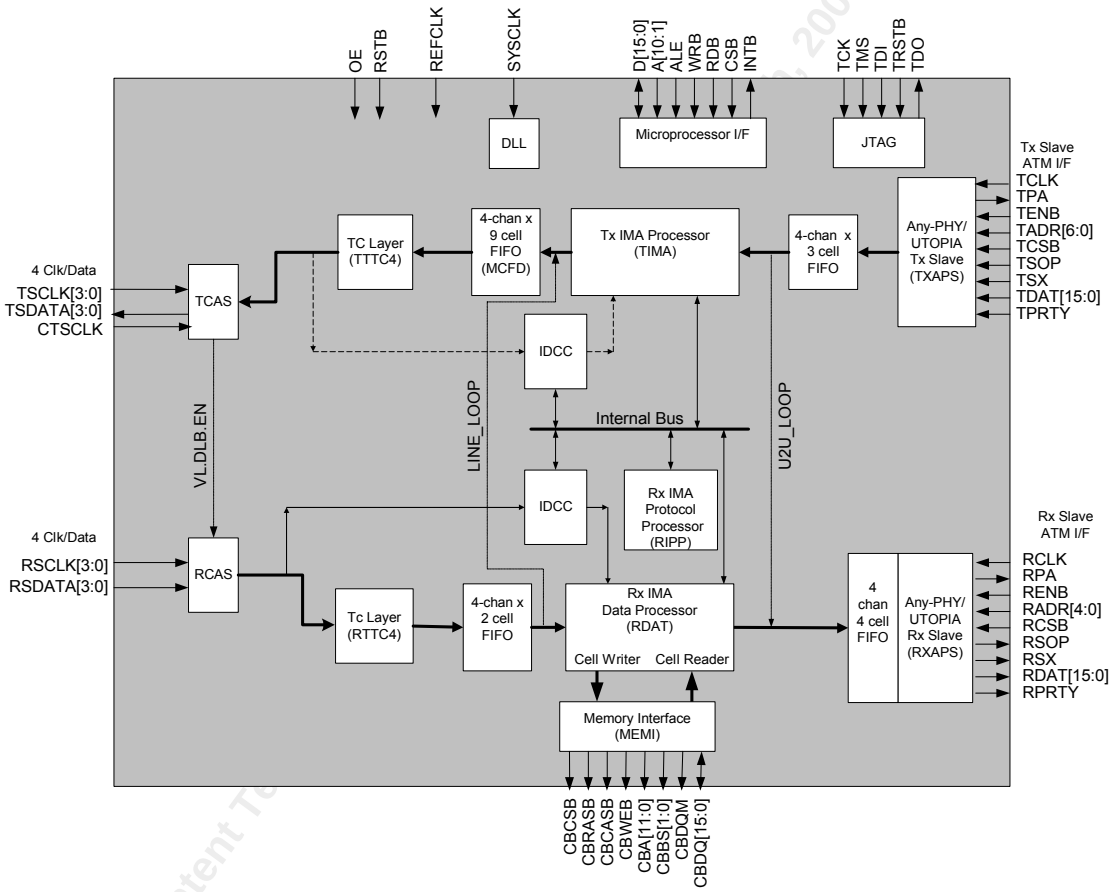
The PM7326 S/UNI APEX device performs the traffic shaping, management, and switching to route cells between the WAN Uplink PHY line card and the Baseband Cards. Additional Common cards are hot swappable using the Vortex backplane architecture, and allow design of a fully redundant, 1:1 protection switching system placing the costly core architecture onto a centralized common card. Between the multiple cards, an embedded inter-card communications channel, and system timing distribution provides for a low cost, high functionality intershelf/intrashef interconnect architecture.

Figure 3 3G Wireless Base Station Controller with IMA WAN PHY Line Card



5 Block Diagram

Figure 4 S/UNI IMA 4 Block Diagram



6 Description

The PM7348 S/UNI IMA 4 is a monolithic integrated circuit that implements the Inverse Multiplexing for ATM (IMA 1.1) with backward compatibility to IMA 1.0 and the Transmission Convergence (TC) layer function. The S/UNI IMA 4 supports 4 independent T1, E1 or unchannelized links. Each link is dynamically configurable to support IMA 1.1, backward compatible IMA 1.0, or ATM HEC cell delineation. ATM over Fractional T1/E1 is also supported. Unchannelized links may be used to support applications such as G.SHDSL or ADSL.

All links within an IMA group must be the same nominal rate as required by the IMA specification, however the link rates within a group can be different across groups.

IMA is a protocol designed to combine the transport bandwidth of multiple links into a single logical link. The logical link is called a group. The S/UNI IMA 4 can support up to 4 independent groups with each group capable of supporting a maximum of all available links. Any link that is not participating in an IMA group can use the cell delineation features of the S/UNI IMA 4 for implementing either ATM over T1/E1 or ATM over xDSL.

In the transmit direction, the S/UNI IMA 4 accepts cells from the Any-PHY/UTOPIA Interface. The S/UNI IMA 4 performs the IMA function that consists of taking a cell stream destined for a group and distributing the cells in a round-robin fashion to the links within a group, adding IMA Control Protocol (ICP) cells, filler cells, and stuff cells as needed. The ICP cells convey state information to the far end and are used to format an IMA frame. The IMA Frame is used as a mechanism to synchronize the links at the far end. Cell rate decoupling is performed at the IMA sub-layer via filler cells. Filler cells are used instead of physical layer cells for cell rate decoupling, thus a continuous stream of cells is sent to the TC layer. The stuff cells are used to maintain synchronization between the links in a group by absorbing the rate differential when links are running on different clocks.

The data from the IMA sub-layer is passed on to the TC layer. In the TC layer, the HEC is calculated and inserted into the cell headers and optional scrambling of the payload is performed. The cell stream is then mapped into the T1 or E1 payload with zeros inserted for the framing and overhead bits or bytes.

The links are then transmitted via the serial interfaces. The clock is provided from each serial clock pin. An optional common-clock mode is provided to enable all links to run from the same clock.

On the receive side, the data is received from the clock/data interface. The TC layer searches for cell delineation as per the procedures outlined in ITU-T Recommendation I.432.1. Once cell delineation is obtained, the payload is optionally descrambled and the cells are passed to the IMA sub-layer. The TC layer provides counts of errored headers as well as OCD and LCD error interrupts.

The receive IMA sublayer performs IMA-frame delineation and stuff-cell removal. Based upon the ICP cell information, the S/UNI IMA 4 determines the differential delay between the links within a group and applies the link and group state machine logic to coordinate the activation and deactivation of groups and links with the far end. As cells are received, they are stored in an external FIFO structure; this structure is based upon the IMA frame boundaries and the IMA frame sequence number. When links or groups are determined to be active by the link and group state machines, the data is played out to the Any-PHY/UTOPIA Interface at a constant rate to mimic the existence of a single higher bandwidth physical link.

Once a group of links is established, links can be added or deleted from the group. Under software control, the S/UNI IMA 4 performs all necessary steps to add or delete links from previously established groups.

To aid diagnostics, a line side loopback and a UTOPIA side loopback are provided. Also, an ICP cell trace feature is provided. When the ICP cell trace is enabled for a group, the S/UNI IMA 4 device places ICP cells into a buffer that is accessible to the microprocessor.

7 Pin Diagram

The S/UNI IMA 4 device is packaged in a 324-pin PBGA package that has a body size of 23 mm by 23 mm and a ball pitch of 1 mm.

Figure 5 S/UNI IMA Pinout (Bottom View)

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VDD	TMS	NC	NC	VDD	D[11]	D[7]	D[5]	D[3]	A[10]	VSS	A[5]	A[2]	RDB	SCANENB	VDDI	NC	NC	NC	NC	NC	NC	A
B	TDAT[0]	TCK	TDI	TDO	D[15]	D[14]	D[10]	D[6]	D[4]	D[0]	A[7]	A[4]	A[1]	CSB	NC	NC	NC	NC	VSS	NC	NC	NC	B
C	TDAT[4]	TDAT[1]	TDAT[6]	VSS	TRSTB	VSS	D[12]	D[9]	VDDI	D[1]	A[8]	VSS	ALE	INTB	NC	NC	NC	NC	NC	VSS	NC	NC	C
D	VSS	TDAT[2]	TPRTY	VSS	D[13]	D[8]	VDD	VSS	D[2]	A[9]	A[6]	VDD	A[3]	WRB	VSS	SCANMODEB	NC	VSS	VDD	VSS	NC	NC	D
E	TDAT[7]	TDAT[5]	TDAT[3]	TCLK															VDDI	NC	NC	VDD	E
F	TDAT[10]	TDAT[8]	VDD	TDAT[13]															TSCLK[2]	NC	VSS	VSS	F
G	TDAT[12]	TDAT[11]	TDAT[9]	VSS															VSS	VSS	VSS	TSCLK[3]	G
H	TSX	TDAT[15]	TDAT[14]	TSOP															NC	TSCLK[0]	CTSCLK	TSCLK[1]	H
J	TADR_SCAN[1]	TADR_SCAN[0]	TCSB	TADR_SCAN[2]					VSS	VSS	VSS	VSS	VSS	VSS					TSDATA[3]	NC	NC	NC	J
K	TADR_SCAN[5]	TADR_SCAN[4]	TADR_SCAN[3]	TADR_SCAN[6]					VSS	VSS	VSS	VSS	VSS	VSS					TSDATA[0]	VSS	TSDATA[2]	TSDATA[1]	K
L	TPA	VSS	TENB	VDD					VSS	VSS	VSS	VSS	VSS	VSS					NC	NC	NC	VDD	L
M	RPRTY	VDDI	RDAT[0]	VSS					VSS	VSS	VSS	VSS	VSS	VSS					VSS	NC	NC	NC	M
N	RDAT[2]	RDAT[3]	RDAT[4]	RDAT[1]					VSS	VSS	VSS	VSS	VSS	VSS					NC	NC	REFCLK	NC	N
P	RDAT[6]	RDAT[7]	RDAT[8]	RDAT[5]					VSS	VSS	VSS	VSS	VSS	VSS					NC	RSCLK[1]	RSCLK[0]	NC	P
R	RDAT[11]	VDD	RDAT[12]	RDAT[9]															VDD	RSDATA[1]	RSDATA[0]	RSCLK[3]	R
T	RDAT[14]	RCLK	RSX	RDAT[10]															RSCLK[2]	VSS	VSS	RSDATA[2]	T
U	RDAT[15]	RCSB	VDDI	RDAT[13]															VDDI	VSS	VSS	RSDATA[3]	U
V	VSS	VSS	RADR[2]	RSOP															VSS	VSS	VDD	VSS	V
W	RADR[0]	VSS	RENB	NC	CBDQ[2]	VDDI	VDD	CBDQ[8]	CBDQ[11]	CBDQ[15]	CBBS[1]	CBA[0]	CBA[2]	CBA[6]	VDD	CBA[10]	CBCASB	NC	VDD	NC	NC	VSS	W
Y	RADR[1]	RADR[3]	VDD	NC	VDD	VSS	CBDQ[3]	CBDQ[6]	VSS	CBDQ[12]	CBDQM	VSS	CBA[5]	CBA[9]	CBWEB	SYSCLK	NC	VDD	NC	NC	NC	VSS	Y
AA	RADR[4]	NC	NC	NC	RSTB	CBDQ[1]	CBDQ[4]	CBDQ[7]	CBDQ[9]	CBDQ[13]	CBBS[0]	VDDI	CBA[4]	CBA[8]	CBA[11]	VSS	NC	NC	NC	VSS	VSS	NC	AA
AB	RPA	VSS	NC	OE	CBDQ[0]	VDD	CBDQ[5]	VSS	CBDQ[10]	CBDQ[14]	VSS	CBA[1]	CBA[3]	CBA[7]	VSS	CBRASB	CBCSB	NC	NC	NC	NC	NC	AB
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

8 Pin Description

8.1 Receive Slave ATM Interface (Any-PHY mode) (28 Signals)

Pin Name	Type	Pin No.	Function
RCLK	Input	T21	The **Receive Clock** (RCLK) signal transfers data blocks from the S/UNI IMA 4 across the receive Any-PHY interface. The RPA, RSOP, RSX, RDAT[15:0], and RPRTY outputs are updated on the rising edge of RCLK. The RENB, RADR[4:0], and RCSB inputs are sampled on the rising edge of RCLK. The RCLK input must cycle at a 52 MHz or lower instantaneous rate.
RPA	Tristate Output	AB22	The **Receive Packet Available** (RPA) is an active high signal that indicates if at least one cell is queued for transfer. The S/UNI IMA 4 device drives the RPA with the cell availability status two RCLK cycles after RADR[4:0] matches the S/UNI IMA device's address. The RPA output is high-impedance at all other times. The RPA output is updated on the rising edge of RCLK.
RENB	Input	W20	The **Receive Enable Bar** (RENB) is an active low signal used to initiate the transfer of cells from the S/UNI IMA 4 to an ATM layer component, such as a traffic management device. The RENB input is sampled on the rising edge of RCLK.
RADR[4] RADR[3] RADR[2] RADR[1] RADR[0]	Input	AA22 Y21 V20 Y22 W22	The **Receive Address** (RADR[4:0]) signals are used to address the S/UNI IMA 4 device for the purposes of polling and selection for cell transfer. The RADR[4:0] signals are valid only when the RCSB signal is sampled active in the following RCLK cycle. The RADR[4:0] input bus is sampled on the rising edge of RCLK.
RCSB	Input	U21	The **Receive Chip Select** (RCSB) is an active low signal that selects the S/UNI IMA 4 receive interface. When the RCSB is sampled low, it indicates that the RADR[4:0] sampled at the previous clock is a valid address. If the RCSB is sampled high, the device is not selected and the RADR[4:0] sampled on the previous cycle is not a valid address and is ignored. When sufficient address space is provided by RADR[4:0] for all devices on the bus, this signal may be tied low. The RCSB input is sampled on the rising edge of RCLK.
RSOP	Tristate Output	V19	The **Receive Start of Packet** (RSOP) is an active high signal that marks the start of the cell on the RDAT[15:0] bus. When RSOP is active, the first word of the cell is present on the RDAT[15:0] bus. The RSOP output is updated on the rising edge of RCLK.
RSX	Tristate Output	T20	The **Receive Start of Transfer** (RSX) signal is an active high signal that marks the first cycle of a data block transfer on the RDAT[15:0] bus. When the RSX signal is active, the coinciding data on the RDAT[15:0] bus represents the in-band PHY address. The RSX output is updated on the rising edge of RCLK.

Pin Name	Type	Pin No.	Function
RDAT[15] RDAT[14 RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Tristate Output	U22 T22 U19 R20 R22 T19 R19 P20 P21 P22 P19 N20 N21 N22 N19 M20	The **Receive Cell Data** (RDAT[15:0]) signals carry the ATM cell words that are read from the S/UNI IMA 4 internal cell buffers. When this interface is operating in 8-bit mode, the data is carried on RDAT[7:0]. The RDAT[15:0] output bus is updated on the rising edge of RCLK.
RPRTY	Tristate Output	M22	The **Receive Parity** (RPRTY) signal provides the parity (programmable for odd or even parity) of the RDAT[15:0] bus. When the interface is operating in 8-bit mode, the parity is calculated over RDAT[7:0] The RPRTY output is updated on the rising edge of RCLK.

8.2 Receive Slave ATM Interface (UTOPIA L2 mode) (26 Signals)

Pin Name	Type	Pin No.	Function
RCLK	Input	T21	The **Receive Clock** (RCLK) signal transfers data blocks from the S/UNI IMA 4 across the receive UTOPIA L2 interface. The RCA, RSOC, RDAT[15:0], and RPRTY outputs are updated on the rising edge of RCLK. The RENB and RADR[4:0] inputs are sampled on the rising edge of RCLK. The RCLK input must cycle at a 52 MHz or lower instantaneous rate.
RCA	Tristate Output	AB22	The **Receive Cell Available** (RCA) is an active high signal that, when polled using the RADR[4:0] signals, indicates if at least one cell is queued for transfer on the selected logical channel FIFO . The S/UNI IMA 4 device drives RCA with the cell availability status for the polled port one RCLK cycle after a valid RADR[4:0] address is sampled. The RCA output is high-impedance at all other times. The RCA output is updated on the rising edge of RCLK.
RENB	Input	W20	The **Receive Enable Bar** (RENB) is an active low signal used to initiate the transfer of cells from the S/UNI IMA 4 to an ATM-layer component, such as a traffic management device. The RENB input is sampled on the rising edge of RCLK.
RADR[4] RADR[3] RADR[2] RADR[1] RADR[0]	Input	AA22 Y21 V20 Y22 W22	The **Receive Address** (RADR[4:0]) signals are used to address the S/UNI IMA 4 device for the purposes of polling and selecting for cell transfer. The RADR[4:0] input bus is sampled on the rising edge of RCLK.

Pin Name	Type	Pin No.	Function
RSOC	Tristate Output	V19	The **Receive Start of Cell** (RSOC) is an active high signal that marks the first word of the cell on the RDAT[15:0] bus. The RSOC output is updated on the rising edge of RCLK.
RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Tristate Output	U22 T22 U19 R20 R22 T19 R19 P20 P21 P22 P19 N20 N21 N22 N19 M20	The **Receive Cell Data** (RDAT[15:0]) signals carry the ATM cell words that are read from the S/UNI IMA 4 internal cell buffers. When this interface is operating in 8-bit mode, the data is carried on RDAT[7:0]. The RDAT[15:0] output bus is updated on the rising edge of RCLK.
RPRTY	Tristate Output	M22	The **Receive Parity** (RPRTY) signal provides the parity (programmable for odd or even parity) of the RDAT[15:0] bus. When the interface is operating in 8-bit mode, the parity is calculated over RDAT[7:0] The RPRTY output is updated on the rising edge of RCLK.

8.3 Transmit Slave Interface (ANY-PHY mode) (30 Signals)

Pin Name	Type	Pin No.	Function
TCLK	Input	E19	The **Transmit Clock** (TCLK) signal transfers cells across the ANY-PHY interface to the internal downstream cell buffers. The TPA output is updated on the rising edge of TCLK. The TENB. TSX, TSOP, TDAT[15:0], TPRTY, TADR[6:0], and TCSB inputs are sampled on the rising edge of TCLK. The TCLK input must cycle at a 52 MHz or lower instantaneous rate.
TPA	Tristate Output	L22	The **Transmit Packet Available** (TPA) is an active high signal that indicates the availability of space in the selected logical channel FIFO when polled using the TADR[6:0] signals. The S/UNI IMA 4 device drives TPA with the cell availability status of the polled port two TCLK cycles after TADR[6:0] matches the S/UNI IMA's device address. The TPA output is high-impedance at all other times. The TPA output is updated on the rising edge of TCLK.
TENB	Input	L20	The **Transmit enable bar** (TENB) is an active low signal that indicates cell transfers to the internal cell buffers. The TENB input is sampled on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TADR[6] TADR[5] TADR[4] TADR[3] TADR[2] TADR[1] TADR[0]	Input	K19 K22 K21 K20 J19 J22 J21	The **Transmit Address** (TADR[6:0]) signals are used to address logical channels for the purpose of polling and device selection. The TADR[6:0] signals are valid only when the TCSB signal is sampled active in the following TCLK cycle. The TADR[6:0] input bus is sampled on the rising edge of TCLK.
TCSB	Input	J20	The **Transmit Chip Select** (TCSB) is an active low signal that selects the S/UNI IMA 4 device's transmit interface. When the TCSB is sampled low, it indicates that the TADR[6:0] sampled at the previous clock is a valid address. If the TCSB is sampled high, the device is not selected and the TADR[6:0] sampled on the previous cycle is not a valid address and is ignored. When sufficient address space is provided by TADR[6:0] for all devices on the bus, this signal may be tied low. The TCSB is asserted low one cycle after a valid address is present on the TADR[6:0] signals. The TCSB input is sampled on the rising edge of TCLK.
TSOP	Input	H19	The **Transmit Start of Packet** (TSOP) is an active high signal that marks the start of the cell on the TDAT[15:0] bus. When TSOP is active, the first word of the cell is present on the TDAT[15:0] bus. The TSOP output is sampled on the rising edge of TCLK.
TSX	Input	H22	The **Transmit Start of Transfer** (TSX) signal is an active high signal that marks the first cycle of a data-block transfer on the TDAT[15:0] bus. When the TSX signal is active, the coinciding data on the TDAT[15:0] bus represents the in-band PHY address. The TSX output is sampled on the rising edge of TCLK.
TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	H21 H20 F19 G22 G21 F22 G20 F21 E22 C20 E21 C22 E20 D21 C21 B22	The **Transmit Cell Data** (TDAT[15:0]) signals carry the ATM cell octets that are transferred to the internal cell buffer. When this interface is operating in 8-bit mode, only TDAT[7:0] is used. The TDAT[15:0] input bus is sampled on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TPRTY	Input	D20	The **Transmit Parity** (TPRTY) signal provides the parity (programmable for odd or even parity) of the TDAT[15:0] bus. The TPRTY signal is considered valid only when valid data and inband address are transferring as indicated by the TENB signal asserted low or the TSX signal asserted high. When this interface is operating in 8-bit mode, this signal provides the parity of TDAT[7:0]. A parity error is indicated by a status bit and a maskable interrupt. The TPRTY input signal is sampled on the rising edge of TCLK.

8.4 Transmit Slave Interface (UTOPIA L2 mode) (26 Signals)

Pin Name	Type	Pin No.	Function
TCLK	Input	E19	The **Transmit Clock** (TCLK) signal transfers cells across the ANY-PHY interface to the internal downstream cell buffers. The TCA output is updated on the rising edge of TCLK. The TENB, TSOC, TDAT[15:0], TPRTY, TADR[4:0] inputs are sampled on the rising edge of TCLK. The TCLK input must cycle at a 52 MHz or lower instantaneous rate.
TCA	Tristate Output	L22	The **Transmit Cell Available** (TCA) is an active high signal that indicates the availability of space in the selected logical channel FIFO when polled using the TADR[4:0] signals. The S/UNI IMA 4 drives TCA with the cell space availability status for the polled port on TCLK cycles after a valid TADR[4:0] address is sampled. The TCA output is high-impedance when not polled. The TCA output is updated on the rising edge of TCLK.
TENB	Input	L20	The **Transmit enable bar** (TENB) is an active low signal that indicates cell transfers to the internal cell buffers. The TENB input is sampled on the rising edge of TCLK.
TADR[4] TADR[3] TADR[2] TADR[1] TADR[0]	Input	K21 K20 J19 J22 J21	The **Transmit Address** (TADR[4:0]) signals are used to address logical channels for the purposes of polling and device selection. The TADR[4:0] input bus is sampled on the rising edge of TCLK.
TSOC	Input	H19	The **Transmit Start of Cell** (TSOC) is an active high signal that marks the first word of the cell on the TDAT[15:0] bus. The TSOC input is sampled on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	H21 H20 F19 G22 G21 F22 G20 F21 E22 C20 E21 C22 E20 D21 C21 B22	The **Transmit Cell Data** (TDAT[15:0]) signals carry the ATM cell octets that are transferred to the internal cell buffer. The TDAT[15:0] signals are considered valid only when the TENB signal is asserted low. When this interface is operating in 8-bit mode, only TDAT[7:0] is used. The TDAT[15:0] input bus is sampled on the rising edge of TCLK.
TPRTY	Input	D20	The **Transmit Parity** (TPRTY) signal provides the parity (programmable for odd or even parity) of the TDAT[15:0] bus. The TPRTY signal is considered valid only when valid data is transferring as indicated by the TENB signal asserted low. When this interface is operating in 8-bit mode, this signal provides the parity of TDAT[7:0]. A parity error is indicated by a status bit and a maskable interrupt. The TPRTY input signal is sampled on the rising edge of TCLK.

8.5 Microprocessor Interface (31 Signals)

Pin Name	Type	Pin No.	Function
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	B18 B17 D18 C16 A17 B16 C15 D17 A16 B15 A15 B14 A14 D14 C13 B13	The **Micro Data** (D[15:0]) signals provide a data bus to allow the S/UNI IMA 4 device to interface to an external microprocessor. Both read and write transactions are supported. The microprocessor interface configures and monitors the S/UNI IMA 4 device.

Pin Name	Type	Pin No.	Function
A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1]	Input	A13 D13 C12 B12 D12 A11 B11 D10 A10 B10	The **Micro Address** (A[10:1]) signals provide an address bus to allow the S/UNI IMA 4 device to interface to an external microprocessor. The A[10:1] indicate a word address. The S/UNI IMA 4 microprocessor interface is not byte addressable. The A[10:1] input signals are sampled while the ALE is asserted high.
ALE	Input	C10	The **Address Latch Enable** (ALE) is an active high signal that latches the A[10:1] signals during the address phase of a bus transaction. When ALE is set high, the address latches are transparent. When ALE is set low, the address latches hold the address provided on A[10:1]. The ALE input has an internal pull-up resistor.
WRB	Input	D9	The **Write Strobe Bar** (WRB) is an active low signal that qualifies write accesses to the S/UNI IMA 4 device. When the CSB is set low, the D[15:0] bus contents are clocked into the addressed register on the rising edge of WRB.
RDB	Input	A9	The **Read Strobe Bar** (RDB) is an active low signal that qualifies read accesses to the S/UNI IMA 4 device. When the CSB is set low, the S/UNI IMA 4 device drives the D[15:0] bus with the contents of the addressed register on the falling edge of RDB.
CSB	Input	B9	The **Chip Select Bar** (CSB) is an active low signal that qualifies read/write accesses to the S/UNI IMA 4 device. The CSB signal must be set low during read and write accesses. When the CSB is set high, the microprocessor-interface signals are ignored by the S/UNI IMA 4 device. If the CSB is not required (register accesses are controlled only by WRB and RDB), then it should be connected to an inverted version of the RSTB signal.
INTB	Open-Drain Output	C9	The **Interrupt Bar** (INTB) is an active low signal indicating that an enabled bit in the Master Interrupt Register was set. When INTB is set low, the interrupt is active and enabled. When INTB is tristate, there is no interrupt pending or it is disabled.

8.6 SDRAM I/F (33 Signals)

Pin Name	Type	Pin No.	Function
CBCSB	Output	AB6	The **Cell Buffer SDRAM Chip Select Bar** (CBCSB) is an active low signal used to control the SDRAM. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. The CBCSB output is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
CBRASB	Output	AB7	The **Cell Buffer SDRAM Row Address Strobe Bar** (CBRASB) is an active low signal used to control the SDRAM. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. The CBRASB output is updated on the rising edge of SYSCLK.
CBCASB	Output	W6	The **Cell Buffer SDRAM Column Address Strobe Bar** (CBCASB) is an active low signal used to control the SDRAM. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. The CBCASB output is updated on the rising edge of SYSCLK.
CBWEB	Output	Y8	The **Cell Buffer SDRAM Write Enable Bar** (CBWEB) is an active low signal used to control the SDRAM. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. The CBWEB output is updated on the rising edge of SYSCLK.
CBA[10] CBA[9] CBA[8] CBA[7] CBA[6] CBA[5] CBA[4] CBA[3] CBA[2] CBA[1] CBA[0]	Output	W7 Y9 AA9 AB9 W9 Y10 AA10 AB10 W10 AB11 W11	The **Cell Buffer SDRAM Address** (CBA[10:0]) signals identify the row address (CBA[10:0]) and column address (CBA[7:0]) for the locations accessed. The CBA[10:0] output is updated on the rising edge of SYSCLK.
CBBS	Output	AA12	The **Cell Buffer SDRAM Bank Select** (CBBS) signals determine which bank of a dual/quad bank Cell Buffer SDRAM chip is active. CBBS is generated along with the row address when CBRASB is asserted low. The CBBS outputs are updated on the rising edge of SYSCLK.
CBDQM	Output	Y12	The **Cell Buffer SDRAM Input/Output Data Mask** (CBDQM) signal is held high until the SDRAM initialization is complete and then set low for normal operation. The CBDQM output is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
CBDQ[15] CBDQ[14] CBDQ[13] CBDQ[12] CBDQ[11] CBDQ[10] CBDQ[9] CBDQ[8] CBDQ[7] CBDQ[6] CBDQ[5] CBDQ[4] CBDQ[3] CBDQ[2] CBDQ[1] CBDQ[0]	I/O	W13 AB13 AA13 Y13 W14 AB14 AA14 W15 AA15 Y15 AB16 AA16 Y16 W18 AA17 AB18	The **Cell Buffer SDRAM Data** (CBDQ[15:0]) signals interface directly with the Cell Buffer SDRAM data ports. The CBDQ[15:0] bi-directional signals are sampled and updated/tristated on the rising edge of SYSCLK.

8.7 Clk/Data (17 signals)

Pin Name	Type	Pin No.	Function
TSCLK[3] TSCLK[2] TSCLK[1] TSCLK[0]	Input	G1 F4 H1 H3	The **Transmit Serial Clock** (TSCLK[3:0]) signals contain the transmit clocks for the 4 independently timed links. The TSDATA[3:0] signals are updated on the falling edge of the corresponding TSCLK[3:0] clock. For channelized T1 or E1 links, TSCLK[n] must be gapped during the framing bit (for T1 interfaces) or during time-slot 0 (for E1 interfaces) of the TSDATA[n] stream. The S/UNI IMA 4 uses the gapping information to determine the time-slot alignment in the transmit stream. For unchannelized links, TSCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e., not part of the ATM Cell). The TSCLK[3:0] input signal is nominally a 50% duty cycle clock of 1.544 MHz for T1 links and 2.048 MHz for E1 links. The TSCLK[3:0] may operate at higher rates in the unchannelized mode. At higher rates, the amount of lines available is limited. See section 12.3.1 for more details.

Pin Name	Type	Pin No.	Function
TSDATA[3] TSDATA[2] TSDATA[1] TSDATA[0]	Output	J4 K2 K1 K4	The **Transmit Serial Data** (TSDATA[3:0]) signals contain the transmit data for the 4 independently timed links. For channelized links, TSDATA[n] contains the 24 (T1) or 31 (E1) time-slots that comprise the channelized link. TSCLK[n] must be gapped during the T1 framing bit position or the E1 frame alignment signal (time-slot 0). The S/UNI IMA 4 uses the location of the gap to determine the channel alignment on TSDATA[n]. For unchannelized links, TSDATA[n] contains the ATM cell data. For certain transmission formats, TSDATA[n] may contain place holder bits or time-slots. TSCLK[n] must be externally gapped during the placeholder positions in the TSDATA[n] stream. The TSDATA[3:0] output signals are updated on the falling edge of the corresponding TSCLK[3:0] clock, or on the falling edge of the CTSCLK when the CTSCLK_SEL is set.
RSCLK[3] RSCLK[2] RSCLK[1] RSCLK[0]	Input	R1 T4 P3 P2	The **Receive Serial Clock** (RSCLK[3:0]) signals contain the recovered line clock for the 4 independently timed links. The RSDATA[3:0] signals are sampled on the rising edge of the corresponding RSCLK[3:0] clock. For channelized T1 or E1 links, RSCLK[n] must be gapped during the framing bit (for T1 interfaces) or during time-slot 0 (for E1 interfaces) of the RSDATA[n] stream. The S/UNI IMA 4 device uses the gapping information to determine the time-slot alignment in the receive stream. RSCLK[3:0] is nominally a 50% duty cycle clock of 1.544 MHz for T1 links and 2.048 MHz for E1 links. For unchannelized links, RSCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e., not part of the ATM cell). The RSCLK[3:0] input signal is nominally a 50% duty cycle clock of 1.544 MHz for T1 links and 2.048 MHz for E1 links. The RSCLK[3:0] may operate at higher rates in the unchannelized mode. At higher rates, the amount of lines available is limited See section 12.3.1 for more details.
RSDATA[3] RSDATA[2] RSDATA[1] RSDATA[0]	Input	U1 T1 R3 R2	The **Receive Serial Data** (RSDATA[3:0]) signals contain the recovered line data for the 4 independently timed links. For channelized links, RSDATA[n] contains the 24 (T1) or 31 (E1) time-slots that comprise the channelized link. RSCLK[n] must be gapped during the T1 framing bit position or the E1 frame alignment signal (time-slot 0). The S/UNI IMA 4 uses the location of the gap to determine the channel alignment on RSDATA[n]. For unchannelized links, RSDATA[n] contains the ATM cell data. For certain transmission formats, RSDATA[n] may contain place-holder bits or time-slots. RSCLK[n] must be externally gapped during the place-holder positions in the RSDATA[n] stream. The RSDATA[3:0] input signals are sampled on the rising edge of the corresponding RSCLK[3:0] clock.

Pin Name	Type	Pin No.	Function
CTSCLK	Input	H2	The **Common Transmit Serial Clock** (CTSCLK) signal is a common transmit line clock that can optionally be used by all 4 serial links instead of each link's transmit serial line clock (TSCLK[n]). Ground if not used. The CTSCLK input signal is nominally a 50% duty cycle clock of 1.544 MHz for T1 links and 2.048 MHz for E1 links.

8.8 General (71 signals)

Pin Name	Type	Pin No.	Function
RSTB	Input	AA18	The **Reset Bar** (RSTB) is an active low signal that provides an asynchronous S/UNI IMA 4 reset. RSTB is a Schmitt-triggered input with an internal pull-up resistor.
OE	Input	AB19	The **Output Enable** (OE) is an active high signal that allows all of the outputs of the device to operate in their functional state. When this signal is low, all outputs of the S/UNI IMA 4 go to the high impedance state, with the exception of TDO**.**
SYSCLK	Input	Y7	The **System Clock** (SYSCLK) signal is the master clock for the S/UNI IMA 4 device. The core S/UNI IMA 4 logic (including the SDRAM interface) is timed to this signal. External SDRAM devices share this clock and must have clocks aligned within 0.2ns skew of the clock seen by the S/UNI IMA 4 device. This clock must be stable prior to deasserting RSTB 0->1.
REFCLK	Input	N2	The **Reference Clock** (REFCLK) signal is an externally generated clock with a nominal 50% duty cycle. In CLK/Data mode, REFCLK is required and may be operated at frequencies up to 52 MHz. In general, for T1 and E1 links, 33 MHz is sufficient. See section 12.3.1 for details on selecting the proper frequency.
NC		M2 N1 N3 P4 P1 L4 B2 A1 C2 B1 D2 E3 C1 D1 E2 F3 L3 L2 M1 M3 N4 W2 Y2 AA1 W3 AB1 Y4 AB2 AA4 AB3 AB4 AA5 Y6 Y3 AB5 AA6 W5 W19 AB20 AA19	**No Connect.** Do not connect this pin.

Pin Name	Type	Pin No.	Function
		AA20 Y19 AA21 A20 A19 B8 C8 B7 A6 D6 C7 B6 A5 C6 B5 A4 C5 A2 A3 B3 C4 W12 AA8 H4 J3 J2 J1	

8.9 JTAG & Scan Interface (7 Signals)

Pin Name	Type	Pin No.	Function
TCK	Input	B21	The **Test Clock** (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	A21	The **Test Mode Select** (TMS) is an active high signal that controls the test operations carried out using the IEEE P1149.1 test access port. The TMS signal has an internal pull-up resistor. The TMS input is sampled on the rising edge of TCK.
TDI	Input	B20	The **Test Data Input** (TDI) signal carries test data into the S/UNI IMA 4 via the IEEE P1149.1 test access port. The TDI signal has an internal pull-up resistor. The TDI input is sampled on the rising edge of TCK.
TDO	Tristate	B19	The **Test Data Output** (TDO) signal carries test data out of the S/UNI IMA 4 via the IEEE P1149.1 test access port. TDO is a tristate output that is inactive except when the scanning of data is in progress. The TDO output is updated/tristated on the falling edge of TCK.
TRSTB	Input	C18	The **Active low Test Reset** (TRSTB) is an active low signal that provides an asynchronous S/UNI IMA 4 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt-triggered input with an internal pull-up resistor. Note that when not being used, TRSTB must be connected to the RSTB input.
SCAN_MODEB	Input	D7	The **Active low Scan Mode** (SCAN_MODEB) is an active low signal that places the S/UNI IMA 4 into a manufacturing test mode. Must be tied high to disable the scan logic.
SCANENB	Input	A8	The **Active low Scan Enable (**SCANENB) is an active low signal that enables the internal scan logic for production testing. Must be tied high to disable the scan logic.

8.10 Power (120 Signals)

Pin Name	Type	Pin No.	Function
VDDI (1.8 V)	Power	E4 U4 AA11 W17 U20 M21 C14 A7	The core power pins (VDDI[7:0]) should be connected to a well-decoupled +1.8 V DC supply.
VSS (VSSI, VSSO, VSSQ)	Ground	A12 AA2 AA3 AA7 AB12 AB15 AB21 AB8 B4 C11 C17 C19 C3 D3 D15 D19 D22 D5 D8 F1 F2 G2 G3 G19 G4 J9 J10 J11 J12 J13 J14 K3 K9 K10 K11 K12 K13 K14 L9 L10 L11 L12 L13 L14 L21 M4 M9 M10 M11 M12 M13 M14 M19 N9 N10 N11 N12 N13 N14 P9 P10 P11 P12 P13 P14 T2 U2 U3 V1 V3 V4 T3 V21 V22 W1 W21 Y1 Y11 Y14 Y17	**VSS** The VSS pins should be connected to GND. VSSO pins are ground pins for ports. VSSQ pins are “quiet” ground pins for ports. VSSI pins are core ground pins. All grounds should be connected together.

Pin Name	Type	Pin No.	Function
VDD (3.3V)	Power	A18 A22 AB17 D11 D16 D4 E1 F20 L1 L19 R21 R4 V2 W16 W4 W8 Y18 Y20 Y5	VDD (3.3V) The I/O power pins (VDD) should be connected to a well-decoupled +3.3 V DC supply. These pins include the VDDO pins for the switching, as well as the VDDQ for the quiet power pins.

Notes on Pin Description:

1. All S/UNI IMA 4 I/O present minimum capacitive loading and operate at TTL logic levels and can tolerate 5.0V levels.
2. Inputs RSTB, ALE, TCK, TMS, TDI and TRSTB, TSCLK, CTSCLK, RSCLK, RSDATA, and OE have internal pull-up resistors.
3. All outputs and bi-directional signals have 6mA drive capability, except for the following, which have a 4mA drive capability: CBCSB, CBRASB, CBCASB, CBWEB, CBA[10:0], CBBS, CBDQM, CBDQ[15:0], TDO.
4. Power to the VDD (3.3V) pins should be applied *before* power to the VDDI (1.8V) pins is applied. Similarly, power to the VDDI (1.8V) pins should be removed *before* power to the VDD (3.3V) pins is removed.

9 Functional Description

This section describes the function of each entity in the S/UNI IMA 4 block diagram. Throughout this document the use of the term “transmit” implies data read in from the cell interface and sent out the line side interface. Conversely, “receive” describes the data path from the line side interface to the cell interface.

The term “virtual PHY” refers to a single flow on the Any-PHY/UTOPIA bus. Each IMA group or a single TC connection is mapped to a virtual PHY. For simplicity, both an IMA group and a TC connection are referenced as a group.

Each IMA group can map data to/from multiple links. Each TC group is mapped to a single link.

The term “link” refers to a single T1/E1 link or unchannelized link on the clock/data interface. When supporting fractional T1/E1 via the Clock/Data interface, the timeslots that are chosen to be part of the fractional connection are also referred to as a link.

Within the clock/data interface, the external links are mapped to a contiguous space identified as Virtual Links. To support multiple fractional TC flows on a single external signal, a mapping splits a single channelized external signal into multiple Virtual Links. At the per-link FIFOs, the clock/data Virtual Link naming convention is used synonymously with the Physical Link naming convention.

9.1 Any-PHY/UTOPIA Interfaces

The ATM cell interfaces are Any-PHY compliant 8/16 bit slave interfaces that are compatible with the following options:

- Any-PHY Slave.
- UTOPIA Level 2, 4-port slave (multi-PHY-mode).
- UTOPIA Level 2, single port slave (single address mode) for receive side only.

9.1.1 Transmit Any-PHY/UTOPIA Slave (TXAPS)

In the transmit direction, each S/UNI IMA 4 receives cells on the Any-PHY/UTOPIA L2 compatible interface operating at clock rates up to 52 MHz and supporting 16-bit and 8-bit wide cells. The S/UNI IMA 4 operates as a bus slave only.

Cell transfers are cell-based, that is, an entire cell is transferred from one PHY device before another is selected. Polling occurs concurrently with cell transfers to ensure maximum throughput. Data pausing is not supported in Any-PHY mode. If the TENB is deasserted prior to a complete cell being transferred, the cell transfer error interrupt is triggered.

UTOPIA Level 2 Multi-Address Slave Mode

In the UTOPIA Level 2 Multi-address Slave mode, the transmit interface of the S/UNI IMA 4 appears as a 4 port multi-PHY. An 11-bit configuration register TCAEN (only 4 bits are used in UL2 mode) controls the response to polling the individual channels within this group of 31 ports. Setting high on TCAEN[0] enables addresses 0 through 7 and TCAEN[3] enables addresses 24 through 30. This typically lets more than one slave device share the Transmit Any-PHY/UTOPIA master bus.

Each FIFO only asserts TCA when polled (using TADR) if it is not in the process of transferring a cell and if there is room in the FIFO for a complete cell. Unlike Any-PHY, in UTOPIA Mode the virtual PHY port must first be selected prior to the start of the data transfer. This selection is done using the same address lines that are used for polling in combination with the TENB pin.

Any-PHY Slave Mode

In the Any-PHY slave mode, the transmit interface of the S/UNI IMA 4 device appears as a multi-PHY device with 4 ports used for the data path where all ports are identified in the in-band address. The configuration register TCAEN controls the response to polling the individual channels within this group of 4 ports. Setting high on TCAEN[0] enables any group of four ports within the addresses 0 through 7, and TCAEN[3] enables any group of four ports within the addresses 24 through 31. This is typically used to allow more than one slave device to share the Transmit Any-PHY/UTOPIA master bus.

Conceptually, the Any-PHY protocol can be divided into two processes: polling and cell transfer.

Polling in the transmit direction is used by the bus master – typically a traffic buffering and management device – to determine when a buffered data cell can be safely sent to a PHY. The S/UNI IMA 4 device provides an independent three-deep cell buffer FIFO for each virtual PHY. In total, there are 4 FIFOs. This arrangement ensures that there is no head-of-line blocking, while providing latitude to the master for servicing high data rate ports as well as low data rate ports.

The traffic manager need only poll those virtual PHYs for which it has cells queued. A cell transfer can be initiated after a polled virtual PHY asserts the TPA output. Each virtual PHY's cell buffer availability status (i.e., the status that is driven onto the TPA output when the virtual PHY is polled) is deasserted when the first byte of the last cell is written into the buffer. It is re-asserted only when the FIFO can accept another complete cell.

In Any-PHY mode, polling is performed using the TADR[6:0] bus in conjunction with the TCSB. Each S/UNI IMA 4 device uses the TADR[2:0] bits to indicate the 4 logical virtual PHY's (the other 4 within this range are unused). The upper bits from the TADR bus, TADR[6:3], are compared to the configured address to select the device. The remaining address bits from the traffic manager are decoded externally and are used to drive the TCSB. The address prepend field in the cell transfer contains the entire 16-bit address. In 8-bit mode, the prepend address is reduced to 8-bits.

In Any-PHY mode, the cell transfer is initiated after a successful poll. The virtual PHY address is prepended to the cell, thus performing an inband selection. The S/UNI IMA 4 device monitors the address prepend on the cell transfer to detect its cells.

For Any-PHY mode, if a second TSX is asserted prior to a complete cell being transferred, the cell transfer error interrupt is triggered. This indicates that a runt cell was transferred to the S/UNI IMA 4 device. This is an Any-PHY protocol violation. Also this interrupt signal is triggered if the TENB is deasserted prior to a complete cell is transferred since pausing is not supported in Any-PHY mode.

Transmit Cell Transfer Format

The Transmit Cell Transfer Format is shown in Figure 6 and Figure 7. Word/byte 0 is required for cell transfers to an Any-PHY slave. The address prepend is the S/UNI IMA 4 virtual PHY ID. The virtual PHY ID can be mapped to a TC link or to an IMA group. Optional prepends are supported, but are ignored by the S/UNI IMA 4.

Inclusion of optional words is statically configurable for the interface. The optional words are ignored.

Figure 6 16-bit Transmit Cell Transfer Format

	Bits 15-8	Bits 7-0
Word 0 (Any-PHY only)	**Address Prepend**	
Word 1 (Optional)	**Optional Prepend**	
Word 2	**H1**	**H2**
Word 3	**H3**	**H4**
Word 4	**HEC/UDF**	
Word 5	**PAYLOAD1**	**PAYLOAD2**
Word 6	**PAYLOAD3**	**PAYLOAD4**
	•	•
	•	•
	•	•
Word 28	**PAYLOAD47**	**PAYLOAD48**

Figure 7 8-bit Transmit Cell Transfer Format

	Bits 7-0
Byte 0 (Any-PHY only)	**Address Prepend**

Byte 1 (Optional)	**Optional Prepend[15:8]**
Byte 2 (Optional)	**Optional Prepend[7:0]**
Byte 3	**H1**
Byte 4	**H2**
Byte 5	**H3**
Byte 6	**H4**
Byte 7*	**HEC**
Byte 8	**PAYLOAD1**
	•
	•
	•
Byte 55	**PAYLOAD48**

9.1.2 Receive Any-PHY/UTOPIA Slave (RXAPS)

In the receive direction, each S/UNI IMA 4 transmits cells on an Any-PHY/UTOPIA L2 compatible interface operating at clock rates up to 52 MHz and supporting 16-bit and 8-bit wide cells. The S/UNI IMA 4 operates as a bus slave.

In all modes, an optional prepend is allowed on the bus. This prepend is set to zero and has no significance to the S/UNI IMA 4 but is provided for interoperability.

UTOPIA Level 2 Multi-Address Slave Mode

In UTOPIA Level 2 Multi-Address Slave mode, the S/UNI IMA 4 operates as a 4 port multi-PHY with each virtual PHY stored in its own FIFO. A 4-bit configuration register, RCAEN, controls the response to polling the individual channels within this group of 4 ports. Setting RCAEN[0] enables any group of four ports within the addresses 0 through 7, and RCAEN[3] enables any group of four ports within the addresses 24 through 30. This is typically used to allow more than one slave device to share the Receive UTOPIA master bus. When polled, the Receive Packet Available (RPA) output indicates if there is at least one cell available for transfer from the polled link. Upon selection, the interface handles data pausing anywhere in the middle of a cell transfer.

UTOPIA Level 2 Single-Address Slave Mode

In UTOPIA Level 2 Single Address Slave mode, the S/UNI IMA 4 device operates as a single device with a single large 124 cell FIFO, with all cells being identified by their virtual PHY ID (VPHY ID) in an address prepend. Each IMA or TC connection is limited to a maximum of 16 cells in the FIFO. The address prepend may be optionally mapped to the HEC/UDF field to maintain the standard cell length. When the address presented on the Any-PHY/UTOPIA Interface RADR pins matches a programmable 5-bit configuration register (DEVID), the RXAPS responds to polls. In all other cases, the output signals are tristated that allows other slave devices to respond. When polled, the RPA output indicates if there is at least one cell available for transfer from any link.

Any-PHY Slave Mode

In Any-PHY Slave mode, the S/UNI IMA 4 device operates as a single device with a single large 124 cell FIFO, with all cells being identified by their virtual PHY ID (VPHY ID) in an address prepend. Each IMA or TC connection is limited to a maximum of 16 cells in the FIFO. When the address presented on the Any-PHY/UTOPIA Interface RADR pins matches a programmable 5-bit configuration register (DEVID), the RXAPS responds to polls. In all other cases, the output signals are tristated that allows other slave devices to respond. When polled, the RPA output indicates if there is at least one cell available for transfer from any link. In Any-PHY mode, data pausing is not supported.

To support current and future ATM Layer devices, the cell interface is configurable as either an Any-PHY or UTOPIA L2 interface. Table 2 summarizes the distinctions between the two protocols.

Table 2 UTOPIA L2 and Any-PHY Comparison

Attribute	UTOPIA L2	Any-PHY
Latency	RDAT[15:0], RPRTY, and RSOP are driven or become high impedance immediately upon sampling RENB low or high, respectively. The RPA is driven with the cell availability status one CLK cycle after the RADR[4:0] pins match the S/UNI IMA 4's address. A match is defined as either matching the programmed value in single PHY mode or being within the correct range for multi-PHY mode.	RDAT[15:0], RPRTY, RSOP and RSX are driven or become high impedance on the RCLK rising edge following the one that samples RENB low or high, respectively. The RPA is driven with the cell availability status two CLK cycles after RADR[4:0] pins match the S/UNI IMA 4's address.
RSX	Undefined. It is low when not high impedance.	High coincident with the first word of the cell data structure.
RSOP	High coincident with the first word of the cell data structure.	High coincident with the first byte of the cell header.
Paused transfers	Permitted by deasserting RENB high, but the S/UNI IMA's address must be presented on RADR[4:0] the last cycle RENB is high to reselect the same PHY.	Not Permitted.

Attribute	UTOPIA L2	Any-PHY
Autonomous deselection	Not supported. A subsequent cell is output (provided one is available) if RENB is held low beyond the end of a cell.	The outputs become high impedance after the last word of a cell is transferred and until the S/UNI IMA 4 device is reselected.

Receive Cell Transfer Format

The cell format for the receive direction is the same as the transmit interface; see Figure 8 and Figure 9 for the formats.

Figure 8 16-bit Receive Cell Transfer Format

	Bits 15-8	Bits 7-0
Word 0 (Any-PHY and single channel UL2 only*)	**Address Prepend**	
Word 1 (Optional)	**Optional Prepend**	
Word 2	**H1**	**H2**
Word 3	**H3**	**H4**
Word 4*	**HEC/UDF**	
Word 5	**PAYLOAD1**	**PAYLOAD2**
Word 6	**PAYLOAD3**	**PAYLOAD4**
	•	•
	•	•
	•	•
Word 28	**PAYLOAD47**	**PAYLOAD48**

Note:

- Address prepend for Single Channel UL2 may be inserted in HEC/UDF field instead of prior to the cell.

Figure 9 8-bit Receive Cell Transfer Format

	Bits 7-0
Byte 0 (Any-PHY and single channel UL2 only*)	**Address Prepend**
Byte 1 (Optional)	**Optional Prepend[15:8]**
Byte 2 (Optional)	**Optional Prepend[7:0]**

Byte 3	**H1**
Byte 4	**H2**
Byte 5	**H3**
Byte 6	**H4**
Byte 7*	**HEC**
Byte 8	**PAYLOAD1**
	•
	•
	•
Byte 55	**PAYLOAD48**

Note:

- Address prepend for Single Channel UL2 may be inserted in HEC/UDF field instead of prior to the cell

For Any-PHY mode or single-PHY mode, the address prepend field encoding indicates the virtual PHY ID. The virtual PHY ID contains 2 sections, the lower 7 bits indicates the virtual PHY ID with valid values for 0 to 7, while the upper bits are user programmable and not used by the device but may be required in a user's system for unique device identification when multiple devices exist on a bus.

For UTOPIA multi-PHY mode, the address prepend is not used.

9.1.3 Summary of Any-PHY/UTOPIA Modes

The following table summarizes the available modes of the Any-PHY/UTOPIA Interfaces.

Table 3 Available Modes of the Any-PHY/UTOPIA Interfaces

Mode Dir & Protocol	UL2 Single PHY	UL2 Multi-PHY	Any-PHY
TX Poll	Not supported	PHY Channels: 4	PHY Channels: 4
		Channel Enable Register: TCAEN(3:0)	Channel Enable Register: TCAEN(10:0)
		Channel Address Pins: TADR(1:0)	Device ID Register: CFG_ADDR_MSB(6:3)
		Status Pin: TCA	Channel Address Pins: TADR(6:0)
			Address Qualifier Pin: TCSB
			Status Pin: TCA
TX Select	Not supported	PHY Channels: 4	PHY Channels: 4
		Channel Enable Register: TCAEN(3:0)	Channel Enable Register: TCAEN(10:0)

Mode Dir & Protocol	UL2 Single PHY	UL2 Multi-PHY	Any-PHY
		Channel Address Pins: TADR(4:0)	Device ID Register: CFG_ADDR(15:7) or (7)
		Select Pin: TENB	Channel Address: Prepend bits (6:0)
			Device Address: Prepend bits (bit 15:7, for 16 bit mode) or (bit 7 for 8-bit mode)
			Select Pin: TENB
TX Transfer	Not supported	Cell Size: 8 bit X 53 or 55 bytes	Cell Size: 8 bit X 54 or 56 bytes
		Cell Size: 16 bit X 27 or 28 words	Cell Size: 16 bit X 28 or 29 words
		Enable Pin: TENB	Enable Pin: TENB, TSX to indicate first byte of transfer.
		Pause in Cell: w/ TENB	
RX Poll	PHY Channels: 1	PHY Channels: 4	PHY Channels: 1 (in-band addressing identifies virtual PHY's)
	Device ID Register: DEVID(4:0)	Channel Enable Register: RCAEN(3:0)	Device ID Register: DEVID(4:0)
	Device Address Pins: RADR(4:0)	Channel Address Pins: RADR(4:0)	Device Address Pins: RADR(4:0)
	Status Pin: RCA	Status Pin: RCA	Status Pin: RCA
RX Select	PHY Channels: 1	PHY Channels: 4	PHY Channels: 1
	Device ID Register: DEVID(4:0)	Channel Enable Register: RCAEN(3:0)	Device ID Register: DEVID(4:0)
	Device Address Pins: RADR(4:0)	Channel Address Pins: RADR(4:0)	Device Address Pins: RADR(4:0)
	Select Pin: RENB	Select Pin: RENB	Select Pin: RENB
RX Transfer	Cell Size: 8 bit X 53, 54, 55 or 56 bytes	Cell Size: 8 bit X 53 or 55 bytes	Cell Size: 8 bit X 54 or 56 bytes
	Cell Size: 16 bit X 27, 28 or 29 words	Cell Size: 16 bit X 27 or 28 words	Cell Size: 16 bit X 28 or 29 words
	Enable Pin: RENB	Enable Pin: RENB	Enable Pin: RENB
	Channel Address: Prepend or UDF	Pause in Cell: w/ RENB	Channel Address: Prepend

9.1.4 ANY-PHY/UTOPIA Loopback

For diagnostic purposes, the capability to loopback all Any-PHY/UTOPIA traffic back to the Any-PHY/UTOPIA bus is provided. Cells are taken from the Transmit group FIFOs and placed into the respective Receive Group FIFOs, or to a single FIFO on a space available basis. If the receive interface is in Any-PHY or single address UTOPIA L2 mode, all TX ports are looped back to the respective Rx port.

9.2 IMA Sub-layer

9.2.1 Overview

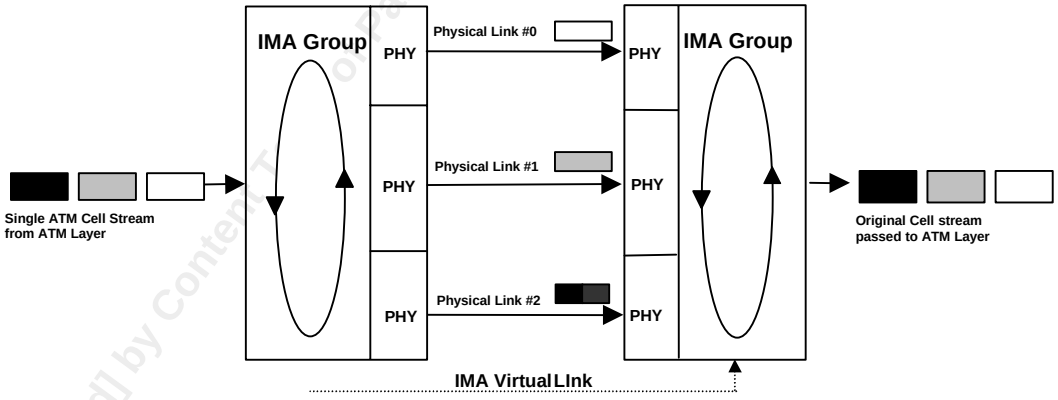
The IMA protocol provides inverse multiplexing of a single ATM stream over multiple physical links and reassembles the original cell stream at the far-end. The inverse multiplexing is performed on a cell basis; hence, the IMA protocol is described as a cell-based protocol. See Figure 10.

The protocol is based upon the concept of an IMA frame. An IMA frame is programmable in size and is delineated by an IMA Control Protocol (ICP) Cell. It is recommended that the ICP cells of each link in the IMA group be offset from each other to reduce the notification time of link/group status changes.

The transmitter is responsible for aligning the IMA frames on all links within a group, and for ensuring that cells are transmitted continuously by adding filler cells as necessary. To maintain frame alignment in the presence of independently timed line clocks, a cell based stuffing algorithm is used.

Since the IMA frames are aligned on transmission, this allows the receive end to recover the IMA frames and align them to remove any differential delay between the physical links.

Figure 10 Inverse Multiplexing



Tx direction cells distributed across links in round robin sequence
Rx direction cells recombined into single ATM stream

9.2.2 IDCC scheduler

The IMA Data Cell Clock (IDCC) scheduler calculates the IMA Data Cell Rate (IDCR) for each group that is used by both the Receive and the Transmit IMA processors. There is one scheduler for each direction (TXIDCC and RXIDCC), and each scheduler can monitor the rate of up to 4 reference clocks; each scheduler can also generate up to 4 IDCC clocks based upon IDCR. For each group, the reference link can be selected to be one of the 4 monitored links. Each of the monitored links can only be the reference link for one group. IDCR is calculated using the following equation, with N_{on} and M set independently for each IDCR generator. N_{on} is the number of active links, M is the size of the IMA frame, and TRL Cell Rate (TRLCR) is the cell rate of the reference link.

$$IDCR = N_{on} \text{ X } TRLCR \text{ X } (M-1/M) \text{ X } (2048/2049)$$

TRLCR is generated from the byte rate. The byte rate is obtained by monitoring the data transfers on the internal bus in the TC layer.

For each IDCR clock tick, a service request is generated and placed into a rate based FIFO. Since there may be many requests generated in a short amount of time and the rate at which each request is generated may be different, a method must arbitrate between the requests to prevent blocking of high rate requests by large numbers of low rate requests. To achieve this, each request is placed into a priority FIFO. The priority of the request is based upon its rate. There are a total of 5 rate-based FIFOs. When a service request is accepted by the Transmit IMA processor (TIMA) or the Receive IMA Data Processor (RDAT), the next request to be presented is taken from the highest priority FIFO that has an entry. In this manner, the higher rate requests get higher priority than the lower rate requests. Since the S/UNI IMA 4 device can service all of the requests, this algorithm limits the CDV experienced by any service request to approximately one inter-arrival time of the service request for each group.

Rate changes are restricted to IMA frame boundaries. An IMA frame boundary occurs once every (M-1)*N service requests. When a request is received to change the rate(N_{on}), the request is saved until the next IMA frame boundary, at which point it takes effect. By restricting rate changes to frame boundaries, the rate accuracy is preserved preventing FIFO underflows/overflows. Since rate changes are not instantaneous, a vector that represents the active Link IDs (LIDs) in the group is passed with the service request. This way, the entity receiving the service requests learns of the change in rate and of which links should currently be in the round robin for servicing.

All IMA-based rate changes are internally managed by the S/UNI IMA 4 device; no user interaction is necessary for correct scheduling.

The IDCC is also used for scheduling the TC data flow. In this case, the rate generated is simply the cell rate of the TC link and is not modified for IMA ICP cells or stuff cells according to the following equation:

IDCR = TRLCR

For all TC connections, the IDCC must be configured in TC mode for the physical link.

9.2.3 Transmit IMA Processor (TIMA)

The TIMA is responsible for the transmit IMA functions. This consists of distributing the cells arriving from the ATM layer to links in a group and for inserting ICP cells, filler cells, and stuff cells as required by the IMA protocol. Additionally, the TIMA can support cell transmission on connections using only the Transmission Convergence (TC) sublayer without the use of the IMA protocol sublayer.

IMA Frame

The Transmit IMA processor creates the IMA frame by inserting an ICP cell after every (M-1) cells per link. Values of M supported are 32, 64, 128, and 256. The ICP cell is offset within the IMA frame. This offset is programmable on a per-link basis, and the offsets should spread throughout the frame. To avoid interaction between groups, the offsets within a group may not be aligned at the same offset. If offsets are aligned at the same offset within a group, the CDV experienced by other groups is increased. Each frame is identified with an IMA frame sequence number (IFSN); this number is the same for every link in the group that is within the same frame and increments with each frame. The TIMA is responsible for aligning the transmission of the IMA frame on all links within a group.

Stuffing Procedure

The TIMA can support both Independent Transmit Clock (ITC) and Common Transmit Clock (CTC) modes. The difference between these modes is the stuffing protocol. The method of stuffing is set independently from the clocking mode present in the ICP cell.

In CTC mode, a stuff cell is added after 2048 cells on each link. The stuff cell is identical to the ICP cell and is inserted immediately following the ICP cell. The programmed ICP offsets determine at which cell in the frame the stuff event occurs.

In ITC mode, a stuff cell is added to the reference link after 2048 cells on the reference link. On all other links in the group, stuff cells are added as necessary to compensate for data rate differences between the link and the reference link of the group. The added stuff cells (or lack of stuff cells) keep the data rate between links equalized.

The stuff cell is generated immediately after the ICP cell and both the ICP cell and the stuff cell are identified as stuff cells via the Link Stuff Indication (LSI) field of the ICP cell.

In CTC mode, the stuff event is advertised in the ICP cell of the preceding frame. The stuff event may also be advertised in the four preceding frames. It is programmable per group if the ICP cell is advertised starting 1 frame or four frames prior to the occurrence of the stuff event.

In ITC mode, the stuff event may be advertised in the ICP cell of the preceding frame or in the four preceding frames. If the stuff event must be advertised for four preceding frames, a DS1/E1 clock tolerance of +/- 50 ppm, or better, is required. If a frequency tolerance of +/- 50 ppm cannot be met among the independent transmit clocks, the TIMA can provide the single frame advertisement of stuff events.

To determine when a stuff cell is needed on ITC mode links (not the TRL), a link stuff detection unit with rate counters tracks the relative rate of data being read from the link FIFOs within a group to the rate of data being read from the TRL FIFO for the same group. When the relative rate counter indicates that the rate differences have accounted for a slip of a cell, a stuff cell is inserted.

Data Flow

The TIMA can support up to 4 groups (IMA group or TC link). Each FIFO on the ATM-layer interface side represents either an IMA group or a TC group. Each group's behavior is controlled by the internal memory tables and records.

For IMA groups, the following internal memory structures are used:

The Transmit IMA Group Configuration Record for configuring group options and mapping to a port on the ATM interface (VPHY ID).

Transmit IMA Group Context Record contains statistics and the current ICP cell image.

Transmit LID to the Physical Link Mapping Table maps individual physical links into a group and assign the LIDs.

TIMA Physical Link Context Record contains per-link statistics, and state information.

For TC links, only one record is used, the Transmit Physical Link Record, to maintain statistics and to map the physical link to a port on the ATM interface (VPHY ID). Regardless of the setting of the TCAEN bits, the VPHY ID may only be programmed in the TIMA between values of 0 and 3. The Any-PHY/UTOPIA Interface converts all incoming addresses down to values in this range, depending on TCAEN.

The TIMA performs cell transfers from the group FIFOs to the link FIFOs in response to service requests from the Tx IDCC. The Tx IDCC schedules both IMA groups, as well as low rate TC-only connections. Groups are scheduled according to their rates. Higher-rate groups are prioritized above the lower-rate groups. The TIMA operates at a rate sufficient to ensure the Tx IDCC does not suffer request congestion provided the ICP cells are spread throughout the frame on IMA groups. If there is no service request pending, the TIMA remains idle. If a group is unused, no cells are pulled from the respective group FIFO. Therefore, when de-activating groups, ATM cell flow to the S/UNI IMA 4 device should be terminated prior to de-activating the group to prevent stale data from being stored in the group FIFO.

IMA Service

For each IMA group-service request, a cell is transferred from the group FIFO to one of the link FIFOs. If no cell is available from the group FIFO, an IMA filler cell is generated and placed in the link FIFO. The link FIFOs within a group are serviced in a round-robin fashion, with the round-robin order determined by the LID. If the next link in the round robin is due to receive an ICP cell, the ICP cell is generated using the link and group state information from the Transmit IMA Group Context Record, and the LID and LSI from the link. If a stuff event is scheduled, the stuff ICP cell is also inserted. Whenever an ICP cell is inserted, the IMA group servicing proceeds to the next link in the round robin without waiting for another service request. The IMA group service is complete when either: (1) a cell is transferred from the group FIFO or (2) an ATM filler cell is generated. When links are in the process of being added, but are not yet available for carrying data traffic, IMA frames consisting of filler cells and ICP cells are generated. Such links are not scheduled by the Tx IDCC scheduler, but are processed with the currently active links.

During group start-up, even with all of the transmit links in the unusable state, the Tx IDCC scheduler is started and IMA frames are generated. During group start-up (i.e., links are not yet in the active state), a group can be configured such that cells received via the UTOPIA L2 / Any-PHY bus can be dropped to avoid the accumulation of stale data or to drop stale data in the group FIFO left over from a previous use of the VPHY ID. During link additions, IMA frames are generated on new links when they are added to the group.

TC Only Service

For TC-only mode groups, servicing is also initiated by group service requests from the Tx IDCC. However, servicing a group FIFO simply entails transferring a cell from the group FIFO to the proper link FIFO. If a cell is not present in the group FIFO, no cells are transferred and the servicing of the request is complete. In TC mode, no other cells are inserted into the data stream by the IMA sub-layer (physical layer idle cells are generated by the physical layer).

Timing Reference Link Maintenance

It is possible to have the timing reference link for an IMA group change from one link to another while the IMA connection is in operation. If an IMA group is operating in CTC mode, the reference link used for the scheduling is simply switched. The next stuff cell insertion still occurs 2049 cells after the previous stuff. If the IMA group is operating in ITC mode and the reference link is switched, the first stuff insertion on the new TRL occurs at approximately the same frame a stuff would have been inserted had it not become the TRL. At the time of the TRL change, the existing accrued rate differential on the new TRL prorates the number of cells out of 2048 until the next TRL stuff. Although the first stuff occurs at approximately the proper number of cells to maintain the correct differential delay, the actual time of the stuff is dependent on the new TRL rate.

Similarly, the first stuff cell insertion on the previous TRL occurs in approximately the same frame a stuff cell would have been inserted had it still been the TRL although the actual frame for stuff insertion is also dependent on the rate difference with the new TRL. This minimizes any effects on the differential delay for the group as well as reducing any FIFO level changes. All subsequent stuff cell insertions on the TRL then happen after every 2048 cells and all subsequent stuff cell insertions on the former TRL are dependent only on the link's rate difference from the new TRL.

9.2.4 Receive IMA Data Processor (RDAT)

The Receive IMA Data Processor (RDAT) performs the IMA data-flow functions in the receive direction including the IMA Frame Synchronization Mechanism (IFSM), storage of data for accommodating differential delay, defect detection, and playout of data in a round robin fashion.

One 16 Mbit (1 Mbit x 16) SDRAM, available as a single chip device, is required. Differential-delay tolerance may be configured through registers on a per-group basis to any value up to the maximum listed in Figure 11. Buffering is allocated on a per link basis. Each link is allocated the same number of cell buffers. Each link is allocated 1024 cell buffers. See Figure 11 for the required memory sizes.

Figure 11 Max Differential Delay Tolerance

# of T1/E1 Links	Cells of Buffering	Delay (T1) in ms	Delay (E1) in ms	SDRAM size
4 T1/ 4 E1	1024	282 ms	226 ms	1Mbit x16

Writing Data to the Delay Compensation Buffers (DCB)

When there is a full cell of data in the RX Link FIFOs, the link requests service. The RDAT arbitrates between links requiring service in a round-robin fashion.

When a link is chosen for service, if it is not an IMA link, the cells are stored in external memory in a per link FIFO.

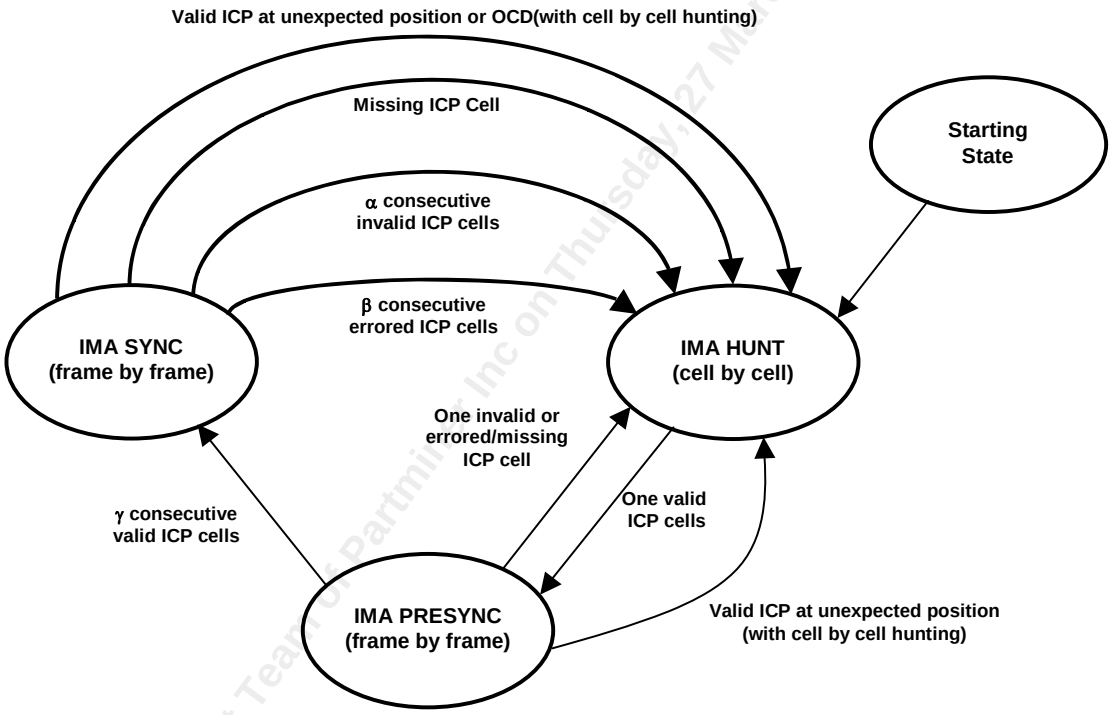
For IMA links, the IFSM is performed to locate the IMA Frame. Once the IMA frame is located, the RDAT calculates the location to store the cells. The cells are stored in a time-based FIFO structure. The buffer address for a cell is created from the cell number in the IMA frame concatenated with the lower x (depends upon M) bits of the IMA frame sequence number. Each link has its own reserved FIFO. The cells are stored in this manner such that they are aligned in time in the external memory and the differential-delay removal is simplified.

During periods in which the link is in a defect state, incoming cells s replaced with filler cells prior to being written to the DCB.

IMA Frame Synchronization Mechanism (IFSM)

For IMA links, the RDAT performs the IFSM. The IFSM is based on the cell delineation mechanism in I.432. The details of the IFSM can be found in AF-PHY-0086.001 “Inverse Multiplexing for ATM (IMA) Specification Version 1.1”, March 1999. The state Machine is shown in Figure 12.

Figure 12 IFSM State Machine



During group start-up, the fields in the ICP cells are validated by the RX IMA Protocol Processor (RIPP) block and the validated information determines if the ICP cells are valid or not. Validation by the RIPP checks the group fields of the ICP cell to ensure that they match the rest of the group and checks the LID to ensure that it is unique in the group. An ICP cell is invalid if the IMA OAM Label, the LID, the IMA_ID, M, IFSN or the offset is not the same as the validated values. If the ICP cell cannot be validated by the RIPP (i.e., the IMA_ID is different from the rest of the group or the LID is a duplicate), the IFSM remains in the starting state.

Once the ICP cells are validated by the RIPP, the IFSM enters the IMA Hunt state. In this state, each cell is examined to see if it is a valid ICP cell. When a single valid ICP cell is received, the IFSM enters the IMA Presync state.

While in the Presync state, at each expected ICP location (determined by the ICP offset and the IMA Frame Length), the cell is examined (frame by frame). Once gamma (γ) valid ICP cells are received, the IFSM enters the IMA Sync state. If either: (1) an invalid (or errored) ICP cell is received or (2) a valid ICP cell is received in an unexpected location, the IFSMl re-enters the IMA Hunt state. While in the IMA Hunt state, the stuff indicators are ignored.

While in the IMA Sync state, ICP cells are continually examined for each frame. If beta (β) consecutive ICP cells with HEC or CRC-10 errors (errored ICP cells) are received, then the IFSM reenters the IMA Hunt state. Also, if alpha (α) consecutive invalid ICP cells are received, the IFSM reenters the IMA Hunt state. If a cell is received at the expected ICP position without an HEC error or OCD and without the IMA OAM cell header, or is a filler cell, it is considered a missing ICP cell, and the IFSM reenters the IMA Hunt state immediately. Finally, if a valid ICP cell is received at an unexpected position, or OCD is detected, the IFSM reenters the IMA Hunt state.

Alpha, Beta, and Gamma are globally programmable for the device. The RDAT keeps working-counts for these parameters for each link. Note that alpha (the count of consecutive invalid ICP cells) is not reset when an errored cell is received. Although beta (the count of consecutive errored ICP cells) is reset when an invalid ICP cell is received.

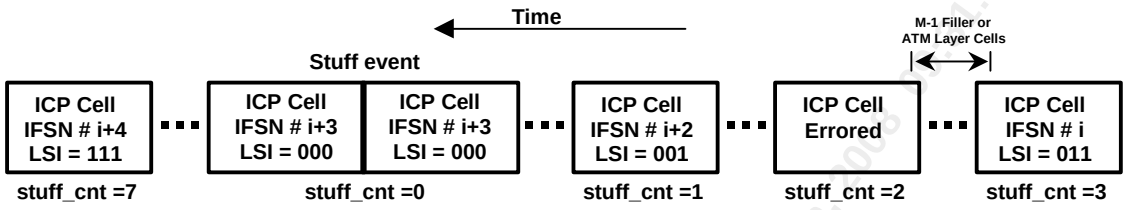
Stuff Events

At this point, the RDAT detects and removes the stuff cells. Stuff cells are identified by the LSI field with the ICP cells. Stuff events consist of two back-to-back ICP cells on the same link. One of the ICP cells is considered a stuff cell. Since stuff cells are inserted for the purpose of equalizing the data rate on links with independent clocks, stuff cells are removed.

To improve robustness in the presence of errors, the transmitter must advertise that a stuff event is going to occur in the ICP cell in the frame preceding the stuff event. The transmitter may also advertise the stuff event for the 4 frames preceding the stuff event.

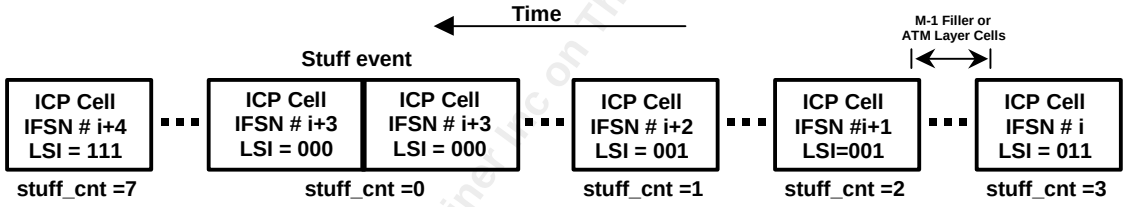
Once a valid non-errored ICP cell is received with a LSI of 001, 010, 011, or 100, the RDAT maintains an internal stuff count in link-context memory. This count is decremented every frame, until the stuff event occurs. The count is decremented even if an incoming ICP cell is errored or invalid (as shown in Figure 13). An ICP cell received with an invalid stuff sequence (i.e., LSI of 001, when a LSI of 010 was expected) is declared invalid, and the internal stuff count is decremented from the previous value (as shown in Figure 14. The internal count is reset to the maximum when the stuff event occurs. A stuff sequence of 111 followed by 000 is not considered an invalid stuff sequence (i.e., the RDAT accepts immediate notification of a stuff event, to support the case when the 001 stuff cell was errored).

Figure 13 Stuff Event with Errored ICP (Advanced Indication)



IFSN: IMA Frame Sequence Number
LSI: Link Stuffing Indication

Figure 14 Invalid Stuff Sequence (Advanced Indication)



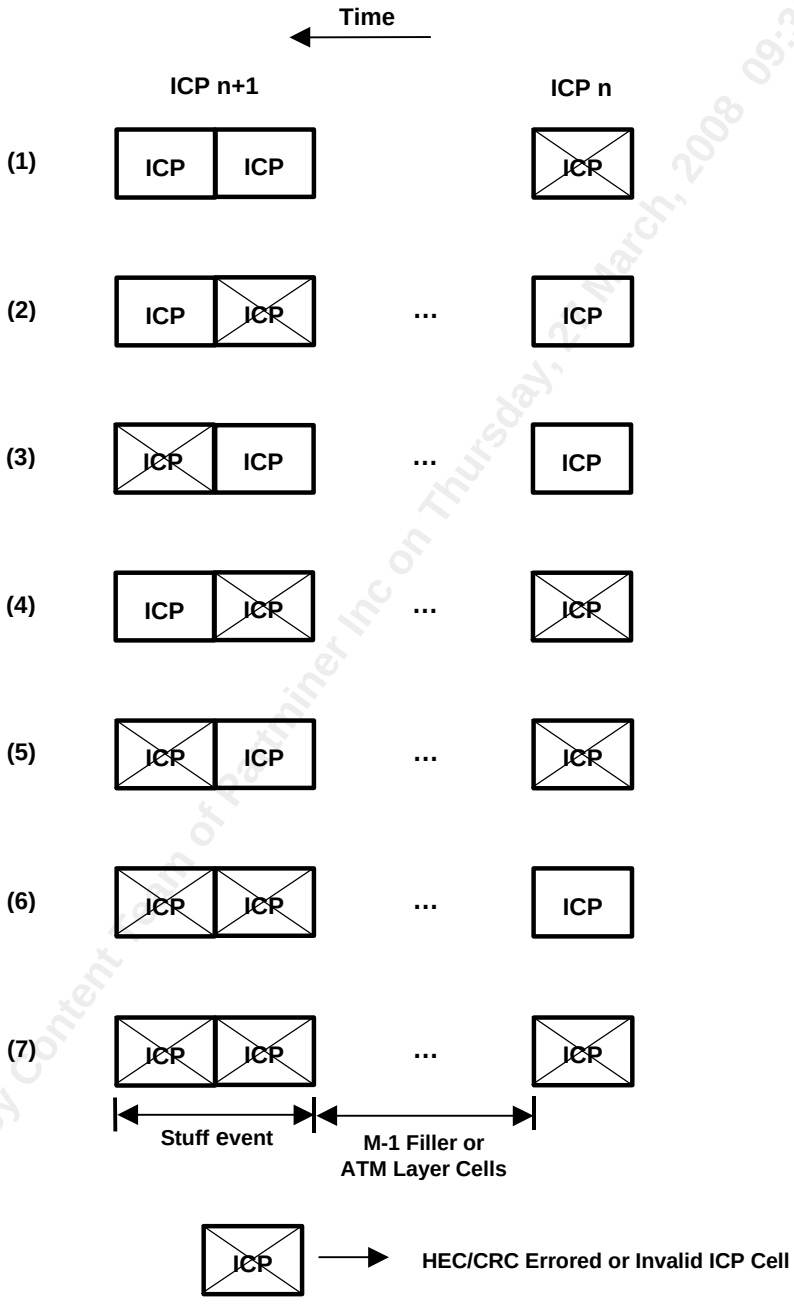
IFSN: IMA Frame Sequence Number
LSI: Link Stuffing Indication

IMA Frame Synchronization with Stuff Events

The RDAT maintains synchronization while receiving stuff events subjected to HEC or CRC errors, as shown in Figure 15. When one of the ICP cells comprising a stuff event is errored or invalid, the other is used. If both are errored or invalid, then the internally maintained stuff count identifies the stuff event (given that the advanced indicators were correct).

All of the cases assume that the IFSM is in the IMA Sync state prior to the window shown, and that the current errored/invalid counts are zero. Cases (1) through (6) require that alpha or beta be programmed to a value greater than one for synchronization to be maintained. Case (7) requires that alpha or beta be programmed to a value greater than two for synchronization to be maintained. Case (7) also requires that advance link stuff indication be given prior to the window shown to detect the stuff event.

Figure 15 Errored/Invalid ICP Cells in Proximity to a Stuff Event

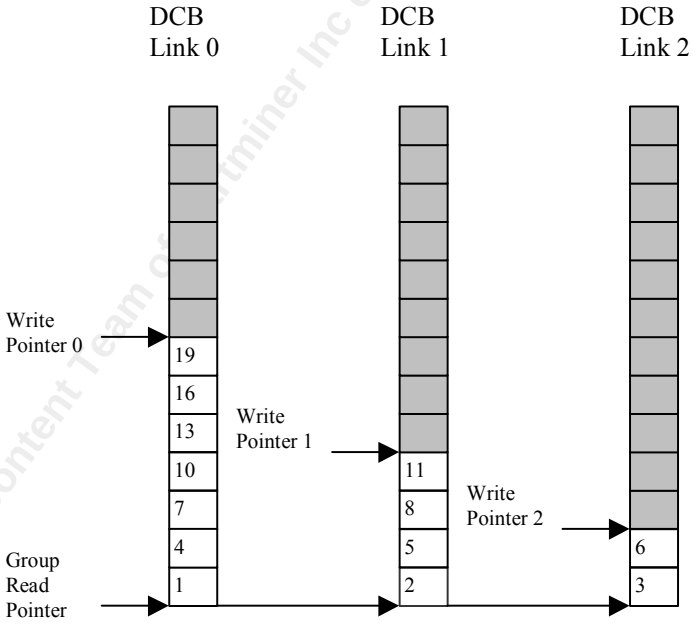


Delay Compensation Buffers

Since IMA must re-create the original cell stream in the proper order, delay compensation buffers (DCBs) are used to remove the differential delay between the links in a group. As cells arrive from each link, they are placed in that link's DCB. Links with the least transport delay have the largest amount of data in the DCB, while links with the largest amount of transport delay have the least amount of data in the DCB.

At group start-up, all the links are compared to determine the link with the largest transport delay and the link with the least transport delay. The difference between these is the differential delay. Data is queued for all links until the corresponding data arrives for the link with the largest transport delay. Figure 16, shows a group with 3 links with a differential delay of 5 cells. Link 0 has the shortest transport delay and link 2 has the longest transport delay. Once the data has arrived for all of the links, it is played out to the ATM layer at the IDCC rate, thus keeping the depths of each DCB at a nominally constant level. (Depths are instantaneously affected by the presence of stuff cells and ICP cells, but these effects are transitory).

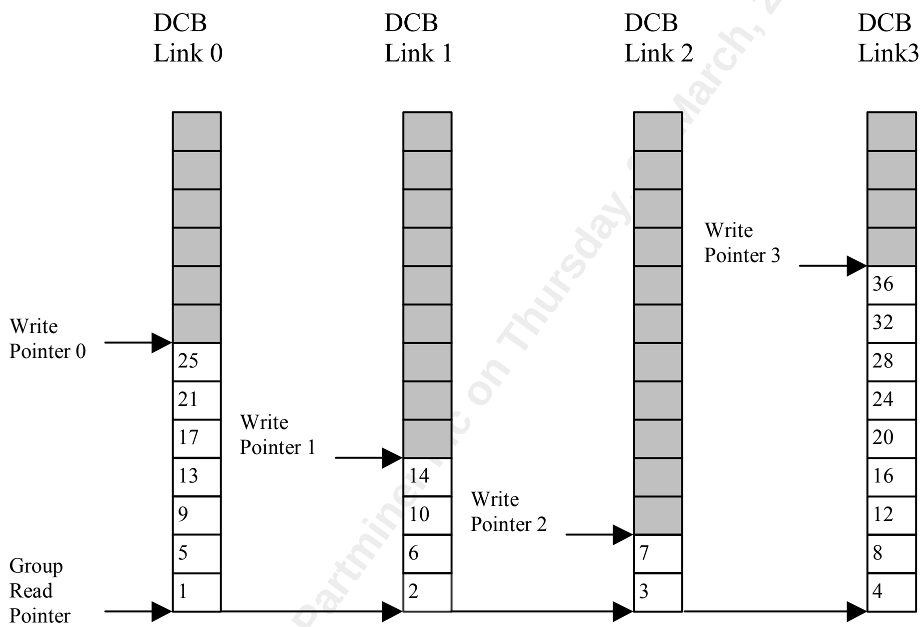
Figure 16 Snapshot of DCB Buffers



When a group is already started, IMA supports the addition of links to the group. As illustrated by Figure 16, adding a link with a transport delay that is within the range of the existing links does not present any problems. The DCB for the new link must be aligned with the existing links and added to the round robin for playout.

Adding a link with a smaller transport delay increases the differential delay of the group. This requires that the depth of the DCB buffer be larger than any of the existing links. As long as the differential delay is within acceptable bounds, the new link can be accepted. The DCB for the new link is aligned with the existing links and added to the round robin for playout.

Figure 17 Snapshot of DCB Buffers after addition of Link with smaller transport delay



Adding a link with a larger transport delay requires the DCB buffer depth to be smaller than the DCB for the link with the largest delay. If the desired DCB depth for the new link is less than 0, this means that the data for the other links is played out prior to the arrival of data for the new link. This is shown in Figure 18. For the new link to be accepted, delay must be added to all other links in the group. When delay is added to the other links in the group, the playout of ATM cells is halted until enough delay is built up. This causes CDV for the group. Once the delay is added, the DCB for the new link can be aligned with the existing links and added to the round robin for playout. Figure 19 shows the case after delay was added to the existing links within the group. The adding of delay to a group may be disabled. In this case, the new link is rejected due to a LODS defect meaning that the DCB could not be aligned with the group. The LODS defect is not reported as the LODS_OVERRUN_INT or LODS_UNDERRUN_INT in the Link Event Interrupt Bit Mapping. Before a link is successfully added to a group, if the link fails LASR because of a LODS defect, the defect is reported as DIFF_DELAY_INT.

Figure 18 Snapshot of DCB Buffers when trying to add Link with larger transport delay

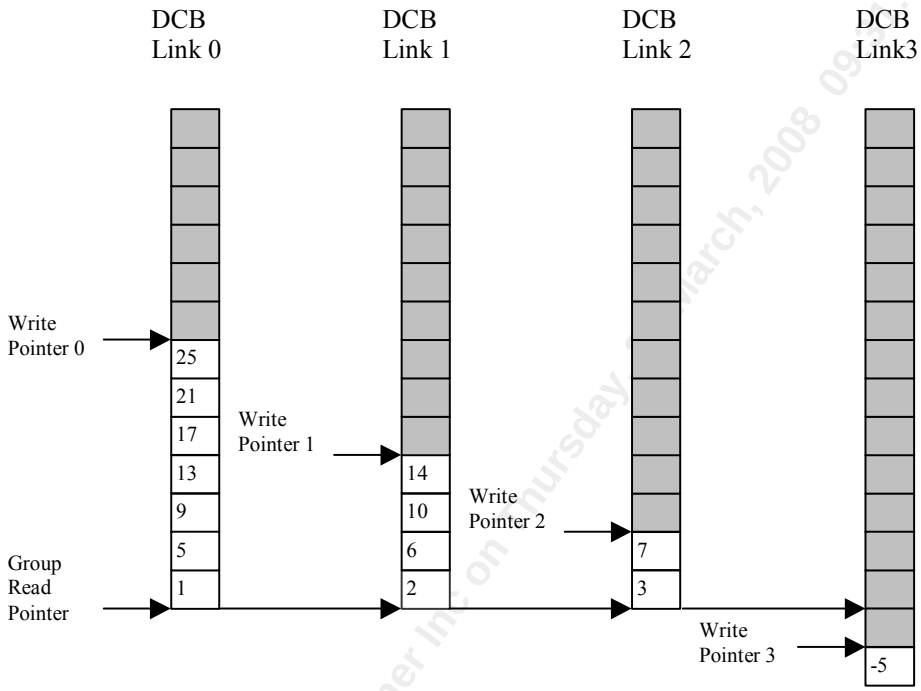
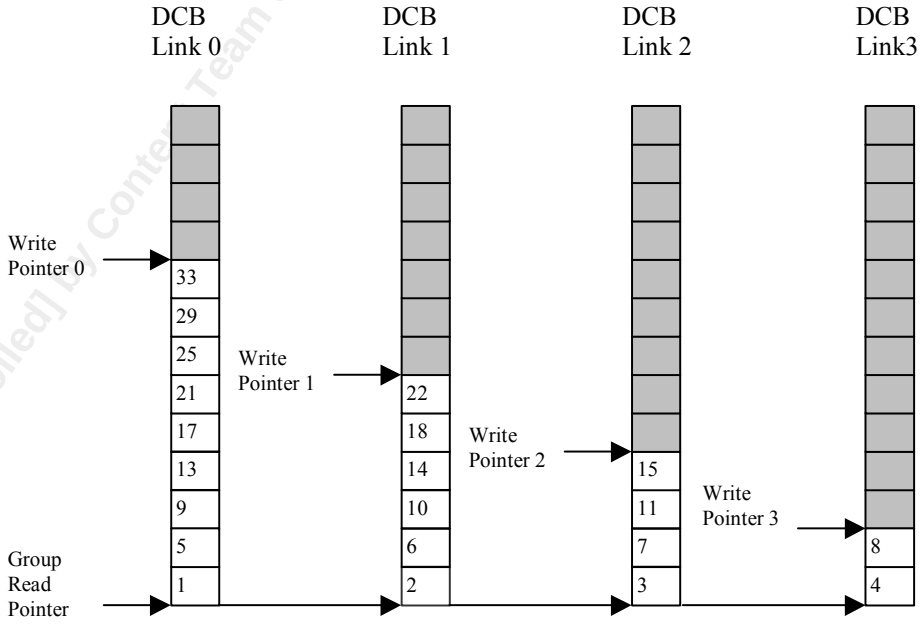
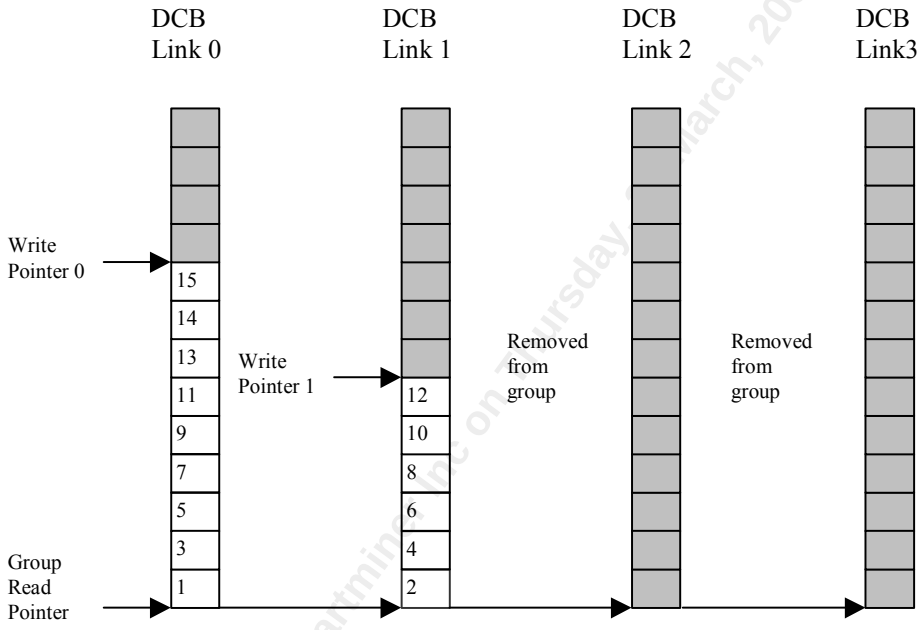


Figure 19 Snapshot of DCB Buffers after delay adjustment



When links are deleted from a group, the DCB buffer depths of the remaining links are not affected. Figure 20 shows that links 2 and 3 are deleted from the group and the depth of the delay compensation buffers remain unchanged.

Figure 20 Snapshot of DCB Buffers after deletion of links from group



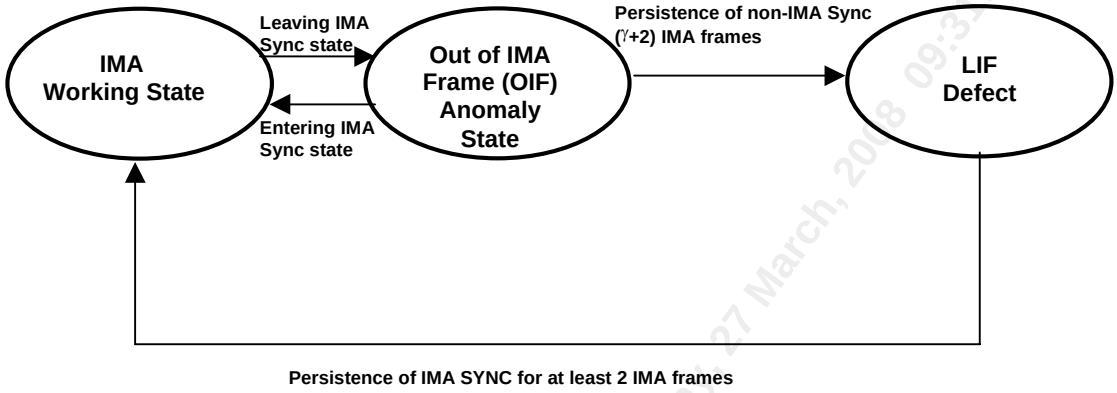
IMA Link Error Handling

For IMA operation, the RDAT is responsible for detecting Loss of IMA Frame defects (LIF), Idle Cells on IMA Links, Loss of Cell Delineation defects (LCD), and DCB overruns/underruns that contribute to Loss of Delay Synchronization (LODS). This information is forwarded to the RIPP with the ICP messages for processing and reporting.

IMA Error/Maintenance State Machine (IESM)

A state machine is maintained for the LIF defect detection. This state machine is called the IMA Error/Maintenance State machine [IESM]. The state diagram for the IESM is shown in Figure 21. The RDAT maintains an IESM for each link. The LIF Defect state is the initial state for this process, thus all links initially come up in the LIF condition.

Figure 21 IMA Error/Maintenance State Diagram



The IMA Working state enables the RDAT to write user cells to the DCB. If the IFSM leaves the IMA Sync state, the IESM state machine transitions to the OIF Anomaly state, and the OIF anomaly counter is incremented.

In the OIF Anomaly state, incoming user cells are written as filler cells to the DCB, and write pointers are incremented. If the IFSM does not return to the IMA Sync state within gamma + 2 frames, the IESM state transitions to the LIF Defect state. (Gamma is programmable, and is the same gamma used in the IFSM). If the IMA Sync state is entered prior to gamma + 2 frames, the IESM state transitions back to the IMA Working State. This is considered a “fast recovery” from the OIF Anomaly.

In the LIF Defect state, incoming user cells are written as filler cells to the DCB, and write pointers are incremented. The LIF-latched status bit is set in the link-context memory. The IESM state machine transitions to the IMA Working state when IMA Sync is detected for two consecutive IMA frames. If the IMA Sync state is entered and then exited during LIF, then the OIF anomaly counter is incremented. When the IESM enters the working state, user cells may be forwarded once again if an overrun (with respect to the configured depth for the link) is not detected. The overrun detection provides the necessary differential-delay checking required after a defect.

Loss of Cell Delineation Status (LCD)

LCD is detected by the TC layer and the information is passed to the RDAT. When a link is in LCD, a LCD-latched status bit is set in link context memory, which is cleared by the ICP cell processing procedure. Cells received while the LCD latched status bit is set are written to the DCB as filler cells, and the write pointers are incremented. After an LCD condition is exited, the delay synchronization of the link must be rechecked and resynchronized.

DCB Overrun Status

When cells are written into the DCB, overruns are checked by comparing the group read pointer against the link write pointer. If the difference between the pointers exceeds the maximum allowed DCB depth, then an overrun is detected. For IMA, this causes the overrun latched status-in-link context to be set.

An overrun condition does not cause the IFSM to exit the sync state.

All user cells are dropped while the overrun condition persists. The overrun condition is reset at the reception of an ICP cell with an acceptable delay as long as the link is clear of LIF or OIF. For TC, an interrupt to the processor is generated and normal operation resumes once the overrun condition has ended.

DCB Underrun Status

When cells are read from the DCB, underruns are checked by comparing the group read pointer against the link write pointer. When an underrun is detected, all user cells are dropped until the underrun condition is cleared. The underrun condition is only cleared at the reception of an ICP cell, such that the differential delay may be re-checked. An underrun condition does cause the IFSM to exit the sync state. Note: If the device remains in the LIF state for a long time (1 hour for E1, longer for T1), DCB underrun may be detected by the device. This occurs because stuff events cannot be detected during LIF, and the internal pointers may wrap-around. DCB overrun does not occur in this situation, as it is automatically masked during LIF.

Idle Cells on IMA Links

When idle cells are detected on an IMA link, they are reported. Idle cells on IMA links may be present for two reasons. They may have been inserted at the ATM layer of the transmitter as a rudimentary method for traffic management; in which case the IMA layer should treat them as user cells and the IMA_IDLE_FWD_EN configuration bit should be set to allow these cells to be forwarded. Otherwise, they may have been inserted at the TC layer to assist with rate matching; this is illegal for IMA links. Idle cells are treated as user cells by the RDAT for IMA processing, although they are not forwarded to the ATM layer if the IMA_IDLE_FWD_EN is not set.

DCB Playout

The IDCC scheduler provides the rate for data to be played out to the ATM layer for an IMA group. For each cell to be played out, the IDCC generates a service request. Upon the IDCC service request, the RDAT plays out data from the FIFOs in a round-robin fashion. For each service request, the RDAT runs the round robin servicing until it processes either a filler cell or user cell. If ICP cells are encountered, the ICP cell is dropped and the servicing continues until a user or filler cell is found. If a user cell is found, it is transferred from the external memory to the appropriate group FIFO. If a filler cell is found, it is dropped.

The RDAT is not sensitive to the alignment of ICP cells within a group. There is no performance degradation even if all of the ICP cells in a group have the same offset.

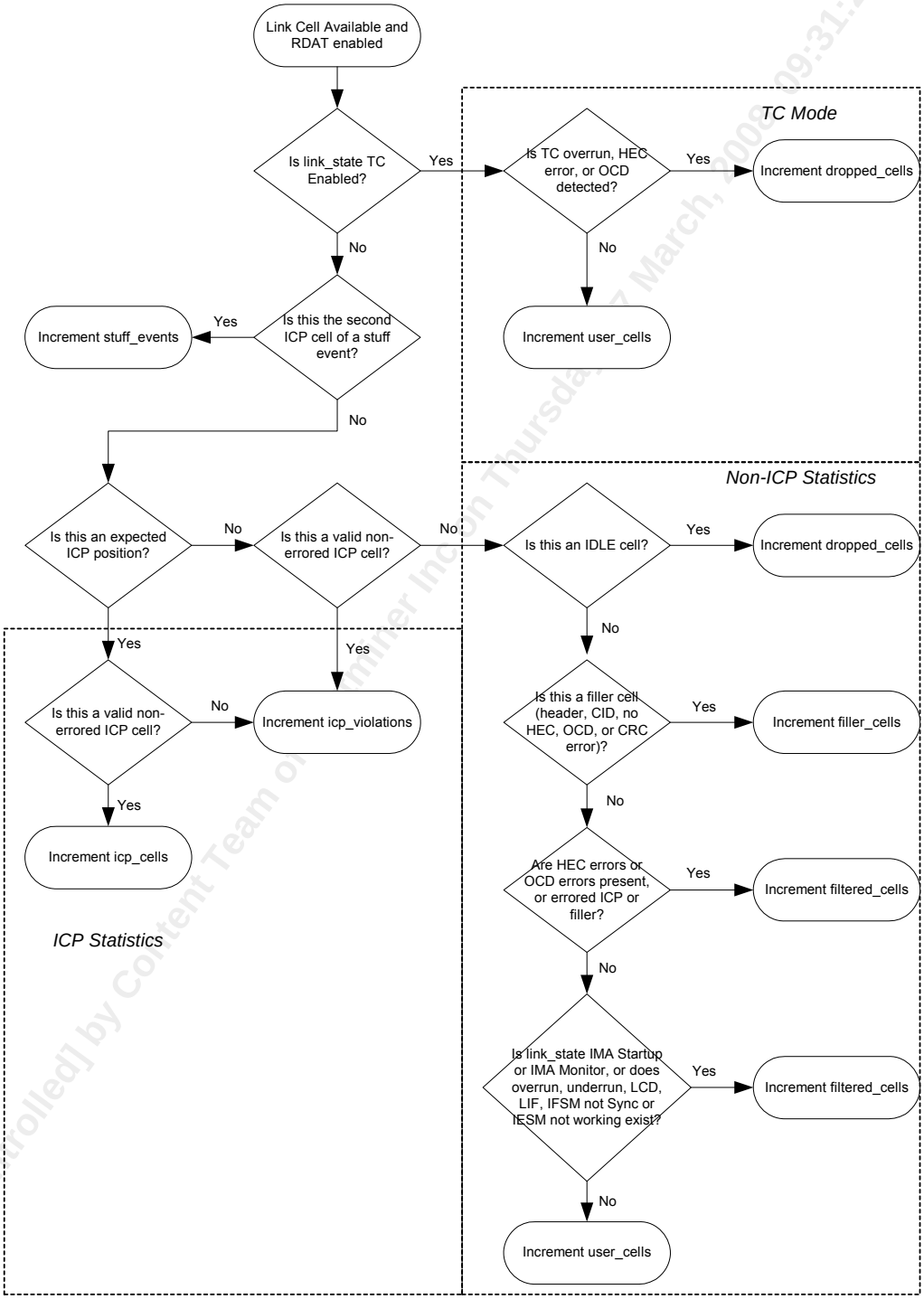
If the device is in Any-PHY mode or UTOPIA L2 Single Port mode, there is only a single FIFO shared among all of the groups. The RDAT ensures that no more than 16 cells are stored in the shared FIFO for a single group. If the S/UNI IMA 4 is in UTOPIA L2 Multi-port mode, each group has its own FIFO. Note that each group does not have a dedicated buffer of 16 cells; the 16 cell limit prevents a small number of groups from monopolizing the shared FIFO depth. The shared FIFO is 124 cells deep.

If the group FIFO is not emptied in a timely fashion, data is dropped; this is similar to the procedure used by any other PHY level device. The IDCC service request FIFO is serviced regardless of the state of the Group FIFO. For multi-port mode, if the respective Group FIFO is full, the cell is dropped. In Any-PHY mode and UTOPIA L2 Single Port mode, if either the shared FIFO is full or there are already 16 cells for the current group in the FIFO, the cell is dropped.

Receive Statistics

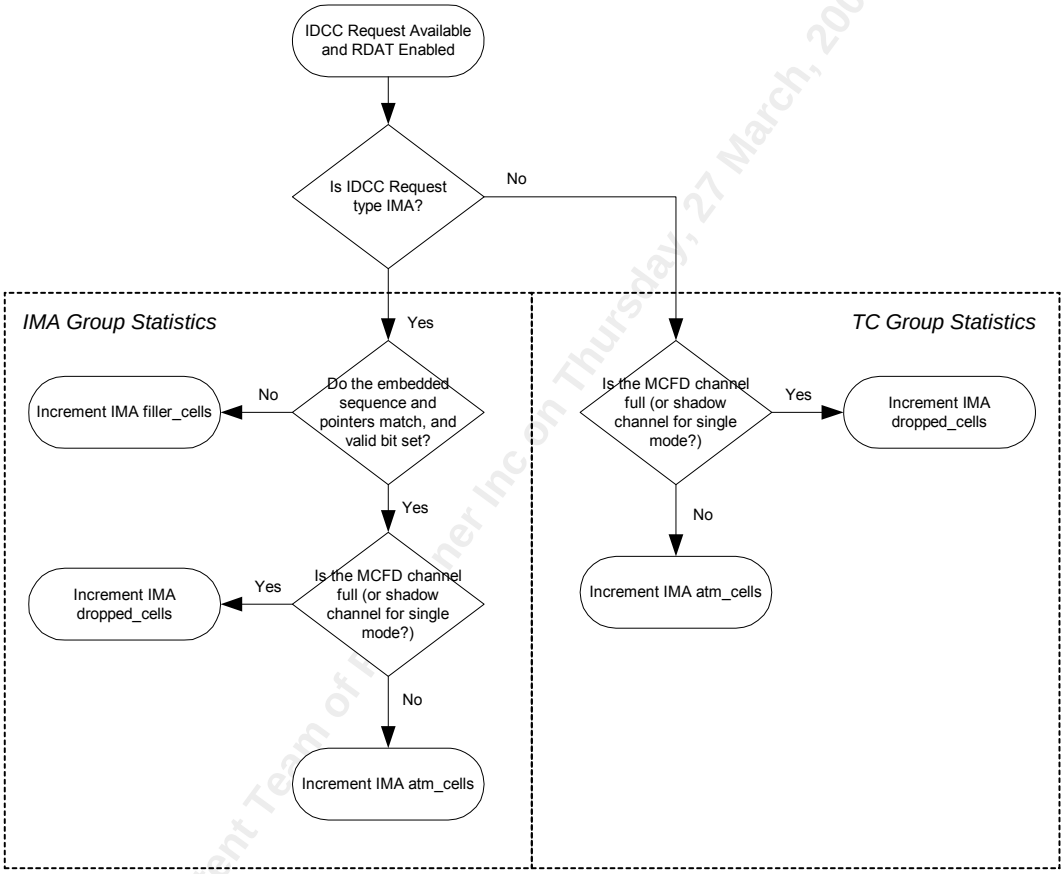
The RDAT maintains statistics on a per-link basis during link data processing, and on a per-group basis during ATM data processing. These statistics may be accessed though the indirect ECBI register interface, and are defined in section 10.8. For the link statistics, eight statistics are provided. The OIF anomaly statistics may be incremented in addition to one and only one of the other seven statistics, as shown in Figure 22.

Figure 22 Link Statistics Flow Diagram



For the group (reader) statistics, four counters are provided for IMA groups, and two for TC groups. One and only one of these six counters may be incremented for a given cell, as shown in Figure 23.

Figure 23 Group Statistics Flow Diagram



9.2.5 Receive IMA Protocol Processor (RIPP)

The Receive IMA Protocol Processor (RIPP) block is responsible for maintaining and controlling the link and group state machines. The RIPP can accept commands from the management plane to initiate group and link state machine actions. The RIPP then controls the contents of ICP cells generated for the transmit data path, as well as analyzes the link and group states received within the ICP cells. The receive link and group states are used to maintain and update the link and group states. The RIPP coordinates group-wide state transactions and performs the group-wide procedures such as the Synchronized Link activation during Group Start-up Procedure and the Link Addition and Slow Recovery (LASR) procedure. When the links change state, the RIPP also coordinates the rate change between the round-robin procedures located in the receive and transmit data paths and their respective rate schedulers.

Since failures are based upon the persistence of defects, the defects are detected and passed as interrupts/status to the management plane. PM is responsible for the integration of defects into failure conditions and to set the failure conditions in the S/UNI IMA 4.

Table 4 PM command description

Command	Description
Add_group	Starts up a group state machine and the link state machines for the links configured in the group. Group and links need to be configured prior to issuing this command. As a result of this command, the transmitter starts sending out IMA frames on the links specified as part of the group, and the receiver starts looking for and analyzing ICP cells received on the links within the group. If a sufficient number of links are detected to be active, the group transitions to the operational state and start to transmit and receive ATM traffic.
Delete_group	Remove an existing group and all its links immediately. This command takes the group state machine to the “not configured” state and all of the links in the group to the “not in group” state. The transmit links stops transmitting IMA frames and starts transmitting physical-layer idle cells until the links are reused. For group deletion without any loss of data, the links may be deleted or inhibited to stop traffic on the group or the group may be inhibited prior to deleting the group.
Restart_group	Restart the specified group. When executed, the GSM goes back to “start-up” state and all tx links return to the “unusable” state and the Rx links return to the “unusable” state but report “Not in Group” since the LID is not yet validated. This command is intended to enable the change of parameters during the group start-up phase and to provide a local group reset for other conditions.
Inhibit_group	Set the internal group inhibiting status flag. Once a group is considered inhibited, it goes to BLOCKED state instead of the OPERATIONAL state when sufficient links exist in the group. If the group is already in OPERATIONAL state when the command is issued, the GSM goes to BLOCKED state, and blocks the Tx data path. However, the Rx data path remains on.
Not_inhibit_group	Clear the internal group inhibiting status. If the group is currently in BLOCKED state, the GSM goes to OPERATIONAL state.
Start_LASR	Start LASR procedure on one or more links. The links involved may either be new links or existing links with a failure/fault/inhibiting condition. If the group configuration is symmetric, links should be added in both the Tx and Rx direction.

Command	Description
Delete_link	Remove one or more links from the group. If the group configuration is symmetric, links should be deleted in both the Tx and RX directions. When a Tx link is deleted, user traffic is no longer sent on the link and the Tx LSM state is reported as “Not in Group”, but IMA frames are still generated. When either a timeout expires (TX_link_deleted_timeout) or the FE Rx is detected to be no longer active, the deleted links stop generating IMA frames and start generating idle cells until the link is reused. When an Rx link is deleted, the Rx LSM state is reported as “Not in Group”, but traffic is still received and passed to the ATM layer, until either a timeout expires (RX_link_deleted_timeout) or FE Tx state is detected to be no longer active. Data received after this point is no longer forwarded to the ATM layer. The Rx link is available for reuse after all the data accumulated in the DCB is forwarded to the ATM layer. No data is lost in the link deletion procedure unless the timeout occurs prior to the FE state change detection.
Set_rx_phy_defect	Indicate to S/UNI IMA 4 that the given link(s) have/have not physical defects (such as LOS/LOF/OOF/AIS) which are not detectable internally. This causes the S/UNI IMA 4 to start reporting physical layer defects in the RX Defect Indication field in the ICP field for the affected links. When the defect bit is set in the command, this also sets an internal state which prevents the affected LSM’s from progressing towards active (until the unusable_link command is issued), and immediately terminates any currently active timers which are waiting on FE state changes for the affected LSM’s. The termination of these timers (such as RX_link_deleted_timeout, RX_link_blocked_timeout, or TX_link_deleted_timeout) may result in an immediate NE LSM state change.
Unusable_link	Force Links to an unusable state and provide the cause. This command must be issued after the set_rx_phy_defect command is issued prior to recovering the links. For Rx Links, if the cause is inhibited, the links are taken through the blocking state to preserve data sent prior the link being inhibited. If the cause is a fault or a failure condition, the link is taken directly to the UNUSABLE state. At this point, data would have already begun to be discarded due to the defects detected on the link. For Tx Links, data stops being accepted on the Unusable links and IMA frames are generated consisting of filler cells.
Update_test_ptn	Update the TX test pattern info to be sent in the outgoing ICP cells. This command activates, deactivates, or changes the test pattern that is being sent out on the Group. PM must take care to wait at least two frames in between updates to the test pattern to comply with the IMA test pattern standard.
Update_TX_TRL	Update the transmit TRL. When a TRL is changed, three steps are performed: (1) the TRL sent in the ICP cell is changed;(2) the TRL used for calculating the IDCC is changed, and (3) the TRL used in the stuffing algorithm is changed.

Command	Description
Read_event	Read and clear the latched event status, and read the link/group status of the specified group and all its links. The result read from the internal context memory is stored in Cmd_data00 through Cmd_data1F. Refer to RIPP Command Data Registers for further details.
Read_delay	Reads a snapshot of the link-defect status and link-delay information for all of the links within the group. The delay information can be used to determine differential delay, the link with the most delay, and any other delay characteristics of the group. The delay information is provided in units of cells.
Adjust_delay	Adjusts the delay of a group by removing the amount of specified delay. While the delay is being adjusted, links cannot be added or recovered for the group.

In addition to performing commands from PM, the RIPP processes the ICP cells forwarded by the RDAT. When ICP cells arrive from a group, they may be out of order in time due to differential delay between links. The RIPP must examine the ICP cell and determine if it has any new information that needs processing. This can be determined via the IMA frame number and the SSCI field. When processing the ICP cells and the link states, attention must be taken not to violate the group-wide procedures. When link or group states are changed, updated ICP cells are sent to the TIMA for transmission. Any state changes are also communicated to the appropriate schedulers and round-robin processors.

Group Startup and Differential Delay

On group startup, when at least P_{rx} Links obtain IMA frame synchronization, the links are evaluated. As each link is evaluated, the differential delay of the accepted links is tracked. If a link cannot be accepted because the acceptance of the link would violate the programmed maximum DCB threshold (fastest link minus current data read pointer), the link remains in the unusable state and begin to report a LODS defect. Accepted links start reporting a usable state. The LODS defect is not reported as the LODS_OVERRUN_INT or LODS_UNDERRUN_INT in the Link Event Interrupt Bit Mapping. Before a link is successfully added to a group, if the link fails LASR because of a LODS defect, the defect is reported as DIFF_DELAY_INT.

At this point, as additional links acquire frame sync, they are evaluated and either are accepted or begin to report an LODS defect. When all links have acquired frame sync or the timer has expired, the accepted receive links are reported as active. If at least P_{rx} links are accepted, the group state machine transitions to operational.

If sufficient links are not accepted, the group does not become operational. Note that within any collection of links that are targeted to form an IMA group the group may not become operational even though there are combinations of P_{rx} links that meet the programmed maximum DCB threshold. This would occur in situations where the internal algorithm used to determine link order may not select the combination or “tightest” grouping of links that would otherwise meet the programmed maximum DCB threshold. In this case, the relative delays of the links are available to PM using the read_delay command. The microprocessor can then analyze this information, remove the offending link or links and restart the group.

Link Addition and Differential Delay

Once a group is started, the delay profile for the group is determined. To add links, the delay on the new links must be compatible with the existing links in the group and be able to be synchronized with the existing links within the DCB constraints.

There are two mechanisms regarding delay that can be used.

The first method uses the guardband capability. At group start-up, a guardband is added to the link with the longest transport delay. This guardband results in additional delay to be queued in the DCBs for each link in the group. The guardband allows for links with a longer transport delay to be added in the future without introducing any additional CDV. Note that new links with the same or slightly shorter transport delay than the existing link with the longest transport delay (by up to 3 cells) may be rejected from link addition, if the guardband is programmed to 0. This is due to differential delay measurement jitter associated with ICP and stuff cell processing. For this reason, if the first method is used, the guardband should be programmed to a value of 3 or greater.

The second method allows the delay accumulated per link to be increased dynamically. This method introduces additional delay to all of the links within the group when a link with a larger transport delay is added to the group. The process of adding additional delay to the links within a group causes additional CDV to be introduced when the playout of data is stopped while the delay is accumulated.

The RIPP determines the delay of the links that are being added and performs the appropriate action to either include the link in the group or to reject the link if the link cannot be synchronized within the DCB constraints. If a link is rejected due to delay, a LODS defect is reported on the link. The LODS defect is not reported as the LODS_OVERRUN_INT or LODS_UNDERRUN_INT in the Link Event Interrupt Bit Mapping. Before a link is successfully added to a group, if the link fails LASR because of a LODS defect, the defect is reported as DIFF_DELAY_INT.

When links are deleted from the group, the delay of the remaining links is not adjusted.

See “Delay Compensation Buffers” in section 9.2.4 for more details on the management of the DCB buffers.

Removing Accumulated Delay

In some situations, removal of accumulated delay may be desired. This usually occurs after a group is operational for a period of time and the link characteristics in terms of transport delay have changed. The adjust_delay command is provided to remove delay from the group. The execution of this command affects the CDV of the group while the delay is reduced. Any delay adjustment to the group also affects the CDV of a connection carried on that group. This is additive, if 20 ms of delay is removed from the group, a particular connection within the group experiences an additional 20 ms of CDV. This is generally only a concern to CBR or VBR-rt traffic flows. This increase in CDV may cause traffic to be policed out or real time applications to experience slips.

To minimize the effect on the group traffic rate, while the delay is being reduced, the ATM cells from the group is transferred to the ATM layer at a rate of (1+1/16)*IDCR versus IDCR. In other words, the group plays out data 6.25% faster to the ATM layer during the process of delay reduction.

The amount of time the delay removal takes depends upon the amount of delay to be removed. For example, a group where 200 ms of delay is to be removed takes approximately 3 seconds for the process to complete.

While delay adjustments are being made to a group, new links cannot be added and links cannot be recovered from an error state. The S/UNI IMA 4 device rejects any requests to start a LASR procedure. However, while delay adjustments are in progress, links can be deleted or made unusable.

Group Startup Procedure

When the Add_Group Command is issued, the Group state machine enters the start-up state and start to send IMA frames on the configured Tx links.

Startup State

While in the startup state, the configured TX link state machines report the Unusable state and the Rx-link state machines report Not_In_Group. At this point, the S/UNI IMA 4 device monitors the incoming ICP cells. When ICP cells are received with the FE indicating that the Group is in Startup, the S/UNI IMA 4 device transitions to the Start-up-Ack state if the M value, the Group Symmetry, the OAM Label and IMA_ID (optional) values are acceptable. Otherwise, the S/UNI IMA 4 device transitions to the Config-Aborted State.

Config-Aborted State

When entering the Config-Aborted State, a timer is started and an interrupt is generated. The S/UNI IMA 4 stays in the config-aborted state until either:

The management plane restarts the group using the Restart_Group Command. The restart can be done with either the same parameters or with different parameters.

The config-abort timeout expires.

Startup-Ack State

When entering the Startup-Ack State, a timer is started. In the Startup-Ack state, the S/UNI IMA 4 device waits for the FE to report the Start_Up_Ack state. If the timer expires prior to the FE-reporting Start_Up_Ack (or insufficient links, blocked, or operational states), the S/UNI IMA 4 device transitions back into the Start_Up state. Otherwise, when the FE reports Start-up-Ack, the S/UNI IMA 4 device transitions to the Insufficient Links state.

Insufficient Links

When in the Insufficient Links state, the Start_LASR command should be executed to start the LASR procedure to bring up additional links

The LASR procedure starts two timers; one for the Tx links and one for the Rx links.

When the LASR procedure is complete (all links become active or timeout), if sufficient links are active, the group state machine transitions into the Operational State unless the Group is blocked.

If sufficient links are not active after the LASR procedure completes, an interrupt is generated. Since links only transition into the Active state via a LASR procedure, PM can activate a new LASR procedure with the same set of links and/or with additional links to bring up the group.

Blocked and Operational States

While in the Blocked and Operational States, the link state machines are monitored to ensure that sufficient links stay active. If insufficient links are detected active, the Group state machine transitions into the insufficient links state and stops accepting data from the ATM layer for transmission.

LASR Procedure

Links only become active as part of the LASR procedure. The add_group command automatically spawns a LASR procedure. To add links or recover links after group start-up, use the Start_LASR command.

If an LASR procedure is in progress, additional Start_LASR commands is rejected.

TX Links

When the LASR procedure starts, all Tx Links (participating in the LASR) in the unusable state or Not_In_Group state immediately transitions into the Usable state if they are not faulted or inhibited. (Note that the FE Rx Links may be reporting “Not in Group” at this point since their LIDs are not validated). Links in other states remain in the same state. If test patterns are to be transmitted on the links to test them prior to putting them in service, the Tx links should be configured to be brought up with the inhibited state set. This keeps the Tx links in the unusable state until they are released by a new LASR command (the PM_UNUSABLE status can only be cleared by a LASR).

Once the Tx Links start to report the Usable state, a programmable timer is started. When either the timer expires or all of the FE Rx links report the active state, the acceptable Tx Links transitions to the Active state. This completes the LASR for the TX links.

Rx Links

During the LASR procedure, the LIDs for the receive links are validated. Until the LIDS are validated, the RX Links report the “Not in Group” state. As the LIDS are validated, the Rx Links start to report the unusable state. This transition is not synchronized with other links in the group.

After all the receive links have their differential delay checked and have no defects (obtained IMA Frame sync) or a programmable timeout occurs, all of the accepted links transition to the usable state.

After the Rx links are reported usable, another programmable timeout is started. Once all of the links are reported TX Usable by the FE or the timeout expires, the accepted links begin reporting RX_Active. If operating in symmetrical mode, the NE TX links must be in the usable/Active state in order for the accepted links to transition into RX_Active. If some additional links have become usable since the last timeout, they skip directly from the unusable to the active state.

This completes the LASR for the Rx Links. When the LASR for both the RX and TX links is complete, the LASR procedure is complete. If the LASR completes due to a timeout and not all of the links are in the active state, an interrupt is generated (if enabled) to inform PM that the links were not brought to the active state.

Deactivating Links

Links may be brought down by either PM or by the far end. PM may declare a fault on a link, inhibit a link, or delete the link. The Far-end state changes may also cause the link to go down. This is the method of coordinating link deactivation between the NE and FE.

Far End link deactivation

If the FE Tx states transition into an unusable state, the NE Rx states go to the usable state and all data received prior to this point is played out.

If the FE Rx states transition into a not active state, the NE TX link transitions into the usable state and stops transmitting data on that link.

Near End (management) Link Deactivation

If the NE Rx link is removed from the group, the S/UNI IMA 4 device transitions to the deleted state until all previously received data is played out to the ATM layer; at which point, it deactivates itself and be removed from the round-robin.

In absence of defects, the S/UNI IMA 4 device brings down the link without loss of data.

Rate Changes

When the RIPP changes the state of a link to active, it programs the appropriate IDCC scheduler with the new rate. This is done by providing a vector that identifies the active LIDs for the group. This vector determines the number of links for the rate calculation and is then passed on to the TIMA or RDAT to indicate the LIDs to include in the round robin. The IDCC only changes its rate at IMA frame boundaries.

9.2.6 Support of IMA Test Pattern Procedure

S/UNI IMA 4 device supports the IMA test pattern procedure in both the TX direction (NE initiated) and RX direction (FE initiated).

In the TX direction, the S/UNI IMA 4 device updates the TX test control info and TX test pattern field in the outgoing ICP cells, as prompted by the relevant Update_test_ptn command. PM must take care to wait at least 2 frames in between updates to the test pattern to comply with the IMA test pattern standard. Meanwhile, the S/UNI IMA 4 device compares the RX test pattern field received in the incoming ICP cells with the TX test pattern value being transmitted, and saves the result on a per-link basis in the group context memory.

In the RX direction, the S/UNI IMA 4 device analyzes the TX test control info field in the incoming ICP cells. If the test link command field is set to “active”, the TX test pattern field in the incoming ICP cells on the selected link is copied to the RX test pattern field in the outgoing ICP cells. Otherwise the RX test pattern field in the outgoing ICP cells are filled with “0xFF”.

9.2.7 Support of Symmetric/Asymmetric Operation Modes

S/UNI IMA 4 device supports all three possible group symmetry modes: symmetric configuration and symmetric operation; symmetric configuration and asymmetric operation; asymmetric configuration and asymmetric operation.

For symmetric configuration, the number of TX and RX links in the group must be the same; for asymmetric configuration, that restriction does not apply.

The support for asymmetric/symmetric operation modes is part of the S/UNI IMA functionality. The symmetric operation mode is treated as a special case of the asymmetric operation, where the TX and RX LSM on the same physical link are inter-dependent.

9.2.8 Support of Different IMA Versions

Note that the technique used to report RX information over the Link Information fields in the ICP cells when the group is configured in the symmetrical configuration and operation mode differs in the IMA v1.1 implementations and the IMA v1.0 implementations.

The details of the differences between IMA v1.1 and IMA v1.0 can be found in appendix C of the ATM Forum IMA 1.1 specification.

The S/UNI IMA 4 device is primarily designed to be IMA v1.1 compliant. However, it may also be programmed to analyze the incoming ICP cells and generate outgoing ICP cells using IMA v1.0 style, given the group is symmetrically configured. IMA v1.0 is not supported for asymmetrical groups. Support of IMA V1.0 versus IMA v1.1 is selectable on a per-group basis.

Since the Rx link state is reported on the TX LID byte, the rx_link state is reported as unusable prior to LID validation unlike in IMA 1.1 where it is reported as “Not in Group” prior to LID validation.

9.2.9 SDRAM Interface

The S/UNI IMA 4 device uses the external SDRAM to buffer queued cells. The cell-buffer SDRAM interface permits a single device, with 1M addressing capability, for a total of 16 Mbits of storage. It has a 16-bit wide data bus, with CRC-16 checking applied on a per-cell basis. Each cell takes up 64 bytes of memory. The CRC-16 is applied to words 0 through 30. If an error occurs, an interrupt is sent to the microprocessor, and the cell is sent to the ATM layer anyway. Note that a 64 Mbit or 256 Mbit SDRAM may also be used if 16 Mbit SDRAM is not available. This does not increase the differential delay tolerance of the device beyond 1024 cells. The hookup would be identical to the 16 Mbit hookup diagram.

The following diagram shows the cell storage map with the 64-byte memory boundary.

Figure 24 Cell Storage Map

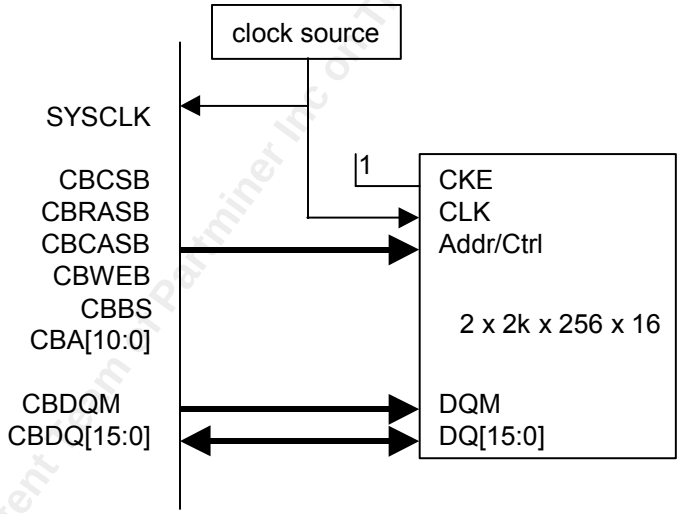
Word #	15 Bits 0	
Write Pointer + 0	DCB Status[15:0]	
1	DCB Status[31:16]	
2	Header1	Header2
3	Header3	Header4
4	Reserved	

5	STATUS	Reserved
6	Payload1	Payload2
…		
…		
28	Payload45	Payload46
29	Payload47	Payload48
30	Reserved	
31	CRC-16	

The clock source drawn in the following diagrams must be completely skew aligned between the S/UNI IMA 4 device and the SDRAM clock input pins.

The following diagram shows the configuration supported:

Figure 25 16 Mbit SDRAM



There are three processes, all of which are arbitrated by the SDRAM arbiter, that access the cell buffer SDRAM:

- The RDAT, which reads and writes cell and status information. The granularity of access by the RDAT is a concatenated 1-cell write, 1-cell read. Either the write or the read may not be performed, depending on the RDAT's requirements.

- The microprocessor interface, which performs diagnostic reading or writing of 64 bytes of data. This data is aligned with the cell data. This access is allowed only when the SDRAM is placed in Diagnostic mode and is provided both to enable SDRAM testing and to initialize the SDRAM. While it is in diagnostic mode, all regular accesses from the RDAT are disabled.

- The refresh controller, which has a programmable refresh rate.

The SDRAM interface performs the initialization sequence for the SDRAM. This sequence is triggered by the SDRAM enable bit in the SDRAM control register. The sequence programs the SDRAM with a CAS latency of 3, sequential access, write burst mode, and a burst length of 8. Applications should ensure that sufficient time is provided between SDRAM powerup and when this enable bit is set.

9.3 Link FIFOs

In the transmit direction, per link FIFOs exist to provide an elastic store to ensure proper operation. The number of cells in the FIFO at any particular time varies as a function of the CDV introduced by the insertion of stuff cells and ICP cells, the effects of the physical link interface, and the smoothing of data from the ATM layer for group level CDV. During operation, these FIFOs are loaded a cell at a time and emptied in a TDM fashion. The Link FIFOs in the transmit direction are 9 cells deep.

In the receive direction, the link FIFOs serve as an interface between the TDM domain and the ATM cell domain. Cells are gathered in the FIFO for each link and then burst out to the external memory by the RDAT. The Link FIFOs in the receive direction are 2 cells deep.

A diagnostic loopback capability is provided to loopback data from the receive link FIFOs to the transmit link FIFO; this loops back all links when enabled.

9.4 TC Layer

9.4.1 TX TC Layer (TTTC)

The TX TC layer (TTTC) performs the TC layer functions. These functions consist of optional HEC generation, optional payload scrambling, and cell-rate decoupling through physical layer (idle) cell insertion.

This function removes data byte by byte from the per-link FIFOs as required to provide data to the physical layer function. When the physical layer function needs a byte of data, it requests data from the (TTTC). The TTTC then reads a byte of data from the per-link FIFO. If that byte is the first byte of a cell and the logical channel FIFO is empty, the TTTC formats the next 53 bytes as a physical layer (idle) cell. If the byte is the fifth byte of a cell, the byte is optionally overwritten by the HCS. The HCS is a CRC-8 ($x^8 + x^2 + x + 1$) calculation over the first 4 octets of the ATM cell header. In accordance with ITU-T Recommendation I.432.1, the coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before insertion (coset addition is not configurable). The sixth through 53rd bytes may be scrambled by a $x^{43}+1$ self-synchronous scrambler.

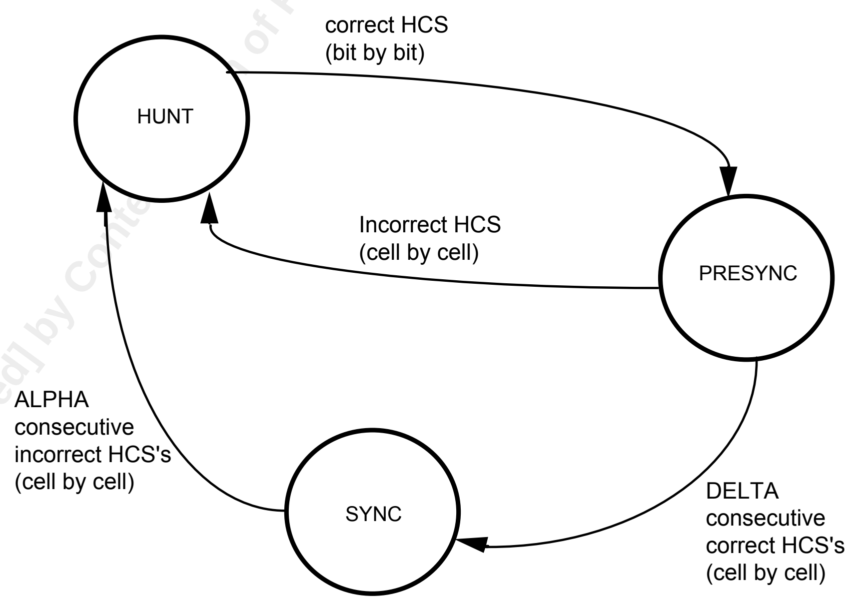
Note: Since the Link FIFOs are cell based, an underrun cannot happen in the middle of a cell.

9.4.2 Rx TC Layer (RTTC)

The Rx TC (RTTC) layer implements HCS cell delineation, payload descrambling, idle cell filtering and header error detection to recover valid ATM cells. These functions are performed in accordance with ITU-T Recommendation I.432.1.

Cell delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the ATM cell header. The HCS is a CRC-8 ($x^8 + x^2 + x + 1$) calculation over the first 4 octets of the ATM cell header. In accordance with ITU-T Recommendation I.432.1, the coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result (coset addition is not configurable). When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. The cell delineation circuitry performs a sequential bit-by-bit hunt for a correct HCS sequence. This state is referred to as the HUNT state. When a correct HCS is found, a particular cell boundary is assumed and the PRESYNC state is entered. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication, then an incorrect HCS should be received within the next DELTA cells and the delineation state machine falls back to the HUNT state. If an incorrect HCS is not found in this PRESYNC period, then a transition to the SYNC state is made, cell delineation is declared, and all non-idle cells with a correct HCS are passed on. In the SYNC state, synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. If this happens, a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in Figure 26.

Figure 26 Cell delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the cell delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6.

The loss of cell delineation (LCD) alarm is declared after a programmable threshold of incorrect cells occurs while not in the SYNC state. The threshold is set by the LCD Count Threshold register. The threshold has a default value of 104, which translates to 28 ms at 1.55 Mbps. All idle cells may be filtered out and not passed to the IMA sub-layer. They are identified as cells containing all-zero VPI and VCI fields and a one in the CLP bit. Optionally, unassigned cells (like idle cells except CLP is a zero) may also be filtered. Note that these should not be filtered for IMA links.

All cells with an incorrect HCS octet may optionally be dropped. These cells can also be preserved and tagged as errored. Preservation of HEC errored cells is required for correct operation of IMA. Failure to preserve the cells leads to increased numbers of OIF violations and data misordering. Header correction is not implemented.

For IMA operation, there are two unique features: the first is optionally passing cells with errored HEC; the second results in passing cells during OCD and LCD. This is to enable the IMA to perform a fast recovery from error conditions. An OCD event results in a loss of IMA frame sync to ensure differential delay checking is performed.

9.5 Line Side Physical Layer

9.5.1 TX Clock/Data (TCAS)

The S/UNI IMA 4 device supports up to 4 two-pin Clock/Data serial interfaces to interface with standard framers. Each link is independent and has its own associated clock. To enable easier support of CTC, a common clock is also supported using the CTSCLK pin. The S/UNI IMA 4 device responds to the active edge of each transmit clock by generating a single bit.

When the external framer needs to insert transmission overhead (such as framing bits) into the data stream provided by the S/UNI IMA 4 device, the framer must gap the transmit clock provided to the S/UNI IMA 4 device. This prevents the S/UNI IMA 4 device from outputting data bits during the overhead bit period(s).

The Transmit Channel Assigner block (TCAS) processes up to 4 virtual links. Data for all links is sourced from a single byte-serial stream from the TC layer. For each link, the TCAS provides a holding register. The TCAS also performs parallel-to-serial conversion to form a bit-serial stream. When multiple links are in need of data, TCAS requests data from upstream blocks on a fixed priority basis with link TSDATA[0] having the highest priority and link TSDATA[3] the lowest.

Links containing a T1 or an E1 stream may be channelized. Data at each time-slot may be assigned either: (1) to be sourced from the virtual link or (2) to be unassigned. This mechanism of assigning timeslots enables support of fractional links. The link clock should only be active during time-slots 1 to 24 of a T1 stream and inactive during the frame bit. Similarly, the clock is only active during time-slots 1 to 31 of an E1 stream and inactive during the framing byte. The first bit of time-slot 1 of a channelized link is identified by noting the absence of the clock and its re-activation. With knowledge of the transmit link and time-slot identity, the TCAS performs a table look-up to identify which timeslots are in use.

Links may also be unchannelized. In that case, all data bytes on that link belong to the virtual link. The TCAS performs a table look-up to identify the link to which a data byte belongs using only the outgoing link identity, as no time-slots are associated with unchannelized links. The link clock is only active during bit-times containing data to be transmitted; it is inactive during bit-times that are to be ignored by the downstream devices, such as framing and overhead bits.

9.5.2 Rx Clock/Data (RCAS)

The S/UNI IMA 4 provides up to 4 two-pin Clock/Data serial interfaces for interconnecting to T1/E1 framers. Each link is independent and has its own associated clock. For each link, the data is sent through a serial to parallel conversion to form data bytes. The data bytes are multiplexed, in byte serial format, for delivery to the TC layer. In the event where multiple streams have accumulated a byte of data, multiplexing is performed on a fixed priority basis, with link #0 having the highest priority and link #3 the lowest.

For the clock and data interface, the framer must gap the clock for all framing bits for T1 and for the framing byte for E0.

Links containing a T1 or an E1 stream may be channelized. For channelized links, the link clock is only active during time-slots 1 to 24 of a T1 stream; it is inactive during the frame bit. Similarly, the clock is only active during time-slots 1 to 31 of an E1 stream and inactive during the framing bytes. Each time-slot may be independently configured to be provisioned (contain valid data) or unprovisioned. The RCAS performs a table lookup to assign the provisioned time-slots to a virtual link. After the selected timeslots are grouped into a virtual link, virtual links are referred to as links. This look-up should be used to remove byte 16 of the E1 frame, since byte 16 contains signaling data not ATM data and also implements a fractional T1 or E1. The first bit of time-slot 1 of a channelized link is identified by noting the absence of the clock and its re-activation.

Links may also be unchannelized. In this mode, all data is assumed to be valid ATM data. The link clock is only active during bit times containing data to be processed and inactive during bits that are to be ignored by the RCAS, such as framing and overhead bits.

The RCAS provides diagnostic line-side loopback that is selectable on a per-channel basis. When a channel is in diagnostic loopback, data on the received links originally destined for that channel is ignored. Transmit data of that channel is substituted in its place.

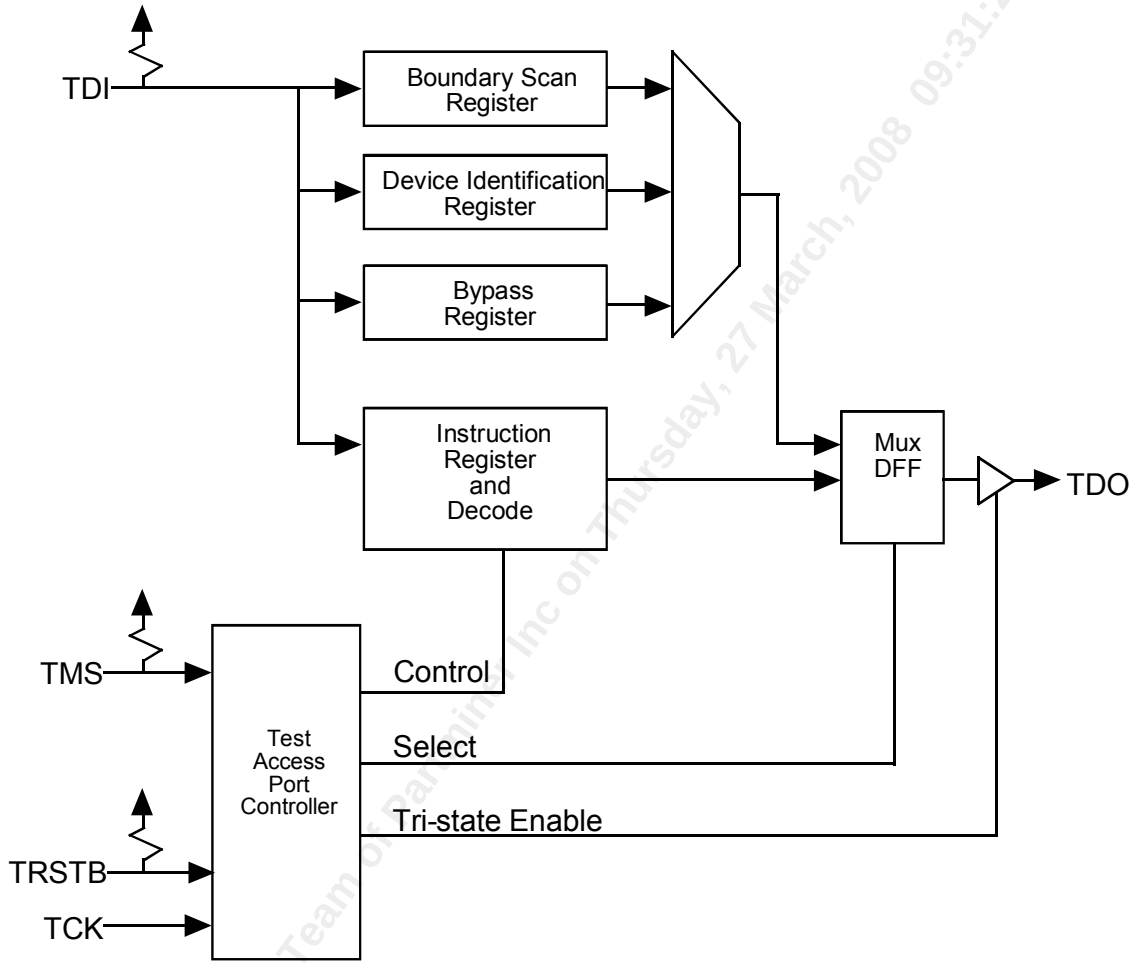
9.6 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI IMA 4 identification code is 173400CD hexadecimal.

9.6.1 JTAG Support

The S/UNI IMA 4 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins; TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input directs the TAP controller through its states. The basic boundary scan architecture is shown next.

Figure 27 Boundary Scan Architecture



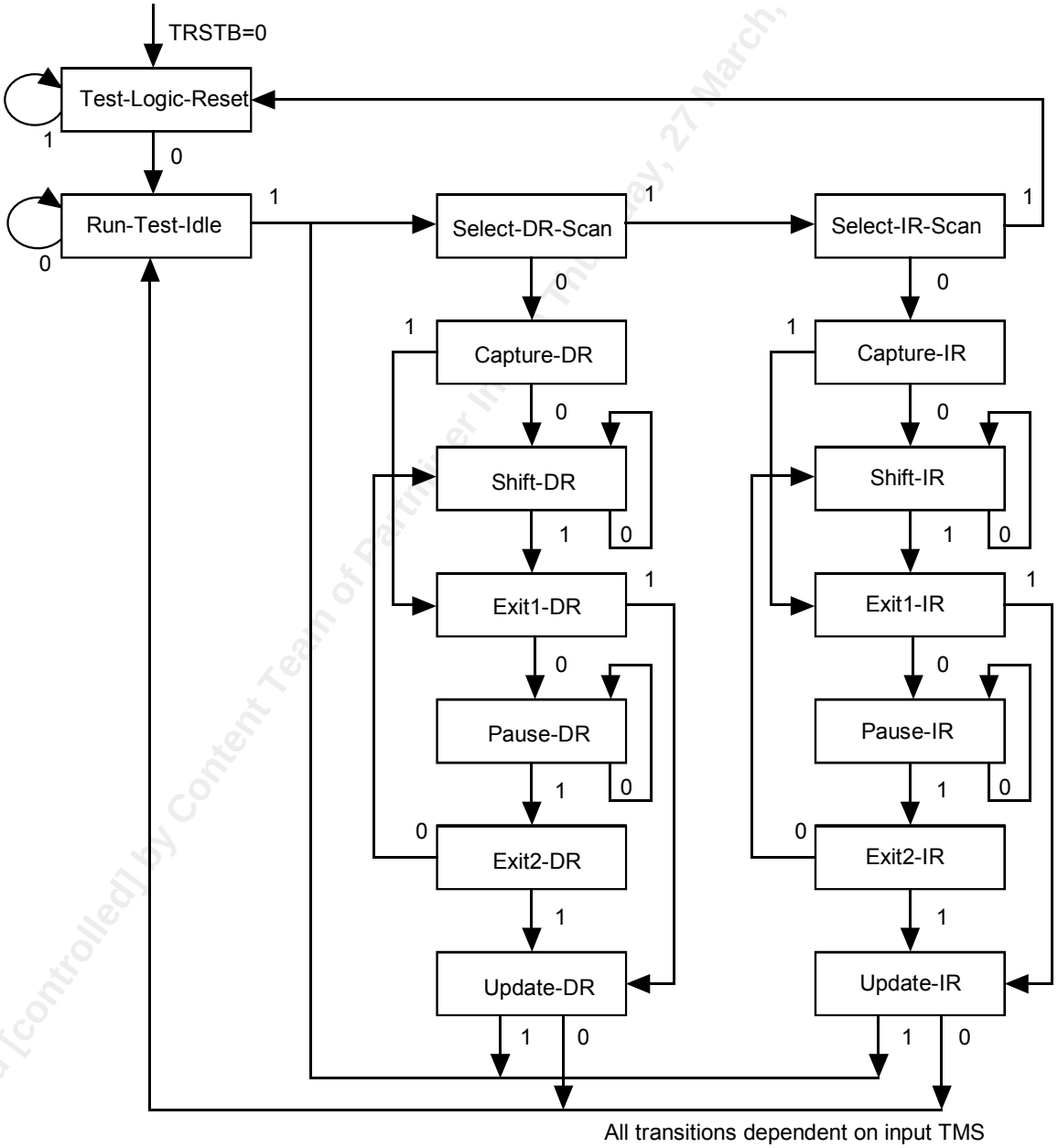
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register, and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block selects the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

9.6.2 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described next.

Figure 28 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state disables the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state executes tests.

Capture-DR

The capture data register state loads parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state shifts the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state loads a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state loads the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state shifts both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state loads a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

9.6.3 Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction bypasses the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction connects the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction tests the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

9.7 Microprocessor Interface

The Microprocessor Interface Block provides the interrupt logic and an interface to normal-mode registers contained within the design blocks. The normal mode registers are required for normal operation.

9.7.1 Mapping and Link Identification

Within the clock/data interface, the external links are mapped to a contiguous space identified as Virtual Links. To support multiple fractional TC flows on a single external signal, a mapping splits a single channelized external signal into multiple Virtual Links. At the per-link FIFOs, the clock/data Virtual Link naming convention is replaced 1:1 with the Physical Link naming convention.

The S/UNI IMA 4 device processes 4 Physical Links, numbered 0 to 3. The Clock and Data Interface uses 4 External Signal pins, which are mapped to 4 Virtual Links. The 4 streams to/from the line interfaces are referred to a Physical Links elsewhere inside the device.

Clock/Data

Within the Clock and Data Interface, the external signals RSCLK/TSCLK and RSDATA/TSDATA are identified by sequential numbers from 0 to 3.

Within the RCAS/TCAS, these 4 external signals are mapped to a contiguous space identified as Virtual Links 0 through 3. To support multiple fractional TC flows on a single external signal, RCAS/TCAS mapping splits a single channelized external signal into multiple Virtual Links. At the per-link FIFOs, the RCAS/TCAS Virtual Link naming convention is replaced 1:1 with the Physical Link naming convention.

IMA

Within the IMA sublayer, mapping is performed between the physical link Ids and the Any-PHY/UTOPIA L2 virtual PHY address. This mapping can be a one-to-one relationship as for TC connections or it may be a many-to-one relationship as for an IMA group.

The physical link to Virtual PHY mapping is independent in the RX and TX directions.

The selection of the RX VPHY ID in Any-PHY or single port UTOPIA L2 mode is unconstrained as this ID exists only as a prepend. In multiple port UTOPIA L2 mode, the RX VPHY ID must be a unique value between 0 and 3 for each flow.

The selection of the TX VPHY ID is limited by the following rule:

All groups must have a unique value between 0 and 7.

Note:

- The actual address used on the Any-PHY bus to access a particular channel is a combination of the TX VPHY ID (bits 2:0), which TCAEN bit is set (bits 6:3), and the Tx Any-PHY Address Config Reg(bits 15:7).

9.7.2 Interrupt Driven Error/Status Reporting

The interrupt logic has several layers. The top layer of the interrupt logic, the Master Interrupt Register, indicates from which block the interrupt came. Once the block is determined the processor can access the appropriate block to determine the interrupt cause.

TC Layer Interrupts

The TC layer sources 4 different interrupts that are reported through a FIFO structure. As each interrupt occurs it is placed into a FIFO along with a Link Identifier to uniquely identify the link. The error conditions reported through this structure include HEC Errors, Loss of Cell Delineation (LCD) state change, Out of Cell Delineation (OCD) state change, and Receive Link FIFO overflow. To determine the actual states of LCD and OCD it is necessary to query the individual link status. If this FIFO overflows, it is necessary to query the status of all links to retrieve accurate state information.

IMA Interrupts

The IMA sub-layer sources four interrupts: RIPP_INTR, TIMA_INTR, RDAT_INTR, and ICP_CELL_AVL. The RIPP_INTR indicates that either a status change or an error occurred on an IMA group. The RIPP Interrupt status FIFO contains the groups that have enabled conditions active. The RIPP Interrupt status FIFO is managed so that each group only ever has a single entry in the FIFO. To facilitate interrupt processing, a RIPP command is provided to gather all interrupts and status for a group and all of the links within the group in one snapshot.

TIMA_INTR provides information that a link FIFO has overflowed. During normal operations, this only happens when: (1) the TIMA is misconfigured or (2) the rate difference between the clocks in an IMA group is greater than the maximum tolerance. To determine which link has experienced a problem, the TIMA Link FIFO Overflow Status registers should be read.

RDAT_INTR indicates either: (1) that cells were dropped due to Any-PHY/UTOPIA congestion or (2) that TC group cells were dropped due to FIFO overflow. To determine the cause of the interrupt, the RDAT Master Interrupt register should be read.

ICP_CELL_AVL indicates that an ICP cell is available in the ICP cell buffer. To enable diagnostics, the capability to forward a group's ICP cells to the microprocessor is provided. When a cell is forwarded to the microprocessor, it is placed in the ICP cell buffer and the interrupt is triggered. As new ICP cells arrive, they overwrite the ICP cell buffer unless the buffer is locked for reading. Once the ICP cell buffer is locked, further ICP cells are not forwarded until the ICP cell buffer is unlocked. This trace can be enabled on a per-group basis.

Miscellaneous Interrupts

MISC_INTR indicates that an interrupt condition exists in the Miscellaneous Interrupt register. These bits are read-and-clear and usually indicate that transitory conditions have occurred, such as parity errors, SDRAM CRC errors, interrupt FIFO overflows, and UTOPIA L2 interface errors.

9.7.3 Registers

The Register Memory Map in Table 5 shows where the normal mode registers are accessed. The resulting register organization is split into sections: Master configuration registers, TC Layer, Clock/Data Interface and IMA Sublayer registers.

On power up, the S/UNI IMA 4 requires configuration. For proper operation, register configuration is necessary to program addresses for the Any-PHY ports, enable the SDRAM, configure the Line interface, and choose IMA or TC mode for each link/group. By default, interrupts are not enabled.

The Line-side-access defaults to a disabled state; this results in all line side output pins being tristated. When the Clock/Data line mode is chosen, the pins are enabled.

Table 5 Register Memory Map

Address	Register
0x000 – 0x05E	**Master Configuration and Interrupts**
0x000	Global Reset
0x002	Global Configuration
0x004	JTAG ID (MSB)
0x006	JTAG ID (LSB)
0x008	Master Interrupt Register
0x00A	Miscellaneous Interrupt Register
0x00C	RTTC Interrupt FIFO
0x00E	Reserved
0x010	Master Interrupt Enable Register
0x012	Miscellaneous Interrupt Enable Register
0x014	TC Interrupt Enable Register
0x016-0x01E	Reserved
0x020	Transmit Any-PHY/UTOPIA Cell Available Enable
0x022	Receive UTOPIA Cell Available Enable
0x024	Receive Any-PHY/UTOPIA Config Register (RXAPS_CFG)
0x026	Transmit Any-PHY/UTOPIA Config Register (TXAPS_CFG)
0x028	Transmit Any-PHY Address Config Register (TXAPS_ADD_CFG)

Address	Register
0x02A-0x03E	Reserved
0x040	SDRAM Configuration
0x042	SDRAM Diagnostics
0x044	SDRAM Diag Burst RAM Indirect Access
0x046	SDRAM Diag Indirect Burst Ram Data LSB
0x048	SDRAM Diag Indirect Burst Ram Data MSB
0x04A	SDRAM DIAG WRITE CMD 1
0x04C	SDRAM DIAG WRITE CMD 2
0x04E	SDRAM DIAG READ CMD 1
0x050	SDRAM DIAG READ CMD 2
0x052-0x05E	Reserved
0x060-0x07E	**TC Layer**
0x060	TTTC Indirect Link Control Register
0x062	TTTC Indirect Link Configuration Register
0x064-0x06E	TTTC Reserved
0x070	RTTC Indirect Link Control Register
0x072	RTTC Indirect Link Configuration Register
0x074	RTTC Indirect Link Interrupt and Status Register
0x076	RTTC Indirect Link HCS Error Count Register
0x078	LCD Count Threshold
0x07A-0x0FE	Reserved
0x100-0x1FE	**Clock/Data Interface**
0x100	RCAS Indirect Link and Time-slot Select
0x102	RCAS Indirect Channel Data
0x104	RCAS Framing Bit Threshold
0x106	RCAS Channel Disable
0x108 – 0x13E	RCAS Reserved
0x140 – 0x14E	RCAS Link #0 to Link #3 Configuration
0x180	TCAS Indirect Link and Time-slot Select
0x182	TCAS Indirect Channel Data
0x184	TCAS Framing Bit Threshold
0x186	TCAS Idle Time-slot Fill Data
0x188	TCAS Channel Disable Register
0x18A – 0x1BE	TCAS Reserved
0x1C0 – 0x1CE	TCAS Link #0 to Link #3 Configuration
0x200-0x3FE	**IMA Sublayer**
0x200	RIPP Control
0x202	RIPP Indirect Memory Access Control

Address	Register
0x204-0x206	RIPP Indirect Memory Data Register Array
0x208	Delay Configuration Register
0x20C	RIPP Timer Tick Configuration Register
0x20E	Group Timeout Register #1
0x210	Group Timeout Register #2
0x212	Tx Link Timeout Register
0x214	Rx Link Timeout Register
0x216	RIPP Interrupt Status Register
0x218	RIPP Group Interrupt Enable Register
0x21A	RIPP Tx Link Interrupt Enable Register
0x21C	RIPP Rx Link Interrupt Enable Register
0x220-0x22C	RIPP Command Register
0x22E	Command Read Data Control Register
0x230	ICP Cell Forwarding Status Register
0X232	ICP Cell Forwarding Control Register
0x240-0x29E	RIPP Command Data Register Array
0x2C0-0x2DE	Forwarding ICP Cell Buffer
0x300	RDAT Indirect Memory Command
0x302	RDAT Indirect Memory Address
0x304	RDAT Indirect Memory Data LSB
0x306	RDAT Indirect Memory Data MSB
0x308	RDAT Configuration
0x30A	Receive ATM Congestion Status LSB
0x30C	Receive ATM Congestion Status MSB
0x30E	Receive TC Overrun Status
0x310	RDAT Master interrupt Status
0x312	Receive ATM Congestion Interrupt Enable LSB
0x314	Receive ATM Congestion Interrupt Enable MSB
0x316	RDAT Master Interrupt Enable
0x318-0x31E	Reserved
0x320	TIMA Indirect Memory Command
0x322	TIMA Indirect Memory Address
0x324	TIMA Indirect Memory Data LSB
0x326	TIMA Indirect Memory Data MSB
0x328	TX Link FIFO Overflow Status
0x336	TIMA Interrupt Enable
0x340	TXIDCC Indirect Link Access
0x342	TXIDCC Indirect Link Data Register #1

Address	Register
0x344-0x34E	Reserved
0x350	RXIDCC Indirect Link Access
0x352	RXIDCC Indirect Link Data Register #1. (For RxIDCC Link Table) / RXIDCC Indirect Link Data Register (LSB) (For RxIDCC Group Table)
0x354	RXIDCC Indirect Link Data Register (MSB) (For RxIDCC Group Table)
0x356-0x364	Reserved
0x366	DLL Control Status
0x368-0x3FF	Reserved

For all register accesses, CSB must be low.

10 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI IMA 4. Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI IMA 4 device to determine the programming state of the block.
3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect S/UNI IMA 4 operation unless otherwise noted.
5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI IMA 4 operates as intended, reserved-register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

10.1 Global Registers

Register 0x000: Global Reset

Bit	Type	Function	Default
15	R/W	RESET	1
14	RO	BIST_DONE	X
13:7		Unused	0
6:4	RO	TYPE[2:0]	000
3:0	RO	ID[3:0]	0001

ID[3:0]

The ID bits can be read to provide a binary number indicating the S/UNI IMA 4 feature version. These bits are incremented only if features are added in a revision of the chip.

TYPE[2:0]

The TYPE bits can be read to distinguish the S/UNI IMA 4 device from the other members of the S/UNI IMA family of devices. The S/UNI IMA 4 device is identified by a value of "000".

BIST_DONE

The BIST_DONE indicates when the internal ram initialization is complete. Once the ram initialization is complete, the internal rams may be accessed. Prior to BIST_DONE transitioning to a "1", any internal ram accesses are ignored.

RESET

The RESET bit implements a software reset for the entire S/UNI IMA 4 device. If the RESET bit is a logic 1, the entire S/UNI IMA 4 device is held in reset except for the microprocessor interface. While in reset, the only register that is write accessible is the Global Reset register. This bit is not self-clearing; therefore, a logic 0 must be written to bring the S/UNI IMA 4 device out of reset. Holding the S/UNI IMA 4 device in a reset state effectively puts it into a low power, stand-by mode. A hardware reset sets the RESET bit, thus asserting the software reset.

Register 0x002: Global Configuration

Bit	Type	Function	Default
15:8		Unused	0
7	R/W	CHAN_CD	0
6	R/W	MAX_DCB_DEPTH	0
5	R/W	CTSCLK_SEL	0
4	R/W	LINE_EN	0
3	R/W	LINE_LOOP	0
2	R/W	U2U_LOOP	0
1	R/W	LINE_MODE	0
0		Reserved	0

LINE_MODE

Enables the selected line interface mode.

0) Disabled (all line Interface signals are tristated) .

1) Clock/Data Mode.

U2U_LOOP

When set, all cells received by the Any-PHY/UTOPIA Interface are sent back out to the Any-PHY/UTOPIA (regardless of single- or multi-addressing mode). For proper operation, if the Receive interface is in multi address UTOPIA mode, the Transmit Interface must also be in UTOPIA Mode.

0) Any-PHY/UTOPIA in normal mode.

1) Any-PHY/UTOPIA in remote loopback mode.

LINE_LOOP

When set, all cells received by the Clock/Data interface are sent back out to the Clock/Data interface.

0) Line Side in normal mode.

1) Line Side remote loopback mode.

LINE_EN

When LINE_EN is set, line side traffic flow is enabled. This configuration bit should be written to a one after the LINE_MODE is configured and prior to normal operation.

CTSCLK_SEL

When CTSCLK_SEL is set and LINE_MODE="1", the CTSCLK pin is used as the clock for all Transmit Serial Line Clocks. When CTSCLK_SEL is not set and LINE_MODE="1", the TSCLK[3:0] pins are used for all Transmit Serial Line Clocks.

MAX_DCB_DEPTH

This indicates the number of cells that can be stored for a single link in the external SDRAM. This determines the number of bits the RDAT uses for the read and write pointers. This bit should be set to a '1' for the S/UNI IMA 4 device.

0) 256 cells per link.

1) 1024 cells per link.

CHAN_CD

This indicates that the channelized cell delineation may be used. Channelized cell delineation results in faster cell delineation since an octet-by-octet search is performed instead of a bit by bit search. This option may only be used when operating the clk/data interface in channelized mode. If any links are operating in unchannelized mode, this bit may not be set.

0) Use bit by bit search for cell delineation. (Safe mode).

1) Use octet or nibble search for cell delineation (only should be set if operating with channelized line interface for all links).

Register 0x004: JTAG ID (MSB)

Bit	Type	Function	Default
15:0	RO	JTAGID(31:16)	0x1734

JTAGID[31:16]

The JTAG ID register (JTAGID[31:16]) of the S/UNI IMA 4 device. The JTAG ID is the same as the one read by the JTAG port.

Register 0x006: JTAG ID (LSB)

Bit	Type	Function	Default
15:0	RO	JTAGID(15:0)	0x00CD

JTAGID[15:0]

The JTAG ID register (JTAGID[15:0]) of the S/UNI IMA 4 device. The JTAG ID is the same as the one read by the JTAG port.

10.2 Master Interrupt Registers

Register 0x008: Master Interrupt Register

Bit	Type	Function	Default
15:9	RO	Unused	0
8	RO	TC_INTR	0
7	RO	MISC_INT	0
6:4	RO	Reserved	0
3	RO	ICP_CELL_AVL	0
2	RO	RDAT_INTR	0
1	RO	TIMA_INTR	0
0	RO	RIPP_INTR	0

This register is the top of the Interrupt Tree. It indicates which lower level interrupt registers have interrupts pending. Note that the respective bits remain set as long as the underlying condition remains active.

RIPP_INTR

When set, there is an interrupt pending from the RIPP block. Read the RIPP_INTR_FIFO located in Register 0x216 to determine the group that caused the interrupt. This bit indicates current status and only clears when RIPP_INTR_FIFO is empty. On read:

0) No interrupt pending from the RIPP block.

1) Interrupt pending from the RIPP block.

TIMA_INTR

When set, there is an interrupt pending from the TIMA block. Read the TIMA_OVERFLOW_REG located in register 0x328 to determine the cause of the interrupt. This bit indicates current status and only clears when no interrupt conditions remain in TIMA_OVERFLOW_REG. On read:

0) No interrupt pending from the TIMA block.

1) Interrupt pending from the TIMA block.

RDAT_INTR

When set, there is an interrupt pending from the RDAT block. Read the RDAT_INTR_STATUS_REG located in register 0x310 to determine the cause of the interrupt. This bit indicates current status and only clears when no interrupt conditions remain in RDAT_INTR_STATUS_REG. On read:

0) No interrupt pending from the RDAT block.

1) Interrupt pending from the RDAT block.

ICP_CELL_AVL

When set, it indicates that a new ICP Cell is available in the RIPP Forwarding ICP cell buffer. The RIPP Forwarding ICP cell buffer can be used to extract ICP cells for a group. This bit is cleared when register 0x230 ICP Cell Forwarding Status is read.

0) No ICP cell is available.

1) An ICP cell is available in the RIPP Forwarding ICP buffer.

MISC_INTR

When set, it indicates that an interrupt is pending in the Miscellaneous Interrupt Register located in register 0x00A. This bit indicates current status, and only clears when no interrupt conditions exist in the Miscellaneous Interrupt register. On read:

0) No Miscellaneous interrupt pending.

1) Miscellaneous interrupt pending.

TC_INTR

When set, indicates that a TC layer is pending in the Receive TC Interrupt FIFO. This bit indicates current status and only clears when the Receive TC Interrupt FIFO is empty.

0) No TC Interrupts in the Receive TC Interrupt FIFO.

1) TC Interrupts are present in the Receive TC Interrupt FIFO.

Register 0x00A: Miscellaneous Interrupt Register

Bit	Type	Function	Default
15:5	R2C	Reserved	0
4	R2C	TC_INTR_FOVR_ERR	0
3	R2C	SDRAM_CRC_ERR	0
2	R2C	TX_UTOP_CELLXFERR	0
1	R2C	TX_UTOP_PAR_ERR	0
0	R2C	RX_UTOP_XFR_ERR	0

This register collects the miscellaneous interrupts. These interrupt bits are cleared on read. If any bit in this register is set and is enabled, the MISC_INT bit is set in the Master Interrupt register.

RX_UTOP_XFR_ERR

When set, it indicates that the Receive Any-PHY/UTOPIA Interface was requested to send a cell when it did not have one available. This condition is a protocol error in the Receive Any-PHY/UTOPIA bus. This bit is cleared on read.

0) No protocol error occurred.

1) The Rx Any-PHY/UTOPIA interface was requested to send a cell when a cell was not available.

TX_UTOP_PAR_ERR

When set, it indicates that the Transmit ANY-PHY/UTOPIA Interface experienced a parity error. This bit is cleared on read.

0) No parity error occurred on the TX ANY-PHY/UTOPIA interface.

1) A parity error occurred on the TX ANY-PHY/UTOPIA interface.

TX_UTOP_CELLXFERR

When set, it indicates that the Transmit ANY-PHY/UTOPIA Interface experienced a second TSX asserted prior to a complete cell being transferred. This indicates that a runt cell was transferred to the S/UNI IMA 4; this is protocol violation. Also, in AnyPHY mode, this interrupt signal is triggered if the TENB is deasserted prior to a complete cell is transferred since pausing is not supported in Any-PHY mode.

0) No cell transfer error occurred on the TX ANY-PHY/UTOPIA interface.

1) A cell transfer error occurred on the TX ANY-PHY/UTOPIA interface.

SDRAM_CRC_ERR

When set, it indicates that a SDRAM CRC Error occurred when a cell buffer was read from SDRAM. This bit is cleared on read.

0) No SDRAM CRC error occurred.

1) SDRAM CRC error occurred.

TC_INTR_FOVR_ERR

When set, it indicates that the RTTC Interrupt FIFO overflowed and status reporting information was lost. To determine the status of the physical Links, the physical-link status for each link must be polled. This bit is cleared on read.

0) The RTTC Interrupt FIFO has not overflowed.

1) The RTTC Interrupt FIOF has overflowed.

Register 0x00C: Receive TC Interrupt FIFO

Bit	Type	Function	Default
15	RO	FIFO_BUSY	0
14	RO	FIFO_NOT_EMPTY	0
13:6	RO	Unused	0
5:4	RO	LINK_ID	X
3	RO	HCS_ERR	X
2	RO	LCD_ERR	X
1	RO	FOVR_ERR	X
0	RO	OOCD_ERR	X

OOCD_ERR

When set, it indicates that the 0x074: OOCDV bit changed state on the link indicated by LINK_ID. This bit is valid only when FIFO_NOT_EMPTY is set and FIFO_BUSY is not set.

0) The OOCDV bit did not change state for the link identified by LINK_ID.

1) The OOCDV bit changed state for the link identified by LINK_ID.

FOVR_ERR

When set, it indicates that the RTTC Link FIFO overflowed on link LINK_ID. This bit is valid only when FIFO_NOT_EMPTY is set and FIFO_BUSY is not set.

0) RTTC Link FIFO did not overflow on the Link identified by LINK_ID.

1) RTTC Link FIFO overflowed on the Link identified by LINK_ID.

LCD_ERR

When set, it indicates that the 0x074:LCDV bit changed state on the Link identified by LINK ID. This bit is valid only when FIFO_NOT_EMPTY is set and FIFO_BUSY is not set.

0) The LCDV bit did not change state on the Link identified by LINK ID.

1) The LCDV bit changed state on the Link identified by LINK ID.

HCS_ERR

When set, it indicates that a Header Check Sequence Error occurred on the Link identified by LINK ID. This bit is valid only when FIFO_NOT_EMPTY is set and FIFO_BUSY is not set.

0) No HCSE error occurred on the Link identified by LINK ID.

1) HCSE error occurred on the Link identified by LINK ID.

LINK_ID[1:0]

Indicates the Physical-Link number associated with the error. This field indicates the link number (0 to 3). This field is valid only when FIFO_NOT_EMPTY is set and FIFO_BUSY is not set.

FIFO_NOT_EMPTY

Indicates that the FIFO is not empty and that the data read is valid. This bit is valid only when FIFO_BUSY is not set.

0) FIFO empty, data is not valid.

1) FIFO not empty, data is valid.

FIFO_BUSY

Indicates that the FIFO is in the process of retrieving the next entry. The Busy bit is generally cleared within 4 sysclk cycles from the previous read of this field. While this bit is set, the other contents of this register are invalid.

Register 0x010: Master Interrupt Enable Register

Bit	Type	Function	Default
15:9	R/W	Reserved	0
8	R/W	TC_INTR_EN	0
7	R/W	MISC_INTR_EN	0
6 :4	R/W	Reserved	0
3	R/W	ICP_CELL_AVL_EN	0
2	R/W	RDAT_INTR_EN	0
1	R/W	TIMA_INTR_EN	0
0	R/W	RIPP_INTR_EN	0

The enable-bits control the corresponding interrupt bits in the Master Interrupt Register. When an enable-bit is set to logic 1, the corresponding error event causes INTB to go active.

Register 0x012: Miscellaneous Interrupt Enable Register

Bit	Type	Function	Default
15:5	RO	Unused	0
4	R/W	TC_INTR_FOVR_ERR_EN	0
3	R/W	SDRAM_CRC_ERR_EN	0
2	R/W	TX_UTOP_CELLXFERR_EN	0
1	R/W	TX_UTOP_PAR_ERREN	0
0	R/W	RX_UTOP_XFR_ERR_EN	0

The enable-bits control the corresponding interrupt bits in the Miscellaneous Interrupt register. When an enable-bit is set to logic 1, the corresponding error event causes the MISC_INT bit to be set in the Master Interrupt Register.

Register 0x014: TC Interrupt Enable Register

Bit	Type	Function	Default
15:4	RO	Unused	0
3	R/W	HCS_ERR_EN	0
2	R/W	LCD_ERR_EN	0
1	R/W	FOVR_ERR_EN	0
0	R\W	OOCD_ERR_EN	0

The enable-bits provide a global enable for the corresponding interrupt bits in the RTTC Interrupt FIFO. If an enable-bit is not set, the corresponding error event does not cause an entry to be written into the TC_INTR FIFO. When an enable-bit is set to logic 1, the corresponding error event, if enabled for the link, causes an entry to be written into the TC INTR FIFO.

10.3 UTOPIA Interface Registers

These registers control the configuration of the UTOPIA interface.

Register 0x020: Transmit Any-PHY/UTOPIA Cell Available Enable

Bit	Type	Function	Default
15:11	R	Unused	0
10:0	R/W	TCAEN[10:0]	0

TCAEN[10:0]

The TCAEN[10:0] bits control the response to polling on the Any-PHY/UTOPIA Transmit port. The TCAEN[10:0] bits can be used to select which group of 8 virtual PHY's the device should respond to. Only one bit should be set to enable a range of 8 addresses; for example, setting TCAEN[0] enables addresses 0 through 7, setting TCAEN[9] enables addresses 72 through 79, and setting TCAEN[10] enables addresses 80 through 83. If a disabled PHY address is polled, TCA remains high impedance. Similarly, PHY selection is ignored and no cell is transferred to the S/UNI IMA 4 when a disabled PHY is addressed. This is typically used to allow more than one slave device to share the Transmit UTOPIA bus or to preserve addresses on the Any-PHY bus. Disabling all traffic to the Any-PHY/UTOPIA input port is achieved by setting all TCAEN[10:0] bits to logic 0.

Register 0x022: Receive UTOPIA Cell Available Enable

Bit	Type	Function	Default
15:4		Unused	0
3:0	R/W	RCAEN[3:0]	0

RCAEN[3:0]

The RCAEN[3:0] bits control the response to polling on the receive UTOPIA port when in UTOPIA Level 2 Multi-Address mode. The RCAEN[3:0] bits can be used to select which group of 8 addresses the S/UNI IMA 4 device responds to. Only one bit should be set; for example, setting RCAEN[0] enables addresses 0 through 7 and setting RCAEN[3] enables addresses 24 through 30. S/UNI IMA 4 device drives the RCA output signal either high or low, when polled with an address corresponding to a set RCAEN bit, depending on the Group FIFO status.

If a disabled PHY address is polled, RCA remains high impedance. Similarly, PHY selection is ignored and no cell is transferred from the S/UNI IMA 4 device when a disabled PHY is addressed. This is typically used to allow more than one slave device to share the Receive UTOPIA bus. Disabling all traffic to the UTOPIA input port while in Multi-PHY mode is achieved by setting all RCAEN[3:0] bits to logic 0. This field is ignored when in Any-PHY or Single Port UTOPIA mode.

Register 0x024: Receive Any-PHY/UTOPIA Config Reg (RXAPS_CFG)

Bit	Type	Function	Default
15	R/W	RA_ENABLE	0
14:13	R	Unused	0
12:8	R/W	RA_DEVID[4:0]	0
7:6	R	Unused	0
5	R/W	RA_HECUDF	0
4	R/W	RA_PREPEND	0
3	R/W	RA_16_BIT_MODE	0
2	R/W	RA_EVEN_PAR	0
1	R/W	RA_ANY-PHY_EN	0
0	R/W	RA_UTOP_MODE	0

This register controls the receive side configuration of the Any-PHY/UTOPIA Interface

RA_UTOP_MODE

Selects the operating mode for the receive-side interface. This bit is ignored when ANY-PHY_EN is set:

0) UTOPIA-2 Single Address Slave with address prepend:

– Virtual PHY address is prepended as byte/word if RA_HECUDF = 0

– Virtual PHY address appears in HECUDF byte/word if RA_HECUDF = 1

1) UTOPIA-2 Multi-Address Slave.

RA_ANY-PHY_EN

Enables Any-PHY mode for receive side interface.

0) UTOPIA mode. (Use RA_UTOP_MODE for UTOPIA type).

1) Any-PHY mode.

RA_EVEN_PAR

Determines the generated parity across data bytes/words sourced by the receive interface.

0) Odd parity.

1) Even parity.

RA_16_BIT_MODE

When set, the Any-PHY/UTOPIA receive side interface operates in 16-bit mode.

0) 8-bit mode.

1) 16-bit mode.

RA_PREPEND

When set, two bytes are prepended to cells on the Any-PHY/UTOPIA bus. This prepend is zero. This prepend is independent of the address prepend used for Any-PHY mode.

0) No additional bytes are prepended to the cells.

1) Two additional bytes are prepended to the cells.

RA_HECUDF

This bit is only valid in Single Address UTOPIA Mode.

0) Place the virtual PHY ID in a prepend.

1) Place the virtual PHY ID in the HECUDF.

RA_DEVID[4:0]

This field provides the device ID that is used for polling and selection in the Any-PHY mode or in the Single Address UTOPIA Mode. When the address presented on the Any-PHY/UTOPIA RADR Interface pins matches this address, the S/UNI IMA 4 device responds to polls. The S/UNI IMA 4 device is selected for a cell transfer when the address on RADR at the last cycle that RENB is high matches RA_DEVID.

RA_ENABLE

Enables the Receive Any-PHY/UTOPIA interface. Prior to this bit being set, all outputs are tristated and all inputs are ignored on the Interface.

Register 0x026: Transmit Any-PHY/UTOPIA Config Reg (TXAPS_CFG)

Bit	Type	Function	Default
15	R/W	TA_ENABLE	0
14:5	R	Unused	0
4	R/W	TA_PREPEND	0
3	R/W	TA_16_BIT_MODE	0
2	R/W	TA_EVEN_PAR	0
1	R/W	TA_ANY-PHY_EN	0
0	R/W	Unused	0

This register controls the transmit-side configuration of the Any-PHY/UTOPIA Interface

TA_ANY-PHY_EN

Enables Any-PHY mode for the transmit side interface:

0) UTOPIA-2 Multi-Address Slave.

1) Any-PHY mode.

TA_EVEN_PAR

Determines the checked parity across data bytes/words received by the Any-PHY/UTOPIA transmit Interface.

0) Odd parity.

1) Even parity.

TA_16_BIT_MODE

When set, the TX Any-PHY/UTOPIA interface operates in 16-bit mode.

0) 8-bit mode.

1) 16-bit mode.

TA_PREPEND

When set, a single 2-byte prepend is expected on the Any-PHY/UTOPIA transmit interface. This prepend is independent of the address prepend used for Any-PHY mode. The prepend is ignored, but the capability is provided to enhance interoperability.

0) No two-byte prepend is expected.

1) Two-byte prepend is expected.

TA_ENABLE

Enables the Transmit Any-PHY/UTOPIA interface. Prior to this bit being set, all outputs are tristated and all inputs are ignored on the Interface.

Register 0x028: Transmit Any-PHY Address Config Register (TXAPS_ADD_CFG)

Bit	Type	Function	Default
15:7	R/W	CFG_ADDR_MSB	0
6:0	R/W	Unused	0

CFG_ADDR_MSB[15:7]

These bits contain the configured slave address used for Any-PHY polling and selection in the transmit direction. Depending on the mode of the Any-PHY/UTOPIA interface different bits of this field are used.

In Any-PHY 16-bit mode device selection, the upper nine bits of the prepended address on the Any-PHY bus is compared with CFG_ADDR_MSB to select the device. The lower seven bits of the prepended address on the Any-PHY bus are not compared with this field, and are used only to route each cell to the targeted virtual PHY FIFO.

In Any-PHY 8-bit mode device selection, the MSB of the prepended address octet on the Any-PHY bus is compared with CFG_ADDR_MSB[7] to select the device. The lower seven bits of the prepended address on the Any-PHY bus are not compared with this field, and are used only to route each cell to the targeted virtual PHY FIFO.

In both 8-bit and 16-bit Any-PHY device polling, when the TCSB pin is low during the proper clock cycle, the device drives the TPA output signal with the virtual PHY FIFO status of the virtual PHY identified by the TADR[6:0] address pins, if that virtual PHY is enabled with its corresponding Register 0x020 TCAEN[10:0] bit. CFG_ADDR_MSB[15:11] are not used during device polling.

In UTOPIA Level 2 mode, this register is not used. To disable UTOPIA transmit ports, the Transmit Any-PHY/UTOPIA Cell-Available Enable register is provided.

10.4 SDRAM Registers

Register 0x040: SDRAM Configuration

Bit	Type	Function	Default
15:12		Unused	0
11:1	R/W	REF_RATE [10:0]	0
0	R/W	SDRAM_EN	0

This register configures and enables the SDRAM interface.

SDRAM_EN

The SDRAM_EN enables the SDRAM interface. A transition from 0 to 1 starts the SDRAM self-initialization procedure. This procedure takes 70 SYSCLK cycles to complete. Note that no other SDRAM accesses are allowed during this period.

SDRAM_EN is provided to ensure that the power-up of the SDRAM is completed before the SDRAM self-initialization sequence is started. The power-up time is controlled by SDRAM_EN. Typically, this must be at least 200 us. When SDRAM_EN = '0', no SDRAM accesses occurs and the chip does not operate properly.

0) SDRAM accesses are disabled.

1) SDRAM accesses are enabled.

REF_RATE[10:0]

Defines the SYSCLK divide-down factor to determine the SDRAM refresh rate. The REF_RATE must be configured prior to setting the SDRAM_EN. A zero value effectively disables refresh. The value in this register must be programmed to a value greater than 100 (0x64).

For Example, if the SDRAM requires 4K refreshes in 64 ms with a SYSCLK of 50 MHz, the REF_RATE should be programmed to:

$$REF\_RATE = \frac{Sys\_Clk}{(\#\_of\_refresh)/(time\_period)} = \frac{50MHZ}{\left(4096/64ms\right)} = 781 = 0x30D$$

Register 0x042: SDRAM Diagnostics

Bit	Type	Function	Default
15:1	N/A	Unused	0
0	R/W	DIAG_MODE	0

DIAG_MODE

The SDRAM Diagnostic Mode (DIAG_MODE) allows the microprocessor to access the SDRAM for testing and initialization. While in diagnostic mode, the normal SDRAM accesses are inhibited and the S/UNI IMA 4 device does not operate properly.

0) Diagnostic access is disabled and the S/UNI IMA 4 device operates normally.

1) Diagnostic access is enabled. The SDRAM may be accessed via indirect access as described in section 10.4 using registers 0x44-0x50.

Register 0x044: SDRAM DIAG Burst RAM Indirect Access

Bit	Type	Function	Default
15	RO	BR_BUSY	0
14:5	N/A	Unused	N/A
4:0	R/W	BR_ADDR[4:0]	0

Writing to this register triggers either a write to the Burst Write RAM or a read from the Burst Read RAM. See 12.6.1 for further details.

BR_ADDR [4:0]

The Burst-ram address (BR_ADDR [4:0]) indicates the RAM address to be configured or interrogated. The Burst ram is divided into 2 segments: the first is Burst Write RAM, which stores data to be loaded into the External SDRAM; the second is the Burst Read RAM, which collects data read from the External SDRAM. The access to the burst-write RAM is a write operation while the access to the burst-read RAM is a read operation. See Figure 29 for the format of the Burst RAM.

- 0x00-0x0F: Burst-Write RAM
- 0x10-0x1F: Burst-Read RAM

BR_BUSY

The indirect access command bit (BR_BUSY) reports the progress of an indirect access. BR_BUSY is set high when the register is written to trigger an indirect access; it stays high until the access is complete. Once the access is complete, the BR_BUSY signal is reset. This register should be polled: (1) to determine when data from an indirect read operation is available in the SDRAM Indirect Burst RAM Data register or (2) to determine when a new indirect write operation may start.

Register 0x046: SDRAM DIAG Indirect Burst Ram Data LSB

Bit	Type	Function	Default
15:0	R/W	BR_DATA_LSB	0

This register should not be written while the BR_BUSY bit is set in the SDRAM Burst RAM Indirect Access register.

BR_DATA_LSB

The BR_DATA_LSB represents either: (1) the least significant 16 bits of the data to be written to internal memory or (2) the least significant 16 bits of the read data resulting from the previous read operation. The read data is not valid until after the BR_BUSY bit is cleared.

Register 0x048: SDRAM DIAG Indirect Burst RAM Data MSB

Bit	Type	Function	Default
15:0	R/W	BR_DATA_MSB	0

This register should not be written while the BR_BUSY bit is set in the SDRAM Burst RAM Indirect Access register.

BR_DATA_MSB

The BR_DATA_MSB represents either: (1) the most significant 16 bits of the data to be written to internal memory or (2) the most significant 16 bits of the read data resulting from the previous read operation. The read data is not valid until after the BR_BUSY bit is cleared.

The following explains the Burst RAM accessed by the indirect access.

Burst RAM: The microprocessor has access to the external SDRAM for testing and initialization. There is a 64-byte cell buffer for writing to the external SDRAM and a 64-byte cell buffer for storing data read from the external SDRAM.

Figure 29 shows the format of the cell in the Burst RAM.

Figure 29 Burst RAM Format

Word #	31 Bits 0
0x00	Burst Write (0)
0x01	Burst Write (1)
…	
…	
0x0F	Burst Write(15)
0x10	Burst Read (0)
0x11	Burst Read (1)
…	
…	
0x1F	Burst Read(15)

Register 0x04A: SDRAM DIAG WRITE CMD 1

Bit	Type	Function	Default
15:0	R/W	WR_BUFFER_ADDR[15:0]	0

WR_BUFFER_ADDR[15:0]

Indicates the lower 16 bits of the addresses of the cell buffer to write. SDRAM DIAG Write CMD 2 provides the upper address bit and triggers the burst access to happen.

Register 0x04C: SDRAM DIAG WRITE CMD 2

Bit	Type	Function	Default
15	R	WRBUSY	0
14:1		Unused	
0	R/W	WR_BUFFER_ADDR[16]	0

A write to the SDRAM DIAG WR_CMD 2 register triggers a transfer of data from the Write Burst Ram to the external SDRAM. The lower bits of the address of the cell buffer in the external SDRAM are given in the SDRAM DIAG WRITE CMD 1 register.

WR_BUFFER_ADDR[16]

Indicates the upper bit of the addresses of the cell buffer to write. SDRAM DIAG Write CMD 1 provides the lower address bits.

WRBUSY

The Write Busy bit (WRBUSY) reports the progress of the write access to SDRAM. WRBUSY is set high when this register is written; this triggers the SDRAM access; it stays high until the access is complete. At which point, WRBUSY is set low. This register should be polled to determine when a new diagnostic write operation may commence. While the WRBUSY bit is set, no indirect accesses to the write burst ram should be performed.

Register 0x04E: SDRAM DIAG READ CMD 1

Bit	Type	Function	Default
15:0	R/W	RD_BUFFER ADDR[15:0]	0

RD_BUFFER_ADDR[15:0]

Indicates the lower 16 bits of the addresses of the cell buffer to read. SDRAM DIAG Read CMD 2 provides the upper address bit and triggers the burst access to happen.

Register 0x050: SDRAM DIAG READ CMD 2

Bit	Type	Function	Default
15	R	RDBUSY	0
14:1		Unused	
0	R/W	RD_BUFFER ADDR[16]	

A write to the SDRAM DIAG READ CMD 2 register triggers a transfer of data from the external SDRAM to the Read Burst Ram. The lower bits of the address of the cell buffer in the external SDRAM are given in the SDRAM DIAG READ CMD 1 register.

RD_BUFFER_ADDR[16]

Indicates the upper bit of the addresses of the cell buffer to read. SDRAM DIAG READ CMD 1 provides the lower address bits.

RDBUSY

The Read Busy bit (RDBUSY) reports the progress of the read access to SDRAM. RDBUSY is set high when this register is written; this triggers the SDRAM access; it stays high until the access is complete. At which point, RD_BUSY is set low. This register should be polled to determine when the data is available in the Burst Ram.

10.5 TC Layer Registers

Register 0x060: TTTC Indirect Link Control Register

Bit	Type	Function	Default
15	R	LBUSY	0
14	R/W	LRWB	0
13:2		Reserved	0
1:0	R/W	LINK[1:0]	0

This register provides the link number used to access the TTTC link provision RAM. Writing to this register triggers an indirect link register access.

LINK[1:0]

LINK[1:0] specifies the link to be configured or interrogated in the indirect link access. Only 4 links are available. Valid values for the LINK field should range from 0x0 to 0x3.

LRWB

The link indirect access control bit (LRWB) selects between either a configure (write) or interrogate (read) access to the link-context RAM. Writing a logic 0 to LRWB triggers an indirect write operation. Data to be written is taken from the Indirect Link Data registers. Writing a logic 1 to LRWB triggers an indirect read operation. The read data can be found in the Indirect Link Data registers.

LBUSY

The indirect link access status bit (LBUSY) reports the progress of an indirect access A write to the Indirect Link Address register triggers an indirect access and sets LBUSY to logic 1; it remains a logic 1 until the access is complete. This register should be polled to determine either: (1) when data from an indirect read operation is available in the Indirect Link Data registers or (2) when a new indirect write operation may commence. The LBUSY is not expected to remain at logic 1 for more than 86 REFCLK cycles.

Register 0x062: TTTC Indirect Link Configuration Register

Bit	Type	Function	Default
15:3		Unused	0
2	R/W	DHCS	0
1	R/W	Reserved	0
0	R/W	DSCR	0

This register contains either: (1) data read from the TTTC link provision RAM after an indirect Link read operation or (2) data to be inserted into the TTTC link provision RAM in an indirect Link write operation.

DSCR

The indirect scrambling disable bit (DSCR) configures scrambling. The scramble disable bit to be written to the link provision RAM, in an indirect link write operation, must be set up in this register before triggering the write. When DSCR is logic 1, scrambling is disabled. When DSCR is logic 0, the 48-byte payload is scrambled. DSCR reflects the value written until the completion of a subsequent indirect link-read operation.

DHCS

The Disable HCS (Header Check Sequence) bit (DHCS) configures the insertion of the HCS in the fifth byte of the cell. The value of DHCS to be written to the link provision RAM, in an indirect link write operation, must be set up in this register before triggering the write. When DHCS is logic 0, the CRC-8 calculation over the first four bytes of the cell overwrites the fifth byte. When DHCS is logic 1, the fifth byte of the cell passes through unmodified. DHCS reflects the value written until the completion of a subsequent indirect link-read operation.

Register 0x070: RTTC Indirect Link Control Register

Bit	Type	Function	Default
15	R	LBUSY	0
14	R/W	LRWB	0
13	R/W	DRHCSE	0
12:2		Reserved	0
1:0	R/W	LINK[1:0]	0

This register provides the link number used to access the RTTC link provision RAM. Writing to this register triggers an indirect link-register access.

LINK[1:0]

LINK[1:0] specifies the link to be configured or interrogated in the indirect link access. Only 4 links are available. Valid values for the LINK field should range from 0x0 to 0x3.

DRHCSE

Disable Reset of the HCS Error Count (DRHCSE) disables automatic reset of the HCS Error Counter (HCSERR). When the bit is set to logic 0, automatic reset of the HCS Error Counter is enabled. If an indirect read is initiated (i.e., CRWBs written with logic 1) with DRHCSE logic 0, the HCS Error Counter is reset to zero upon completion of the indirect read. When the DRHCSE bit is set to logic 1, automatic reset of the HCS Error Counter is disabled.
An indirect read results in the interrupt status, as well as the HCSERR count, being read (and possibly cleared). In this situation, the DRHCSE bit is useful for separating interrupt processing from HCSERR count accumulation because it can disable the HCSERR count reset when querying for interrupts.

LRWB

The Link indirect access control bit (LRWB) selects between a configure (write) or interrogate (read) access to the Link context RAM. Writing a logic 0 to LRWB triggers an indirect write operation. Data to be written is taken from the Indirect Link Data registers. Writing a logic 1 to LRWB triggers an indirect read operation. The read data can be found in the Indirect Link Data registers.

LBUSY

The indirect access status bit (LBUSY) reports the progress of an indirect access. A write to the Indirect Link Address register triggers an indirect access and sets LBUSY to logic 1. LBUSY stays high until the access is completed. At which point, LBUSY is set low. This register should be polled to determine either: (1) when data from an indirect read operation is available in the Indirect Data register or (2) when a new indirect write operation may start.

Register 0x072: RTTC Indirect Link Configuration Register

Bit	Type	Function	Default
15:11		Unused	
10	R/W	LCDOOCDPASS	0
9	R/W	HCSPASS	0
8	R/W	UNASSPASS	0
7	R/W	IDLEPASS	0
6	R/W	DDSCR	0
5	R/W	DHCSADD	0
4	R/W	DDELIN	0
3	R/W	OOCDE	0
2	R/W	HCSE	0
1	R/W	FOVRE	0
0	R/W	LCDE	0

This register contains either: (1) data read from the RTTC Link provision RAM after an indirect Link read operation or (2) data to be inserted into the RTTC Link provision RAM in an indirect Link write operation.

The bits to be written to the RTTC Link provision RAM, in an indirect Link write operation, must be set up in this register before triggering the write. The bits reflect the value written until the completion of a subsequent indirect Link read operation.

The reset state of the bits enables standard ATM cell processing as stipulated in ITU-T Recommendation I.432.1

LCDE

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set to logic 1, the interrupt is enabled.

FOVRE

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set to logic 1, the interrupt is enabled.

HCSE

The HCSE bit enables the generation of an interrupt due to the detection of an HCS error. When HCSE is set to logic 1, the interrupt is enabled.

OOCDE

The OOCDE bit enables the generation of an interrupt due to a change in the cell delineation state. When OOCDE is set to logic 1, the interrupt is enabled.

DDELIN

The indirect disable delineate enable bit (DDELIN) configures the TC processor to perform cell delineation and header error detection on the incoming data stream. When DDELIN is set to logic 0, the cell alignment is established and maintained on the incoming data stream. When DDELIN is set to logic 1, the RTTC does not perform any processing on the incoming stream, but passes data through transparently.

DDSCR

The DDSCR bit controls the descrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set to logic 1, cell payload descrambling is disabled. When DDSCR is set to logic 0, payload descrambling is enabled.

DHCSADD

The DHCSADD bit controls the addition of the coset polynomial, x6+x4+x2+1, to the HCS octet prior to comparison. When DHCSADD is a logic 0, the polynomial is added, and the resulting HCS is compared. When DHCSADD is a logic 1, the polynomial is not added, and the unmodified HCS is compared. This bit should be set to 0 for normal operation.

IDLEPASS

The IDLEPASS bit controls the function of the idle cell filter. When IDLEPASS is written with a logic 0, all idle cells (i.e., the first four bytes of a cell: x00, x00, x00, and x01) are filtered out. When IDLEPASS is logic 1, idle cells are passed to the Receive IMA Data Processor. For IMA links, this bit must be set to a logic 1 to allow for proper IFSM operation (the Receive IMA Data Processor drops cells according to the configuration of IMA_IDLE_FWD_EN and the current defects and RX LSM). For TC-only links, the Receive IMA Data Processor forwards idle cells. If this is undesirable, then IDLEPASS must be configured to a logic 0.

UNASSPASS

When UNASSPASS is written with a logic 0, all unassigned cells (i.e., the first four bytes of a cell: x00, x00, x00, and x00) are filtered out. When UNASSPASS is logic 1, unassigned cells are passed to the Receive IMA Data Processor. For IMA links, this bit must be set to a logic 1 to allow for proper IFSM operation (the device forwards unassigned cells). For TC-only links, the Receive IMA Data Processor forwards unassigned cells. If this is undesirable, then UNASSPASS must be configured to a logic 0.

HCSPASS

The HCSPASS bit controls the dropping of cells based on the detection of an HCS error. When HCSPASS is logic 0, cells containing an HCS error are dropped. When HCSPASS is a logic 1, cells are passed to the Receive IMA Data Processor regardless of errors detected in the HCS. For IMA links, this bit must be set to a logic 1 to allow for proper IFSM operation. All HCS errored cells are dropped by the Receive IMA Data Processor (regardless of the mode). For TC-only links, the HCSPASS bit has no effect.

LCDOOCDPASS

The LCDOCDPASS bit controls the dropping of cells based on the detection of an out of cell delineation and loss of cell delineation. When LCDOOCDPASS is logic 0, cells containing an OOCD error and an LCD error are dropped. When LCDOOCDPASS is a logic 1, cells are passed to the Receive IMA Data Processor regardless of errors detected in the OOCD and LCD. For IMA links, this bit must be set to a logic 1 to allow for proper IFSM operation (the Receive IMA Data Processor drops these cells). For TC-only links, the Receive IMA Data Processor drops cells with OCD, but does not drop good cells received during LCD after OCD has exited. Therefore, for TC-only mode, LCDOCDPASS should be set to a logic 0.

Register 0x074: RTTC Indirect Link Interrupt and Status Register

Bit	Type	Function	Default
15:6		Unused	
5	R	OOCDV	1
4	R	LCDV	0
3	R	OOCDI	0
2	R	HCSI	0
1	R	FOVRI	0
0	R	LCDI	0

This register contains data read from the RTTC Link provision RAM after an indirect read operation.

LCDI

The LCDI bit is set high when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register. Note that the state of the Receive TC Interrupt FIFO is independent of this bit (clearing on read does not affect the FIFO behavior).

FOVRI

The FOVRI bit is set to logic 1 when a FIFO overrun occurs. This bit is reset immediately after a read to this register. Note that the state of the Receive TC Interrupt FIFO is independent of this bit (clearing on read does not affect the FIFO behavior).

HCSI

The HCSI bit is set high when an HCS error is detected. This bit is reset immediately after a read to this register. Note that the state of the Receive TC Interrupt FIFO is independent of this bit (clearing on read does not affect the FIFO behavior).

OOCDI

The OOCDI bit is set high when the logical Link enters or exits the SYNC state. The OOCDV bit indicates if the logical Link is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register. Note that the state of the Receive TC Interrupt FIFO is independent of this bit (clearing on read does not affect the FIFO behavior).

LCDV

The LCDV bit gives the Loss of Cell Delineation state. When LCD is logic 1, an out of cell delineation (OCD) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LCD is logic 0, no OCD has persisted for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[7:0] register bits in the LCD Count Threshold register.

OOCDV

The OOCDV bit is high when the logical Link is not currently in the SYNC state.

Register 0x076: RTTC Indirect Link HCS Error Count Register

Bit	Type	Function	Default
15:0	R	HCSERR[15:0]	0

This register contains data read from the RTTC Link provision RAM after an indirect read operation.

HCSERR[15:0]

The HCSERR[7:0] bits indicate the number of HCS error events that occurred during the last accumulation interval. When the number of HCS error events during the last accumulation interval exceeds 64K, the HCSERR[15:0] retains a value of FFFFH until the next accumulation interval (HCSERR[15:0] is reset).

Register 0x078: LCD Count Threshold

Bit	Type	Function	Default
15:8		Unused	
7:0	R/W	LCDC[7:0]	0x68

LCDC[7:0]

The LCDC[7:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[7:0].

The default value of LCDC[7:0] is 104; this translates to 28 ms at 1.5 Mbps.

10.6 Line Clock/Data Interface

Register 0x100: RCAS Indirect Link and Time-slot Control Register

Bit	Type	Function	Default
15	R	BUSY	X
14	R/W	RWB	0
13:10	R/W	Unused	0
9:8	R/W	LINK[1:0]	0
7:5		Unused	X
4:0	R/W	TSLOT[4:0]	00

This register provides the link number and time-slot number used to access the time-slot provision RAM. Writing to this register triggers an indirect register access.

TSLOT[4:0]

The indirect time-slot number bits (TSLOT[4:0]) indicate the time-slot to be configured or interrogated in the indirect access. For a channelized T1 link, time-slots 1 to 24 are valid. For a channelized E1 link, time-slots 1 to 31 are valid. For unchannelized links, only time-slot 0 is valid.

LINK[1:0]

The indirect link number bits (LINK[1:0]) select amongst the 4 receive links to be configured or interrogated in the indirect access.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the timeslot provision RAM. The address to the timeslot provision RAM is constructed by concatenating the TSLOT[4:0] and LINK[1:0] bits. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the PROV, the VLDLBEN, and the VLINK[6:0] bits of the Indirect Link Data register. Writing a logic one to RWB triggers an indirect read operation. Addressing of the RAM is the same as in an indirect write operation. The data read can be found in the PROV, the VLDLBEN, and the VLINK[1:0] bits of the Indirect Link Data register.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written; this is done to trigger an indirect access, and stays high until the access is complete. At which point, BUSY is set low. This register should be polled to determine either: (1) when data from an indirect read operation is available in the Indirect Data register or (2) when a new indirect write operation may commence.

Register 0x102: RCAS Indirect Link Data Register

Bit	Type	Function	Default
15:10	R	Unused	X
9	R/W	VLDLBEN	0
8	R/W	PROV	0
7:2		Unused	X
1:0	R/W	VLINK[1:0]	00

The RCAS Timeslot Provision RAM maps either timeslots from a physical link or an entire physical link to a Virtual Link. It also provisions timeslots/links and enables Diagnostic Loopback.

This register contains either: (1) the data read from the RCAS Timeslot Provision RAM after an indirect read operation or (2) the data to be inserted into the RCAS Timeslot Provision RAM during an indirect write operation.

VLINK[1:0]

VLINK[1:0] is the Virtual Link to which this RCAS LINK/TSLOT is mapped. Valid values are 0x0 to 0x3. For proper operation, timeslots from multiple physical links cannot be mapped to the same VLINK.

After an indirect read operation is completed, VLINK[1:0] reports the virtual link number read from the RCAS Timeslot Provision RAM. The Virtual Link number to be written to the RCAS Timeslot Provision RAM in an indirect write operation must be set up in this register before triggering the write. VLINK[1:0] reflects the value written until the completion of a subsequent indirect read operation.

PROV

The indirect provision enable bit (PROV) reports the timeslot provision enable flag read from the timeslot provision RAM after an indirect read operation is completed. The provision enable flag to be written to the timeslot provision RAM in an indirect write operation must be set up in this register before triggering the write. When PROV is set high, the current receive data byte is processed as part of the virtual link (as indicated VLINK[1:0]). When PROV is set low, the current time-slot does not belong to any virtual link and the receive data byte is ignored. PROV reflects the value written until the completion of a subsequent indirect read operation.

VLDLBEN

When the indirect virtual link based diagnostic loopback enable bit VLDLBEN=1, the current receive data byte is over-written by a data byte retrieved from the loopback FIFO of the Virtual Link as indicated by VLINK[1:0]. When VLDLBEN=0, the current receive data byte is processed normally.

VLDLBEN reports the value read from the RCAS Timeslot Provision RAM after an indirect read operation is completed. VLDLBEN must be set up in this register before triggering an indirect write. VLDLBEN reflects the value written until the completion of a subsequent indirect read operation.

Register 0x104: RCAS Framing Bit Threshold

Bit	Type	Function	Default
15:7	R	Unused	X
6:0	R/W	FTHRES[6:0]	0x3F

This register contains the threshold used by the clock-activity monitor to detect framing bits/bytes.

FTHRES[6:0]

The framing bit threshold bits (FTHRES[6:0]) contain the threshold used by the clock activity monitor to detect for the presence of framing bits. A counter in the clock-activity monitor increments at each REFCLK and is cleared by a rising edge of the RSCLK. When the counter exceeds the threshold given by FTHRES[6:0], a framing bit/byte is detected. FTHRES[6:0] should be set as a function of the REFCLK period and the expected gapping width of RSCLK during framing bits/bytes.

For E1 only device operation, the following equation should be used to determine the acceptable range of values for FTHRES:

$$\left(\frac{REFCLK.Freq}{RSCLK.E1.Freq}\right)*1.5 < FTHRES < \left(\frac{REFCLK.Freq}{RSCLK.E1.Freq}\right)*7$$

For T1 device operation and mixed T1 and E1 device operation (T1 requirements are more rigorous), the following equation should be used to determine FTHRES:

$$FTHRES \approx \left[\left(\frac{REFCLK.Freq}{RSCLK.T1.Freq}\right)*1.5\right] - 3$$

For example, for T1 or mixed T1 and E1, with a REFCLK.Freq = 19.44MHz, FTHRES[6:0] = 15.

Register 0x106: RCAS Link Disable

Bit	Type	Function	Default
15	R	VLDIS	0
14:2		Unused	X
1:0	R/W	DVLINK[1:0]	0

This register allows the squelching of output data from a particular virtual link.

DVLINK[1:0]

The disable virtual link bits (DVLINK[1:0]) specify the virtual link whose output data from the RCAS are to be squelched. When VLDIS is set high, the virtual link specified by DVLINK[1:0] is disabled, even if the virtual link is provisioned.

VLDIS

When set high, the virtual link disable bit (VLDIS) squelches valid data on the output of RCAS for the virtual link indicated by DVLINK[1:0].

Register 0x140- 0x14E: RCAS Link #0 to Link #3 Configuration

Bit	Type	Function	Default
15:3	R	Unused	X
2	R/W	Reserved	0
1	R/W	E1	0
0	R/W	CEN	0

This register configures operational modes of receive link #0 to link #3 (RSDATA[N]/ RSCLK[N] where $0 \leq N \leq 3$).

CEN

The channelize enable bit (CEN) configures link #N for channelized operation.

When CEN=1, RSCLK[N] must be gapped during the T1 framing bit and during the E1 framing byte. The data bit on RSDATA[N] that is clocked in by the first rising edge of RSCLK[N] after an extended low period is considered to be the most significant bit of time-slot 1.

When CEN=0, link #N is unchannelized. The E1 register bit is ignored. RSCLK[N] must be gapped during non-data bits. All data bits are treated as a contiguous stream with arbitrary byte alignment.

E1

The E1 frame structure select bit (E1) configures link #N for channelized E1 operation when CEN is set high. RSCLK[N] is held low during the FAS and NFAS framing bytes. The data bit on RSDATA[N] that is associated with the first rising edge of RSCLK[N] after an extended low period is considered to be the most significant bit of time-slot 1. Link data is present at time-slots 1 to 31. When E1 is set low and CEN is set high, link #N is configured for channelized T1 operation. RSCLK[N] is held low during the framing bit. The data bit on RSDATA[N] that is associated with the first rising edge of RSCLK[N] after an extended low period is considered to be the most significant bit of time-slot 1. Link data is present at time-slots 1 to 24. E1 is ignored when CEN is set low.

Register 0x180: TCAS Indirect Link and Time-slot Control Register

Bit	Type	Function	Default
15	RO	Busy	X
14	R/W	RWB	0
13:10		Unused	X
9:8	R/W	LINK[1:0]	0
7:5		Unused	X
4:0	R/W	TSLOT[4:0]	0

This register provides the link number and time-slot number used to access the timeslot provision RAM. Writing to this register triggers an indirect register access and transfers the contents of the Indirect Link Data register to an internal holding register.

TSLOT[4:0]

The indirect time-slot number bits (TSLOT[4:0]) indicate the time-slot to be configured or interrogated in the indirect access. For a channelized T1 link, time-slots 1 to 24 are valid. For a channelized E1 link, time-slots 1 to 31 are valid. For unchannelized links, only time-slot 0 is valid.

LINK[1:0]

The indirect link number bits (LINK[1:0]) select amongst the 4 transmit links to be either configured or interrogated in the indirect access.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the timeslot provision RAM. The address to the timeslot provision RAM is constructed by concatenating the TSLOT[4:0] and LINK[1:0] bits. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the PROV and the VLINK[1:0] bits of the Indirect Data register. Writing a logic one to RWB triggers an indirect read operation. Addressing of the RAM is the same as in an indirect write operation. The data read can be found in the PROV and the VLINK[1:0] bits of the Indirect Link Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written to trigger an indirect access, and stays high until the access is complete. At which point, BUSY is cleared (low). Alternatively, BUSY is set high when TCAS first comes out of reset until the RAM is initialized. This register should be polled to determine either: (1) when data from an indirect read operation is available in the Indirect Data register or (2) when a new indirect write operation may start. Any indirect operation that is initiated while BUSY is still high is corrupted.

Register 0x182: TCAS Indirect Link Data Register

Bit	Type	Function	Default
15:9		Unused	X
8	R/W	PROV	0
7:2		Unused	X
1:0	R/W	VLINK[1:0]	0

The TCAS Timeslot Provision RAM maps Virtual Links to either timeslots in a physical link or to an entire physical link. It also provisions timeslots.

This register contains either: (1) the data read from the TCAS Timeslot Provision RAM after an indirect read operation or (2) the data to be inserted into the TCAS Timeslot Provision RAM during an indirect write operation.

VLINK[1:0]

VLINK[1:0] is the Virtual Link from which this TCAS LINK/TSLOT is mapped. Valid values are 0x0 to 0x3. For proper operation, timeslots from multiple physical links cannot be mapped to the same VLINK.

After an indirect read operation is completed, VLINK[1:0] reports the virtual link number read from the TCAS Timeslot Provision RAM. The Virtual Link number to be written to the TCAS Timeslot Provision RAM in an indirect write operation must be set up in this register before triggering the write. VLINK[1:0] reflects the value written until the completion of a subsequent indirect read operation.

PROV

The indirect provision enable bit (PROV) reports the timeslot provision enable flag read from the timeslot provision RAM after an indirect read operation is completed. The provision enable flag to be written to the timeslot provision RAM in an indirect write operation must be set up in this register before triggering the write. When PROV is set high, the current time-slot is assigned to the virtual link as indicated by VLINK[1:0]. When PROV is set low, the time-slot does not belong to any virtual link. The transmit link data is set to the contents of the Idle Time-slot Fill Data register. PROV reflects the last value read or written until the completion of a subsequent indirect read operation.

Register 0x184: TCAS Framing Bit Threshold

Bit	Type	Function	Default
15:7		Unused	X
6:0	R/W	FTHRES[6:0]	0x1F

This register contains the threshold used by the clock activity monitor to detect for framing bits/bytes.

FTHRES[6:0]

The framing bit threshold bits (FTHRES[6:0]) contain the threshold used by the clock activity monitor to detect the presence of framing bits. A counter in the clock activity monitor increments at each REFCLK and is cleared by a rising edge of the TSCLK. When the counter exceeds the threshold given by FTHRES[6:0], a framing bit/byte is detected. FTHRES[6:0] should be set as a function of the REFCLK period and the expected gapping width of TSCLK during framing bits/bytes.

For E1 only device operation, the following equation should be used to determine the acceptable range of values for FTHRES:

$$\left(\frac{REFCLK.Freq}{TSCLK.E1.Freq}\right)*1.5 < FTHRES < \left(\frac{REFCLK.Freq}{TSCLK.E1.Freq}\right)*7$$

For T1 device operation and mixed T1 and E1 device operation (T1 requirements are more rigorous), the following equation should be used to determine FTHRES:

$$FTHRES \approx \left[\left(\frac{REFCLK.Freq}{RSCLK.T1.Freq}\right)*1.5\right] - 3$$

For example, for T1 or mixed T1 and E1, with a REFCLK.Freq = 19.44MHz, FTHRES[6:0] = 15.

Register 0x186: TCAS Idle Time-slot Fill Data

Bit	Type	Function	Default
15:8		Unused	X
7:0	R/W	FDATA[7:0]	0xFF

This register contains the data to be written to the disabled time-slots of a channelized link.

FDATA[7:0]

The fill data bits (FDATA[7:0]) are transmitted during disabled (PROV set low) time-slots or virtual links.

Register 0x188: TCAS Link Disable Register

Bit	Type	Function	Default
15	R/W	VLDIS	0
14:2		Unused	X
1:0	R/W	DVLINK[1:0]	0

This register indicates a virtual link that is to be disabled (unprovisioned) while individual time-slots are changed. This allows virtual links to either turn on or off at once instead of gradually while each time-slot in the provisioning RAM is written.

DVLINK[1:0]

The disable virtual link bits (DVLINK[1:0]) indicate the virtual link to be disabled. If VLDIS=1, all time-slots mapped to this virtual link is forced unprovisioned, and the value in FDATA[7:0] is transmitted.

VLDIS

The virtual link disable bit (VLDIS) disables the virtual link in DVLINK[1:0]. When VLDIS=1, all time-slots mapped to DVLINK[1:0] are forced unprovisioned, and the PROV bit of those time-slots are ignored. When VLDIS=0, the virtual link's provisioning state is set by the PROV bit.

Register 0x1C0 – 0x1C7: TCAS Link #0 to Link #3 Configuration

Bit	Type	Function	Default
15:3		Unused	X
2	R/W	Reserved	0
1	R/W	E1	0
0	R/W	CEN	0

This register configures the operational modes of transmit link #0 to link #3 (TSDATA[N] / TSCLK[N]; where $0 \leq N \leq 3$).

CEN

The channelize enable bit (CEN) configures link #N for channelized operation.

When CEN=1, TSCLK[N] must be gapped during the T1 framing bit or the E1 framing byte. Thus, on the first rising edge of TSCLK[N] after the extended low period, a downstream device can sample the MSB of timeslot one.

When CEN=0, Link #N is unchannelized, and the E1 register bit is ignored. TSCLK[N] can be gapped during non-data bits, and all data bits are treated as a contiguous stream without regard to timeslots.

E1

The E1 frame structure select bit (E1) configures link #N for channelized E1 operation when CEN is set high. TSCLK[N] is held low during the FAS and NFAS framing bytes. The most significant bit of time-slot 1 is placed on TSDATA[N] on the last falling edge of TSCLK[N] ahead of the extended low period. Link data is present at time-slots 1 to 31. When E1 is set low and CEN is set high, link #N is configured for channelized T1 operation. TSCLK[N] is held low during the framing bit. The MSB of time-slot 1 is placed on TSDATA[N] on the last falling edge of TSCLK[N] ahead of the extended low period. Link data is present at time-slots 1 to 24. E1 is ignored when CEN is set low.

10.7 RIPP Registers

Register 0x200: RIPP Control

Bit	Type	Function	Default
15	R/W	RIPP_EN	0
14		Reserved	0
13	R	RIPP_BUSY	0
12:0		Reserved	0

RIPP_BUSY

This is a status signal indicating that the RIPP main-state machine is currently active. This bit is generated by RIPP.

RIPP_EN

The RIPP_EN enables the RIPP main state machine for normal operations. When RIPP_EN = 0 and RIPP_BUSY = 0, all RIPP operations are disabled. The RIPP_EN should be set to a '1' for normal operations after the initialization of RIPP context memory.

Register 0x202: RIPP Indirect Memory Access Control

Bit	Type	Function	Default
15	RO	MEM_BUSY	0
14	R/W	MEM_RWB	0
13	R/W	MEM_SEL	0
12:10		Reserved	
9:0	R/W	MEM_ADDR	0

This register controls the indirect access to the internal memory. There are two separate RAMs used by RIPP. One is the configuration memory, which holds the configuration information for all groups and links programmed by the microprocessor; the other is the context memory, which stores the state context used as the working space for the RIPP internal state machine. Each of them is 32-bits wide and contains 1024 words.

MEM_ADDR

The indirect memory address (MEM_ADDR [9:0]) indicates the memory word address to be read or written.

The memory-address organization of the internal RAMs is shown in Table 6 and Table 7.

Table 6 RIPP Configuration Memory Address Space

Address space	Description
0x000 – 0x03F	Group configuration record area.
0x2A0 – 0x2A3	TX link configuration record area.
0x350 – 0x353	RX Link Configuration Record area.

Table 7 RIPP Context Memory Address Space

Address space	Description
0x000 – 0x03F	Group context record area.
0x2A0 – 0x2A7	TX link context record area.
0x350 – 0x357	RX link context record area.

MEM_SEL

The memory select (MEM_SEL) selects between the two internal RAMs. A logic ‘0’ selects the configuration memory, while a logic ‘1’ selects the context memory.

MEM_RWB

The memory indirect access control bit (MEM_RWB) selects between a configure (write) or interrogate (read) access to the RIPP internal context RAM. Writing a logic 0 to MEM_RWB triggers an indirect write operation. Data to be written is taken from the RIPP Indirect Memory Data registers. Writing a logic 1 to MEM_RWB triggers an indirect read operation. The read data can be found in the RIPP Indirect Channel Data registers

MEM_BUSY

The memory indirect access status bit (MEM_BUSY) reports the progress of an indirect access. To trigger an indirect access, MEM_BUSY is set high when this register is written; it stays high until the access is complete; at that point, MEM_BUSY is set low. This register should be polled to determine either: (1) when data from an indirect read operation is available in the Indirect Data register or (2) when a new indirect write operation may commence.

Register 0x204 – 0x206: RIPP Indirect Memory Data Register Array

Address	Bit	Type	Function	Default
0x204	15:0	R/W	MEM_DATA_LSB	0
0x206	15:0	R/W	MEM_DATA_MSB	0

MEM_DATA_LSB

The MEM_DATA_LSB represents either: (1) the least significant 16 bits of the data to be written to internal memory or (2) the least significant 16 bits of the read data resulting from the previous read operation. The read data is not valid until after the MEM_BUSY bit is cleared.

MEM_DATA_MSB

The MEM_DATA_MSB represents either: (1) the most significant 16 bits of the data to be written to internal memory or (2) the least significant 16 bits of the read data resulting from the previous read operation. The read data is not valid until after the MEM_BUSY bit is cleared.

The actual memory data structure is shown in Table 8 through Table 14.

RIPP Group Configuration Record Memory

Purpose: Contains the PM programmed configuration data for the corresponding groups.

Usage: IMA Groups only

Maintained by: PM

Record Size: 16 32-bit words

MEM_ADDR = Area_base_address + Group_tag * 0x10 + Word Offset

Table 8 RIPP Group Configuration Record Structure

Word	Bit	Data field	Description
0	31:24	IMA_OAM_LABel	IMA OAM label value for the group. This indicates the IMA version for the current group, and compares against the IMA version number carried in octet 6 of the incoming ICP cells.

Word	Bit	Data field	Description
	23:22	Group_sym_MODE	Group symmetry mode. This is programmed by PM during group configuration. It is then used by RIPP to compare against the Group Symmetry mode field in the incoming ICP cells during group start-up process. If the two values do not match, the startup process is aborted. This field is also inserted into outgoing ICP cells. The supported values for this field are: "00": Symmetrical configuration and operation "01": Symmetrical configuration and asymmetrical operation "10": Asymmetrical configuration and asymmetrical operation "11": Reserved
	21	Group_ICP_FWD_EN	Group ICP cell forwarding enable. '0': Disable ICP cell forwarding to PM. '1': Enable ICP cell forwarding to PM. An interrupt is generated upon each ICP cell to be forwarded to PM, and the content of the ICP cell is copied to microprocessor's directly accessible registers.
	20	Group_ICP_FWD_Filter	Group ICP cell forwarding filtering enable. '0': No filtering. All ICP cells from RDAT are forwarded to PM. '1': Filtering. RIPP filters out the ICP cells that carry no new information (determined by the SCCI field) before forwarding to PM. In this mode, the RIPP forwards a minimum of 1 cell per frame for the group in the absence of SCCI changes.
	19	IMA_10_enable	IMA version 1.0 style link state reporting enable. This field selects how the link state field in the incoming and outgoing ICP cells should be interpreted. Note that this bit is ignored if the group is in asymmetric configuration mode. '0': IMA version 1.1 style (default) '1' IMA version 1.0 style.
	18:10	reserved	
	9	PM_ADJUST_DELAY_DONE_INT_EN	PM adjust delay procedure done Interrupt enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.

Word	Bit	Data field	Description
	8	FE_TRL_INT_EN	Invalid RX TRL Interrupt enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	7	GROUP_TIMING_INT_EN	Group timing interrupt enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	6	FE_TIMEOUT_INT_EN	FE Timeout Interrupt Enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	5	GROUP_TIMEOUT_INT_EN	Group Timeout Enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	4	FE_ABORT_INT_EN	FE Abort Interrupt Enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	3	NE_ABORT_INT_EN	NE Abort Interrupt Enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	2	GTSM_INT_EN	GTSM Interrupt Enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.

Word	Bit	Data field	Description
	1	FE_GSM_INT_EN	FE GSM Interrupt Enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	0	NE_GSM_INT_EN	NE GSM Interrupt Enable. When disabled, this event cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
1	31:24	TX_IMA_ID	IMA ID value to use in the TX (outgoing) ICP cells. This field is programmed by PM during group record initialization.
	23:22	TX_M	Transmit IMA frame length (M). Used by TIMA in the transmit IMA operation. “00”: M = 32 “01”: M = 64 “10”: M = 128 “11”: M = 256
	21:16	P_tx	Minimum number of active TX links required in the group in order for the group to be operational.
	15:8	TX_end_channel	TX End-to-end channel. This data field is used by RIPP to generate the end-to-end channel field in the outgoing ICP cells.
	7	TX_CLK_MODE	Transmit clock mode. “0”: ITC mode. “1”: CTC mode. This field is used in the outgoing TX ICP cells. Note the actual clock mode used by TIMA may differ from this. After a group is added, this field should not be changed, unless a group restart is to be issued.
	6:0	Reserved	
2	31:25	Reserved	
	24	RX_IMA_ID_CFG_EN	This bit selects if the IMA ID value used in the RX direction is configured by PM or captured from incoming ICP cells. ‘0’: IMA ID captured from ICP cells and saved in context memory (RX_IMA_ID). ‘1’: IMA ID configured by PM in the RX_IMA_ID_CFG field in the configuration memory.

Word	Bit	Data field	Description
	23:16	RX_IMA_ID_CFG	RX IMA ID value programmed by PM.
	15:14	Reserved	
	13:8	P_RX	Minimum number of active RX links required in the group in order for the group to be operational.
	7:4	Reserved	
	3:0	RX_M_RANGE	4-bit vector indicating the M values deemed acceptable. Used during group parameter negotiation. Bit 3: M = 256 (‘0’: unacceptable, ‘1’: acceptable) Bit 2: M = 128 (‘0’: unacceptable, ‘1’: acceptable) Bit 1: M = 64 (‘0’: unacceptable, ‘1’: acceptable) Bit 0: M = 32 (‘0’: unacceptable, ‘1’: acceptable)
3	31:26	Reserved	
	25:16	Rx_DELAY_TOL	Receive differential Delay tolerance. This field is the maximum allowed amount of delay to be accumulated for a link within the group. This threshold is used in determining if links are acceptable for adding to a group. This must be set to a value greater than RX_DELAY_GUARDBAND+min_lower_guardband+min_upper_guardband.
	15:11	Reserved	
	10	RX_ADD_DELAY_EN	Receive IMA group delay-adding enable. When enabled, the RIPP rolls back the RDAT read pointers, which effectively adds more delay to the group, to accommodate the new link if it is necessary. ‘0’: disabled. ‘1’: enabled.

Word	Bit	Data field	Description
	9:0	RX_delay_guard_band	Receive IMA group link differential delay guard-band value. This is the suggested distance between RDAT cell write pointer on the slowest link and the RDAT cell read pointer (expressed in the unit of cells), which is set by RIPP when it activates the RX data path during group start-up. This value is not used after group start-up. A guardband placed at group startup helps allow admittance of slower links later. This guardband is in addition to the min_lower_guardband defined in the Delay Configuration Register, which accounts for pointer jitter. Note that this is only a recommended behavior; if necessary, RIPP may choose to not to maintain this guard band to accept a slow link. If RX_ADD_DELAY_EN is disabled, then the RX_DELAY_GUARDBAND should be configured to a value of 3 or greater to prevent rejection of link additions solely due to differential delay measurement jitter (associated with ICP cells and stuff events).
4	31:0	Reserved	
5:15	31:0	RX_PHY_TABLE	This table contains the physical link numbers of all RX links assigned to the group by PM. The table has 32 entries that are packed into 11 32-bit words; each entry corresponds to one RX link. The order of links in the table is determined by PM prior to group start-up, and is not related to the LIDs or physical link numbers. Entries in this table correspond to bits in the RX_LINK_VEC. See Table 9 for the detailed bit mapping. In symmetrical configuration mode, this table must be configured identical to the TIMA Transmit-LID-to-Physical-Link Mapping Table , where the physical link pointers are loaded into the table indexed by the TX LID (i.e., if TX LID 2 was assigned TX Physical Link 45, then RX Physical link pointer 2 would be set to 45). In asymmetrical configuration mode, this table may be loaded in any order, regardless of the TX Physical link pointers or RX LID values, as long as the entries correspond to bits in the RX_LINK_VEC. A simple method for loading entries into this table is to begin at zero and fill the table from there (although holes appear as links are deleted).

Table 9 RX Physical Link Table

Word	Bit	Description
0	31:27	Reserved
	26:20	RX Physical link pointer 2
	19:17	Reserved
	16:10	RX Physical link pointer 1
	9:7	Reserved
	6:0	RX Physical link pointer 0
……	…..	
Word 11	31:17	Reserved
	16:10	RX Physical link pointer 31
	9:7	Reserved
	6:0	RX Physical link pointer 30

RIPP TX Link Configuration Record Memory

Purpose: Contains the PM programmed configuration data for the corresponding TX links.

Usage: IMA Groups only

Maintained by: PM

Record Size: 1 32-bit word

MEM_ADDR = Area_base_address + physical link number * 0x1+ Word Offset

Table 10 RIPP TX Link Configuration Record Structure

Word	Bit	Data field	Description
0	31:18	Reserved	
	17:16	TX_LINK_Group_tag	Group tag value of the group to which this Tx physical link is assigned. This field is programmed by PM during link record initialization.
	15:11	TX_LID	LID value for the physical link. This field is programmed by PM during link record initialization.
	10:5	Reserved	

Word	Bit	Data field	Description
	4	TX_ACTIVE_INT_EN	TX Active interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	3	FE_RX_UNUSABLE_INT_EN	FE RX Unusable interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	2	FE_RX_DEFECT_INT_EN	FE RX Defect interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	1	TX_TIMEOUT_INT_EN	Tx_Timeout interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). ‘0’ Interrupt not enabled ‘1’ Interrupt enabled.
	0	RESERVED	

RIPP RX Link Configuration Record Memory

Purpose: Contains the PM programmed configuration data for the corresponding RX links.

Usage: IMA Groups only

Maintained by: PM

Record Size: 1 32-bit word

MEM_ADDR = Area_base_address + physical link number * 0x1+ Word Offset

Table 11 RIPP RX Link Configuration Record Structure

Word	Bit	Data field	Description
0	31:18	Reserved	

Word	Bit	Data field	Description
	17:16	rx_link_Group_tag	Group tag value of the group to which this Rx physical link is assigned. This field is programmed by PM during link record initialization.
	15:11	Reserved	
	10	RX_ACTIVE_INT_EN	RX Active Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	9	IDLE_CELL_INT_EN	Idle cell interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	8	FE_TX_UNUSABLE_INT_EN	FE TX unusable Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	7	DIFF_DELAY_INT_EN	Differential Delay Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	6	LODS_OVERRUN_INT_EN	LODS, DCB overrun Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	5	LODS_UNDERRUN_INT_EN	LODS, DCB underrun Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.

Word	Bit	Data field	Description
	4	LCD_INT_EN	LCD Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	3	LIF_INT_EN	LIF Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	2	Invalid_ICP_INT_EN	Invalid_ICP interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	1	RX_TIMEOUT_INT_EN	Rx Timeout Interrupt enable. When disabled, this event on this link cannot cause an entry to be written to the RIPP Interrupt FIFO for this group (although the status returned by read_event may be set). '0' Interrupt not enabled '1' Interrupt enabled.
	0	Reserved	

RIPP Group Context Record Memory

Purpose: Contains the current state machine states and status information for the corresponding groups.

Usage: IMA Groups only

Maintained by: RIPP

Record Size: 16 32-bit words

MEM_ADDR = Area_base_address + Group_tag * 0x10 + Word Offset

Unless otherwise specified, all data and the reserved fields should be cleared (to all '0's) by PM prior to adding the group; they are cleared by RIPP during a group restart process

Table 12 RIPP Group Context Record Structure

Word	Bit	Data field	Description
0	31	*GROUP_EN*	Indicates if the current group is enabled. This bit is set by PM using the add_group command, and cleared by PM using the Delete_group command. '0': not enabled (group in NOT_CONFIGURED state) '1': the group is enabled and currently active. This field remains at its current value during a group-restart.
	30:27	*GSM*	Group state machine state. "0000": Start-up "0001": Start-up-Ack "0010": Config-Aborted – Unsupported M "0011": Config-Aborted – Incompatible group symmetry "0100": Config-Aborted – Unsupported IMA versions "0111": Config-Aborted – Other reasons "1000": Insufficient-links "1001": Blocked "1010": Operational Others: Reserved
	26:24	Reserved	
	23	*GTSM*	Group traffic state machine state "0": down (no ATM data transmission is allowed) "1": up (ATM data transmission is allowed)
	22:21	*GWP_Active*	Group-wide procedure in progress. "00": No group-wide procedure is currently in progress. "01": Group startup procedure is in progress. "10": LASR is in progress. Others: reserved
	20	*Reserved*	
	19	*LSM_SYNC_TRANS*	Indicates if there is a transition on the LSM_SYNC state machine in the last processing cycle for the group. '0': There was no transition. '1': There was a transition.

Word	Bit	Data field	Description
	18:16	*LSM_SYNC*	Current state of LSM_SYNC state machine, which synchronizes LSM transition during group startup and LASR procedure. "000": IDLE "001": LSM_SYNC_GETM (Group parameter negotiation finished). "010": LSM_SYNC_RX_USABLE (RX ready to go to usable state, delay evaluation needed). "011": LSM_SYNC_RX_ACTIVE_RDAT (RX ready to start receiving, starting RDAT and IDCC) "100": LSM_SYNC_RX_ACTIVE (RX ready to report ACTIVE to FE) "101": LSM_SYNC_TX_ACTIVE (TX ready to report active to FE)
	15:12	*FE_GSM*	Far-end GSM states. This is copied from the group state field in the incoming ICP cells
	11:6	NUM_TX_LINKS_ACTIVE	Total number of tx links that are currently in an active state.
	5:0	NUM_RX_LINKS_ACTIVE	Total number of rx links that are currently in an active state.
1	31	*GROUP_TIMER_EN1*	Group timer 1 enable. The enable bit is set when the timer is loaded; it is cleared when either a timeout occurs or the timer is disabled.
	30:28	*RESERVED*	
	27:24	*GROUP_TIMER1*	Group-level timer 1. Implemented as 4-bit down counter. The counter is loaded with the appropriate timeout value when the timer is enabled, and decrements on every timer tick, until it reaches zero. A timeout event is declared when a timer tick occurs and the counter equals zero, if the timer is enabled.
	23	*GROUP_TIMER_EN2*	Group timer 2 enable. The enable bit is set when timer is loaded; it is cleared when either a timeout occurs or the timer is disabled.
	22:20	*RESERVED*	
	19:16	*GROUP_TIMER2*	Group-level timer 2. Implemented as 4-bit down counter. The counter is loaded with the appropriate timeout value when the timer is enabled, and decrements on every timer tick, until it reaches zero. A timeout event is declared when a timer tick occurs and the counter equals to zero, if the timer is enabled.

Word	Bit	Data field	Description
	15	*GROUP_INT_ACTIVE*	Indicates if there is currently an interrupt active from the group (including all the links). This bit is set to ‘1’ by RIPP upon generating an interrupt and cleared upon PM issuing a read_event command. No new interrupt is generated once this bit is set. This field remains at its current value during a group-restart.
	14	GROUP_inhibit_status	Group inhibiting status. ‘0’: Group is not inhibited. ‘1’: Group is inhibited. This field can be programmed by PM during group record initialization, and can be modified later using Inhibit_group Not_inhibit_group commands. Note it is possible to inhibit the group before issuing the add_group command. This field remains at its current value during a group-restart.
	13	*RESERVED*	
	12	*FE_TRL_STATUS*	When set, indicates that the TRL specified in the last received ICP cell is a link that is “in-group”. If the TRL received in the last ICP cell is not “in-group”, this bit is cleared, and the TRL remains with the last specified valid TRL. During the period in which the specified TRL is not “in-group”, the scheduling of the cells played out to the ATM layer is not accurate and the depth of the DCB buffers may drift and cause DCB buffer overruns or underruns. If on group startup, the TRL is not detected to be “in-group”, the group does not start up.
	11	*GROUP_TIMING_ERROR*	Group timing error. The FE IMA transmit clock mode does not match the NE transmit clock mode.
	10	*RESERVED*	
	9	*PM_ADJUST_DELY_INT*	PM adjust_delay procedure done interrupt. The adjust_delay procedure invoked by the PM command has successfully finished or aborted.
	8	*FE_TRL_INT*	FE TRL Interrupt. The FE_TRL_STATUS bit has changed state.
	7	*GRP_TIMING_INT*	Group timing interrupt. The GROUP_TIMING_ERROR has changed state.
	6	*FE_TIMEOUT_INT*	Startup-Ack Timeout: The FE fails to transition into the STARTUP-ACK state prior to the NE timing out.
	5	*GR_TIMEOUT_INT*	GSM fails to come out of Insufficient-links state during a group start-up procedure before the relevant timer expires.

Word	Bit	Data field	Description
	4	*FE_ABORT_INT*	FE entered CONFIG-ABORTED state during group start-up.
	3	*NE_ABORT_INT*	Entered NE Config aborted state. FE group parameters unacceptable during group start-up. Possible causes are IMA OAM label proposed by FE not acceptable. Group symmetry proposed by FE not acceptable. RX M proposed by FE not acceptable
	2	*GTSM_INT*	GTSM state change.
	1	*FE_GSM_INT*	FE GSM state change.
	0	*NE_GSM_INT*	NE GSM state change.
2	31:24	*TX_SCCI*	Current TX SCCI value for the group. Each time the Tx ICP cell class B&C info changes, the SCCI field increments by one. This field remains at its current value during a group-restart.
	23:16	*TX_RX_TEST_PTN*	Tx test pattern field to be sent in the transmit ICP cell. If the test link command active bit in the incoming ICP cell from RDAT is set, this field is updated using the TX test pattern field in the same ICP cell; otherwise this field is set to “FF” internally. This field remains at its current value during a group-restart.
	15:7	*RESERVED*	
	6:0	TX_TRL_PHY_ID	Physical link ID for TX TRL. This field must be programmed by PM prior to group startup to ensure TX IDCC ticks are generated and TIMA start sending ICP cells once the group is added. Once a group is added, the TRL can be changed by using UPDATE_TX_TRL command. This field remains at its current value during a group-restart.
3	31:25	*RESERVED*	
	24	TX_GSM_2FRAME	Indicates if at least 2 Tx frames were transmitted since the last gsm change. This is ensures the group status and info field stays the same for at least 2 TX frames, as stated in IMA specification. ‘0’: Less than 2 frames were transmitted since the last GSM transition. ‘1’: At least 2 frames were transmitted since the last GSM transition.
	23:16	TX_LAST_GSM_TRANS_IFSN	The Tx frame sequence number transmitted since the last GSM transition.

Word	Bit	Data field	Description
	15	*TX_TEST_EN*	Enable Tx test pattern procedure. "0": Disabled. The test pattern field in the outgoing ICP cells is filled with zeros. "1": Enabled. RIPP copies the stored Tx_test_pattern info over to the test pattern field. This field is set and changed using the Update_test_ptn PM command. This field remains at its current value during a group-restart.
	14:13	*RESERVED*	
	12:8	*TX_TEST_LID*	Tx LID of the test link. This field is set and changed using the Update_test_ptn PM command. This field remains at its current value during a group-restart.
	7:0	*TX_TX_TEST_PTN*	Tx test pattern field to be sent in the transmit ICP cell. This field is set and changed using the Update_test_ptn PM command. This field remains at its current value during a group-restart.
4	31:0	*TX_PHY_VALID*	32 bit vector in which each bit corresponds to one TX physical link in the TIMA Transmit LID to Physical Link Mapping Table "0": table entry not valid "1": table entry valid (physical link pointed by the corresponding TX_PHY_TABLE entry is assigned to the current group.) This field remains at its current value during a group-restart.
5	31:0	*TX_LASR_ACT*	32-bit vector in which each bit corresponds to one TX physical link in the TIMA Transmit LID to Physical Link Mapping Table. "0": the link is not currently involved in a LASR procedure. "1": the link is currently involved in an active LASR procedure.
6	31:30	Reserved	

Word	Bit	Data field	Description
	29	RX_FE_INFO_VALID	This indicates if the context data fields captured from incoming ICP cells) are valid or not. '0': Invalid. '1': Valid. This bit is set internally by RIPP during group startup after it captures the first valid incoming ICP cells. This field remains at its current value during a group-restart.
	28	Reserved	
	27:26	*RX_M*	Receive IMA frame length (M). This parameter is captured from incoming ICP cells during group startup negotiation process, and later used by RDAT in the receive IMA operation. "00": M = 32 "01": M = 64 "10": M = 128 "11": M = 256
	25:24	FE_SYM_MODE	Group symmetrical mode as indicated by the FE in the latest ICP cell analyzed
	23:16	FE_IMA_OAM_LABEL	IMA OAM label value as indicated by the FE in the latest ICP cell analyzed
	15:8	*RX_SCCI*	Current RX SCCI value for the group. This value is captured from the incoming ICP cells and used to determine if the ICP cell should be processed. This field remains at its current value during a group-restart.
	7:0	RX_IMA_ID	Stores the RX_IMA_ID. If the RX_IMA_ID_CGF_EN bit is set to 1, the user must copy this value fro the RX_IMA_ID_CFG field in the configuration memory. Otherwise, initialize this field to 0x00 and RIPP places the captured value of the IMA ID byte into this field..
7	31:0	*RX_PHY_VALID*	32 bit vector in which each bit corresponds to one RX physical link in RX_PHY_TABLE. "0": table entry not valid "1": table entry valid (physical link pointed by the corresponding RX_PHY_TABLE entry is assigned to the current group). This field is cleared by PM during group record initialization. It may be modified during normal operations by issuing the appropriate PM command, such as add_group, add_link, delete_group, delete_link. This field remains at its current value during a group-restart.

Word	Bit	Data field	Description
8	31:0	*RX_LASR_ACT*	32 bit vector in which each bit corresponds to one RX physical link in RX_PHY_TABLE (which is located in RIPP Group configuration memory). "0": the link is not involved in LASR. "1": the link is currently involved in an active LASR procedure.
9	31:0	*RX_TEST_PTN_MATCH*	32-bit vector in which each bit corresponds to the current test pattern match result on one RX link. The order of RX links is defined in RX_PHY_TABLE (which is located in the RIPP Group configuration memory). "0": the Rx_test_pattern field in the incoming ICP cells on the link does not match the Tx_test_pattern field in the outgoing ICP cells. "1": the Rx_test_pattern field in the incoming ICP cells on the link matches the Tx_test_pattern field in the outgoing ICP cells.
10	31:0	RX_LID_ALLOC	32-bit vector in which each bit indicates if the LID value represented by the bit index is occupied. For example, Bit 31 corresponds to LID value 31, bit 0 corresponds to LID 0, and so on. '0': LID is not allocated to any links. '1': LID is allocated to one of the Rx links in the group.
11	31	RX_TX_TEST_CMD	The TX_TEST_CMD field captured from incoming ICP cells.
	30:29	Reserved	
	28:24	RX_TX_TEST_LID	The TX_TEST_LID field captured from incoming ICP cells.
	23:7	reserved	
	6:0	Last_Scci_phy_link_id	Physical link ID of the Rx link on which the last "analyzable" ICP cell comes. A ICP cell is considered analyzable if 1). the current processing cycle is ICP and 2). the ICP cell is valid, and 3). the ICP cell carries a new SCCI, or the ICP cell comes from the same link of the last analyzed ICP cell; and 4). RX_IMA_ID matches the configured value (or if no value is configured, the value captured from the first ICP cell if group is started/restarted)

Word	Bit	Data field	Description
12	31	RX_TRL_VALID	This indicates if the RX IDCC the TRL of the current group is turned on or not. TRL is identified by the RX_TRL_PHY_ID field, which is translated from the TX_TRL_ LID in the incoming ICP cells, after it is validated by RIPP. ‘0’: Invalid. TRL off. ‘1’: Valid. TRL on. This bit is set internally by RIPP when it first turns on the TRL in RX IDCC (when LSM_SYNC reaches the right state and TRL LID is validated). The FE can change the TRL_LID during normal operations, in which case the new TRL LID is re-verified and saved.
	30:23	reserved	
	22:16	RX_TRL_PHY_ID	Receive timing reference physical link ID. RX_TRL_PHY_ID is translated via a lookup into the RX_PHY_TABLE using the TRL_LID field in the incoming ICP cells, and then used to control the Rx IDCC.
	15:13	reserved	
	12:8	rx_trl_lid	The TRL LID info captured from incoming ICP cells.
	7	delay_adjust_ACTIVE	Indicates if an adjust_delay procedure is active. Adjust delay could be started by thePM command adjust_delay, or internally by the LASR procedure. ‘0’: No delay adjustment is in progress. ‘1’: Delay adjustment is in progress.
	6	delay_adjust_rdat_toggle	The last value of the delay_toggle bit read from the RDAT group context memory. A transition on this bit determines if the ongoing adjust_delay process is finished.
	5	delay_adjust_is_PM	Indicates if the current adjust_delay process is started by PM. ‘0’: the adjust-delay is started internally by LASR. ‘1’ the adjust-delay is started by PM.
	4:0	reserved	
10:15	31:0	*RESERVED*	

RIPP TX Link Context Record Memory

Purpose: Contains the current state machine states and status information for the corresponding TX links.

Usage: IMA Groups only

Maintained by: RIPP

Record Size: 2 32-bit words

MEM_ADDR = Area_base_address + physical link number * 0x2 + Word Offset

Unless otherwise specified, all the data fields and the reserved fields should be cleared (to all '0's) by PM prior to adding the link, and are internally cleared by RIPP during a group-restart.

Table 13 RIPP TX Link Context Record Structure

Word	Bit	Data field	Description
0	31	*TX_LINK_EN*	Flag bit indicating if the link is enabled or not. "0": not enabled, link in UNASSIGNED state "1: enabled. This field is set by RIPP during add_link or add_group command processing. It is cleared by RIPP upon finishing deleting the link. It may be polled by PM to determine the progress of link addition or deletion. This field remains at its current value during a group-restart.
	30:27	*TX_LSM*	TX Link state machine state. "0000": DELETED(NOT_IN_GROUP) "0010": UNUSABLE "1100": USABLE "1110": ACTIVE Others: reserved This field is cleared by PM during link record initialization.
	26:7	*RESERVED*	
	6:4	*FE_RX_LSM*	Far end RX LSM state for the link. This is copied from the appropriate TX LSM state field in the incoming ICP cells.
	3	TX_LINK_PM_UNuSABLE	This field indicates that the PM considers the link unusable. This bit is set up on PM issuing UNUSABLE_LINK command, and cleared up on PM issuing RECOVER_LINK command. This field is programmed by PM during link record initialization. This field remains at its current value during a group-restart.

Word	Bit	Data field	Description
	2:0	TX_LINK_PM_UNuSABLE_CAUSE	Cause specified by PM for the link to be unusable. This field is used by RIPP to notify FE. "000": No cause specified "010": Fault. "011": Mis-connected "100": Inhibited "101": Failed Others: Reserved (currently considered the same as no cause specified). This field is programmed by PM during link record initialization. This field remains at its current value during a group-restart.
1	31:10	*RESERVED*	
	9:8	*FE_RX_DEFECT*	Defect status reported in last receive ICP cell. 00) No defect 01) Physical Link Defect (e.g., LOS, OOF/LOF, LCD) 10) LIF 11) LODS
	7:5		Reserved
	4	*TX_ACTIVE_INT*	Indicates that the NE TX LSM transitioned into/out of Active state. This bit is reset immediately after the read_event command is executed for the group of which this link is a member.
	3	*FE_RX_UNUSABLE_INT*	Indicates that FE RX LSM transitioned into/out of unusable state. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	2	*FE_RX_DEFECT_INT*	Indicates that the FE RX Defect indication changed. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	1	*TX_TIMEOUT_INT*	Indicates the LASR procedure timed out prior to the link entering the ACTIVE state. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	0	*RESERVED*	

RIPP RX Link Context Record Memory

Purpose: Contains the current state machine states and status information for the corresponding RX links.

Usage: IMA Groups only

Maintained by: RIPP

Record Size: 2 32-bit words

MEM_ADDR = Area_base_address + physical link number * 0x2 + Word Offset

Unless otherwise specified, all the data fields and the reserved fields should be cleared (to all '0's) by PM prior to adding the link, and internally cleared by RIPP during group restart.

Table 14 RIPP RX Link Context Record structure

Word	Bit	Data field	Description
0	31	*RX_LINK_EN*	Flag bit indicating if the link is enabled or not. "0": not enabled, link in UNASSIGNED state. "1: enabled. This field is set by RIPP during add_link or add_group command processing. It is cleared by RIPP upon finishing deleting the link. It may be polled by PM to determine the progress of link addition or deletion. This field remains at its current value during a group-restart.
	30:25	*RX_LSM*	RX Link state machine state. "000000": START_UP, No M is negotiated yet. "000010": DELETED, waiting for FE "000100": DELETED, waiting for DCB underrun "000110": UNUSABLE_NO_LID (report to FE as Not_In_Group) "001000": UNUSABLE "001010": UNUSABLE, waiting for DCB underrun "001100": Blocking, waiting for FE "110000": USABLE "110010": USABLE, waiting for data in DCB to be played out, reporting USABLE. "110011": USABLE, waiting for FE "110100": ACTIVE, waiting for RX cell reader to become active, reporting USABLE. "110110": ACTIVE, waiting for the global synchronization event to report ACTIVE to the FE.

Word	Bit	Data field	Description
			"111000: ACTIVE, reporting ACTIVE Others: reserved This field is cleared (UNASSIGNED state) by PM during link record initialization. Note the LINK_PM_UNUSABLE_CAUSE encodes the UNUSABLE states in outgoing ICP cells. The value transmitted in the ICP cell is a combination of part of the RX_LSM and part of the LINK_PM_UNUSABLE_CAUSE.
	24	Reserved	
	23	*RX_LID_VALID*	Flag bit indicating if the value in the RX_LID field is valid or not. "0": invalid "1: valid. This field is cleared by PM during link record initialization. It is set by RIPP when the RDAT LID is validated.
	22:21	*RESERVED*	
	20:16	*RX_LID*	LID value for the RX physical link. This field is cleared by PM during link record initialization. It is set by RIPP when the RDAT LID is validated.
	15:7	*RESERVED*	
	6:4	*FE_TX_LSM*	Far end TX LSM state for the link. This is copied from the appropriate TX LSM state field in the incoming ICP cells.
	3	RX_LINK_PM_UNuSABLE	This field indicates the PM considers the link unusable. This bit is set up on PM issuing UNUSABLE_LINK command, and cleared when PM issues the RECOVER_LINK command. This field is programmed by PM during link record initialization. This field remains at its current value during a group-restart.

Word	Bit	Data field	Description
	2:0	RX_LINK_PM_UNuSABLE_CAUSE	Cause specified by PM for the link to be unusable. This field is used by RIPP to notify FE. "000": No cause specified "010": Fault. "011": Mis-connected "100": Inhibited "101": Failed Others: Reserved (currently considered the same as no cause specified). This field is programmed by PM during link record initialization. This field remains at its current value during a group restart.
1	31:21	*RESERVED*	
	20	*LINK_DELAY_GOOD*	The result of the last differential delay evaluation for the link.
	19	*LODS_OVR*	LODS, DCB overrun. Indicates that the DCB buffer is in an overrun condition. This occurs when the transport delay for the link is detected to be outside the programmed limit and the transport delay is longer than the other links within the group.
	18	*LODS_UNDERRUN*	LODS, DCB under-run. Indicates that the DCB buffer is in an underrun condition.
	17	*LCD*	LCD, Loss of Cell Delineation Defect is present on this link.
	16	*LIF*	LIF, A loss of IMA Frame defect condition is present on this link.
	15:11	*RESERVED*	
	10	*RX_ACTIVE_INT*	RX LSM transition into/out of Active state. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	9	*IDLE_CELL_INT*	Physical layer idle cells were received on the RX link. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	8	*FE_TX_UNUSABLE_INT*	FE TX LSM transitioned into or out of the UNUSABLE state. This bit is reset immediately after the read_event command is executed for the group of which this link is a member.

Word	Bit	Data field	Description
	7	*DIFF_DELAY_INT*	Differential Delay is out of bounds on link addition/or recovery. This indicates the delay on the link was out of bounds of the programmed differential delay and the link failed to come up for this reason. This bit is reset immediately after the read_event command is executed for the group of which this link is a member.
	6	*LODS_OVERRUN_INT*	LODS, DCB overrun. An overrun condition occurred. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	5	*LODS_UNDERRUN_INT*	LODS, DCB underrun. Indicates that the DCB buffer experienced an underrun condition and has disabled itself from forwarding traffic to the ATM layer. An underrun occurs when the transport delay for the link is detected to be outside the programmed limit and the transport delay is smaller than the other links within the group In general, this happens only if the transport delay of the link changes. An underrun condition requires that the link delay be revalidated prior to being placed back in service. This bit is reset immediately after the read_event command is executed for the group of which this link is a member.
	4	*LCD_INT*	A change of state of the LCD status bit was detected. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	3	*LIF_INT*	A change of state of the LIF status bit was detected. This interrupt is automatically masked by the device during a group-wide procedure that includes this link, such as add_group, Restart_group, and Start_LASR (for link addition and link recovery). This bit is reset immediately after read_event command is executed for the group of which this link is a member.

Word	Bit	Data field	Description
	2	*INVALID_ICP _INT*	Invalid ICP parameters detected on RX link during validation of the ICP cell parameters causing validation to fail. Possible reasons include: Invalid LID (i.e., duplicate). Invalid ICP cell offset (out of range). Invalid RX IMA ID, which may indicate a misconnectivity problem. Invalid OAM label received after IMA version being determined through negotiation. Invalid Group symmetry received after symmetry being determined through negotiation. This bit is reset immediately after read_event command is executed for the group of which this link is a member.
	1	*RX_TIMEOUT_INT*	Indicates the LASR procedure timed out prior to the link entering the ACTIVE state. This bit is reset immediately after the read_event command is executed for the group of which this link is a member.
	0	*INVALID_FE_TX_INT*	Invalid FE TX LSM states were detected in an incoming non-errored ICP cell. This bit is reset immediately after the read_event command is executed for the group of which this link is a member.

Register 0x208: Delay Configuration Register

Bit	Type	Function	Default
15:8		Reserved	
7:4	R/W	Min_upper_guardband	3
3:0	R/W	Min_lower_guardband	3

Min_lower_guardband

This value represents the minimum lower guard band needed to be introduced in the RIPP differential delay calculation to account for the RDAT write pointer jitters relative to the RDAT read pointer. To make sure that no underrun occurs, the following relationship must be satisfied to accept a link:

Distance between the observed link write pointer and the read pointer >= min_lower_guardband.

When removing delay from a group with the ADJUST_DELAY command, PM must not reduce the minimum delay on any link in the group below this threshold. Otherwise, LODS underrun may occur after the operation is complete. This guardband is used during group startup and LASR operations.

Min_upper_guardband

This value represents the minimum upper guard band needed to be introduced in the RIPP differential delay calculation to account for the RDAT write pointer jitters relative to the RDAT read pointer. To make sure that no overrun occurs, the following relationship must be satisfied to accept a link:

Distance between the observed link write pointer and the read pointer + Min_upper_guardband <= RX_DELAY_TOL.

When adding delay to a group with the ADJUST_DELAY command, PM must not increase the maximum delay on any link in the group above RX_DELAY_TOL – Min_upper_guardband. Otherwise, LODS overrun may occur after the operation is complete. This guardband is used during group startup and LASR operations.

Register 0x20C: RIPP Timer Tick Configuration Register

Bit	Type	Function	Default
15:0	R/W	Timer_tick_interval	0x3473

Timer_tick_interval

This value controls the interval between timer tick events. The timer ticks are internally generated by counting sysclk pulses. The count of sysclk pulses between timer ticks is a 26 bit integer, the most significant 16 bits of which are specified here, and the lower 10-bits are set to '0's internally. To give an example, a Timer_tick_interval value of 0x3473 represents a value of 0XD1CC00 (13,749,248 decimal) sysclk pulses; this translates to about 250 milliseconds in real time assuming a 55 MHz sysclk.
Also, note that programming a value of 0 in this register is equivalent to programming a value of 1 (there is a non-zero interval).

Register 0x20E: Group Timeout Register #1

Bit	Type	Function	Default
15:12	R/W	Group_startup_ack_timeout	0x4
11:8	R/W	Group_config_abort_timeout	0x4
7:4	R/W	RX_usable_timeout	0x4
3:0	R/W	RX_active_timeout	0x4

This register holds the time-out values used at different states of the group state machine or the group-wide procedures (such as group start-up and LASR). The actual time represented by the timeout value in this register can be obtained as:

Real_time = Timeout_value * Internal_timer_tick_interval

Also, note that actual timeout period may be one less than the specified timeout interval, due to the asynchronous nature of events with respect to the timer. For example, if the interval is 0.25 ns, and the timeout_value is specified as 4, then the timeout occurs after 0.75 ns to 1.00 ns in that state. To guarantee a timeout of at least 1 second, a value of 0x5 would have to be written.

Group_config_abort_timeout

The timeout value determines how long the GSM should stay in Config_Aborted state before it can move back to Start-up state, if no new parameters are proposed by the FE and PM does not issue a Restart_group command.

Group_startup_ack_timeout

The timeout value determines how long the GSM should stay in Start-up-Ack state before it can move back to Start-up state, if the FE GSM is not in one of the following states: Start-up-Ack, Insufficient-Links, Blocked, or Operational.

RX_usable_timeout

During the group start-up or LASR, this timeout value determines how long the RIPP should wait before it can move any RX LSM's to Usable state (unless all the RX links involved are out of defect status). In the case of group start-up, the timer is started when the GSM enters Insufficient-links state; during LASR, it is started when the PM issues add_link command.

RX_active_timeout

During the group start-up or LASR, this timeout value determines how long the RIPP should wait before it can move any RX LSM's to Active state (unless all the links involved are being reported TX = Usable by the FE). The timer is started after the RX = usable synchronization point.

Register 0x210: Group Timeout Register #2

Bit	Type	Function	Default
15:4		Reserved	
3:0	R/W	TX_active_timeout	0x4

This register holds additional group time-out values used at different states of the group state machine or the group-wide procedures (such as group startup and LASR). The actual time represented by the timeout value in this register can be obtained as:

```
Real_time = TX_active_timeout * Internal_timer_tick_interval
```

Also, note that the actual timeout period may be one less than the specified timeout interval, due to the asynchronous nature of events with respect to the timer. For example, if the interval is 0.25 ns, and the Tx_active_timeout is specified as 4, then the timeout occurs after 0.75 ns to 1.00 ns in that state. To guarantee a timeout of at least 1 second, a value 0x5 must be written.

TX_active_timeout

During the group start-up or LASR, this value determines how long the RIPP should wait before it can move any TX LSMs to Active state, unless all the links involved are being reported RX = Active by the FE, and all NE RX link state machines are active (for symmetric mode). In the case of group start-up, the timer is started when the GSM enters Insufficient-links state; during LASR, it is started when the PM issues add_link command.

Register 0x212: TX Link Timeout Register

Bit	Type	Function	Default
15:4	R/W	Reserved	0
3:0	R/W	TX_link_deleted_timeout	0x4

This register holds the time-out values used at different states of the TX LSM. The actual time represented by the timeout value in this register can be obtained as:

```
Real_time = Timeout_value * Internal_timer_tick_interval
```

Also, note that actual timeout period may be one less than the specified timeout interval, due to the asynchronous nature of events with respect to the timer. For example, if the interval is 0.25 ns, and the timeout_value is specified as 4, then the timeout occurs after 0.75 ns to 1.00 ns in that state. To guarantee a timeout of at least 1 second, a value of 0x5 would have to be written.

TX_link_deleted_timeout

During link deletion, this value determines how long the TX LSM should stay in the DELETED state before it can move to the UNASSIGNED state (if the FE does not report RX != Active). The set_rx_phy_defect command immediately terminates this timer (causing an immediate transition to the UNASSIGNED state), as it is assumed that the FE state is unknown.

Register 0x214: RX Link Timeout Register

Bit	Type	Function	Default
15:8	R/W	Reserved	0
7:4	R/W	RX_link_blocked_timeout	0x4
3:0	R/w	RX_link_deleted_timeout	0x4

This register holds additional time-out values used at different states of the RX LSM. The actual time represented by the timeout value in this register can be obtained as:

```
Real_time = Timeout_value * Internal_timer_tick_interval
```

Also, note that actual timeout period may be one less than the specified timeout interval, due to the asynchronous nature of events with respect to the timer. For example, if the interval is 0.25 ns, and the timeout_value is specified as 4, then the timeout occurs after 0.75 ns to 1.00 ns in that state. To guarantee a timeout of at least 1 second, a value of 0x5 would have to be written.

RX_link_deleted_timeout

In the case of link deletion, this value determines how long the RX LSM should stay in the DELETED state before it can move to the UNASSIGNED state (if the FE does not report TX != Active). The set_rx_phy_defect command immediately terminates this timer (causing an immediate transition to the UNASSIGNED state), as it is assumed that the FE state is unknown.

RX_link_blocked_timeout

In the case of link inhibiting, this value determines how long the RX LSM should stay in the BLOCKED state before it can move to the UNUSABLE state (if the FE does not report TX != Active). The set_rx_phy_defect command immediately terminates this timer (causing an immediate transition to the UNUSABLE state), as it is assumed that the FE state is unknown.

Register 0x216: RIPP Interrupt FIFO

Bit	Type	Function	Default
15	RO	FIFO_BUSY	0
14	RO	FIFO_NOT_EMPTY	0
13:8		Reserved	
7:0	RO	Group tag	0

This register is the read interface to the RIPP Interrupt FIFO. Each read to this register causes a read to the FIFO, which automatically updates this register.

Group_tag

Group_tag identifies the group that generated the interrupt. Group_tag is valid only if FIFO_NOT_EMPTY=1 and FIFO_BUSY=0.

FIFO_NOT_EMPTY

Current FIFO status. FIFO_NOT_EMPTY=1 means the FIFO is not empty; and FIFO_NOT_EMPTY=0 means the FIFO is empty. FIFO_NOT_EMPTY is valid only if FIFO_BUSY=0.

FIFO_BUSY

Indicates that the FIFO is busy retrieving the next entry. FIFO_BUSY usually clears within four SYSCLK cycles from the end of a read.

Register 0x218: RIPP Group Interrupt Enable Register

Bit	Type	Function	Default
15:10	R/W	Reserved	0
9	R/W	PM_ADJUST_DELAY_DONE_INT_EN	0
8	R/W	INVALID_TRL_INT_EN	0
7	R/W	GRP_TIMING_INT_EN	0
6	R/W	FE_TIMEOUT_INT_EN	0
5	R/W	GR_TIMEOUT_INT_EN	0
4	R/W	FE_ABORT_INT_EN	0
3	R/W	NE_ABORT_INT_EN	0
2	R/W	GTSM_INT_EN	0
1	R/W	FE_GSM_INT_EN	0
0	R/W	NE_GSM_INT_EN	0

The enable bits provides a global enable for the corresponding IMA group interrupts. If an interrupt enable bit is not set, the respective interrupt cannot cause an entry to be written to the RIPP Interrupt FIFO for any group (although the status returned by read_event may be set). If a bit is set, the individual group interrupt enable is used.

0 – Disable group interrupt for all links.

1– Use individual group interrupt enable.

Register 0x21A: RIPP TX Link Interrupt Enable Register

Bit	Type	Function	Default
15:5	R/W	RESERVED	0
4	R/W	TX_ACTIVE_INT_EN	0
3	R/W	FE_RX_UNUSABLE_INT_EN	0
2	R/W	FE_RX_DEFECT_INT_EN	0
1	R/W	TX_TIMEOUT_INT_EN	0
0	R/W	Unused	0

The enable bits provide a global enable for the corresponding TX link interrupts. If an interrupt enable bit is not set, the respective interrupt cannot cause an entry to be written to the RIPP Interrupt FIFO for any TX link in any group (although the status returned by read_event may be set). If a bit is set, the individual Tx Link Interrupt enable is used.

0 – Disable corresponding Tx Link interrupt for all links.

1 – Use individual corresponding Tx Link interrupt enable.

Register 0x21C: RIPP RX Link Interrupt Enable Register

Bit	Type	Function	Default
15:11	R/W	RESERVED	0
10	R/W	RX_ACTIVE_INT_EN	0
9	R/W	IDLE_CELL_INT_EN	0
8	R/W	FE_TX_UNUSABLE_INT_EN	0
7	R/W	DIFF_DELAY_INT_EN	0
6	R/W	LODS_OVERRUN_INT_EN	0
5	R/W	LODS_UNDERRUN_INT_EN	0
4	R/W	LCD_INT_EN	0
3	R/W	LIF_INT_EN	0
2	R/W	Invalid_ICP_INT_EN	0
1	R/W	RX_TIMEOUT_INT_EN	0
0	R/W	Unused	0

The enable bits provide a global enable for the corresponding Rx link interrupts. If an interrupt enable bit is not set, the respective interrupt cannot cause an entry to be written to the RIPP Interrupt FIFO for any RX link in any group (although the status returned by read_event may be set) for all links. If a bit is set, the individual Rx Link Interrupt enable is used.

0 – Disable group link interrupt for all links.

1 – Use individual link interrupt enable for each link.

Register 0x220-22C: RIPP Command Register

Address	Bit	Type	Function	Default
0x220	15	RO	CMD_BUSY	0
	14:10	R/W	CMD_CODE	0
	9	RO	CMD_ACK	0
	8		Reserved	
	7:0	R/W	CMD_WR_DATA00	0
0X222	15:0	R/W	CMD_WR_DATA01_LSB	0
0X224	15:0	R/W	CMD_WR_DATA01_MSB	0
0X226	15:0	R/W	CMD_WR_DATA02_LSB	0
0X228	15:0	R/W	CMD_WR_DATA02_MSB	0
0X22A	15:0	R/W	CMD_WR_DATA03_LSB	0
0X22C	15:0	R/W	CMD_WR_DATA03_MSB	0

These array registers control the issuing of PM commands. Writing to the first location in the array (0x30) causes a new command to be issued to RIPP. The command operands are carried in the rest of the registers.

CMD_ACK

This bit indicates if a command is accepted (logic high) or rejected (logic low) by RIPP. It is updated by RIPP before the CMD_BUSY is cleared. PM should read this register after a command is issued to determine if the command was accepted (CMD_ACK = 1). The command may be rejected due to one of the following causes:

- Command was issued to an invalid group (never added or inactive)
- A group-wide procedure such as startup or LASR is already active for the group.
- Command tried to add a group that already exists.
- Adjust_delay command was issued but an automatic or previous PM adjust_delay command for this group is already in progress.
- An invalid CMD_CODE was issued.

CMD_CODE

This is set by the microprocessor to indicate which command is being issued. See Table 15 for the details.

CMD_BUSY

This bit indicates if the RIPP Command Register is busy evaluating the previous command. If CMD_BUSY=0, then PM can issue a new command to this register. If CMD_BUSY=1, then the RIPP is busy evaluating the previous command, and PM must wait until CMD_BUSY=0 before issuing the next command.
Note that RIPP command processing consists of two steps. First, the RIPP uses the CMD_BUSY bit to indicate that it has received the command. Second, the RIPP uses the CMD_ACK to indicate if the command is accepted. All submitted commands are received (CMD_BUSY=0), but it is possible that some commands are not accepted (CMD_ACK=0).

CMD_WR_DATA00

8-bit field used to carry the first operand of the current command. See Table 15 for the details.

CMD_WR_DATA01 – CMD_WR_DATA03

32-bit data fields used to carry the rest of the operands of the current command. See Table 15 for the details.

Table 15 Command Register Encoding

Command	Cmd_code	Cmd_wr_data00	Cmd_wr_data01 through cmd_wr_data03
Add_group	00000	Group_tag	Cmd_wr_data01: TX_PHY_VALID vector Cmd_wr_data02: RX_PHY_VALID vector Cmd_wr_data03: Don't care.
Delete_group	00001	Group_tag	Don't care.
Restart_group	00010	Group_tag	Don't care.
Inhibit_group	00100	Group_tag	Don't care.
Not_inhibit_group	00101	Group_tag	Don't care.
Start_LASR	01000	Group_tag	Cmd_wr_data01: TX_PHY_VALID Cmd_wr_data02: RX_PHY_VALID Cmd_wr_data03: Don't care.
Delete_link	01001	Group_tag	Cmd_wr_data01: TX_PHY_VALID Cmd_wr_data02: RX_PHY_VALID Cmd_wr_data03: Don't care.

Command	Cmd_code	Cmd_wr_data00	Cmd_wr_data01 through cmd_wr_data03
Set_rx_phy_defect	01010	Group_tag	Cmd_wr_data01: Don't care. Cmd_wr_data02: RX_LINK_VEC Cmd_wr_data03: Bit 0: rx link physical defect status (LOS, LOF, AIS): '0': no defect '1': defect exists and must be reported to FE. Bits 31-1: Don't care.
Unusable_link	01100	Group_tag	Cmd_wr_data01: TX_LINK_VEC Cmd_wr_data02: RX_LINK_VEC Cmd_wr_data03: Bit 6:4: TX_CAUSE. Encoding: "001": No cause specified "010": Fault. "011": Mis-connected "100": Inhibited "101": Failed Others: Reserved (no effect, command void) Bit 2:0: RX_CAUSE. Encoding: "001": No cause specified "010": Fault. "011": Mis-connected "100": Inhibited "101": Failed Others: Reserved (no effect, command void) Bit 31-7: Don't Care.
Update_test_ptn	10000	Group_tag	Cmd_wr_data01: Bit 13: test pattern active indication Bit 12:8: LID value of the TX Link to be tested. Bit 7:0: Tx test pattern Bit 31-14: Don't care. Cmd_wr_data02: Don't care. Cmd_wr_data03: Don't care.

Command	Cmd_code	Cmd_wr_data00	Cmd_wr_data01 through cmd_wr_data03
Update_tx_trl	10001	Group_tag	Cmd_wr_data01: Bit 4:0: LID value of the TX Link to be used as the new TRL. Bit 31-5: Don't care. Cmd_wr_data02: Don't care. Cmd_wr_data03: Don't care.
Read_event	11000	Group_tag	Don't care.
Read_delay	11001	Group_tag	Don't care.
Adjust_delay	11010	Group_tag	Cmd_wr_data01: Bit15 : DELAY_ADJUST_MODE '0': Remove delay '1': Add delay Bit 9:0: Indicates the amount of delay to be added to/removed from a Group, in cells (R). Due to ICP deration of the cell rate, the device removes A=R*(M/(M-1)) cells of delay. Therefore, the requested amount must be derated from the ideal to account for this, R=A*((M-1)/M), where M is the frame length (32, 64, 128, 256). Bit 31-10: Don't care. Cmd_wr_data02: Don't care. Cmd_wr_data03: Don't care.

Register 0x22E: Command Read Data Control Register

Bit	Type	Function	Default
15:2		Reserved	0
1:0	R/W	Cmd_read_data_page_sel	0

CMD_READ_DATA_PAGE_SEL

Selects which page in the command read data register array is to be made available in the Command Read Data Register Array. A logic '0' selects page 0, while a logic '1' selects page 1 and a logic '2' selects page 2. The pages may be changed at anytime to enable access to the complete information provided by the read event command. See "Register 0x240-0x02BE" for details of the contents of the pages.

Register 0x230: ICP Cell Forwarding Status Register

Bit	Type	Function	Default
15:1	R	Reserved	0
0	R2C	PM_ICP_AVL	0

This register serves as the current PM_ICP_AVL interrupt status.

PM_ICP_AVL

The RIPP state machine sets this bit to indicate that there is a new ICP cell copied over to the ICP cell buffer register area. It is cleared upon the microprocessor reading this register location.

Register 0x232: ICP Cell Forwarding Control Register

Bit	Type	Function	Default
15:2		Reserved	0
1	R/W	ICP_FWD_LOCK_REQ	
0	R	ICP_FWD_LOCK_GRANT	0

ICP_FWD_LOCK_GRANT

This bit serves as an access lock bit controlling the access to the forwarding ICP buffer. A read from this location returns the current lock status. When the ICP_FWD_LOCK_GRANT reads back as '1', the microprocessor is granted read access to the buffer; further writes by the RIPP internal logic are prohibited. Otherwise RIPP has control over the area.

ICP_FWD_LOCK_REQ

Writing '1' to the register location requests the lock for microprocessor read access; while writing '0' releases the lock.

Register 0x240- 0x2BE: RIPP Command Data Register Array

Address	Bit	Type	Function	Default
0x240	15:0	R	CMD_DATA00_LSB	0
0x242	15:0	R	CMD_DATA00_MSB	0
0x244	15:0	R	CMD_DATA01_LSB	0
0x246	15:0	R	CMD_DATA01_MSB	0
0x248	15:0	R	CMD_DATA02_LSB	0
0x24A	15:0	R	CMD_DATA02_MSB	0
0x24C	15:0	R	CMD_DATA03_LSB	0
0x24E	15:0	R	CMD_DATA03_MSB	0
0x250	15:0	R	CMD_DATA04_LSB	0
0x252	15:0	R	CMD_DATA04_MSB	0
0x254	15:0	R	CMD_DATA05_LSB	0
0x256	15:0	R	CMD_DATA05_MSB	0
0x258	15:0	R	CMD_DATA06_LSB	0
0x25A	15:0	R	CMD_DATA06_MSB	0
0x25C	15:0	R	CMD_DATA07_LSB	0
0x25E	15:0	R	CMD_DATA07_MSB	0
0x260	15:0	R	CMD_DATA08_LSB	0
0x262	15:0	R	CMD_DATA08_MSB	0
0x264	15:0	R	CMD_DATA09_LSB	0
0x266	15:0	R	CMD_DATA09_MSB	0
0x268	15:0	R	CMD_DATA0A_LSB	0
0x26A	15:0	R	CMD_DATA0A_MSB	0
0x26C	15:0	R	CMD_DATA0B_LSB	0
0x26E	15:0	R	CMD_DATA0B_MSB	0
0x270	15:0	R	CMD_DATA0C_LSB	0
0x272	15:0	R	CMD_DATA0C_MSB	0
0x274	15:0	R	CMD_DATA0D_LSB	0
0x276	15:0	R	CMD_DATA0D_MSB	0
0x278	15:0	R	CMD_DATA0E_LSB	0
0x27A	15:0	R	CMD_DATA0E_MSB	0
0x27C	15:0	R	CMD_DATA0F_LSB	0
0x27E	15:0	R	CMD_DATA0F_MSB	0
0x280	15:0	R	CMD_DATA10_LSB	0
0x282	15:0	R	CMD_DATA10_MSB	0
0x284	15:0	R	CMD_DATA11_LSB	0
0x286	15:0	R	CMD_DATA11_MSB	0
0x288	15:0	R	CMD_DATA12_LSB	0

Address	Bit	Type	Function	Default
0x28A	15:0	R	CMD_DATA12_MSB	0
0x28C	15:0	R	CMD_DATA13_LSB	0
0x28E	15:0	R	CMD_DATA13_MSB	0
0x290	15:0	R	CMD_DATA14_LSB	0
0x292	15:0	R	CMD_DATA14_MSB	0
0x294	15:0	R	CMD_DATA15_LSB	0
0x296	15:0	R	CMD_DATA15_MSB	0
0x298	15:0	R	CMD_DATA16_LSB	0
0x29A	15:0	R	CMD_DATA16_MSB	0
0x29C	15:0	R	CMD_DATA17_LSB	0
0x29E	15:0	R	CMD_DATA17_MSB	0
0x2A0	15:0	R	CMD_DATA18_LSB	0
0x2A2	15:0	R	CMD_DATA18_MSB	0
0x2A4	15:0	R	CMD_DATA19_LSB	0
0x2A6	15:0	R	CMD_DATA19_MSB	0
0x2A8	15:0	R	CMD_DATA1A_LSB	0
0x2AA	15:0	R	CMD_DATA1A_MSB	0
0x2AC	15:0	R	CMD_DATA1B_LSB	0
0x2AE	15:0	R	CMD_DATA1B_MSB	0
0x2B0	15:0	R	CMD_DATA1C_LSB	0
0x2B2	15:0	R	CMD_DATA1C_MSB	0
0x2B4	15:0	R	CMD_DATA1D_LSB	0
0x2B6	15:0	R	CMD_DATA1D_MSB	0
0x2B8	15:0	R	CMD_DATA1E_LSB	0
0x2BA	15:0	R	CMD_DATA1E_MSB	0
0x2BC	15:0	R	CMD_DATA1F_LSB	0
0x2BE	15:0	R	CMD_DATA1F_MSB	0

The 64 registers in address range 0x240-0x2BE serve as a data bank organized as three pages, each with 32 32-bit words. These registers hold the return value from the command. The value of cmd_read_data_page_select determines which page is currently accessible.

See Table 16 for the details.

Table 16 Command Data Register Array Format

Command	Cmd_data00 through cmd_data1F
Read_event	Page 0: Group Interrupt/Status. Cmd_data00: 32-bit vector where each bit corresponds to a Tx LID. A logic '0' means no interrupt exists on the link, while a logic '1' means an interrupt does exist on the link. Cmd_data01: 32-bit vector where each bit corresponds to an Rx link. The vector is organized corresponding to the RX_PHY_TABLE in the Group Configuration Record. A logic '0' means no interrupt exists on the link, while a logic '1' means an interrupt does exist on the link. Cmd_data02: Group Interrupt/Status. See Table 17 for bit descriptions. Cmd_data03 – Cmd_data1F: Don't care. Page 1: Link Interrupt Status. Cmd_dataN (N = 0x0, …. 0x1F): See Table 18 for bit descriptions. Page 2: Link Status. Cmd_dataN (N = 0x0, …. 0x1F): See Table 19 for bit descriptions. Note that the Tx/Rx links here are sorted in the same order as in the TX_PHY_VALID and RX_PHY_VALID vectors.
Read_delay	Page 0: Cmd_dataN (N = 0x0, …. 0x1F): Bit 31-29: Don't care. Bit 28: Current overrun defect status. Bit 27: Current LCD defect status. Bit 26: Current LIF defect status. Bit 25-23: Don't care. Bit 22-21: Current IFSM state (IMA Sync = 2) Bit 20-16: Don't care. Bit 15:0: DCB write pointer for link N. Note that the DCB write pointer should only be considered valid if the attached status bits are 0 and the IFSM state is Sync (2). Note that the Tx/Rx links here are sorted in the same order as in the TX_PHY_VALID and RX_PHY_VALID vectors. Page 1: Cmd_data00: Bit 15:0: Group DCB read pointer. Bit 31-16: Don't care. Cmd_data01: Bit 31:0: Current RDAT Group reader active vector. If no links are active (i.e., all 32 bits are zeros), the Group DCB read pointer is invalid. Cmd_data02 – Cmd_data1F: Don't care. Page 2: Don't Care.

Table 17 Group Error/Status Bit Mapping

	Bit	Data Field	Description
	31:26	RESERVED	Reserved
Group Interrupts (10 bit)	25	PM_ADJUST_DELAY_DONE_INT	PM adjust_delay procedure done. This means an adjust_delay procedure invoked by the PM command is successfully finished or aborted.
	24	FE_TRL_INT	FE TRL status change.
	23	GRouP_TIMING_INT	Group timing mismatch. This means the FE IMA transmit clock mode does not mach the NE transmit clock mode.
	22	FE_TIMEOU_INT	Startup-Ack Timeout. The FE fails to transition into the STARTUP-ACK state prior to the NE timing out.
	21	GRoup_TIMEOUT_INT	GSM fails to come out of an insufficient-links state during a group start-up procedure before the relevant timer expires.
	20	FE_ABORT_INT	FE entered CONFIG-ABORTED state during group start-up.
	19	NE_ABORT_INT	Entered NE Config aborted state, FE group parameters unacceptable during group start-up. Possible causes are: IMA OAM label proposed by FE not acceptable. Group symmetry proposed by FE not acceptable. RX M proposed by FE not acceptable
	18	GTSM_INT	GTSM state change.
	17	FE_GSM_INT	FE GSM state change.
	16	NE_GSM_INT	NE GSM state change.
Group Status (10 bit)	15:11	RESERVED	Reserved
	10	FE_TRL_STATUS	When set to a '1', the FE specified an in-group link to be the TRL in the latest analyzed ICP cell.
	9	GROUP_TIMING_MISMATCH	Group timing mismatch
	8	GTSM	GTSM state

	Bit	Data Field	Description
	7:4	FE_GSM	FE GSM state: Group state machine state. “0000”: Start-up “0001”: Start-up-ACK “0010”: Config-Aborted – Unsupported M “0011”: Config-Aborted – Incompatible group symmetry “0100”: Config-Aborted – Unsupported IMA versions “0101”: Reserved “0110”: Reserved “0111”: Config-Aborted – Other reasons “1000”: Insufficient-links “1001”: Blocked “1010”: Operational “1011”-“1111” Reserved
	3:0	NE_GSM	NE GSM state

Table 18 Link Event Interrupt Bit Mapping

Word	Bit	Data Field	Description
RX Link Event Status (12 bit)	31:27		Reserved
	26	RX_ACTIVE_INT	RX LSM transition into/out of Active state.
	25	IDLE_CELL_INT	Physical layer idle cells were received on the RX link. The far end transmitter sends, in most cases, idle cells on this link after the FE_TX_LSM becomes UNASSIGNED (when the FE transmit link is deleted).
	24	FE_TX_UNUSABLE_INT	FE TX LSM transitioned into or out of the UNUSABLE state.
	23	DIFF_DELAY_INT	Differential Delay is out of bounds on link addition/or recovery. This indicates the delay on the link was out of bounds of the programmed differential delay and that the link failed to come up for this reason.
	22	LODS_OVERRUN_INT	LODS, DCB overrun. An overrun condition occurred. Note that this interrupt can only be set after a link is successfully added to a group (and is not set when a link is rejected due to DIFF_DELAY_INT).

Word	Bit	Data Field	Description
	21	LODS_UNDERRUN_INT	LODS, DCB underrun. Indicates that the DCB buffer experienced an underrun condition and has disabled itself from forwarding traffic to the ATM layer. An underrun occurs when the transport delay for the link is detected to be outside the programmed limit and the transport delay is smaller than the other links within the group In general, this happens only if the transport delay of the link changes. An underrun condition requires that the link delay be revalidated prior to being placed back in service. If the device remains in the LIF state for a long time (1 hour for E1, longer for T1), DCB underrun may be detected by the device. This occurs because stuff events cannot be detected during LIF, and the internal pointers may wrap-around. Note that this interrupt can only be set after a link is successfully added to a group (and is not set when a link is rejected due to DIFF_DELAY_INT).
	20	LCD_INT	A change of state of the LCD status bit is detected.
	19	LIF_INT	A change of state of the LIF status bit is detected. This interrupt is automatically masked by the device during a group-wide procedure that includes this link, such as add_group, Restart_group, and Start_LASR (for link addition or link recovery).
	18	INVALID_ICP _INT	Invalid ICP parameters detected on Rx link during validation of the ICP cell parameters causing validation to fail. Possible reasons include: Invalid LID (i.e., a duplicate). Invalid ICP cell offset (out of range). Invalid RX IMA ID, which may indicate a misconnectivity problem. Invalid OAM label received after IMA version was determined through negotiation. Invalid Group symmetry received after symmetry was determined through negotiation.
	17	RX_TIMEOUT_INT	Indicates the LASR procedure timed out prior to the link entering the ACTIVE state.
	16	reserved	Reserved
TX Link Event Status	15:5	reserved	Reserved

Word	Bit	Data Field	Description
(8 bit)	4	TX_ACTIVE_INT	Indicates that the NE TX LSM transitioned into/out of Active state.
	3	FE_RX_UNUSABLE_INT	Indicates that FE RX LSM transitioned into/out of unusable state.
	2	FE_RX_DEFECT_INT	Indicates that the FE RX Defect indication changed.
	1	TX_TIMEOUT_INT	Indicates the LASR procedure timed out prior to the link entering the ACTIVE state.
	0	reserved	Reserved

Table 19 Link Status Bit Mapping

Word	Bit	Data Field	Description
RX Link Event Status	31	DATA_PLAYOUT	Reserved
(15 bit)	30	LODS_OVR	LODS, DCB overrun indicated by RDAT.
	29	LODS_UNDERRUN	LODS, DCB under-run indicated by RDAT.
	28	LCD	LCD, indicated by RDAT.
	27	LIF	LIF, indicated by RDAT.
	26:24	FE_TX_LSM	FE Tx LSM state “000”: Not in Group “001”: UNUSABLE “010”: UNUSABLE (Fault) “011”: UNUSABLE (Mis-connected) “100” :UNUSABLE (Inhibited) “101”: UNUSABLE (Failed) “110”: USABLE “111”: ACTIVE
	23:21	RX_LSM_ICP	NE Rx LSM state.
	20:16	RX_LID	Rx LID
TX Link Event Status	15:8		Reserved
(8 bit)	7:6	FE_RX_DEFECT	FE Rx Defect
	5:3	FE_RX_LSM	FE Rx LSM state
	2:0	TX_LSM_ICP	NE Tx LSM state.

Register 0x2C0- 0x2FE: Forwarding ICP Cell Buffer

Address	Bit	Type	Function	Default
0x2C0	15:0	R	ICP_WORD00_LSB	0
0x2C2	15:0	R	ICP_WORD00_MSB	0
0x2C4	15:0	R	ICP_WORD01_LSB	0
0x2C6	15:0	R	ICP_WORD01_MSB	0
0x2C8	15:0	R	ICP_WORD02_LSB	0
0x2CA	15:0	R	ICP_WORD02_MSB	0
0x2CC	15:0	R	ICP_WORD03_LSB	0
0x2CE	15:0	R	ICP_WORD03_MSB	0
0x2D0	15:0	R	ICP_WORD04_LSB	0
0x2D2	15:0	R	ICP_WORD04_MSB	0
0x2D4	15:0	R	ICP_WORD05_LSB	0
0x2D6	15:0	R	ICP_WORD05_MSB	0
0x2D8	15:0	R	ICP_WORD06_LSB	0
0x2DA	15:0	R	ICP_WORD06_MSB	0
0x2DC	15:0	R	ICP_WORD07_LSB	0
0x2DE	15:0	R	ICP_WORD07_MSB	0
0x2E0	15:0	R	ICP_WORD08_LSB	0
0x2E2	15:0	R	ICP_WORD08_MSB	0
0x2E4	15:0	R	ICP_WORD09_LSB	0
0x2E6	15:0	R	ICP_WORD09_MSB	0
0x2E8	15:0	R	ICP_WORD0A_LSB	0
0x2EA	15:0	R	ICP_WORD0A_MSB	0
0x2EC	15:0	R	ICP_WORD0B_LSB	0
0x2EE	15:0	R	ICP_WORD0B_MSB	0
0x2F0	15:0	R	ICP_WORD0C_LSB	0
0x2F2	15:0	R	ICP_WORD0C_MSB	0
0x2F4	15:0	R	ICP_WORD0D_LSB	0
0x2D6	15:0	R	ICP_WORD0D_MSB	0
0x2F8	15:0	R	ICP_WORD0E_LSB	0
0x2FA	15:0	R	ICP_WORD0E_MSB	0
0x2FC	15:0	R	ICP_WORD0F_LSB	0
0x2FE	15:0	R	ICP_WORD0F_MSB	0

The 32 registers in the address range 0x2A0-0x2DE serve as a data bank organized as 16 32-bit words. Those words are used to store the ICP cell forwarded to PM. See Table 20 for the details the format.

Table 20 Receive ICP Cell Buffer Structure

Word	Bits	Parameter	Description			
		icp_data	Octets 6-53 of the payload contained in the last non-errored ICP cell for this link.			
			31:24	**23:16**	**15:8**	**7:0**
0			Octet 6	Octet 7	Octet 8	Octet 9
1			Octet 10	Octet 11	Octet 12	Octet 13
2			Octet 14	Octet 15	Octet 16	Octet 17
3			Octet 18	Octet 19	Octet 20	Octet 21
4			Octet 22	Octet 23	Octet 24	Octet 25
5			Octet 26	Octet 27	Octet 28	Octet 29
6			Octet 30	Octet 31	Octet 32	Octet 33
7			Octet 34	Octet 35	Octet 36	Octet 37
8			Octet 38	Octet 39	Octet 40	Octet 41
9			Octet 42	Octet 43	Octet 44	Octet 45
10			Octet 46	Octet 47	Octet 48	Octet 49
11			Octet 50	Octet 51	Octet 52	Octet 53
12	31:10		Reserved.			
	9	*position_error*	The current ICP cell was received in an unexpected position within the IMA frame. If the contents of the cell are valid, then the ICP cell is considered valid, but the IFSM transitions to the IMA Hunt state.			
	8	*header_invalid*	The ATM cell header is not a correct ICP cell header. This bit should only be set when no ICP cells are received on this link.			
	7	*cid_invalid*	The Cell ID does not indicate the OAM Cell Type is ICP. This bit should only be set when no ICP cells are received on this link.			
	6	*label_invalid*	The OAM Label does not indication IMA version 1.1.			
	5	*lid_mm*	The link identifier in the current ICP cell does not match the LID in validation memory.			
	4	*ima_id_mm*	The IMA ID in the current ICP cell does not match the IMA ID in validation memory.			
	3	*m_mm*	The IMA Frame Length in the current ICP cell does not match the length in validation memory.			
	2	*seq_error*	The IMA Frame Sequence Number in the current ICP cell does not match the sequence number maintained by the RDAT.			

Word	Bits	Parameter	Description
	1	*icp_offset_mm*	The ICP Cell Offset in the current ICP cell does not match the offset in validation memory.
	0	*stuff_invalid*	The link stuff indication in the current ICP cell has not progressed properly from the previous value.
13:15			Reserved.

10.8 RDAT Registers

Register 0x300: RDAT Indirect Memory Command

Bit	Type	Function	Default
15	RO	MEM_BUSY	0
14	R/W	MEM_RWB	0
13:4		Unused	0
3:0	R/W	MEM_SELECT	0

Writing to this register triggers an indirect memory access to the RDAT tables. The indirect memory address (and data register for write operations) must be configured prior to writing the register.

MEM_SELECT

The indirect memory select indicates the memory table within the RDAT that is accessed.

MEM_SELECT	RDAT Memory Table	Address Range
0x00	RDAT Link Statistics Memory	0x000-0x00F
0x01	RDAT IMA Group Statistics Memory	0x000-0x00F
0x02	RDAT TC Link Statistics Memory	0x000-0x007
0x03	RDAT Validation Memory	0x000-0x007
0x04	RDAT Link Context Memory	0x000-0x007
0x05	RDAT Link Message Status Memory	0x000-0x003
0x06-0x07	Reserved	
0x08	Receive ICP Cell Buffer	0x000-0x03F
0x09	RDAT IMA Group Context Memory	0x000-0x00F
0x0A	RDAT TC Link Context Memory	0x000-0x003
0x0B-0x0C	Reserved	
0x0D	Receive ATM Congestion Count Register	N/A
0x0E-0x0F	Reserved	

MEM_RWB

The memory indirect access control bit (MEM_RWB) selects between a configure (write) or interrogate (read) access to the RDAT internal memory. Writing a logic 0 to MEM_RWB triggers an indirect write operation. Data to be written is taken from the Indirect Memory Data registers. Writing a logic 1 to MEM_RWB triggers an indirect read operation. The read data can be found in the Indirect Memory Data registers. The address within a memory table can be found in the Indirect Memory Address register.

MEM_BUSY

The indirect memory access status bit (MEM_BUSY) reports the progress of an indirect access A write to the Indirect Memory Command register triggers an indirect access and sets the MEM_BUSY bit to a logic 1, MEM_BUSY remains logic 1 until the access is complete. This register should be polled to determine either: (1) when data from an indirect read operation is available in the Indirect Memory Data registers or (2) when a new indirect write operation may commence.

Register 0x302: RDAT Indirect Memory Address

Bit	Type	Function	Default
15:11		Unused	0
10:0	R/W	MEM_ADDR	0

This register should not be written while the MEM_BUSY bit is set.

MEM_ADDR

The indirect memory address indicates the word address within the memory table selected with the MEM_SELECT in the command register.

Register 0x304: RDAT Indirect Memory Data LSB

Bit	Type	Function	Default
15:0	R/W	MEM_DATA_LSB	0

This register should not be written while the MEM_BUSY bit is set.

MEM_DATA_LSB

The MEM_DAT_LSB represents either: (1) the least significant 16 bits of the data to be written to internal memory or (2) the least significant 16 bits of the read data resulting from the previous read operation. The read data is not valid until after the RDAT clears the MEM_BUSY bit. The actual definition of each memory table is described under the Indirect Memory Data MSB Register description.

Register 0x306: RDAT Indirect Memory Data MSB

Bit	Type	Function	Default
15:0	R/W	MEM_DATA_MSB	0

This register should not be written while the MEM_BUSY bit is set.

MEM_DATA_MSB

The MEM_DAT_MSB represents either: (1) the most significant 16 bits of the data to be written to internal memory or (2) the most significant 16 bits of the read data resulting from the previous read operation. The read data is not valid until after the RDAT clears the MEM_BUSY bit. The actual definition of each memory table is described next.

RDAT Link Statistics Memory (MEM_SELECT=0)

Purpose: Stores cell and event counts for each Physical Link.

Usage: TC Links and links in IMA Groups. Each word contains two counts for IMA links, one count for TC Links. In IMA mode, each cell may cause the oif_anomalies count to be incremented, and also may cause one and only one of the other counters to be incremented. In TC mode, each cell causes one and only one counter to be incremented. All counters roll over unless otherwise noted.

Maintained by: RDAT.

Record Size: Four 32-bit words.

MEM_ADDR = (Physical Link Number X 4) + Word Offset

Table 21 RDAT Link Statistics Record (IMA)

Word	Bits	Parameter	Description
0	31:16	*stuff_events*	Count of the number of stuff events received on this link.
	15:0	*oif_anomalies*	Count of the number of times this link has transitioned from the IMA Sync state to the IMA Hunt state in the IFSM.
1	31:16	*icp_violations*	Count of HEC errored, OCD errored, CRC-10 errored, invalid, or missing ICP cells received on this link. This also includes valid ICP cells received at unexpected positions. For stuff events, this statistic may only be counted for the first cell in the event. This counter does not increment prior to link validation.
	15:0	*icp_cells*	Count of the number of valid, non-errored ICP cells received on this link. For stuff events, this statistic may only be counted for the first cell in the event.

Word	Bits	Parameter	Description
2	31:16	*filler_cells*	Count of the number of non-errored filler cells received on this link that are written to the buffer.
	15:0	*user_cells*	Count of the number of user cells received on this link that are written to the buffer.
3	31:16	*filtered_cells*	Count of the non-filler, non-idle cells which were not written to the delay compensation buffer while in IMA Startup or IMA Monitor, or cells received with HEC or OCD indications, or CRC-10 errored IMA OAM cells, or cells received while overrun, underrun, LCD, LIF, or OIF conditions exist..
	15:0	*dropped_cells*	Count of the number of idle cells received on this link while not Disabled. All idle cells are counted here, regardless of if they are dropped (despite the name of this counter).

Table 22 RDAT Link Statistics Record (TC)

Word	Parameter	Description
0		Reserved.
1		Reserved.
2	*user_cells*	Count of the number of user cells received on this link that are written to the DCB.
3	*dropped_cells*	Count of the number of cells dropped due to TC overrun, HEC error, or OCD while in TC mode.

RDAT IMA Group Statistics Memory (MEM_SELECT=1)

Purpose: Stores cell and event counts for each IMA Group.

Usage: IMA Groups only. All counters roll over unless otherwise noted

Maintained by: RDAT

Record Size: Four 32-bit words

MEM_ADDR = (Group Tag X 4) + Word Offset

Table 23 RDAT IMA Group Statistics Record

Word	Parameter	Description
0	*user_cells*	Count of the number of user cells that are read from the DCB and transferred to the ATM layer for this group.
1	*dropped_cells*	Count of the number of cells that are dropped solely due to ATM layer congestion for this group.
2		Reserved

Word	Parameter	Description
3	*filler_cells*	Count of the number of filler cells that are read from the DCB (and not transferred to the ATM layer) for this group. Buffers that do not contain the correct embedded information match this criterion. The cell writer may mark cells in this manner for many reasons. For example, when the link is not yet IMA enabled.

RDAT TC Link Statistics Memory (MEM_SELECT=2)

Purpose: Stores cell and event counts for each Physical Link.

Usage: TC Links only. All counters roll over unless otherwise noted.

Maintained by: RDAT

Record Size: Two 32-bit words

MEM_ADDR = (TC Tag X 2) + Word Offset

Table 24 RDAT TC Link Statistics Record

Word	Parameter	Description
0	*user_cells*	Count of the number of cells that are read from the DCB and transferred to the ATM layer for this TC Link.
1	*dropped_cells*	Count of the number of cells that are dropped solely due to Receive Cell Interface congestion for this TC Link.

RDAT Validation Memory (MEM_SELECT=3)

Purpose: Contains configuration information for each Physical Link. Used by the RDAT to validate incoming ICP cells in IMA mode, and to control the flow of data to the DCB's. For TC Links, the single bit tc_mode bit must be set. For IMA links, this record should be cleared before link addition.

Usage: IMA Groups and TC Links

Maintained by: Microprocessor (for TC mode only), RIPP

Record Size: Two 32-bit words

MEM_ADDR = (Physical Link Number X 2) + Word Offset

Table 25 RDAT Validation Record

Word	Bits	Parameter	Description
0	31	tc_mode	tc_mode controls if the link is in TC mode or part of an IMA group 0 IMA link. Flow of cells is controlled by the IMA protocol and the current IMA state 1 TC Enabled. Cells received for this link are stored in a four-cell FIFO in the SDRAM and scheduled for immediate transmission out the group FIFO.
0	30:29	*link_state*	Link Data State. Valid only in IMA mode. This field reports the current state as set by the RIPP to determine how the RDAT should handle incoming cells: 00 Disabled. Cells are read from the link FIFOs and dropped. 01 IMA startup. All ICP cells are forwarded to the RIPP via the ICP FIFO, but the IFSM is not started and the delay compensation buffers remain idle for this link. 10 IMA Monitor. The IFSM is enabled. ICP cells are forwarded to the RIPP (all during the IFSM HUNT state, just cells at the expected ICP cell position during the PRESYNC and SYNC states). No cells are written to valid buffer locations in the DCB, but the write pointers are incremented. 11 IMA Enabled. Same as IMA Monitor, except that user and filler cells are written to the DCB.
	28:26		Reserved.
	25:24	*m*	IMA frame length. The value is programmed by the RIPP to allow the RDAT to perform the IFSM, and to validate the value for M in the incoming ICP cells. 00 32 cells 01 64 cells 10 128 cells 11 256 cells.
	23:16	*ima_id*	IMA ID. This value is the group identifier, which is programmed by the RIPP to allow the RDAT to validate this value in the incoming ICP cells.
	15:8	*icp_offset*	ICP Cell Offset. This value is programmed by the RIPP to allow the RDAT to determine the frame boundary on this link, and to validate this value in the incoming ICP cells.
	7		Reserved.
	6	*ima_version*	IMA Version supported for this link. This factors into IMA OAM label checking, if the label_disable bit is not set. 0 = IMA version 1.1 1 = IMA version 1.0
	5	*label_disable*	When set, the IMA OAM label within the incoming ICP cells is not used for validation of these cells. When not set, the IMA OAM label must match that specified by the ima_version field.

Word	Bits	Parameter	Description
	4:0	*lid*	Logical identifier for this link. This value is programmed by the RIPP to allow the RDAT to validate the incoming ICP cells.
1	31:10		Reserved.
	9:0	*dcb_thresh*	Configured overrun threshold of the delay compensation buffer for this link (in cells − IMA only). This must be less than or equal to the value specified in MAX_DCB_DEPTH in the Global configuration register. When this threshold is exceeded (distance between the read and write pointers), the overrun_latch error status is set. This threshold is programmed by the RIPP at link startup.

RDAT Link Context Memory (MEM_SELECT=4)

Purpose: Contains IMA state information for each IMA Physical Link. For IMA connections, RDAT uses this memory to maintain the IFSM, IESM, OSM, and the DCB write pointer for each Physical Link. Note that for IMA links the group tag must be initialized prior to link addition, with all other fields initialized to zero. For TC Links, this memory is used for the external write pointer and should be initialized to zero.

Usage: IMA Groups and TC Links

Maintained by: RDAT

Record Size: Two 32-bit words

MEM_ADDR = (Physical Link Number x 2) + Word Offset

Table 26 RDAT Link Context Record

Word	Bits	Parameter	Description
0	31	*lcd_latch*	Loss of Cell Delineation Defect latched status. This status is maintained by the RDAT to report occurrences of LCD on this link. This bit is set when an LCD defect is detected (as reported in the HEC field), and s cleared by the RDAT when a valid ICP cell is received. The bit may remain set if the LCD condition persists.
	30	*overrun_latch*	DCB Overrun latched status. This status is maintained by the RDAT to report occurrences of DCB overrun. This bit is set when a DCB overrun is detected, and is cleared by the RDAT when a valid ICP cell is received. The bit may remain set if the overrun condition persists.
	29	*underrun_latch*	DCB Underrun latched status. This status is maintained by the RDAT to report occurrences of DCB underrun. This bit is set when a DCB underrun is detected (by the cell reader process), and is cleared by the RDAT when a valid ICP cell is received. The bit may remain set if the underrun condition re-occurs.
	28:25		

Word	Bits	Parameter	Description
	24:15		Reserved
	14:13	*iesm_state*	IMA Error/Maintenance State. This state is maintained by the RDAT to indicate the current state in the IESM for this link. 11 Reserved. 10 IMA Working. User cells may be written to the DCB. 01 OIF Anomaly. User cells are replaced with filler cells in the DCB. 00 LIF Defect. User cells are replaced with filler cells in the DCB.
	12:10	*oif_cnt*	Count of the number of IMA frames while in the Out of IMA Frame (OIF) anomaly. This value is compared against gamma + 2 to detect the loss of an IMA frame (LIF) Gamma is set in Register 0x308. Once the LIF condition is detected, this count is reset, and counts the persistence of IMA Sync for two IMA frames.
	9	*last_cell_stuff*	Active high bit indicating when the last cell received on this link was a stuff cell (required for proper IFSM processing).
	8	*icp_init_done*	RDAT clears this bit at the start of a Link Addition procedure. RDAT sets this bit when any valid cell is received on this link after the link is added to the Group.
	7:2		Reserved.
	1:0	*group_tag*	The group tag associated with this link. The value is initialized by PM; it is used by the cell write process to retrieve the group read pointer, to detect overrun conditions.
1	31	*Reserved*	
	30	*Reserved*	
	29	*idleerr*	Idle Cell Received during IMA status. This status is maintained by the RDAT to report occurrences of idle cells on IMA links to PM via the RIPP. This bit is set when an idle cell is detected on an IMA link, and is cleared when the RDAT message clear command is issued with the idleerr_clear bit set (indicating that the RIPP has acknowledged the problem).
	28:26		Reserved.

Word	Bits	Parameter	Description
	25:23	*stuff_cnt*	Current link stuff count. This indicates the occurrence of the next stuff event. When an ICP cell is received, this count is set to the value in the link stuff indication in that cell. In the event of an errored, invalid, or missing ICP cell, the count is automatically decremented (unless the count is 000 or 111). Note that an invalid stuff sequence is interpreted as an invalid ICP cell. 111 No imminent stuff event. 110-101 Reserved. 100 Stuff event in 4 ICP cell locations. 011 Stuff event in 3 ICP cell locations. 010 Stuff event in 2 ICP cell locations. 001 Stuff event in 1 ICP cell locations. 000 The next cell received on this link is a stuff event.
	22:21	*ifsm_state*	IMA Frame Synchronization Mechanism State. This state is maintained by the RDAT to indicate the current state in the IFSM for this link. 00 IMA Hunt. Performs a cell-by-cell search for IMA framing. Cells are not written to the DCB. 01 IMA PreSync. Performs a frame-by-frame search for valid ICP cells. Cells are not written to the DCB (although write pointers are maintained). 10 IMA Sync. Verifies IMA framing on a frame-by-frame basis. Valid cells are written to the DCB. 11 Reserved.
	20:18	*state_cnt*	State count. This count is used within the IFSM, and has dual meaning, depending on the state. In the IMA PreSync state, this is the current number of consecutive valid ICP cells. This value is compared against the device gamma value to determine when the IFSM may enter the IMA Sync state from the IMA PreSync state. Once the IMA Sync or Hunt state is entered, this value is reset to 0. In the IMA Sync state, this is the current number of consecutive errored ICP cells. This value is compared against the device beta value to determine when the IFSM may enter the IMA Hunt state from the IMA Sync state. Once the IMA Hunt state is entered, or a non-errored cell is received, this value is reset to 0.
	17:16	*invalid_cnt*	Current number of consecutive invalid ICP cells. This value is compared against the device alpha value to determine when the IFSM may enter the IMA Hunt state from the IMA Sync state. Once the IMA Hunt state is entered, or a valid cell is received, this value is reset to 0, and this value may only be incremented in the IMA Sync state.

Word	Bits	Parameter	Description
	15:0	*write_ptr*	Current delay compensation buffer write pointer for this link. The least significant portion of the write pointer is the cell number within the IMA frame, while the most significant portion represents the IMA Frame Sequence Number. The actual number of bits per field depends on the value for M for this link. Bits 9:0 for MAX_DCB_DEPTH = 1024 represent the actual buffer write pointer (or bits 7:0 for MAX_DCB_DEPTH = 256). The write pointer is initialized by the RDAT when a valid ICP cell is received while in the IMA Hunt state, and is incremented otherwise. Only bits 12:0 are used for overrun detection, underrun detection, and differential delay calculations. The most significant 3 bits are only used for IFSN validation. Each increment of the write pointer represents a single cell time at the link line rate. All write pointers within a group can be compared to determine the differential delay.

RDAT Link Message Status Memory (MEM_SELECT=5)

Purpose: Contains the current message status indicator for each Physical Link. This information is used solely by RDAT for communication with the RIPP, and must be initialized using read-modify-write by PM at link addition to clear the msg_status bit and leave the reserved portion unchanged.

Usage: IMA Groups only

Maintained by: RDAT

Record Size: One 32-bit word

MEM_ADDR = Physical Link Number

Table RDAT Link Message Status Record

Bits	Parameter	Description
9	*msg_status*	RDAT message FIFO status. This bit is set by the RDAT when a message for this link is written to the RDAT message FIFO. The bit is cleared when a command for this link is written to the RDAT message clear command register.
8		*Reserved*
7:0		*Reserved*

Receive ICP Cell Buffer (MEM_SELECT=8)

Purpose: Contains the most recently received non-errored ICP cell (valid or invalid) for each Physical Link. The RDAT initializes this buffer with the first cell received during link addition. This record is provided for read access only.

Usage: IMA Groups only

Maintained by: RDAT

Record Size: 16 32-bit words.

MEM_ADDR = (Physical Link Number X 16) + Word Offset

Table 27 Receive ICP Cell Buffer Structure

Word	Bits	Parameter	Description			
		icp_data	Octets 6-53 of the payload contained in the last non-errored ICP cell for this link.			
			31:24	**23:16**	**15:8**	**7:0**
0			Octet 6	Octet 7	Octet 8	Octet 9
1			Octet 10	Octet 11	Octet 12	Octet 13
2			Octet 14	Octet 15	Octet 16	Octet 17
3			Octet 18	Octet 19	Octet 20	Octet 21
4			Octet 22	Octet 23	Octet 24	Octet 25
5			Octet 26	Octet 27	Octet 28	Octet 29
6			Octet 30	Octet 31	Octet 32	Octet 33
7			Octet 34	Octet 35	Octet 36	Octet 37
8			Octet 38	Octet 39	Octet 40	Octet 41
9			Octet 42	Octet 43	Octet 44	Octet 45
10			Octet 46	Octet 47	Octet 48	Octet 49
11			Octet 50	Octet 51	Octet 52	Octet 53
12	31:10		Reserved.			
	9	*position_error*	The current ICP cell was received in an unexpected position within the IMA frame. If the contents of the cell are valid, then the ICP cell is considered valid, but the IFSM transitions to the IMA Hunt state.			
	8	*header_invalid*	The ATM cell header is not a correct ICP cell header. This bit should only be set when no ICP cells are received on this link.			
	7	*cid_invalid*	The Cell ID does not indicate the OAM Cell Type is ICP. This bit should only be set when no ICP cells are received on this link.			
	6	*label_invalid*	The OAM Label does not indication IMA version 1.1.			
	5	*lid_mm*	The link identifier in the current ICP cell does not match the LID in validation memory.			
	4	*ima_id_mm*	The IMA ID in the current ICP cell does not match the IMA ID in validation memory.			
	3	*m_mm*	The IMA Frame Length in the current ICP cell does not match the length in validation memory.			
	2	*seq_error*	The IMA Frame Sequence Number in the current ICP cell does not match the sequence number maintained by the RDAT.			
	1	*icp_offset_mm*	The ICP Cell Offset in the current ICP cell does not match the offset in validation memory.			
	0	*stuff_invalid*	The link stuff indication in the current ICP cell has not progressed properly from the previous value.			

Word	Bits	Parameter	Description
13:15			Reserved.

RDAT IMA Group Context Memory (MEM_SELECT=9)

Purpose: Contains state information for each IMA Group. VPHY_ID is the only field that must be configured by PM (prior to IMA group startup).

Usage: IMA Groups only

Maintained by: RDAT, PM

Record Size: Four 32-bit words

MEM_ADDR = (Group Tag X 4) + Word Offset

Table 28 RDAT IMA Group Context Record

Word	Bits	Parameter	Description
0	31:16	vphy_id	Virtual PHY ID. For multi-channel UTOPIA mode, this identifies which channel in the RXAPS FIFO cells received for this group are written to. The least significant 5 bits determine the destination channel of the RXAPS FIFO for this IMA group, and the upper 11-bits are unused. For Any-PHY mode and single channel UTOPIA, this identifies the address that is prepended to all cells as they are written to the single channel RXAPS FIFO. For single channel UTOPIA mode and Any-PHY mode, the least significant 7 bits must uniquely identify a channel (legal values of 0-7 and the upper 9 bits are user selectable.
	15:0		Reserved.
1	31	*adj_delay_toggle*	RDAT toggles this bit each time an Adjust_delay procedure completes.
	30:13		Reserved
	12:0	*read_ptr*	Current read pointer for the delay compensation buffers associated with this group. The most significant bits represent an extension of the pointer, which is based on the IMA frame sequence number. This field is initialized at link addition using the DCB depth command (with the initiate bit set).
2	31:0		Reserved
3	31:0		Reserved

RDAT TC Link Context Memory (MEM_SELECT=0xA)

Purpose: Contains state information for each TC Link. VPHY_ID is the only field that must be configured.

Usage: TC Links only

Maintained by: RDAT, microprocessor

Record Size: One 32-bit word

MEM_ADDR = TC Tag

Table 29 RDAT TC Link Context Record

Bits	Parameter	Description
31:16	vphy_id	Virtual PHY ID. For UTOPIA L2 Multi-Address mode, this identifies to which channel in the RXAPS FIFO cells received for this group are written. The least significant 5 bits determine the destination channel of the RXAPS FIFO for this IMA group, and the upper 11-bits are unused. For Any-PHY and UTOPIA L2 Single-Address modes, this identifies the address that is prepended to all cells as they are written to the single channel RXAPS FIFO. For single channel UTOPIA mode and Any-PHY mode, the least significant 7 bits must uniquely identify a channel (legal values of 0-7 and the upper 9 bits are user selectable.
15:0	*read_ptr*	Current read pointer for the delay compensation buffers associated with this TC connection.

Receive ATM Congestion Count Register (MEM_SELECT=0xD)

Purpose: Contains a global count of the number of cells dropped due to Receive Cell Interface congestion. RDAT increments this counter and sets one of the Receive ATM Congestion Status bits each time it drops a cell.

Usage: Global

Maintained by: RDAT

Record Size: one word

MEM_ADDR is not used for accesses to this register

Table 30 Receive ATM Congestion Count Register

Bits	Parameter	Description
31:0	cong_count	Count of the total number of cells dropped due to ATM congestion.

Register 0x308: RDAT Configuration

Bit	Type	Function	Default
15	R/W	RDAT_ENABLE	0
14:9		Unused	0
8	R/W	IMA_IDLE_FWD_EN	0
7:5	R/W	GAMMA	1
4:2	R/W	BETA	2
1:0	R/W	ALPHA	2

ALPHA

ALPHA represents the number of consecutive invalid ICP cells that causes the IFSM to transition from the IMA Sync state to the IMA Hunt state.

Value	Definition
0	Undefined
1-2	Number of consecutive invalid ICP cells
3	Undefined

BETA

BETA represents the number of consecutive errored ICP cells that causes the IFSM to transition from the IMA Sync state to the IMA Hunt state.

Value	Definition
0	Undefined
1-5	Number of consecutive errored ICP cells
6-7	Undefined

GAMMA

GAMMA represents the number of consecutive valid ICP cells that allows the IFSM to transition from the IMA PreSync state to the IMA Sync state. GAMMA+2 also represents the number of frames the IESM waits after detecting OIF before entering the LIF state.

Value	Definition
0	Undefined
1-5	Number of consecutive valid ICP cells
6-7	Undefined

IMA_IDLE_FWD_EN

When set, this bit allows the RDAT to forward received Idle cells to the ATM layer as if they were user cells (in the absence of defects and errors). By default, idle cells are dropped.

RDAT_ENABLE

When set, this bit enables the RDAT state machines. When disabled, the link FIFOs are not serviced and IDCC requests are ignored. The operation of the microprocessor accesses are not affected by this enable.

Register 0x30A: Receive ATM Congestion Interrupt

Bit	Type	Function	Default
15:8		Unused	0
7:0	R2C	CONG[7:0]	0

The status in this register is latched, and it is cleared when read.

CONG[7:0]

CONG[7:0] is a bit-vector indicating on which channel a cell was dropped at the Receive Cell Interface.

In UTOPIA-2 Multi-Address mode, a set bit indicates that a cell is dropped on the corresponding channel due to a full RXAPS FIFO.

In Any-PHY and UTOPIA-2 Single Address modes, bit 0 set indicates that a cell is dropped because the single shared RXAPS FIFO is full, or because 16 cells are already stored in the FIFO for the current IMA Group or TC Link Bits 7:1 are unused.

Read the Receive ATM Congestion Count Register (MEM_SELECT=0xD) to determine the total number of cells dropped.

Register 0x30E: Receive TC Link FIFO Overrun Interrupt Register

Bit	Type	Function	Default
15:2		Unused	0
1:0	R	PHYSICAL_LINK	0

PHYSICAL_LINK

Indicates the most recent physical link number that experienced Link FIFO overrun. PHYSICAL_LINK is valid only when TC_OVERRUN=1 in the RDAT Master Interrupt Status Register. This registers is not used to report overruns on Physical Links that are allocated to IMA Groups.

Register 0x310: RDAT Master Interrupt Register

Bit	Type	Function	Default
15	RO	Reserved	0
14:3		Unused	0
2	R2C	TC_OVERRUN	0
1	RO	Reserved	0
0	RO	ATM_CONG	0

ATM_CONG

When set, this bit indicates that an interrupt bit is set in the Receive ATM Congestion Interrupt register. This bit clears when no interrupt conditions are present in that register, or when the conditions are not enabled using the Receive ATM Congestion Interrupt Enable register.

TC_OVERRUN

When set, this bit indicates that a Link FIFO overrun has occurred on the physical link indicated in the TC Overrun status register. Note that Link FIFO overrun occurs only if the setup procedures are not followed properly by PM. This bit is not used to report overruns on Physical Links that are allocated to IMA Groups. This bit clears when this register is read.

Register 0x312: Receive ATM Congestion Interrupt Enable

Bit	Type	Function	Default
15:8		Unused	0
7:0	R/W	CONG_INTR_EN[7:0]	0x0000

CONG_INTR_EN[7:0]

The CONG_INTR_EN vector enables the ATM FIFO congestion status for RDAT_INTR interrupt generation. When a bit is a one, the associated status generates an interrupt.

Register 0x316: RDAT Master Interrupt Enable

Bit	Type	Function	Default
15	R/W	Reserved	0
14:3		Unused	0
2	R/W	OVERRUN_INTR_EN	0
1	R/W	Reserved	0
0	R/W	CONG_INTR_EN	0

CONG_INTR_EN

When set to a one, the CONG_INTR_EN allows the presence of an enabled interrupt in the ATM Congestion Status register to cause an RDAT interrupt.

OVERRUN_INTR_EN

The OVERRUN_INTR_EN bit enables the TC overrun status for RDAT_INTR interrupt generation. When the enable bit is a one, a TC overrun generates an interrupt.

10.9 TIMA registers

Register 0x320: TIMA Indirect Memory Command

Bit	Type	Function	Default
15	R	MEM_BUSY	0
14	R/W	MEM_RWB	0
13:3		Unused	0
2:0	R/W	MEM_SELECT	0

Writing to this register triggers an indirect memory access to the TIMA Context tables. The indirect memory address (and data register for write operations) must be configured prior to writing this register.

MEM_SELECT

The indirect memory select indicates the memory table (or register bank) within the TIMA that is accessed.

MEM_SELECT	TIMA Memory	Address Range
0	Transmit IMA Group Context Table	0x000-0x03F
0	Transmit IMA Group Configuration Table	0x2A0-0x2A3
1	Transmit LID to Physical Link Mapping Table	0x000-0x07F
2	Transmit Physical Link Context Table	0x000-0x007
3-7	Reserved	

MEM_RWB

The memory indirect access control bit (MEM_RWB) selects between a configure (write) or interrogate (read) access to the TIMA internal. Writing a logic 0 to MEM_RWB triggers an indirect write operation. Data to be written is taken from the Indirect Memory Data registers. Writing a logic 1 to MEM_RWB triggers an indirect read operation. The read data can be found in the Indirect Memory Data registers. The address within a memory table can be found in the Indirect Memory Address register.

MEM_BUSY

The indirect memory access status bit (MEM_BUSY) reports the progress of an indirect access. A write to the Indirect Memory Command register triggers an indirect access and sets MEM_BUSY to a logic 1; MEM_BUSY remains logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the TIMA Indirect Memory Data registers or to determine when a new indirect write operation may commence.

Register 0x322: TIMA Indirect Memory Address

Bit	Type	Function	Default
15:11		Unused	0
10:0	R/W	MEM_ADDR	0

This register provides the address for indirect memory access to the TIMA Context tables..

MEM_ADDR

The indirect memory address indicates the word address within the memory table selected with the MEM_SELECT in the TIMA Indirect Memory Command register.

Register 0x324: TIMA Indirect Memory Data LSB

Bit	Type	Function	Default
15:0	R/W	MEM_DATA_LSB	0

This register should not be written while the MEM_BUSY bit is set.

MEM_DATA_LSB

The MEM_DATA_LSB represents either: (1) the least significant 16 bits of the data to be written to internal memory or (2) the least significant 16 bits of the read data resulting from the previous read operation. The read data is not valid until after the TIMA clears the MEM_BUSY bit. The actual definition of each memory table is described under TIMA Indirect Memory Data MSB. If a memory location is read which does not support any bits of 15:0, then the corresponding register bit is loaded with 0. If a memory location is written which does not support bits 15:0, then the data in the corresponding register bit is ignored.

Register 0x326: TIMA Indirect Memory Data MSB

Bit	Type	Function	Default
15:0	R/W	MEM_DATA_MSB	0

This register should not be written while the MEM_BUSY bit is set.

MEM_DATA_MSB

The MEM_DATA_MSB represents either: (1) the most significant 16 bits (31:16) of the data to be written to internal memory or (2) the most significant bits of the data resulting from the previous read operation. The read data is not valid until after the TIMA clears the MEM_BUSY bit. If a memory location is read which does not support bits 31:16, then corresponding register bits are loaded with 0. If a memory location is written that does not support bits 31:16, then data in the corresponding register bits is ignored. Note that a write operation corrupts the read data. The actual definition of each memory table is described next.

Transmit IMA Group Context Table (MEM_SELECT=0)

Purpose: Contains state information, statistics, and ICP cell information (delivered by the RIPP) for each IMA Group.

Usage: IMA Groups only

Maintained by: TIMA

Record Size: 16 32-bit words

MEM_ADDR = (Group Tag X 16) + Word Offset

Table 31 Transmit IMA Group Context Record

Word	Bits	Parameter	Description
0	31:7		Reserved.
	6:0	*TRL cell count*	Cell count from the last 2048 cell stuff on the Timing Reference Link. Each count represents 32 cells and is used in conjunction with the M value in the ICP cell to determine when 2048 cells are transferred. This field must be set to 0 by the PM before group startup. Maintained by TIMA state machine.
1	31:16	*Discarded Cells*	Number of cells discarded from ATM layer when the IMA group was in a non-operational state.
	15:0		Reserved.
2	31:0	*Number of Cell Per Group*	Continuously running cell count of all ATM cells read from the associated group FIFO and sent to link FIFOs. Maintained by TIMA state machine.

Word	Bits	Parameter	Description
3	31:0	*Number of ATM Filler Cells*	Continuously running cell count of ATM filler cells (generated when there is no ATM cell to send) delivered on all links in the group. Maintained by TIMA state machine.
4	31:0		Reserved
5	31:24		Reserved
	23:16	*ICP octet 11*	ICP cell octets that are maintained by RIPP and placed into the outgoing ICP cells for all links in the group.
	15:8	*ICP octet 12*	
	7:0	*ICP octet 13*	
6	31:0	*ICP octet 14* *ICP octet 15* *ICP octet 16* *ICP octet 17*	
7	31:0	*ICP octet 18* *ICP octet 19* *ICP octet 20* *ICP octet 21*	
8	31:0	*ICP octet 22* *ICP octet 23* *ICP octet 24* *ICP octet 25*	
9	31:0	*ICP octet 26* *ICP octet 27* *ICP octet 28* *ICP octet 29*	
10	31:0	*ICP octet 30* *ICP octet 31* *ICP octet 32* *ICP octet 33*	
11	31:0	*ICP octet 34* *ICP octet 35* *ICP octet 36* *ICP octet 37*	
12	31:0	*ICP octet 38* *ICP octet 39* *ICP octet 40* *ICP octet 41*	
13	31:0	*ICP octet 42* *ICP octet 43* *ICP octet 44* *ICP octet 45*	
14	31:0	*ICP octet 46* *ICP octet 47* *ICP octet 48* *ICP octet 49*	
15	31:24	*ICP octet 50*	
	23:16	*ICP octet 51*	

Word	Bits	Parameter	Description
	15:0		Reserved

Transmit IMA Group Configuration Table (MEM_SELECT=0)

Purpose: Contains IMA configuration data programmed by PM.

Usage: IMA Groups only

Maintained by: Microprocessor

Record Size: One 32-bit word

MEM_ADDR = 0x2A0 + Group Tag

Table 32 Transmit IMA Group Configuration Table Record

Bits	Parameter	Description
31:23		Unused
22:16	VPHY Address	VPHY address (group FIFO number) that is assigned to this group. The PM should modify this field only during group configuration. Valid values are 0 to 7.
15:9		Unused
10	Disable Cell Discard	Configuration bit that determines if the ATM cell-discarding feature is enabled for this IMA Group. When set to 0, ATM cells are read and discarded from the group FIFO (one for each request) if there are no active links in the group. When set to 1, cell discarding does not occur for the group.
9	Stuff Advertise Mode	Configuration bit that determines if stuff cell advertising is done either four ICP cells ahead or one ICP cell ahead of the stuff event. This bit should be changed only on Group startup, otherwise the number of cells between TRL stuff events is not correct. 0 = one ICP cell ahead; 1 = four ICP cells ahead
8	Stuff Mode	Configuration bit that determines if ITC or CTC stuff mode is used for this group. Note that it is possible to advertise ITC Transmit Clock Mode in an ICP cell but still use a common clock and CTC stuff mode. 0 = ITC stuff mode, 1 = CTC stuff mode
7:0	OAM Label	Static field to be inserted into octet 6 of ICP cells and OAM cells.

Transmit-LID-to-Physical-Link Mapping Table (MEM_SELECT=1)

Purpose: Maps physical links to IMA Groups.

Usage: IMA Groups only

Maintained by: Microprocessor

Organization: A single linear table. Each entry is addressed by using the Group Tag concatenated with the link ID (LID). In general, this table is sparsely populated since each of the physical link tags can exist in only one table entry.

MEM_ADDR = (Group Tag X 32) + LID value

Table 33 Transmit LID to Physical Link Mapping Table

Bits	Description
1:0	Physical Link for corresponding Group Tag and Link ID. Only values 0 to 3 are valid for this field.

Transmit Physical Link Context Table (MEM_SELECT=2)

Purpose: Contains state information and statistics for each TC Link or IMA Link. Each record is addressed by either the TC tag from the IDCC or the physical link tag from the Transmit-LID-to-Physical-Link mapping Table.

Usage: IMA Groups and TC Links

Maintained by: TIMA and microprocessor

Record Size: Two 32-bit words

MEM_ADDR = (Physical Link Tag or TC Tag X 2) + Word Offset

Table 34 TIMA Physical Link Context Record

Word	Bits	Parameter	Description
0	31	unused	unused

Word	Bits	Parameter	Description
	30:24	CTC Cell Count	Cell count from the last 2048 cell stuff on the CTC mode link (if so configured). Each count represents 32 cells and is used in conjunction with the M value in the ICP cell to determine when 2048 cells are transferred. This field should be set to a count value of either 1 or 4 frames worth of cells (in units of 32) depending on the stuff advertise mode used, 1 ahead or 4 ahead respectively, so the initial stuff on the CTC mode link occurs after 2048 cells. The following table gives possible initialization values: Stuff Adv Mode M Initial CTC Cell Count 1 32 1 1 64 2 1 128 4 1 256 8 4 32 4 4 64 8 4 128 16 4 256 32
	23:16	ICP offset or TC mode VPHY address	**IMA mode**: this field is indexed by the Physical Link tag and determines the cell count within a frame at which an ICP is to be inserted for the link. The width of the field used by the TIMA is dependent on the value of M used for the particular group and is shown in the following: M=256 ICP offset determined by bits [23:16] M=128 ICP offset determined by bits [23:17] M=64 ICP offset determined by bits [23:18] M=32 ICP offset determined by bits [23:19] The mapping of the ICP offset is set such that the offset should not have to be changed if M is changed. Values 0 to 255 are valid. **TC mode**: This field is indexed by the TC tag delivered by the IDCC and determines the VPHY ATM source FIFO associated with the TC connection. Only values 0 to 3 are valid.
	15:13		Reserved
	12:9	Link FIFO Depth on SOF	Count value used to store the link FIFO depth that existed before the first cell was sent to the corresponding link FIFO at the start of the most recent frame. Maintained but is not used by internal TIMA logic. The data is still useful for monitoring the link FIFO depths from the PM layer.
	8:6	Startup Cell Count	Cell count used to track the first cells sent into each Link FIFO after startup. Used to inhibit cell reads from the Link FIFO until 7 cells are written into the Link FIFO so that the nominal cell depth can be achieved. This field must be initialized to 7 by PM before the link is enabled to ensure proper startup. However, if the link is to be used for a TC mode connection, this field must be initialized to a value of 0 to prevent any read inhibit.
	5:3		Reserved

Word	Bits	Parameter	Description
	2:0	Previous LSI	Link Stuff Indication. Decrementing count field used to count ICP cells until a stuff event (if scheduled). Decremented and then inserted into octet 10 of ICP cells associated with the link. Used only in IMA mode and maintained by TIMA. Must be initialized to 111b by PM before link startup.
1	31:16	IMA Mode Stuff Event Count or TC Mode User Cell Count (upper word))	**IMA mode**: this field is indexed by the Physical Link tag and stores a continuously running count of the number of Stuff Events inserted on the link. It is maintained by the transmit engine and is read by the PM. This field should only be reset when the link is not enabled. **TC mode**: this field is indexed by the TC tag delivered by the IDCC and stores the upper 16-bit word of a continuously running 32-bit count of the total number of ATM user cells sent on the link. It is maintained by the transmit engine and is read by the PM. This field should only be reset when the link is not enabled.
	15:0	IMA mode Total User Cell Count or TC Mode User Cell Count (lower word))	**IMA mode**: this field is indexed by the Physical Link tag and stores a continuously running count of the number ATM user cells transferred on the link. It is maintained by the transmit engine and is read by the PM. This field should only be reset when the link is not enabled. **TC mode**: this field is indexed by the TC tag delivered by the IDCC and stores the lower 16-bit word of a continuously running 32-bit count of the total number of ATM user cells sent on the link. It is maintained by the transmit engine and is read by the PM. This field should only be reset when the link is not enabled.

Register 0x328: Transmit Link FIFO Overrun Interrupt Register

Bit	Type	Function	Default
15:4	R	Reserved	0
3:0	R2C	Link_FIFO_OVERFLOW_STAT [3:0]	0

The Transmit Link FIFO Overrun Interrupt register reports an overrun on the TTC Link FIFOs, which occurs when a write is attempted to a full FIFO. If an overrun occurs during the same cycle as a read, the set of an interrupt bit overrides the clear operation.

Programming errors such as duplicate mapping of multiple LIDs to the same link FIFO can cause link FIFO overflows. In addition, many changes of group transmit TRL LID may cause overflows (as slight rate inaccuracies can accumulate during these operations). Overflows should never occur under normal operation. If they do occur, no cells are dropped.

Link FIFO Overflow Status[3:0]

On read, each bit reports the status of the corresponding link FIFO (1= overflow, 0 = no overflow).

Each set overflow status bit is cleared after a read.

Register 0x336: TIMA Interrupt Enable

Bit	Type	Function	Default
15:1		Reserved	0
0	R/W	Link FIFO Overflow Interrupt Enable	0

The interrupt enable bits control if the corresponding interrupt source causes an interrupt on the INTB output or is masked.

Link FIFO Overflow Interrupt Enable

1) link FIFO overflow interrupts are enabled.
0) link FIFO overflow interrupts are not enabled.

10.10 TX IDCC registers

Register 0x340: TXIDCC Indirect Link Control Register

Bit	Type	Function	Default
15	R	CBUSY	0
14	R/W	LRWB	0
13:9	N/A	Unused	N/A
8:7	R/W	LSEL[1:0]	0
6:2	N/A	Unused	N/A
1:0	R/W	LADDR[1:0]	0

Writing to this register triggers an indirect channel register access.

LADDR [1:0]

The indirect link address number (LADDR [1:0]) indicates the link to be configured or interrogated in the indirect link access.

LSEL

LSEL selects the RAM to interrogate or configure.

00 – Unused
01 – Link Table
10 – Reserved
11 – Reserved

LRWB

The link indirect access control bit (LRWB) selects between a configure (write) or interrogate (read) access to the RAM. Writing logic 0 to LRWB triggers an indirect write operation. Data to be written is taken from the Indirect Link Data registers. Writing logic 1 to LRWB triggers an indirect read operation.

CBUSY

The indirect access command bit (CBUSY) reports the progress of an indirect access. CBUSY is set high to trigger an indirect access; it stays high until the access is complete. Once the access is complete, the CBUSY signal is reset by the device. This register should be polled to determine either: (1) when data from an indirect read operation is available in the Indirect Data register or (2) when a new indirect write operation may commence.

Register 0x342: TXIDCC Indirect Link Data Register

Bit	Type	Function	Default
15:8	N/A	Unused	N/A
7	R/W	TC Mode	0
6:0	R/W	Reserved	0

TC Mode

If this bit is set, the associated link is in pass-through mode. Here, the TRL and the Group Tag are don't-care values.

10.11 RX IDCC Registers

Register 0x350: RXIDCC Indirect Link Control Register

Bit	Type	Function	Default
15	R	CBUSY	0
14	R/W	LRWB	0
13:9	N/A	Unused	N/A
8:7	R/W	LSEL[1:0]	0
6:2	N/A	Unused	N/A
1:0	R/W	LADDR[1:0]	0

Writing to this register triggers an indirect channel register access.

LADDR [1:0]:

When LSEL=01 (indicating a Link Table access), the indirect link address number (LADDR [1:0]) indicates the physical link to be configured or interrogated in the indirect access. When LSEL=10 (indicating a Group Table access), the indirect link address number (LADDR [1:0]) indicates the IMA Group to be configured or interrogated in the indirect access.The indirect link address number (LADDR [1:0]) indicates the link to be configured or interrogated in the indirect link access.

LSEL

LSEL selects the RAM to interrogate or configure.

00 – Unused
01 – Link Table
10 – Group Table
11 – Reserved

LRWB

The link indirect access control bit (LRWB) selects between a configure (write) or interrogate (read) access to the RAM. Writing logic 0 to LRWB triggers an indirect write operation. Data to be written is taken from the Indirect Link Data registers. Writing logic 1 to LRWB triggers an indirect read operation.

CBUSY

The indirect access command bit (CBUSY) reports the progress of an indirect access. CBUSY is set high to trigger an indirect access, and stays high until the access is complete. Once the access is complete, the CBUSY signal is reset by the device. This register should be polled to determine when data from an indirect read operation is available in the Indirect Data register or to determine when a new indirect write operation may commence.

Register 0x352 RXIDCC Indirect Link Data Register (For RxIDCC Link Table)

Bit	Type	Function	Default
15:8	N/A	Unused	N/A
7	R/W	TC Mode	0
6	R/W	TRL	0
5:0	R/W	Group Tag	000000

The RxIDCC Link Table indirect data is accessed for valid addresses using LSEL = b'01 in register 0x350.

TC Mode

If this bit is set, the associated link is in passthrough mode. The TRL and the Group Tag are don't care values.

TRL

Timing Reference Link. If set, indicates that the particular link is the Timing reference for the IMA Group. Normally, hardware directly controls this value and it should not be altered unless the hardware function must be overridden.

Group Tag

Specifies the IMA Group to which a link belongs if the TRL bit is set. Normally, hardware directly controls this value and it should not be altered unless the hardware function must be overridden. The legal range of the Group_Tag is b'00 to b'11.

Register 0x352: RXIDCC Indirect Link Data Register (LSB) (For RxIDCC Group Table)

Bit	Type	Function	Default
15:0	R/W	Link Pending Vector(15:0)	0x0000

The RxIDCC Group Table indirect data is accessed for valid addresses using LSEL = b'10 in register 0x350.

Link Pending Vector(15:0)

Bit vector with one bit per IMA Rx LID. When set, indicates that the corresponding Link's Rx LSM is in the Active state. When cleared, indicates that the corresponding Link's Rx LSM is not in the Active state.

Register 0x354: RXIDCC Indirect Link Data Register (MSB) (For RxIDCC Group Table)

Bit	Type	Function	Default
15:0	R/W	Link Pending Vector(31:16)	0x0000

The RxIDCC Group Table indirect data is accessed for valid addresses using LSEL = b'10 in register 0x350.

Link Pending Vector(31:16)

Bit vector with one bit per IMA Rx LID. When set, indicates that the corresponding Link's Rx LSM is in the Active state. When cleared, indicates that the corresponding Link's Rx LSM is not in the Active state.

Register 0x354: RXIDCC Indirect Link Data Register (MSB) (For RxIDCC Group Table)

Register 0x366: DLL Status Register

Bit	Type	Function	Default
15:1	R	Reserved	X
0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit (RUN) indicates the DLL has locked. After system reset, RUN is logic zero until the DLL has locked. For proper operation the DLL must be indicate RUN.

The RUN register bit is cleared only by a system reset.

11 JTAG Test Port

The S/UNI IMA 4 device JTAG Test Access Port (TAP) allows access to the TAP controller and the four TAP registers: instruction, bypass, device identification, and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified, and the device scan path can be bypassed. For more details on the JTAG port, refer to section 9.6.

Table 35 Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 36 Identification Register

Length	32 bits
Version number	1H
Part Number	7340H
Manufacturer's identification code	0CDH
Device identification	173400CDH

Table 37 Boundary Scan Register

Length = 437 bits

Pin/Enable	Cell Type	Register Bit
Unconnected	IN_CELL	0
Unconnected	IN_CELL	1
Unconnected	IN_CELL	2
Unconnected	IN_CELL	3
Unconnected	OUT_CELL	4
Unconnected	ENABLE	5
Unconnected	OUT_CELL	6
Unconnected	ENABLE	7
Unconnected	OUT_CELL	8
Unconnected	ENABLE	9
Unconnected	OUT_CELL	10
Unconnected	ENABLE	11
Unconnected	OUT_CELL	12
Unconnected	ENABLE	13
Unconnected	OUT_CELL	14
Unconnected	ENABLE	15
Unconnected	OUT_CELL	16
Unconnected	ENABLE	17
Unconnected	OUT_CELL	18
Unconnected	ENABLE	19
Unconnected	IN_CELL	20
Unconnected	IN_CELL	21
Unconnected	IN_CELL	22
Unconnected	IN_CELL	23
Unconnected	IN_CELL	24
Unconnected	IN_CELL	25
Unconnected	IN_CELL	26
Unconnected	IN_CELL	27

Pin/Enable	Cell Type	Register Bit
Unconnected	IN_CELL	28
Unconnected	IN_CELL	29
Unconnected	IN_CELL	30
Unconnected	IN_CELL	31
intb	OUT_CELL	32
oeb_intb	ENABLE	33
csb	IN_CELL	34
rdb	IN_CELL	35
wrb	IN_CELL	36
ale	IN_CELL	37
a[1]	IN_CELL	38
a[2]	IN_CELL	39
a[3]	IN_CELL	40
a[4]	IN_CELL	41
a[5]	IN_CELL	42
a[6]	IN_CELL	43
a[7]	IN_CELL	44
a[8]	IN_CELL	45
a[9]	IN_CELL	46
a[10]	IN_CELL	47
d[0]	IO_CELL	48
oeb_d[0]	ENABLE	49
d[1]	IO_CELL	50
oeb_d[1]	ENABLE	51
d[2]	IO_CELL	52
oeb_d[2]	ENABLE	53
d[3]	IO_CELL	54
oeb_d[3]	ENABLE	55
d[4]	IO_CELL	56
oeb_d[4]	ENABLE	57
d[5]	IO_CELL	58
oeb_d[5]	ENABLE	59
d[6]	IO_CELL	60
oeb_d[6]	ENABLE	61
d[7]	IO_CELL	62
oeb_d[7]	ENABLE	63
d[8]	IO_CELL	64
oeb_d[8]	ENABLE	65
d[9]	IO_CELL	66

Pin/Enable	Cell Type	Register Bit
oeb_d[9]	ENABLE	67
d[10]	IO_CELL	68
oeb_d[10]	ENABLE	69
d[11]	IO_CELL	70
oeb_d[11]	ENABLE	71
d[12]	IO_CELL	72
oeb_d[12]	ENABLE	73
d[13]	IO_CELL	74
oeb_d[13]	ENABLE	75
d[14]	IO_CELL	76
oeb_d[14]	ENABLE	77
d[15]	IO_CELL	78
oeb_d[15]	ENABLE	79
Unconnected	IN_CELL	80
Unconnected	IN_CELL	81
Unconnected	IN_CELL	82
Unconnected	IN_CELL	83
Unconnected	OUT_CELL	84
Unconnected	ENABLE	85
Unconnected	OUT_CELL	86
Unconnected	ENABLE	87
Unconnected	OUT_CELL	88
Unconnected	ENABLE	89
Unconnected	OUT_CELL	90
Unconnected	ENABLE	91
Unconnected	IN_CELL	92
Unconnected	IN_CELL	93
Unconnected	IN_CELL	94
Unconnected	IN_CELL	95
Unconnected	OUT_CELL	96
Unconnected	ENABLE	97
Unconnected	OUT_CELL	98
Unconnected	ENABLE	99
Unconnected	OUT_CELL	100
Unconnected	ENABLE	101
Unconnected	OUT_CELL	102
Unconnected	ENABLE	103
tprty	IO_CELL	104
oeb_tprty	ENABLE	105

Pin/Enable	Cell Type	Register Bit
tdat[0]	IO_CELL	106
oeb_tdat[0]	ENABLE	107
tdat[1]	IO_CELL	108
oeb_tdat[1]	ENABLE	109
tdat[2]	IO_CELL	110
oeb_tdat[2]	ENABLE	111
tdat[3]	IO_CELL	112
oeb_tdat[3]	ENABLE	113
tdat[4]	IO_CELL	114
oeb_tdat[4]	ENABLE	115
tdat[5]	IO_CELL	116
oeb_tdat[5]	ENABLE	117
tdat[6]	IO_CELL	118
oeb_tdat[6]	ENABLE	119
tdat[7]	IO_CELL	120
oeb_tdat[7]	ENABLE	121
tdat[8]	IO_CELL	122
oeb_tdat[8]	ENABLE	123
tclk	IN_CELL	124
tdat[9]	IO_CELL	125
oeb_tdat[9]	ENABLE	126
tdat[10]	IO_CELL	127
oeb_tdat[10]	ENABLE	128
tdat[11]	IO_CELL	129
oeb_tdat[11]	ENABLE	130
tdat[12]	IO_CELL	131
oeb_tdat[12]	ENABLE	132
tdat[13]	IO_CELL	133
oeb_tdat[13]	ENABLE	134
tdat[14]	IO_CELL	135
oeb_tdat[14]	ENABLE	136
tdat[15]	IO_CELL	137
oeb_tdat[15]	ENABLE	138
tsx	IO_CELL	139
oeb_tsx	ENABLE	140
tsop	IN_CELL	141
tcsb	IO_CELL	142
oeb_tcsb	ENABLE	143
tadr_scan[0]	IO_CELL	144

Pin/Enable	Cell Type	Register Bit
oeb_tadr_scan[0]	ENABLE	145
tadr_scan[1]	IO_CELL	146
oeb_tadr_scan[1]	ENABLE	147
tadr_scan[2]	IO_CELL	148
oeb_tadr_scan[2]	ENABLE	149
tadr_scan[3]	IO_CELL	150
oeb_tadr_scan[3]	ENABLE	151
tadr_scan[4]	IO_CELL	152
oeb_tadr_scan[4]	ENABLE	153
tadr_scan[5]	IO_CELL	154
oeb_tadr_scan[5]	ENABLE	155
tadr_scan[6]	IO_CELL	156
oeb_tadr_scan[6]	ENABLE	157
Unconnected	IN_CELL	158
Unconnected	IN_CELL	159
Unconnected	IN_CELL	160
Unconnected	IN_CELL	161
tenb	IN_CELL	162
tpa	OUT_CELL	163
oeb_tpa	ENABLE	164
rprty	IO_CELL	165
oeb_rprty	ENABLE	166
rdat[0]	IO_CELL	167
oeb_rdat[0]	ENABLE	168
rdat[1]	IO_CELL	169
oeb_rdat[1]	ENABLE	170
rdat[2]	IO_CELL	171
oeb_rdat[2]	ENABLE	172
rdat[3]	IO_CELL	173
oeb_rdat[3]	ENABLE	174
rdat[4]	IO_CELL	175
oeb_rdat[4]	ENABLE	176
rdat[5]	IO_CELL	177
oeb_rdat[5]	ENABLE	178
rdat[6]	IO_CELL	179
oeb_rdat[6]	ENABLE	180
rdat[7]	IO_CELL	181
oeb_rdat[7]	ENABLE	182
rdat[8]	IO_CELL	183

Pin/Enable	Cell Type	Register Bit
oeb_rdat[8]	ENABLE	184
rdat[9]	IO_CELL	185
oeb_rdat[9]	ENABLE	186
rdat[10]	IO_CELL	187
oeb_rdat[10]	ENABLE	188
rdat[11]	IO_CELL	189
oeb_rdat[11]	ENABLE	190
rdat[12]	IO_CELL	191
oeb_rdat[12]	ENABLE	192
rdat[13]	IO_CELL	193
oeb_rdat[13]	ENABLE	194
rdat[14]	IO_CELL	195
oeb_rdat[14]	ENABLE	196
rclk	IN_CELL	197
rdat[15]	IO_CELL	198
oeb_rdat[15]	ENABLE	199
rsx	IO_CELL	200
oeb_rsx	ENABLE	201
rsop	IO_CELL	202
oeb_rsop	ENABLE	203
rcsb	IO_CELL	204
oeb_rcsb	ENABLE	205
radr[0]	IO_CELL	206
oeb_radr[0]	ENABLE	207
radr[1]	IO_CELL	208
oeb_radr[1]	ENABLE	209
radr[2]	IO_CELL	210
oeb_radr[2]	ENABLE	211
radr[3]	IO_CELL	212
oeb_radr[3]	ENABLE	213
radr[4]	IO_CELL	214
oeb_radr[4]	ENABLE	215
renb	IN_CELL	216
rpa	OUT_CELL	217
oeb_rpa	ENABLE	218
Unconnected	IN_CELL	219
Unconnected	IN_CELL	220
Unconnected	IN_CELL	221
Unconnected	IN_CELL	222

Pin/Enable	Cell Type	Register Bit
Unconnected	IN_CELL	223
Unconnected	IN_CELL	224
Unconnected	IN_CELL	225
Unconnected	IN_CELL	226
Unconnected	IN_CELL	227
Unconnected	IN_CELL	228
Unconnected	IN_CELL	229
Unconnected	IN_CELL	230
Unconnected	IN_CELL	231
Unconnected	IN_CELL	232
Unconnected	IN_CELL	233
Unconnected	IN_CELL	234
oe	IN_CELL	235
rstb	IN_CELL	236
Unconnected	IN_CELL	237
Unconnected	IN_CELL	238
Unconnected	IN_CELL	239
Unconnected	IN_CELL	240
cbdq[0]	IO_CELL	241
oeb_cbdq[0]	ENABLE	242
cbdq[1]	IO_CELL	243
oeb_cbdq[1]	ENABLE	244
cbdq[2]	IO_CELL	245
oeb_cbdq[2]	ENABLE	246
cbdq[3]	IO_CELL	247
oeb_cbdq[3]	ENABLE	248
cbdq[4]	IO_CELL	249
oeb_cbdq[4]	ENABLE	250
cbdq[5]	IO_CELL	251
oeb_cbdq[5]	ENABLE	252
cbdq[6]	IO_CELL	253
oeb_cbdq[6]	ENABLE	254
cbdq[7]	IO_CELL	255
oeb_cbdq[7]	ENABLE	256
cbdq[8]	IO_CELL	257
oeb_cbdq[8]	ENABLE	258
cbdq[9]	IO_CELL	259
oeb_cbdq[9]	ENABLE	260
cbdq[10]	IO_CELL	261

Pin/Enable	Cell Type	Register Bit
oeb_cbdq[10]	ENABLE	262
cbdq[11]	IO_CELL	263
oeb_cbdq[11]	ENABLE	264
cbdq[12]	IO_CELL	265
oeb_cbdq[12]	ENABLE	266
cbdq[13]	IO_CELL	267
oeb_cbdq[13]	ENABLE	268
cbdq[14]	IO_CELL	269
oeb_cbdq[14]	ENABLE	270
cbdq[15]	IO_CELL	271
oeb_cbdq[15]	ENABLE	272
cbdqm	IO_CELL	273
oeb_cbdqm	ENABLE	274
cbbs	OUT_CELL	275
oeb_cbbs	ENABLE	276
Unconnected	OUT_CELL	277
Unconnected	ENABLE	278
cba[0]	IO_CELL	279
oeb_cba[0]	ENABLE	280
cba[1]	IO_CELL	281
oeb_cba[1]	ENABLE	282
cba[2]	IO_CELL	283
oeb_cba[2]	ENABLE	284
cba[3]	IO_CELL	285
oeb_cba[3]	ENABLE	286
cba[4]	IO_CELL	287
oeb_cba[4]	ENABLE	288
cba[5]	IO_CELL	289
oeb_cba[5]	ENABLE	290
cba[6]	IO_CELL	291
oeb_cba[6]	ENABLE	292
cba[7]	IO_CELL	293
oeb_cba[7]	ENABLE	294
cba[8]	IO_CELL	295
oeb_cba[8]	ENABLE	296
cba[9]	IO_CELL	297
oeb_cba[9]	ENABLE	298
cba[10]	IO_CELL	299
oeb_cba[10]	ENABLE	300

Pin/Enable	Cell Type	Register Bit
Unconnected	IO_CELL	301
Unconnected	ENABLE	302
cbweb	OUT_CELL	303
oeb_cbweb	ENABLE	304
cbcasb	OUT_CELL	305
oeb_cbcasb	ENABLE	306
cbrasb	OUT_CELL	307
oeb_cbrasb	ENABLE	308
cbcsb	OUT_CELL	309
oeb_cbcsb	ENABLE	310
sysclk	IN_CELL	311
Unconnected	IN_CELL	312
Unconnected	IN_CELL	313
Unconnected	IN_CELL	314
Unconnected	IN_CELL	315
Unconnected	IN_CELL	316
Unconnected	IN_CELL	317
Unconnected	IN_CELL	318
Unconnected	IN_CELL	319
Unconnected	IN_CELL	320
Unconnected	IN_CELL	321
Unconnected	IN_CELL	322
Unconnected	IN_CELL	323
Unconnected	IN_CELL	324
Unconnected	IN_CELL	325
Unconnected	IN_CELL	326
Unconnected	IN_CELL	327
Unconnected	IN_CELL	328
Unconnected	IN_CELL	329
Unconnected	IN_CELL	330
Unconnected	IN_CELL	331
Unconnected	IN_CELL	332
Unconnected	IN_CELL	333
Unconnected	IN_CELL	334
Unconnected	IN_CELL	335
Unconnected	IN_CELL	336
Unconnected	IN_CELL	337
Unconnected	IN_CELL	338
Unconnected	IN_CELL	339

Pin/Enable	Cell Type	Register Bit
Unconnected	IN_CELL	340
Unconnected	IN_CELL	341
Unconnected	IN_CELL	342
Unconnected	IN_CELL	343
Unconnected	IN_CELL	344
Unconnected	IN_CELL	345
Unconnected	IN_CELL	346
Unconnected	IN_CELL	347
rsdata[3]	IN_CELL	348
rsdata[2]	IN_CELL	349
rsdata[1]	IN_CELL	350
rsdata[0]	IN_CELL	351
rsclk[3]	IN_CELL	352
rsclk[2]	IN_CELL	353
rsclk[1]	IN_CELL	354
rsclk[0]	IN_CELL	355
Unconnected	IN_CELL	356
Unconnected	IN_CELL	357
Unconnected	IN_CELL	358
Unconnected	IN_CELL	359
Unconnected	IN_CELL	360
Unconnected	IN_CELL	361
Unconnected	IN_CELL	362
Unconnected	IN_CELL	363
Unconnected	IN_CELL	364
refclk	IN_CELL	365
Unconnected	IN_CELL	366
Unconnected	IN_CELL	367
Unconnected	IN_CELL	368
Unconnected	IN_CELL	369
Unconnected	IN_CELL	370
Unconnected	IN_CELL	371
Unconnected	OUT_CELL	372
Unconnected	ENABLE	373
Unconnected	OUT_CELL	374
Unconnected	ENABLE	375
Unconnected	OUT_CELL	376
Unconnected	ENABLE	377
Unconnected	OUT_CELL	378

Pin/Enable	Cell Type	Register Bit
Unconnected	ENABLE	379
Unconnected	OUT_CELL	380
Unconnected	ENABLE	381
Unconnected	OUT_CELL	382
Unconnected	ENABLE	383
Unconnected	OUT_CELL	384
Unconnected	ENABLE	385
Unconnected	OUT_CELL	386
Unconnected	ENABLE	387
Unconnected	OUT_CELL	388
Unconnected	ENABLE	389
Unconnected	OUT_CELL	390
Unconnected	ENABLE	391
Unconnected	OUT_CELL	392
Unconnected	ENABLE	393
Unconnected	OUT_CELL	394
Unconnected	ENABLE	395
tsdata[0]	OUT_CELL	396
oeb_tsdata[0]	ENABLE	397
tsdata[1]	OUT_CELL	398
oeb_tsdata[1]	ENABLE	399
tsdata[2]	OUT_CELL	400
oeb_tsdata[2]	ENABLE	401
tsdata[3]	OUT_CELL	402
oeb_tsdata[3]	ENABLE	403
Unconnected	OUT_CELL	404
Unconnected	ENABLE	405
Unconnected	OUT_CELL	406
Unconnected	ENABLE	407
Unconnected	OUT_CELL	408
Unconnected	ENABLE	409
Unconnected	OUT_CELL	410
Unconnected	ENABLE	411
ctsclk	IN_CELL	412
tsclk[0]	IN_CELL	413
tsclk[1]	IN_CELL	414
tsclk[2]	IN_CELL	415
tsclk[3]	IN_CELL	416
Unconnected	IN_CELL	417

Pin/Enable	Cell Type	Register Bit
Unconnected	IN_CELL	418
Unconnected	IN_CELL	419
Unconnected	IN_CELL	420
Unconnected	OUT_CELL	421
Unconnected	ENABLE	422
Unconnected	OUT_CELL	423
Unconnected	ENABLE	424
Unconnected	OUT_CELL	425
Unconnected	ENABLE	426
Unconnected	OUT_CELL	427
Unconnected	ENABLE	428
Unconnected	OUT_CELL	429
Unconnected	ENABLE	430
Unconnected	OUT_CELL	431
Unconnected	ENABLE	432
Unconnected	OUT_CELL	433
Unconnected	ENABLE	434
Unconnected	OUT_CELL	435
Unconnected	ENABLE	436

11.1.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table.

Figure 30 Input Observation Cell (IN_CELL)

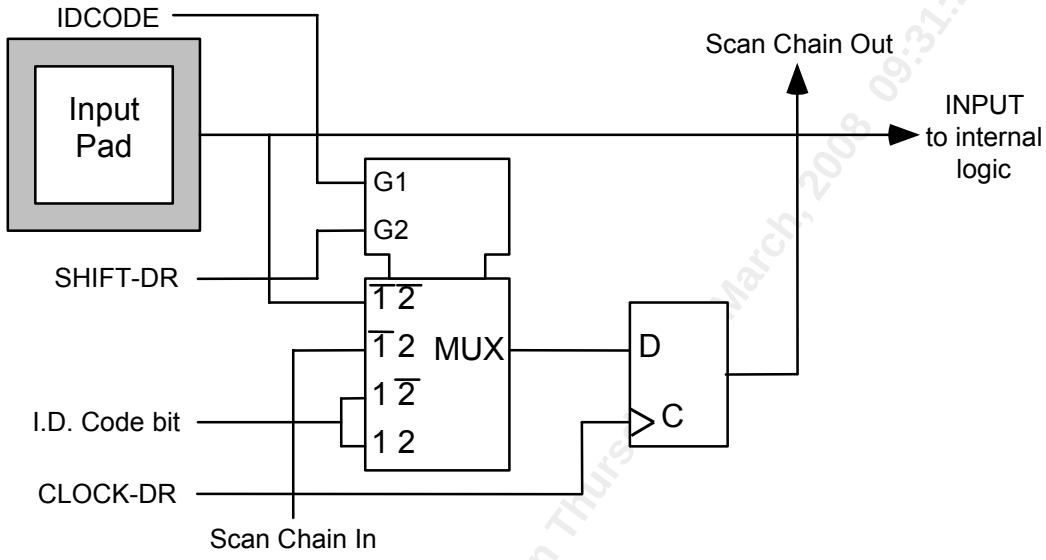


Figure 31 Output Cell (OUT_CELL)

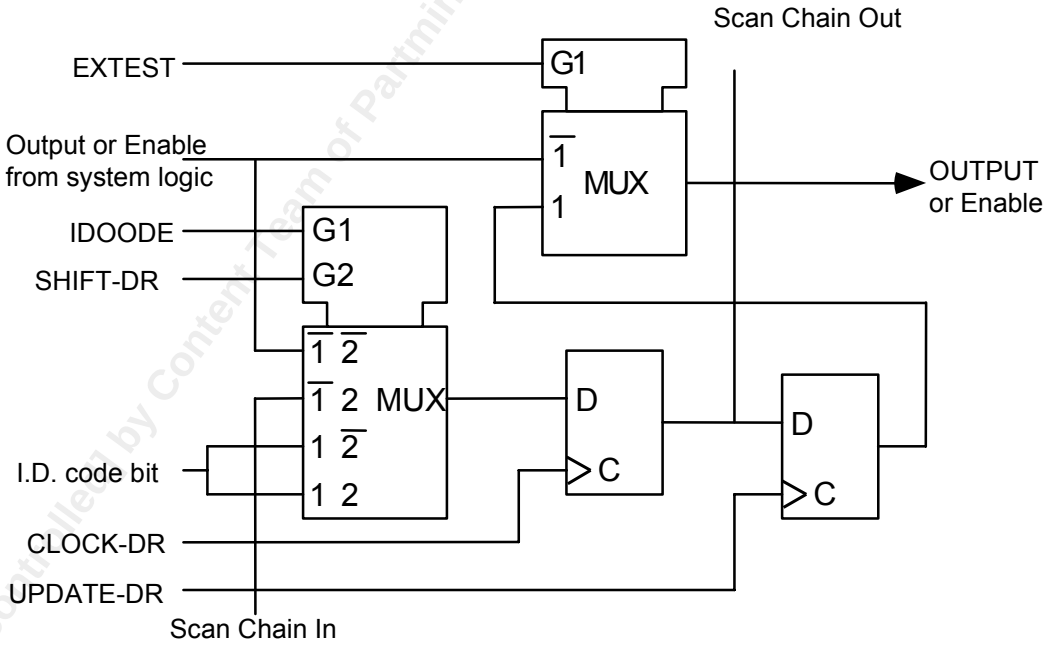


Figure 32 Bi-directional Cell (IO_CELL)

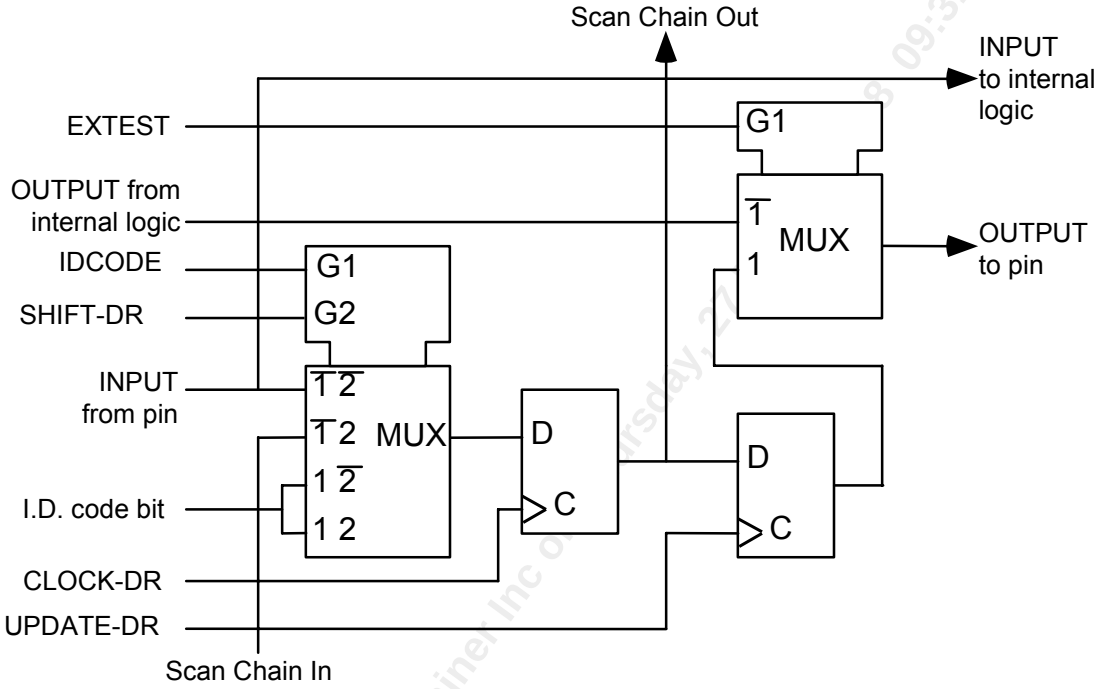
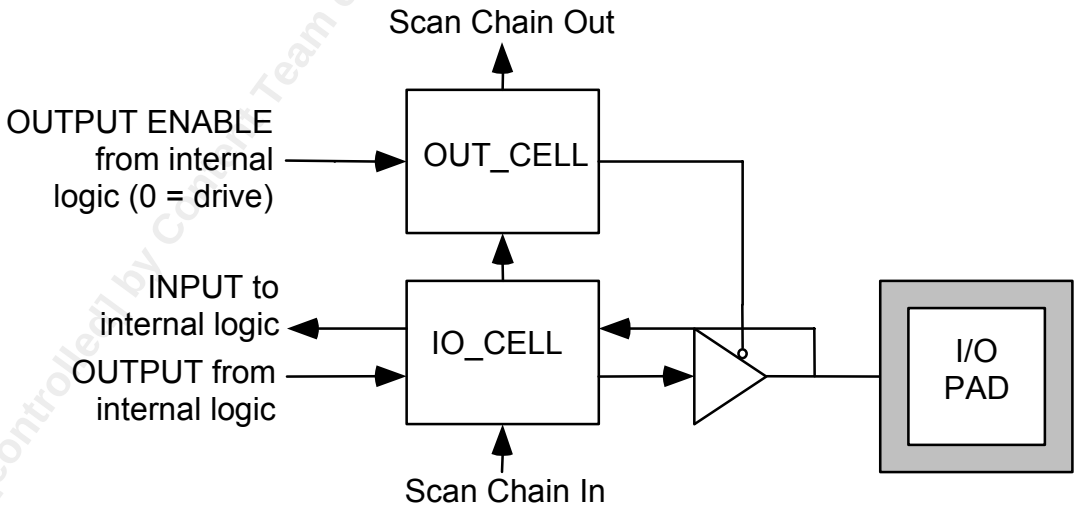


Figure 33 Layout of Output Enable and Bi-directional Cells



12 Operation

12.1 Hardware Configuration

The S/UNI IMA 4 device is powered up with the line interface disabled.

The Any-PHY/UTOPIA interface can also be set up in different modes. The Any-PHY/UTOPIA interface remains tri-state until configured and the respective RA_ENABLE/TA_ENABLE bits are set.

12.2 Startup

The S/UNI IMA 4 device uses an internal DLL on SYSCLK to maintain low skew on the external SDRAM interface. When the chip is taken out of hardware reset, the DLL goes into hunt mode and adjusts the internal SYSCLK until it aligns with the external SYSCLK. The microprocessor should poll the RUN bit in DLL CONTROL STATUS register until this bit is set.

At this point the entire chip with the exception of the microprocessor interface and the DLL are in reset. Before any configuration can be done, including accessing the ram, the chip must be taken out of software reset by clearing the RESET bit in the Global Reset Register. Once taken out of reset, the internal ram reset procedure is automatically initiated. The microprocessor should poll the BIST_DONE bit in the Global Reset register to determine when the internal RAM reset is complete. While the internal ram is initializing, access to all internal rams is prohibited, and accesses attempted during this period of time are ignored.

Once the chip is taken out of reset, the external SDRAM should be cleared to all zeros to ensure no false CRC errors are reported. Access to the SDRAM is through the SDRAM Diagnostic access port as described in 12.6.1. At this point, the Any-PHY/UTOPIA interface is disabled and all Any-PHY/UTOPIA outputs are tri-stated. Also, the line side interfaces are disabled and all internal registers are in their reset state.

12.3 Configuring the S/UNI IMA 4 Device

12.3.1 Configuring Clock/Data Interface

The Clock/Data interface has 2 major modes, Channelized for E1/T1 traffic and unchannelized for other traffic types.

Each link should be configured for channelized/unchannelized mode using the RCAS/TCAS link configuration registers. If configuring channelized links, the T1/E1 mode should be configured at the same time.

One configured, the links are still disabled. The links must be mapped and provisioned (enabled)

Channelized

When channelized links are chosen, the RCAS/TCAS Framing Bit threshold must be configured to detect the gap in the clock for the framing bit/byte. This value is dependent upon frame type T1/E1, serial clock speed and REFCLK frequency.

The Link Disable feature may be used when configuring a link to squelch all data from a link while it is being provisioned.

For the Tx direction, the data sent in idle timeslots may be selected with the TCAS Idle Time-slot Fill data.

For T1, all timeslots are used to carry the ATM cell data so all timeslots should be mapped to the same virtual link. A one-to-one mapping between physical links and virtual links is recommended.

For E1, timeslots 0 and 16 are used for signaling data and do not contain ATM cell data. Therefore, timeslots 1-15 and 17-31 must be mapped and provisioned (enabled) to carry ATM cell data. All of the timeslots in a link should be mapped to the same virtual link. A one-to-one mapping between physical links and virtual links is recommended.

For Fractional links, multiple fractional ATM flows may exist on the same physical link. Each flow should be mapped to a unique virtual link. There is a limit of 4 virtual links for the S/UNI IMA 4.

Unchannelized

Unchannelized is usually used for data streams that are not either T1 or E1 framed. When using the unchannelized interface, the user is responsible for providing a clock that has all framing or overhead bits gapped out. The S/UNI IMA 4 receives/sources one bit of data for each clock pulse.

The unchannelized mode allows a wider range of clock frequencies. As the serial line frequency increases, the number of links supported decreases.

Rules for Choosing Clock frequencies

For up to four lines running at frequencies up to 6.8 MHz each, REFCLK can be from 19.44 to 33 MHz, SYSCLK can be from 20 to 55 MHz, with the SYSCLK frequency greater than the REFCLK frequency.

$$\text{SYSCLK(min)} = \max\left(\frac{50MHz * Line.Throughput.Mbps}{130Mbps}, REFCLK.freq, 20MHz\right)$$

$$\text{REFCLK(min)} = \max\left(\frac{\left(14 + NumLines * \frac{4}{3}\right) * Line.Clock.Freq}{4}, 19.44MHz\right)$$

$$Num.Lines_{\max} \le \left(\left(\frac{4 * REFCLK.Freq}{Line.Clock.Freq}\right) - 14\right) * \frac{3}{4}$$

12.3.2 Configuring TC layer Options

TC layer options in the transmit direction include scrambling and HEC generations. Scrambling should be set as required by the physical layer.

TC layer options in the receive direction include descrambling, and interrupt reporting and error handling options. To properly support IMA applications, the TC layer functions should not filter out errored cells but pass them to the IMA-LAYER and let the IMA-LAYER filter them out. The options LCDOCDPASS, HCSPASS and UNASSPASS should be set for IMA applications.

For TC-only operations, the configuration of HCSPASS has no effect, as all HCS errored cells are dropped by the device regardless. LCDOCDPASS must be configured to drop for TC-only operations to ensure cells continue to be dropped when OCD is exited but LCD is not yet ended. IDLEPASS and UNASSPASS can be programmed according to the desired application in TC-only operations.

When running IMA, there should never be any idle cells. IDLEPASS must be set when running IMA to ensure correct defect event reporting in the absence of all other cells.

The configuration options are programmed one link at a time by following the RTTC/TTTC steps.

RTTC/TTTC Programming Steps:

1. For each write access, wait until the LBUSY bit in the RTTC/TTTC Indirect Status Register is clear. Note that the LBUSY bit might not be ready for up to 86 REFCLK cycle after an access.

2. Write to the RTTC/TTTC Link Data Register to specify the desired configuration options for that link.

3. Write into the RTTC/TTTC Indirect Status register specifying the LINK that is about to be configured and if this is to be a write or a read access, by clearing or setting the LWRB bit in this register.

12.3.3 UTOPIA Interface Configuration

There is little setup required to configure the Any-PHY/UTOPIA Interface. For typical operation, the following registers need to be written to select the mode of operation and the predefined address or address range of the S/UNI IMA 4 device and the number of active ports of the S/UNI IMA 4 device.

- Transmit Any-PHY/UTOPIA Cell available Enable.
- Receive UTOPIA Cell Available Enable.
- Transmit Any-PHY Address Config Register.
- Receive Any-PHY/UTOPIA Config Register.
- Transmit Any-PHY/UTOPIA Config Register.

Once the registers are written with the proper configuration information, the enable bit should be set to enable normal operation.

12.4 IMA_LAYER Configuration

12.4.1 Indirect access to internal memory tables

The IMA-Layer operations are configured by internal memory tables. The access to these tables is by indirect access. The following procedure applies for the indirect accesses in the RIPP, RDAT, TIMA, TXIDCC, and RXIDCC blocks.

Write accesses

The indirect write access procedure is as follows:

1. Wait until the "BUSY" bit in the *Block* Indirect Memory Access Control Register is clear.

2. Write to the *Block* Data Indirect Data Register(s) to specify the data to be written for that link.

3. Write into the *Block* Indirect Memory Address register specifying the address that is about to be configured and then write *Block* Indirect Memory Command register to specify the table to be accessed and if the access is to be a write or a read access, by clearing or setting the RWB bit in this register. Note that is some instances, the *Block* Indirect Memory Address register is combined with the *Block* Indirect Memory Access Control Register.

Read Accesses

The indirect read access procedure is as follows:

1. Wait until the "BUSY" bit in the *Block* Indirect Memory Access Control Register is clear.

2. Write into the *Block* Indirect Memory Address register specifying the address that is about to be configured and then write *Block* Indirect Memory Command register to specify the table to be accessed and if the access is to be a write or a read access, by clearing or setting the RWB bit in this register. Note that is some instances, the *Block* Indirect Memory Address register is combined with the *Block* Indirect Memory Access Control Register.

3. Poll the "Busy" bit in the *Block* Indirect Memory Access Control until it is cleared.

4. Read returned data from the *Block* Data Indirect Data Register(s).

12.4.2 Configuring Links for Transmission Convergence Operations

After all of the interfaces are configured, to configure a link for ATM over T1/E1, the mapping from physical link to Any-PHY/UTOPIA address must be set and the link must be set to TC mode within the IMA sublayer.

Also, all link-based statistics should be cleared.

For TC only links, all RIPP tables are not used and should not be programmed.

Transmitter

To map the physical link to an ANY-PHY/UTOPIA address, the VPHY address field must be programmed in the TIMA Physical Link Context Record for the physical link. All other fields in this table should be cleared to zero. This table may be accessed by the TIMA Indirect Memory access registers.

To put the physical link into TC mode set the TC_MODE bit in the TXIDCC. This bit may be accessed by the TXIDCC Indirect Memory Access registers.

Receiver

To map the physical link to an Any-PHY/UTOPIA address, the VPHY address field must be programmed in the RDAT TC Context Record for the physical link. All other fields in this table should be cleared to zero. This table may be accessed by the RDAT Indirect Memory access registers.

To put the physical link into TC mode, set the TC_MODE bit in the RXIDCC. This bit may be accessed by the RXIDCC Indirect Memory Access registers. Enabling the RXIDCC before the RDAT Validation Record ensures that the external FIFOs run at empty conditions, as designed.

The RDAT Link Statistics Record, the RDAT TC Group Statistics Record, the RDAT Link Context Record should also be cleared to zero to reset the statistic counts. The RDAT Validation Record should be set to TC_MODE.

Set the RDAT_EN bit in the RDAT CONFIGURATION register.

Removing Links from Transmission Convergence Operations

To disable a link in TC mode in the transmitter, the TC_MODE bit in the TXIDCC must be cleared. To disable a link in TC mode in the receiver, first the RDAT Validation Record should be cleared, then the TC_MODE bit in the RXIDCC must be cleared. This sequence ensures that transient interrupts are not generated.

12.4.3 Configuring For IMA Operations

All IMA timeouts are programmable. The actual timeout period may be one less than the specified timeout interval, due to the asynchronous nature of events with respect to the timer. For example, if the interval is 0.25 ns, and the timeout_value is specified as 4, then the timeout occurs after 0.75 ns to 1.00 ns in that state. To guarantee a timeout of at least 1 second, a value of 0x5 would have to be written (this is not the register default).

The global IMA interrupt enables default to disabled. In an interrupt driven system, these interrupt should be selectively enabled in registers 0x218, 0x21A, and 0x21C.

RIPP_EN in Register 0x200 controls if the internal IMA state machine's engine is enabled. This must be set for proper operation.

IMA groups are configured using the following per group tables:

- **RIPP Group Configuration Record**: Group options and configuration.
- TIMA TX-LID-to-Physical-Link Mapping Table: maps Group Tag/LID to physical Link.
- **TIMA TX Group Configuration Record**: maps group to Any-PHY/UTOPIA port ID, sets stuffing mode and OAM label.
- **RDAT IMA Group Context Record**: maps group to Any-PHY/UTOPIA port ID.

and also the following per link tables:

- **RIPP TX Link Configuration Record**: maps physical Link to Group Tag/LID, enables TX Link Interrupts.
- **RIPP RX Link Configuration Record**: maps physical Link to Group Tag, enables RX link interrupts.
- **TIMA TX Physical Link Context Record**: sets ICP offset.
- **RDAT Link Context Record**: maps physical link to group.

Configuring a Group for IMA

IMA groups within the S/UNI IMA 4 are identified by a "group tag". The group tag is an identifier with values from 0 to 3 that uniquely identifies the group for programming and reporting purposes within the S/UNI IMA 4. The group tag is completely independent of the Group ID located within the ICP cells.

Once a group tag is chosen for a group, the following records need to be programmed for the group:

- **RIPP Group Configuration Record**: Initial group options and configuration. After the group is started, the following configuration options may be changed only with a RIPP command or in conjunction with a group restart.
  - Expected OAM Label.
  - Group Symmetry.
  - IMA 1.1 versus IMA 1.0.
  - IMA ID.
  - M.
  - Expected Clk Mode (ITC/CTC).
  - The following entries within the **RIPP Group Configuration Record** may be changed without a group restart of RIPP command. When changing these fields, care must be taken not to change other fields.
  - Minimum # of Links.
  - Differential delay tolerance and options.
  - per group Interrupt enables.
  - Rx Physical links that are in the group.

Note that, to support a desired maximum expected network differential delay, the RX_DELAY_TOL parameter must meet the following requirement:

```
RX_DELAY_TOL > Max_network_diff_dly + RX_DELAY_GUARDBAND + Min_upper_guardband +
Min_lower_guardband
```

- **TX LID to Link Mapping Table:**
  - Select the LIDs to be used by the TX Links and program the physical links into the appropriate Group Tag/LID locations.
- **TIMA Group Configuration Record:**
  - TX VPHY ID
  - Stuff Advertise Mode
  - Actual stuffing mode(ITC/CTC) used
  - Transmitted OAM label
- **RDAT IMA Group Context Record**
  - RX VPHY ID
- **RIPP Group Context Record**
  - The PM should configure the RX_IMA_ID field during Group initialization if RX_IMA_ID_CFG_EN = 1. If RX_IMA_ID_CFG_EN = 0, RX_IMA_ID can be configured to 0.

  Also, while configuring a group, the context records that contain statistics should be initialized. The following records should be initialized to zero:

- RDAT IMA Group Statistics Record.
- TIMA Group Context Record.

Configuring a Link for IMA

All link-based records are indexed by the physical link ID.

Prior to configuring a link, the user should check to ensure that it is not in use already. This is necessary since link deletion from a group may take some time due to the necessity of allowing the DCB buffer for the link to drain. Reading the RX_ENABLE bit in the RIPP RX Link context record and the TX_ENABLE bit in the RIPP TX Link Context record can check this.

The following fields in the following records need to be programmed; other fields in the records should be cleared to zero.

- RIPP TX Link Configuration Record
  - TX_LID.
  - Group Tag.
  - per link Interrupt enables.
- RIPP RX Link Configuration Record
  - Group Tag.
  - per link Interrupt Enables.
- TIMA Physical Link Context Record
  - ICP Offset.
  - Startup Cell Count = b’111.
  - Previous_LSI = b’111.
  - CTC_CELL_COUNT as appropriate (see registers section).
- RDAT Link Context Record
  - Group Tag.

Also, while configuring a link, the context records that contain statistics and assorted context should be initialized to zero. The following records should be initialized to zero:

- RIPP TX Link Context Record.
- RIPP RX Link Context Record.
- RDAT Link Statistics Record.
- RDAT Link Validation Record.
- RXIDCC Link Data.
- TXIDCC Link Data.

In addition, the msg_status bit in the RDAT Link Message Status Record must be cleared using a read-modify-write operation. The other bits in the record contain link specific internal context that must be maintained. There is no contention for this memory between PM and the RDAT if the operation is performed while the link is not enabled for TC or IMA operation.

Note: If a link is being re-added to a group, and there are currently no active links in the group (i.e., the physical link was previously a member of the group, and was deleted), do not clear the RXIDCC Link Data. In this special case, the RXIDCC record contains import state information pertaining to the group that, if cleared, can prevent future link additions from succeeding.

12.5 IMA Operations

IMA operations are controlled via commands issued to the RIPP (Receive IMA protocol processor). In general, once started, the RIPP performs the hand shaking of state transitions between the near-end and far-end of an IMA connection.

12.5.1 Issuing a RIPP Command

The RIPP commands control the LSM and GSM state machines. The group is identified by the group tag and the links involved are identified with a 32-bit vector. The TX_LINK_VEC has one bit for each TX LID and bit 0 indicates TX LID 0 and bit 31 indicates TX LID31.

For symmetrical operations, the RX LIDs are not known until the ICP cells from a link are validated. The user controls the relationship between physical links and the RX Link vector through the RX Physical Link Table in the RIPP Group Configuration record. The RX physical Link Table should be configured according to the TX LID values. For example, the physical link ID for the Link with TX LID = 0 should be programmed as the RX physical link 0. When using the RIPP commands, the physical link entered for RX physical link 0 is controlled by bit 0 of the RX_LINK_VEC and the physical link entered for RX Physical link 31 in the table is controlled by bit 31 of the RX_LINK_VEC.

For asymmetric operations, since there is not a TX link for each possible RX link and the RX LIDs are not known until the ICP cells from a link are validated, the user controls the relationship between physical links and the RX Link vector through the RX Physical Link Table in the RIPP Group Configuration record. There are no restrictions on how this table should be configured in asymmetrical mode. The contents of the RX_PHY_TABLE do not depend on LID values. When using the RIPP commands, the physical link entered for RX physical link 0 is controlled by bit 0 of the RX_LINK_VEC and the physical link entered for RX Physical link 31 in the table is controlled by bit 31 of the RX_LINK_VEC.

The RIPP command procedure is as follows:

1. Wait until the “CMD_BUSY” bit in the RIPP Command Register is clear.

2. Once the CMD_BUSY bit is clear, write the necessary data for the command registers 0x222 - 0x22C (RIPP CMD_WR_DATA1 through RIPP CMD WR_DATA3).

3. Write the RIPP CMD Register with the command code and group tag for the command.

4. Poll the "CMD_BUSY" bit in the RIPP Command Register and when cleared, check the status of the command. Commands may be rejected when illegal actions are requested. An example of an illegal action is to start a LASR when one is already in progress.

5. If the command was a "Read_event" or "Read Delay", the returned data can now be read from the RIPP Command Data Register Array located at addresses 0x240 – 0x2BE.

12.5.2 Summary of RIPP Commands

The following is a summary of all RIPP commands that are currently supported. For the detailed command bit encoding info, refer to the "registers" section.

1. Add_group

Function	Add one new group to the device. Note that this must be the first command to be issued to the group, if any other command is issued prior to this, it is considered invalid and rejected.
Parameters	Group tag and vector of LIDS to be included in group
Pre-requisite	Require configuration of all link and group records as detailed in 0 and 0.
Restriction	None.

2. Delete_group

Function	Immediately remove an existing group and its links.
Parameters	Group Tag
Pre-requisite	None.
Restriction	None.

3. Restart_group

Function	Restart the specified group (GSM goes back to start-up state).
Parameters	Group Tag
Pre-requisite	If any group configuration information must be changed, PM must do so prior to issuing this command by writing to the RIPP Group Configuration memory.
Restriction	None

4. Inhibit_group

Function	Set the internal group inhibiting status flag. Once a group is considered inhibited, it does not go to OPERATIONAL state even if sufficient links exist in the group. If the group is already in OPERATIONAL state when the command is issued, the GSM goes to BLOCKED state and thus block the TX data path. However the RX data path remains on.
Parameters	Group Tag
Pre-requisite	None.
Restriction	None.

5. Not_inhibit_group

Function	Clear the internal group inhibiting status. If the group is currently in BLOCKED state and there are sufficient links in the group, the GSM goes to OPERATIONAL state.
Parameters	Group Tag
Pre-requisite	None.
Restriction	None.

6. Start_LASR

Function	Start LASR procedure on one or more links. The links involved may either be new links or existing links with a failure/fault/inhibiting condition. TX_LINK_VEC and RX_LINK_VEC are 32-bit vectors with the same bit mapping as TX_PHY_VALID or RX_PHY_VALID respectively, the bits corresponding to the new links are set to '1'. If the group configuration is symmetric, the TX_LINK_VEC and RX_LINK_VEC should be identical.
Parameters	Group Tag and vector of LIDS to be included in LASR
Pre-requisite	Link records need to be properly initialized by PM prior to issue this command. Also RDAT/TIMA must be initialized properly to reflect the new links, if any.
Restriction	This command is rejected if there is currently an active group-wide procedure for the same group, such as Restart_group or Start_LASR.

7. Delete_link

Function	Remove links from the group. The TX_LINK_VEC and RX_LINK_VEC fields indicate the links to be removed. If the group configuration is symmetric, the TX_LINK_VEC and RX_LINK_VEC should be identical.
Parameters	Group Tag and vector of LIDS to be deleted
Pre-requisite	None.
Restriction	Deletion of a TRL Link is a special case. A group cannot operate normally without both the TX TRL and the RX TRL. Therefore, the TRL link should not be deleted unless it is the last link in the direction. Also, IMA protocol requires there to be at least one link in both directions, therefore PM should not delete the last link left in either direction in cases other than a complete group removal.

8. Set_rx_phy_defect

Function	Indicate to RIPP that the given link(s) have/have no physical defects (such as LOS/AIS) which are not detectable internally. TX_LINK_VEC and RX_LINK_VEC indicate the links affected.
Parameters	Group Tag and vector of LIDS to be included in group
Pre-requisite	None.
Restriction	None.

9. Unusable_link

Function	Indicate to RIPP that the given link(s) are unusable for certain reasons. TX_LINK_VEC and RX_LINK_VEC indicate the links affected. TX_CAUSE and RX_CAUSE indicate the reason for the link to be UNUSABLE. Note it is possible to change the cause for the link to be unusable even after it enters the unusable state.

Parameters	Group Tag and vector of LIDS to be made unusable and the cause to report why the link is unusable
Pre-requisite	None.
Restriction	It is required that PM must use one of the four defined causes (failed, fault, mis-connected, inhibited) if an unusable cause is to be reported to the far-end via the ICP cell.

10. Update_test_ptn

Function	Update the TX test pattern info to be sent in the outgoing ICP cells for the group. This command also causes the SCCI field in the next outgoing ICP cell to increase.
Parameters	Group Tag and TX Test pattern and Test pattern LID
Pre-requisite	None.
Restriction	None.

11. Update_tx_trl

Function	Update the transmit timing information (TX TRL and clock mode) to be sent in the outgoing ICP cells. The TRL is also used to control the TX IDCC. This command also causes the SCCI field in the next outgoing ICP cell to increase.
Parameters	Group Tag and LID for new TRL
Pre-requisite	None.
Restriction	It is up to the user to pick a valid TRL to satisfy the requirement in the IMA spec. At least, a TRL that is currently configured to be in the group should be selected; otherwise the group cannot operate normally. Any previous add_group or Start_LASR operations for this group must be completed prior to changing the transmit TRL.

12. Read_event

Function	Read and clear the latched event status of the specified group and all its' links. The result read from the internal context memory is stored in Cmd_rd_data00 through cmd_rd_data1F. Refer to the “registers” section for further details.
Parameters	Group Tag
Pre-requisite	None.
Restriction	This command is rejected on Deleted groups.

13. Read_delay

Function	Read all the DCB write pointers and link defect status of all links in the specified group. The result is stored in Cmd_rd_data00 through cmd_rd_data1F. Refer to the “registers” section for further details.
Parameters	Group Tag
Pre-requisite	None.
Restriction	None.

14. Adjust_delay

Function	Start an adjust_delay procedure on the specified group. The amount of delay to be removed/added is specified as part of parameters.

Parameters	Group Tag and amount of delay in cells
Pre-requisite	None.
Restriction	This command is rejected if there is currently another adjust_delay procedure in progress or if there is currently a group-wide procedure (group start-up or LASR) in progress for the same group.

12.5.3 Adding a Group

Prior to issuing this command, the RX_LINK_EN bits and TX_LINK_EN bits in the RIPP Link Context should be checked to make sure they are zero (this indicates that, if these links were previously in another group, the previous delete link operation is complete). Then, the Group and Link configuration should be performed. Next, the Add_Group command should be issued. This command initiates the Group and Link State Machines. Is starts the GSM arbitration and automatically starts a LASR procedure.

The Add_Group command continues after the CMD_ACK is returned. The completion of the command is generally indicated by an event that indicated either that the process timed-out or the group has become operational. If a timeout occurs, PM should take appropriate action and either restart the group with new parameters or add additional links to the group.

The event that indicates that the Add_Group command has completed successfully is either the GTSM_INT with the GTSM state = Operational or GSM_INT with the GSM state = Operational.

Events that indicate that the Add_Group command has completed but was not successful are the following:

- NE_ABORT_INT
- FE_ABORT_INT
- GRoup_TIMEOUT_INT
- FE_TIMEOUT_INT

Events that indicate that individual links are experiencing problems and did not become active are the following:

- DIFF_DELAY_INT
- INVALID_ICP_INT
- RX_TIMEOUT_INT
- TX_TIMEOUT_INT

To track the progress of the command, interrupts may be enabled for GSM state changes and for the LSM state changes for all of the links. This may result in a large number of events if the group includes a large number of links.

If the TRL link is not validated on the RX side, since the group does not have a valid TRL, the group does not come up and reports GROUP_TIMEOUT_INT, and FE_TRL_STATUS should remain zero. This occurs when the receive physical link corresponding to the far end transmit TRL LID is not connected.

12.5.4 Deleting a Group

There are two methods of bringing a group down. To bring a group down and preserve data that has already been transmitted, it is recommended that the links be deleted first using the Delete_link command. This results in the GSM transitioning to the insufficient links state when the number of active links falls below the minimum required links. Once the delete links is complete and all of the accumulated DCB data is played out, the Delete_group command deletes the existing group. To determine if the deleted links have all of the DCB data played out, the TX_LINK_EN and RX_LINK_EN bits may be polled in the RIPP Link Context records. Once the Delete_group command is executed, all links within the group immediately stops transmitting IMA frames, and all received cells queued in the DCB buffer are dropped.

If data preservation is not a concern, a group may be removed immediately by issuing the Delete_group command. It is recommended that interrupts be disabled prior to the group deletion since the group deletion itself causes an interrupt to occur. If a Read_event command is issued on a deleted group, the command is rejected. If interrupts are not disabled, care must be taken to ensure proper servicing of the RIPP Interrupt FIFO prior to reusing the group to avoid overrunning the RIPP Interrupt FIFO (interrupt from group prior to deletion and interrupt from group after re-use both in FIFO, and the FIFO is sized to have a maximum of one event per group.)

12.5.5 Restart Group

To restart a group or issue a local reset to a group, the Restart_group command is used. Upon a Restart_group, the specified group's GSM immediately transitions to the Start-up state and tries to renegotiate the IMA parameters. This command should be used after changing the M values, IMA ID, group symmetry, or OAM value on a group.

12.5.6 Inhibit Group/Not inhibit Group

To move a GSM into/out of the Blocked state, the Inhibit_group and Not_inhibit_group commands may be used. These commands set a mode such that the current GSM state is not important. Once set to the inhibit mode, the GSM goes to the Blocked state instead of the Operational state. The Not_inhibit_group command must be executed to remove this setting.

12.5.7 Adding a link or Links to an Existing Group (Start LASR)

To add links to an existing group, the START_LASR command is used. Prior to issuing this command, the RX_LINK_EN bits and TX_LINK_EN bits in the RIPP Link Context should be checked to make sure they are zero (this indicates that, if these links were previously in another group, the previous delete link operation is complete). Then, the link configuration should be performed as in 0. The Start_LASR command initiates the Link Addition and Slow Recovery Procedure. The LASR procedure is paced by either (1) all of the indicated links' LSM's transitioning to the appropriate states or (2) the programmed link timeouts in the presence of defective or slow links.

The LASR procedure continues after the CMD_ACK is returned. While a LASR procedure is in process, no other LASR procedure may be started on the same group.

The completion of the command is generally indicated by an event that indicated either that the process timed-out or the links have become operational. If a timeout occurs, PM should take appropriate action and either restart the LASR procedure in the case that the handshaking was just slow or replace defective links.

The event that indicates that the Start_LASR command has completed successfully for symmetrical groups is the TX_ACTIVE_INT for all links involved. Due to the group-wide synchronization, this event should occur for all links simultaneously. For asymmetrical groups, the RX_ACTIVE_INT indicates the completion of the LASR for receive links.

Events that indicate that individual links are experiencing problems and did not become active are the following:

- DIFF_DELAY_INT
- INVALID_ICP_INT
- RX_TIMEOUT_INT
- TX_TIMEOUT_INT

If a link is rejected with a DIFF_DELAY_INT, and the "rx_add_delay_en" is disabled in the RIPP group configuration memory, then it may be possible to correct the problem and recover the link. A "read_delay" command can be issued after the LASR is completed to determine the differential delay profile for the group. If the new link appears to be above the RX_DELAY_TOL, the RX_DELAY_TOL can be increased, or delay may be removed from the group (as described in section 12.5.13), as long as this does not cause the current slowest link to detect an LODS_UNDERRUN (i.e., resulting depth is less than MIN_LOWER_GUARDBAND). If the new link appears to be below the MIN_LOWER_GUARDBAND (or negative in delay), then delay may be added to the group (as described in section 12.5.14), as long as this does not cause the current fastest link to detect an LODS_OVERRUN (i.e., resulting depth is greater than RX_DELAY_TOL – MIN_UPPER_GUARDBAND). Once these measures are taken, a new LASR operation may be initiated (link recovery), and this link should then be accepted into the group.

Note that if a link is rejected during link addition due to differential delay problems, the DIFF_DELAY_INT is issued, but the LODS_OVERRUN_INT and LODS_UNDERRUN_INT is not set, as these interrupts are only evaluated after successful link addition.

If a timeout event occurs, another LASR procedure must be execute to continue attempting to bring links to the active state.

Note that the LIF_INT is automatically masked by the device during a group-wide procedure that includes this link, such as add_group, Restart_group, or Start_LASR (for link addition and link recovery). Therefore, the LIF_INT may not be used to determine the success of the link addition. Also, note that, once a link is rejected, LIF is not reevaluated until another LASR procedure is executed (attempts at IMA framing are halted once the LASR experiences timeout).

To track the progress of the command interrupts may be enable the LSM state changes for all of the links. This may result in a large number of events if the group includes a large number of links.

12.5.8 Reporting Link Defects in the ICP Cell

LIF, LODS, and LCD defects are automatically detected and reported in the ICP cell by the S/UNI IMA 4. Other physical layer defects such as LOS, OOF, and AIS are not detected by the S/UNI IMA 4. To enable reporting of these defects, the Set_rx_defect command is provided to force the contents of the RDI field in the ICP cell. When the defect bit is set in the command, this also sets an internal state which prevents the affected LSM's from progressing towards active (until the unusable_link command is issued), and immediately terminates any currently active timers which are waiting on FE state changes for the affected LSM's. The termination of these timers (such as RX_link_deleted_timeout, RX_link_blocked_timeout, or TX_link_deleted_timeout) may result in an immediate NE LSM state change.

12.5.9 Faulting/Inhibiting Links

The S/UNI IMA 4 reports defects to the upper layer S/W and allows the upper layer S/W declare fault conditions based upon defect information. To force a link into a Fault or Failure state, the Unusable_Link command is used. This link can operate on multiple links at a time. Once executed, the LSM of the affected links are transitioned to the Unusable state. If inhibiting the link without data loss is required, it is necessary to specify the cause as "inhibited". Normally when inhibiting a link, the link is active for a while. If a link is inhibited immediately after becoming active, data loss can occur. If the S/UNI IMA 4 device is not yet received ICP cells from the link that indicates the link is active when the link is inhibited, data loss may occur. Note that links currently experiencing defect conditions still experience loss of data even when inhibiting. When links are faulted, the existing data within the DCB is still played out on the ATM interface.

12.5.10 Change TRL

To change the TRL link, the Update_TRL command is used. The new TRL is immediately used for scheduling the group and is reported as the TRL in the next ICP cell. If CTC timing is used, the stuffing is not affected. If ITC timing is used, the reference link is changed to the new TRL. The first stuff on the new TRL occurs on approximately the same frame as the stuff that would have occurred when it was a non-reference link. After the first stuff on the new TRL, the new TRL is stuffed every 2049 cells.

12.5.11 Deleting a Link from a Group

A link can be deleted from a group by using the delete Link command. On the transmit side, the link stops accepting ATM cells immediately and transmits filler cells only. The links are removed from the TX round robin on the next frame boundary. On the receive side, the deleted link/links transition to the Deleted state to ensure that all transmitted data is received into the DCB buffer. Once the FE TX state is detected as not active or the RX_LINK_DELETED timeout occurs, the RX links stop writing data to the DCB buffers. The DCB buffers allowed to underrun (preserving any previously stored data) prior to being disabled and removed from the receive round robin. The RX_LINK_EN bits and TX_LINK_EN bits in the RIPP Link context records should be monitored to determine when the links can be reassigned to a different group.

12.5.12 Test Pattern Procedures

The test pattern procedure consists of two parts, issuing the test pattern and checking the test pattern.

To issue a test pattern, the Update_test_ptn command is used. This starts the transmission of the new test pattern. PM must take care to wait at least two frames in between updates to the test pattern to comply with the IMA test pattern standard. The S/UNI IMA 4 device loops back the test pattern indicated in the ICP cell.

Since each link may experience different round trip delays, the checking of the test pattern is split between the user and the S/UNI IMA 4 device. The S/UNI IMA 4 device compares test pattern received in the ICP cell with the test pattern that was sent on every received ICP cell. The S/UNI IMA 4 device stores the success or failure of this operation in the word 9 of the RIPP Group Context register. The user is responsible for checking the results after a sufficient time has passed for a round trip delay on all links.

12.5.13 Removing Accumulated Delay from a Group

In certain situations, such as when the RX_ADD_DELAY_EN is enabled, a group may accumulate delay over time (after multiple LASR operations). A group may also accumulate delay due to many changes of far end transmit TRL LID (due to slight rate inaccuracies that accumulate when switching references). It may also be desirable to remove delay if a link is rejected from a LASR operation with a DIFF_DELAY_INT (and rx_add_delay_en is disabled for the group). To remove unwanted delay, the adjust_delay command can be issued. A read_delay command may be issued to determine the smallest amount of delay in the group (associated with the link with the longest transport delay). The maximum amount of delay that may be removed from the group without causing LODS on links in the group is:

Actual delay (A) = Min(group depths) – Min_lower_guardband

The Min_lower_guardband is specified in register 0x208, and defaults to a value of 3. Due to internal deration of the scheduling rate associated with ICP cells, the device derates the requested delay specified (R) with the command:

A = R * (M/(M-1)), where M is the frame length (32, 64, 128, 256)

To account for this, the requested delay must be appropriately derated:

R = A * ((M-1)/M)

To summarize, the maximum requested delay is defined:

R = [Min(group_depths) – Min_lower_guardband] * ((M-1/M)

12.5.14 Adding Delay to a Group

In certain situations, such as when many changes of far end transmit TRL LID occur (due to slight rate inaccuracies that accumulate when switching references), delay may need to be added to a group (either in response to an LODS underrun condition or to prevent one from occurring). This may also be desirable if a link is rejected from a LASR operation with a DIFF_DELAY_INT (and rx_add_delay_en is disabled for the group). To add delay, the adjust_delay command can be issued. A read_delay command may be issued to determine the largest amount of delay in the group (associated with the link with the smallest transport delay). The maximum amount of delay that may be added to the group without causing LODS on links in the group is:

Actual delay (A) = RX_DELAY_TOL - Max(group depths) – Min_upper_guardband

The Min_upper_guardband is specified in register 0x208, and defaults to a value of 3. The RX_DELAY_TOL is specified in the RIPP Group Configuration Table. Due to internal deration of the scheduling rate associated with ICP cells, the device derates the requested delay specified (R) with the command:

A = R * (M/(M-1)), where M is the frame length (32, 64, 128, 256)

To account for this, the requested delay must be appropriately derated:

R = A * ((M-1)/M)

To summarize, the maximum requested delay is defined:

R = [RX_DELAY_TOL - Max(group depths) – Min_upper_guardband] * ((M-1/M)

12.5.15 IMA Events

All of IMA events are reported via a group-based structure. IMA events include link defects and link and group state machine changes. Any enabled IMA event causes a RIPP_INTR. All IMA events may be enabled for reporting at the Group/link level as well as a globally. Both the individual link/group enable as well as the global enable must be set to have an IMA event cause an RIPP_INTR.

As enabled IMA events occur, a message is placed with the RIPP_INTR FIFO. Once a message is placed with the FIFO, another message is not generated until the read_event command is executed for the group. During this period of time, additional events can accumulate and are reported with the Read_event command when executed. The Read_event command queries the links within the group and provides all of the link and group information in a single data structure. To ease the processing load, a map that shows which links are experiencing INTR conditions is provided in page 0 of the returned status. Page 1 contains the interrupt conditions and Page 2 provides the status. The majority of the error/interrupt processing may be performed with the information provided by the Read_event command.

12.5.16 End-to-end Channel Communication

According to the IMA specification, end-to-end channel is a proprietary communication channel via the corresponding field in the ICP cells. The S/UNI IMA 4 device provides access to this facility through the following means:

- In the outgoing direction, the end-to-end channel may be updated by writing to the TX_END_CHANNEL field in the RIPP group configuration record at any time.
- In the incoming direction, the end-to-end channel information may be accessed by reading the ICP cell buffer memory.

12.6 Diagnostic features

12.6.1 ICP Cell Trace

The S/UNI IMA 4 device can be configured to forward incoming ICP cells to microprocessor, by setting the proper bits in the RIPP Group Configuration memory. The content of the forwarded ICP cell is stored in the ICP cell buffer registers.

The ICP cell data exchange between RIPP and the microprocessor is controlled via the use of a lock bit (which is located in the ICP cell forwarding Control register) and the PM_ICP_AVL interrupt. The data exchange protocol is as follows:

1. S/UNI IMA 4 device sees a new ICP cell and starts polling the lock bit.
2. If the lock bit is current set, the cell is not forwarded.
3. The ICP cell data content is copied to the ICP cell buffer registers.
4. The PM_ICP_AVL bit is set, this causes an ICP_CELL_AVL_INT.
5. To read the ICP cell, the lock bit must be set by writing '1' to the ICP_FWD_LOCK_REQ bit in the ICP forwarding control register. Once the lock is granted when the ICP_FWD_LOCK_GRANT bit read back as '1'. The lock bit must be set prior to clearing the interrupt, otherwise it is possible to have multiple interrupt generated.
6. The interrupt should be cleared by reading the ICP cell forwarding status register.
7. The data may be readout from Forwarding ICP cell buffer registers.
8. The ICP_FWD_LOCK_REQ should be cleared bit by writing to the register location.

12.6.2 SDRAM Diagnostic Access

Diagnostic access of the external SDRAM is provided to enable SDRAM initialization and testing. The access to the SDRAM is provided on a cell buffer granularity. Each cell buffer is 64 bytes. By providing cell buffer burst access to the SDRAM, the SDRAM diagnostic accesses use the same burst access timing as is used when the S/UNI IMA 4 device is operating.

Prior to performing any diagnostic accesses to the SDRAM, the SDRAM interface must be placed in diagnostic mode. In diagnostic mode, all automatic accesses from the S/UNI IMA 4 device (except refresh) are disabled and all accesses are controlled via the microprocessor interface.

To write to the SDRAM, first the image of the cell must be written into the SDRAM DIAG Burst-Write RAM using the SDRAM DIAG Burst RAM Indirect Access. Once the image of the cell is written, a command to transfer the data into the external SDRAM should be issued using the SDRAM DIAG WRITE CMD registers. The SDRAM DIAG WRITE CMD registers specify the address of the cell buffer to be written in the external SDRAM.

For a read operation, a read command is issued using the SDRAM DIAG READ CMD registers. This command transfers data from the SDRAM into the internal cell buffer. When the command is complete as indicated by the RDBUSY bit in the command register, the data may be read out of the cell buffer using the SDRAM DIAG Burst RAM indirect access.

Note that there is no CRC protection for data in diagnostic mode.

By providing both Read Command registers and write command registers, a back-to-back read/write access may be performed to the SDRAM.

12.7 IMA Performance Parameters and Failure Alarms Support

A number of IMA performance parameters and failure alarms are defined in the IMA spec (section 12.2.2) as a standardized interface to IMA unit management functions. The following text summarizes the support provided by S/UNI IMA 4 device to implement those functions.

Table 38 IMA Performance Parameter Support

Req.	Performance parameter	S/UNI IMA 4 support
R-125	IV-IMA	
O-20	OIF-IMA	
R-126	SES-IMA	NE RX IMA defects cause interrupts.
R-127	SES-IMA-FE	RDI-IMA defects cause interrupts.
R-128	UAS-IMA	Derived from SES-IMA, no support.
R-129	UAS-IMA-FE	Derived from SES-IMA-FE, no support.
R-130	TX-UUS-IMA	S/UNI IMA 4 provides read access to the TX LSM in RIPP link context records. Note after link start-up, it is up to PM to put the LSM into UNUSABLE state.
R-131	RX-UUS-IMA	S/UNI IMA 4 provides read access to the RX LSM in link context records. Note after link start-up, it is up to PM to put the LSM into UNUSABLE state.
R-132	TX-UUS-IMA-FE	S/UNI IMA 4 may generate an interrupt once FE TX LSM enters UNUSABLE state.
R-133	RX-UUS-IMA-FE	S/UNI IMA 4 may generate an interrupt once FE RX LSM enters UNUSABLE state.
R-134	TX-FC	Failure condition is declared by PM, no support provided.
R-135	RX-FC	Failure condition is declared by PM, no support provided.
O-21	TX-FC-FE	S/UNI IMA 4 may generate an interrupt once FE TX LSM is in UNUSABLE state, PM may then read the FE LSM state in the RIPP context memory to determine the case.
O-22	RX-FC-FE	S/UNI IMA 4 may generate an interrupt once FE RX LSM is in UNUSABLE state, or an RDI-IMA indication is sent by FE.
O-23	TX-STUFF-IMA	S/UNI IMA 4 provides counter of inserted stuff events per link.
O-24	RX-STUFF-IMA	S/UNI IMA 4 provide counter of received stuff events per link
R-136	GR-UAS-IMA	S/UNI IMA 4 may generate an interrupt when a GTSM transition happens.

Req.	Performance parameter	S/UNI IMA 4 support
R-137	GR-FC	S/UNI IMA 4 provides interrupt and read access to internal context for various error conditions. See Table 39 for details.
O-25	GR-FC-FE	S/UNI IMA 4 provides interrupt and read access to internal context for various error conditions. See Table 39 for details.

Table 39 IMA Failure Alarm Support

Req.	Failure Alarm	S/UNI IMA 4 support
R-138	LIF	The S/UNI IMA 4 device may generate an interrupt and latch the internal LIF error status once a link enters or exits LIF defect.
R-139	LODS	The S/UNI IMA 4 device may generate an interrupt and latch the internal LODS error status once a link enters or exits LODS defect.
R-140	RFI-IMA	The S/UNI IMA 4 device may generate an interrupt and latch the internal RDI-IMA status when RDI-IMA condition is entered or exited on a TX link. It is up PM to declare the alarm condition.
R-141	TX-Mis-Connected	It is up to PM to detect misconnectivity on TX links, possibly through the use of test patterns. FE may indicate that the link is misconnected by moving the RX LSM to corresponding UNUSABLE state. RIPP then generates an interrupt and latch the error status.
R-142	RX-Mis-Connected	It is up to PM to detect misconnectivity on RX links. One possible way is to use the RX_IMA_ID field in the group context. Instead of letting RIPP capture the RX_IMA_ID from incoming ICP cells, PM can choose to initialize the group context with a expected RX_IMA_ID and set the RX_IMA_ID_VALID field to '1'. In this case the misconnected RX links likely has a wrong IMA ID value and does not come up, which eventually causes an interrupt. Also PM may use the test pattern procedure for this purpose.
O-28	TX-Fault	It is up to PM to declare fault conditions on TX links. To facilitate this, RIPP provides read access to the NE/FE LSM and GSM states in the context memory.
O-29	RX-Fault	It is up to PM to declare fault conditions on RX links. To facilitate this, RIPP provides read access to the NE/FE LSM and GSM states in the context memory.
R-143	TX-Unusable-FE	The S/UNI IMA 4 device may generate an interrupt and latch the internal FE_TX_Unusable error status, once FE TX LSM enters UNUSABLE state.
R-144	RX-Unusable-FE	The S/UNI IMA 4 device may generate an interrupt and latch the internal FE_RX_Unusable error status, once FE RX LSM enters UNUSABLE state.

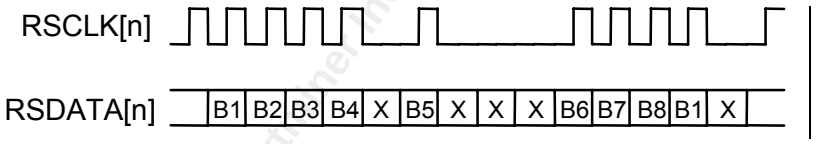
Req.	Failure Alarm	S/UNI IMA 4 support
R-145	Start-up-FE	The S/UNI IMA 4 device may generate an interrupt if a FE GSM state transition occurs. PM may then read the FE GSM state from the RIPP context memory.
R-146	Config-Aborted	The S/UNI IMA 4 device may generate an interrupt and latch the internal Config-Aborted error status, once it decides the FE parameters are unacceptable and the GSM should go to Config-Aborted state.
R-147	Config-Aborted-FE	The S/UNI IMA 4 device may generate an interrupt and latch the internal Config-Aborted-FE error status, once it detects the FE GSM is in Config-Aborted state.
R-148	Insufficient-Links	The S/UNI IMA 4 device may generate an interrupt if GSM state transition occurs. PM may then read the GSM state from the RIPP context memory.
R-149	Insufficient-Links-FE	The S/UNI IMA 4 device may generate an interrupt if a FE GSM state transition occurs. PM may then read the FE GSM state from the RIPP context memory.
R-150	Blocked-FE	The S/UNI IMA 4 device may generate an interrupt if a FE GSM state transition occurs. PM may then read the FE GSM state from the RIPP context memory.
R-151	GR-Timing-Mis-match	The S/UNI IMA 4 device may generate an interrupt and latch the relevant error status, once it detects a mismatch between TX and RX clock modes.

13 Functional Timing

13.1 Receive Link Input Timing

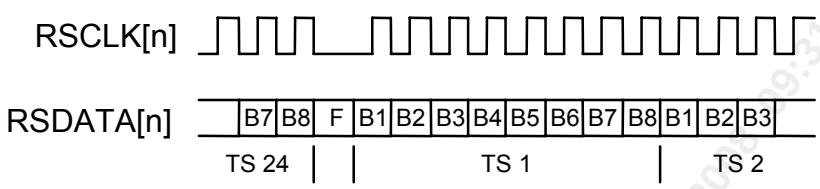
The timing relationship of the receive clock (RSCLK[n]) and data (RSDATA[n]) signals of an unchannelized link is shown in Figure 34. The receive data is viewed as a contiguous serial stream. There is no concept of time-slots in an unchannelized link. Each eight bits is grouped together into a byte with arbitrary alignment. The first bit received (B1 in Figure 34) is deemed the most significant bit of an octet. The last bit received (B8) is deemed the least significant bit. Bits that are to be processed by the S/UNI IMA 4 device are clocked in on the rising edge of RSCLK[n]. Bits that should be ignored (X in Figure 34) are squelched by holding RSCLK[n] quiescent. In Figure 34, the quiescent period is shown to be a low level on RSCLK[n]. A high level, affected by extending the high phase of the previous valid bit, is also acceptable. Selection of bits for processing is arbitrary and is not subject to any byte alignment or frame boundary considerations.

Figure 34 Unchannelized Receive Link Timing



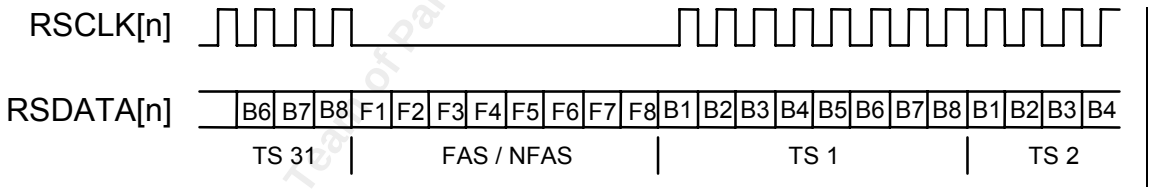
The timing relationship of the receive clock (RSCLK[n]) and data (RSDATA[n]) signals of a channelized T1 link is shown in Figure 35. The receive data stream is a T1 frame with a single framing bit (F in Figure 35) followed by octet bound time-slots 1 to 24. RSCLK[n] is held quiescent during the framing bit. The RSDATA[n] data bit (B1 of TS1) clocked in by the first rising edge of RSCLK[n] after the framing bit is the most significant bit of time-slot 1. The RSDATA[n] bit (B8 of TS24) clocked in by the last rising edge of RSCLK[n] before the framing bit is the least significant bit of time-slot 24. In Figure 35, the quiescent period is shown to be a low level on RSCLK[n]. A high level, affected by extending the high phase of bit B8 of time-slot TS24, is equally acceptable. In channelized T1 mode, RSCLK[n] can only be gapped during the framing bit. It must be active continuously at 1.544 MHz during all time-slot bits. Time-slots can be ignored by setting the PROV bit in the corresponding word of the receive channel provision RAM in the RCAS block to low.

Figure 35 Channelized T1 Receive Link Timing



The timing relationship of the receive clock (RSCLK[n]) and data (RSDATA[n]) signals of a channelized E1 link is shown in Figure 36. The receive data stream is an E1 frame with a single framing byte (F1 to F8 in Figure 36) followed by octet bound time-slots 1 to 31. RSCLK[n] is held quiescent during the framing byte. The RSDATA[n] data bit (B1 of TS1) clocked in by the first rising edge of RSCLK[n] after the framing byte is the most significant bit of time-slot 1. The RSDATA[n] bit (B8 of TS31) clocked in by the last rising edge of RSCLK[n] before the framing byte is the least significant bit of time-slot 31. In Figure 36, the quiescent period is shown to be a low level on RSCLK[n]. A high level, affected by extending the high phase of bit B8 of time-slot TS31, is equally acceptable. In channelized E1 mode, RSCLK[n] can only be gapped during the framing byte. It must be active continuously at 2.048 MHz during all time-slot bits. Timeslots can be ignored by setting the PROV bit in the corresponding word of the receive channel provision RAM in the RCAS block to low.

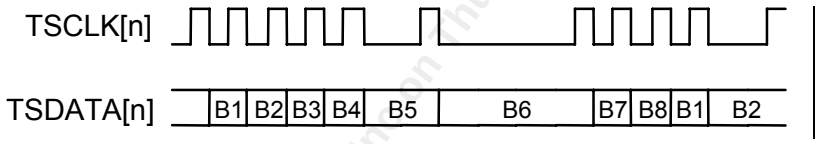
Figure 36 Channelized E1 Receive Link Timing



13.2 Transmit Link Output Timing

The timing relationship of the transmit clock (TSCLK[n]) and data (TSDATA[n]) signals of an unchannelized link is shown in Figure 37. The transmit data is viewed as a contiguous serial stream. There is no concept of time-slots in an unchannelized link. Each eight bits is grouped together into a byte with arbitrary byte alignment. Octet data is transmitted from most significant bit (B1 in Figure 37) and ending with the least significant bit (B8 in Figure 37). Bits are updated on the falling edge of TSCLK[n]. A transmit link may be stalled by holding the corresponding TSCLK[n] quiescent. In Figure 37, bits B5 and B2 are shown to be stalled for one cycle while bit B6 is shown to be stalled for three cycles. In Figure 37, the quiescent period is shown to be a low level on TSCLK[n]. A high level, affected by extending the high phase of the previous valid bit, is also acceptable. Gapping of TSCLK[n] can occur arbitrarily without regard to either byte or frame boundaries.

Figure 37 Unchannelized Transmit Link Timing



The timing relationship of the transmit clock (TSCLK[n]) and data (TSDATA[n]) signals of a channelized T1 link is shown in Figure 38. The transmit data stream is a T1 frame with a single framing bit (F in Figure 38) followed by octet bound time-slots 1 to 24. TSCLK[n] is held quiescent during the framing bit. The most significant bit of each time-slot is transmitted first (B1 in Figure 38). The least significant bit of each time-slot is transmitted last (B8 in Figure 38). The TSDATA[n] bit (B8 of TS24) before the framing bit is the least significant bit of time-slot 24. In Figure 38, the quiescent period is shown to be a low level on TSCLK[n]. A high level, affected by extending the high phase of bit B8 of time-slot TS24, is equally acceptable. In channelized T1 mode, TSCLK[n] can only be gapped during the framing bit. It must be active continuously at 1.544 MHz during all time-slot bits. Time-slots that are not provisioned to belong to any channel (the PROV bit in the corresponding word of the transmit channel provision RAM in the TCAS block set low) transmit the contents of the Idle Fill Time-slot Data register.

Figure 38 Channelized T1 Transmit Link Timing w/ Clock gapped Low

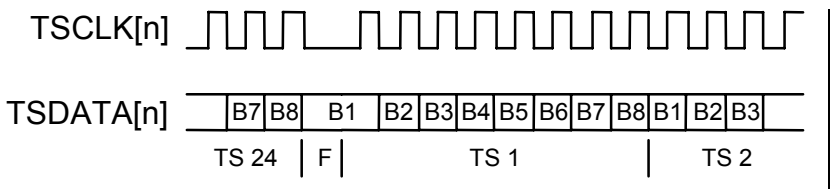
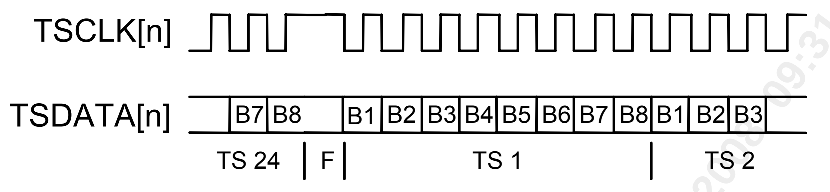


Figure 39 Channelized T1 Transmit Link Timing w/ Clock gapped high



The timing relationship of the transmit clock (TSCLK[n]) and data (TSDATA[n]) signals of a channelized E1 link is shown in Figure 40. The transmit data stream is an E1 frame with a single framing byte (FAS/NFAS in Figure 40) followed by octet bound time-slots 1 to 31. TSCLK[n] is held quiescent during the framing byte. The most significant bit of each time-slot is transmitted first (B1 in Figure 40). The least significant bit of each time-slot is transmitted last (B8 in Figure 40). The TSDATA[n] bit (B8 of TS31) before the framing byte is the least significant bit of time-slot 31. In Figure 40, the quiescent period is shown to be a low level on TSCLK[n]. A high level, affected by extending the high phase of bit B8 of time-slot 31, is equally acceptable. In channelized E1 mode, TSCLK[n] can only be gapped during the framing byte. It must be active continuously at 2.048 MHz during all time-slot bits. Time-slots that are not provisioned to belong to any channel − i.e., the PROV bit in the corresponding word of the transmit channel provision RAM in the TCAS block is set low − transmit the contents of the Idle Time-slot Fill Data register.

Figure 40 Channelized E1 Transmit Link Timing w/ Clock gapped Low

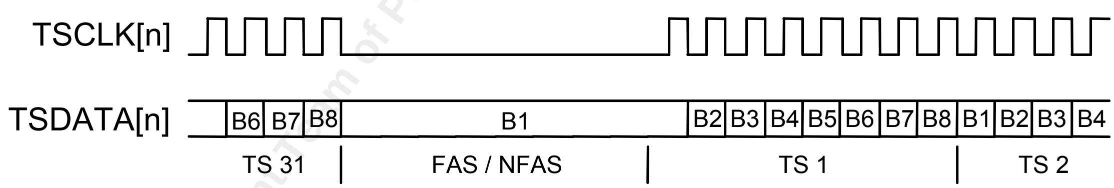
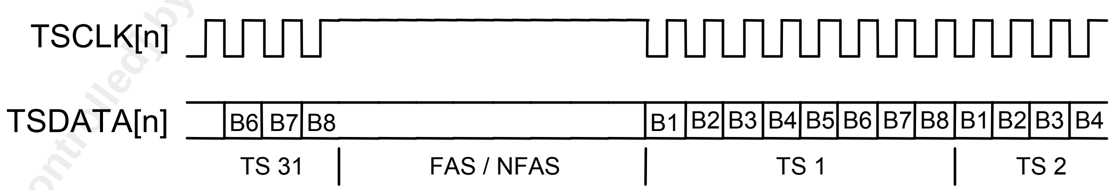


Figure 41 Channelized E1 Transmit Link Timing w/ Clock gapped High



Alternatively, the CTSCLK can be used instead of the TSCLK[n] to lock the clocks of all the links together

13.3 Any-PHY/UTOPIA L2 Interfaces

While the following diagrams present representative waveforms, they are not an attempt to unambiguously describe the interfaces. The Pin Description section is intended to present the detailed pin behavior and constraints on use.

The following parameters apply to all Any-PHY/UTOPIA interface figures:

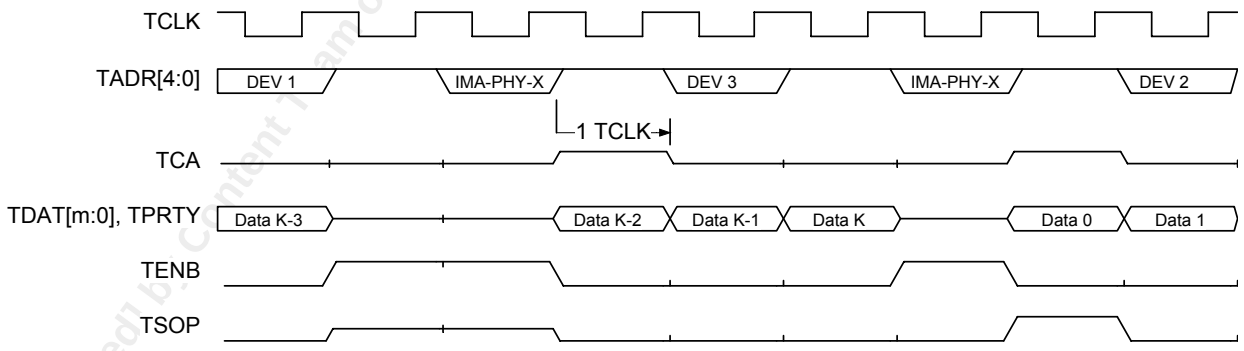
- m = 7 for 8-bit mode, 15 for 16-bit mode
- k = is a function of 8/16 bit mode and number of prepends selected.

13.3.1 UTOPIA L2 Transmit Slave Interface

Figure 42 gives an example of the functional timing of the transmit interface when configured as a 31-port UTOPIA L2 compliant transmit slave. The interface responds to the enabled addresses as defined by the register Transmit Cell Available Enable by asserting the TCA corresponding to the addressed PHY when it can accept a complete cell. As a result, the master selects one of the S/UNI IMA 4 device's PHY's by presenting the PHY address again during the last cycle TENB is high. If the device had not been selected, TSOC, TDAT[m:0], and TPRTY would have remained high-impedance.

Figure 42 shows that a cell transfer may be paused by deasserting TENB. The device is reselected by presenting the PHY's address the last cycle TENB is high to resume the transfer.

Figure 42 UTOPIA L2 Transmit Slave

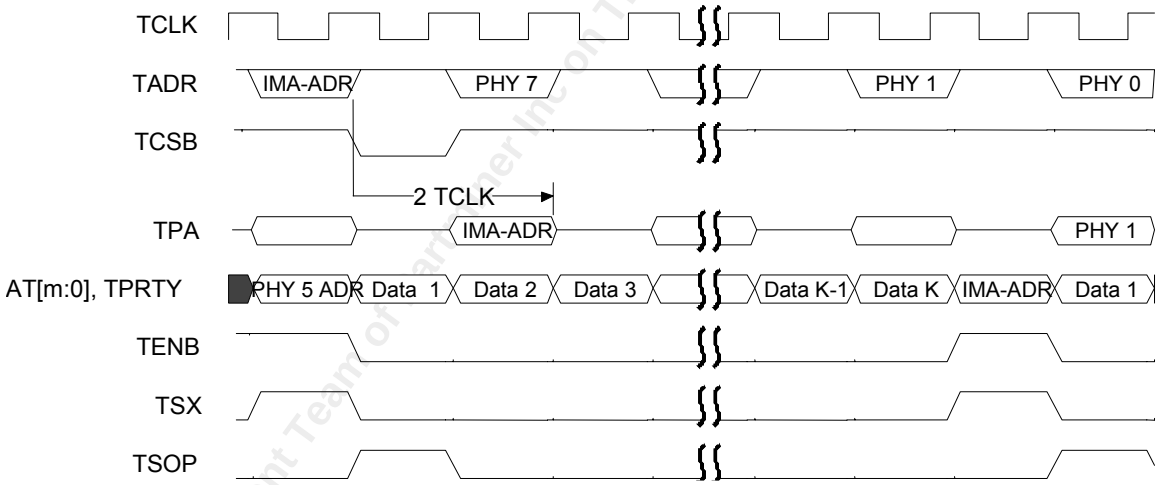


13.3.2 Any-PHY Transmit Slave Interface

Figure 43 shows an example of the functional timing of the transmit interface when configured as a 4-port Any-PHY compliant transmit slave. The Any-PHY master polls the ports in the S/UNI IMA 4 device and the S/UNI IMA 4 device responds by driving TPA. If the S/UNI IMA's polled port can accept a complete cell, TPA is driven active otherwise the TPA is driven inactive. Positive responses are recorded by the master and eventually results in a data transfer. Ports are selected for data transfers via an in-band address prepend in first word of the data transfer. Polling continues independent of the data transfer state.

Data transfers are initiated with the assertion of TENB and TSX; they complete without pausing.

Figure 43 Any-PHY Transmit Slave

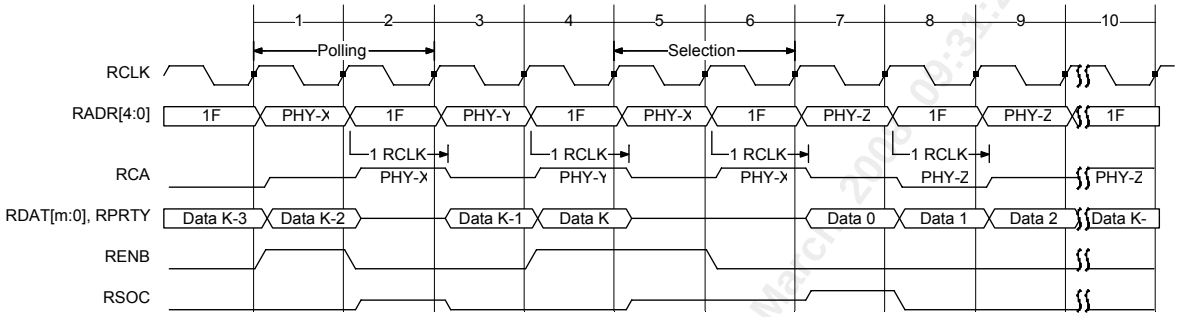


13.3.3 UTOPIA L2 Multi-PHY Receive Slave Interface

Figure 44 shows and example of the functional timing of the receive interface when configured as a 31-port UTOPIA L2 compliant receive slave. The interface responds to addresses (as specified by the register Receive Cell Available Enable) by asserting the RCA corresponding to the addressed PHY when it can provide a complete cell. As a result, the master selects one of the S/UNI IMA 4 device's PHY's by presenting the PHY address again during the last cycle RENB is high. Had not the device been selected, RSOC, RDAT[m:0], and RPRTY would have remained high-impedance.

Figure 44 shows that a cell transfer may be paused by deasserting RENB. The device is reselected by presenting the PHY's address the last cycle RENB is high to resume the transfer.

Figure 44 UTOPIA L2 Multi-PHY Receive Slave

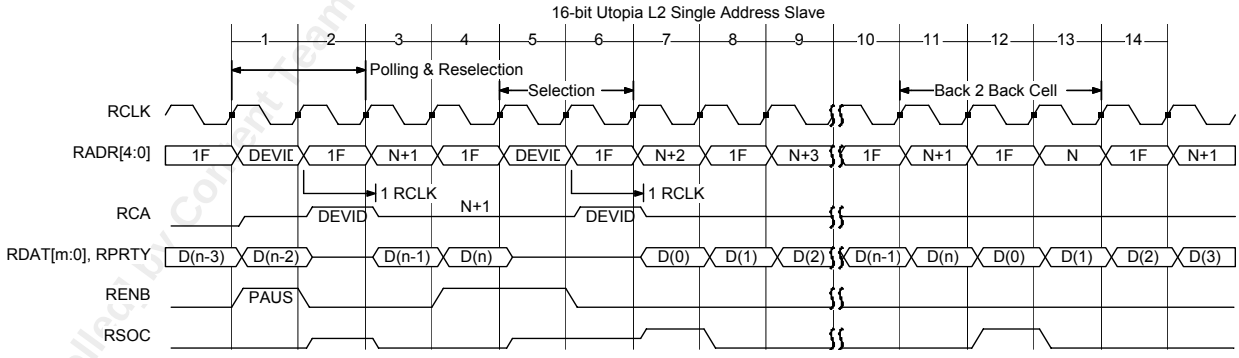


13.3.4 UTOPIA L2 single-PHY Receive Slave Interface

Figure 45 shows an example of the functional timing of the receive interface when configured as a single port UTOPIA L2 compliant slave. The interface responds to the address that matches the DEVID specified in the RXAPS Configuration register by asserting the RCA when it can provide a complete cell. As a result, the master selects the S/UNI IMA 4 device's PHYs by presenting the PHY address again during the last cycle RENB is high. If the device is not selected, RSOC, RDAT[m:0], and RPRTY remain high-impedance.

Figure 45 shows that a cell transfer may be paused by deasserting RENB. The device is reselected by presenting the PHY's address the last cycle RENB is high to resume the transfer.

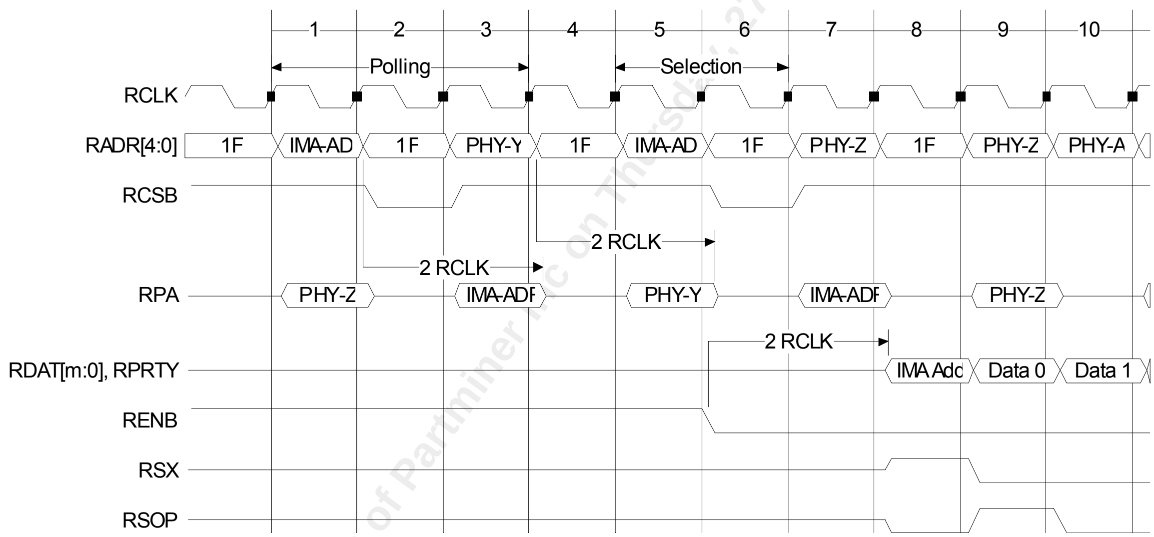
Figure 45 UTOPIA L2 Single-PHY Receive Slave



13.3.5 Any-PHY Receive Slave Interface

Figure 46 shows an example of the functional timing of the receive interface when configured as an Any-PHY compliant receive slave. The interface responds to the polling of address “IMA” (which matches the address defined by the Receive Any-PHY/UTOPIA Config register) by asserting RPA when it can deliver a complete cell. The Any-PHY master repolls addresses until it receives an asserted RPA. As a result, the master re-selects the same RADR again during the last cycle RENB is high to initiate a transfer. Once transfer is initiated, RENB must remain asserted until the last data is received.

Figure 46 Any-PHY Receive Slave



13.4 SDRAM Interface

The following three diagrams show the timing for signals destined for the pins of the SDRAM during the Activate-Read (with Auto-precharge), Activate-Write (with Auto-precharge), and Auto-refresh command sequences and Power-Up and Initialization Sequence. The cbcmd signal is not a signal; it merely represents the memory access command formed by the combination of the individual SDRAM control signals (e.g., cbcsb and cbrasb). Also note that reads/writes of cell buffers are done in bursts of eight words, with 4 bursts per cells; the first and third bursts involve the even banks and the second and fourth bursts involve the odd banks in the SDRAM.

Figure 47 SDRAM Read Timing

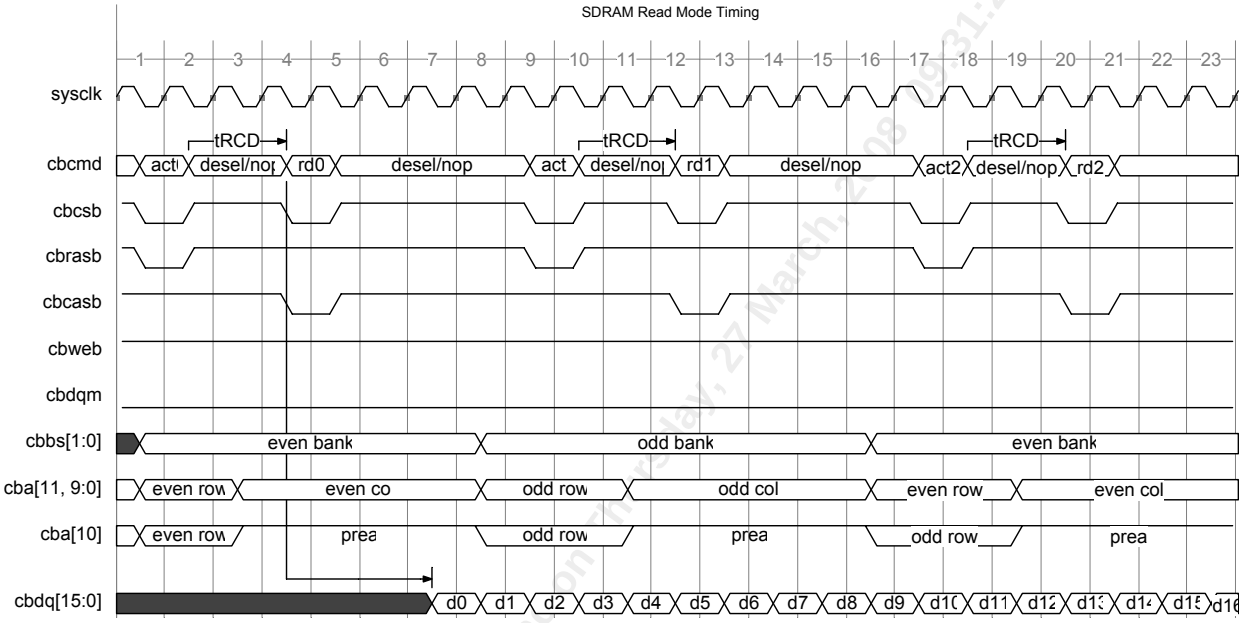


Figure 48 SDRAM Write Timing

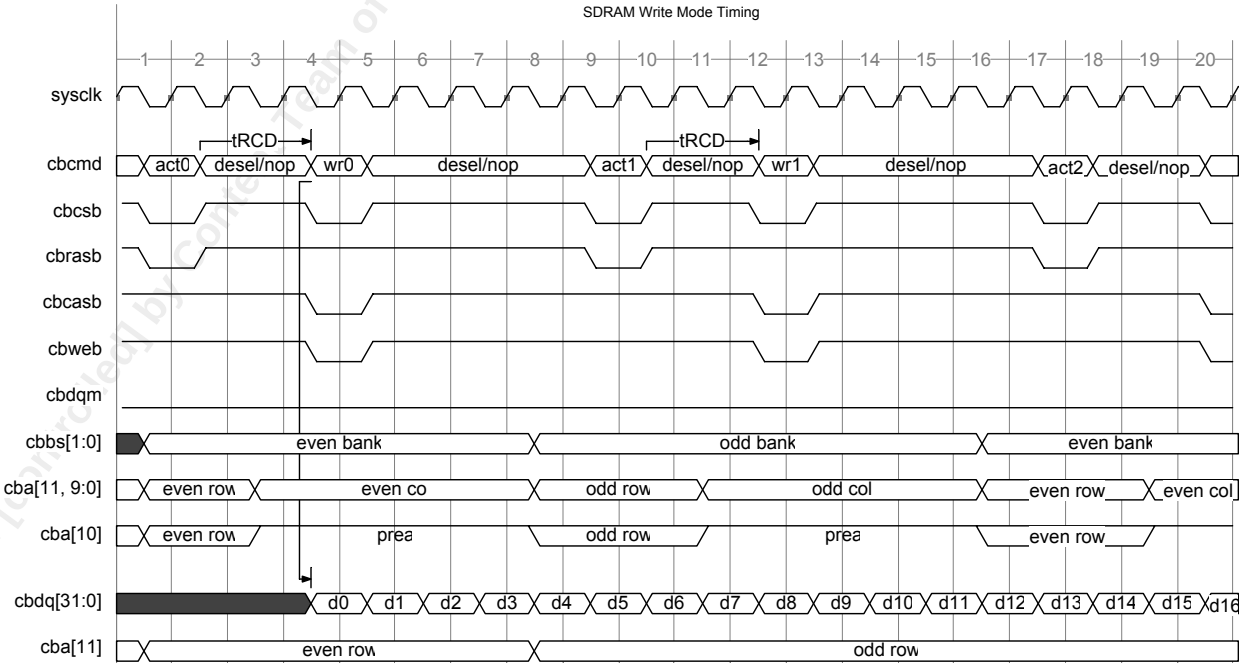


Figure 49 SDRAM Refresh

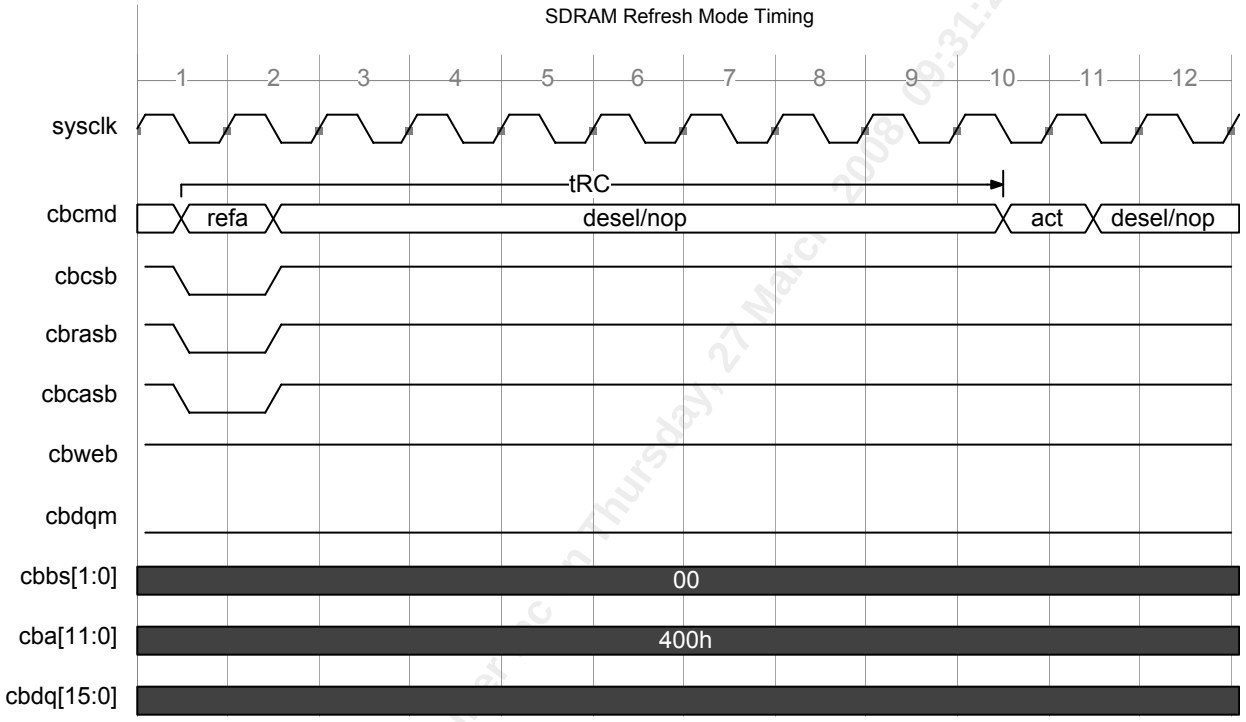
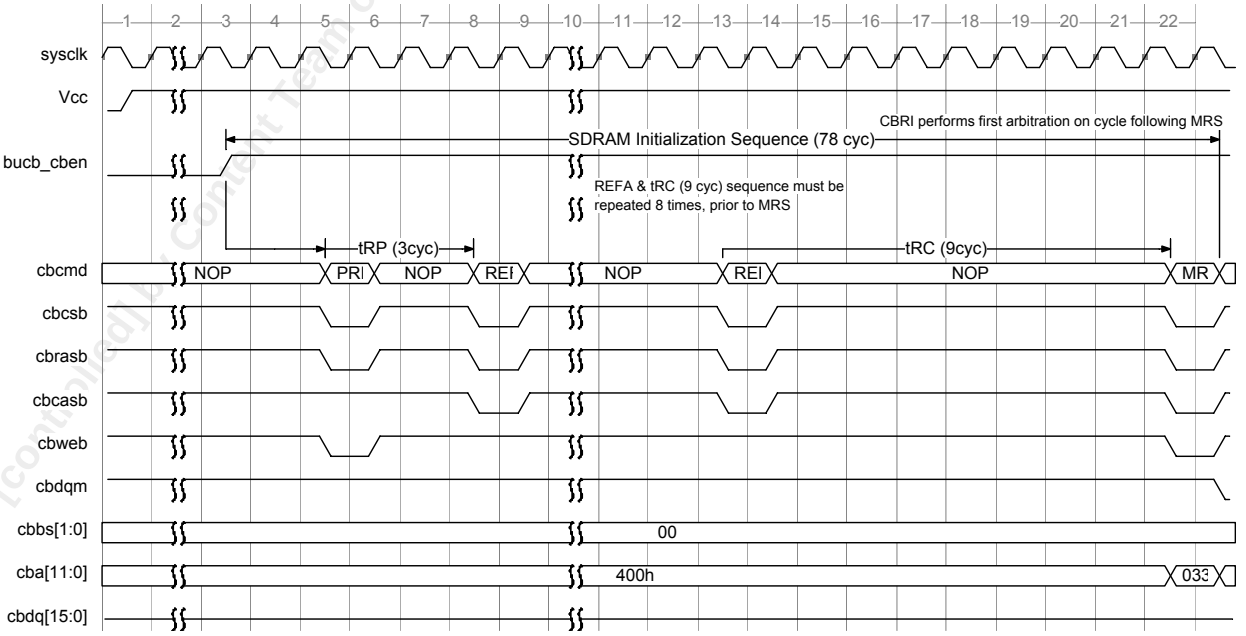


Figure 50 Powerup and Initialization Sequence



14 Absolute Maximum Ratings

Maximum ratings are the worst-case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 40 Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
1.8V Supply Voltage	-0.3V to +3.6V
3.3V Supply Voltage	-0.3V to +6.0V
Voltage on Any Pin(except 5V compatible)	-0.3V to V_{VDDO}+0.3V
Voltage on Any Pin(5V compatible)	-0.3V to 5.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

15 D. C. Characteristics

T_A = -40°C to +85°C, V_{DD} = $VDD_{typical}$ ± 8%
(Typical Conditions: T_A = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V, V_{AVDDQ} = 3.3V)

Table 41 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDI}	Power Supply	1.656	1.8	1.944	Volts	
V_{VDDO}	Power Supply	3.03	3.3	3.56	Volts	
V_{VDDQ}	Power Supply	3.03	3.3	3.56	Volts	
V_{IL}	Input Low Voltage			0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage			0.4	Volts	Guaranteed output Low voltage at VDD=3.03V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4			Volts	Guaranteed output High voltage at VDD=3.03V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		0.4		Volts	Applies to RSTB and TRSTB only.
I_{ILPU}	Input Low Current	10		200	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 2 and 3.
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz
I_{DDOP}	Operating Current (device core)			190	mA	V_{DD} = 1.944 v
I_{DDOP}	Operating Current (device I/O, with clock/data mode, 2.048MHz links)		90		mA	V_{DD} = 3.3 v Outputs typically loaded

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DDOP}	Operating Current (device I/O, with clock/data mode, 8MHz links)		95		mA	V_{DD} = 3.3 v Outputs typically loaded

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

16 A.C. Timing Characteristics

(T_A = -40°C to +85°C, VDD = 3.3 V ± 8%)

Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is measured from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified between a clock and an input, the hold time is measured from the 50% point of the clock to the 50% point of the input.

Notes on Output Timing:

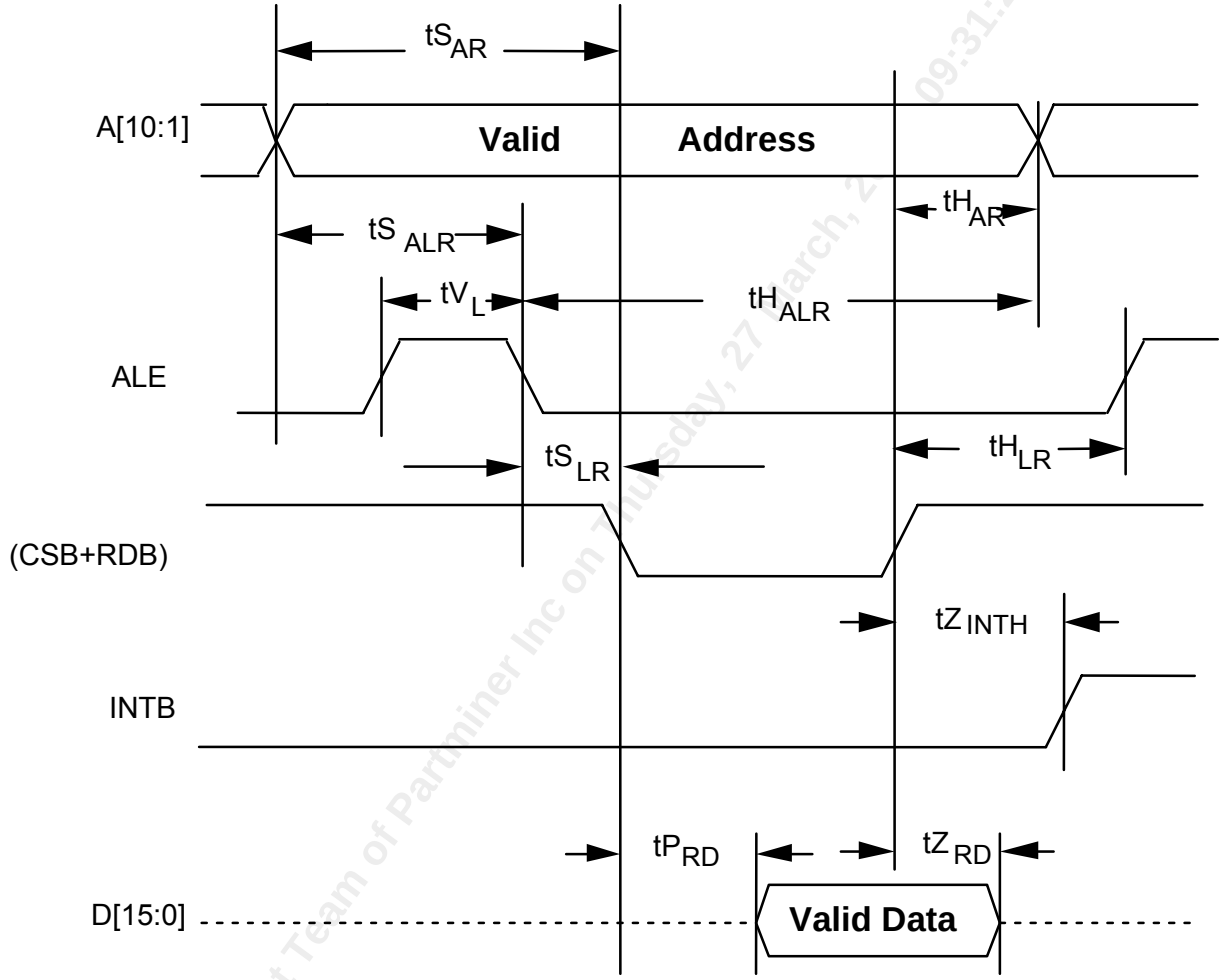
1. Output timing is measured between the 50% point of the clock to the 50% point of the output.

16.1 Microprocessor Interface Timing Characteristics

Table 42 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	5		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	5		ns
tH_{ALR}	Address to Latch Hold Time	5		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		30	ns
tZ_{RD}	Valid Read Negated to Output Tristate		20	ns
tZ_{INTH}	Valid Read Negated to Output Tristate		50	ns

Figure 51 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

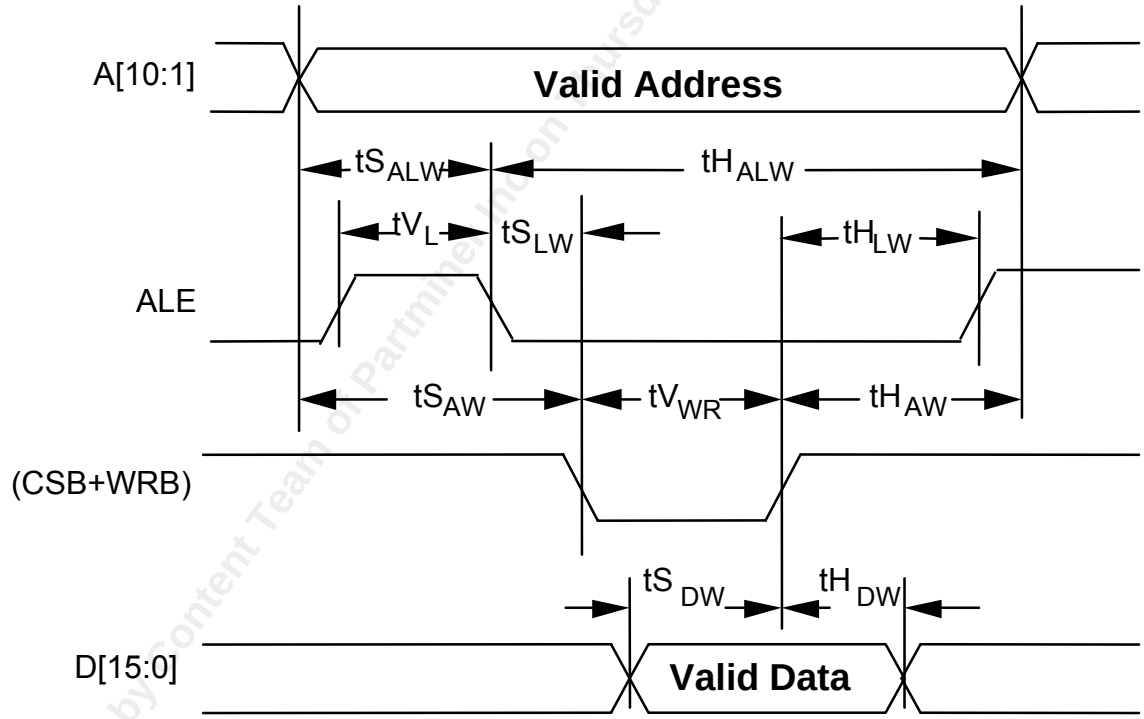
1. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus (D[15:0]).
2. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
3. In non-multiplexed address/data bus architectures, ALE should be held high so that parameters tSALR, tHALR, tVL, and tSLR are not applicable.
4. Parameter tHAR is not applicable if address latching is used.

Table 43 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	5		ns

Symbol	Parameter	Min	Max	Units
tS_{DW}	Data to Valid Write Set-up Time	10		ns
tS_{ALW}	Address to Latch Set-up Time	5		ns
tH_{ALW}	Address to Latch Hold Time	5		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	20		ns

Figure 52 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so that parameters tS_{ALW}, tS_{ALW}, tV_{L}, tS_{LW} and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.

Table 44 RTSB Timing

Symbol	Description	Min	Max	Units
tVRSTB	RSTB Pulse Width	100		ns

Figure 53 RSTB Timing

16.2 Synchronous I/O Timing

Figure 54 Synchronous I/O Timing

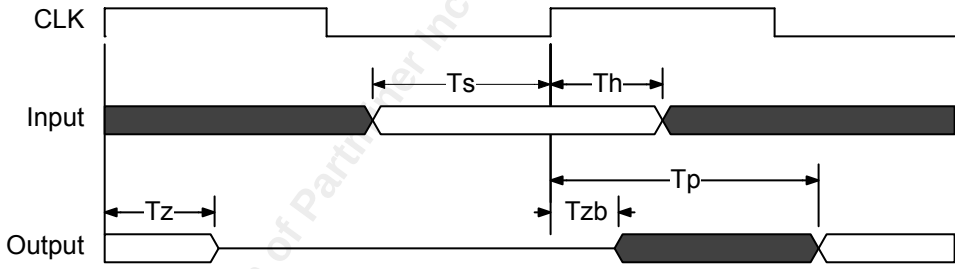


Table 45 SYSCLK and REFCLK Timing

Symbol	Description	Min	Max	Units
f_{SYSCLK}	Frequency, SYSCLK	20	55	MHz
D_{SYSCLK}	Duty Cycle, SYSCLK	40	60	%
f_{REFCLK}	Frequency, REFCLK		52	MHz
D_{SYSCLK}	Duty Cycle, REFCLK	40	60	%

Table 46 Cell Buffer SDRAM Interface

Symbol	Description	Min	Max	Units
Ts	Input Set-up time to SYSCLK	2.5		ns
Th	Input Hold time to SYSCLK	0.3		ns
Tp	SYSCLK High to Output Valid	1	10.5	ns

Symbol	Description	Min	Max	Units
Tz	SYSCLK High to Output High-Impedance	1	10	ns
Tzb	SYSCLK High to Output Driven	1		ns

Notes:

1. Maximum output propagation delays are measured with a 20pF load on the outputs.
2. Minimum output propagation delays are measured with a 0 pF load on the outputs.

Table 47 Any-PHY/UTOPIA Transmit Interface

Symbol	Description	Min	Max	Units
f_{CLK}	TCLK Frequency		52	MHz
D_{CLK}	TCLK Duty Cycle	40	60	%
Ts	Input Set-up time to TCLK (except TCSB)	4		ns
Ts	Input Set-up time to TCLK (TCSB only)	6		ns
Th	Input Hold time to TCLK	1		ns
Tp	TCLK High to Output Valid	1	12	ns
Tz	TCLK High to Output High-Impedance	1	12	ns
Tzb	TCLK High to Output Driven	1		ns

Notes:

1. Maximum output propagation delays are measured with a 50pF load on the outputs.
2. Minimum output propagation delays are measured with a 0 pF load on the outputs.

Table 48 Any-PHY/UTOPIA Receive Interface

Symbol	Description	Min	Max	Units
f_{CLK}	RCLK Frequency		52	MHz
D_{CLK}	RCLK Duty Cycle	40	60	%
Ts	Input Set-up time to RCLK (except RCSB)	4		ns
Ts	Input Set-up time to RCLK (RCSB)	6		ns
Th	Input Hold time to RCLK	1		ns
Tp	RCLK High to Output Valid	1	12	ns
Tz	RCLK High to Output High-Impedance	1	12	ns
Tzb	RCLK High to Output Driven	0		ns

Notes:

1. Maximum output propagation delays are measured with a 50pF load on the outputs.
2. Minimum output propagation delays are measured with a 0 pF load on the outputs.

Table 49 Serial Link Input

Symbol	Description	Min	Max	Units
	RSCLK[3:0] Frequency (See Note 1)	1.542	1.546	MHz
	RSCLK[3:0] Frequency (See Note 2)	2.046	2.05	MHz
	RSCLK[3:0] Frequency (See Note 3)		8	MHz
	RSCLK[3:0] Duty Cycle	40	60	%
tS_{RD}	RSCLK[3:0] Set-Up Time	5		ns
tH_{RD}	RSCLK[3:0] Hold Time	5		ns

Notes:

1. Applicable only to channelized T1 links and measured between framing bits.
2. Applicable only to channelized E1 links and measured between framing bytes.
3. Applicable only to unchannelized links of any format and measured between any two RCLK rising edges

Table 50 Serial Link Output

Symbol	Description	Min	Max	Units
	TSCLK[3:0] Frequency (See Note 3)	1.542	1.546	MHz
	TSCLK[3:0] Frequency (See Note 4)	2.046	2.05	MHz
	TSCLK[3:0] Frequency (See Note 5)		8	MHz
	TSCLK[3:0] Duty Cycle	40	60	%
t_{PTD}	TSCLK[3:0] Low to TSDATA[3:0]Valid (See Note 1 and Note 2)	2	27	ns

Notes on Output Timing:

1. Maximum output propagation delays are measured with a 50 pF
2. Minimum output propagation delays are measured with a 0 pF
3. Applicable only to channelized T1 links and measured between framing bits.
4. Applicable only to channelized E1 links and measured between framing bytes.
5. Applicable only to unchannelized links of any format and measured between any two TCLK rising edges

16.3 JTAG Timing

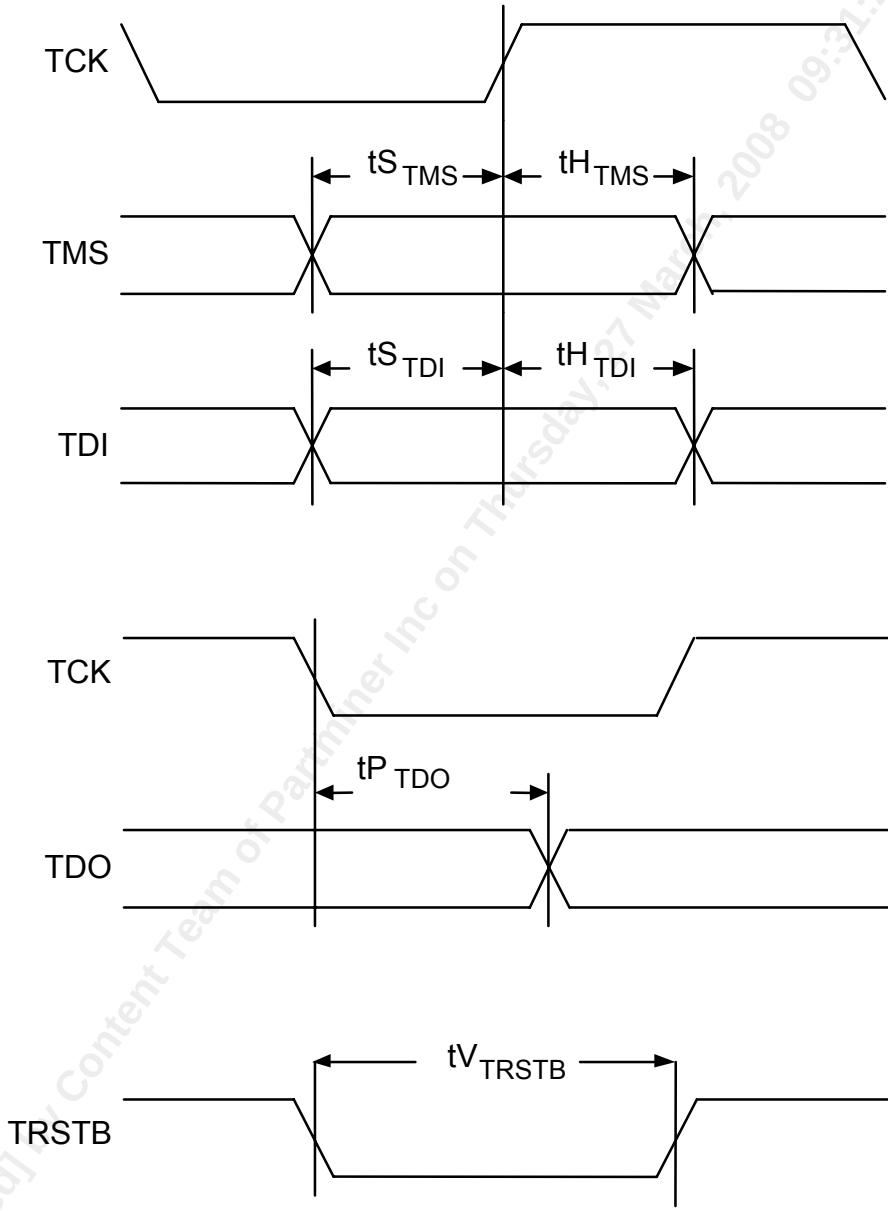
Table 51 JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

Notes:

1. Maximum output propagation delays are measured with a 100 pF load
2. Minimum output propagation delays are measured with a 0 pF

Figure 55 JTAG Port Interface Timing



17 Ordering and Thermal Information

Table 52 Ordering and Thermal Information

Part No.	Description
PM7348-PI	324-Pin Plastic Ball Grid Array (PBGA)
PM7348-PGI	324-Pin PBGA, 23mm x 23mm; 1.0mm BP (RoHS-Compliant)

This product is designed to operate over a wide temperature range in industrial applications such as Outside Plant Equipment. For the thermal characteristics below, a power of 0.684 watts was used (as derived from section 15).

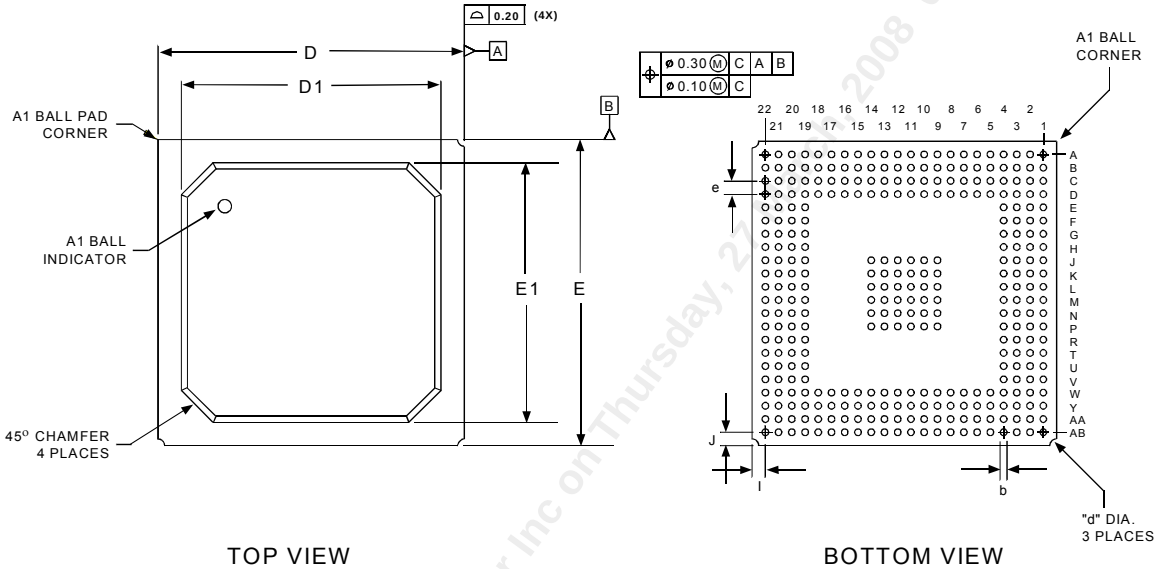
Maximum long-term operating junction temperature (TJ) to ensure adequate long-term life.	88°C
Maximum junction temperature (TJ) for short-term excursions with guaranteed continued functional performance.	125°C
Minimum ambient temperature (TA)	-40°C

Table 53 Thermal information – Theta Ja vs. Airflow

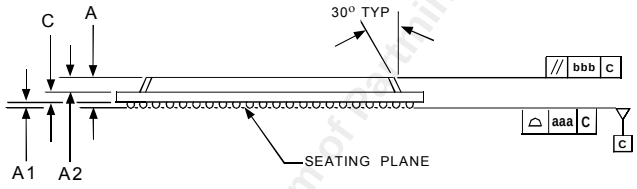
		Forced Air (Linear Feet per Minute)				
Theta JA @ specified power	Conv	100	200	300	400	500
Dense Board	41.3	36.9	33.9	31.8	30.5	29.5
JEDEC Board	22.9	21.2	20.0	19.2	18.6	18.2

18 Mechanical Information

324 PIN PBGA –23x23 MM BODY - (P SUFFIX)



TOP VIEW BOTTOM VIEW



SIDE VIEW

NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES COPLANARITY.
3) DIMENSION bbb DENOTES PARALLEL.

PACKAGE TYPE : 324 PLASTIC BALL GRID ARRAY - PBGA																	
BODY SIZE : 23 x 23 x 2.28 MM (4 layer)																	
Dim.	A (2 layer)	A (4 layer)	A1	A2	D	D1	C (2 layer)	C (4 layer)	E	E1	l	J	b	d	e	aaa	bbb
Min	1.82	2.07	0.40	1.12	-	19.00	0.30	0.55	-	19.00	-	-	0.50	-	-	-	-
Nom.	2.03	2.28	0.50	1.17	23.00	19.50	0.36	0.61	23.00	19.50	1.00	1.00	0.63	1.00	1.00	-	-
Max.	2.22	2.49	0.60	1.22	-	20.20	0.40	0.67	-	20.20	-	-	0.70	-	-	0.15	0.35

Notes:

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Microchip:
PM7348-PGI