The documentation and process conversion measures necessary to comply with this revision shall be completed by 23 March 2007.

INCH-POUND
MIL-PRF-19500/474F
23 January 2007
SUPERSEDING
MIL-PRF-19500/474E
3 November 1997

* PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, SILICON, MULTIPLE DIODE ARRAYS, TYPES 1N5768, 1N5770, 1N5772, 1N5774, 1N6100, 1N6101, 1N6496, 1N6506, 1N6507, 1N6508, 1N6509, 1N6510, AND 1N6511, JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon, multiple diode arrays. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figures 1, 2, 3, 4, 5, 6, 7, and 8.

* 1.3 Maximum ratings. Unless otherwise specified T_A = +25°C.

Type	$V_{BR(R)}$ 1/ 2/	I_O 1/ 3/ T_A = +25°C	I_{FSM} 1/ t_p = 1/120 s	P_T T_A = +25°C	T_J	T_{STG}
	V dc	mA dc	mA dc	mW	°C	°C
1N5768	60	300	500	500 4/	-65 to +175	-65 to +200
1N5770	60	300	500	500 4/		
1N5772	60	300	500	500 4/		
1N5774	60	300	500	500 4/		
1N6496	60	300	500	500 4/		
1N6506	60	300	500	600 5/		
1N6507	60	300	500	600 5/		
1N6508	60	300	500	600 5/		
1N6509	60	300	500	600 5/		
1N6100	75	300	500	500 4/		
1N6101	75	300	500	600 5/		
1N6510	75	300	500	500 4/		
1N6511	75	300	500	600 5/		

1/ Each diode.
2/ Pulsed: PW = 100 ms maximum; duty cycle ≤ 20 percent.
3/ Derate at 2.0 mA/°C above +25°C.
4/ Derate at 3.33 mW/°C above +25°C.
5/ Derate at 4.0 mW/°C above +25°C.

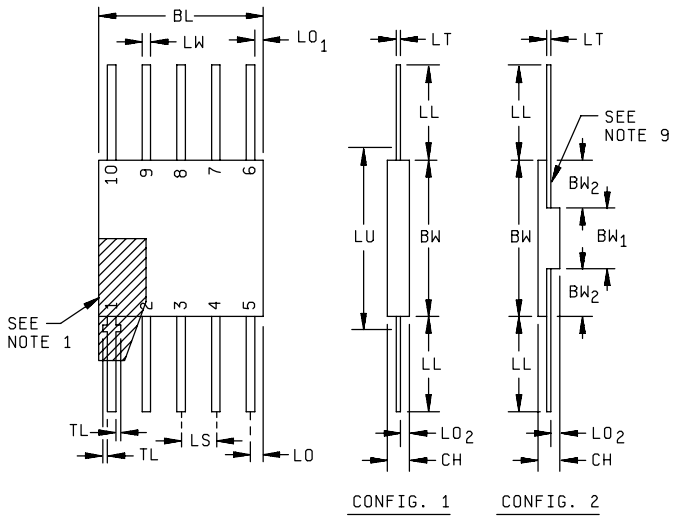
Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

1.4 Primary electrical characteristics, each diode.

Type	V_{F1} (1) I_F = 100 mA dc		V_{F2} 1/ I_F = 500 mA dc		I_{R1} V_R = 40 V dc		C_t		t_{fr} I_F = 500 mA dc		t_{rr} $I_F = I_R$ = 200 mA dc R_L = 100 Ω I_{rr} = 20 mA dc	
	V dc		V dc		μA dc		pF		ns		ns	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
1N5768		1.0		1.5		0.1		4		40		20
1N5770		1.0		1.5		0.1		8		40		20
1N5772		1.0		1.5		0.1		8		40		20
1N5774		1.0		1.5		0.1		8		40		20
1N6496		1.0		1.5		0.1		8		40		20
1N6506		1.0		1.5		0.1		4		40		20
1N6507		1.0		1.5		0.1		8		40		20
1N6508		1.0		1.5		0.1		8		40		20
1N6509		1.0		1.5		0.1		8		40		20

Type	V_{F1} I_F = 100 mA dc		I_{R2} V_R = 20 V dc		C_t		t_{fr} I_F = 100 mA dc		t_{rr} $I_F = I_R$ = 10 mA dc R_L = 100 Ω I_{rr} = 1 mA dc	
	V dc		nA dc		pF		ns		ns	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
1N6100		1.0		25		4		15		5
1N6101		1.0		25		4		15		5
1N6510		1.0		25		4		15		5
1N6511		1.0		25		4		15		5

(1) Pulsed: PW = 300 μs ± 50 μs, duty cycle ≤ 2 percent, 90 μs after leading edge of pulse.

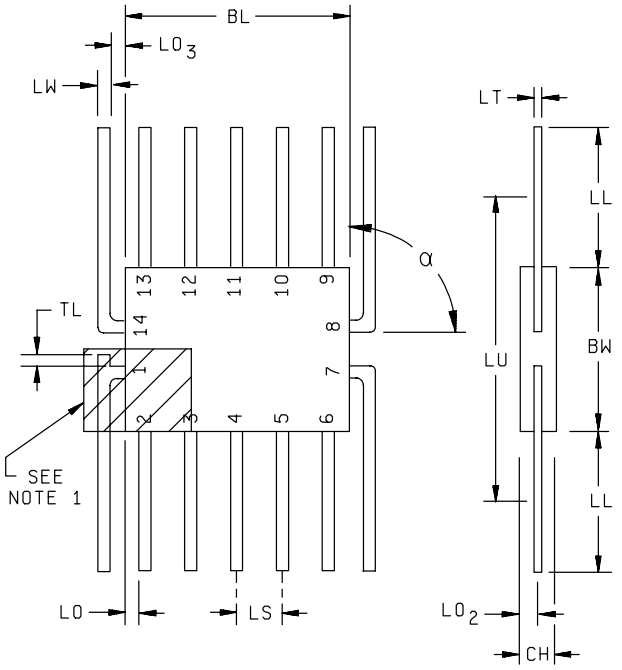


Symbol	Inches		Millimeters		Notes	Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max			Min	Max	Min	Max	
BL		.290		7.37	3	LO_1	.005		0.13		7, 8
BW	.235	.260	5.97	6.60		LO_2	.005	.050	0.13	1.27	2
BW_1	.125		3.18			LS	.050 BSC		1.27 BSC		4, 6
BW_2	.030		0.76			LT	.003	.006	0.08	0.15	5
CH	.030	.095	0.76	2.41		LU		.280		7.11	3
LL	.240	.370	6.10	9.40		LW	.010	.019	0.25	0.48	5
LO		.045		1.14	7	TL	.008	.015	0.20	0.38	1

NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark. Alternatively, a tab (dimension TL) may be used to identify pin 1. This tab may be located on either side as shown. If a pin 1 identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply.
2. Dimension LO_2 shall be measured at the point of exit of the lead from the body. Dimension LO_2 shall be .0085 inch (0.216 mm) minimum when lead finish A is solder.
3. These dimensions allow for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 10.
5. All leads: Dimensions are pre-solder dip.
6. Eight spaces.
7. Applies to all four corners (lead numbers 1, 5, 6, and 10).
8. Dimension LO may be .000 inch (0.00 mm) if lead numbers 1, 5, 6, and 10 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body. For all bottom-brazed or side-brazed configurations, dimension LO shall be measured from the edge of the furthest extension of the metal pad or lead.
9. Optional configuration. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Dimensions are in inches. Millimeters are given for general information only.

* FIGURE 1. Physical dimensions for types 1N5768, 1N5770, and 1N5772.

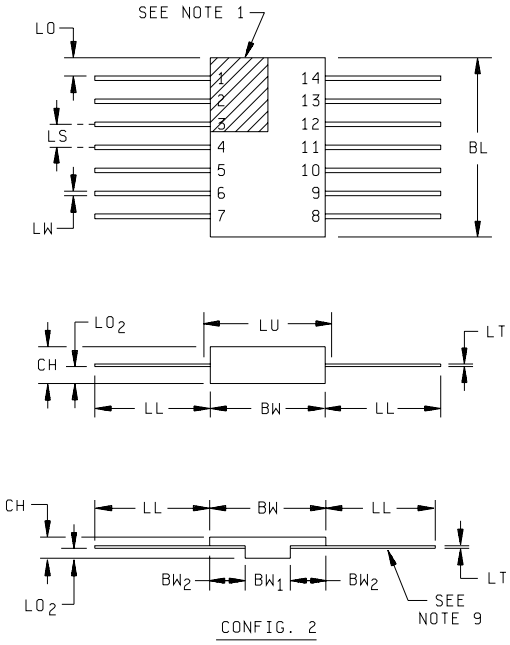


Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BL		.280		7.11	4
BW	.235	.260	5.97	6.60	
CH	.030	.095	0.76	2.41	
LL	.250	.370	6.35	9.40	
LO_2	.010	.040	0.25	1.02	3
LO	.005		0.13		8
LO_3	.004		0.10		9
LS	.050 BSC		1.27 BSC		6
LT	.003	.006	0.08	0.15	5
LU		.280		7.11	4
LW	.010	.019	0.25	0.48	5
TL	.008	.015	0.20	0.38	1

NOTES:
This package is inactive and shall be replaced with the package on figure 3.

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark. Alternatively, a tab (dimensions TL) may be used to identify pin 1. This tab may be located on either side as shown. If a pin 1 identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply.
2. Dimension LO_2 shall be measured at the point of exit of the lead from the body. Dimension LO_2 shall be .0085 inch (0.216 mm) minimum when lead finish A is applied.
3. These dimensions allow for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
5. All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish A is applied. Dimensions given are pre-solder dip.
6. Twelve places.
7. Applies to all four corners (lead numbers 2, 6, 9, and 13).
8. Dimensions LO may be .000 inch (0.00 mm) if lead numbers 2, 6, 9, and 13 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body.
9. Applies to lead numbers 1, 7, 8, and 14.
10. Lead configuration is optional within dimension BW except dimensions LT and LW apply.
11. Dimensions are in inches. Millimeters are given for general information only.

* FIGURE 2. Physical dimensions for types 1N5774 and 1N6100.

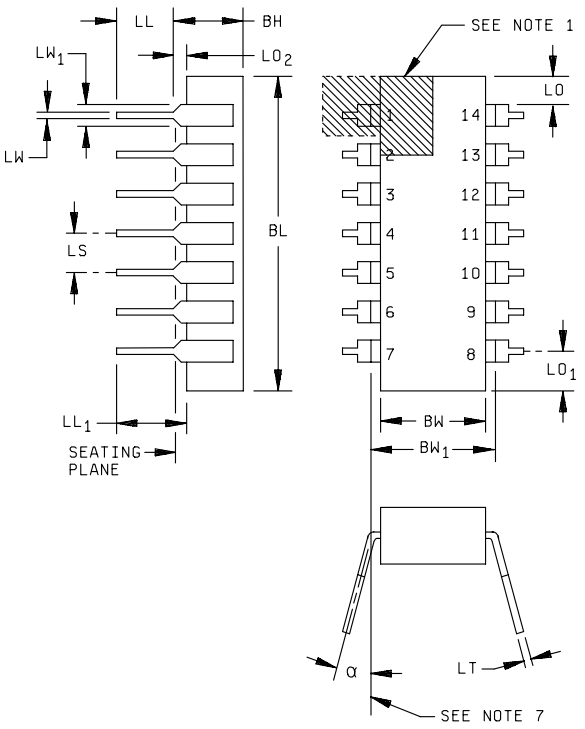


Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BL		.390		9.91	3
BW	.235	.260	5.97	6.60	
BW_1	.125		3.18		
BW_2	.030		0.76		
CH	.045	.095	1.14	2.41	
LL	.250	.370	6.35	9.40	
LO	.005		0.13		7, 8
LO_2	.026	.045	0.66	1.14	2
LS	.050 BSC		1.27 BSC		4, 6
LT	.003	.006	0.08	0.15	5
LU		.280		7.11	3
LW	.010	.019	0.25	0.48	5

NOTES

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. Dimension LO_2 shall be measured at the point of exit of the lead from the body. Dimension LO_2 minimum shall be reduced by .0015 inch (0.038 mm) maximum when lead finish is solder.
3. These dimensions allow for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
5. All leads: Dimensions are pre-solder dip.
6. Twelve spaces.
7. Applies to all four corners.
8. Dimensions LO may be .000 inch (0.00 mm) if lead numbers 1, 7, 8, and 14 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body.
9. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Lead configuration is optional within dimension BW except dimensions LW and LT apply.
11. Dimensions are in inches. Millimeters are given for general information only.

* FIGURE 3. Alternate physical dimensions for types 1N5774 and 1N6100.

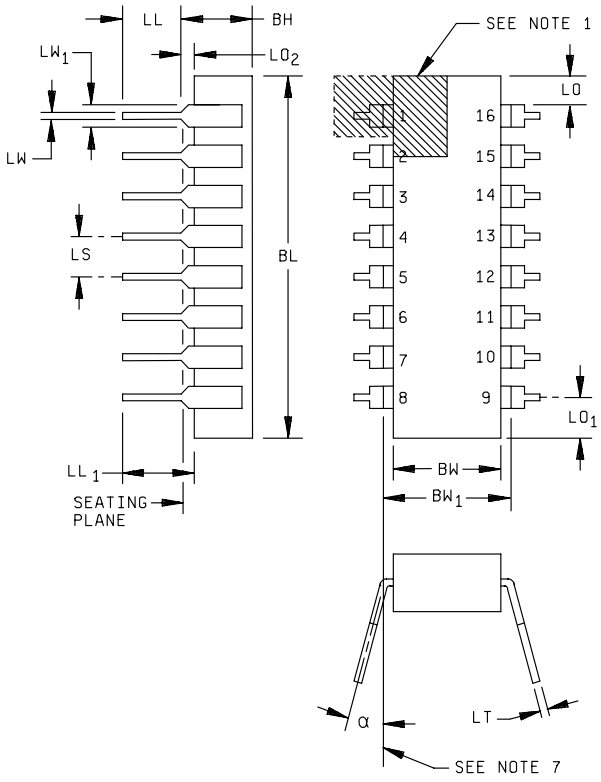


Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BH		.200		5.08	
BL		.785		19.94	4
BW	.220	.310	5.59	7.87	4
BW_1	.290	.320	7.37	8.13	7
LL	.100	.200	2.54	5.08	
LL_1	.150		3.81		
LO	.005		0.13		6
LO_1		.098		2.49	6
LO_2	.015	.060	0.38	1.52	3
LS	.100 BSC		2.54 BSC		5, 9
LT	.008	.015	0.20	0.38	8
LW	.014	.023	0.36	0.58	8
LW_1	.020	.070	0.51	1.78	2, 8
α	0°	15°	0°	15°	

NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. The minimum limit for dimension LW_1 may be .023 inch (0.58 mm) for lead numbers 1, 7, 8, and 14 only.
3. Dimension LO_2 shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 inch (0.25 mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (lead numbers 1, 7, 8, and 14).
7. Lead center when α is 0 degrees. BW_1 shall be measured at the centerline of the leads.
8. All leads: Dimensions are pre-solder dip. Pointed or round lead ends are allowed.
9. Twelve spaces.
10. Dimensions are in inches. Millimeters are given for general information only.

FIGURE 4. Physical dimensions for types 1N6506, 1N6507, 1N6508, 1N6509 and 1N6511.

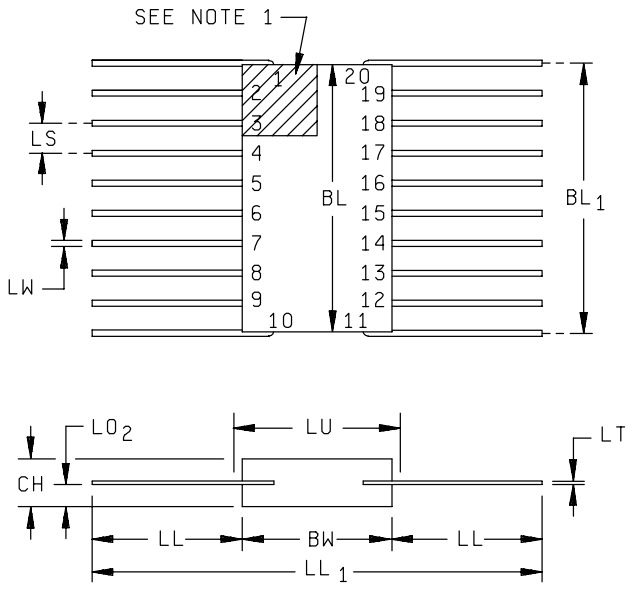


Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BH		.200		5.08	
BL		.785		19.94	4
BW	.220	.310	5.59	7.87	4
BW_1	.290	.320	7.37	8.13	7
LL	.100	.200	2.54	5.08	
LL_1	.150		3.81		
LO	.005		0.13		6
LO_1		.098		2.49	6
LO_2	.015	.060	0.38	1.52	3
LS	.100 BSC		2.54 BSC		5, 9
LT	.008	.015	0.20	0.38	8
LW	.014	.023	0.36	0.58	8
LW_1	.030	.070	0.76	1.78	2, 8
α	0°	15°	0°	15°	

NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. The minimum limit for dimension LW_1 may be .020 inch (0.51 mm) for lead numbers 1, 8, 9, and 16 only.
3. Dimension LO_2 shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 inch (0.25 mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (lead numbers 1, 8, 9, and 16).
7. Lead center when α is 0 degrees. BW_1 shall be measured at the centerline of the leads.
8. All leads: Dimensions are pre-solder dip. Pointed or round lead ends are allowed.
9. Fourteen spaces.
10. Dimensions are in inches. Millimeters are given for general information only.

FIGURE 5. Physical dimensions for type 1N6101.

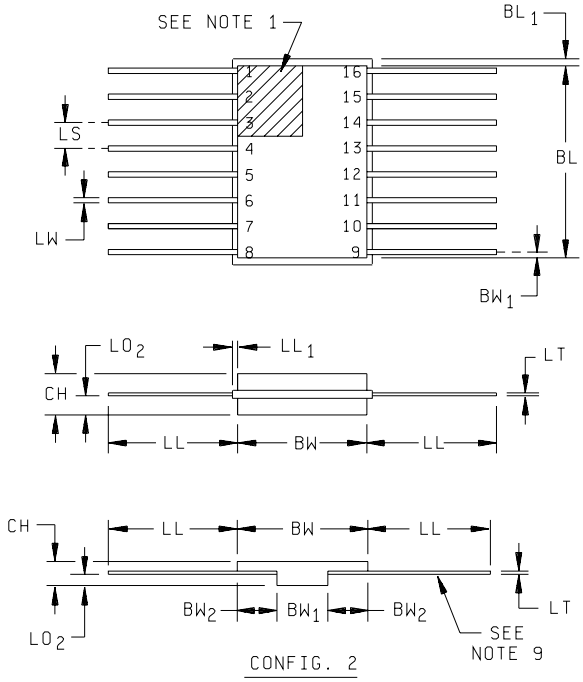


Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BL	.255	.278	6.48	7.06	
BL_1		.288		7.32	2
BW	.194	.200	4.93	5.08	
CH	.045	.095	1.14	2.41	
LL	.265	.290	6.73	7.37	
LL_1	.724	.780	18.39	19.81	
LO_2	.020	.025	0.51	0.64	4
LS	.030 TP		0.76 TP		3, 5
LT	.004	.006	0.10	0.15	6
LU		.210		5.33	2
LW	.010	.019	0.25	0.48	6

NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area limited by pin 3 and package centerline. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The true position pin spacing is located within ±.005 inch (0.13 mm) of its true longitudinal position relative to pins 1 and 20.
4. Dimension LO_2 shall be measured at the point of exit of the lead from the body.
5. Eighteen spaces.
6. All leads: Dimensions are pre-solder dip.
7. Dimensions are in inches. Millimeters are given for general information only.

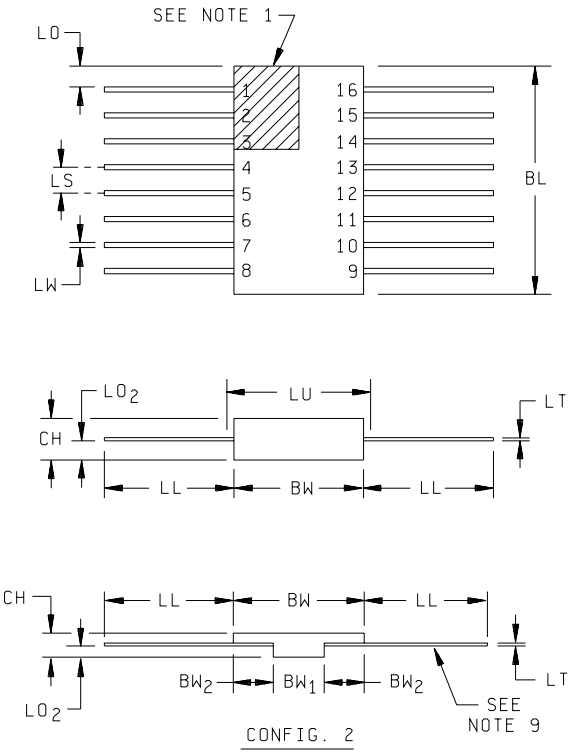
* FIGURE 6. Physical dimensions for type 1N6496.



Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BL	.370	.400	9.40	10.16	
BL_1		.020		0.51	2
BW	.245	.260	6.22	6.60	
BW_1		.015		0.38	
BW_2	0.030		0.76		
CH	.045	.095	1.14	2.41	
LL	.250	.370	6.35	9.40	
LL_1		.015		0.38	
LO_2	.025	.040	0.64	1.02	4
LS	.050 BSC		1.27 BSC		3, 5
LT	.003	.008	0.08	0.20	7
LW	.015	.019	0.38	0.48	7

NOTES:
1. This package is inactive and shall be replaced with the package on figure 8.
2. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area limited by pin 3 and package centerline. The manufacturer's identification shall not be used as a pin 1 identification mark.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The true position pin spacing is located within ±.005 inch (0.13 mm) of its true longitudinal position relative to pins 1 and 16.
5. Dimension LO_2 shall be measured at the point of exit of the lead from the body.
6. Fourteen spaces.
7. All leads: Dimensions are pre-solder dip.
8. Dimensions are in inches. Millimeters are given for general information only.
9. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

* FIGURE 7. Physical dimensions for type 1N6510.



Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BL	.370	.400	9.40	10.16	
BW	.235	.260	5.97	6.60	
BW_1	.125		3.18		
BW_2	.030		0.76		
CH	.045	.095	1.52	2.41	
LL	.250	.370	6.35	9.40	
LO	.005		0.13		
LO_2	.005	.050	0.13	1.27	2
LS	.050 BSC		1.27 BSC		3, 5
LT	.003	.006	0.08	0.15	6
LW	.015	.019	0.38	0.48	6

NOTES:
1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area limited by pin 3 and package centerline. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The true position pin spacing is located within ±.005 inch (0.13 mm) of its true longitudinal position relative to pins 1 and 14.
4. Dimension LO_2 shall be measured at the point of exit of the lead from the body.
5. Twelve places.
6. All leads: Dimensions are pre-solder dip.
7. Dimensions are in inches.
8. Millimeters are given for general information only.
9. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

* FIGURE 8. Physical dimensions for type 1N6510.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-883 - Microcircuits.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM F30 - Standard Specification for Iron-Nickel Sealing Alloys

(Application for copies should be addressed to ASTM International, PO Box C700, 100 Barr Harbor West, Conshohocken, PA 19428-2959 Website is http://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

* 3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

- V_{fr} - Forward recovery voltage. Specified maximum forward voltage used to determine forward recovery time.
- I_{RX} - Reverse current for each diode of test section.
- V_{FX} - Forward voltage for each diode of test section.
- I_{Ri} - Isolation current between any two interconnect pins of adjacent parallel sets of diodes with all other pins open circuited.

* 3.4 Interface and physical dimension. The interface and physical dimension shall be as specified in MIL-PRF-19500, and figures 1, 2, 3, 4, 5, 6, 7, and 8. Schematic diagrams are specified in figure 9. No organic or polymeric materials shall be used.

* 3.4.1 Lead material and finish. Lead material shall be Kovar, F-15 alloy, or alloy 42 as specified in ASTM F-30. Lead finish shall be gold-plated or solderable in accordance with MIL-PRF-19500. Where a choice of lead material of finish is desired, it shall be specified in the contract or order (see 6.2).

3.4.2 Die mounting. Pure glass shall not be used for die mounting. Metal glass die mounting is acceptable with qualifying activity approval for die with area greater than 1,000 square mils.

3.5 Marking. Devices shall be marked as specified in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTXV, and JANTX levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. Specified electrical measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurements	
	JANS level	JANTX and JANTXV levels
1	Method 2010 of MIL-STD-883, condition B.	Method 2010 of MIL-STD-883, condition B (JANTXV only).
7	Optional	Optional
9	Not applicable	Not applicable
11	I_{R1} and V_{F1}	I_{R1} and V_{F1}
12	See 4.3.1.	See 4.3.1.
13	Subgroups 2 and 3 of table I herein; ΔI_{R1} = 100 percent ofinitial reading or 10 nA dc,whichever is greater. ΔV_{F1} = ± 25 mV dc of initial reading.	Subgroup 2 of table I herein; ΔI_{R1} = 100 percent ofinitial reading or ± 25 nA dc,whichever is greater. ΔV_{F1} = ± 30 mV dc of initial reading.
14	Required	Required

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows (see 4.5.7): T_A = +150°C. Time = 72 hours minimum. V_R = 50 V dc for 1N5768, 1N5770, 1N5772, 1N5774, 1N6496, 1N6506, 1N6507, 1N6508, and 1N6509. V_R = 60 V dc for 1N6100, 1N6101, 1N6510, and 1N6511.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, table I herein, and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) and table E-VIb (JAN, JANTX, JANTXV) of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Conditions
B7	1027	T_A = +150°C each diode DC blocking, V_R = 50 V dc.

4.4.2.2 Group B inspection, table E-VIb (JANTX and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Conditions
B3	1027	DC blocking; T_A = +150°C; V_R = 50 V dc.
B4	2037	Test condition A

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.3.1 Group C inspection, table E-VII of MIL-PRF-19500.

Subgroup	Method	Conditions
C2	1056	Test condition A
C6	1026	T_A = +150°C; V_R = 50 V dc.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of MIL-PRF-19500, and table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Measurement of reverse current for 1N5772, 1N5774, 1N6496 1N6508, and 1N6509. For 1N5772, 1N5774, 1N6496, 1N6508, and 1N6509, the reverse current shall be measured using a circuit which bypasses the shunt resistance through the other diodes not under test, around the current meter. Care should be taken to assure that the voltage drop across the current meter is less than 10 millivolts.

4.5.2 Forward voltage. This parameter shall be measured 90 microseconds after the leading edge of the pulse.

4.5.3 Peak forward voltage. During this test, the maximum shunt capacitance across the diode shall be 19 pF and the equipment bandwidth shall be 80 MHz minimum.

4.5.4 Pin-to-pin capacitance. This parameter is the total pin-to-pin capacitance across each individual diode and may not necessarily represent actual diode capacitance since they are all connected together at either the anode or cathode and these connections represent additional capacitance.

4.5.5 Reverse current (I_{RX}) and forward voltage (V_{FX}). Each common anode section and each common cathode section shall be tested separately. Each diode in the test section shall be measured individually after the array has reached thermal equilibrium.

4.5.6 Isolation current (I_R); bridging current(I_{Rbr}). These devices shall be subjected to the isolation current/bridging current tests as specified:

a. For types 1N5772, 1N5774, 1N6496, 1N6508, and 1N6509, the bridging current shall be measured by supplying the forcing function to every other interconnect pin and measuring the remaining interconnect pins (excluding common anode and common cathode pins), I_{Rbr}. Repeat the test, reversing the polarity of the forcing function.

b. For types 1N6100, 1N6101, 1N6511, and 1N6510, the bridging current shall be measured by applying the forcing function to every other diode (anode and cathode simultaneously) and measuring the remaining diodes (anode and cathode simultaneously), I_{Rbr}. Repeat the test, reversing the polarity of the forcing function.

c. For types 1N5774, 1N6496, and 1N6509, the isolation current shall be measured between the individual circuits by applying the forcing function to the anode and cathode of one circuit and measuring to the anode and cathode of other circuit, I_{Ri}. Repeat the test, reversing the polarity of the forcing function.

d. For types 1N5768 and 1N6506, the forcing function shall be applied to every other anode and measured on the remaining anodes, I_{Rbr}. Repeat the test, reversing the polarity of the forcing function.

e. For types 1N5770 and 1N6509, the forcing function shall be applied to every other cathode and measured on the remaining cathodes, I_{Rbr}. Repeat the test, reversing the polarity of the forcing function.

* 4.5.7 Free air power burn-in and life tests. The use of a current limiting or ballast resistor is permitted provided that each device under test still sees the full P_t (minimum) and that the minimum applied voltage, where applicable, is maintained throughout the burn-in period. Method 3100 of MIL-STD-750 shall be used to measure T_J.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical Inspection	2071					
Subgroup 2						
Breakdown voltage	4021		$V_{(BR)}$			
1N5768, 1N5770, 1N5772 1N5774, 1N6496, 1N6506 1N6507, 1N6508, 1N6509		I_R = 10 µA dc; PW = 100 ms maximum duty cycle ≤ 20 percent		60		V dc
1N6100, 1N6101, 1N6510 1N6511		I_R = 5 µA dc; PW = 100 ms maximum; duty cycle ≤ 20 percent		75		V dc
Reverse current	4016	DC method (see 4.5.1)				
All types		V_R = 40 V dc	I_{R1}		.1	µA dc
1N6100, 1N6101, 1N6510 1N6511		V_R = 20 V dc	I_{R2}		25	nA dc
Forward voltage	4011	PW = 300 µs ± 50 µs; duty cycle ≤ 2 percent (see 4.5.2)				
All types		I_F = 100 mA dc	V_{F1}		1.0	V dc
1N5768, 1N5770, 1N5772 1N5774, 1N6496, 1N6506 1N6507, 1N6508, 1N6509		I_F = 500 mA dc	V_{F2}		1.5	V dc
Subgroup 3						
High temperature operation:		T_A = +150°C				
Reverse current	4016	DC method; V_R = 40 V dc				
Low temperature operation:		T_A = -55°C	I_{R3}		50	µA dc
Forward voltage	4011	I_F = 10 mA dc	V_{F3}		1	V dc

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Forward recovery voltage (peak)	4026	PW ≥ 150 ns; R_S = 50Ω; t_r = 10 ns; duty cycle ≤ 2 percent (see 4.5.3)	V_{F4}			
1N5768, 1N5770, 1N5772, 1N5774, 1N6496, 1N6506, 1N6507, 1N6508, 1N6509		I_F = 500 mA			5	V (pk)
1N6100, 1N6101, 1N6510, 1N6511		I_F = 100 mA			5	V (pk)
Capacitance (pin-to-pin)	4001	V_R = 0 V dc; f = 1 MHz (see 4.5.4)	C_t			
1N5770, 1N5772, 1N5774, 1N6496, 1N6507, 1N6508, 1N6509					8	pF
1N5768, 1N6100, 1N6101, 1N5605, 1N6510, 1N6511					4	pF
Forward recovery time	4026	PW ≥ 150 ns; R_S = 50Ω; duty cycle ≤ 2 percent, t_r = 10 ns; V_{fr} = 1.1 V dc	t_{fr}			
1N5768, 1N5770, 1N5772, 1N5774, 1N6496, 1N6506, 1N6507, 1N6508, 1N6509		I_F = 500 mA dc			40	ns
1N6100, 1N6101, 1N6510, 1N6511		I_F = 100 mA dc			15	ns
Reverse recovery time						
1N5768, 1N5770, 1N5772 1N5774, 1N6496, 1N6506 1N6507, 1N6508, 1N6509	4031	Condition B; I_F = I_R = 200 mA; R_L = 100 Ω; I_{rr} = 20 mA	t_{rr}		20	ns
1N6100, 1N6101, 1N6510 1N6511		Condition B; I_F = I_R = 10 mA; R_L = 100 Ω; I_{rr} = 1 mA			10	ns
Forward voltage (match) 1N6100, 1N6101, 1N6510 1N6511	4011	I_F = 10 mA	V_{F5}		5	mV

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Not applicable						
Subgroup 6						
Surge current	4066	I_{FSM} = 500 mA(pk); 10 surges at one per minute; t_p = 1/120 s; choose four diodes from each array in cycles.				
Electrical measurements		See table. I, subgroup 2				
Subgroup 7						
Reverse current (except omit for the following devices.)	4016	DC method; V_R = 40 V dc; I_F = 25 mA dc for each of the other diodes in the test section (see 4.5.5).	I_{RX}		10	µA dc
1N6100, 1N6101, 1N6510, 1N6511						
Forward voltage (except omit for the following devices.)	4011	I_F = 25 mA dc; I_F = 25 mA dc for each of the other diodes in the test section (see 4.5.5)	V_{FX}		1.0	V dc
1N6100, 1N6101, 1N6510 1N6511						
Bridging current (all devices)	4016	DC method; V_R = +40 V dc and -40 V dc (see 4.5.6.a through 4.5.6.d)	I_{Rbr}		0.8	µA dc
Isolation current	4016	DC method; V_R = +40 V dc and -40 V dc (see 4.5.6.c)	I_{Ri}			
1N5774 1N6496 1N6509					0.8	µA dc

1/ For sampling plan, see MIL-PRF-19500.

TABLE II. Group E inspection (all quality levels) for qualification and requalification only.

Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
Subgroup 1			n = 45, c = 0
Temperature cycling	1051	500 cycles, -65°C to +175°C	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurement		See table I, subgroup 2.	
Subgroup 2			
Intermittent operating life	1037	10,000 cycles.	
Electrical measurements		See table I, subgroup 2.	
Subgroups 4, 5, 6, 7, 8 and 9			
Not applicable			

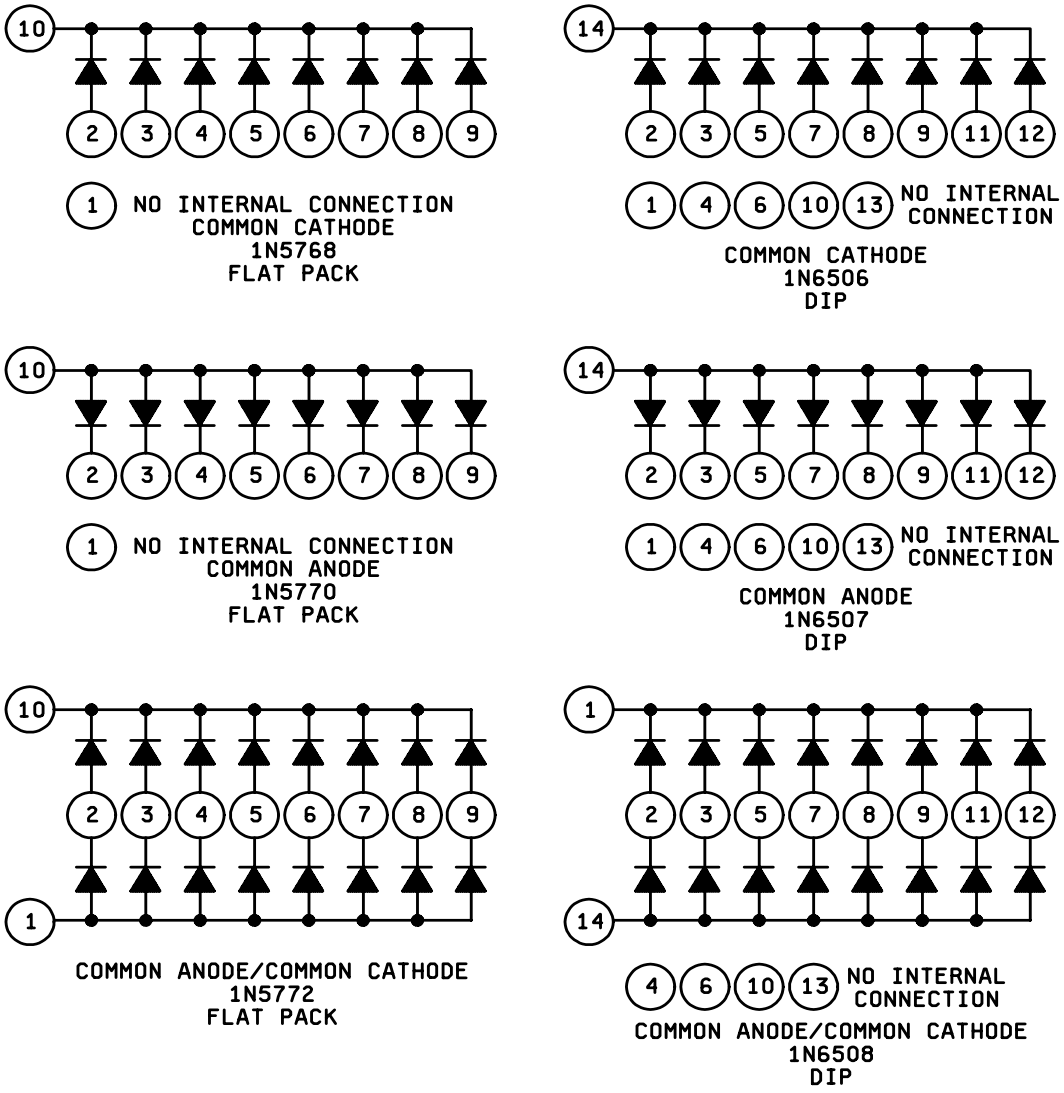
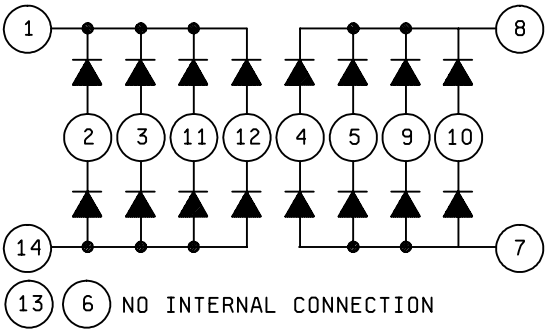


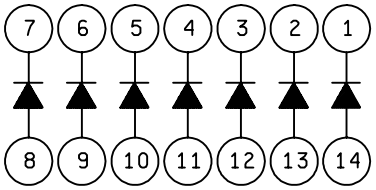
FIGURE 9. Schematics.



DUAL COMMON ANODE/COMMON CATHODE

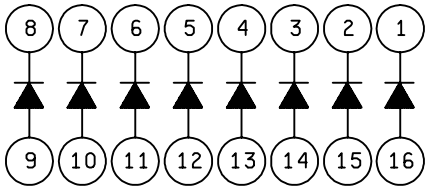
1N5774 FLAT PACK

1N6509 DIP



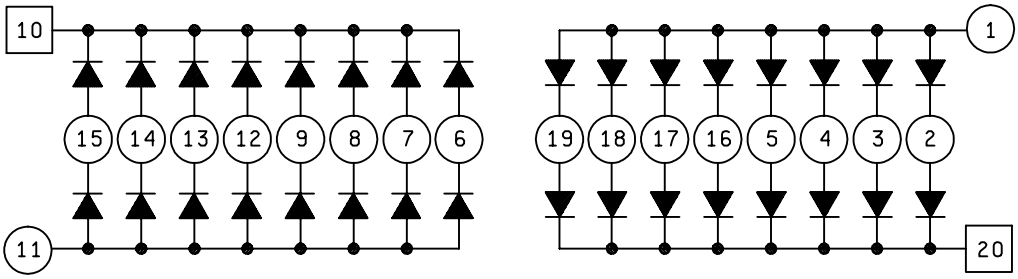
1N6100 FLAT PACK

1N6511 DIP



1N6101 DIP

1N6510 FLAT PACK



DUAL COMMON ANODE/COMMON CATHODE

1N6496 FLAT PACK

FIGURE 9. Schematics - continued.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. Destructive physical analysis when requested.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

* 6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army - AR, AV, MI, SM
Navy - AS, MC
Air Force - 99

Preparing activity:
DLA - CC

(Project 5961-2006-066)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.

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