DC MOTOR PULSE WIDTH MODULATOR

Description

The SG1731 is a pulse width modulator circuit designed specifically for DC motor control. It provides a bi-directional pulse train output in response to the magnitude and polarity of an analog error signal input. The device is useful as the control element in motor-driven servo systems for precision positioning and speed control, as well as in audio modulators and amplifiers using carrier frequencies to 350 kHz.

The circuit contains a triangle waveform oscillator, a wideband operational amplifier for error voltage generation, a summing/ scaling network for level-shifting the triangle waveform, externally programmable PWM comparators and dual ±100 mA, ±22 V totem pole drivers with commutation diodes for full bridge output. A SHUTDOWN terminal forces the drivers into a floating high-impedance state when driven LOW. Supply voltage to the control circuitry and to the output drivers may be from either dual positive and negative supplies, or single-ended.

Features

- ±3.5 V to ±15 V Control Supply
- ±2.5 V to ±22 V Driver Supply
- Dual 100 mA Source/Sink Output Drivers
- 5 kHz to 350 kHz Oscillator Range
- High Slew Rate Error Amplifier
- Adjustable Deadband Operation
- Digital $\overline{\text{SHUTDOWN}}$ Input

High Reliability Features

- Available to MIL-STD-883
- Available to DSCC
  – Standard Microcircuit Drawing (SMD)
- MSC-AMS level "S" Processing Available

Block Diagram

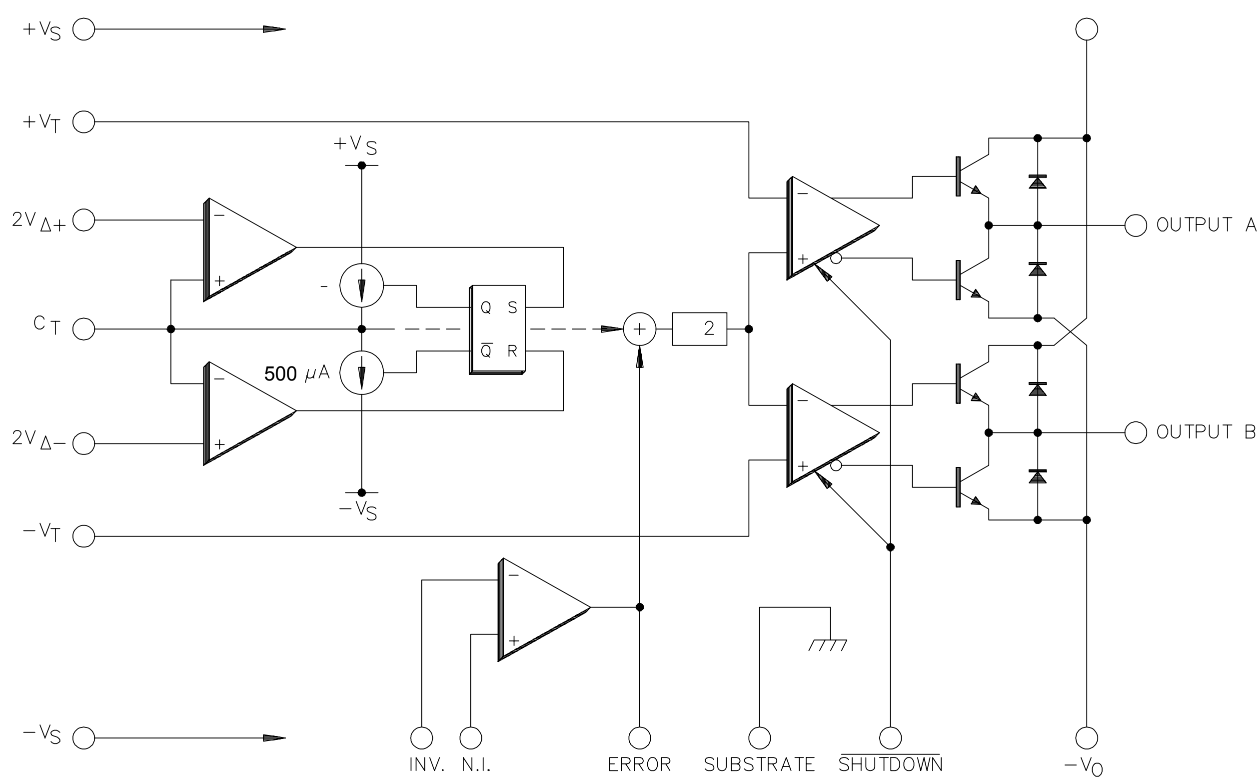

Figure 1 · Block Diagram

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Absolute Maximum Ratings (Note 1)

Supply Voltage ($\pm V_S$) .... ±18 V
Analog Inputs .... $\pm V_S$
Digital Inputs (SHUTDOWN) .... $-V_S$-0.3 V to $-V_S$+18 V
Output Driver Supply Voltage ($\pm V_O$) .... ±25 V
Source/Sink Output Current (continuous) .... 200 mA
Source/Sink Output Current (peak, 500 ns) .... 400 mA

Note 1. Values beyond which damage may occur. Extended operation at the maximum levels may degrade performance and affect reliability.

Output Driver Diode Current (continuous) .... 200 mA
Output Driver Diode Current (peak, 500 ns) .... 400 mA
Operating Junction Temperature
Hermetic (J - Package) .... 150°C
Plastic (N - Package) .... 150°C
Storage Temperature Range........ -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) .... 300°C
RoHS Peak Package Solder Reflow Temp.(40 sec. max. exp.)...... 260°C (+0, -5)

Thermal Data

J Package:
Thermal Resistance-Junction to Case, θ_{JC} .... 30°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} .... 80°C/W
N Package:
Thermal Resistance-Junction to Case, θ_{JC} .... 40°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} .... 65°C/W
L Package:
Thermal Resistance-Junction to Case, θ_{JC} .... 35°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} .... 120°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

Recommended Operating Conditions (Note 2)

Supply Voltage Range ($\pm V_S$) .... ±3.5 V to ±15 V
Error Amp Common-Mode Range .... $-V_S$ + 3 V to V_S - 3 V
Output Driver Supply Voltage Range........ ±2.5 V to ±22 V
Source/Sink Output Current (continuous) .... 100 mA
Source/Sink Output Current (peak, 500 ns) .... 200 mA
Output Driver Diode Current (continuous) .... 100 mA
Output Driver Diode Current (peak, 500 ns) .... 200 mA

Oscillator Frequency Range .... 10 Hz to 350 kHz
Oscillator Voltage (Peak-to-Peak) ....1 V to 10 V
Oscillator Timing Capacitor (C_T) .... 200 pF to 2.5 µF
Operating Ambient Temperature Range
SG1731 .... -55°C to 125°C
SG2731 .... -25°C to 85°C
SG3731 .... 0°C to 70°C

Note 2. Range over which the device is functional and parameter limits are guaranteed.

Electrical Characteristics

(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG1731 with -55°C ≤ T_A ≤ 125°C, SG2731 with -25°C ≤ T_A ≤ 85°C, SG3731 with 0°C ≤ T_A ≤ 70°C, V_S = ±15 V, and V_O = ±22 V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1731/2731/3731			Units
		Min.	Typ.	Max.	
Oscillator Section					
C_T Charging Current	T_A = 25°C	450	500	550	µA
	$T_A = T_{MIN}$ to T_{MAX}	400		600	µA
2V∆± Input Bias Current	V_{CM} = ±5 V			-20	µA
Initial Oscillator Frequency	C_T = 1000 pF, 2V∆± = ±5 V, T_A = 25°C	22.5	25.0	27.5	kHz
Temperature Stability (Note 3)	C_T = 1000 pF, 2V∆± = ±5 V			10	%
Error Amplifier Section (Note 5)					
Input Offset Voltage				10	mV
Input Bias Current				3	µA
Input Offset Current				600	nA
Open Loop Voltage Gain	R_L = 2 kΩ	70			dB
Output Voltage Swing	R_L = 2 kΩ	±10			V
Common-Mode Rejection Ratio		70			dB
Slew Rate (Notes 3 and 4)	T_A = 25°C	5	10		V/µs
Unity Gain Bandwidth (Notes 3 and 4)	T_A = 25°C	0.7	1		MHz
PWM Comparators					
Input Bias Current	$\pm V_T$ = ±3 V			6	µA

Electrical Characteristics (Continued)

Parameter	Test Conditions	SG1731/2731/3731 Min.	Typ.	Max.	Units
$\overline{\text{SHUTDOWN}}$ Section					
Logic Threshold	$-V_S$ = -3.5 V to -15 V	V_S+0.8		V_S+2.0	V
$\overline{\text{SHUTDOWN}}$ HIGH Current	$V_{\overline{SHUTDOWN}}$ = $-V_S$+2.4 V			400	µA
$\overline{\text{SHUTDOWN}}$ LOW Current	$V_{\overline{SHUTDOWN}}$ = $-V_S$			-1.0	mA
Output Drivers (Each Output)					
HIGH Output Voltage	I_{SOURCE} = 20 mA	19.2			V
	I_{SOURCE} = 100 mA	19.0			V
LOW Output Voltage	I_{SINK} = 20 mA			-19.2	V
	I_{SINK} = 100 mA			-19.0	V
Driver Risetime	C_L = 1000 pF			300	ns
Driver Falltime	C_L = 1000 pF			300	ns
Total Supply Current					
V_S Supply Current	$V_{\overline{SHUTDOWN}}$ = $-V_S$ + 0.8 V			14	mA
V_O Supply Current	$V_{\overline{SHUTDOWN}}$ = $-V_S$ + 0.8 V			6	mA

Note 3. These parameters, although guaranteed, are not tested in production.
Note 4. Unity Gain Inverting 10 kΩ Feedback Resistance.
Note 5. V_{CM} = ±12 V.

Application Information

SUPPLY VOLTAGE

The SG1731 requires a supply voltage for the control circuitry (V_S) and for the power output drivers (V_O). Each supply may be either balanced positive and negative with respect to ground, or single-ended. The only restrictions are:

1. The voltage between $+V_S$ and $-V_S$ must be at least 7.0 V; but no more than 44 V.
2. The voltage between $+V_O$ and $-V_O$ must be at least 5.0 V; but no more than 44 V.
3. $+V_O$ must be at least 5 V more positive than $-V_S$. This eliminates the combination of a single-ended positive control supply with a single-ended negative driver supply.

SUBSTRATE CONNECTION

The substrate connection (Pin 10) must always be connected to either $-V_S$ or $-V_O$, whichever is more negative. The substrate must also be well bypassed to ground with a high quality capacitor.

OSCILLATOR

The triangle oscillator consists of two voltage comparators, a set/reset flip-flop, a bi-directional 500 µA current source, and an external timing capacitor C_T. A positive reference voltage (2VΔ+) applied to Pin 2 determines the positive peak value of the triangle, and a negative reference voltage (2VΔ-) at Pin 7 sets the negative peak value of the triangle waveform. Since the value of the internal current source is fixed at a nominal ±500 µA, the oscillator period is a function of the selected peak-to-peak voltage excursion and the value of C_T. The theoretical expression for the oscillator period is:

$$T_{OSC} = \frac{2C_T\,dV}{5 \times 10^{-4}} \quad \text{(Eq.1)}$$

where C_T is the timing capacitor in Farads and dV is V_{OSC} in Volts peak-to-peak.

As a design aid, the solutions to Equation 1 over the recommended range of T_{OSC} and V_{OSC} are given in graphic form in Figure 1. The lower limit on T_{OSC} is 1.85 µs, corresponding to a maximum frequency of 350 kHz. The maximum value of V_{OSC}, (2VΔ+) - (2VΔ-), is 10 V peak-to-peak for linear waveforms.

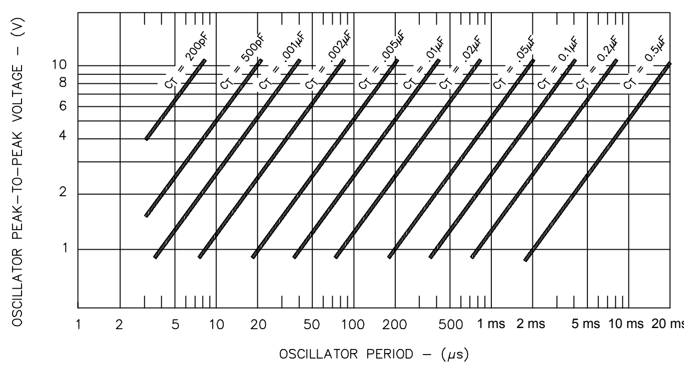


Figure 2 · SG1731 Oscillator Period VS. V_{OSC} and C_T

ERROR AMPLIFIER

The error amplifier of the SG1731 is a conventional internally-compensated operational amplifier with low output impedance. All of the usual feedback and frequency compensation techniques may be use to control the closed-loop gain characteristics. The control supply voltage $\pm V_S$ will determine the input common mode range and output voltage swing; both will extend to within 3 V of the V_S supply.

PULSE WIDTH MODULATION

Pulse width modulation occurs by comparing the triangle waveform to a fixed upper ($+V_T$) and lower ($-V_T$) threshold voltage. A crossing above the upper threshold causes Output A to switch to the HIGH state, and a crossing below

Application Information (Continued)

the lower threshold causes Output B to switch to the HIGH state. If $\pm V_S$ is less than ±8 V then $\pm V_T$ can be obtained with resistors from $\pm V_S$. If $\pm V_S$ is greater than ±8 V use zeners.

Threshold crossings are generated by shifting the triangle waveform up and down with the error voltage (Pin 5). A positive error voltage will result in a pulse width modulated output at Driver A (Pin 13). Similarly, a negative error voltage produces a pulse train at Driver B (Pin 12). Figure 2 illustrates this process for the case where $V\Delta+$ is greater than V_T.

It is important to note that the triangle shifting circuit also attenuates the waveform seen at C_T by a factor of 2. This results in a waveform at the PWM comparators with a positive peak of $V\Delta+$ and a negative peak of $V\Delta-$, and must be taken into account when selecting the values for $+V_T$ and $-V_T$.

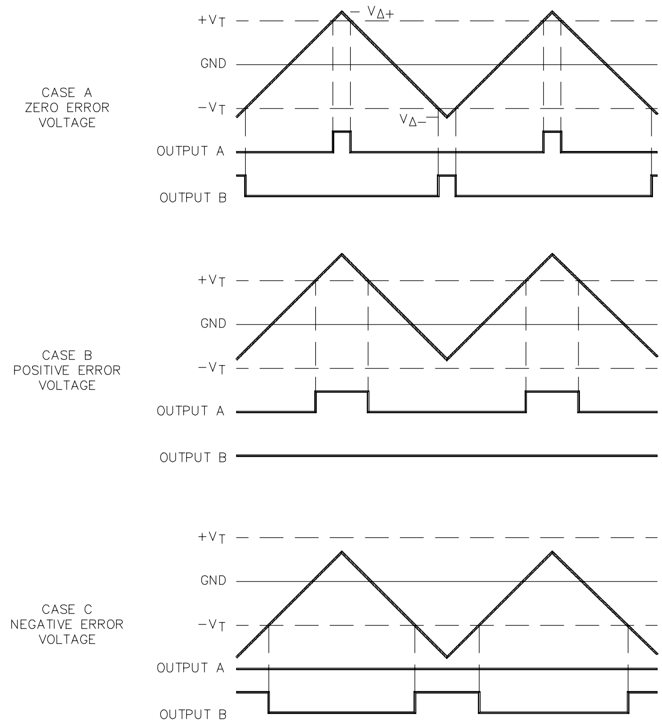


Figure 3 - Pulse Width Modulation with No Deadband

Application Circuits

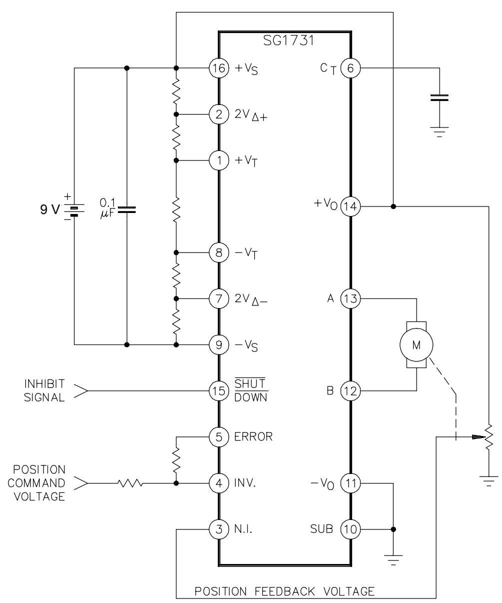


Figure 4

In this simple battery-powered position servo, the control supply and driver supply are both single-ended positive with respect to ground.

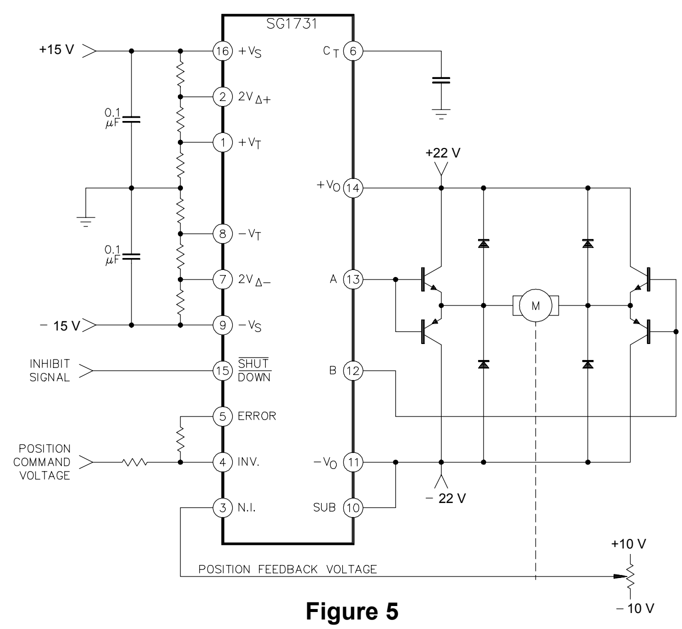


Figure 5

A high torque position servo is obtained by buffering the output drivers to obtain higher output current.

Application Circuits (Continued)

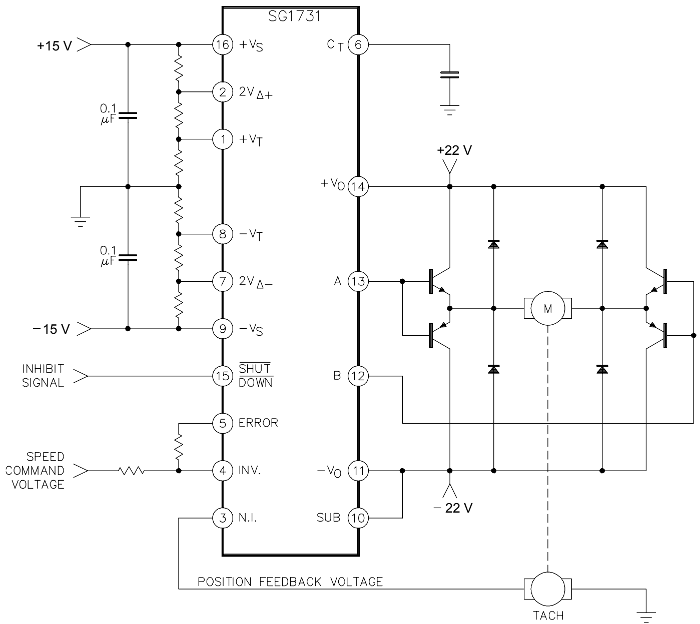


Figure 6

Bi-directional speed control results when the feedback voltage transducer is a tachometer.

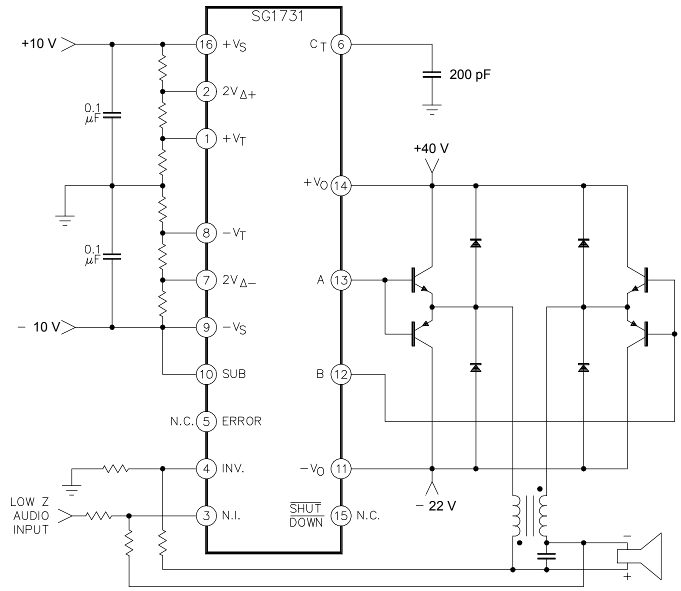
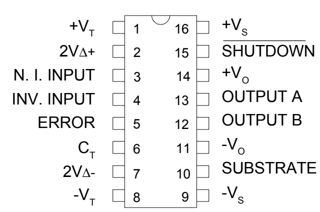
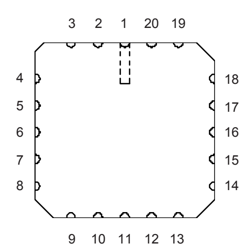


Figure 7

The two-quadrant transfer function of the SG1731 is ideal for pulse width modulated audio power amplifiers.

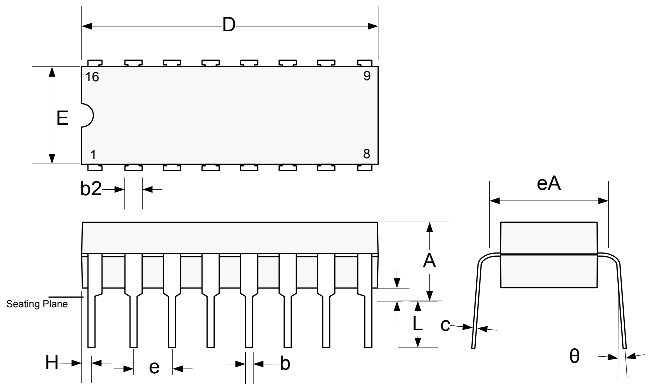
Connection Diagrams & Ordering Information (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1731J- 883B SG1731J-DESC SG1731J	-55°C to 125°C -55°C to 125°C -55°C to 125°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2731N SG3731N	-25°C to 85°C 0°C to 70°C	N Package: RoHS Compliant / Pb-free Transition DC: 0503 N Package: RoHS / Pb-free 100% Matte Tin Lead Finish
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1731L SG1731L- 883B	-55°C to 125°C -55°C to 125°C	1 NC 2 +VT 3 2VΔ+ 4 N. I. INPUT 5 INV. INPUT 6 NC 7 ERROR 8 CT 9 2VΔ- 10 -VT  11 NC 12 -VS 13 SUBSTRATE 14 -VO 15 OUTPUT B 16 NC 17 OUTPUT A 18 +VO 19 SHUTDOWN 20 +VS

Note 1. All packages are viewed from the top.
Note 2. Contact factory for leadless chip carrier availability.
Note 3. Hermetic Packages J, L use Sn63/Pb37 hot solder lead finish, Contact factory for availability of RoHS versions.

Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.

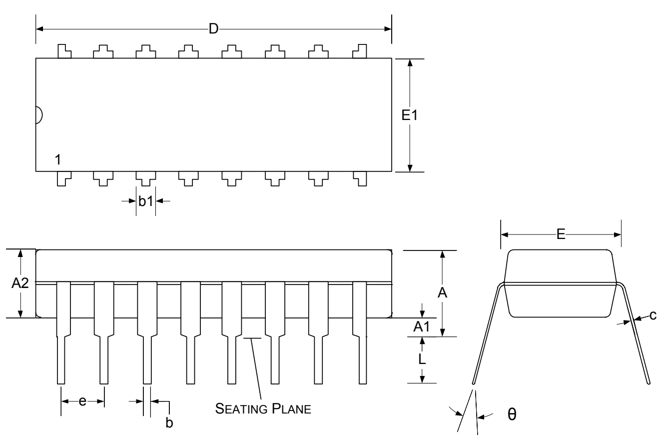


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.08	-	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	5.08	0.125	0.200
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 8 · J 16-Pin Ceramic Dual Inline Package Dimensions



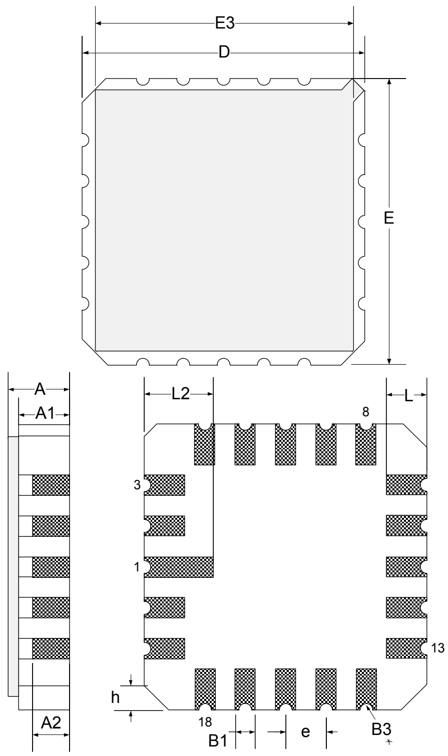
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.33	-	0.210
A1	0.38	-	0.015	-
A2	3.30 Typ.		0.130 Typ.	
b	0.36	0.56	0.014	0.022
b1	1.14	1.78	0.045	0.070
c	0.20	0.36	0.008	0.014
D	18.67	19.69	0.735	0.775
e	2.54 BSC		0.100 BSC	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
L	2.92	0.381	0.115	0.150
θ	-	15°	-	15°

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 9 · N 16-Pin Plastic Dual Inline Package Dimensions

Package Outline Dimensions (Continued)



DIM	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 10 · L 20-Pin Ceramic LCC Package Outline Dimensions

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SG1731-1.4/05.15