MIPI CSI-2 Transmitter Application Note



AN5494

Introduction (Ask a Question)

Mobile Industry Processor Interface (MIPI) CSI-2 (Camera Serial Interface) transmitter is a fundamental element in camera systems, enabling the rapid transfer of video and image data from the sensor to a processing device. Developed by the MIPI Alliance, CSI-2 is a standard interface widely utilized in devices like smartphones, cars, and drones. This transmitter supports 1 to 4 data lanes for high-speed transmission and utilizes D-PHY for communication. It flexibly handles raw, compressed, and metadata formats, achieving impressive data rates, especially with multiple lanes. The robust protocol employs a packet-based system with commands and handshaking for reliable data transfer. Designed for low-power consumption, this transmitter is crucial for battery-operated devices and is adaptable to support various resolutions and frame rates. In essence, the MIPI CSI-2 transmitter plays a pivotal role in modern camera technology, facilitating the efficient and high-quality capture and transmission of visual data.

Microchip FPGAs present a cost-optimized and powerful platform for meeting the following edge computing requirements for intelligent vision systems:

- Power efficiency with two times more performance per watt
- Smaller form-factors as small as 11x11 mm
- Exceptional reliability with zero configuration upsets
- Military-grade security with best cyber and anti-tamper security

Microchip's PolarFire SoC and PolarFire FPGAs integrate camera sensor interfaces like MIPI and Scalable Low-Voltage Signaling (SLVS), an image signal processing unit, and transport interfaces like CoaXPress, HDMI, 10GigE Vision, SDI, and wireless connectivity. They are ideally suited for applications involving embedded vision and deep learning inference. They seamlessly support as well as integrate diverse protocols and interfaces with minimal developer effort as part of a complete system solution.

This application note demonstrates generating MIPI CSI-2 video using the PolarFire[®] FPGA Video and Imaging Kit and MIPI TX FMC card, and receiving and displaying the video using Raspberry Pi 4 Model B.

- The Raspberry Pi 4 Model B uses a 2 lane MIPI configuration to transfer video at 800 Mbps/lane, transmitting Full HD RAW8 video at 30 fps.
- It provides a reference design with 4 lane MIPI configuration to transfer video at 2.5 Gbps/lane, transmitting 4K RAW8 video at 120 fps.

MIPI CSI-2 Transmitter IP supports two output modes: One Byte mode with IOD interface and Two Byte mode with Transceiver interface. This demo showcases the MIPI CSI-2 transmitter design using the Two Byte mode configuration with the Transceiver Interface. It highlights the system's ability to transmit data at 2.5 Gbps per lane through a transceiver.

Summary (Ask a Question)

The following table provides a summary of the MIPI CSI-2 Transmitter IP characteristics.

Core Version	This document applies to MIPI CSI-2 Transmitter v5.0
Supported Device Families	 PolarFire[®] SoC PolarFire
Supported Interfaces	 Native Interface AXI4-Lite Video Interface AXI4 Stream Video Interface
Licensing	The core is license-locked for clear text RTL. It supports the generation of Encrypted RTL for the Verilog version of the core with no license.

Features (Ask a Question)

The following table lists the supported features of the MIPI CSI-2 Transmitter IP.

Table 2. Supported Features

Supported Features	Description
MIPI Specification Version	This document applies to MIPI CSI-2 v2.0
Data Type	Raw-8, Raw-10, Raw-12, Raw-14, Raw-16, and RGB-888
Lanes	1, 2, 4, and 8 lanes
Speed	2.5 Gbps per lane with Transceiver interface
Output Mode	Supports the following output modes: One Byte mode:
	• Up to 1 Gbps per lane with IOD interface for 1, 2, 4, and 8 lanes
	• Up to 1.5 Gbps per lane with Transceiver for 1, 2, 4, and 8 lanes
	Two Byte mode:
	IOD interface is not supported
	• Up to 2.5 Gbps per lane with Transceiver for 1, 2, and 4 lanes
Input Pixels	 Supports the following input pixels: 1: One pixel per clock 4: Four pixels per clock 8: Eight pixels per clock (only supported when Two Byte mode is enabled)
Interface	 Supports the following interfaces: Native Interface AXI4-Lite Video Interface AXI4 Stream Video Interface
Embedded Data	Embedded packet transmission for 1, 2, 4, and 8 lanes
PHY Interface	D-PHY

The following table lists the unsupported features of the MIPI CSI-2 Transmitter.

Table 3. Unsupported Features

Unsupported Features	Description
LP transactions	IP does not support transactions in Low power mode
Line Short Packet	IP does not support Line Start and Line End short packets as it is optional



continued	
Unsupported Features	Description
Virtual Channel Extension (VCX)	VCX field is not supported
LRTE	Latency Reduction and Transport Efficiency (LRTE) is not supported
USL	Unified Serial Link is not supported
Scrambling	Data scrambling is not supported
SROI	Smart Region of Interest is not supported
Deskew	Deskew Feature is not supported

Important: This design

- This design configuration utilizes Raw-8 for 4 Lanes, Two Byte mode with 8-input pixels, Native Interface, 4K Resolution at 120 FPS with Transceiver Interface capable of supporting 2.5 Gbps per lane.
- Datawidth for Raw-8, Raw-10, Raw-12, Raw-14, Raw-16, and RGB-888 are: 8, 10, 12, 14, 16, and 24, respectively.



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1. Design Description (Ask a Question)

The MIPI CSI-2 Transmitter is connected to a XCVR, as shown in the following block diagram. The display controller and test pattern generator are the components of the video source that generate Bayer data. The CCC is provided with a reference clock by the on-board 50 MHz clock. Bayer data is received by the MIPI CSI-2 transmitter and pixel data is arranged in Bytes and Lanes format as per D-PHY specifications. XCVR lanes are connected to byte data accordingly.

Important: The reference design shows Test pattern generator connected to MIPI Tx IP as a video source. Alternatively, a camera or another video source could be connected to MIPI Tx IP with corresponding video pipeline.

The following figures show the block diagram of the design.



Figure 1-1. 2 Lane MIPI Configuration for Raspberry Pi 4 Model B







1.1 Hardware Implementation (Ask a Question)

The following figures show the Libero[®] SoC implementation of the top-level SmartDesign.

Figure 1-3. High-Level MIPI CSI-2 Transmitter Design—2 Lane



Figure 1-4. High-Level MIPI CSI-2 Transmitter Design—4 Lane



The MIPI CSI-2 Transmitter design includes the following key blocks:

- MIPI CSI-2 Transmitter Configuration
- XCVR Configuration
- Display Controller Configuration
- Test Pattern Configuration

Important: A TX PLL is required to generate the XCVR clocks, that is, byte clock, the MIPI bit clock, and 90° phase shifted bit clock, whose frequency is based on the pixel clock and the number of Lanes used.



1.1.1 MIPI CSI-2 Transmitter Configuration (Ask a Question)

The MIPI CSI-2 Transmitter is configured as follows for 4K (3840 x 2160) resolution.

- Raw-8 Data type
- 4 Lanes
- 2 bytes at output
- 8 input pixels

Figure 1-5. MIPI CSI-2 Transmitter Configuration

Configuration		
DataType	RAW-8	•
No of MIPI Lanes	4	•
Byte Frequency in MHz	156	
Horizontal Resolution	3840	
No of Pixels	8	•
Output Mode	2 Bytes	•
Video Interface:	Native	•



Important: For more information, see MIPI CSI-2 Transmitter IP.

1.1.2 XCVR Configuration (Ask a Question)

The transceiver configuration for the MIPI CSI-2 Transmitter implementation is shown in the following figures. For 4 Lane implementation two XCVR Quads are required.

In the following figure, the transceiver is configured in TX only mode in a 3 Lane configuration with one clock and two data lanes. The clock signal is carried by LANEO, while Lanes 1 and 2 carry MIPI CSI-2 Transmitter output data.



	<				
PE XCVR default configuration	General				
10GBASE-R			_		
10GBASE-KR	Transceiver mode	Tx only 💌	Enhanced receiver mana	gement	
SGMII	Number of Issue	2	Receiver calibration	11/4	
QSGMII	Number of Idnes	15		data ana	-
CPRI Rate 1				uala eye	
CPRI Rate 2			Incrementally recalibrate	DFE coefficients	
CPRI Kate 3					
CDDI Pate 5	PMA Settings				
DRI Rate 6					
CDRI Rate 7	TX data rate	2500 Mbps	RX data rate	N/A Mbps	
PRI Rate 8	The share the state of the state	-	DV CDD lash weeks	11/6	
SDI 3G	TX Clock division factor	14	KA CDR look mode	0/8	
SDI HD	TX PLL base data rate	10000.000 Mbps	RX CDR reference clock sour	e N/A 💌	
SDI SD	TV DU bit dark from some	5000 000 MM-	DV CDD andreases shall free	MILL W MILL	
interlaken 6.25G	TX PLE bit dook frequency	3000.000	KA CONTELETED DE DOUTIES	inty n/a enz	
Interlaken 10G			RX JA dock frequency	N/A MHz	
XAUI					
RXAUI	PCS Settings				
JESD204B Receiver Link with AD9680					
IESD204B Transmitter Link with DAC39364	TX PCS-Fabric interface width	16 V bits	RX PCS-Eabric interface width	N/A y bits	
	TX FPGA interface frequency	156.25 MHz	RX FPGA Interface frequency	N/A MHz	
	@ DMA Made				
	- Fride Prode				
	Enable CDR Bit-slip p	iort			
	C Sh 10h Encoding Decoding				
	a contro broom gio control g				
tanto I Manumant I	C 64b6xb Gear Box				
man present	6 6d666h		C 6467h		
	E - 11 - 1		E = 11		
	Enable Disparity		I✓ Enable BER monitor sta	e machine	
	Enable Scrambler/De	scrambler	Enable 32 bits data wid	h	
	C Soft PIPE Interface				
	, bott a concrete				
	Protocol	PCIe Gen1 (2.5 Gbps) *			
	Clocks and Resets				
	Interface Clocks				
	Use as PLL reference	e dock			
	The shorts	Perferel -	DV ded	h//4	
	TX dock	Regional	RX dock	N/A Y	

Figure 1-6. Transceiver Interface Configuration—Instance 1

In the following figure, the transceiver is configured in TX only mode in a 2 Lane configuration with two output data lanes.

Figure 1-7. Transceiver Interface Configuration—Instance 2

PF_XCVR_default_configuration	🗄 General			
10GBASE-R		-1	C Extraction management	
10GBASE-KR	Transceiver mode Tx only	<u> </u>	Chinanceu receiver management	
SGMII	Number of lanes 2		Receiver calibration	N/A
QSGMI			Incrementally recalibrate data even	
CPRI Rate I			E a state a second data	
CPRI Rate 2			Incrementally recalibrate DPE coemcients	
CPRI Rate 3				
CDPI Pate 5	PMA Settings			
CPRI Rate 5				
CPRI Rate 0	TX data rate 2500	Mbps	RX data rate N/A	Mbps
CPRI Rate 7				
CPRI NALE O	TX clock division factor 4	<u> </u>	RX CDR. lock mode N/A	Ψ.
3013G	TV PLI have data rate 10000.000	Mhoe	DV CDD reference clock source	
SDIED		(app		
John SD Jakan 6 250	TX PLL bit dock frequency 5000.000	MHz	RX CDR reference dock frequency N/A	 MHz
Interlaken 10G			DV 14 dark frequency	MHz
XALII			KAUK OOK Inequency	
RYAII				
IESD2048 Receiver Link with AD9680	PCS Settings			
IESD2048 Transmitter Link with DAC 39184				
	TX PCS-Fabric interface width 16	▼ bits	RX PCS-Fabric interface width N/A	- bits
	TX FPGA interface frequency 156.25	MHz	RX FPGA interface frequency N/A	MHz
	G DWA Made			
	PMA Mode			
	Enable CDR Bit-slip port			
	8b10b Encoding/Decoding			
Apply New grant	C 64b6xb Gear Box			
Appry Herristeet.			C 64b67b	
	Enable Disparity		Enable BER monitor state machine	
	Enable Scrambler/Descrambler		Enable 32 bits data width	
	C Soft PIDE Interface			
	1 John a clandride			
	Protocol PCIe Gen1 (2.5	Gbps) 👻		
	Clocks and Resets			
	C) Choice and Resea			
	Interface Clocks			
	Use as PLL reference dock			
	TY dark Designal	-	DV dark N/A	*



Important:

- The outputs within the quad are aligned by enabling TX Lane Alignment in Tx PLL.
- The 90° phase shift between MIPI clock and data lanes within the quad is achieved by oversampling and shifting the clock.
- The outputs of two different quads may not be aligned consistently on every power cycle or reset.
- The total number of XCVR lanes required is n+1, where n is the number of MIPI data lanes and an additional XCVR lane is used for MIPI clock.



1.1.3 Display Controller Configuration (Ask a Question)

The Video and Electronics Standard Association (VESA) standard defines standard timing signals for interfacing with a display such as a monitor. The display controller generates display synchronization signals based on the VESA standard for various display resolutions. It generates the horizontal and vertical sync signals, the horizontal and vertical active signals, and the frame end and data enable signals. The timing parameters for standard resolutions are predefined in the IP, and the resolutions are selected from the configuration options.

4K (3840 x 2160) resolution is configured in the design, as shown in the following figure.



Configuration		
Dynamic Video Format CFG:	Enable 💌	
Video Format:	3840x2160 💌	
Number of Pixels:	4 💌	
Pipeline Delay compensation:	Disable 💌	
Pixel Data Width:	24	
Video Interface:	Native 💌	
Testbench:	User 💌	

1.1.4 Test Pattern Configuration (Ask a Question)

The pattern generator IP generates the test patterns in RGB (red, green, and blue) video format, Bayer format, and is used for troubleshooting and analyzing the video processing pipeline and display. The Bayer format generates video output in RAW format that is identical to a camera sensor output and hence used as a replacement for a camera sensor to test the video processing pipeline.

The test pattern IP generates the following eight different types of video test patterns.

- Color boxes pattern with 8 x 8 grid
- Only red
- Only green
- Only blue
- Horizontal eight color bars
- Vertical eight color bars
- Vertical graded bars from black to white
- Horizontal graded bars from black to white

Currently, vertical graded bars from black to white are configured in the 4-lane design.



Figure 1-9. Test Pattern Configuration

Configuration	
Horizontal Resolution	1920
Vertical Resolution	2160
Pixel Width	8 💌
Pixels per Clock	4 💌
Testbench	User 💌



2. Design Prerequisites (Ask a Question)

Before you begin, perform the following steps:

- Download the design files from AN5494: MIPI CSI-2 Transmitter.
- Download and install the Libero[®] SoC Design Suite from Libero SoC Software Downloads.

2.1 Libero License (Ask a Question)

The demo design supports Libero[®] version 2024.1 and above. To get silver license, see www.microchipdirect.com/fpga-software-products.



3. Setting Up the Hardware (Ask a Question)

Setting up the hardware involves verifying the jumper settings and interfacing the MIPI Transmit FMC (VIDEO-DC-MIPITX) card with the PolarFire Video kit, along with the MIPI cable. For more information, see https://www.microchip.com/en-us/development-tool/VIDEO-DC-MIPITX.



Figure 3-1. MIPI TX Daughter (FMC) Rev 1 Card—Front Side Image

Figure 3-2. MIPI TX Daughter (FMC) Rev 1 Card—Back Side Image



The following figure shows the hardware setup of the MIPI CSI-2 Transmitter with the PolarFire Video kit.



Figure 3-3. Setting up the Hardware



The following table lists the jumper and switch settings of PolarFire Video kit.

	Table	3-1.	Jumper	and	Switch	Settings	of P	olarFire	Video	Kit
--	-------	------	--------	-----	--------	----------	------	----------	-------	-----

Jumper and Switch	Position	Description
J15	Open	SPI Target and Initiator mode selection. By default, select SPI Initiator
J14	MIPI Transmit FMC	MIPI Transmit FMC to be connected
J17	Open	100K PD for TRSTn
J19	Pin 1 and 2	Default: XCVR_VREF is connected to ground
J28	Pin 1 and 2	Default: Programming through the FTDI
J6 - For PolarFire Video kit Rev-2 J24 - For PolarFire Video kit Rev-1	Pin 1 and 3	Default: VDDAUX4 voltage is set to 2.5V
J25	Pin 9 and 10	Bank4 voltage
J36	Pin 1 and 2	Default: Board power-up through the SW4
SW4	OFF or ON	Power On or Off slide switch
J20	12 Volts Input	12V input to the board
J12	USB-UART	USB-UART mini cable

To set up the hardware, perform the following steps:

- 1. Ensure that the following jumper settings are set on the video kit, as shown in the preceding table.
- 2. Connect the MIPI TX daughter card to **J14** of the FMC connector of the PolarFire Video kit, as shown in the preceding figure.
- 3. Connect the ribbon cable between the MIPI Transmit FMC card and the Raspberry Pi **J3** camera connector as shown in the Figure 4-1.



- 4. Connect the host PC and the video kit through **J12** of the video kit using the USB mini cable, as shown in the preceding figure.
- 5. Connect the 12V power supply cable to the **J20** on PolarFire Video kit DC jack, as shown in the preceding figure.
- 6. Power-up the board using the **SW4** slide switch.
- 7. After the power-up, program the PolarFire Video kit device. For more information, see Programming the PolarFire Device section.
- 8. The test pattern generator will start streaming once the PolarFire device is programmed. The Raspberry Pi SD Card Setup and Run section guides you through the steps required to display video data on the monitor using Raspberry Pi 4.

3.1 Programming the PolarFire Device (Ask a Question)

This section describes how to program the PolarFire Video Kit device with the .job file using FlashPro Express. The .job file mpf_an5494_v2024p1_jb to test on Raspberry Pi 4 Model B is provided in the Test Setup Prerequisites section.

To program the PolarFire device, perform the following steps:

- 1. On the host PC, start the FlashPro Express software from its installation directory.
- 2. To create a new job project on the **Project** menu, click **New** or **New Job Project from FlashPro Express Job**.
- 3. In the New Job Project from FlashPro Express Job dialog box, perform the following steps:
 - **Programming job file**: Click **Browse** and navigate to the location where the job file is located and select the file.
 - FlashPro Express job project location: Select Browse and navigate to the location where you
 want to save the project.
- 4. Click **OK**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears.
- 5. Verify that a programmer number appears in the **Programmer** box. If it does not, verify the board connections and click **Refresh/Rescan Programmers**.
- 6. To program the device, click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed.
- 7. To close FlashPro Express, click **Project** > **Exit**.



4. Test Setup: MIPI CSI-2 Transmitter as Camera and Raspberry Pi 4 Model B as MIPI CSI-2 Receiver (Ask a Question)

This section describes the test setup for the MIPI CSI-2 transmitter, which uses a 2-lane MIPI configuration to transfer video at 800 Mbps per lane. It transmits Full HD RAW8 video at 30 fps, with the Raspberry Pi 4 Model B as receiver.

Important: Connecting the MIPI output of this device to a GPU or Snapdragon platform will require the development of additional drivers to recognize the MIPI output as a camera source.

For more instructions on setting up the Raspberry Pi 4 Model B, see www.raspberrypi.com/ documentation/computers/getting-started.html.

4.1 Test Setup Requirements (Ask a Question)

PolarFire MIPI CSI-2 Transmitter design is demonstrated using a PolarFire Video kit, a MIPI Transmit FMC card, and a MIPI cable that is connected to a Raspberry Pi 4 Model B, which is capable of receiving and decoding MIPI CSI-2 Transmitter data as listed in the following table.

The following figure shows the setting up the hardware.

Figure 4-1. Setting up the Hardware—PolarFire Video Kit with Raspberry Pi 4 Model B



The following table lists the hardware and software required for running the demo.

|--|

Requirement	Description
Hardware and Accessories	
PolarFire [®] Video Kit	MPF300-VIDEO-KIT-NS
	Kit Contents:
	 PolarFire Video and Imaging board with MPF300T-1FCG1152E Device
	HDMI cable
	• 12V power pack/AC adapter
	USB 2.0 A male to mini-B
VIDEO-DC-MIPITX	MIPI Transmit FMC card



continued	
Requirement	Description
MIPI cable	MIPI 22 to 15 pin cable
Raspberry Pi	Raspberry Pi 4 model B
USB keyboard and USB mouse	USB keyboard and USB mouse as input devices for Raspberry Pi 4 Model B
5V power pack/AC adapter	Power adapter with type C cable that supports 5V/3A, or as per RPi's minimum requirements
SD Card	SD Card (16 GB or above), any class
Micro HDMI cable	To connect Raspberry Pi 4 Model B Micro HDMI (port 0 or port 1) to HDMI of monitor
HDMI monitor	1920 x 1080, 60 Hz resolution monitor for the HDMI 2.0 transmitter (Tx) port
Software	
Linux®	Ubuntu v20.4
Libero [®] SoC	FlashPro Express is installed with Libero SoC.



4.2 Test Setup Prerequisites (Ask a Question)

Before you begin, ensure to download the following files from AN5494: MIPI CSI-2 Transmitter:

- mpf_an5494_v2024p1_jb Job file to test on Raspberry Pi 4 Model B
- mipi_csi2_tx_using_rpi.zip Raspberry Pi 4 Model B image file

Important: This job file is designed to test the MIPI CSI-2 Transmitter with the Raspberry Pi 4 Model B. It is configured for a data rate of 800 Mbps per lane, supporting Full HD resolution at 30 FPS (1920 x 1080 at 30 FPS), and uses a 2-lane MIPI configuration.



4.3 Running the Demo (Ask a Question)

This section serves as a guide to help configure the Raspberry Pi 4 Model B to receive MIPI data when connected to the PolarFire Video kit, enabling real-time video streaming and analysis. It outlines the process of setting up image data streaming on a Raspberry Pi 4 Model B connected to a PolarFire Video kit through the MIPI Transmit FMC card.

- Demo Design: The demo showcases a Full HD (1920x1080 30 Hz) output using a display controller when the PolarFire Video kit is active.
- Data Generation: The demo simulates camera data by generating MIPI Tx pattern data, which is transmitted to the XCVR and mapped to the MIPI Transmit FMC card.
- Streaming Setup: This guide covers installing the Raspberry Pi OS on a Linux[®] system (Ubuntu) and provides commands to establish a live data stream on the Raspberry Pi 4 Model B.

4.3.1 Raspberry Pi 4 Model B SD Card Setup and Run (Ask a Question)

The following steps and associated commands are required to configure the Raspberry Pi 4 Model B to detect the PolarFire-based MIPI Tx as a camera source:

- Download and extract the mipi_csi2_tx_using_rpi.zip file to obtain the mipi_csi2_tx_using_rpi_v1.img file.
- 2. Download and install the Rpi-imager from the Raspberry Pi Website for the host system's operating system, which can be either Windows[®] or Linux.
- 3. Insert an SD card (at least 16 GB) into the host system, which can be either Windows or Linux running the Rpi-imager.
- 4. Run Rpi-imager and perform the following steps:
 - a. Click CHOOSE DEVICE option and then select Raspberry Pi 4 Model B.







Figure 4-3. Rpi-Imager—CHOOSE DEVICE

		Raspberry Pi Device	
	No filtering Show every possible image		
*	Raspberry Pi 5 The latest Raspberry Pi, Raspberry Pi 5		
	Raspberry Pi 4 Models B, 400, and Compute Modules 4, 4S	Ŀ	
	Raspberry Pi Zero 2 W The Raspberry Pi Zero 2 W		

b. Click **CHOOSE OS** under **Operating System** field and then select **Use custom** option. Navigate to and select the extracted Raspberry Pi image.

Figure 4-4. Rpi-Imager—CHOOSE OS

	Operating System	X
÷	Emulation and game OS Emulators for running retro-computing platforms	>
:0:	Other specific-purpose OS Home automation, 3D printing and specialised operating systems	>
:0]	Freemium and paid-for OS Freemium and paid-for digital signage, 3d printing and thin client operating systems	>
Z	Misc utility images Bootloader EEPROM configuration, etc.	>
Ō	Erase Format card as FAT32	
.img	Use custom Select a custom .img from your computer	

Figure 4-5. Select Rpi Image File



c. Click CHOOSE STORAGE under Storage field and select SD card that is inserted to the system.



Figure 4-6. Rpi-Imager—CHOOSE STORAGE



Important:

i.

After choosing Device, OS, and Storage, the **Rpi-imager** window appears as shown in the following figure. Click **NEXT** to proceed.

Figure 4-7. Rpi-Imager Window

Raspberry Pi					
Raspberry Pi Device	Operating System	Storage			
RASPBERRY PI 4	MIPI_CSI2_TX_USING_RPI_V1.IMG	GENERIC- MICRO SD USB DEVICE			

ii. If you receive a warning stating "All existing data on 'Generic– Micro SD USB Device' will be erased", as shown in the following figure, click **YES** to continue.

Figure 4-8. SD Card Warning



d. To start writing the image to the SD card, click **WRITE**. This process may take 15 to 20 minutes. Upon completion, the following window appears.



Figure 4-9. Rpi Image Write Successful



- 5. Insert the SD card into the SD card slot of the Raspberry Pi 4 Model B.
- 6. Connect a 5V power supply cable to the USB Type-C Power In socket of the Raspberry Pi 4 Model B.
- 7. Ensure that the jumper settings for the video kit are configured as specified in Table 3-1.
- 8. Connect the USB keyboard and USB mouse to the Raspberry Pi 4 Model B.
- 9. Power on the Raspberry Pi 4 Model B and the HDMI monitor.
- 10. Once the Raspberry Pi has finished booting, log in to the system.

This section provides the commands that need to be executed on a Raspberry Pi.

- 1. Open Ubuntu terminal and enter the following command.
 - uname -a

The output should be 6.1.20v71+, as shown in the following figure.

Figure 4-10. RPI Image

mipi@raspberrypi:~ \$ uname -a Linux raspberrypi 6.1.20-v7l+ #1 SMP Tue Mar 28 16:56:02 IST 2023 armv7l GNU/Linu

2. Execute the following V4L2 command to configure and wait for CSI data reception.

```
a. v412-ctl --device=/dev/video0 --set-fmt-
video=width=1920,height=1080,pixelformat=RGGB --stream-mmap --stream-
to=test.raw --stream-count=1.
```

Figure 4-11. How to Configure CSI Data Reception





Important: If the command gets stuck and does complete, it indicates that data reception is not functioning properly.

- b. Do not stop or terminate the command. While the command is running, restart the PolarFire device using the SW4 switch and verify if data is received. If data not received even after restarting the board at least 10 times, recheck the ribbon cable connection, ensure that every step is followed correctly.
- c. If the command returns with the "<" symbol, it indicates that data reception is successful.
- 3. Execute the following command to stream live data from the PolarFire Video kit board, with the output displayed on the monitor as shown in the Figure 4-13.



```
sudo ffplay -f video4linux2 -input format bayer rggb8 -i /dev/video0.
```

Figure 4-12. Data Stream



4.3.2 MIPI CSI-2 Transmitter Validation (Ask a Question)

Output Pattern 1:

The following figure shows the output pattern of the MIPI CSI-2 Transmitter with transceiver for a data rate of 800 Mbps/Lane for Full HD resolution at 30 FPS (1920 x 1080 at 30 FPS) and uses a 2 lane MIPI configuration is tested with the Raspberry Pi 4 model B.

Figure 4-13. Test Pattern—RPi



Output Pattern 2:

The following figure shows the output pattern of the MIPI CSI-2 Transmitter for 2.5 Gbps per lane with XCVR tested with the MIPI Introspect Analyzer (SV3C – DPRX 4-Lane D-PHY Analyzer).



Figure 4-14. Test Pattern—MIPI Analyzer

Terrence Ve Med Vo Vo Med Vo Med No Med No Med No Med Med	343	CSI Packets	LP States	LP Events F	rames							
Algon 0 0 Auxia NAV NO 0 2 211 17.40 Reachings 1.442.7 0 1 0.04 4.04 100 100 2.15 2.13 10.40 Reachings 1.442.7 0 1 0.04 4.04 100 100 2.15 2.13 Reachings 1.442.7 0 1 0.04 4.04 100 100 2.15 2.13 Reachings 1.562.7 1 0.04 4.04 100 100 2.12 2.69 Reachings 1.562.7 1 0.04 4.04 100 100 2.12 2.69 Reachings		Time (ms)	VC	Index	DT	DT Name	Image Width	Image Height	First Packet	Last Packet	FrameRate	
2201 0 1 0 0 4 0 0 100 100 100 100 100 100		0.30258	0	0	0x2A	RAW8	1920	1080	2	1081	126.26	Show Image
		8.22251	0	1	0x2A	RAW8	1920	1080	1082	2163	126.26	ShowImage
		10.14/44	0	2	0x2A	RAWS	1920	1080	2164	3245	120.20	Show Image
		24.06237	0	3	0x2A	RAWS RAWS	1920	1080	4228	4447	120.20	show image
	.0	0,0,eto.2A					I	I	I			

Important: The MIPI Analyzer capture shows 1920 x 1080 video at 126 FPS using one MIPI CSI-2 lane. At this rate, the four-lane connection supports 4K video at 60 FPS.

4.4 Running the Tcl Script—Reference Design with 4 Lane MIPI configuration (Ask a Question)

Tcl scripts are provided in the PolarFire Video Kit reference design with 4 lane MIPI configuration to transfer video at at 2.5 Gbps/lane, transmitting 4K RAW8 video at 120 fps.

To run Tcl, perform the following steps:

- 1. Launch the Libero software.
- 2. Click **Project** > **Execute Script**.
- 3. In the downloaded mpf an5494 v2024p1 df directory, select script.tcl.
- 4. Click Run.

After successful execution of the Tcl script, the Libero project is created within the top directory. For more information, see the Log file mpf an5494 v2024p1 df log.

For more details about the folder structure of mpf_an5494_v2024p1_df and Tcl scripts and commands, see the TCL_Scripts_readme.txt and Tcl Commands Reference Guide. Contact Technical Support for any queries about running the Tcl script.



5. Resource Utilization (Ask a Question)

The following table shows the resource utilization for a 4-lane reference design with MIPI configuration, which transfers video at 2.5 Gbps per lane and transmits 4K RAW8 videos at 120 fps.

Table 5-	-1. Resou	irce Utilizati	ion
			••••

Element	Usage in Numbers
DFFs	2806
LUTs	5469
LSRAMs	27
Math Blocks	1



6. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 6-1. Revision History

Revision	Date	Description
С	01/2025	 The following is the list of changes in revision C of the document: Updated to "Raspberry Pi 4 Model B" from "Raspberry Pi" throughout the document. Updated Figure 3-3 in the Setting Up the Hardware section. Updated Raspberry Pi 4 Model B SD Card Setup and Run section with Rpi-imager GUI figures.
Β	11/2024	 The following is the list of changes in revision B of the document: Updated Introduction section Updated Figure 1-1 and added Figure 1-2 in the Design Description section Updated Hardware Implementation as follows: Added Figure 1-4 and Figure 1-3 Updated all configuration GUI figures Added Figure 1-7 and note in the XCVR Configuration section Added Libero License section Added Figure 3-1, Figure 3-2, and updated Table 3-1 in the Setting Up the Hardware section Updated Running the Tcl Script—Reference Design with 4 Lane MIPI configuration section Updated the weblink of the image file and added steps related to rpi-manager in the Raspberry Pi 4 Model B SD Card Setup and Run section
А	09/2024	Initial release



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