24CS512

512-Kbit, 3.4 MHz I²C Serial EEPROM with 128-Bit Serial Number and Enhanced Software Write Protection

Features

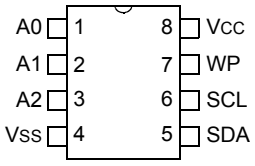
- 512-Kbit EEPROM:
  - Internally organized as one 65,536 x 8-bit block
  - Byte or page writes up to 128 bytes
  - Byte or sequential reads within a block
  - Self-timed write cycle (5 ms maximum)
- High-Speed I²C Interface:
  - High-Speed mode support for 3.4 MHz
  - Industry standard: 1 MHz, 400 kHz and 100 kHz
  - Output slope control to eliminate ground bounce
  - Schmitt Trigger inputs for noise suppression
- Security Register:
  - Preprogrammed 128-bit serial number
  - User-programmable, lockable 128-byte ID page
- Built-in Error Correction Code (ECC) Logic:
  - ECC Status bit via the Configuration register
- I²C Manufacturer Identification Function Support
- Versatile Data Protection Options:
  - Hardware Write-Protect (WP) pin for full array data protection
  - Enhanced software write protection via the Configuration register
- Operating Voltage Range of 1.7V to 5.5V
- Low-Power CMOS Technology:
  - Write current: 3.0 mA maximum at 5.5V
  - Read current: 1.0 mA maximum at 5.5V, 1 MHz
  - Standby current: 1 µA at 5.5V
- High Reliability:
  - More than one million erase/write cycles
  - Build-in ECC logic for increased reliability
  - Data retention: >200 years
  - ESD protection: >4000V
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C

Packages

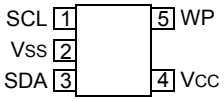
- 8-Lead MSOP, PDIP, SOIC, SOIJ, TSSOP, 8-Pad UDFN, 5-Lead SOT-23 and 8-Ball CSP

Package Types (not to scale)

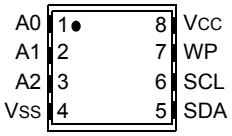
8-Lead MSOP/PDIP/SOIC/ SOIJ/TSSOP
(Top View)



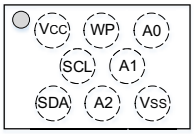
5-lead SOT-23
(Top View)



8-Pad UDFN
(Top View)



8-Ball CSP
(Top View)



Pin Function Table

Name	Function
A0	Device Address Input
A1	Device Address Input
A2	Device Address Input
VSS	Ground
SDA	Serial Data Pin
SCL	Serial Clock Input
WP	Write-Protect Pin
VCC	Supply Voltage

Description

The Microchip Technology Inc. 24CS512 provides 512 Kbits of Serial EEPROM, utilizing an I^2C (2-wire) serial interface with 3.4 MHz High-Speed mode capability. The device is organized as 65,536 bytes of 8 bits each (64-Kbyte), and is optimized for use in consumer and industrial applications where reliable and dependable nonvolatile memory storage is essential. The 24CS512 allows up to eight devices to share a common I^2C (2-wire) bus and is capable of operation across a broad voltage range (1.7V to 5.5V).

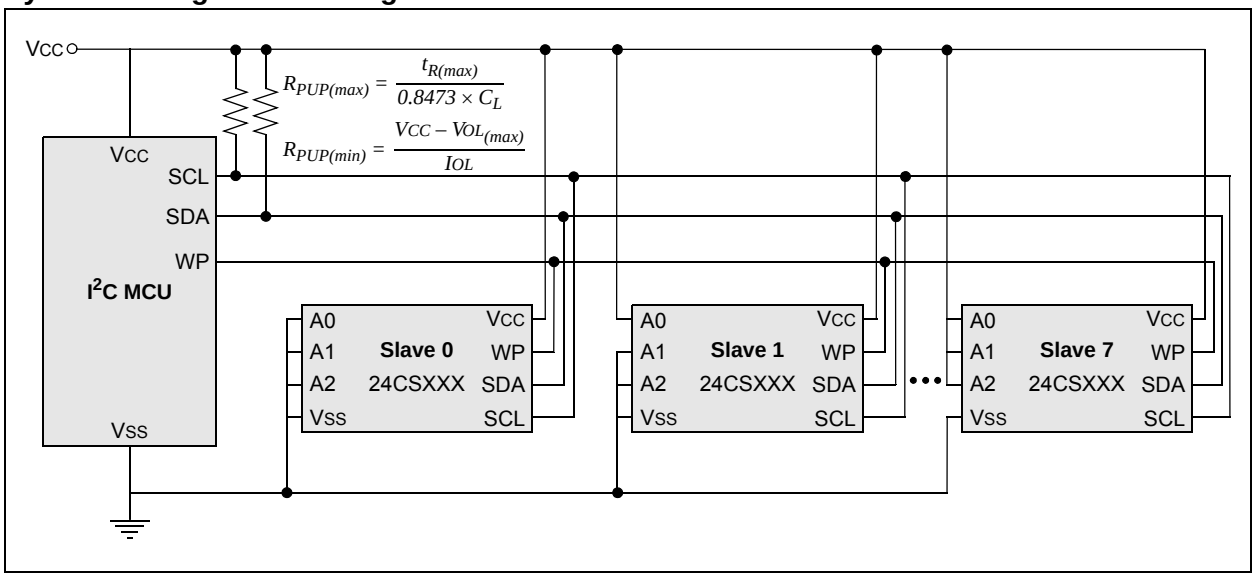
The 24CS512 features a 2-Kbit Security register, separate from the 512-Kbit memory array. The first half of the Security register is read-only and contains a factory-programmed, globally unique, 128-bit serial number in the first 16 bytes. The 128-bit serial number is unique across the entire CS series of Serial EEPROM products, and eliminates the time-consuming step of performing and ensuring serialization of a product on a manufacturing line. The 128-bit read-only serial number is followed by an additional 1 Kbit (128 bytes) of user-programmable EEPROM. The user-programmable section of the Security register can later be permanently write-protected via a software sequence.

The device also contains a Configuration register, which allows the write protection behavior to be configured for legacy hardware write protection or enhanced software write protection which allows the user to protect any of the eight independent 64-Kbit zones. Once the desired configuration is set, the Configuration register can be permanently locked, thereby preventing any further changes to the device operation.

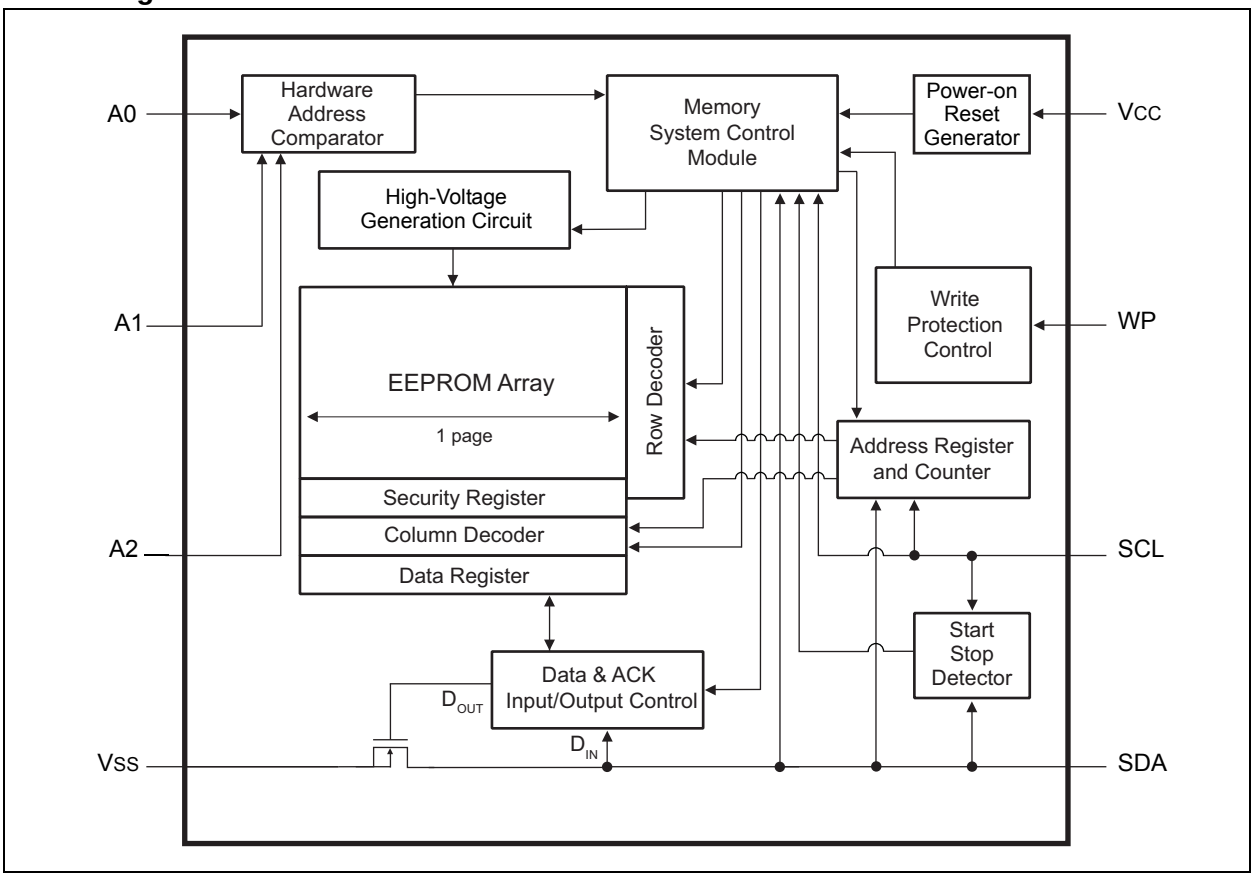
For added reliability, the 24CS512 utilizes a built-in Error Correction Code (ECC) scheme. This scheme can correct up to one incorrectly read bit within a four-byte read out. Additionally, the Configuration register includes a read-only ECC State bit (ECS) that is set when ECC is invoked.

The 24CS512 supports the I^2C Manufacturer Identification (ID) command which will return a unique value for the 24CS512, allowing easy identification within the application.

System Configuration Using Serial EEPROMs



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to 6.5V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +125°C

ESD protection on all pins.....>4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = 1.7V to 5.5V TA = -40°C to +85°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D1	VIH	High-Level Input Voltage	VCC x 0.7	VCC + 1	V	
D2	VIL	Low-Level Input Voltage	-0.6	VCC x 0.3	V	
D3	VOL	Low-Level Output Voltage	—	0.4	V	IOL = 2.1 mA, VCC ≥ 2.5V
			—	0.2	V	IOL = 0.15 mA, VCC < 2.5V
D4	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	VCC x 0.05	—	V	VCC ≥ 2.5V **(Note 1)**
D5	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC, WP = VSS
			—	±1	µA	VIN = VSS or VCC, WP = VCC
D6	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D7	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TAMB = +25°C, FCLK = 1 MHz, VCC = 5.5V **(Note 1)**
D8	ICCREAD	Operating Current	—	1	mA	VCC = 5.5V, FCLK = 1 MHz
D9	ICCWRITE	Operating Current	—	3	mA	VCC = 5.5V
			—	1	mA	VCC = 1.7V
D10	ICCS	Standby Current	—	1	µA	SCL = SDA = VCC = 5.5V, WP = VSS

Note 1: This parameter is not tested but ensured by characterization.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = 1.7V to 5.5V TA = -40°C to +85°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	1000	kHz	1.7V ≤ VCC ≤ 5.5V
			—	3400	kHz	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
2	THIGH	Clock High Time	400	—	ns	1.7V ≤ VCC ≤ 5.5V
			60	—	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
3	TLOW	Clock Low Time	400	—	ns	1.7V ≤ VCC ≤ 5.5V
			160	—	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
4	TR	SDA and SCL Rise Time	—	1000	ns	1.7V ≤ VCC ≤ 5.5V **(Note 1)**
5	TF	SDA and SCL Fall Time	—	300	ns	1.7V ≤ VCC ≤ 5.5V **(Note 1)**
6	THD:STA	Start Condition Hold Time	250	—	ns	1.7V ≤ VCC ≤ 5.5V
			160	—	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
7	TSU:STA	Start Condition Setup Time	250	—	ns	1.7V ≤ VCC ≤ 5.5V
			160	—	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
8	THD:DAT	Data Input Hold Time	0	—	ns	**(Note 2)**
9	TSU:DAT	Data Input Setup Time	50	—	ns	1.7V ≤ VCC ≤ 5.5V
			10	—	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
10	TSU:STO	Stop Condition Setup Time	250	—	ns	1.7V ≤ VCC ≤ 5.5V
			160	—	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
11	TSU:WP	WP Setup Time	600	—	ns	
12	THD:WP	WP Hold Time	1300	—	ns	
13	TAA	Output Valid from Clock	—	400	ns	1.7V ≤ VCC ≤ 5.5V
			—	70	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled
14	TBUF	Bus Free Time: Bus Time must be Free before a New Transmission can Start	500	—	ns	1.7V ≤ VCC ≤ 5.5V
15	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	1.7V ≤ VCC ≤ 5.5V **(Note 3)**
			—	10	ns	2.5V ≤ VCC ≤ 5.5V, HS Mode Enabled **(Note 3)**
16	TWC	Write Cycle Time (byte or page)	—	5	ms	

Note 1: The rise/fall times must be less than the specified maximums in order to achieve the maximum clock frequencies specified for FCLK. Please refer to the I^2C specification for applicable timings.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: Not 100% tested. CB = total capacitance of one bus line in pF.

FIGURE 1-1: BUS TIMING DATA

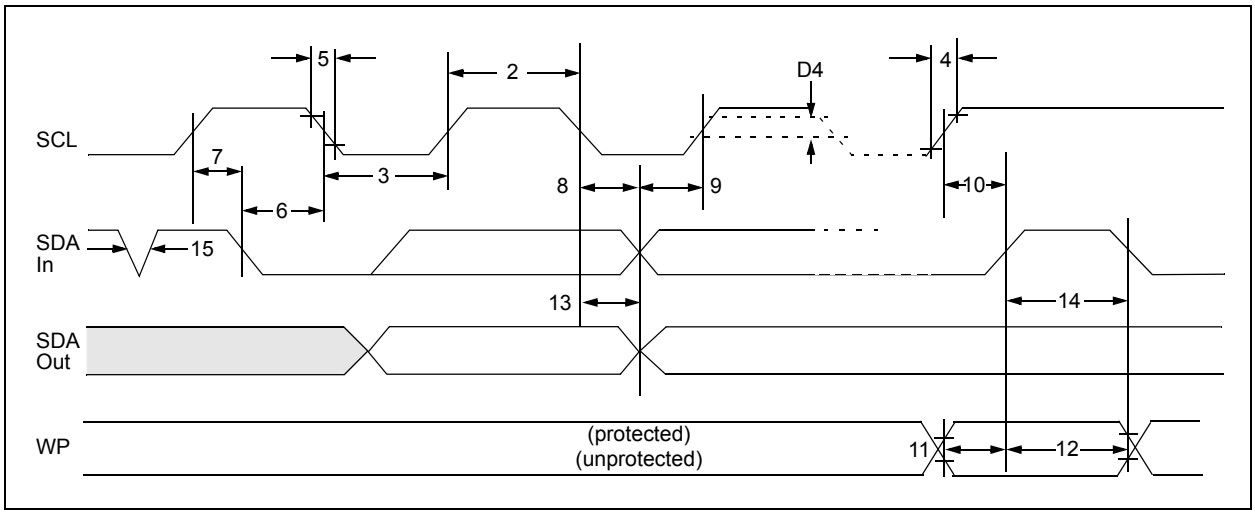


TABLE 1-3: EEPROM CELL PERFORMANCE CHARACTERISTICS

Operation	Test Condition	Min.	Max.	Units
Write Endurance(1)(2)	T_A = 25°C, 1.7V ≤ V_{CC} ≤ 5.5V	1,000,000	—	Write Cycles
Data Retention(1)	T_A = 55°C	200	—	Years

Note 1: Performance is determined through characterization and the qualification process.

2: Due to the memory array architecture, the write cycle endurance is specified for write operations in groups of four data bytes. The beginning of any 4-byte boundaries can be determined by multiplying any integer (N) by four (i.e., 4*N). The end address can be found by adding three to the beginning value (i.e., 4*N+3). See Section 6.3, Internal Writing Methodology for more details on this implementation.

1.1 Power-up Requirements and Reset Behavior

During a power-up sequence, the VCC supplied to the 24CS512 should monotonically rise from VSS to the minimum VCC level, as specified in Table 1-1, with a slew rate no faster than 0.1 V/µs.

1.1.1 DEVICE RESET

To prevent write operations or other spurious events from happening during a power-up sequence, the 24CS512 includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the VCC level crosses the internal voltage threshold (VPOR) that brings the device out of Reset and into Standby mode.

The system designer must ensure that instructions are not sent to the device until the VCC supply has reached a stable value, greater than or equal to the minimum VCC level. Additionally, once the VCC is greater than or equal to the minimum VCC level, the master must wait at least TPUP before sending the first command to the device. See Table 1-4 for the values associated with these power-up parameters.

If an event occurs in the system where the VCC level supplied to the 24CS512 drops below the maximum VPOR level specified, it is recommended that a full-power cycle sequence be performed by first driving the VCC pin to VSS, waiting at least the minimum TPOFF time and then perform a new power-up sequence in compliance with the requirements defined in **Section 1.1 "Power-up Requirements and Reset Behavior"**.

TABLE 1-4: POWER-UP CONDITIONS

Symbol	Parameter	Min.	Max.	Units
TPUP	Time Required after VCC is Stable before the Device can Accept Commands	100	—	µs
VPOR	Power-on Reset Threshold Voltage	—	1.5	V
TPOFF	Minimum Time at VCC = 0V between Power Cycles	1	—	ms

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-Lead MSOP	8-Lead PDIP	8-Lead SOIC	8-Lead SOIJ	8-Lead TSSOP	5-Lead SOT-23	8-Lead UDFN(1)	8-Ball CSP	Function
A0	1	1	1	1	1	—	1	1	Device Address Input
A1	2	2	2	2	2	—	2	2	Device Address Input
A2	3	3	3	3	3	—	3	3	Device Address Input
VSS	4	4	4	4	4	2	4	4	Ground
SDA	5	5	5	5	5	3	5	5	Serial Data
SCL	6	6	6	6	6	1	6	6	Serial Clock
WP	7	7	7	7	7	5	7	7	Write-Protect Pin
VCC	8	8	8	8	8	4	8	8	Device Power Supply

Note 1: The exposed pad on this package can be connected to VSS or left floating.

2.1 A0, A1 and A2 Device Address Inputs

The A0, A1 and A2 inputs are used by the 24CS512 for multiple device operations. The logic levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different hardware slave address bit combinations. These inputs must be connected to either VCC or VSS.

In most applications, the device address inputs, A0, A1 and A2, are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable logic device, the device address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

2.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal; therefore, the SDA bus requires a pull-up resistor to VCC (typically 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz and 330Ω for 3.4 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

2.4 Write-Protect (WP)

This pin must be connected to either VSS or VCC. If tied to VSS, write operations to the memory array and Security register are enabled. If tied to VCC, write operations to the memory array and Security register are inhibited, but read operations are not affected.

Note:	This pin is ignored when using Enhanced Software Write Protection mode and should be tied to either VCC or VSS.

3.0 MEMORY ORGANIZATION

3.1 EEPROM Organization

The 24CS512 is internally organized as 512 pages of 128 bytes each.

3.2 Device Registers

The 24CS512 contains three types of registers that modulate device operation and/or report on the current status of the device. These registers are:

- Configuration register
- Security register
- Manufacturer ID register

3.2.1 CONFIGURATION REGISTER

The Configuration register allows for modification of the device write protection behavior, as well as additional device features. Once the device behavior is set as desired, the Configuration register can be permanently locked (or set to read-only), thereby preventing any subsequent changes. Refer to **Section 9.0 "Configuration Register"** for additional information on the Configuration register.

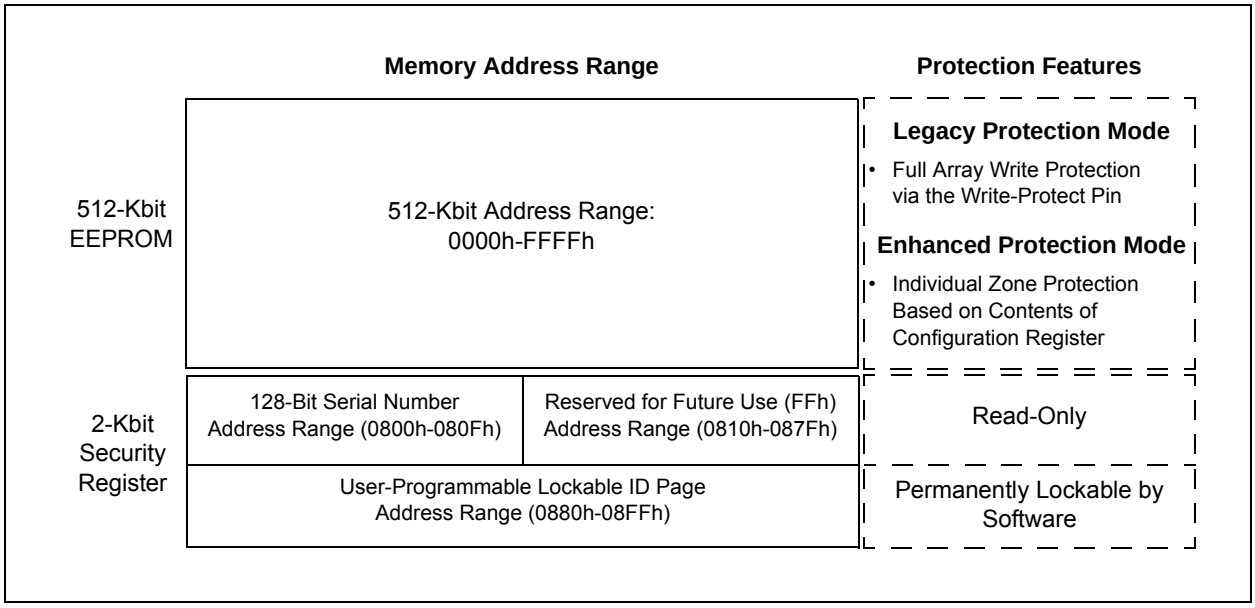
3.2.2 SECURITY REGISTER

The Security register is split into a read-only section and a user-programmable lockable, identification page section. The read-only section contains a preprogrammed, globally unique, 128-bit serial number. The user-programmable (lockable ID page) section of the Security register is ideal for applications that need to irreversibly protect critical or sensitive application data from ever being altered. For more details about the Security register, refer to **Section 10.0 "Security Register"**.

3.2.3 MANUFACTURER ID REGISTER

The Manufacturer ID register is a read-only 24-bit register that contains data in compliance with the I^2C Manufacturer ID sequence. The 24-bit value returned is unique to the 24CS512. Refer to **Section 10.0 "Security Register"** for more details.

FIGURE 3-1: MEMORY ORGANIZATION



3.3 Device Addressing

Communication with the 24CS512 begins with an 8-bit device address byte, comprised of a 7-bit slave address and a Read/Write Select (R/$\overline{W}$) bit. Since multiple slave devices can reside on the serial bus, each slave device must have its own unique address so that the master can access each device independently.

The 7-bit slave address can be constructed in two ways. Most communications utilize a 4-bit device type identifier, followed by a 3-bit hardware slave address. Additionally, the 24CS512 can accept a reserved 7-bit master code, which is then followed by a device type identifier and hardware slave address. This 7-bit master code enables access to different modes of operation within the device.

TABLE 3-1: DEVICE ADDRESS BYTE STRUCTURE

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4-Bit Device Type Identifier				3-Bit Hardware Slave Address			Read/Write Select
7-Bit Reserved Master Code							

The 24CS512 will respond to only specific device type identifiers, as shown in **Section 3.3.1 "Valid Device Address Byte Inputs"**.

The 3-bit hardware slave address is comprised of bits A2, A1 and A0. These bits can be used to expand the address space by allowing up to eight devices with the same device type identifiers on the bus. These hardware slave address bits must correlate with the logic level on the corresponding hardwired device address input pins, A2, A1 and A0.

The device will respond to all valid device address byte combinations that it receives, except for cases where the master code sequence specifically calls for no response.

3.3.1 VALID DEVICE ADDRESS BYTE INPUTS

The 24CS512 will respond to two different device type identifiers, as well as two reserved master codes as shown in Table 3-2.

TABLE 3-2: TABLE OF VALID DEVICE ADDRESS BYTES

Access Region	Device Address Byte Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512-Kbit EEPROM(1)	Device Type Identifier + Hardware Address	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Security Register(1,2)		1	0	1	1	A2	A1	A0	R/$\overline{W}$
Configuration Register(1,2)		1	0	1	1	A2	A1	A0	R/$\overline{W}$
Manufacturer Identification(3)	Reserved Master Code	1	1	1	1	1	0	0	R/$\overline{W}$
High-Speed (HS) Mode(4)		0	0	0	0	1	X	X	X

Note 1: The hardware slave address bits must be set to logic '0' when using the SOT-23 package.

2: Accessing the Security or Configuration register is only possible if any sequence or command to the main EEPROM (if one has been sent) has been properly terminated with a Stop condition. Without proper termination of the previous sequence, all communications with the Security or Configuration registers will not execute successfully.

3: See **Section 11.0 "Manufacturer Identification Register"** for details.

4: See **Section 8.0 "High-Speed Mode"** for details.

3.3.1.1 Read/Write Operation Select Bit

The eighth bit (bit 0) of the device address byte is the Read/Write Select (R/$\overline{W}$) bit. A read operation is initiated if this bit is a logic '1' and a write operation is initiated if this bit is a logic '0'.

Upon the successful comparison of the device address byte, the 24CS512 will respond. If a valid comparison is not made, the device will not respond and will return to a standby state.

3.3.2 WORD ADDRESS BYTES

Two 8-bit word address bytes are transmitted to the device immediately following the device address byte.

The first word address byte contains the eight Most Significant bits (MSbs) of the 16-bit memory array word address to specify which location in the EEPROM to start reading or writing. When accessing the Security register, it is required that the A15 bit of the first word address be set to a logic '0', and the A11 and A10 bits be set to '10b', respectively. When accessing the Configuration register, it is required that the A15 bit of the first word address be set to a logic '1', and the A11 and A10 bits be set to '10b', respectively. Refer to Table 3-3 for details.

Next, the second word address byte is sent to the device, which provides the remaining eight bits of the word address (A7 through A0). Refer to Table 3-4 for details.

TABLE 3-3: FIRST WORD ADDRESS BYTE

Memory Region	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512-Kbit EEPROM	A15	A14	A13	A12	A11	A10	A9	A8
Security Register Read/Write	0	x	x	x	1	0	x	x
Lock Security Register	x	x	x	x	0	1	1	0
Configuration Register	1	x	x	x	1	0	x	x

TABLE 3-4: SECOND WORD ADDRESS BYTE

Memory Region	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512-Kbit EEPROM	A7	A6	A5	A4	A3	A2	A1	A0
Security Register Read/Write	A7	A6	A5	A4	A3	A2	A1	A0
Lock Security Register(1)	x	x	x	x	x	x	x	x
Configuration Register(1)	x	x	x	x	x	x	x	x

Note 1: When accessing the Configuration register or locking the Security registers, the second word address byte must be transmitted to the device, despite containing only don't care values.

4.0 FUNCTIONAL DESCRIPTION

The 24CS512 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24CS512 works as a slave. Both master and slave can operate as a transmitter or receiver, but the master determines which mode is activated.

5.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line, while the clock line is high, will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 5-1).

5.1 Bus Not Busy (A)

Both data and clock lines remain high.

5.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

5.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

5.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

5.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge (ACK) signal after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit. See Figure 5-2 for Acknowledge timing.

Note:	The 24CS512 does not generate any Acknowledge bits if an internal programming cycle is in progress.

A device that Acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During read operations, the master must signal an end of data to the slave by NOT generating an Acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the slave (24CS512) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 5-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

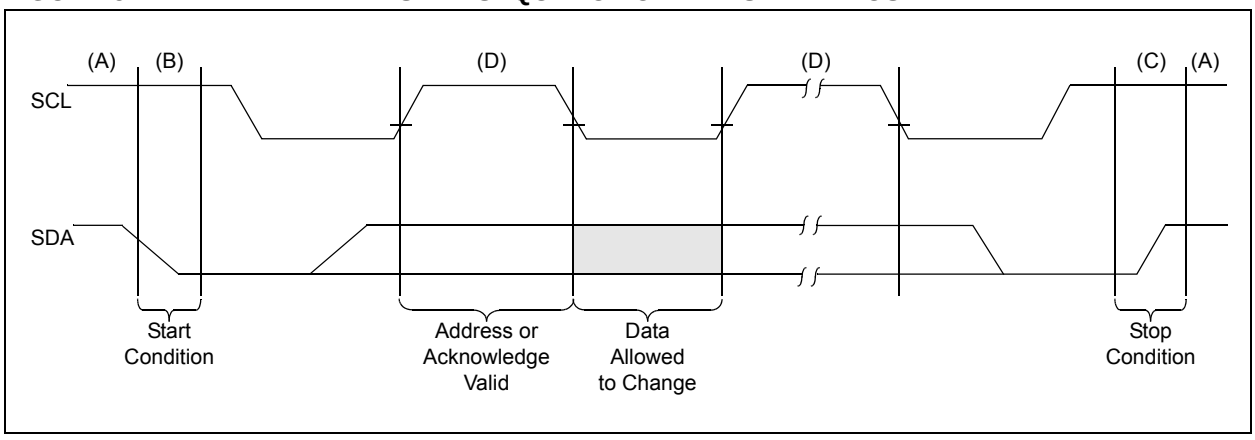
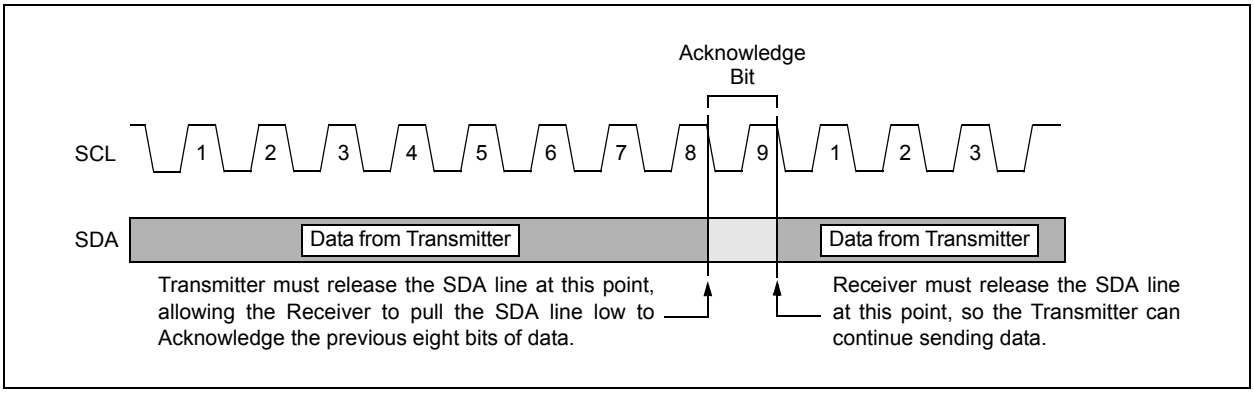


FIGURE 5-2: ACKNOWLEDGE TIMING



5.6 Standby Mode

The 24CS512 features a low-power Standby mode, which is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see **Section 1.1 "Power-up Requirements and Reset Behavior"**).
- A Stop condition is received by the device unless it initiates an internal write cycle (see **Section 6.0 "Write Operations"**).
- At the completion of an internal write cycle (see **Section 6.0 "Write Operations"**).
- An unsuccessful match of the device type identifier or hardware slave address in the device address byte occurs (see **Section 3.3 "Device Addressing"**).
- The master does not Acknowledge the receipt of a data read out from the device; instead, it sends a NACK response (see **Section 7.0 "Read Operations"**).

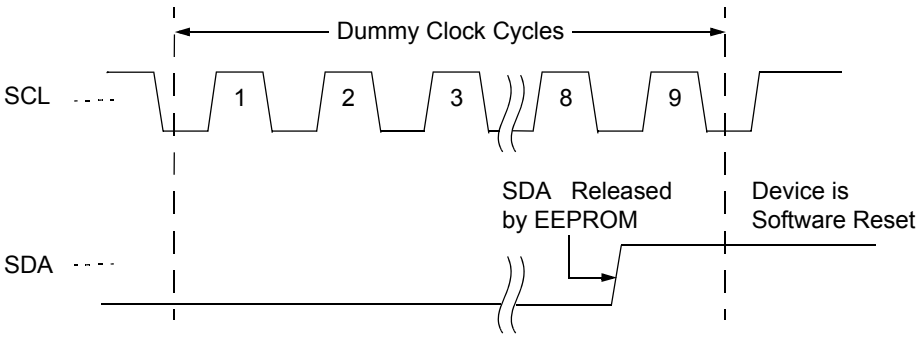
5.7 Software Reset

After an interruption in protocol, power loss or system reset, any 2-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The Software Reset sequence should not take more than nine dummy clock cycles. Note that the Software Reset sequence will not interrupt the internal write cycle and only resets the I^2C interface.

Once the Software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition, followed by the protocol. Figure 5-3 illustrates the Software Reset sequence.

In the event that the device is still non-responsive, or remains active on the SDA bus, a power cycle must be used to reset the device (see **Section 1.1.1 "Device Reset"**).

FIGURE 5-3: SOFTWARE RESET



6.0 WRITE OPERATIONS

All write operations for the 24CS512 begin with the master sending a Start condition, followed by a device address byte with the R/$\overline{W}$ bit set to a logic '0', and then by the word address bytes. The data value(s) to be written to the device immediately follow the word address bytes.

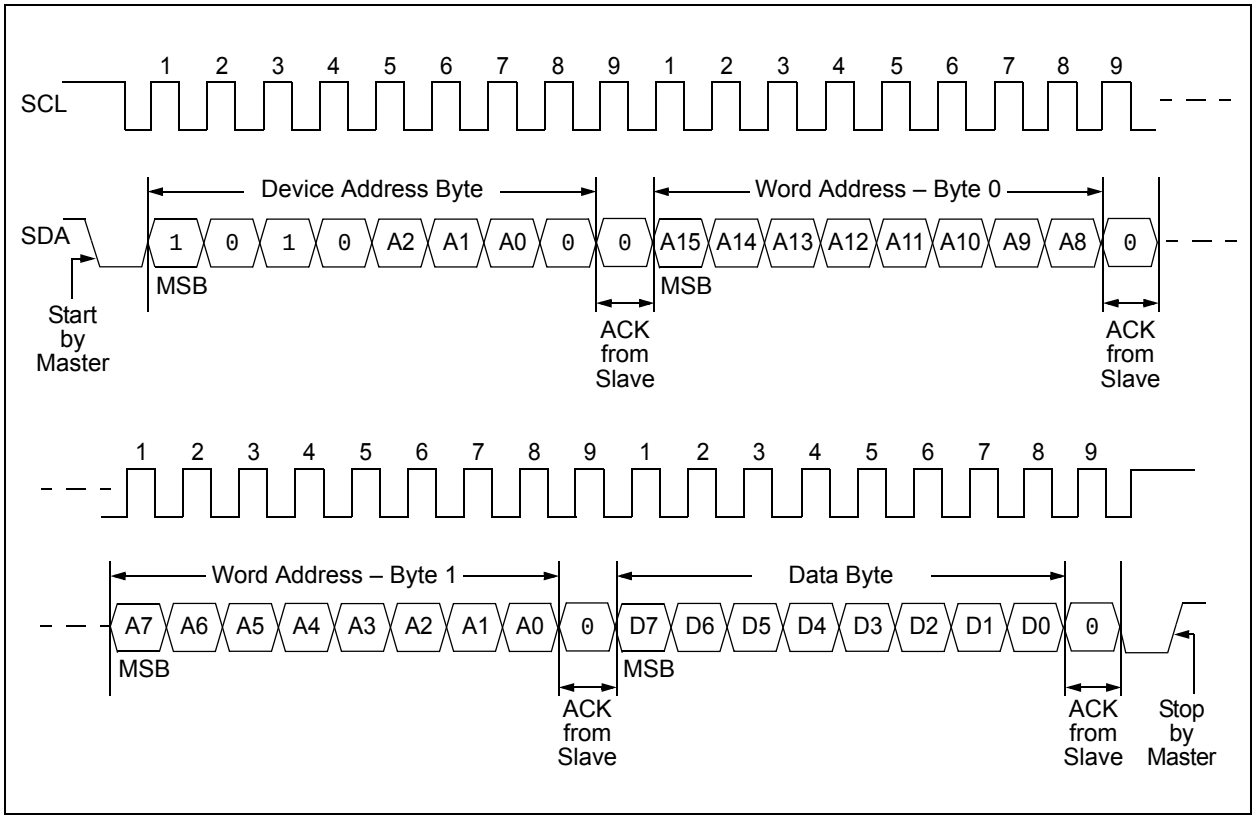
6.1 Byte Write

The 24CS512 supports the writing of a single 8-bit byte. Selecting a data byte in the 24CS512 requires a 16-bit word address.

Upon receipt of the proper device address and word address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the first 8-bit data byte. Following the receipt of the data byte, the EEPROM will respond with an Acknowledge. The addressing device, such as a master, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within TWC, while the data byte is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle and the EEPROM will not respond until the write operation is complete.

If an attempt is made to write to a write-protected portion of the array, no data will be written and the device will immediately accept a new command.

FIGURE 6-1: BYTE WRITE



6.2 Page Write

A page write operation allows up to 128 bytes to be written in the same write cycle, provided all bytes are in the same page of the memory array (where address bits A15 through A7 are the same). Partial page writes of less than 128 bytes are also allowed.

A page write is initiated the same way as a byte write, but the master does not send a Stop condition after the first data byte is clocked in.

Instead, after the EEPROM Acknowledges receipt of the first data byte, the master can transmit up to 127 additional data bytes. The EEPROM will respond with an ACK after each data byte is received.

Once all data to be written has been sent to the device, the master must issue a Stop condition (see Figure 6-2). Once the Stop condition is received, an internal write cycle will begin.

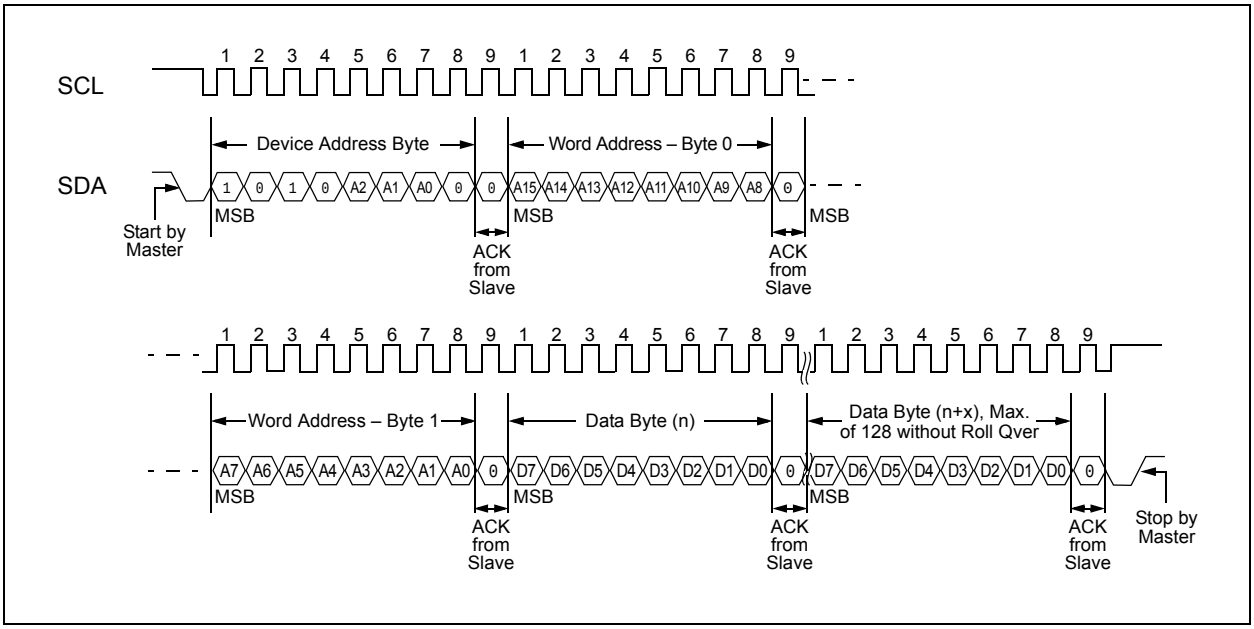
If an attempt is made to write to a write-protected portion of the array, no data will be written and the device will immediately accept a new command.

The lower seven bits of the word address are internally incremented following the receipt of each data byte. The higher order address bits are not incremented and retain the memory page location.

When the incremented word address reaches the page boundary, the address counter will roll over to the beginning of the same page.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at the addresses that are integer multiples of [page size – 1]. If a page write operation attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 6-2: PAGE WRITE



6.3 Internal Writing Methodology

The 24CS512 incorporates a built-in Error Correction Code (ECC) logic scheme. The EEPROM array is internally organized as a group of four connected 8-bit bytes, plus an additional six ECC (Error Correction Code) bits of EEPROM. These 38 bits are referred to as the internal physical data word. During a read operation, the ECC logic compares each 4-byte physical data word with its corresponding six ECC bits. If a single bit out of the 4-byte region reads incorrectly, the ECC logic will detect the bad bit and replace it with the correct value before the data is serially clocked out. This architecture significantly improves the reliability of the 24CS512 compared to an implementation that does not utilize ECC.

It is important to note that data is always physically written to the part at the internal physical data word level, regardless of the number of bytes written. Writing single bytes is still possible with the byte write operation, but internally, the other three bytes within that 4-byte location where the single byte was written, along with the six ECC bits, will be updated. Due to this architecture, the write endurance is rated at the internal physical data word level (4-byte word).

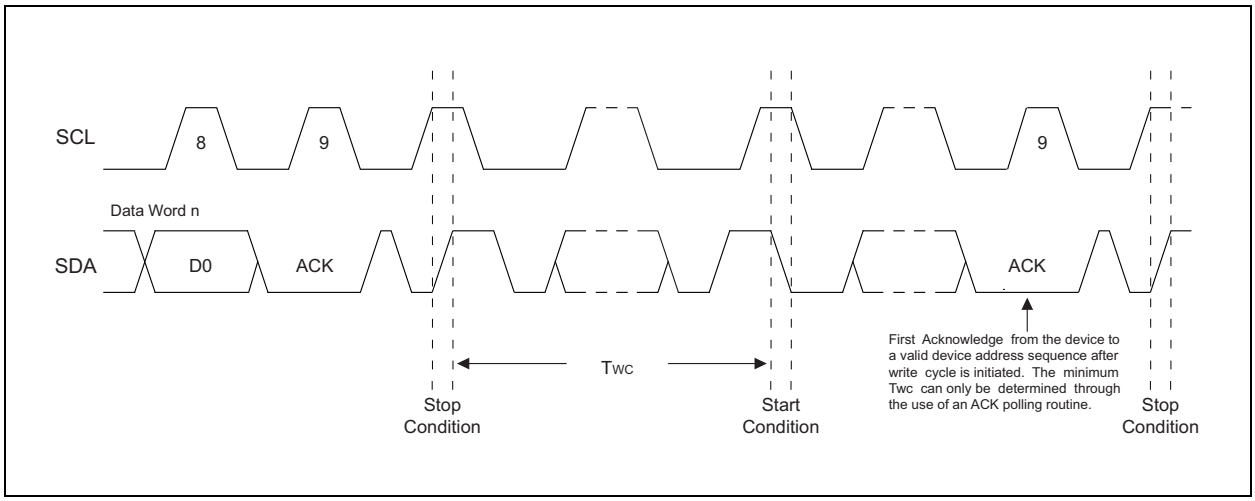
The system designer needs to optimize the application writing algorithms to observe these internal word boundaries in order to reach the write cycle endurance rating.

6.4 Write Cycle Timing

The length of the self-timed write cycle, or TWC, is defined as the amount of time from the Stop condition, that begins the internal write operation, to the Start condition of the first device address byte sent to the 24CS512 that it subsequently responds to with an ACK (see Figure 6-3).

During the internally self-timed write cycle, any attempts to access the device will be ignored.

FIGURE 6-3: WRITE CYCLE TIMING

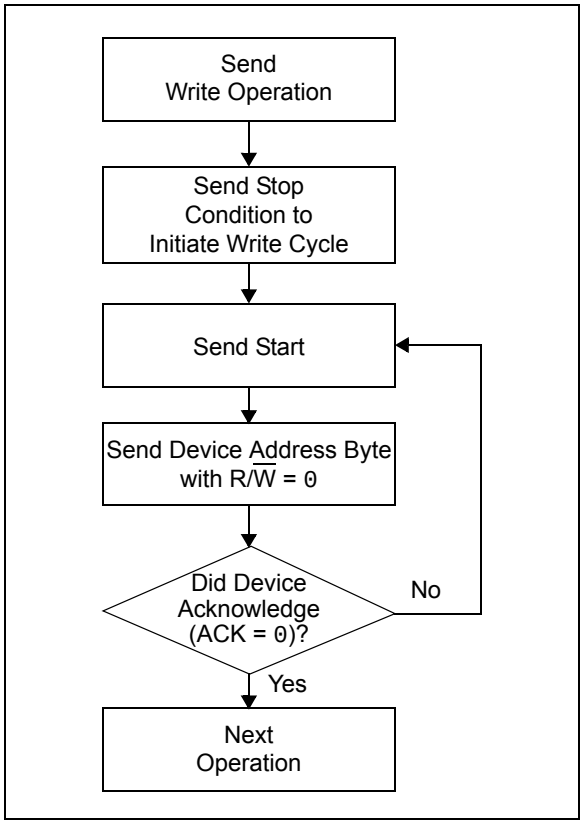


6.5 Acknowledge Polling

Since the device will not Acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write operation has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the device address byte for a write operation (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then a NACK will be returned. If a NACK is returned, then the Start bit and device address byte must be resent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write operation. See Figure 6-4 for flow diagram.

Note:	Polling, while operating in High-Speed mode, is not supported on the 24CS512. Therefore, polling must occur while using Fast mode plus (1 MHz) or slower clock frequencies.

FIGURE 6-4: ACKNOWLEDGE POLLING FLOW



6.6 Write Protection

The 24CS512 can be set in two different Write Protection modes. The selection between the two modes is controlled by the Configuration register EWPM bit. When this bit is a logic '0', the device is set in Legacy Hardware Write Protection mode and when the bit is a logic '1', the device is set for Enhanced Software Write Protection mode.

6.6.1 LEGACY HARDWARE WRITE PROTECTION MODE

When the EWPM bit is set to logic '0', the 24CS512 utilizes a legacy hardware data protection scheme that allows the user to write-protect the entire memory contents when the WP pin is asserted (high). No write protection will be set if the WP pin is deasserted (low).

Note:	Writing to the Security register can be inhibited by asserting the Write-Protect pin. Writing to the Configuration register cannot be inhibited by asserting the Write-Protect pin.

TABLE 6-1: LEGACY HARDWARE WRITE PROTECTION BEHAVIOR

WP Pin	Protected Address Range
1 (high)	Full Array (0000h-FFFFh)
0 (low)	None

6.6.1.1 Write-Protect Pin Timing

The status of the WP pin is sampled at the Stop condition for every byte write or page write operation, prior to the start of an internally self-timed write operation (see Figure 1-1). Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle.

If an attempt is made to write to the device while the WP pin has been asserted, the device will Acknowledge the device address, word address and data bytes, but no write cycle will occur when the Stop condition is issued, and the device will immediately be ready to accept a new read or write operation.

6.6.2 ENHANCED SOFTWARE WRITE PROTECTION MODE

When the EWPM bit is set to logic '1', the 24CS512 is configured for a versatile software write protection scheme by segmenting the EEPROM array into eight independent 64-Kbit zones (see Table 6-2). Each of the eight zones can be write-protected by programming the corresponding bit in the Configuration register. The protection behavior can be made permanent by locking the Configuration register (see **Section 9.5 "Locking the Configuration Register"** for additional details).

Note:	Enhanced software write protection does not affect write operations to the Security and Configuration registers.

TABLE 6-2: 24CS512 ZONE PROTECTION CONTROL

Configuration Register Bit	Protected Zone	Protected Address Range
SWP7	7	E000h-FFFFh
SWP6	6	C000h-DFFFh
SWP5	5	A000h-BFFFh
SWP4	4	8000H-9FFFh
SWP3	3	6000h-7FFFh
SWP2	2	4000h-5FFFh
SWP1	1	2000h-3FFFh
SWP0	0	0000h-1FFFh

7.0 READ OPERATIONS

Read operations are initiated the same way as write operations, with the exception that the Read/Write Select (R/$\overline{W}$) bit in the device address byte must be a logic ‘1’. There are three read operations:

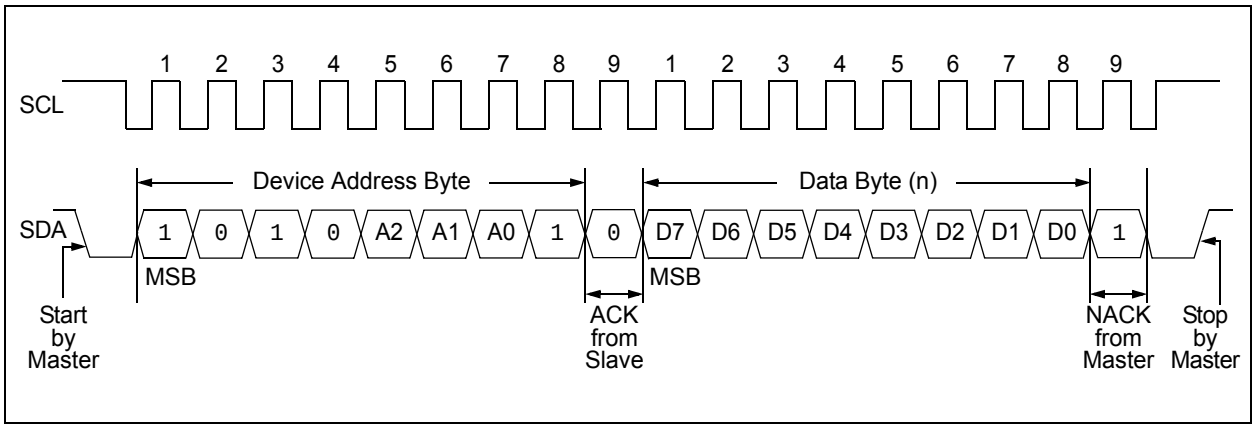
- Current Address Read
- Random Address Read
- Sequential Read

7.1 Current Address Read

The 24CS512 contains an internal Address Pointer that maintains the word address of the last byte accessed, internally incremented by one. Therefore, if the previous read access was to address ‘n’ (n is any legal address), the next current address read operation would access data from address n+1.

A current address read operation will output data according to the location of the internal Address Pointer. This is initiated with a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic ‘1’. The device will ACK this sequence and the current address data byte is serially clocked out on the SDA line. All types of read operations will be terminated if the master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into Standby mode. After the NACK response, the master may send a Stop condition to complete the protocol or it can send a Start condition to begin the next sequence.

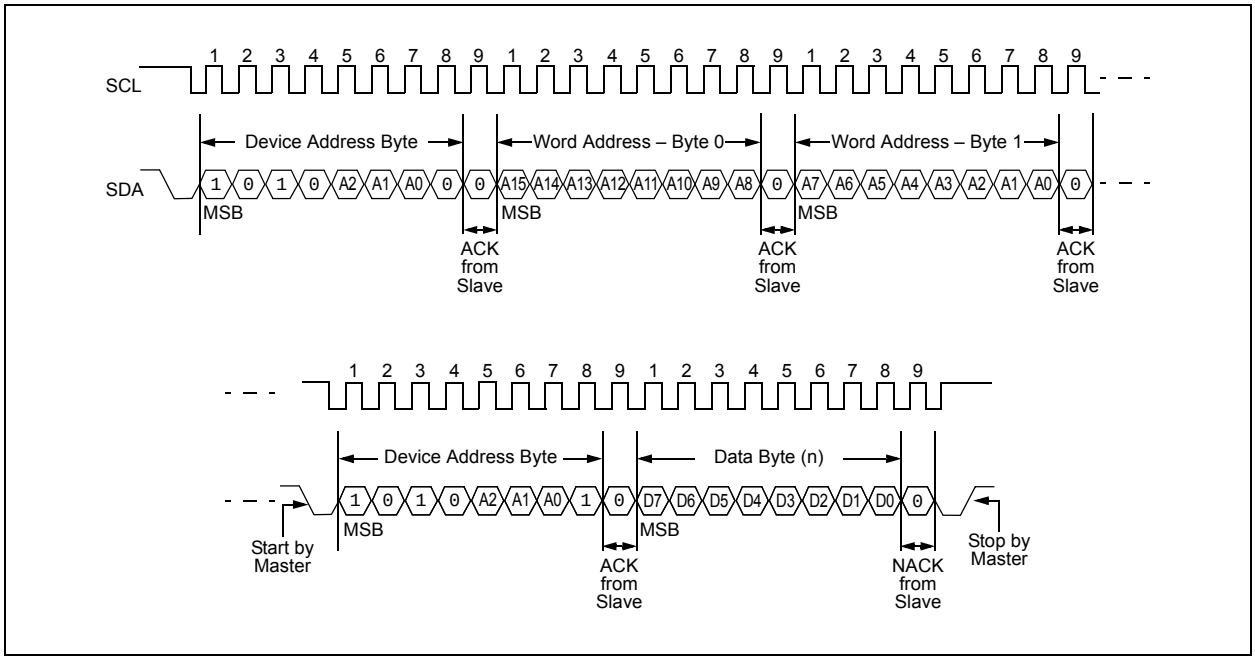
FIGURE 7-1: CURRENT ADDRESS READ



7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24CS512 as part of a write operation (R/$\overline{W}$ bit set to '0'). After the word address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the device address byte again but with the R/$\overline{W}$ bit set to a logic '1'. The 24CS512 will then issue an Acknowledge and transmit the 8-bit data byte. The master will not Acknowledge the transfer, but does generate a Stop condition which causes the 24CS512 to discontinue transmission (Figure 7-2). After a random read operation, the internal Address Pointer will point to the last word address location incremented by one.

FIGURE 7-2: RANDOM READ

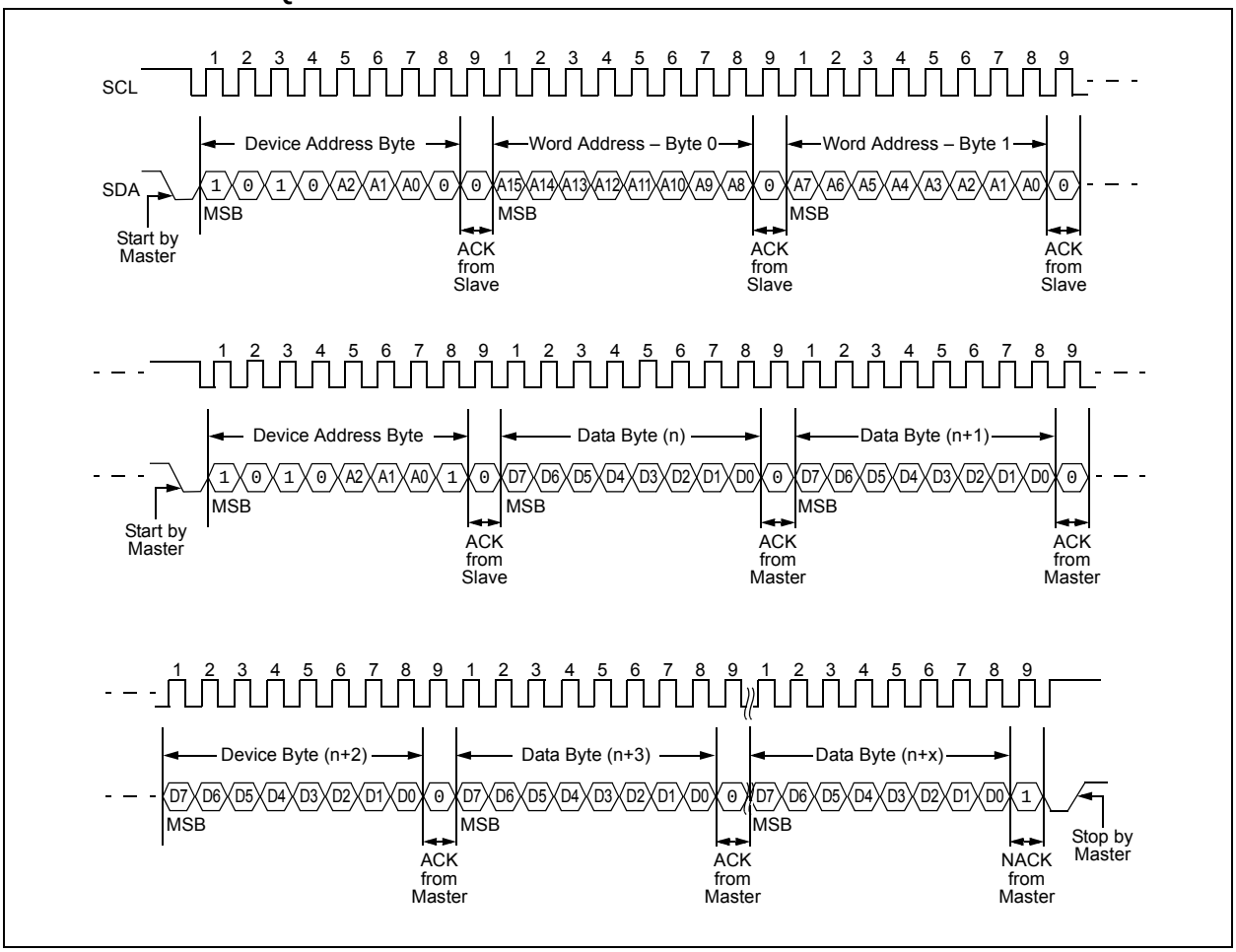


7.3 Sequential Read

A sequential read is initiated by either a current address read or a random read. After the master receives a data byte, the master responds with an Acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out the sequential data byte. When the maximum memory address is reached, the internal Address Pointer will automatically roll over from word address, FFFFh, to word address, 0000h, if the master Acknowledges the byte received from the word address FFFFh.

All types of read operations will be terminated if the master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into Standby mode. After the NACK response, the master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

FIGURE 7-3: SEQUENTIAL READ



8.0 HIGH-SPEED MODE

The 24CS512 supports the I^2C High-Speed (HS) mode allowing it to operate at clock frequencies up to 3.4 MHz for read and write operations.

In order to place the 24CS512 into HS mode, the master must first initiate a Start condition, followed by the reserved HS mode master code of '00001xxxb' (Table 8-1). The HS mode master code must be sent to the device at Fast mode plus (1 MHz) or slower clock frequencies. Since the HS mode master code is meant to be recognized by all slave devices that support the HS mode, the 24CS512 will not Acknowledge (NACK) the HS mode master code.

TABLE 8-1: HIGH-SPEED MODE MASTER CODE

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK Bit
0	0	0	0	1	x	x	x	NACK from Slaves

Once the 24CS512 receives the HS mode master code and the NACK occurs, the 24CS512 will relax its input filters on SDA and SCL to the HS mode tolerance to accept transfers, at up to 3.4 MHz. The device will then enter HS mode and wait for a Repeated Start condition before the next operation can occur.

Next, the master must issue a Start condition, followed by a valid device address byte to which the device will ACK. The master can continue with read or write operations at the higher clock speed and the 24CS512 will continue to operate in the HS mode until one of the following events occurs:

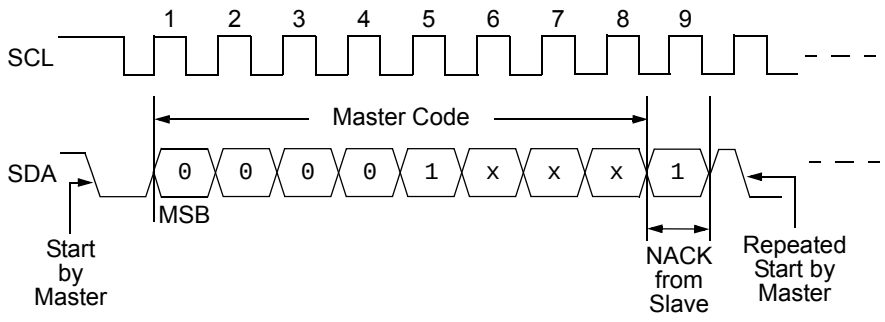
- The master sends a Stop condition. Therefore, the master should use a Repeated Start condition to begin new HS mode operations rather than a Stop-Start sequence.
- A Power-on-Reset (POR) event occurs.

Note: The internal write cycle requires a Stop condition to be sent after the last data byte. This Stop condition will cause the 24CS512 to exit HS mode. Therefore, if more than one page of data is to be written, HS mode must be re-entered for every write operation.

Once the 24CS512 exits the HS mode from one of these events, the device will switch its input and output filters back to the standard I^2C (Legacy) mode. Figure 8-1 illustrates the HS mode entry sequence.

Note: High-Speed mode entry is ignored during a write cycle. Therefore, polling must occur while using Fast mode plus (1 MHz) or slower clock frequencies. Refer to **Section 6.5 "Acknowledge Polling"** for additional information. High-Speed mode can be re-entered after the write cycle has completed.

FIGURE 8-1: HIGH-SPEED MODE ENTRY SEQUENCE



9.0 CONFIGURATION REGISTER

The 24CS512 device contains a 16-bit Configuration register, which is accessed via a specific device address and word address. If desired, the Configuration register can be locked so that it is set to read-only and can no longer be modified, thereby making the current data protection scheme permanent.

9.1 Accessing the Configuration Register

The value of the Configuration register can be determined by executing a random read sequence to a specific address. Changing the value of the Configuration register is accomplished with a byte write sequence with the requirements outlined later in this section.

Accessing this register requires the use of '1011b' (Bh) as the device type identifier in the device address (see Table 9-1). Following the device type identifier is the hardware slave address bits for which the values are determined by the device address input pins, A2, A1 and A0 (see **Section 2.0 "Pin Descriptions"**). Finally, bit 0 is the Read/Write Select (R/$\overline{W}$) bit, where a logic '1' is used for reading and a logic '0' is used for writing.

When accessing the Configuration register, a 16-bit word address must be sent to the device. All bits in the word address are ignored except for bits A15, A11 and A10. Bits A15 and A11 must be set to logic '1' and bit A10 must be set to logic '0'. Refer to Table 9-2 and Table 9-3 for additional information.

TABLE 9-1: CONFIGURATION REGISTER DEVICE ADDRESS

Memory Region	Device Type Identifier				Hardware Address Bits(1)			Read/Write
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Register	1	0	1	1	A2	A1	A0	R/$\overline{W}$

Note 1: The hardware slave address bits must be set to logic '0' when using the SOT-23 package.

TABLE 9-2: CONFIGURATION REGISTER WORD ADDRESS BYTE 0

Word Address	A15	A14	A13	A12	A11	A10	A9	A8
Word Address Byte 0	1	x	x	x	1	0	x	x

TABLE 9-3: CONFIGURATION REGISTER WORD ADDRESS BYTE 1

Word Address	A7	A6	A5	A4	A3	A2	A1	A0
Word Address Byte 1	x	x	x	x	x	x	x	x

9.2 Configuration Register Format

Following the word address bytes are the contents of the 16-bit Configuration register. The Configuration register format and bit definitions are seen in Register 9-1 for the first byte (Byte 0) and in Register 9-2 for the second byte (Byte 1).

REGISTER 9-1: CONFIGURATION REGISTER – BYTE 0

R-0	U-0	U-0	U-0	U-0	U-0	R/W	R/W
ECS	—	—	—	—	—	EWPM	LOCK
bit 15							bit 8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ECS:** Error Correction State bit
- 1 = The previously executed read operation did require the use of the Error Correction Code (ECC) scheme
- 0 = The previously executed read operation did not require the use of the Error Correction Code (ECC) scheme

bit 14-10 **Unimplemented:** Read as '0'

bit 9 **EWPM:** Enhanced Software Write Protection Mode bit
- 1 = Enhanced Protection: WP pin is treated as a don't care and the memory array is protected in accordance with the SWP bits defined in Register 9-2
- 0 = Legacy Protection (factory default): Entire memory array and Security register contents are protected via the WP pin

bit 8 **LOCK:** Lock Configuration Register bit
- 1 = The Configuration register is set to read-only (permanent)
- 0 = The Configuration register can be written to (factory default)

Error Correction State bit (ECS): This bit is used when the user needs to determine whether the on-chip Error Correction Code (ECC) logic scheme has been invoked. For more information related to ECC, refer to **Section 6.3 "Internal Writing Methodology"**. The ECS bit will be set to logic '0' unless the previously executed read operation required the use of the ECC logic scheme. When this occurs, the ECS bit will set to logic '1'. The ECS bit will continue to read a logic '1' until another read operation is issued and the use of the ECC logic scheme was not required or a Power-on Reset (POR) event occurred.

Enhanced Software Write Protection Mode bit (EWPM): This bit is a feature in which the user can select between Legacy Hardware Write Protection mode (logic '0') and Enhanced Software Write Protection mode (logic '1'). Legacy Hardware Write Protection mode allows the entire memory array to be write-protected via the WP pin.

Enhanced Software Write Protection is a software write-protect feature where the memory array is divided into eight separate 64-Kbit (8192-byte) zones. Each zone is independent and is configured using the SWP<7:0> bits (Register 9-2). For additional information related to the write protection schemes, refer to **Section 6.6 "Write Protection"**.

Lock Configuration Register bit (LOCK): This bit allows the user to lock the Configuration register so that it is set to read-only and can no longer be modified, thereby making the current data protection scheme permanent. Refer to **Section 9.5 "Locking the Configuration Register"** for additional information on locking the Configuration register.

REGISTER 9-2: CONFIGURATION REGISTER – BYTE 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SWP7	SWP6	SWP5	SWP4	SWP3	SWP2	SWP1	SWP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

If EWPM = 1:

bit 7 **SWP7:** Software Write Protection Memory Zone 7 bit
1 = Memory Zone 7 (E000h-FFFFh) is write-protected
0 = Memory Zone 7 (E000h-FFFFh) is not write-protected

bit 6 **SWP6:** Software Write Protection Memory Zone 6 bit
1 = Memory Zone 6 (C000h-DFFFh) is write-protected
0 = Memory Zone 6 (C000h-DFFFh) is not write-protected

bit 5 **SWP5:** Software Write Protection Memory Zone 5 bit
1 = Memory Zone 5 (A000h-BFFFh) is write-protected
0 = Memory Zone 5 (A000h-BFFFh) is not write-protected

bit 4 **SWP4:** Software Write Protection Memory Zone 4 bit
1 = Memory Zone 4 (8000h-9FFFh) is write-protected
0 = Memory Zone 4 (8000h-9FFFh) is not write-protected

bit 3 **SWP3:** Software Write Protection Memory Zone 3 bit
1 = Memory Zone 3 (6000h-7FFFh) is write-protected
0 = Memory Zone 3 (6000h-7FFFh) is not write-protected

bit 2 **SWP2:** Software Write Protection Memory Zone 2 bit
1 = Memory Zone 2 (4000h-5FFFh) is write-protected
0 = Memory Zone 2 (4000h-5FFFh) is not write-protected

bit 1 **SWP1:** Software Write Protection Memory Zone 1 bit
1 = Memory Zone 1 (2000h-3FFFh) is write-protected
0 = Memory Zone 1 (2000h-3FFFh) is not write-protected

bit 0 **SWP0:** Software Write Protection Memory Zone 0 bit
1 = Memory Zone 0 (0000h-1FFFh) is write-protected
0 = Memory Zone 0 (0000h-1FFFh) is not write-protected

If EWPM = 0:

bit 7-0 Unused

Software Write Protection Memory Zone bits (SWP<7:0>): These bits divide the memory array into eight separate 64-Kbit (8192-byte) zones. Each zone can be set independently from the seven other protection zones. The corresponding SWP bit should be set to a logic '1' to write-protect that zone. All of the eight SWP bits are set to logic '0' as a factory default. For additional information on the Software Write Protection scheme, refer to **Section 6.6.2 "Enhanced Software Write Protection Mode"**.

Note: In Legacy Hardware Write Protection mode (EWPM = 0), the SWP<7:0> bits are ignored. However, a dummy value must still be sent during the write sequence to initiate the internal write operation.

9.3 Writing to the Configuration Register

When writing to the Configuration register, a byte write sequence must be sent to the device (see **Section 6.1 "Byte Write"** for additional information). The data address values must be compliant with the values found in Table 9-1, Table 9-2 and Table 9-3.

In order for the internal write process to start, both bytes (Byte 0 and Byte 1), along with a confirmation byte, need to be sent to the device. Sending anything other than these three bytes will cause the write cycle to abort and the contents of the Configuration register will not be changed.

The data of the confirmation byte depends on the value being written to the LOCK bit. If the user intends to lock the Configuration register (LOCK = 1), the confirmation byte must be 99h. If the user intends to leave the register unlocked (LOCK = 0), the confirmation byte must be 66h.

Note: Writing to the Configuration register cannot be inhibited by asserting the Write-Protect pin. Refer to **Section 6.6 "Write Protection"**, which describes the device behavior with respect to the Write-Protect pin status.

Note: If an attempt is made to write to the Configuration register after the Configuration register has been locked, the device will Acknowledge the commands, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

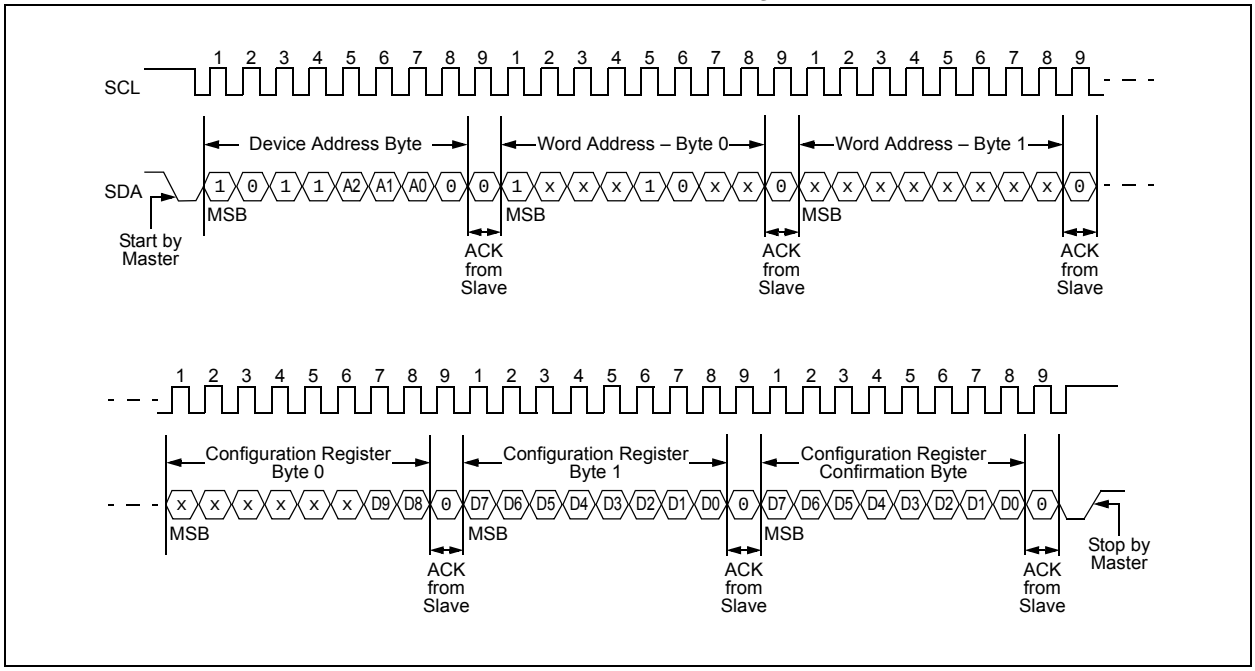
Table 9-4 illustrates the valid data values for the confirmation byte. Figure 9-1 illustrates the Configuration register write sequence.

Note: The Configuration register cannot be unlocked once it is locked.

TABLE 9-4: CONFIGURATION REGISTER CONFIRMATION BYTE

New LOCK Bit Value	D7	D6	D5	D4	D3	D2	D1	D0
1 (locked)	1	0	0	1	1	0	0	1
0 (unlocked)	0	1	1	0	0	1	1	0

FIGURE 9-1: CONFIGURATION REGISTER WRITE SEQUENCE



9.4 Reading the Configuration Register

When reading the Configuration register, a random read sequence must be sent to the device (see **Section 7.2 "Random Read"** for additional information). The address values must be compliant with the values found in Table 9-1, Table 9-2 and Table 9-3.

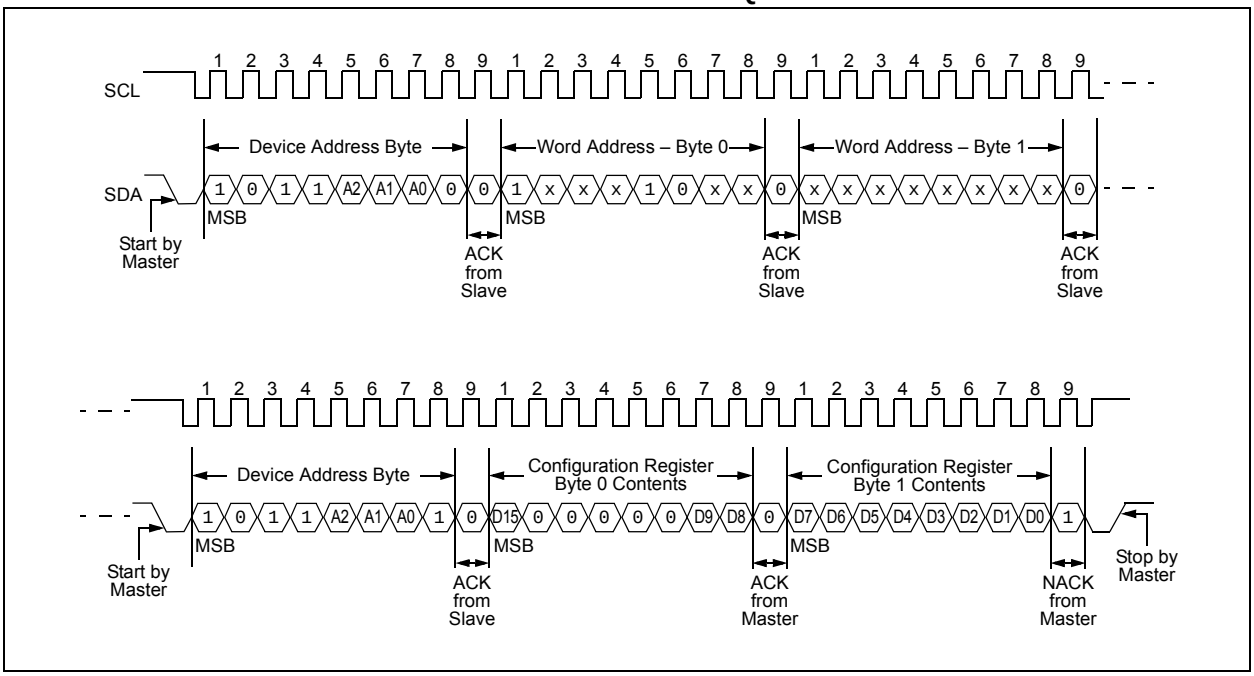
Figure 9-2 illustrates the Configuration register read sequence. It is not possible to read the contents of the Configuration register with a current address read sequence as the correct word address bytes must be sent to the device.

Note:	If a Stop condition is issued after the word address bytes, the read operation to the Configuration register will not execute properly.

Accessing the Configuration register is only possible if any sequence or command to the EEPROM (if one has been sent) has been properly terminated with a Stop condition. Without proper termination of that previous sequence, all communications with the Configuration register will not execute successfully.

Note:	The 24CS512 will automatically roll over from the second Configuration register data byte to the first data byte if the master continues to Acknowledge the data bytes during the read operation.

FIGURE 9-2: CONFIGURATION REGISTER READ SEQUENCE



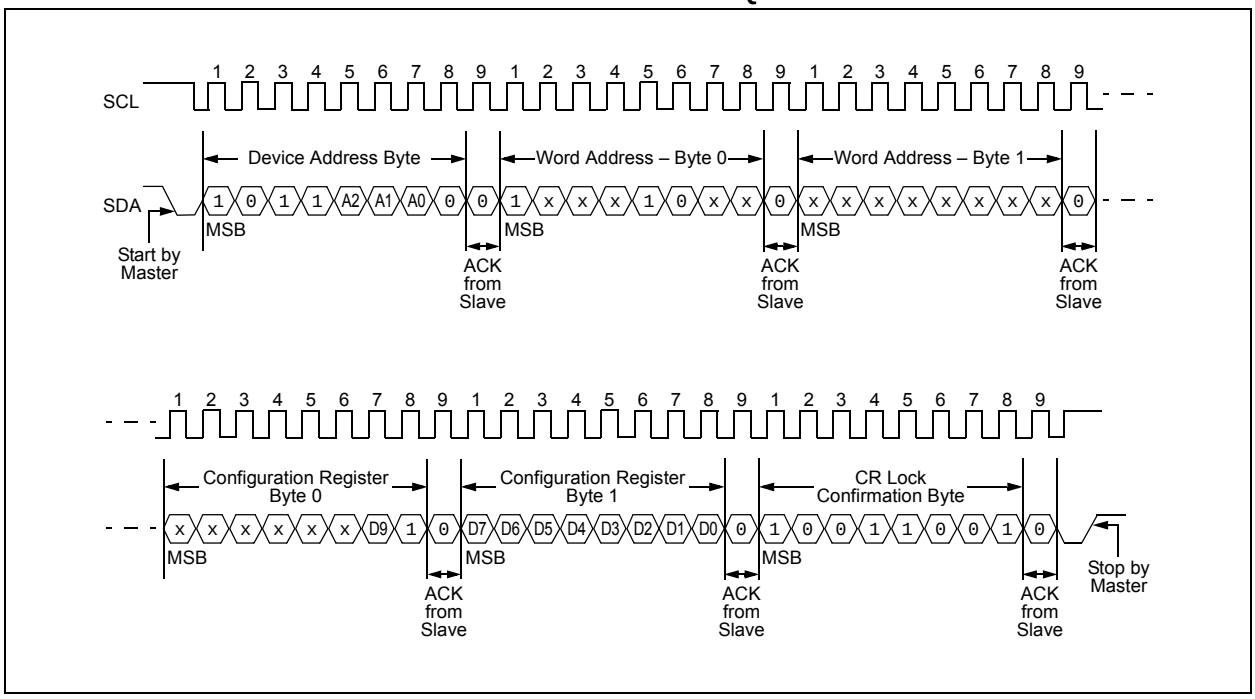
9.5 Locking the Configuration Register

The locking mechanism of the Configuration register is controlled through the LOCK bit. The data of the confirmation byte depends on the value being written to the LOCK bit. If the user intends to lock the Configuration register (LOCK = 1), the confirmation byte must be 99h. If the user intends to leave the register unlocked (LOCK = 0), the confirmation byte must be 66h. A mismatch of the LOCK bit and the confirmation byte will cause the write operation to abort. Refer to Table 9-4 for additional information on the confirmation byte and the LOCK bit. Figure 9-3 illustrates the Configuration register lock sequence.

Note:	Once the Configuration register has been locked, it cannot be unlocked.

Note:	Locking the Configuration register cannot be inhibited by asserting the Write-Protect pin. Refer to **Section 6.6 "Write Protection"**, which describes the device behavior with respect to the Write-Protect pin status.

FIGURE 9-3: CONFIGURATION REGISTER LOCK SEQUENCE



10.0 SECURITY REGISTER

The 24CS512 includes a 256-byte Security register, organized as two 128-byte pages. The Security register is segmented into a 128-byte read-only section and a 128-byte user-programmable lockable identification page section. Device and word address requirements to access the Security register are outlined in **Section 3.3.1 "Valid Device Address Byte Inputs"** and **Section 3.3.2 "Word Address Bytes"**.

The user-programmable portion supports both byte write and page write operations. The read-only section contains a preprogrammed, globally unique, 128-bit serial number. The user-programmable portion may be permanently locked with the lock operation.

Note:	The entire 128-bit serial number must be used to ensure a unique number.

TABLE 10-1: SECURITY REGISTER ORGANIZATION

Security Register Byte Number									
0	1	...	14	15	16	17	...	126	127
Factory Programmed (read-only) 0-15: Device Serial Number					Reserved for Future Use				
128	129	130	131	...		252	253	254	255
User-Programmable Lockable Identification Page									

10.1 Custom Programming Option

The 24CS512 supports the preprogramming and subsequent locking of customer-specific data in the user-programmable portion of the Security register. Contact your local sales representative for support for custom programming options.

10.2 Read Operations in the Security Register

Random read and sequential read operations of the Security register require that the device type be set to '1011b' (Bh) and matching the hardware slave address bits (A2, A1, A0) to their corresponding device address input pins. Following the device address byte, the word address bytes must be sent to the device. Bits A15 and A10 must be set to logic '0' and bit A11 must be set to logic '1'. Current address reads of the Security register are not supported.

The first 16 bytes of the Security register are, by definition, read-only and contain a preprogrammed, globally unique, 128-bit serial number. The remaining 112 bytes on the first page of the Security register are reserved for future use and set to read-only.

The upper 128 bytes of the Security register are user-programmable and can be locked from any future programming operations (see **Section 10.4 "Locking the Security Register"** for more details).

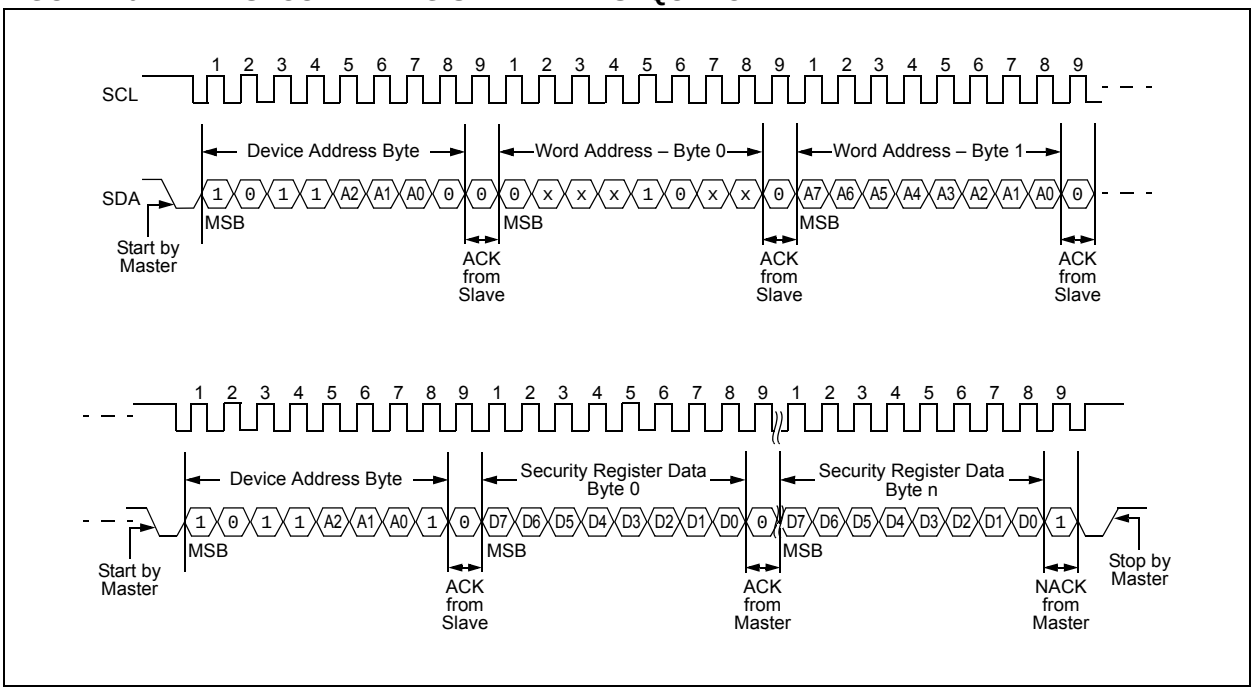
Note:	Accessing the Security register is only possible if any sequence or command to the EEPROM (if one has been sent) has been properly terminated with a Stop condition. Without proper termination of the previous sequence, all communications with the Security register will not execute successfully.

Note:	If the application is to read the first byte of the serial number, the word address input needs to be 0800h.

When the end of the Security register is reached (256 bytes of data), the word address will roll over to the beginning of the Security register, starting with the Most Significant Byte (Byte 0) of the 128-bit serial number.

The serial number read operation, or any read of the Security register, is terminated when the master does not respond with an ACK, and instead, issues a Stop condition.

FIGURE 10-1: SECURITY REGISTER READ SEQUENCE



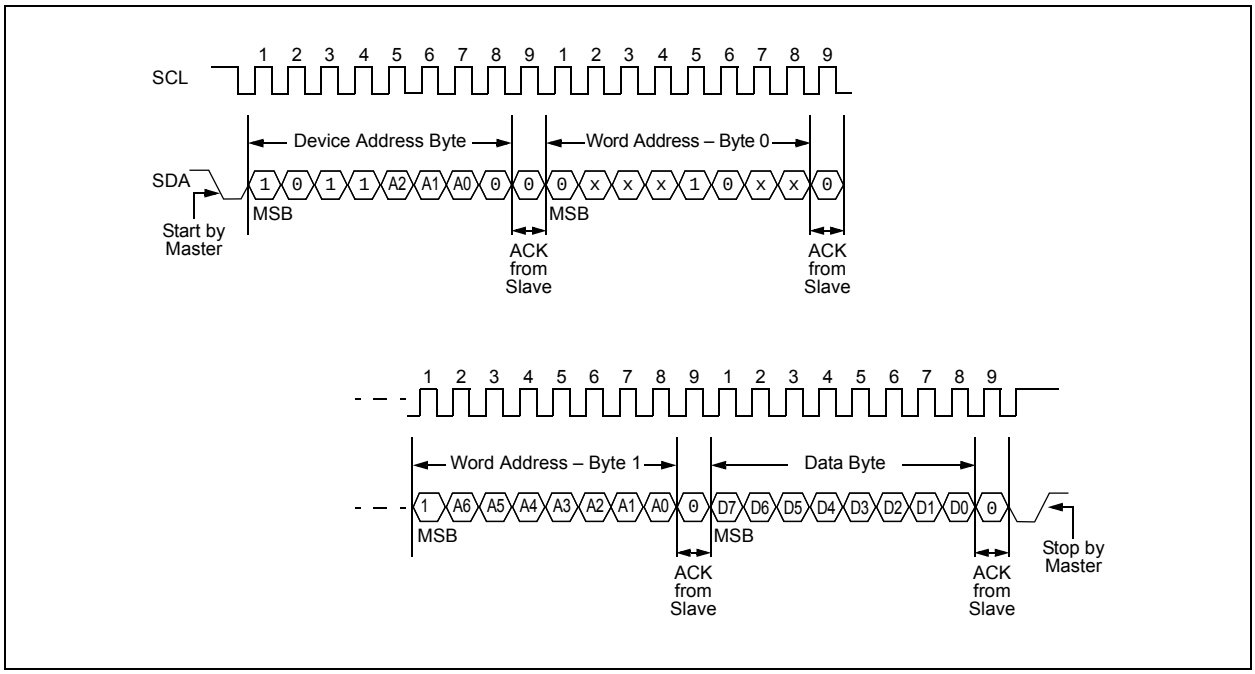
10.3 Write Operations in the Security Register

The Security register supports byte writes, page writes and partial page writes in the upper 128 bytes of the region. Page writes and partial page writes in the Security register have the same page boundary restrictions and behavior as they do in the EEPROM region (see **Section 6.2 "Page Write"**).

Writing in this region requires beginning the device address byte with '1011b' (Bh), matching the hardware slave address bits (A2, A1, A0) to their corresponding device address input pins and sending a logic '0' to the Read/Write Select (R/$\overline{W}$) bit. Following the device address byte, the word address bytes must be sent to the device. Bits A15 and A10 must be set to logic '0' and bit A11 must be set to logic '1'. Figure 10-2 illustrates a byte write operation in the Security register. If an attempt is made to write to the Security register with the WP pin held high, or after the Security register has been locked, no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note:	Enhanced software write protection does not affect write operations to the Security register.

FIGURE 10-2: BYTE WRITE IN THE SECURITY REGISTER



10.4 Locking the Security Register

The user-programmable portion of the Security register can be permanently inhibited from future writing with the lock operation. The status of the lock state can be determined from the check lock operation.

10.4.1 LOCK OPERATION

The lock operation is an irreversible sequence that will permanently prevent all future writing to the upper 128 bytes of the Security register. Once the lock operation has been executed, the entire 256-byte Security register becomes read-only.

Note:	Once the Security register has been locked, *it cannot be unlocked*.

The lock operation protocol emulates a byte write operation to the Security register, however, the A11 through A8 bits of the word address must be set to '0110b' (6h).

The remaining bits of the word address and the data byte are don't care bits. Even though these bits are don't care bits, they still must be transmitted to the device. If the remaining bits are not transmitted, this will cause the write cycle to abort and the Security register to remain unlocked.

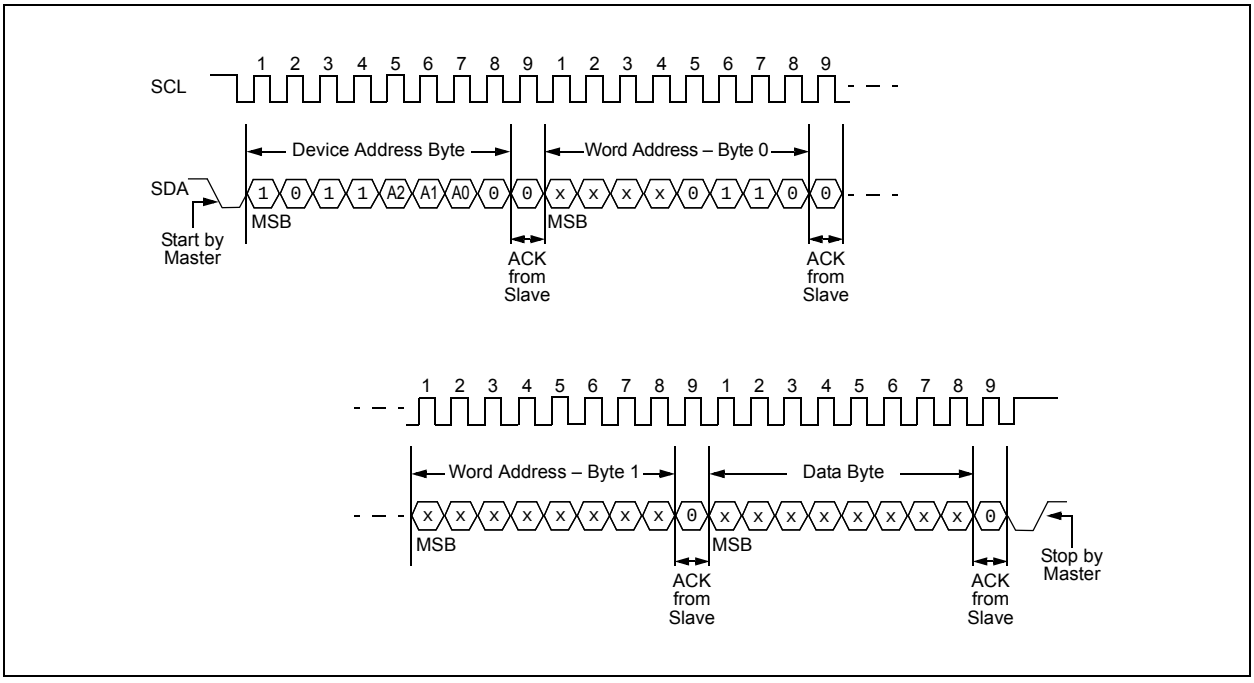
An ACK response to the word address and data byte indicates the Security register is not currently locked. A NACK response indicates the Security register region is already locked.

Refer to **Section 10.4.2 "Determining the Lock State of the Security Register"** for details about determining the lock status of the Security register.

The sequence completes with a Stop condition being sent to the device, which initiates a self-timed internal write cycle. The lock operation will conclude upon completion of that write cycle, subsequently making the Security register permanently read-only.

Note:	The lock operation cannot be inhibited by asserting the Write-Protect pin. Refer to **Section 6.6 "Write Protection"**, which describes the device behavior with respect to the Write-Protect pin status.

FIGURE 10-3: LOCK OPERATION

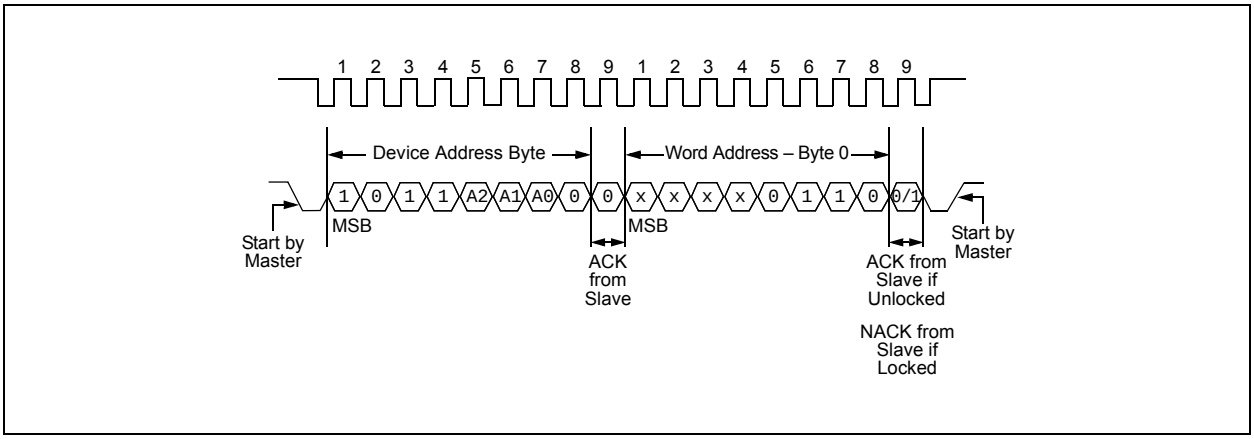


10.4.2 DETERMINING THE LOCK STATE OF THE SECURITY REGISTER

The check lock operation follows the same sequence as the lock operation (including '0110b' in the A11 through A8 bits of the word address) with the exception that only the device address byte and the first word address byte (byte 0) need to be transmitted to the device. An ACK response to the word address byte indicates the lock has not been set while a NACK response indicates the lock has been set. If the lock has already been set, it cannot be undone. The check lock operation is completed by the master sending a Stop condition to the device. This sequence is shown in Figure 10-4.

Note:	Only the device address byte and first word address byte (byte 0) should be sent to determine the lock state of the Security register. Sending the second word address byte (byte 1) and a data byte can inadvertently lock the Security register.

FIGURE 10-4: DETERMINING THE LOCK STATE



11.0 MANUFACTURER IDENTIFICATION REGISTER

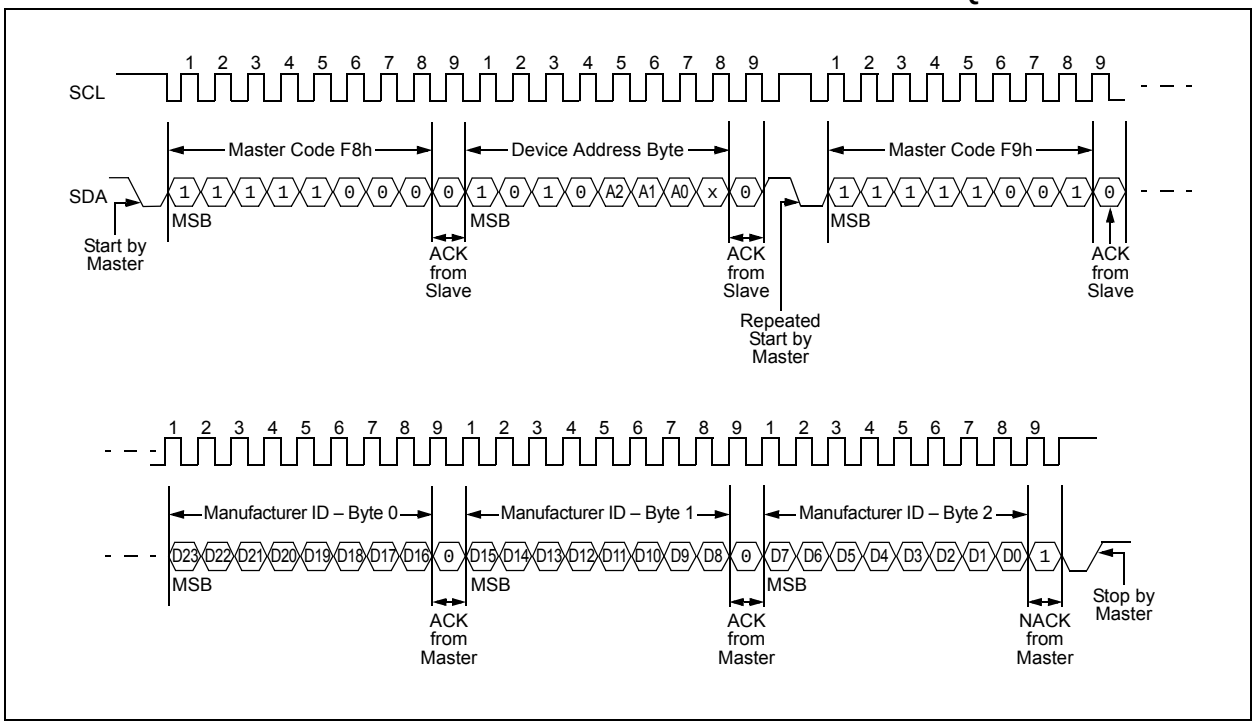
The 24CS512 offers the ability to query the device for the manufacturer, density and revision information. By using the reserved 7-bit master code F8h, the device will return a 24-bit value that corresponds with the reserved I^2C identifier value, along with further data to signify a 512-Kbit density and the device revision.

To read the Manufacturer ID data, the master must send a Start condition, followed by a reserved master code F8h, specified to which all devices on the bus that support the Manufacturer ID will ACK. Next, the specific I^2C device address of the device, from which the Manufacturer ID to be read is sent, followed by a new Start condition. Then, the reserved master code F9h is sent and only the specific device that was previously identified will return an ACK. Now the 24CS512 is ready to return its unique 24-bit Manufacturing ID value.

Note:	A Repeated Start condition must be sent to the 24CS512 when reading the Manufacturer ID. If a Stop condition, followed by a Start condition, is sent, the internal Address Pointer will reset and the Manufacturer ID will not be read.

The first byte of Manufacturer ID data contains the eight Most Significant bits (D23-D16) of the 24-bit data value. The master can then return an ACK to indicate it successfully received the data, upon which the device will send the second byte (D15-D8) of Manufacturer ID data. The process repeats until all three bytes have been read out and the master sends a NACK (logic '1') to complete the sequence. If the master ACKs (logic '0') the third byte, the internal Address Pointer will roll over back to the first byte of Manufacturer ID data.

FIGURE 11-1: MANUFACTURER IDENTIFICATION REGISTER READ SEQUENCE



11.0.1 MANUFACTURER IDENTIFICATION REGISTER DATA

The Manufacturer Identifier portion of the ID is returned in the 12 Most Significant bits of the three bytes read out. The manufacturer reserved I^2C identifier value is '0000-0000-1101b' (00Dh). Therefore, the first byte read out by the device will be 00h. The upper nibble of the second byte read out is Dh.

The Least Significant 12 bits of the 24-bit Manufacturer ID is comprised of an I^2C identifier defined value that indicates the device density and revision. The D11 through D3 bits indicate the device density and the D2 through D0 bits indicate the device revision. The overall 24-bit value returned by the 24CS512 is 00D0C8h. The output is shown more specifically in Table 11-1.

TABLE 11-1: MANUFACTURER IDENTIFICATION REGISTER FORMAT

Data Type	Field Width	Bit Position within 24-Bit Value	24CS512 Response		
			Binary Value	Hex Value	Indication
Manufacturer	12 Bits	D23-D12	0000-0000-1101	00Dh	Reserved Value
Device Density	9 Bits	D11-D3	0000-1100-1	0C8h	2-Wire, 512-Kbit
Device Revision	3 Bits	D2-D0	000		Revision 1

12.0 DEVICE DEFAULT CONDITION

The 24CS512 is delivered with the EEPROM array set to logic ‘1’, resulting in FFh data in all locations of the EEPROM memory array.

The Security register contains a preprogrammed, 128-bit serial number in the lower 16 bytes. The user-programmable portion (lockable ID page) is unlocked and is set to logic ‘1’, resulting in 128 bytes of FFh data.

The Configuration register is set for Legacy Hardware Write Protection mode and is unlocked.

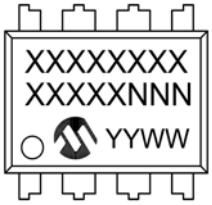
13.0 PACKAGING INFORMATION

13.1 Package Marking Information

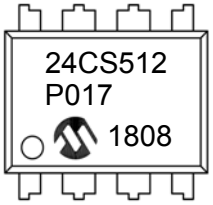
8-Lead MSOP

Example

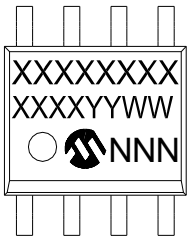
8-Lead PDIP



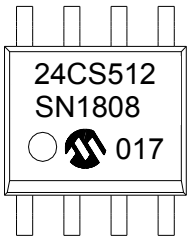
Example



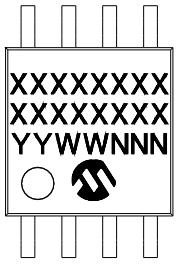
8-Lead 3.9 mm SOIC



Example

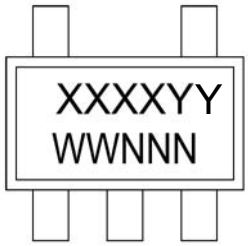


8-Lead 5.28 mm SOIJ

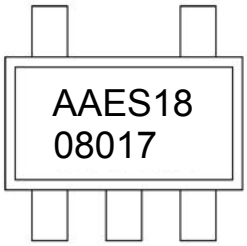


Example

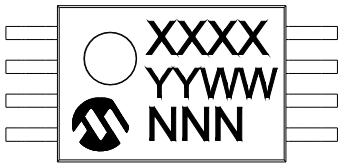
5-Lead SOT-23



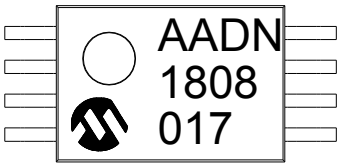
Example



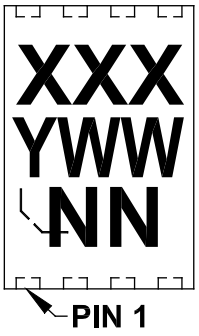
8-Lead 4.4 mm TSSOP



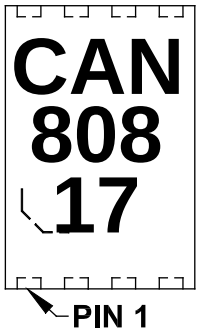
Example



8-Lead 2x3 mm UDFN



Example



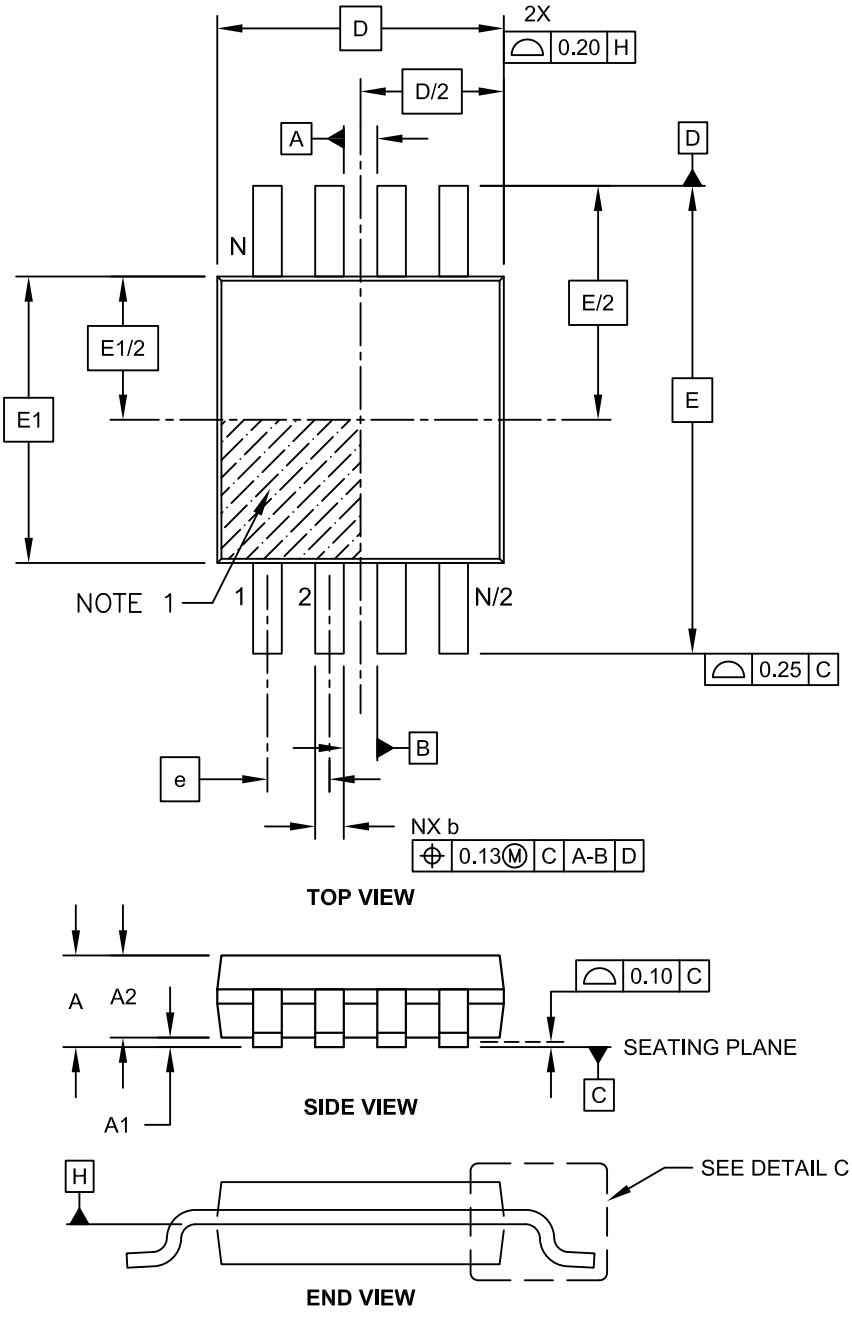
Part Number	1st Line Marking Codes						
	MSOP	PDIP	SOIC	SOIJ	SOT-23	TSSOP	UDFN
24CS512	4CS512	24CS512	24CS512	24CS512	AAES	AADN	CAN

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	*****	These packages are RoHs compliant. The JEDEC® designator can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

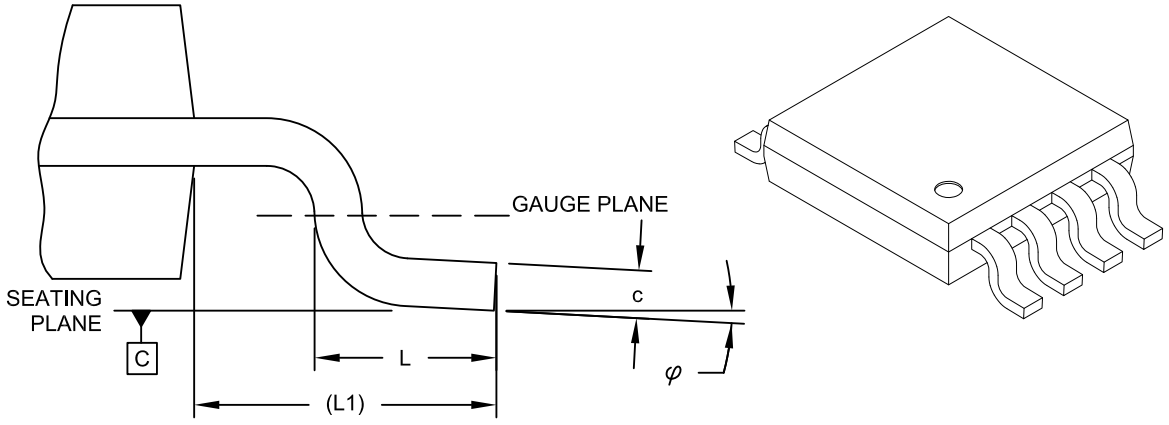
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

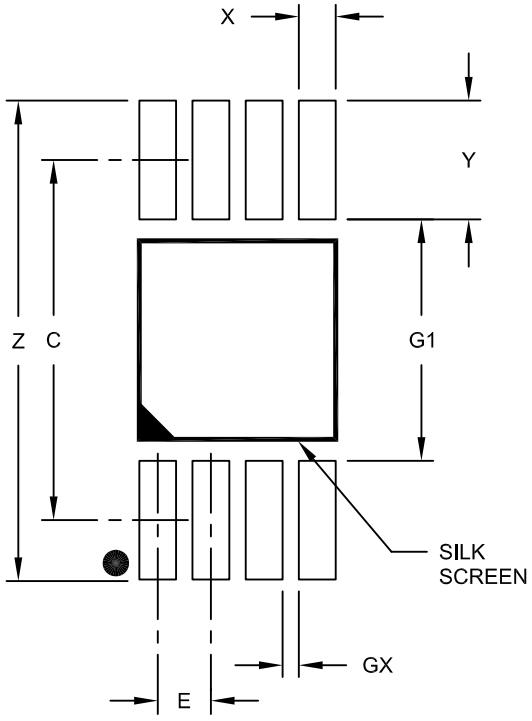
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

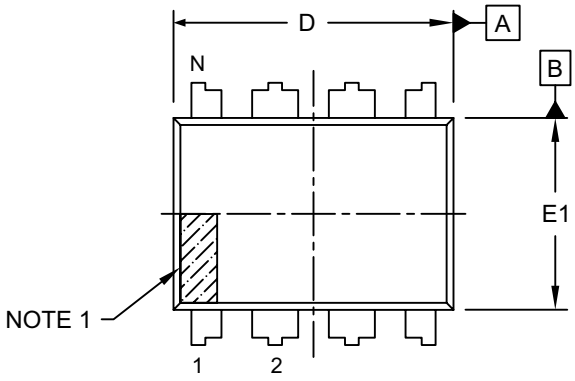
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

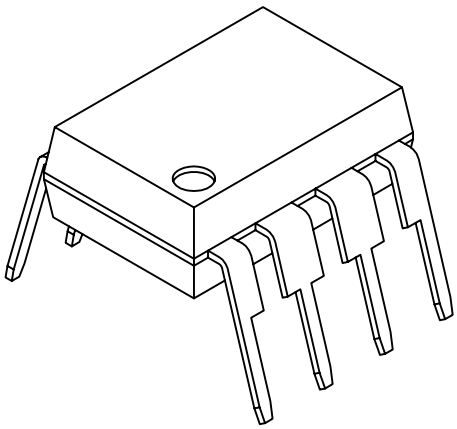
Microchip Technology Drawing No. C04-2111A

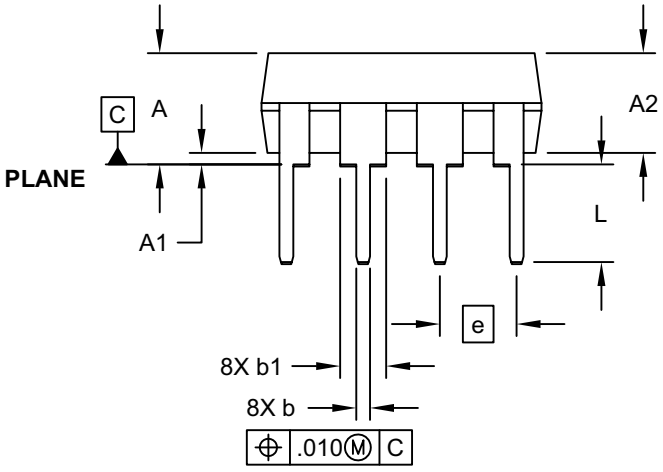
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

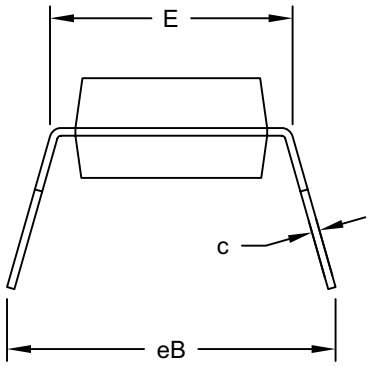


TOP VIEW





SIDE VIEW

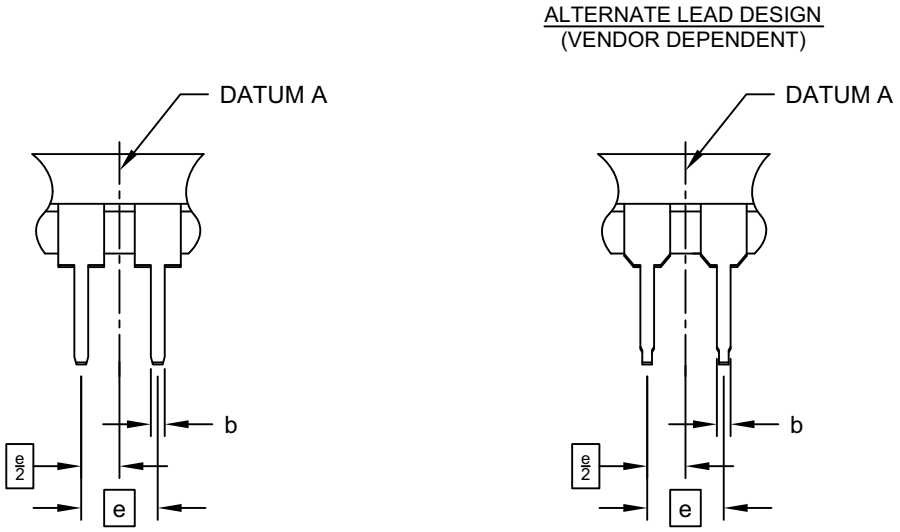


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

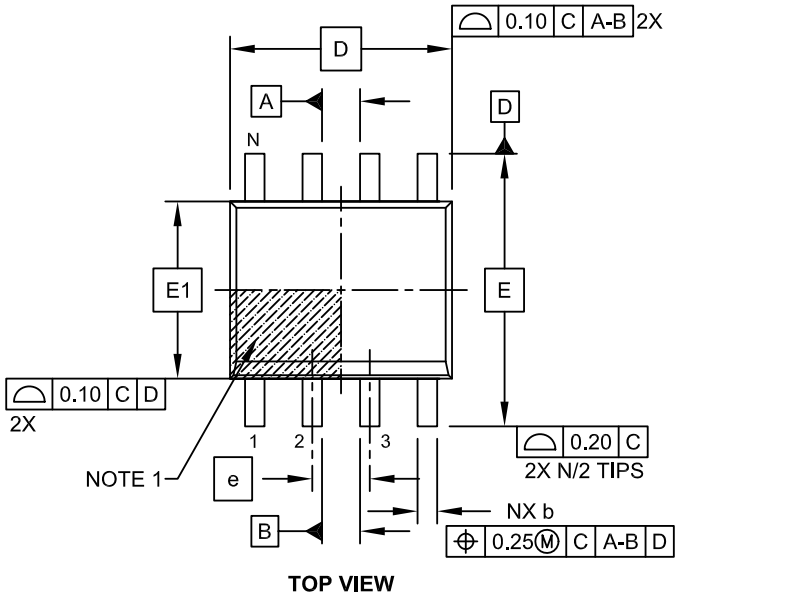
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

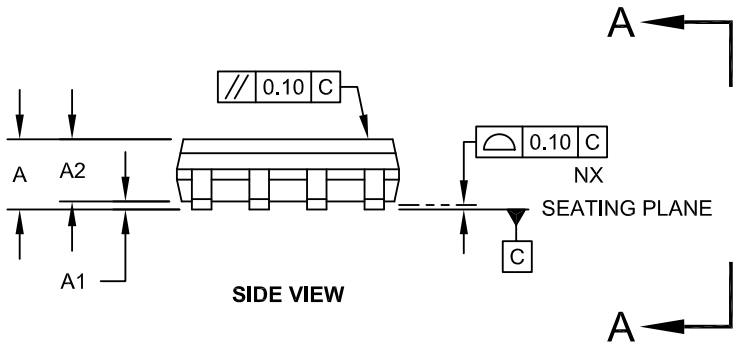
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

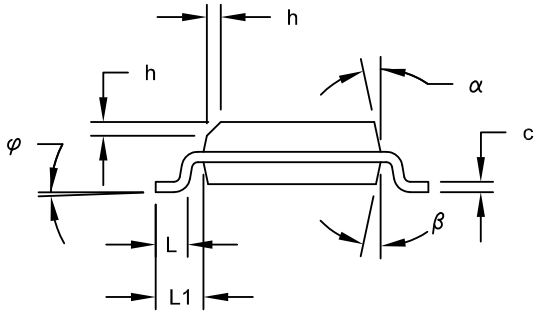
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

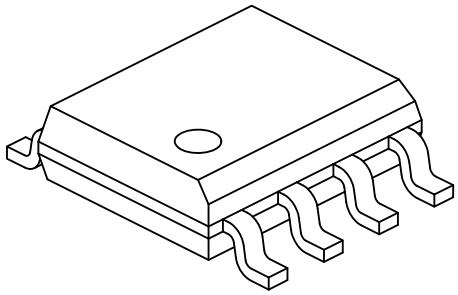


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

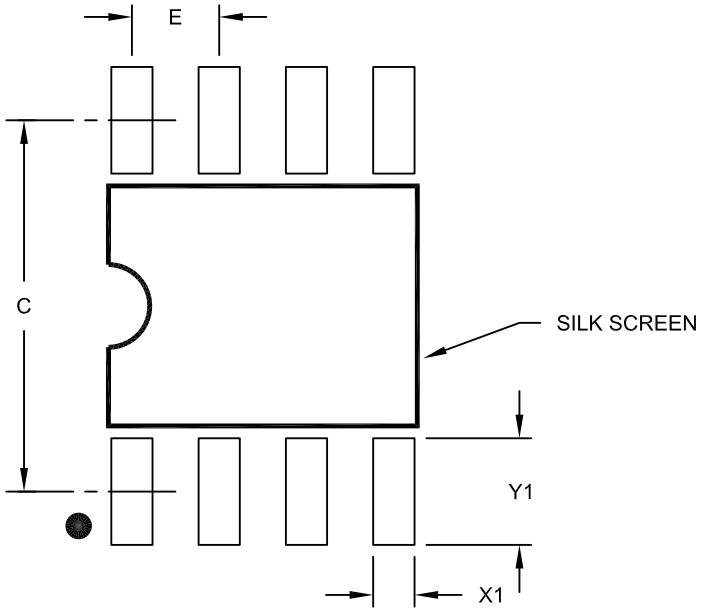
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

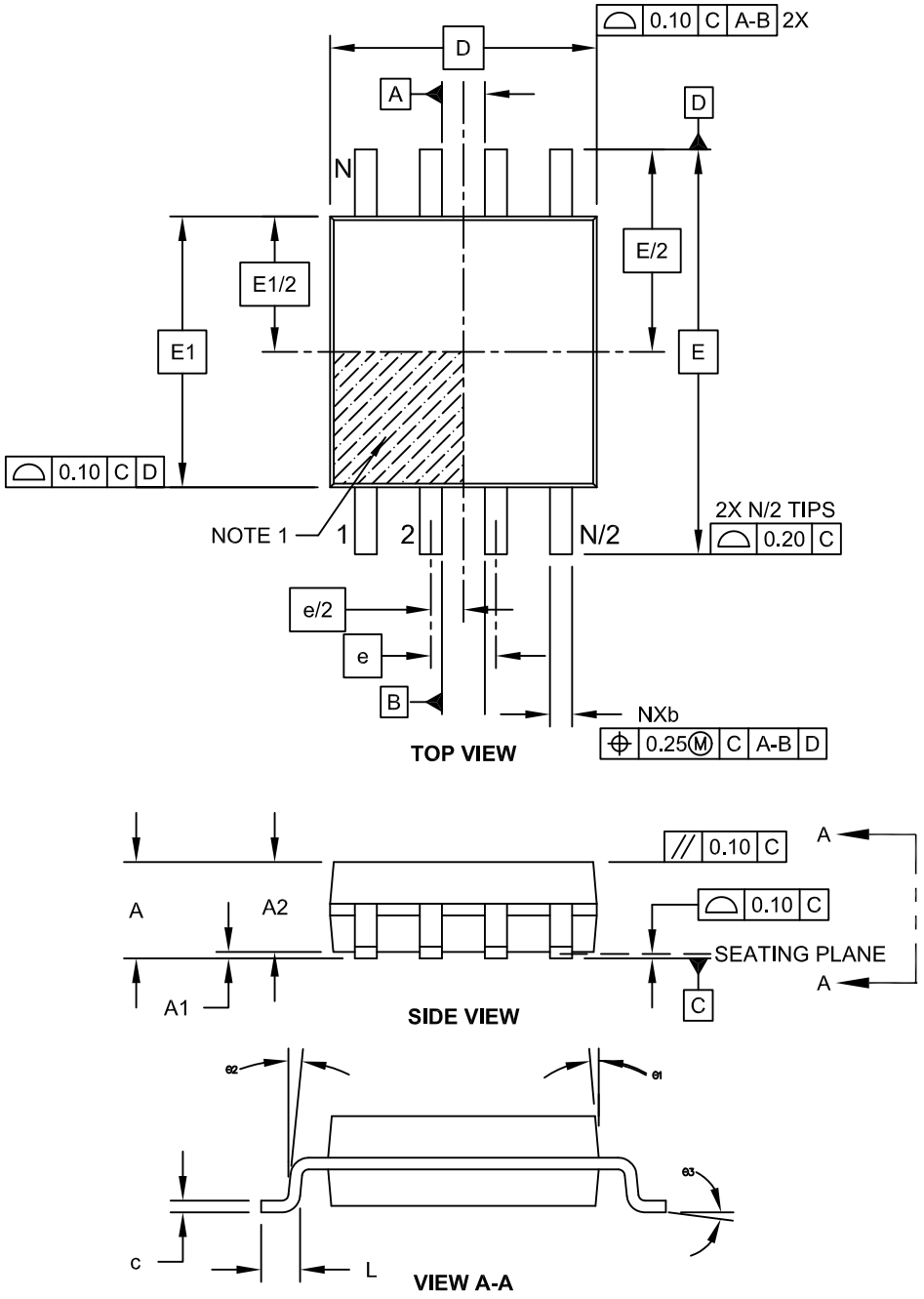
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

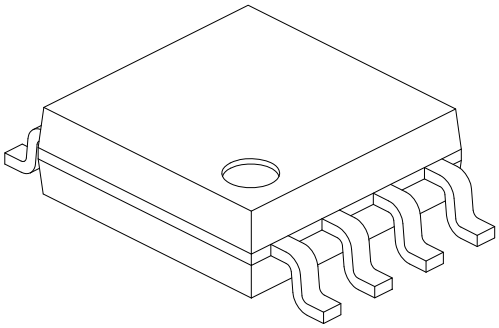
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-056C Sheet 1 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	-	2.03
Standoff §	A1	0.05		0.25
Molded Package Thickness	A2	1.75	-	1.98
Overall Width	E		7.94 BSC	
Molded Package Width	E1		5.25 BSC	
Overall Length	D		5.26 BSC	
Foot Length	L	0.51	-	0.76
Lead Thickness	c	0.15	-	0.25
Lead Width	b	0.36	-	0.51
Mold Draft Angle	θ1	-	-	15°
Lead Angle	θ2	0°	-	8°
Foot Angle	θ3	0°	-	8°

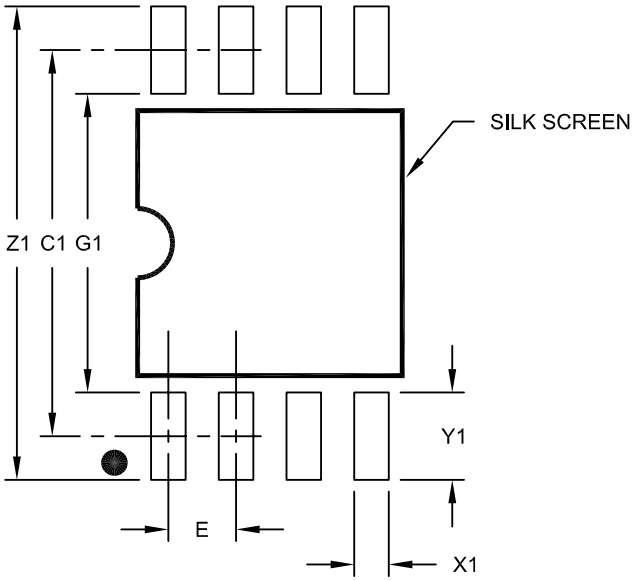
Notes:

1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Overall Width	Z1			9.00
Contact Pad Spacing	C1		7.30	
Contact Pad Width (X8)	X1			0.65
Contact Pad Length (X8)	Y1			1.70
Distance Between Pads	G1	5.60		
Distance Between Pads	G	0.62		

Notes:

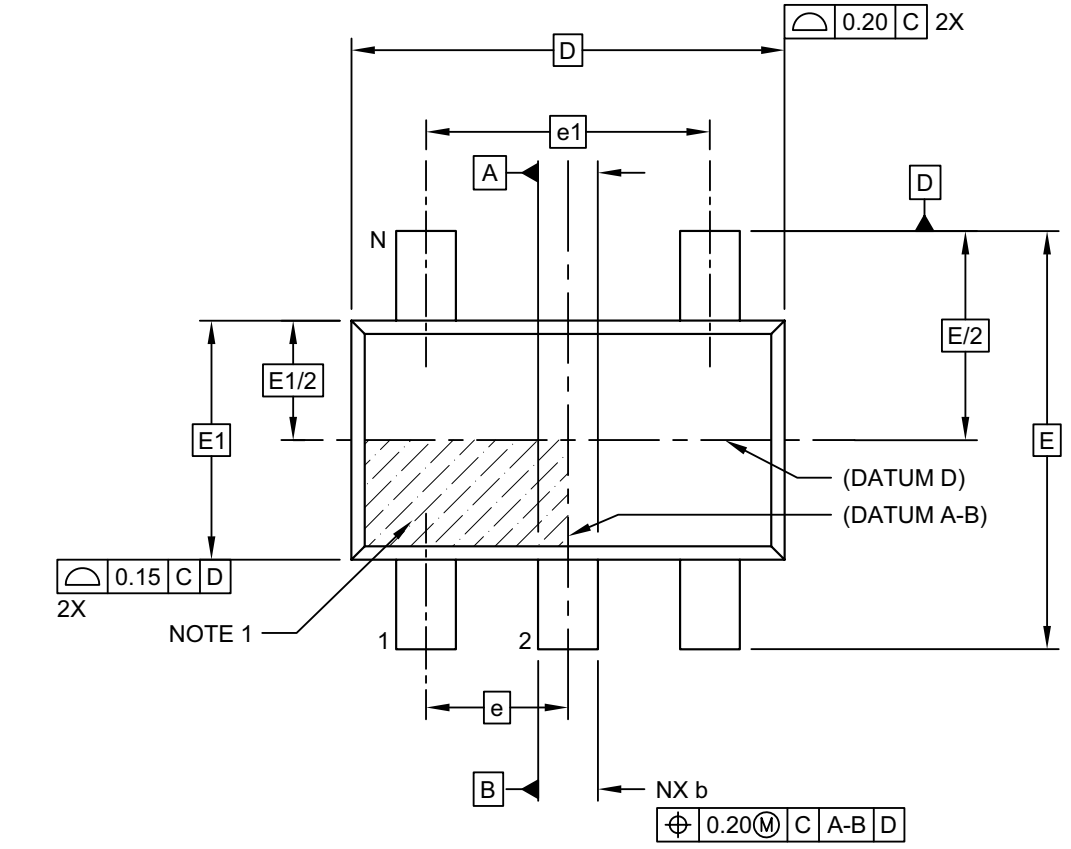
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

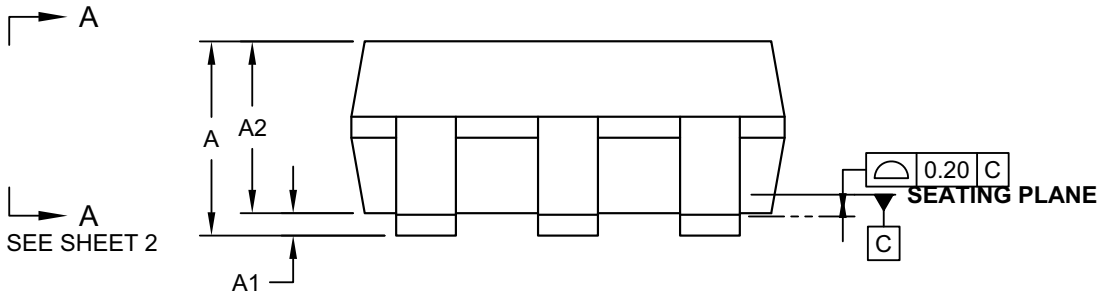
Microchip Technology Drawing No. C04-2056C

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

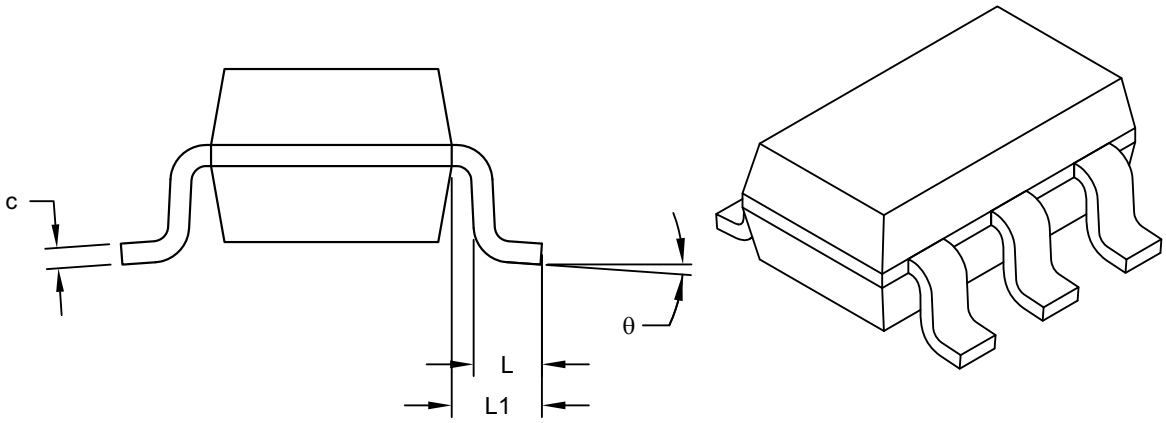


SIDE VIEW

Microchip Technology Drawing C04-028D [OT] Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

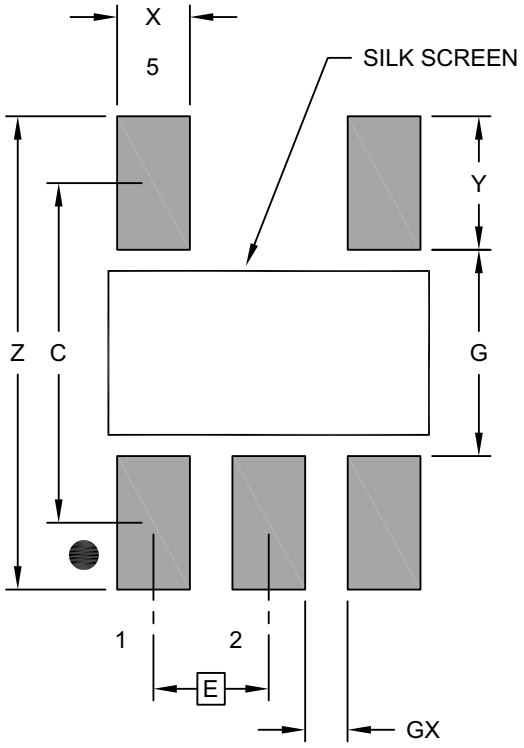
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091D [OT] Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

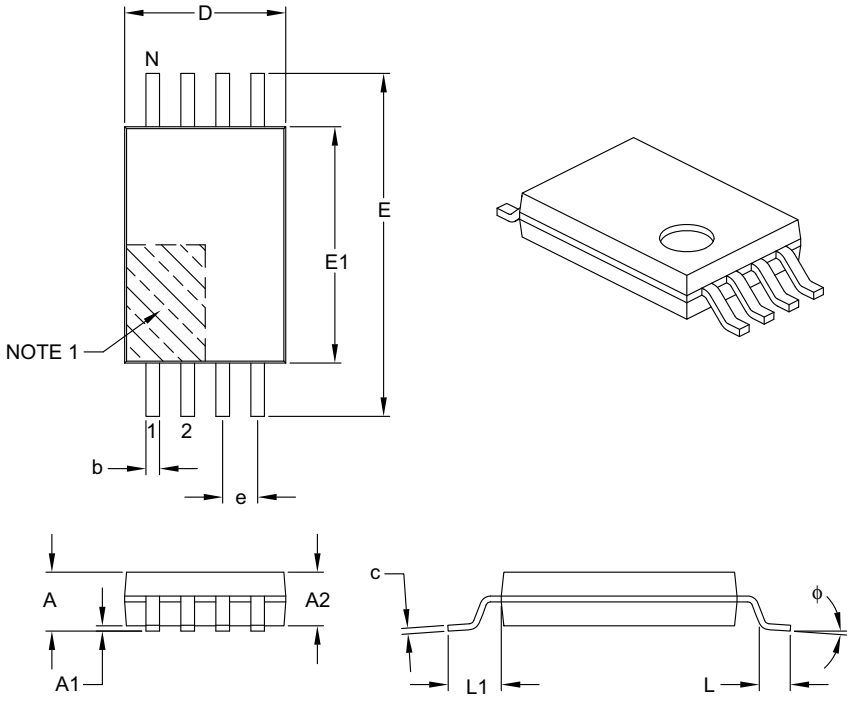
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A [OT]

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

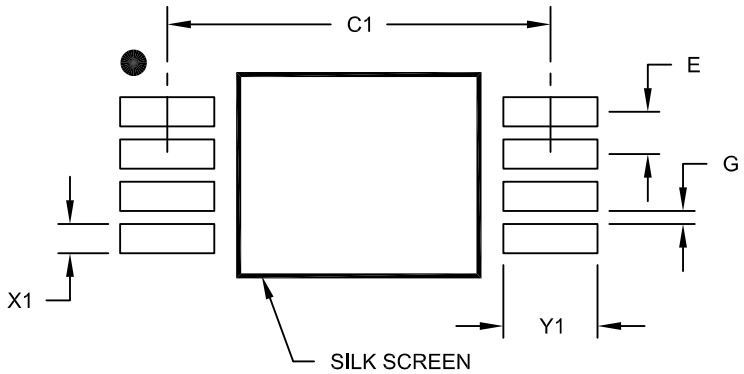
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

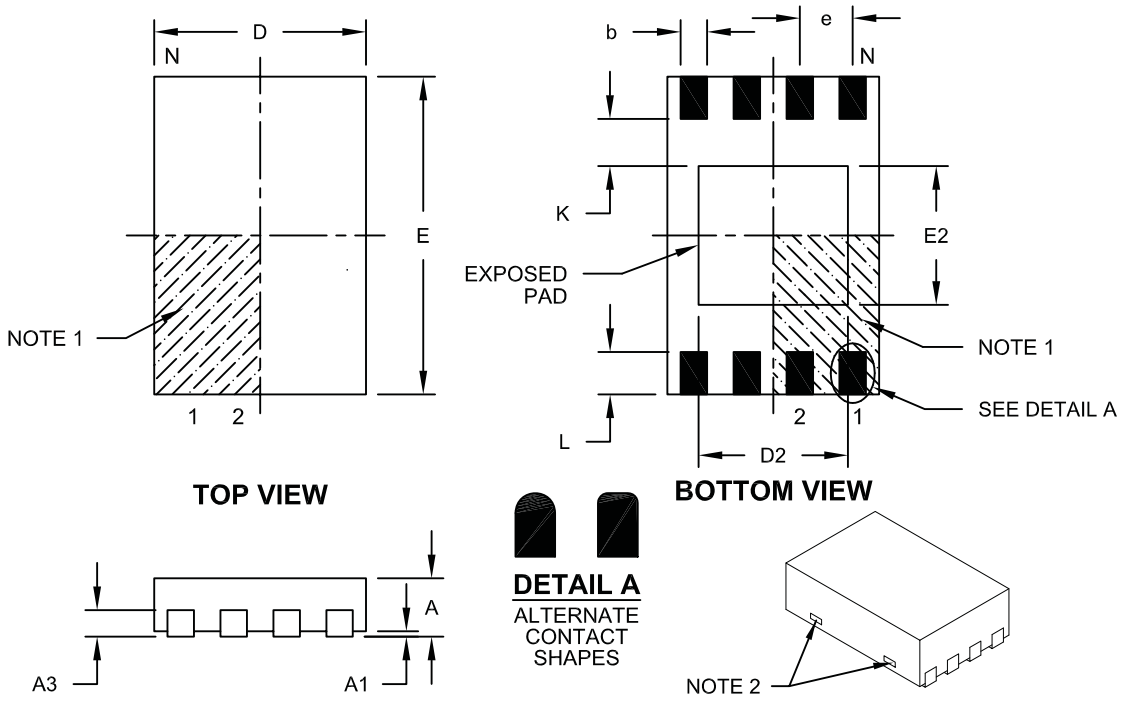
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Plastic Dual Flat, No Lead Package (MU) – 2x3x0.5 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1			0.07
Contact Thickness	A3		0.127 REF	
Overall Length	D	1.95	2.00	2.05
Overall Width	E	2.95	3.00	3.05
Exposed Pad Length	D2	1.30	1.40	1.50
Exposed Pad Width	E2	1.20	1.30	1.40
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.35
Contact-to-Exposed Pad	K		0.55 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

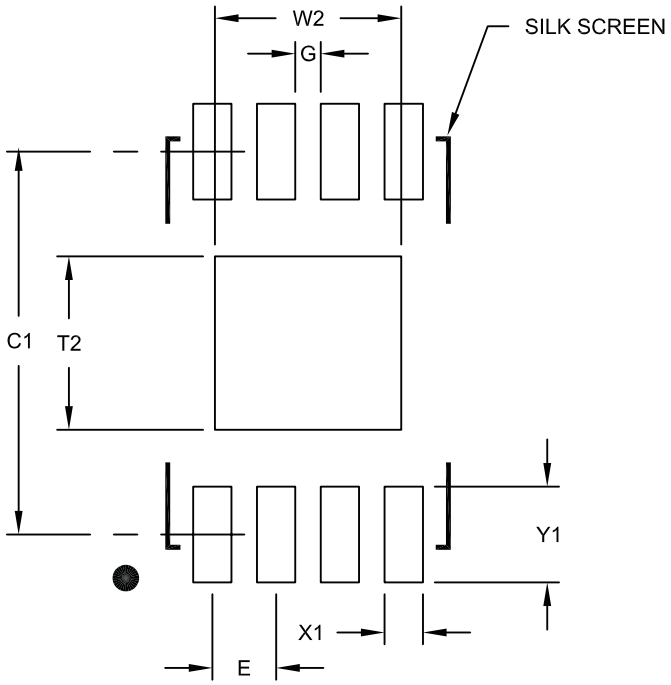
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-136B

8-Lead Plastic Dual Flat, No Lead Package (MU) – 2x3x0.5 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2136A

APPENDIX A: REVISION HISTORY

Revision A (06/2018)

Initial release of this document.

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PART NO.	[X] (1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	24CS512	=	I^2C-Compatible Serial EEPROM with 128-Bit Serial Number
Tape and Reel Option:	Blank	=	Standard Packaging (tube or tray)
	T	=	Tape and Reel(1)
Temperature Range:	I	=	-40°C to+85°C(Industrial)
Package:	MS	=	8-Lead Plastic Micro Small Outline Package
	P	=	8-Lead Plastic Dual In-Line – 300 mil Body
	SN	=	8-Lead Plastic Small Outline – Narrow, 3.90 mm Body
	SM	=	8-Lead Plastic Small Outline – Medium, 5.28 mm Body
	OT	=	5-Lead Plastic Small Outline Transistor
	ST	=	8-Lead Plastic Thin Shrink Small Outline – 4.4 mm Body
	MUY	=	8-Lead Plastic Dual Flat, No Lead Package – 2x3x0.5 mm
	CS0668	=	8-Ball Extremely Thin Fine Pitch Wafer Level Chip Scale Package

Examples:

a) 24CS512T-I/MS = Tape and Reel, Industrial Temp., 1.7V-5.5V, MSOP Package.

b) 24CS512-I/P = Industrial Temp., 1.7V-5.5V, PDIP Package

c) 24CS512T-I/SN = Tape and Reel, Industrial Temp., 1.7V-5.5V, SOIC Package.

d) 24CS512T-I/SM = Tape and Reel, Industrial Temp., 1.7V-5.5V, SOIJ Package.

e) 24CS512T-I/OT = Tape and Reel, Industrial Temp., 1.7V-5.5V, SOT-23 Package.

f) 24CS512-I/ST = Industrial Temp., 1.7V-5.5V, TSSOP Package.

g) 24CS512T-I/MUY = Tape and Reel, Industrial Temp., 1.7V-5.5V, UDFN Package.

h) 24CS512T-I/CS0668 = Tape and Reel, Industrial Temp., 1.7V-5.5V, CSP Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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