Isolated, Constant Current LED Driver

Features

- Programmable true constant current operation
- ±3% LED current accuracy
- Adaptive to external component tolerances and parasitics
- Primary-side current sensing
- Output open circuit protection
- Output short circuit protection
- Input under voltage lockout
- PWM dimming / enable
- 280-400VDC input

Applications

- Lighting fixtures with 6-50W power range

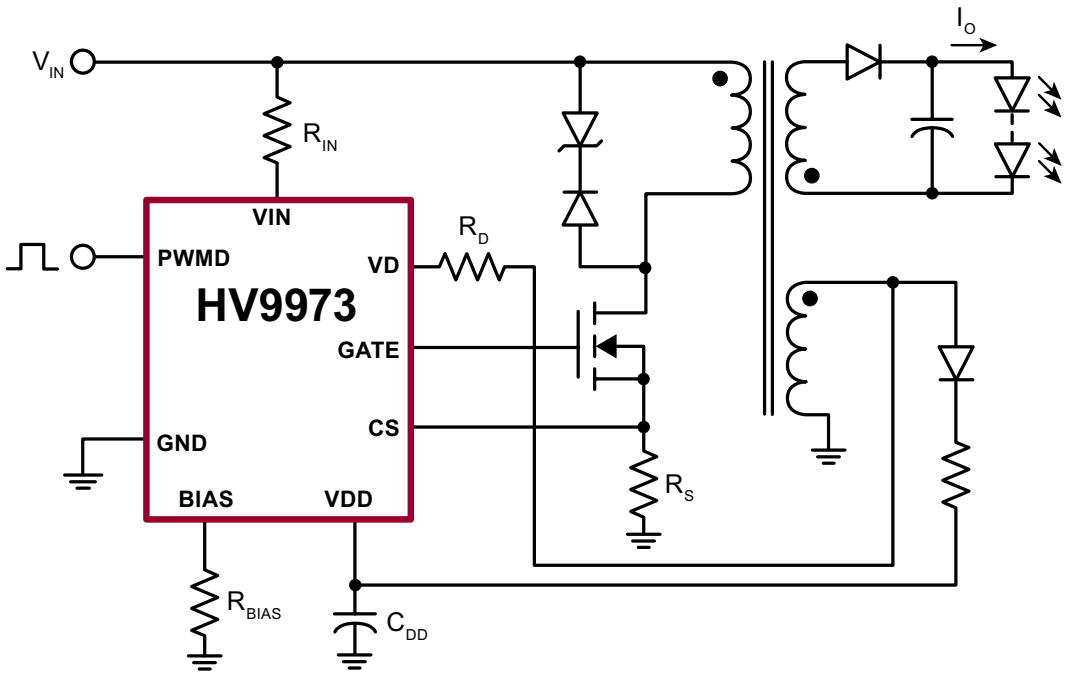
General Description

The HV9973 is a primary-side control IC for driving a discontinuous conduction mode (DCM) flyback LED driver. The IC is optimized for operation at a constant full-load switching frequency of 100kHz and the high input DC voltage range of 280-400VDC. It maintains 3% variation of the LED current setting, and features tight line and load regulation. The proprietary primary-side output current control employed in the HV9973 makes the output current setting insensitive to most component tolerances and parasitics without use of an opto-coupler feedback.

The HV9973 LED driver is fully protected against output open and short circuit conditions and input under-voltage. It also offers a logic input for dimming the LED light output by means of pulse-width modulation of the output current.

The HV9973 is ideally suited for driving high-brightness LEDs in low-power lighting fixtures such as incandescent bulb retrofits.

Typical Application Circuit

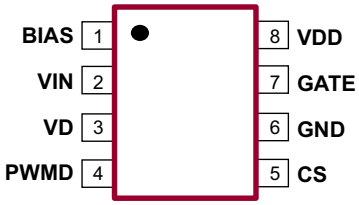


Ordering Information

Part Number	Package Option	Packing
HV9973LG-G	8-Lead SOIC	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Pin Configuration



8-Lead SOIC

Absolute Maximum Ratings*

Parameter	Value
VIN, VD, BIAS current	±5.0mA
VDD voltage	-0.3V to $VDD_{(SHUNT)}$
VDD current	10mA
GATE voltage	-0.3V to V_{DD} +0.3V
CS, PWMD voltage	-0.3V to 6.0V
Continuous power dissipation *(T_A = +25°C) (derate 6.3mW/°C above +25°C)*	630mW
Junction temperature	+125°C
Storage temperature range	-65°C to +150°C

** All voltages referenced to GND pin.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Product Marking

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC

Typical Thermal Resistance

Package	θ_{ja}
8-Lead SOIC	101°C/W

Electrical Characteristics

(Specifications are at T_A = 25°C, V_{DD} = 10V, I_{IN} = 200µA, C_{GATE} = 750pF, BIAS open, unless otherwise noted).

Sym	Description		Min	Typ	Max	Units	Conditions
Power Supply (VDD)							
$V_{DD(SHUNT)}$	Shunt voltage	*	10.50	11.00	11.50	V	---
$V_{DD(START)}$	Start voltage	*	9.95	10.50	11.45	V	V_{DD} rising
$V_{DD(STOP)}$	Under voltage threshold	*	6.65	7.00	7.70	V	V_{DD} falling
I_{DDQ}	Supply standby current	-	-	-	1.0	mA	Gate open
$I_{DDQ(START)}$	Start-up current	*	-	-	65	µA	V_{DD} = 10V

Notes:

* *Specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

† *Parameters guaranteed by design*

Electrical Characteristics

Sym	Description		Min	Typ	Max	Units	Conditions
Feed Forward Inputs (VD, VIN) and Oscillator							
I_{IN}	Operating current range	*	0	-	1000	µA	---
I_D	Operating current range	*	0	-	1000	µA	---
$\Delta Q_{IN(MAX)}$	V_{IN} Input charge swing	*†	-	-	395	pF	I_{IN} = 200µA, I_D = 0
K_{Osc}	Oscillator coefficient	*†	0.555	0.572	0.589	-	---
V_D	VD voltage	*	2.406	2.440	2.474	mV	---
$F_{S(START)}$	Start-up frequency	-	-	10	-	kHz	---
K_C	Effective integrator capacitance ratio V_{IN} to V_D	†	-	0.5	-	-	---
Bias Current Generator (BIAS)							
V_{BIAS}	Output voltage	*	1198	1220	1242	mV	---
GATE Output							
T_{RISE}	GATE output rise time	-	-	40	75	ns	---
T_{FALL}	GATE output fall time	-	-	20	40	ns	---
Current Sense Comparator							
$V_{CS(TH)}$	CS trip threshold	*	1198	1220	1242	mV	---
T_{DELAY}	Propagation delay CS to GATE	*	-	-	100	ns	(V_{CS} - $V_{CS(TH)}$) = 20mV
T_{BLANK}	Leading edge blanking delay	*	200	300	400	ns	---
VIN Under Voltage Comparator							
$I_{IN(UVLO)}$	V_{IN} undervoltage threshold current	-	112	-	128	µA	V_{IN} falling
$\Delta I_{IN(UVLO)}$	V_{DD} undervoltage lockout hysteresis	-	-	20	-	µA	V_{IN} rising
Open Circuit Protection							
$I_{D(OV)}$	Output open circuit threshold	-	66.5	-	73.5	µA	---
PWM Dimming							
$V_{PWMD,HI}$	PWMD input high voltage	*	2.0	-	-	V	---
$V_{PWMD,LO}$	PWMD input low voltage	*	-	-	0.8	V	---
Effective Current Sense Reference Voltage							
V_{EFF}	Effective reference voltage	-	333	-	361	mV	I_{IN} = 162.5µA, I_D = 120µA, See Note 1.
$\Delta V_{EFF}/V_{EFF}$	I_{IN}, I_D regulation of V_{EFF}	†	-	3.0	-	%	125µA ≤I_{IN} ≤ 185µA, 40µA ≤I_D ≤ 120µA

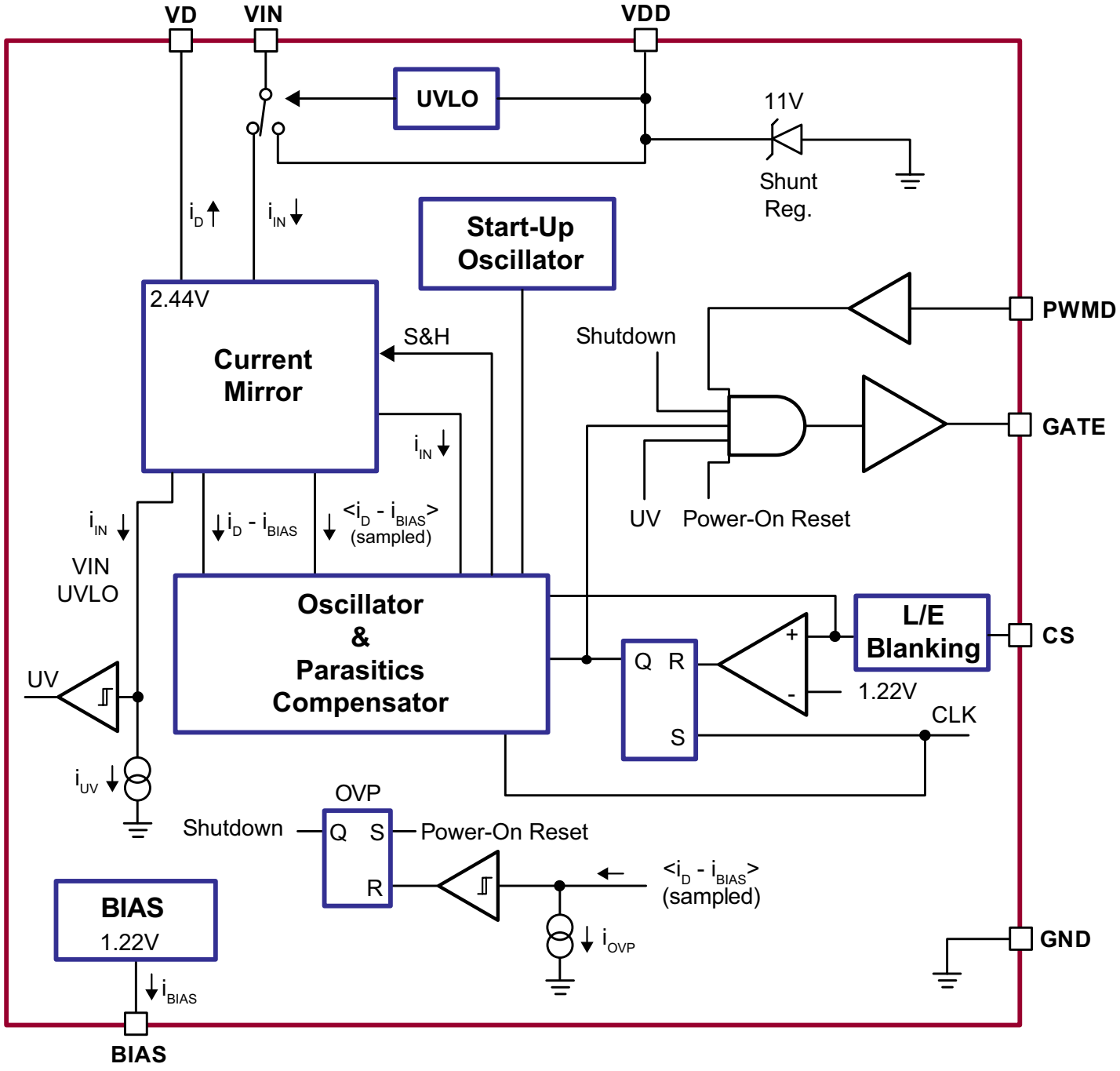
Notes:

* *specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

† *Parameters guaranteed by design.*

1. *Effective output current V_{EFF} = 0.5 • V_{CS} • K_{Osc}. Trimmed to the product of V_{CS} • K_{Osc}.*

Functional Block Diagram



Functional Description

Power Topology and Control Method

The HV9973 regulates the constant output current of a discontinuous conduction mode (DCM) flyback converter. Although it can be used in other applications, it is optimized for operating from a high DC line input voltage of 280-400VDC. The HV9973 is a fully integrated peak-current PWM controller IC. It does not require an optocoupler feedback, and includes protection from output open-circuit, short-circuit, and input under-voltage conditions. A proprietary control scheme permits accurate primary-side control of output current, insensitive to most circuit parasitics, external component tolerances and output voltage variation.

Output current of an HV9973 flyback converter can be expressed as:

$$I_O = \frac{I_{PK} \bullet n \bullet K_{Osc}}{2} \quad (1)$$

Where K_{Osc} = 0.572 is an oscillator coefficient, n is flyback transformer turns ratio of primary to secondary winding, and where I_{PK} is peak primary winding current given by:

$$I_{PK} = \frac{V_{CS(TH)}}{R_S} \quad (2)$$

In (2), $V_{CS(TH)}$ is the reference voltage of the current sense comparator at CS, and R_S is the current sense resistance.

Combining (1) and (2), we can write the output current as:

$$I_O = \frac{V_{CS(TH)} \bullet n \bullet K_{Osc}}{2 \bullet R_S} = \frac{n \bullet V_{EFF}}{R_S} \quad (3)$$

The effective reference voltage V_{EFF} = 347mV. Hence, the desired LED current is programmed by merely selecting the current sense resistor as:

$$R_S = \frac{n \bullet V_{EFF}}{I_O} \quad (4)$$

Note that the output current of the HV9973 LED driver is independent of the input and output voltage, the switching frequency or the transformer inductance.

The switching frequency at a given output voltage V_O can be estimated as:

$$F_S = \frac{n \bullet (V_O + V_F) \bullet K_{Osc}}{L_m \bullet I_{PK}} = \frac{V_{OR} \bullet K_{Osc}}{L_m \bullet I_{PK}} \quad (5)$$

where:

$$V_{OR} = n \bullet (V_O + V_F) \quad (6)$$

In the equation (5), L_m is magnetizing inductance of the transformer primary winding, and V_F is the forward voltage drop at the output rectifier diode. (Note that the switching frequency is not a function of the internal timing components of the HV9973 or the absolute value of R_{IN} and R_D).

Proper selection of maximum switching frequency $F_{S(MAX)}$ at full load, in combination with maximum $V_{OR(MAX)}$ is critical for proper operation of the HV9973. The oscillator circuit ramp may saturate when the maximum charge swing $\Delta Q_{IN(MAX)}$ = 400pC is exceeded at V_{IN}. Therefore, the circuit components should be selected such that:

$$\Delta Q_{IN} = \frac{V_{IN} \bullet T_{ON}}{R_{IN}} \le \Delta Q_{IN(MAX)} \quad (7)$$

Note, that the HV9973 is protected against incorrect oscillator setup. When saturation of the oscillator ramp occurs, the HV9973 shuts off and attempts to go through a start-up cycle again.

The transformer magnetic flux equals the volt-seconds at the transformer winding in the DCM flyback converter:

$$V_{IN} \bullet T_{ON} \approx L_M \bullet I_{PK} \quad (8)$$

Therefore, the charge swing ΔQ_{IN} varies only as a function of external component tolerances and circuit parasitic, and it is the same for all V_{IN} and V_O operating conditions. Combining equations (5), (7) and (8), and taking into consideration tolerances for L_m, R_S and $V_{CS(TH)}$, we get the following design criterion:

$$\frac{V_{OR(MAX)} \bullet K_{Osc(MAX)}}{F_{S(MAX)} \bullet R_{IN(MIN)}} \bullet \frac{L_{m(MAX)}}{L_{m(MIN)}} \bullet \frac{V_{CS(TH)MAX}}{V_{CS(TH)MIN}} \bullet \frac{R_{S(MAX)}}{R_{S(MIN)}} \le \Delta Q_{IN(MAX)} \quad (9)$$

The equation (9) gives the condition for selecting proper ratio of $V_{OR(max)}/F_{S(MAX)}$, which guarantees $\Delta Q_{IN} \le Q_{IN(MAX)}$. Selection of the resistor R_{IN} is dictated by the desired input under-voltage (UV). The recommended selection of R_{IN} = 2.0MΩ produces a UV shutdown at V_{IN} < 240VDC. As an example, we can assume the tolerances of L_m and R_S as ±10% and ±1% correspondingly. We shall also limit the switching frequency under $F_{S(MAX)}$ = 130KHz. With these assumption, the equation (9) gives $V_{OR(MAX)} \le$ 134.1V. Apparently, there

is also limitation on $V_{(OR)MAX}$ related to open circuit protection: $V_{(OR)MAX} < R_{IN(MIN)} \bullet I_{D(OV)MIN}$ (9A). In our case $V_{(OR)MAX} < 120.2V$ and the least of two values should be used. With some margin we should choose $V_{(OR)MAX} = 120V$.

The above example takes full advantage of the available V_{IN} input dynamic range, and, therefore, achieves the most accurate control over the LED current. For this reason, we will use $V_{OR(MAX)} = 120V$ and $F_{S(MAX)} = 130KHz$ in the following equations, as our recommended design inputs. Given, the primary-to-secondary turn ratio is determined simply as:

$$n = \frac{V_{OR(MAX)}}{(V_{O(MAX)} + V_F)} = \frac{120V}{(V_{O(MAX)} + V_F)} \quad (10)$$

The maximum magnetizing inductance of the primary winding $L_{m(MAX)}$ is obtained by combining the equations (2), (7) and (8):

$$L_{m(MAX)} = \frac{\Delta Q_{IN(MAX)} \bullet R_{IN(MIN)} \bullet R_{S(MIN)}}{V_{CS(TH)MAX}} \quad (11)$$

If we assume the primary inductance tolerance of ±10%, the nominal value of L_m is determined simply as:

$$L_m = \frac{L_{m(MAX)}}{1.1} \quad (12)$$

Selection of the maximum magnetizing inductance in accordance with (11) guarantees DCM operation in the entire working range of the input voltage with the proper selection of the input under-voltage and output over-voltage thresholds. *(See "Input Under-Voltage Protection" and "Output Open and Short Circuit Protection" below.)*

Due to presence of the leakage inductance L_{LK}, a voltage spike occurs at the primary winding of the transformer. Although the HV9973 eliminates the effect of the leakage inductance on the LED current, the duration of this spike should be minimized for best efficiency. The time t_{LK} is the leakage spike duration, determined by:

$$t_{LK} = \frac{L_{LK} \bullet I_{PK}}{V_Z - n \bullet (V_{O(MAX)} + V_F)} \quad (13)$$

Here, L_{LK} is primary winding leakage inductance, V_Z is the Zener clamp voltage. Hence, the Zener clamp voltage V_Z should be selected significantly higher than $n\bullet(V_{O(MAX)} + V_F)$. V_Z must also exceed the open-circuit protection threshold.

The HV9973 is powered by an internal shunt regulator, clamping VDD at $V_{DD(REG)} = 11V$. The IC shuts down when the voltage at VDD falls below $V_{DD(UV)} = 7.0V$. Under steady-state operation, the IC is powered by an auxiliary bootstrap winding through a ballast resistor R_{DD}. The primary-to-auxiliary winding turn ratio n_{AUX} and the value of R_{DD} should be selected carefully to ensure operation throughout the input and output voltage range with minimum power dissipation in R_{DD}. Note that the polarity of the auxiliary winding is opposite of the polarity of the secondary winding, such that the auxiliary winding voltage is positive during the on time. The following formulas are providing optimal values for n_{AUX} and R_{DD}, given the output voltage range $V_{O(MIN)}$, $V_{O(MAX)}$ and the input voltage range $V_{IN(MIN)}$, $V_{IN(MAX)}$:

$$n_{AUX} = \frac{V_{IN(MIN)} \bullet V_{IN(MAX)}}{2 \bullet V_{DD(UV)} \bullet V_{IN(MAX)} - V_{IN(MIN)} \bullet V_{DD(REG)}} \quad (14)$$

$$R_{DD} = \frac{\left(\frac{V_{DD(UV)}}{V_{IN(MIN)}} - \frac{V_{DD(REG)}}{V_{IN(MAX)}}\right) \bullet n \bullet (V_{O(MIN)} + V_F) \bullet K_{Osc}}{I_{DDQ} + Q_{GATE} \bullet \frac{(V_{O(MIN)} + V_F)}{(V_{O(MAX)} + V_F)} \bullet F_{S(MAX)}} \quad (15)$$

$$W_{DD} = \frac{\left(\frac{V_{IN(MAX)}}{n_{AUX}} - V_{DD(REG)}\right)^2 \bullet n \bullet (V_{O(MAX)} + V_F) \bullet K_{Osc}}{R_{DD} \bullet V_{IN(MAX)}} \quad (16)$$

where W_{DD} is power dissipation in R_{DD}, and I_{DDQ} is the quiescent current of the HV9973.

Start-Up

Upon applying the input AC power, the input current of VIN is diverted into the hold-up capacitor connected at VDD. The HV9973 consumes less than 60µA in this mode, and its GATE output is off. When a threshold of $V_{DD} = 10.5V$ is reached at VDD, VIN is disconnected from VDD, and the GATE output turns on. The GATE turns off upon reaching $V_{CS(TH)} = 1.22V$ at CS. The frequency of the GATE pulses is determined by the oscillator circuit or by the 10kHz start-up clock, whichever frequency is higher.

The hold-up capacitor connected at VDD must store enough energy to supply power to the HV9973 until adequate bootstrap power supply becomes available. The HV9973 stops switching and makes another attempt to charge the hold-up capacitor, if the voltage at VDD falls below 7.0V.

Although the resistor R_{IN} serves a different purpose in operation, its value must be selected with care to ensure the required 60µA start-up current at $V_{IN(MIN)}$.

Current Sense Comparator

The peak current comparator is using an external sense resistor R_S to compare the primary winding current to the reference voltage $V_{CS(TH)}$ = 1.22V. The corresponding peak current I_{PK} is given by equation (2). When the current in the primary winding exceeds I_{PK}, the comparator resets the PWM flip-flop circuit, and the output pulse is terminated. The next cycle begins upon receiving a clock signal from an internal oscillator circuit. A 300ns leading-edge blanking delay is applied to prevent false triggering of the current sense comparator.

Oscillator Circuit

Upon the end of the start-up cycle, the input current of V_{IN} is reverted to a current mirror circuit for generating the current i_{IN} in accordance with the following equation:

$$i_{IN} = \frac{V_{IN} - 1V}{R_{IN}} \approx \frac{V_{IN}}{R_{IN}} \quad (17)$$

Accordingly, the input current i_D is derived by connecting a resistor R_D from the bootstrap winding to V_D. However, since n_{AUX} >> 1 normally, the voltage V_{AUX} is much higer in comparison to the voltage at the VD pin (V_D = 2.44V). Hence, the current i_D through the resistor R_D can be expressed as:

$$i_D = \frac{V_D - V_{AUX}}{R_D} \quad (18)$$

From this equation, the current i_D is not directly proportional to V_{AUX}. The offset current is given by the following equation:

$$i_{OS} = \frac{V_D}{R_D} \quad (19)$$

The HV9973 cancels out this offset internally by subtracting a current of the same magnitude as i_{OS}. This correction current is programmed by connecting a resistor at the BIAS pin in accordance with:

$$i_{BIAS} = \frac{V_{BIAS}}{3.5 \bullet i_{OS}} \quad (20)$$

In (20), $V_{BIAS} = V_D/2$ is the voltage at the BIAS pin. Combining the equations (19) and (20) gives formula for calculating R_{BIAS} simply as:

$$R_{BIAS} = \frac{R_D}{7} \quad (21)$$

The resulting current $i_{OR} = (i_D - i_{OS})$ represents the instantaneous voltage across the transformer bootstrap winding:

$$i_{OR} = \frac{V_D - V_{AUX}}{R_D} - \frac{V_{BIAS}}{3.5 \bullet R_{BIAS}} = -\frac{V_{AUX}}{R_D} \quad (22)$$

Sampled during the conduction time of the transformer secondary winding, this current represents the reflected output voltage ($V_O + V_F$), where V_F is the voltage drop across the output rectified diode. The value of R_D should scale with R_{IN} in accordance with:

$$R_D = \frac{R_{IN} \bullet K_C \bullet k}{n_{AUX}} \quad (23)$$

In (23), k is the coupling coefficient between the primary and the bootstrap windings. The coupling coefficient can be determined by measuring the leakage inductance $L_{S(AUX)}$ of the auxiliary winding with respect to the primary winding and calculating it in accordance with the equation:

$$k = \sqrt{1 - \frac{L_{S(AUX)}}{L_{AUX}}} \quad (24)$$

Here, L_{AUX} is the bootstrap winding inductance. Since the value of the k is normally very close to 1, then k = 1 could be used as a first approximation.

With proper selection of the resistor R_D in accordance with (23), the oscillator circuit then generates switching frequency:

$$F_S = \frac{n \bullet (V_O + V_F) \bullet K_{Osc} \bullet R_S}{L_m \bullet V_{CS(TH)}} \quad (25)$$

Output Open and Short Circuit Protection

The HV9973 provides a very reliable open circuit protection. If the sampled current i_{OR} exceeds the 140µA threshold, the HV9973 is forced to go through a power-up cycle again. The corresponding output voltage threshold can be calculated as:

$$V_{O(LIM)} = \frac{R_D \bullet n_{AUX}}{n} \bullet 66.5\mu A - V_F \quad (26)$$

Normal operation resumes when the adequate LED load is connected.

Output short circuit protection is inherent to the HV9973 since the switching frequency is directly proportional to the output voltage. Moreover, loss of output voltage is likely to cause insufficient bootstrap power at VDD, resulting in a “hiccup” operating mode and repetitive restart attempts.

Input Under-Voltage Protection

The GATE output of the HV9973 becomes inhibited when the input current at VIN falls below 120µA. The GATE output is enabled again when the VIN current exceeds 140µA. The corresponding input under-voltage thresholds can be calculated as:

$$V_{IN(STOP)} = R_{IN} \bullet 120\mu A \quad (27)$$

$$V_{IN(START)} = R_{IN} \bullet 140\mu A \quad (28)$$

R-C Snubber Design Considerations

Detection of t_{LK} given by the equation (13) is crucial for proper operation of the HV9973. Upon the turn-off of the switching MOSFET, the voltage spike caused by the transformer leakage inductance is followed by high-frequency oscillation. The oscillation occurs at the transformer windings with the period equal to $2\pi\sqrt{L_{LK} \bullet C_{OSS}}$, where C_{OSS} is the output capacitance of the MOSFET. This oscillation is damped naturally by copper and core losses of the transformer, and it subsides during conduction time of the secondary winding. However, extra damping is usually required. Insufficiently damped, the post-spike oscillation may adversely affect accuracy of the output current regulation as well as EMI performance of the LED driver.

Damping of the post-spike oscillation is achieved by connecting of a snubber network (R_{SN}, C_{SN}) across the switching MOSFET. Selection of the R_{SN} and C_{SN} values is based on achieving sufficient damping while minimizing the power losses in the snubber network. At the same time, the oscillation should not be over-damped, as this will prevent detection of t_{LK}.

We recommend the following choice of the snubber network components:

$$C_{SN} = C_{OSS} \quad (29)$$

$$R_{SN} = 1.6\sqrt{\frac{L_{LK}}{C_{SN}}} \quad (30)$$

Note that the output capacitance C_{OSS} is a nonlinear function of the drain voltage. Most datasheets give the C_{OSS} value at the drain voltage of V_{DS} = 25V. Typically, the output capacitance characteristic as a function of V_{DS} is provided in the MOSFET datasheet as well. The equation (29) should use the C_{OSS} value at $V_{DS} = (V_{IN(MIN)} + n \bullet V_{O(MIN)})$, or at the highest V_{DS} given in the plot, whichever voltage is lower.

Also note that the R-C snubber network must be connected between the drain and the source of the MOSFET, rather than being wired to ground or across the primary winding. Otherwise, the current from C_{SN} may cause false tripping of the CS comparator.

Power dissipation in R_{SN} can be estimated by the following formula:

$$W_{RSN} = C_{SN} \bullet V_{IN(MAX)}^2 \bullet F_{S(MAX)} \quad (31)$$

Layout Considerations

The signal inputs VIN and VD operate at relatively low input current ranging from hundreds down to tens of microamps. Therefore, proximity of the switching potential of the MOSFET drain can cause a displacement current in VD and VIN affecting the normal operation of the HV9973. Proper HV9973 PCB layout should avoid direct proximity of the VD and VIN inputs to the high-voltage switching potential.

The resistor R_D should be placed as close as possible to the VD input. Otherwise, a long VD trace can be susceptible to noise coupling, or it can introduce parasitic capacitance with respect to ground capable of distorting the VD input signal.

Design example

The following example illustrates LED driver design with HV9973 for the following conditions:

1. *Input: $V_{IN(MIN)}$ = 240V, $V_{IN(MAX)}$ = 375V*
2. *Output: $V_{O(MIN)}$ = 6.0V, $V_{O(MAX)}$ = 18V, V_F = 0.7V, I_O = 0.5A*
3. *Maximum switching frequency: $F_{S(MAX)}$ = 130kHz*
4. *$V_{IN(STOP)}$ = 240V*

Design:

1. Using formula (27), calculate value of the resistor R_{IN}:

$$R_{IN} = \frac{V_{IN(STOP)}}{120\mu A} = 2.0M\Omega$$

2. Using formula (9), calculate $V_{OR(MAX)}$:

$$V_{OR} = \frac{\Delta Q_{IN(MAX)} \bullet F_{S(MAX)} \bullet R_{IN}}{K_{Osc(MAX)}} \bullet 77.6\% = 134.1V$$

Using formula (9A), calculate $V_{(OR)MAX}$ base on OV protection:

$$V_{OR} = R_{IN(MIN)} \bullet I_{D(OV)MIN} = 131.7V$$

Choose $V_{(OR)MAX}$ = 120V based on 8 - 10% margin from lower value.

3. Using formula (10), calculate primary-to-secondary turns ratio of the flyback transformer:

$$n = \frac{V_{OR(MAX)}}{(V_{O(MAX)} + V_F)} = \frac{115V}{(V_{O(MAX)} + V_F)} = 6.353$$

4. Using formula (4), calculate value of the current sense resistor:

$$R_S = \frac{n \cdot V_{EFF}}{I_O} = 4.47\Omega$$

5. Using formula (2), calculate value of the maximum peak current:

$$I_{PK(MAX)} = \frac{V_{CS(TH)MAX}}{R_{S(MIN)}} = \frac{V_{CS(TH)MAX}}{0.99 \cdot R_S} = 0.277A$$

6. Using formula (11), calculate maximum value of the magnetizing inductance:

$$L_m = \frac{L_{m(MAX)}}{110\%} = \frac{\Delta Q_{IN(MAX)} \cdot 0.99R_{IN} \cdot 0.99R_S}{V_{CS(TH)MAX} \cdot 110\%} = 2.564\mu H$$

7. Using formula (14), calculate turns ratio primary-to-auxiliary winding of the flyback transformer:

$$n_{AUX} = \frac{V_{IN(MIN)} \cdot V_{IN(MAX)}}{2 \cdot V_{DD(UV)} \cdot V_{IN(MAX)} - V_{IN(MIN)} \cdot V_{DD(REG)}} = 6.72$$

8. Using formulas (21) and (23), calculate values of the resistors R_D, R_{BIAS}:

$$R_D = \frac{R_{IN}}{n_{AUX}} = 38.9k\Omega$$

$$R_{BIAS} = \frac{R_D}{7} = 5.56k\Omega$$

9. Using formula (15), calculate value of the resistor R_{DD}:

$$R_{DD} = \frac{\left(\frac{V_{DD(UV)}}{V_{IN(MIN)}} - \frac{V_{DD(REG)}}{V_{IN(MAX)}}\right) \cdot n \cdot (V_{O(MIN)} + V_F) \cdot K_{Osc(MAX)}}{I_{DDQ} + Q_{GATE} \cdot \frac{(V_{O(MIN)} + V_F)}{(V_{O(MAX)} + V_F)} \cdot F_{S(MAX)}} = 62.0\Omega$$

(We have assumed Q_{GATE} = 15nC and $V_{DD(MIN)}$ = 8V to account for the forward voltage drop at the bootstrap winding diode.)

10. Using formula (18), calculate the maximum power dissipation W_{DD} in the resistor R_{DD}:

$$W_{DD} = \frac{\left(\frac{V_{IN(MAX)}}{n_{AUX}} - V_{DD(REG)}\right)^2 \cdot n \cdot (V_{O(MAX)} + V_F) \cdot K_{Osc(MAX)}}{R_{DD} \cdot V_{IN(MAX)}} = 0.028W$$

11. Using formula (30), calculate the resistor R_{SN}. Assume C_{OSS} = 33pF (IRFUC20, 600V, 1A MOSFET), L_{LK} = 20µH:

$C_{SN} = 33pF$

$$R_{SN} = 1.6\sqrt{\frac{L_{LK}}{C_{SN}}} = 1.25k\,\Omega$$

12. Using formula (30), calculate the maximum power dissipation W_{RSN} in the resistor R_{SN}:

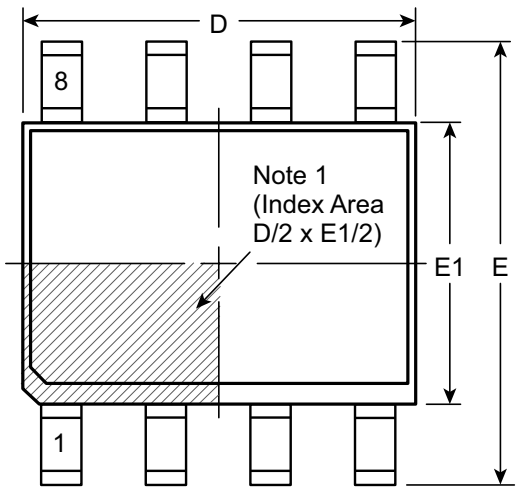
$$W_{RSN} = C_{SN} \cdot V_{IN(MAX)}^2 \cdot F_{S(MAX)} = 0.6W$$

Pin Description

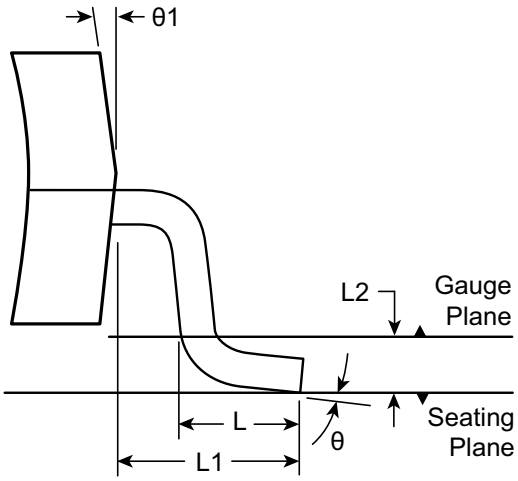
Pin #	Function	Description
1	BIAS	This pin is used for generating a correction current to account for the 2.44V offset at VD. Connect a resistor to ground to program.
2	VIN	This pin is the input voltage feed forward input. Connect a resistor from this pin to the input side of the primary winding of the transformer to program the VIN current. The same resistor is also used for start-up upon initial application of power.
3	VD	This pin is the auxiliary winding feedback input. Connect a resistor from this pin to the transformer bootstrap winding.
4	PWMD	When this pin is pulled to GND, switching of the HV9971 is disabled. When the PWM pin is released, or external TTL high level is applied to it, switching will resume.
5	CS	This pin is for sensing peak output voltage at an external current sense resistor.
6	GND	This pin is the common return for all the internal circuits.
7	GATE	This pin is the output gate driver for an external N-channel power MOSFET.
8	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND. The capacitor must be able to store sufficient energy for starting up the converter.

8-Lead SOIC (Narrow Body) Package Outline (LG)

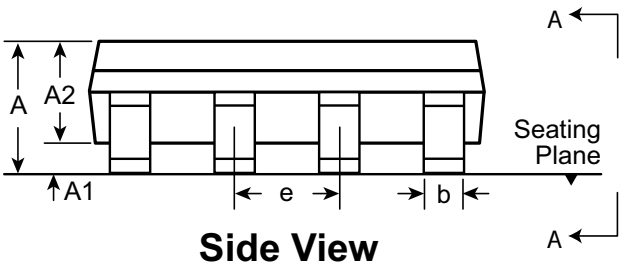
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



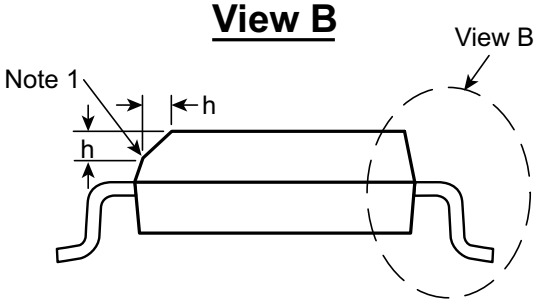
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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