



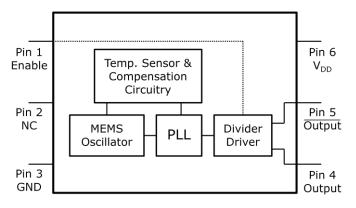
Programmable Low-Jitter Precision LVPECL Oscillator

General Description

The DSC8102 & DSC8122 series of high performance field-programmable oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a of supply voltages wide range Using temperatures. the TIMEFLASH programmer, the end user can easily program the oscillators' frequency in the field for immediate testing or use in advance prototype development or production.

DSC8102 has a standby feature allowing it to completely power-down when EN pin is pulled low; whereas for DSC8122, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 3.2x2.5 mm², and are "drop-in" replacement for standard 6-pin LVPECL quartz oscillators.

Block Diagram



Output Enable Modes

	EN Pin	DSC8102	DSC8122			
	High Outputs Active NC Outputs Active Low Standby		Outputs Active			
			Outputs Active			
			Outputs Disabled			

Features

- Low RMS Phase Jitter: <1 ps (typ)
- High Stability: ±10, ±25, ±50 ppm
- Wide Temperature Range
 - o Industrial: -40° to 85° C
 - Ext. commercial: -20° to 70° C
- High Supply Noise Rejection: -50 dBc
- Wide Freq. Range: 10 to 460 MHz
- Small Industry Standard Footprints o 2.5x2.0, 3.2x2.5, 5.0x3.2, & 7.0x5.0 mm
- Excellent Shock & Vibration Immunity
 - Qualified to MIL-STD-883
- High Reliability
 - o 20x better MTF than quartz oscillators
- Low Current Consumption
- Supply Range of 2.25 to 3.6 V
- Standby & Output Enable Function
- Lead Free & RoHS Compliant
- LVDS & HCSL Versions Available

Applications

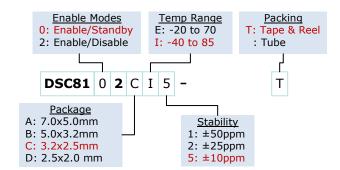
- Storage Area Networks
 - SATA, SAS, Fibre Channel
- Passive Optical Networks
 - o EPON, 10G-EPON, GPON, 10G-PON
- Ethernet
 - o 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express: Gen 1 & Gen 2
- DisplayPort



Absolute Maximum Ratings

Item	Min	Max	Unit	Condition		
Supply Voltage	-0.3	+4.0	V			
Input Voltage	-0.3	V _{DD} +0.3	V			
Junction Temp	-	+150	°C			
Storage Temp	-55	+150	°C			
Soldering Temp	-	+260	°C	40sec max.		
ESD	-		V			
НВМ		4000				
MM		400				
CDM		1500				
Note: 1000+ years of data retention on internal memory						

Ordering Code



Specifications

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage ¹	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled DSC8102 DSC8122		20	0.095 22	mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time ²	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	V_{IH}		0.75xV _{DD}		- 0.25xV _{DD}	V
Output Disable Time ³	t_DA				5	ns
Output Enable Time	t _{EN}	DSC8102 DSC8122			5 20	ms ns
Enable Pull-Up Resistor ⁴		Pull-up resistor exist		40		kΩ
		LVPECL Outputs				
Supply Current	I_{DD}	Output Enabled, $R_L=50\Omega$		56.5	58	mA
Output Logic Levels Output logic high Output logic low	V _{OH} V _{OL}	$R_L = 50\Omega$	V _{DD} -1.08		- V _{DD} -1.55	V
Pk to Pk Output Swing		Single-Ended		800		mV
Output Transition time ³ Rise Time Fall Time	t _R t _F	20% to 80% $R_L = 50\Omega$, $C_L = 0$ pF		250		ps
Frequency	f_0	Single Frequency	10		460	MHz
Output Duty Cycle SYN		Differential	48		52	%
Period Jitter	J_{PER}			2.5		ps _{RMS}
Integrated Phase Noise	$J_{ ext{PH}}$	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	2	ps _{RMS}

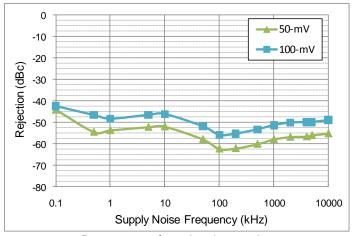
Notes:

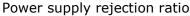
- 1. 2. 3. Pin 6 V_{DD} should be filtered with 0.1uf capacitor.
- t_{su} is time to 100ppm of output frequency after V_{DD} is applied and outputs are enabled. Output Waveform and Test Circuit figures below define the parameters.
- Output is enabled if pad is floated or not connected.

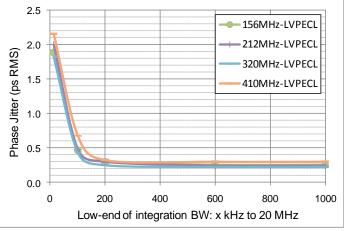
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Nominal Performance Parameters (Unless specified otherwise: T=25° C, V_{DD}=3.3 V)

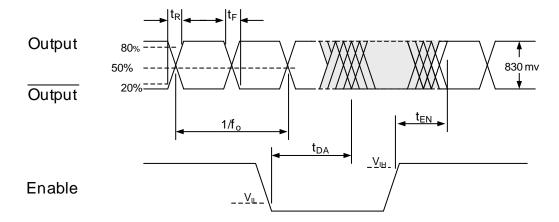




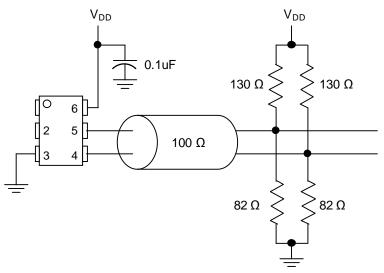


Phase jitter (integrated phase noise)

Output Waveform



Typical Termination Scheme

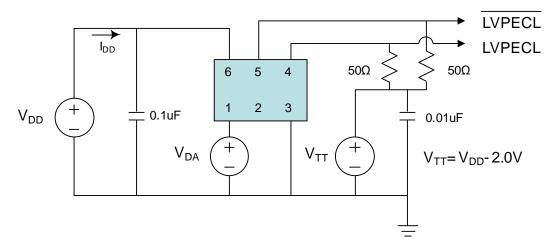


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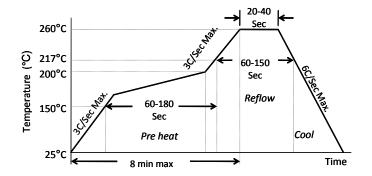
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Test Circuit



Solder Reflow Profile



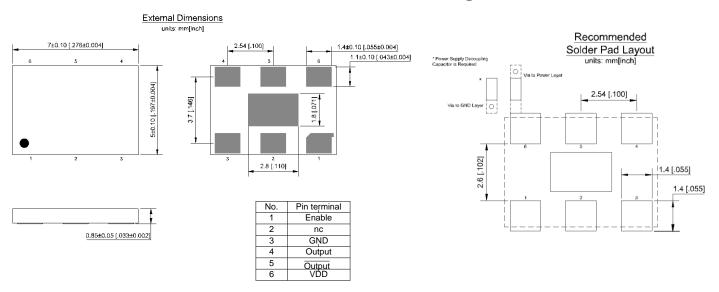
MSL 1 @ 260°C refer to JSTD-020C						
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.					
Preheat Time 150°C to 200°C	60-180 Sec					
Time maintained above 217°C	60-150 Sec					
Peak Temperature	255-260°C					
Time within 5°C of actual Peak	20-40 Sec					
Ramp-Down Rate	6°C/Sec Max.					
Time 25°C to Peak Temperature	8 min Max.					

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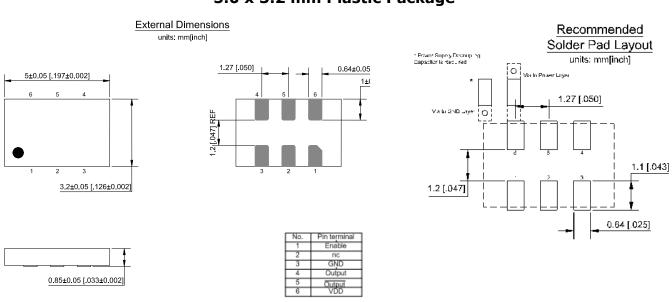


Package Dimensions

7.0 x 5.0 mm Plastic Package



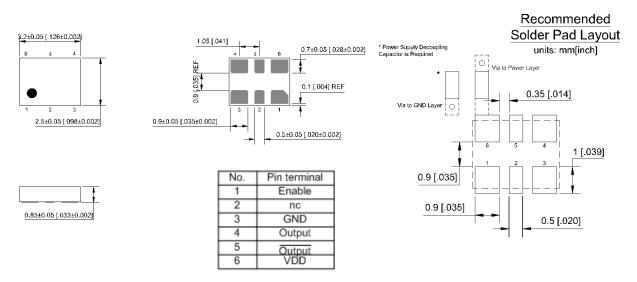
5.0 x 3.2 mm Plastic Package



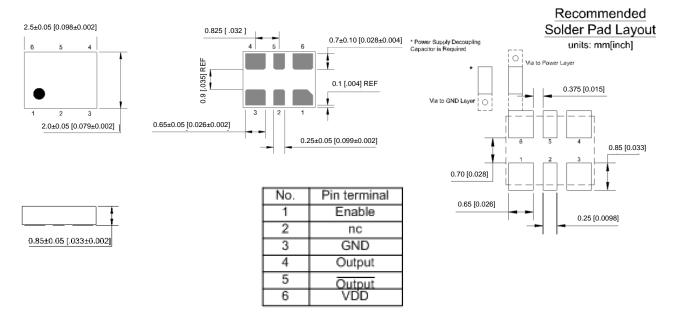


3.2 x 2.5 mm Plastic Package





2.5 x 2.0 mm Plastic Package



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