SY75572L

267MHz 1:2 3.3V HCSL/LVDS Fanout Buffer

PrecisionEdge™

General Description

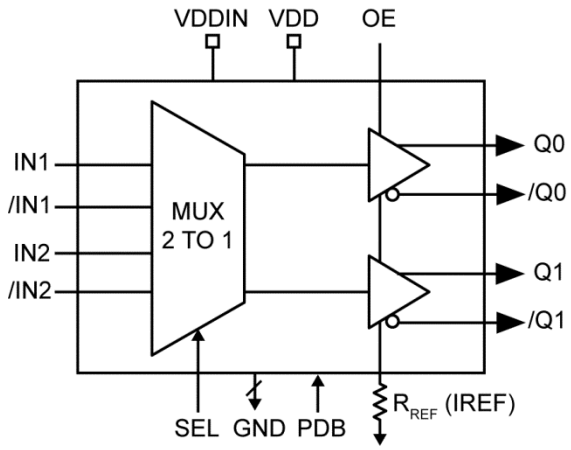
The SY75572L is a high-speed, fully differential 1:2 clock fanout buffer with a 2:1 input MUX optimized to provide two identical output copies with 137fs phase jitter and a maximum of 50ps output-to-output skew. Designed to be used with PCI Express applications, the SY75572L accepts and outputs HCSL or LVDS logic levels.

The SY75572L operates from a 3.3V ±5% power supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). It is available in a 16-pin QFN lead-free package.

The SY75572L is part of Micrel's high-speed, ultra-low jitter, PrecisionEdge™ product line. The SY75572L supports PCIe Gen1-Gen3 requirements with sufficient performance margin for pending PCIe Gen4 applications.

Datasheets and support documentation are available on Micrel's website at: www.micrel.com.

Functional Block Diagram



Features

- Two differential pairs of LVDS or HCSL outputs
- Two pairs of differential inputs accept LVDS or HCSL logic levels
- 267MHz maximum frequency
- Ultra-low phase jitter:
  - 137fs_{RMS}, 200MHz (12kHz–20MHz)
  - 153fs_{RMS}, 156.25MHz (12kHz–20MHz)
  - 212fs_{RMS}, 100MHz (12kHz–20MHz)
- <2ps total jitter (peak-to-peak), 200MHz (BER = 10^{-12})
- 50ps output-to-output skew
- 3.3V ±5% power supply operation
- –40°C to +85°C operating temperature
- Available in 16-pin (3mm × 3mm) QFN lead-free package

Applications

- Blade servers
- Desktop servers
- Workstations
- Storage area networks
- IP routers and switches
- Telecom and datacom
- High performance computing

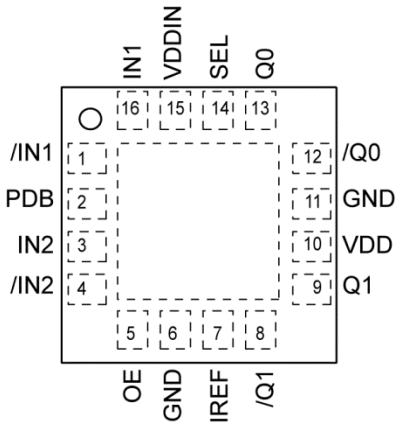
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY75572LMG	QFN-16	Industrial	572L with Pb-Free bar-line indicator	NiPdAu
SY75572LMG TR[2]	QFN-16	Industrial	572L with Pb-Free bar-line indicator	NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and reel.

Pin Configuration



16-Pin QFN

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Pin Description

Pin Number	Pin Name	Pin Function
1	/IN1	HCSL/LVDS inverted input 1.
2	PDB	PDB = 0 powers down the chip and tri-states outputs. The pin is attached to an internal pull-up resistor.
3	IN2	HCSL/LVDS input 2.
4	/IN2	HCSL/LVDS inverted input 2.
5	OE	Tri-state outputs. High = enable outputs. Low = disable outputs. Internal pull-up resistor, outputs are enabled by default.
6	GND	Ground.
7	IREF	External resistor R_{REF} between pin IREF and GND controls reference current.
8	/Q1	Inverted Output 1.
9	Q1	Non-inverted Output 1.
10	VDD	3.3V power supply.
11	GND	Ground.
12	/Q0	Inverted Output 0.
13	Q0	Non-inverted Output 0.
14	SEL	SEL = 0 propagates IN2, /IN2 to outputs. SEL = 1 propagates IN1, /IN1 to outputs. Internal pull-up resistors, IN1, /IN1 is selected by default.
15	VDDIN	3.3V power supply.
16	IN1	HCSL/LVDS input 1.

Absolute Maximum Ratings[3]

Supply Voltage (V_{DD}, V_{DDIN}) 5.5V
Input Voltage (V_{IN}) ..... –0.5V to V_{DDIN} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Maximum Junction Temperature ..... 125°C
Storage Temperature (T_s) ..... –65°C to +150°C
ESD Protection (input) ..... 2000V min.

Operating Ratings[4]

Supply Voltage (V_{DD}, V_{DDIN}) ..... 3.135V to 3.465V
Ambient Op Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[5]
QFN-16
Still-air (θ_{JA}) ..... 59°C/W
Junction-to-board (ψ_{JB}) ..... 38°C/W

DC Electrical Characteristics[6]

V_{DD} = V_{DDIN} = 3.135V to 3.465V, T_A = –40°C to +85°C, unless otherwise stated. R_{REF} = 475Ω

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDIN}	Power Supply Voltage Range		3.135	3.3	3.465	V
C_{IN}	Input Capacitance				6	pF
C_{OUT}	Output Capacitance				5	pF
L_{PIN}	Pin Inductance				4	nH
R_{OUT}	Output Resistance		3			kΩ
$R_{PULL-UP}$	Pull up Resistance	SEL, PDB, OE		110		kΩ
V_{IH}	Input High Voltage	SEL, PDB, OE	2		V_{DDIN} + 0.3	V
V_{IL}	Input Low Voltage	SEL, PDB, OE	–0.3		0.8	V
V_{IH}	Input High Voltage	HCSL, IN, /IN	660	750	850	V
V_{IL}	Input Low Voltage	HCSL, IN, /IN	–150	0		V
V_{IN}	Differential Input Voltage Range	LVDS, IN, /IN	250	350	550	mV
$V_{INPUT\ OFFSET}$	Input Common Mode Voltage	LVDS, IN, /IN,	1.125	1.25	1.375	V
V_{OH}	Output High Voltage	HSCL	660	750	850	mV
V_{OL}	Output Low Voltage	HSCL	–150	0	27	mV
V_{CROSS}[7, 8]	Crossing Point Voltage	Absolute	250	350	550	mV
$V_{CROSS\_VARIATION}$[7, 8, 9]	Variation of Crossing Point Voltage	Variation over all edges			140	mV
I_{DD}	Power Supply Current For V_{DD} + V_{DDIN}	50Ω, 2pF		42	60	mA
		No load, PDB = Low			0.4	mA
		OE = Logic Low			20	mA
I_{IL}[10]	Input Leakage Current	0 < V_{IN} < V_{DDIN}	–5		5	µA

Notes:

3. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
4. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
5. Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air unless otherwise stated. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
7. Test setup is R_L = 50Ω with 2pF, R_{REF} = 475Ω ±1%.
8. Measurement taken from Q and /Q.
9. Measured at the crossing point where instantaneous voltages of Q and /Q are equal.
10. Inputs with pull-up/pull-down resistances are not included.

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AC Electrical Characteristics[6]

V_{DD} = V_{DDIN} = 3.135V to 3.465V, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Frequency	HCSL			267	MHz
		LVDS			100	
t_{PD}	Propagation Delay	Note 11		2	3	ns
t_{SKEW}	Output-to-Output skew	Notes 12, 13			50	ps
t_r, t_f	Output Rise/Fall Times 0.175V to 0.525V / 0.525V to 0.175V	At full output swing. 50Ω, 2pF	150	350	700	ps
T_{r/f_VAR}	Rise/Fall Time Variation	At full output swing. 50Ω, 2pF			125	ps
T_{JITTER}	Phase Jitter	At 200MHz		137		fs_{rms}
		At 156.25MHz		153		fs_{rms}
		At 100MHz		212		fs_{rms}
T_{TJ_JITTER}	Total Jitter	BER = 10^{-12}, T_{DJ} = 0, at 200MHz		2		ps
T_{OE_ENABLE}	Output Enable Time	All Outputs		2		µs
$T_{OE\_DISABLE}$	Output Disable Time	All Outputs		10		ns
T_{DCY}	Duty Cycle		45	50	55	%

Notes:

11. Measured from the differential input crossing point to the differential output crossing point.
12. Output-to-output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage, and transition.
13. This parameter is defined in accordance with JEDEC Standard 65.

Jitter Analysis

Jitter is defined as the deviation of a signal from its ideal position. Phase noise is the presence of signal energy at frequencies other than the carrier. Random jitter has a Gaussian distribution and is specified as an RMS unit, which is one standard deviation of the distribution. Since Gaussian distribution is unbounded in an infinite sample, no communication system can be completely error free. Instead, communication links are rated with a maximum bit error rate (BER), which is typically around 10^{-12} for high-speed communication equipment. Achieving a desired BER requires accounting for a number of standard deviations of random noise by using the appropriate value for N (see Table 1) in the formula in Equation 1.

$$T_J = N \times R_J + D_J \quad \text{Eq. 1}$$

Where T_J is total jitter, R_J is random jitter, and D_J is deterministic jitter. If routing clock signals, the deterministic jitter is usually negligible and the T_J is dominated by the random jitter. Calculating T_J from R_J using Equation 1 gives the values in Table 1.

Table 1. Standard Deviations of Random Noise

BER	N	R_j at 200MHz	T_j at 200MHz
10^{-10}	12.723	$137fs_{RMS}$	1.743ps
10^{-11}	13.412	$137fs_{RMS}$	1.837ps
10^{-12}	14.069	$137fs_{RMS}$	1.927ps
10^{-13}	14.698	$137fs_{RMS}$	2.013ps

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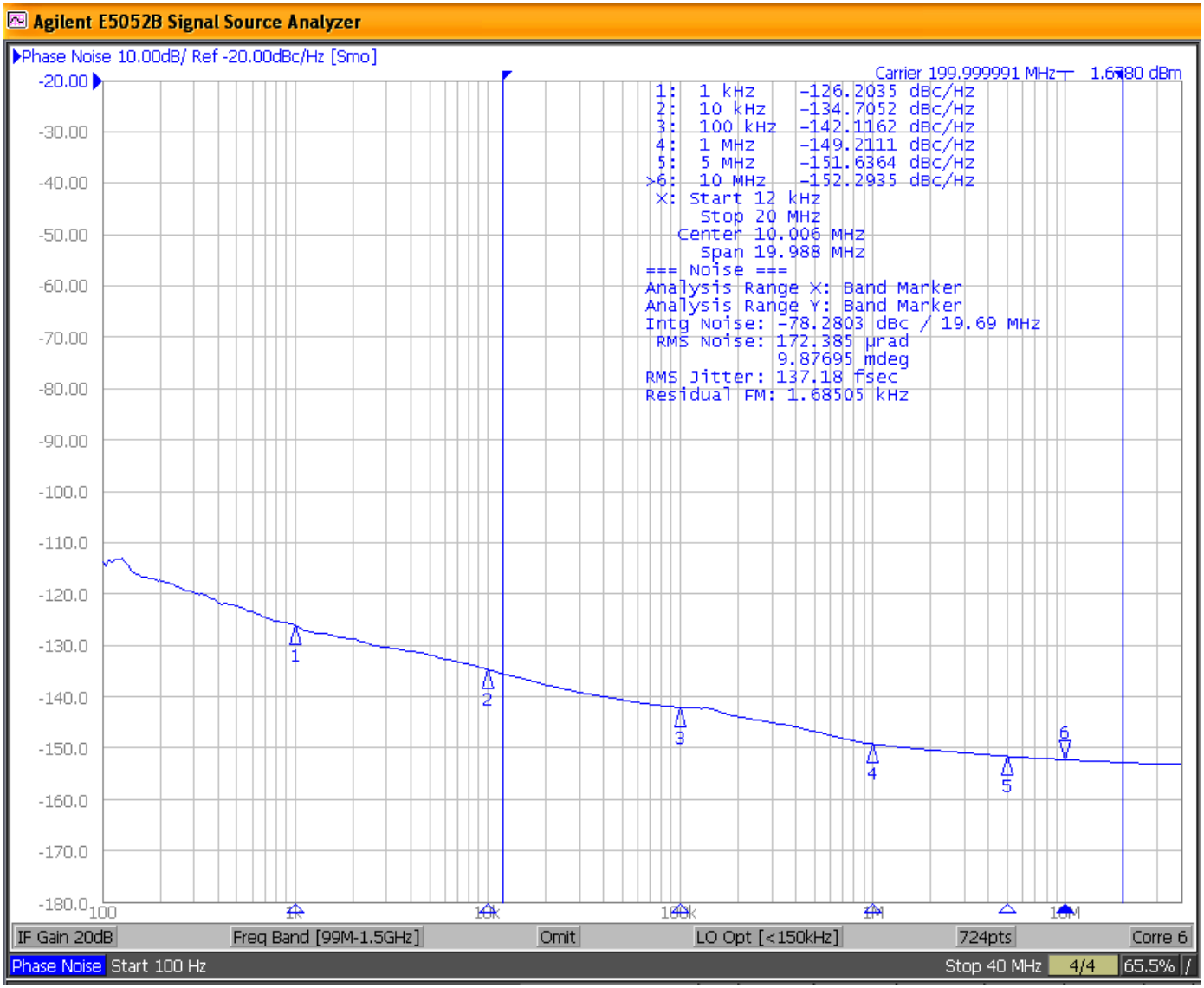
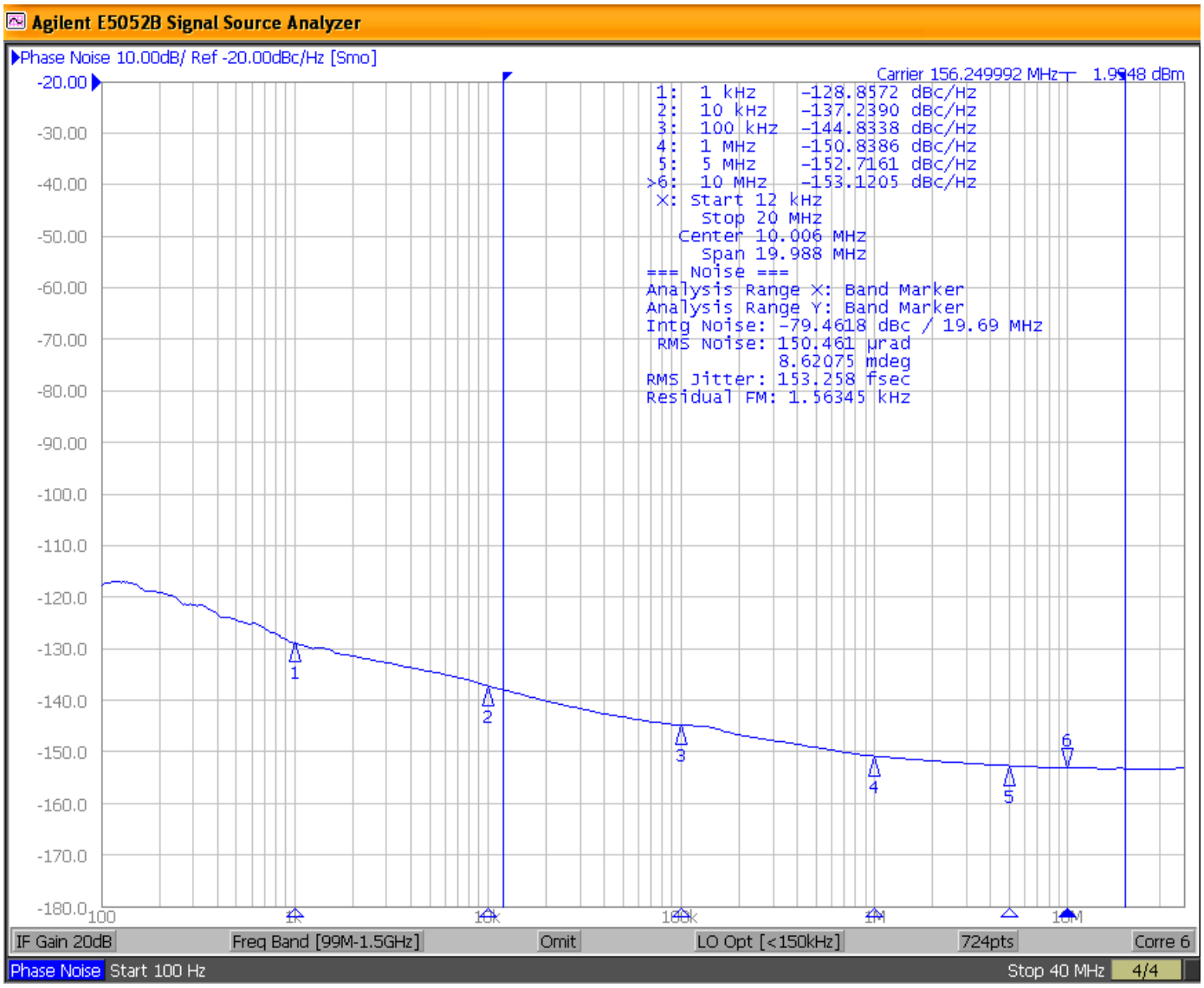
Phase Noise Plots



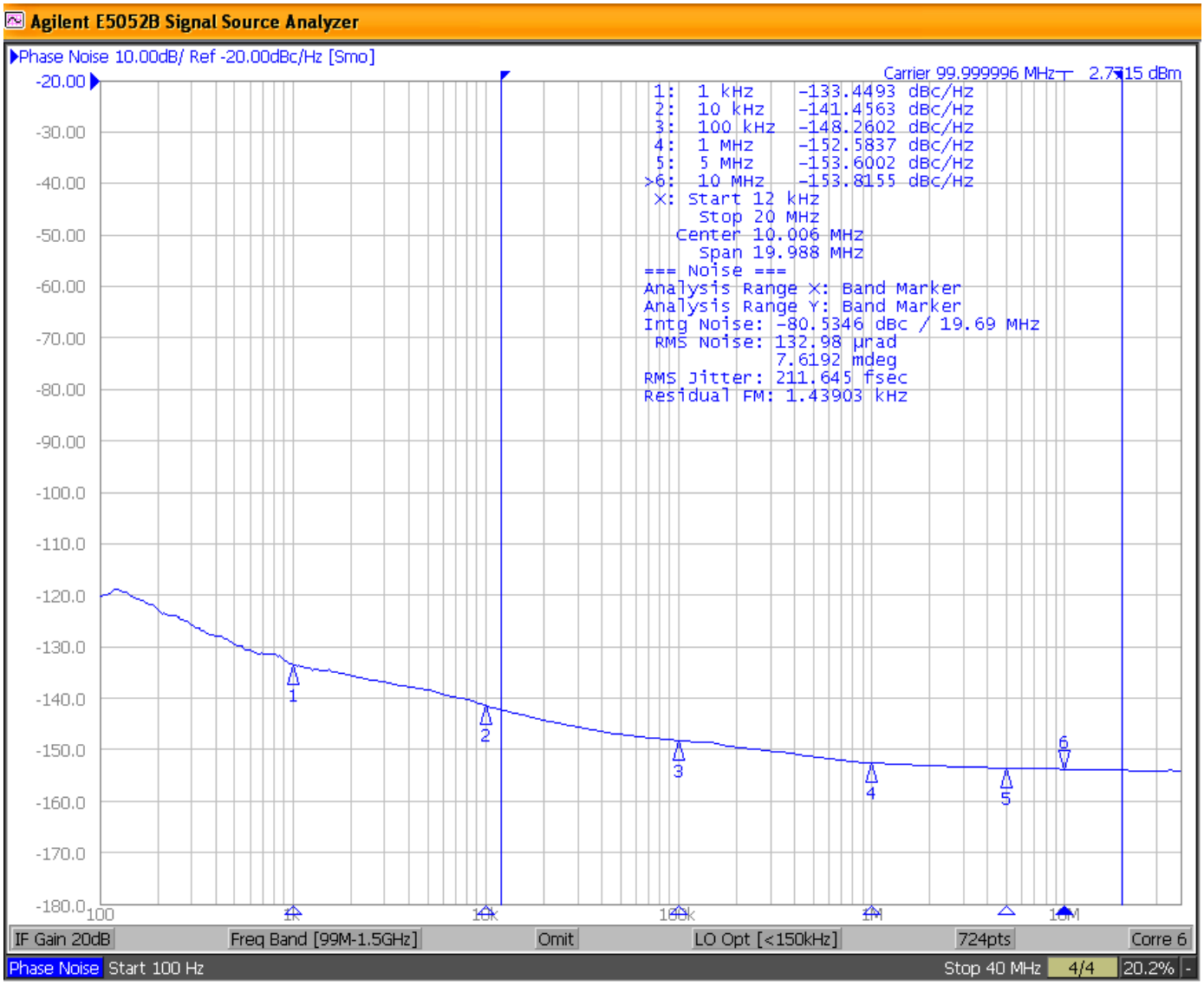
Phase jitter = 137fs$_{RMS}$, 200MHz carrier frequency; integration range: 12kHz–20MHz

Phase Noise Plots (Continued)



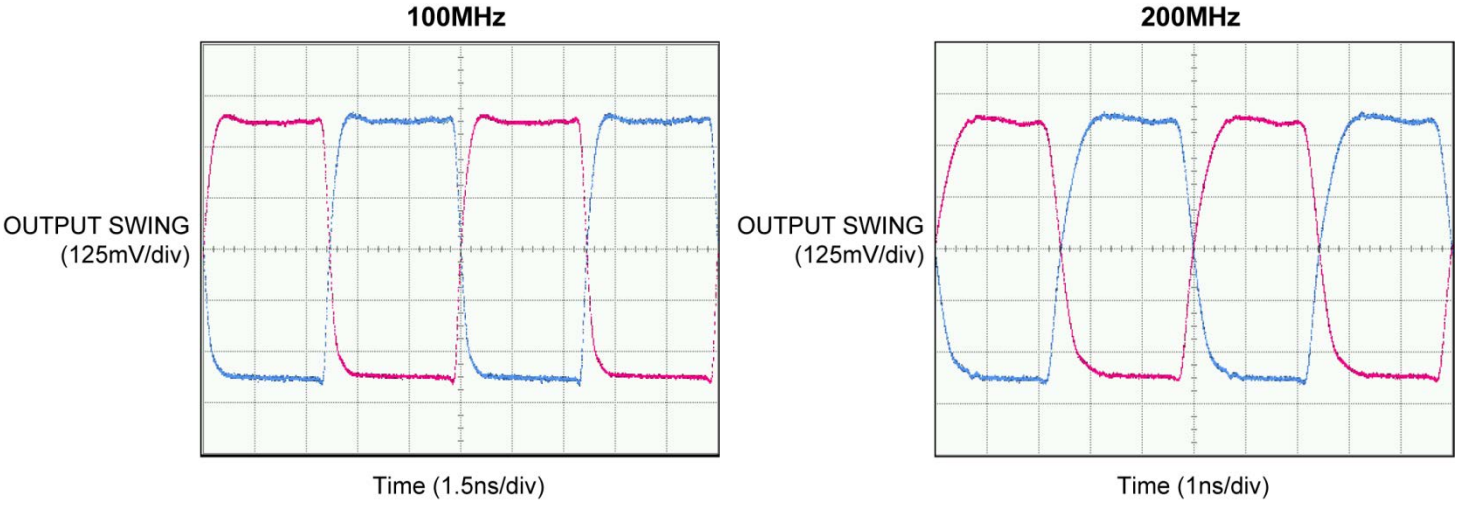
Phase jitter = 153fs$_{RMS}$, 156.25MHz carrier frequency; integration range: 12kHz–20MHz

Phase Noise Plots (Continued)

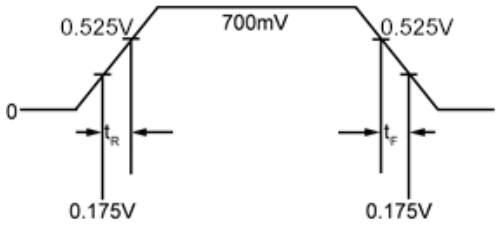


Phase jitter = 212fs$_{RMS}$, 100MHz carrier frequency; integration range: 12kHz–20MHz

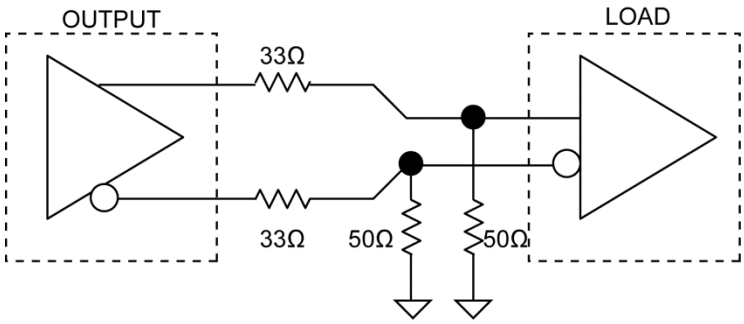
Functional Characteristics



HCSL Waveform Diagram



HCSL Interface Application



PCI Express Device Routing
R_S = 33Ω, R_T = 50Ω

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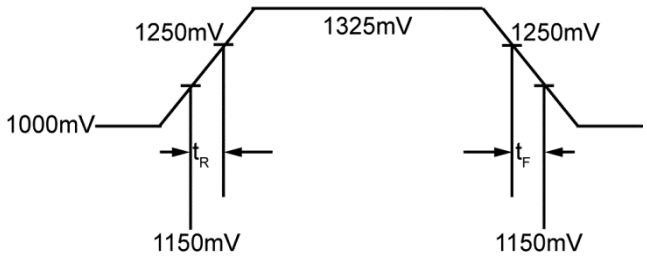
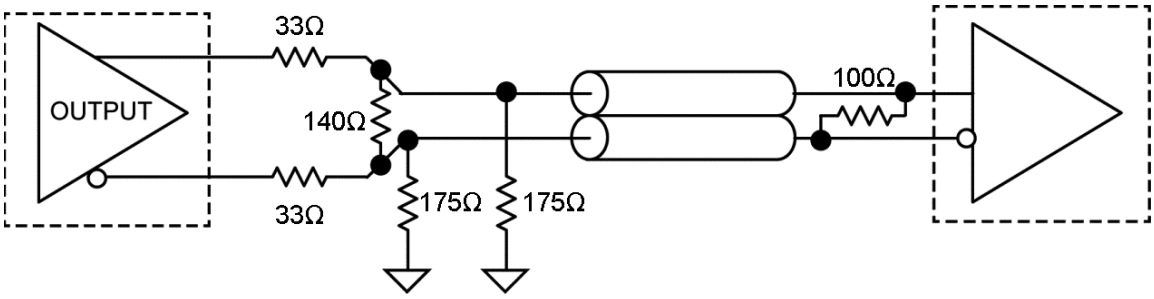
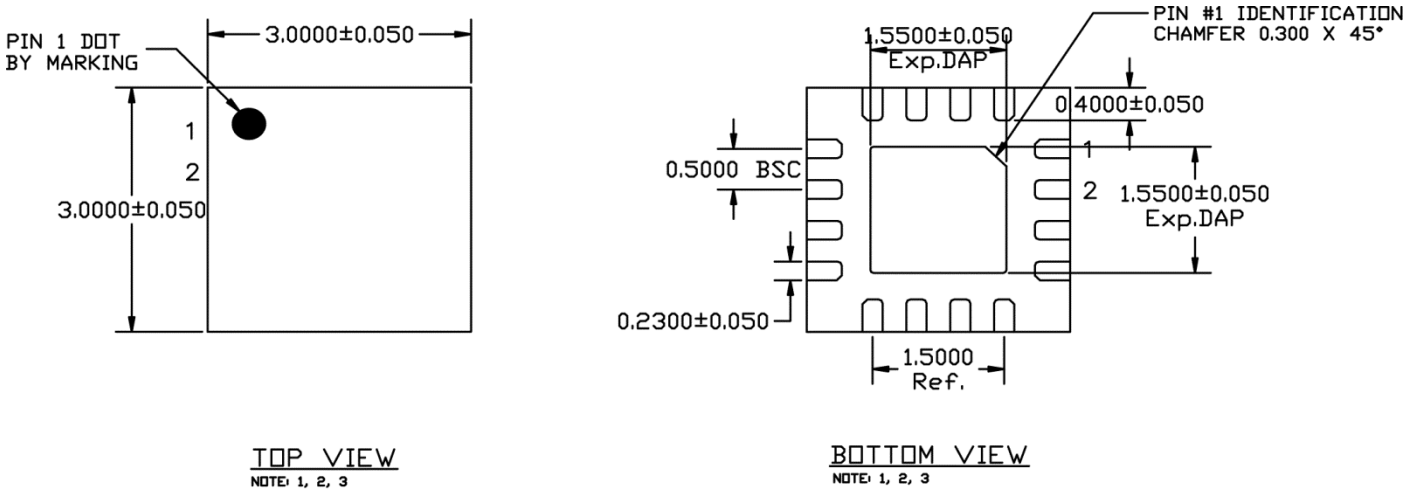
LVDS Waveform Diagram

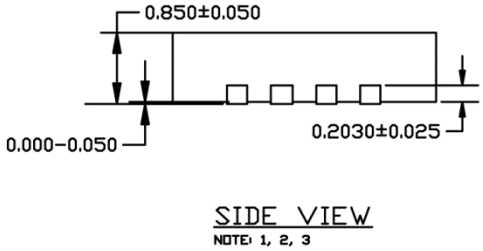


LVDS Interface Application



Package Information[14]





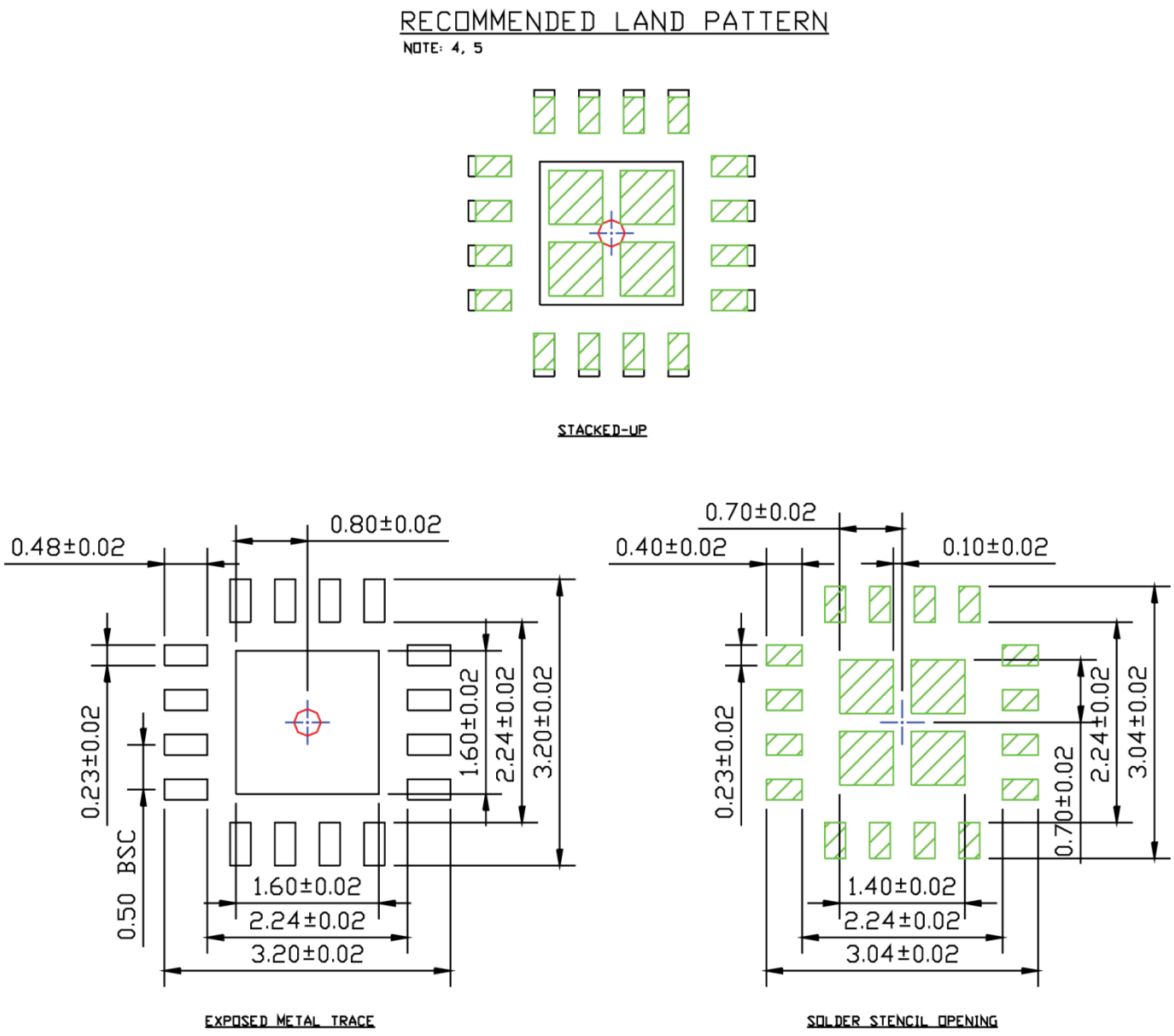
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

16-Pin QFN

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Recommended Land Pattern[14]



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