

85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection

Features

- Gate Drive Supply Voltage up to 16V
- Overcurrent Protection
- Drives High-Side and Low-Side N-Channel MOSFETs with Independent Inputs or With a Single PWM Signal
- TTL Input Thresholds
- On-Chip Bootstrap Diodes
- Fast 35 ns Propagation Times
- Shoot-Through Protection
- Drives 1000 pF Load with 20 ns Rise and Fall Times
- Low Power Consumption
- Supply Undervoltage Protection
- -40°C to $+125^{\circ}\text{C}$ Junction Temperature Range

Applications

- Three-Phase and BLDC Motor Drives
- Three-Phase Inverters

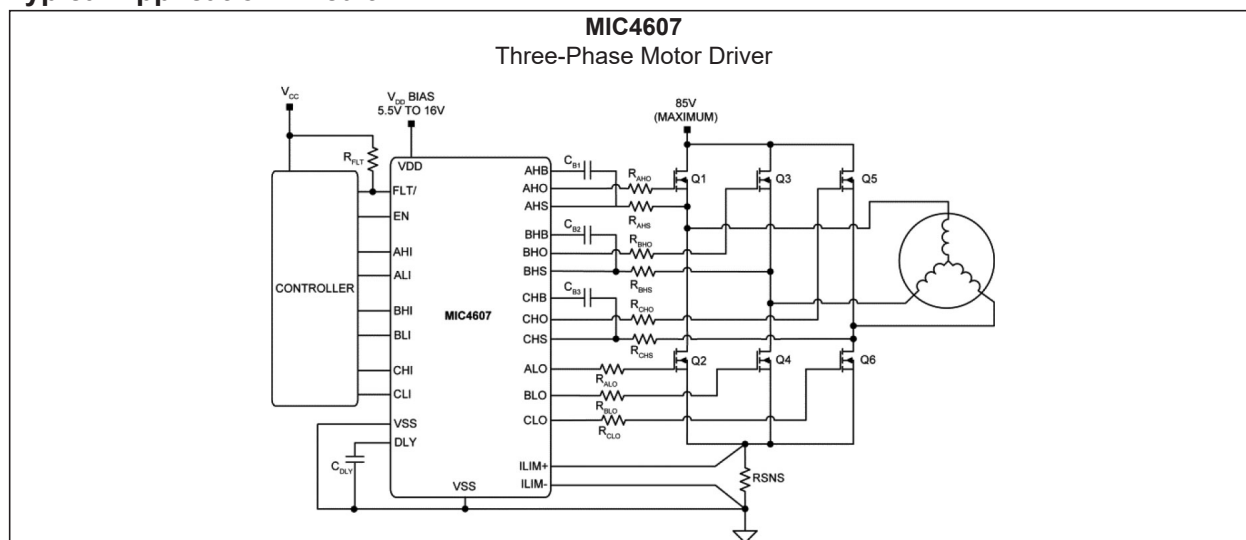
General Description

The MIC4607 is an 85V, three-phase MOSFET driver. The MIC4607 features a fast (35 ns) propagation delay time and a 20 ns driver rise/fall time for a 1 nF capacitive load. TTL inputs can be separate high- and low-side signals or a single PWM input with high and low drive generated internally. High- and low-side outputs are guaranteed to not overlap in either mode. The MIC4607 includes overcurrent protection as well as a high-voltage internal diode that charges the high-side gate drive bootstrap capacitor.

A robust, high-speed, and low-power level shifter provides clean level transitions to the high-side output. The robust operation of the MIC4607 ensures that the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high-speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

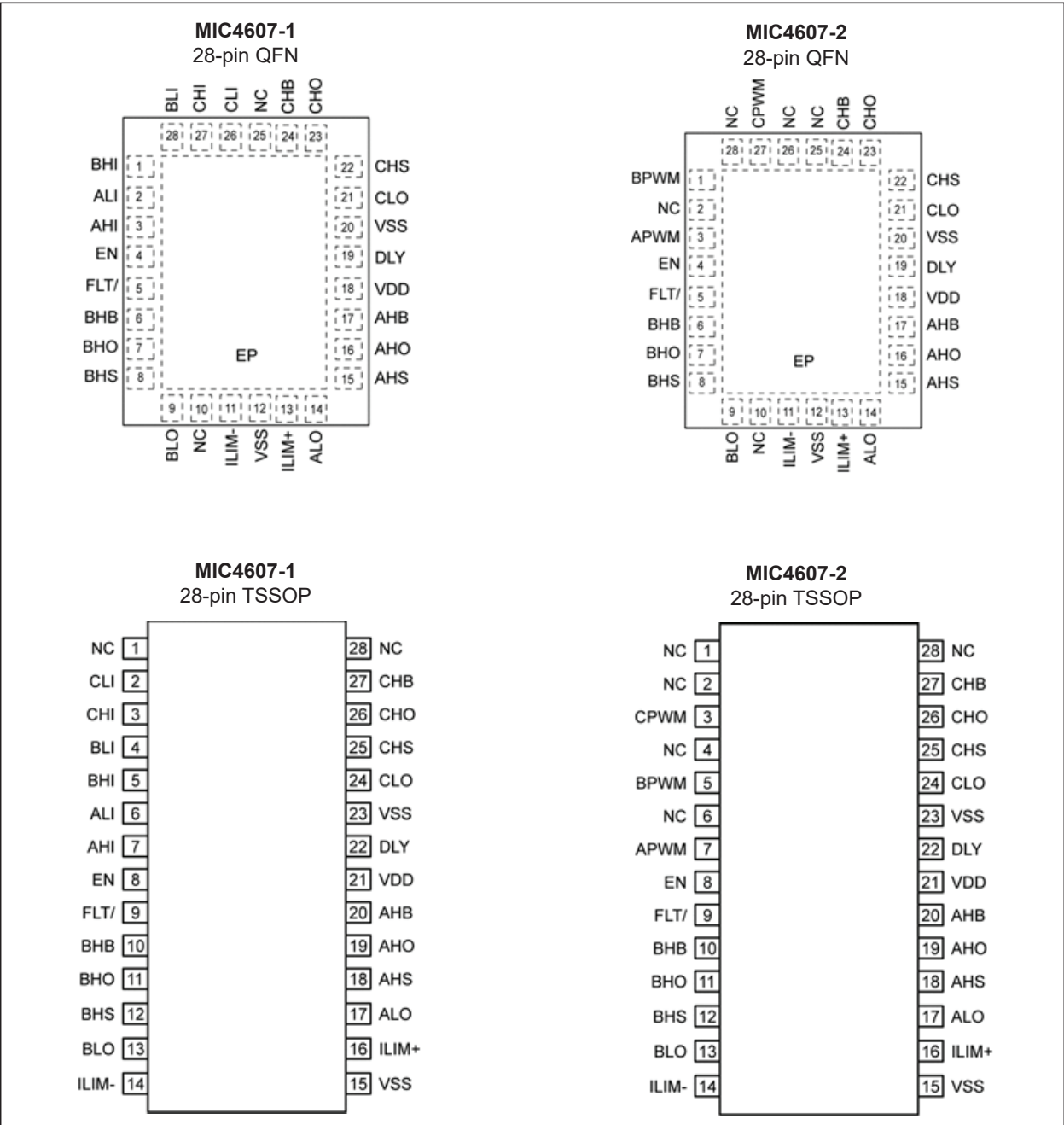
The MIC4607 is available in both a 28-pin 4 mm x 5 mm QFN and 28-pin TSSOP package with an operating junction temperature range of -40°C to $+125^{\circ}\text{C}$.

Typical Application Circuit

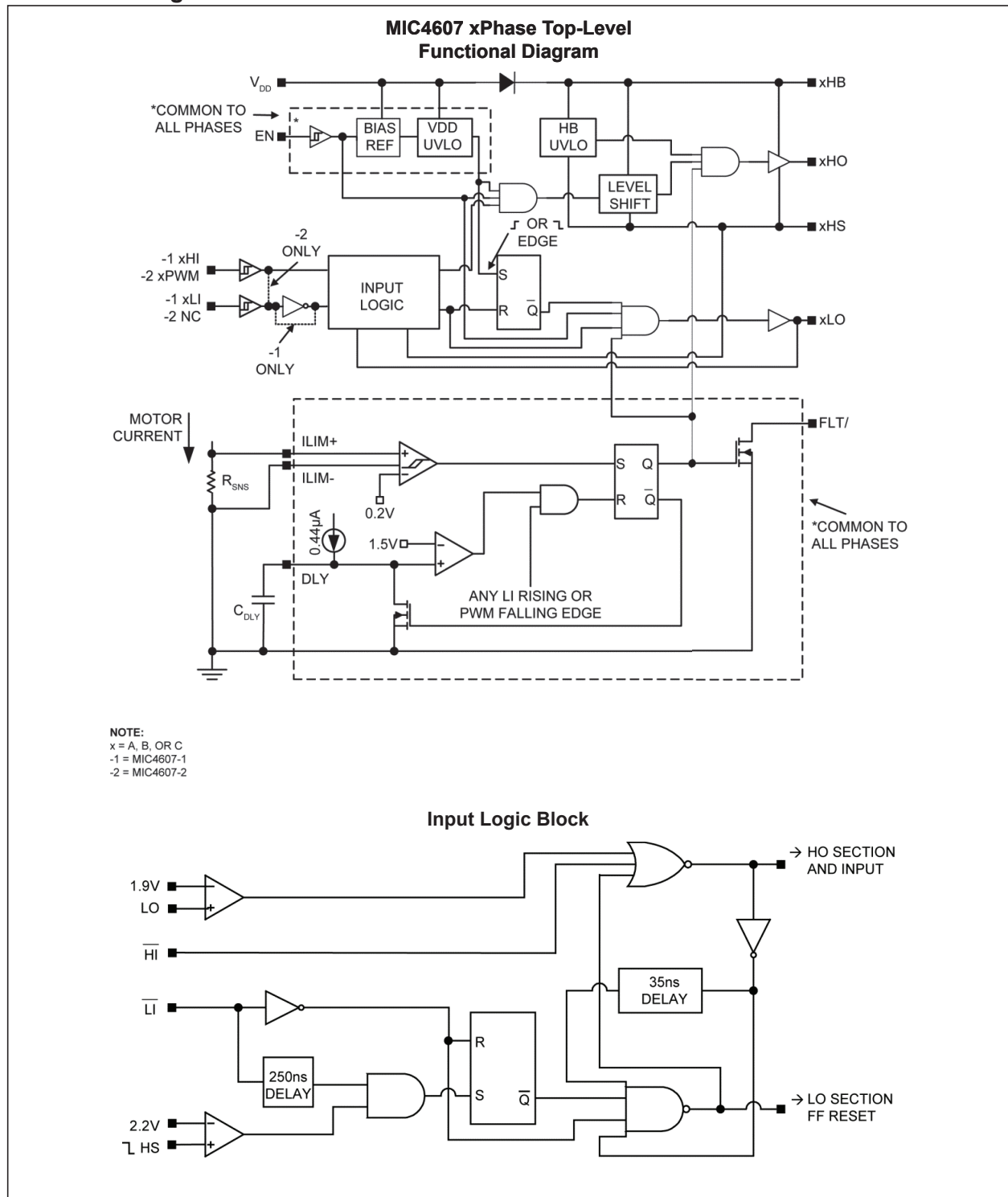


MIC4607

Package Type



Functional Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †, (Note 2)

Supply Voltage (V_{DD} , $V_{xHB} - V_{xHS}$)	–0.3V to 18V
Input Voltages (V_{xLI} , V_{xHI} , V_{xPWM} , V_{EN})	–0.3V to $V_{DD} + 0.3V$
FLT/ Pin	–0.3V to $V_{DD} + 0.3V$
DLY Pin	–0.3V to 18V
Voltage on xLO (V_{xLO})	–0.3V to $V_{DD} + 0.3V$
Voltage on xHO (V_{xHO})	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
Voltage on xHS (Continuous)	–0.3V to 90V
Voltage on xHB	108V
ILIM+	–0.3V to +5V
ILIM–	–0.3V to +2V
Average Current in V_{DD} to HB Diode	100 mA
ESD Protection on All Pins (Note 1):	
HBM	1 kV
MM	200V
CDM	200V

Operational Characteristics ††, (Note 2)

Supply Voltage (V_{DD}), [decreasing V_{DD}]	5.25V to 16V
Supply Voltage (V_{DD}), [increasing V_{DD}]	5.5V to 16V
Voltage on xHS	–0.3V to 85V
Voltage on xHS (repetitive transient <100 ns)	–0.7V to 90V
HS Slew Rate	50 V/ns
Voltage on xHB	$V_{HS} + 5.5V$ to $V_{HS} + 16V$
and/or	$V_{DD} - 1V$ to $V_{DD} + 85V$

† Notice: Exceeding the absolute maximum ratings may damage the device.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 k Ω in series with 100 pF.

2: An “x” in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

DC CHARACTERISTICS (Note 1, 2)

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = V_{xHB} = 12V$; $V_{EN} = 5V$; $V_{SS} = V_{HS} = 0V$; No load on xLO or xHO; $T_A = 25^\circ C$; unless noted. **Bold** values indicate $-40^\circ C < T_J < +125^\circ C$.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current						
V _{DD} Quiescent Current	I _{DD}	—	390	750	μA	xLI = xHI = 0V
V _{DD} Shutdown Current	I _{DDSH}	—	2.2	10	μA	xLI = xHI = 0V; EN = 0V with HS = floating
		—	58	150		xLI = xHI = 0V; EN = 0V; HS = 0V
V _{DD} Operating Current	I _{DDO}	—	0.6	1.5	mA	f = 20 kHz
Per Channel xHB Quiescent Current	I _{HB}	—	20	75	μA	xLI = xHI = 0V or xLI = 0V and xHI = 5V
Per Channel xHB Operating Current	I _{HBO}	—	30	400	μA	f = 20 kHz
xHB to V _{SS} Current, Quiescent	I _{HBS}	—	0.05	5	μA	V _{xHS} = V _{xHB} = 90V
xHB to V _{SS} Current, Operating	I _{HBSO}	—	30	300	μA	f = 20 kHz
Input (TTL: xLI, xHI, xPWM, EN) (Note 3)						
Low-Level Input Voltage	V _{IL}	—	—	0.8	V	—
High-Level Input Voltage	V _{IH}	2.2	—	—	V	—
Input Voltage Hysteresis	V _{HYS}		0.1	—	V	—
Input Pull-Down Resistance	R _I	100	300	500	kΩ	xLI and xHI Inputs (-1 Version)
		50	130	250		xPWM Input (-2 Version)
Undervoltage Protection						
V _{DD} Falling Threshold	V _{DDF}	3.8	4.4	4.9	V	—
V _{DD} Threshold Hysteresis	V _{DDH}	—	0.25	—	V	—
xHB Falling Threshold	V _{HBF}	4.0	4.4	4.9	V	—
xHB Threshold Hysteresis	V _{HBH}	—	0.25	—	V	—
Overcurrent Protection						
Rising Overcurrent Threshold	V _{ILIM+}	175	200	225	mV	(V _{ILIM+} – V _{ILIM–})
ILIM to Gate Propagation Delay	t _{ILIM_PROP}	—	70	—	ns	V _{ILIM+} = 0.5V peak
Fault Circuit						
FLT/ Output Low Voltage	V _{OLF}	—	0.2	0.5	V	V _{ILIM} = 1V; I _{FLT/} = 1 mA
Rising DLY Threshold	V _{DLY+}	—	1.5	—	V	—
DLY Current Source	I _{DLY}	0.3	0.44	0.6	μA	V _{DLY} = 0V
Fault Clear Time	t _{FCL}	—	670	—	μs	C _{DLY} = 1 nF
Bootstrap Diode						
Low-Current Forward Voltage	V _{DL}	—	0.4	0.70	V	I _{VDD-xHB} = 100 μA
High-Current Forward Voltage	V _{DH}	—	0.8	1	V	I _{VDD-xHB} = 50 mA

Note 1: “x” in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.

$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

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DC CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = V_{xHB} = 12V$; $V_{EN} = 5V$; $V_{SS} = V_{HS} = 0V$; No load on xLO or xHO; $T_A = 25^\circ C$; unless noted. **Bold** values indicate $-40^\circ C < T_J < +125^\circ C$.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Dynamic Resistance	R_D	—	4	6	V	—
xLO Gate Driver						
Low-Level Output Voltage	V_{OLL}	—	0.3	0.6	V	$I_{xLO} = 50 \text{ mA}$
High-Level Output Voltage	V_{OHL}	—	0.5	1	V	$I_{xLO} = -50 \text{ mA}$, $V_{OHL} = V_{DD} - V_{xLO}$
Peak Sink Current	I_{OHL}	—	1	—	A	$V_{xLO} = 0V$
Peak Source Current	I_{OLL}	—	1	—	A	$V_{xLO} = 12V$
xHO Gate Driver						
Low-Level Output Voltage	V_{OLH}	—	0.3	0.6	V	$I_{xHO} = 50 \text{ mA}$
High-Level Output Voltage	V_{OHH}	—	0.5	1	V	$I_{xHO} = -50 \text{ mA}$, $V_{OHH} = V_{xHB} - V_{xHO}$
Peak Sink Current	I_{OHH}	—	1	—	A	$V_{xHO} = 0V$
Peak Source Current	I_{OLH}	—	1	—	A	$V_{xHO} = 12V$
Switching Specifications (LI/HI mode with inputs non-overlapping, assumes HS low before LI goes high and LO low before HI goes high).						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}	—	35	75	ns	—
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}	—	35	75	ns	—
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}	—	35	75	ns	—
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}	—	35	75	ns	—
Output Rise/Fall Time	$t_{R/F}$	—	20	—	ns	$C_L = 1000 \text{ pF}$
Output Rise/Fall Time (3V to 9V)	$t_{R/F}$	—	0.8	—	μs	$C_L = 0.1 \text{ }\mu F$
Minimum Input Pulse Width that Changes the Output	t_{PW}	—	50	—	ns	Note 4
Switching Specifications PWM Mode (MIC4607-2) or LI/HI mode (MIC4607-1) with Overlapping LI/HI Inputs						
Delay from PWM Going High / LI Low, to LO Going Low	t_{LOOFF}	—	35	75	ns	—
LO Output Voltage Threshold for LO FET to be Considered Off	V_{LOOFF}	—	1.9	—	V	—
Delay from LO Off to HO Going High	t_{HOON}	—	35	75	ns	—
Delay from PWM or HI Going Low to HO Going Low	t_{HOOFF}	—	35	75	ns	—

Note 1: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.

$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

DC CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = V_{xHB} = 12V$; $V_{EN} = 5V$; $V_{SS} = V_{HS} = 0V$; No load on xLO or xHO; $T_A = 25^\circ C$; unless noted. **Bold** values indicate $-40^\circ C < T_J < +125^\circ C$.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Switch Node Voltage Threshold Signaling HO is Off	V_{SWTH}	1	2.2	4	V	—
Delay between HO FET Being Considered Off to LO Turning On	t_{LOON}	—	35	75	ns	—
Forced xLO On if V_{SWTH} is Not Detected	t_{SWTO}	100	250	500	ns	—

Note 1: “x” in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.

$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{IN} = V_{EN} = 12V$, $V_{BOOST} - V_{SW} = 3.3V$, $V_{OUT} = 3.3V$

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	$^\circ C$	—
Operating Ambient Temperature Range	T_A	-40	—	+125	$^\circ C$	—
Lead Temperature	—	—	260	—	$^\circ C$	Soldering, 10s
Storage Temperature Range	T_S	-60	—	+150	$^\circ C$	—
Maximum Junction Temperature	T_J	—	—	+125	$^\circ C$	—
Package Thermal Resistances						
Thermal Resistance, 4 mm × 5 mm QFN-28L	θ_{JA}	—	43	—	$^\circ C/W$	—
Thermal Resistance, 4 mm × 5 mm QFN-28L	θ_{JC}	—	3.4	—	$^\circ C/W$	—
TSSOP-28L	θ_{JA}	—	70	—	$^\circ C/W$	—
TSSOP-28L	θ_{JC}	—	20	—	$^\circ C/W$	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

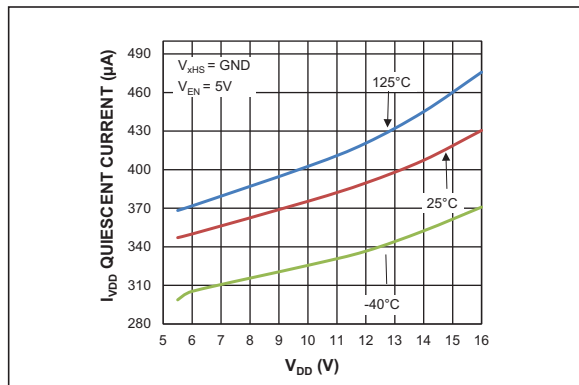


FIGURE 2-1: V_{DD} Quiescent Current vs. V_{DD} Voltage.

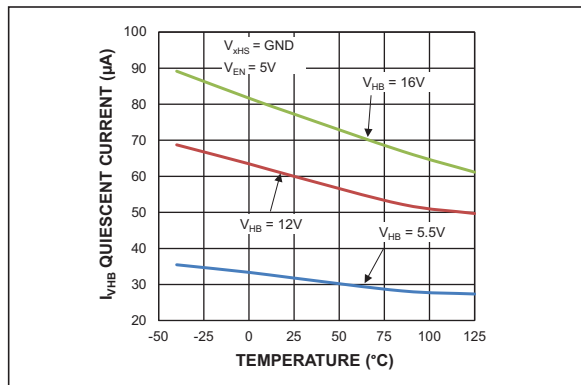


FIGURE 2-4: V_{HB} Quiescent Current (All Channels) vs Temperature.

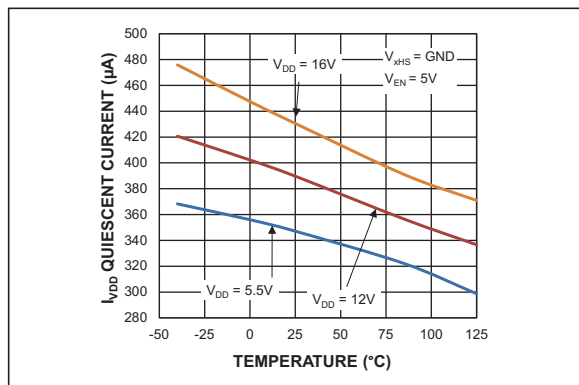


FIGURE 2-2: V_{DD} Quiescent Current vs. Temperature.

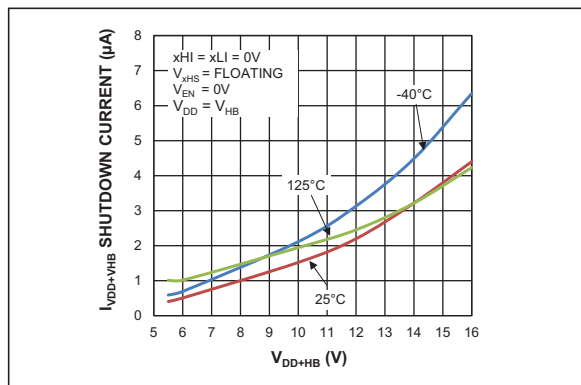


FIGURE 2-5: V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Voltage.

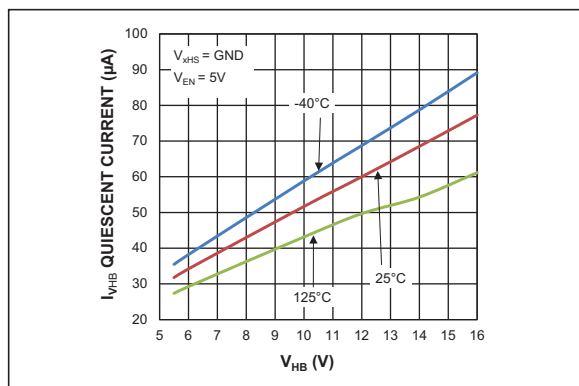


FIGURE 2-3: V_{HB} Quiescent Current (All Channels) vs. V_{HB} Voltage.

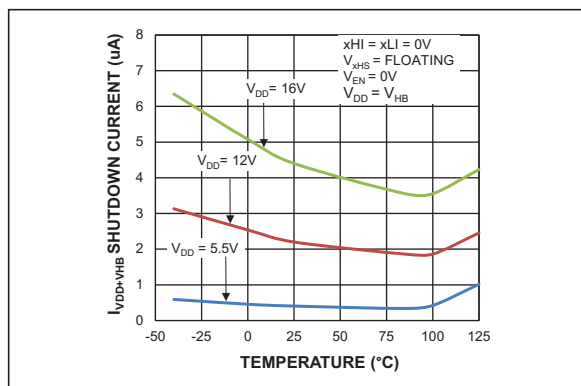


FIGURE 2-6: V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Temperature.

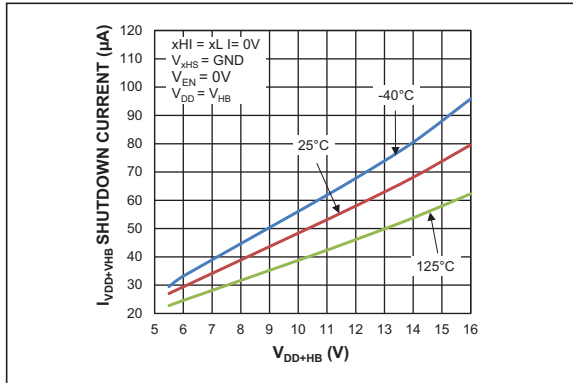


FIGURE 2-7: V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Voltage.

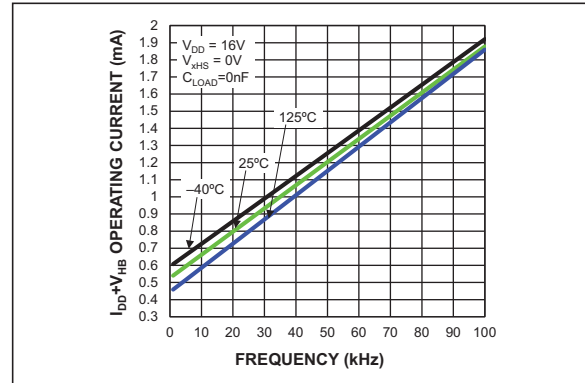


FIGURE 2-10: V_{DD+HB} Operating Current vs. Switching Frequency.

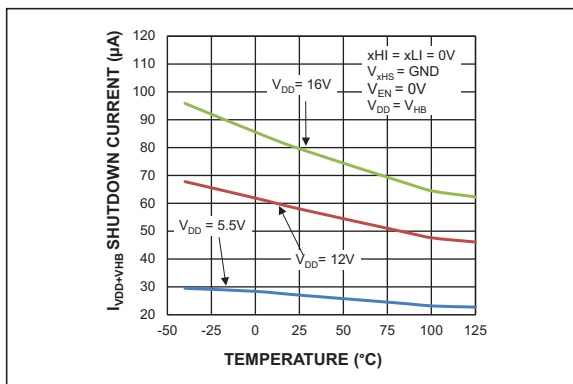


FIGURE 2-8: V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Temperature.

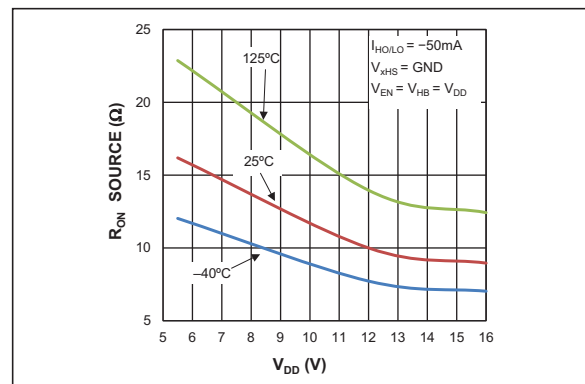


FIGURE 2-11: HO/LO Sink On-Resistance vs. V_{DD} .

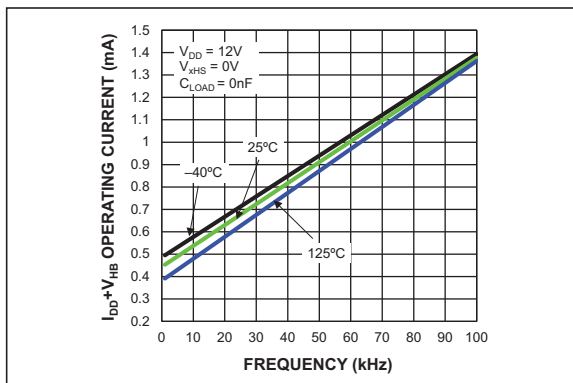


FIGURE 2-9: V_{DD+HB} Operating Current vs. Switching Frequency.

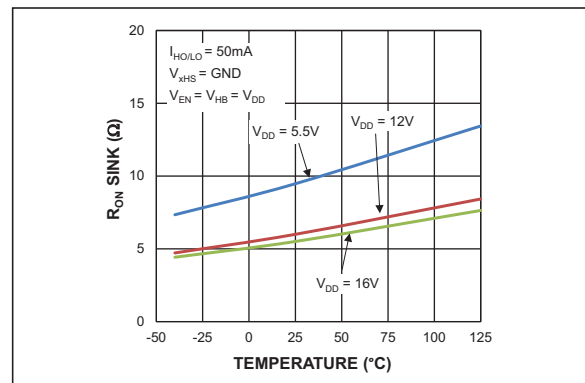


FIGURE 2-12: HO/LO Sink On-Resistance vs. Temperature.

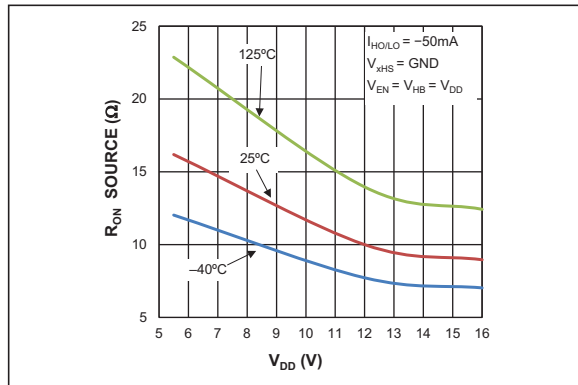


FIGURE 2-13: HO/LO Source On-Resistance vs. V_{DD} .

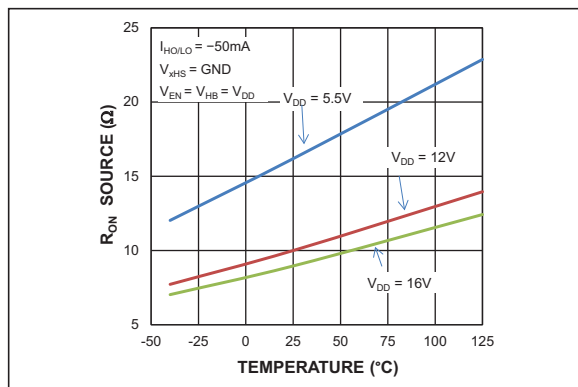


FIGURE 2-14: HO/LO Source On-Resistance vs. Temperature.

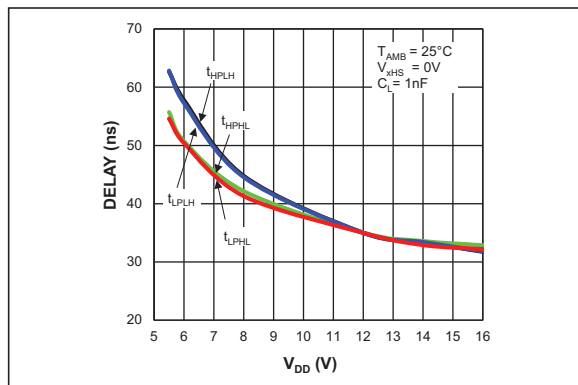


FIGURE 2-15: Propagation Delay (HI/LI Input) vs. V_{DD} Voltage.

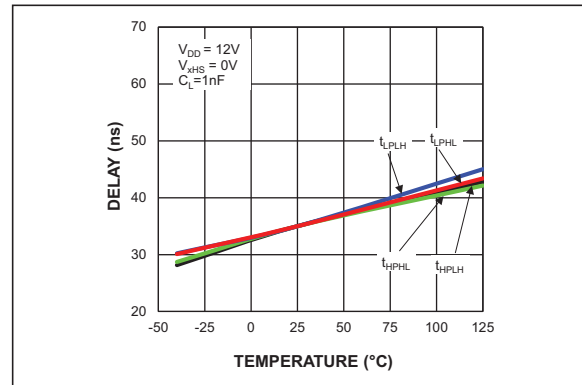


FIGURE 2-16: Propagation Delay (HI/LI Input) vs. Temperature.

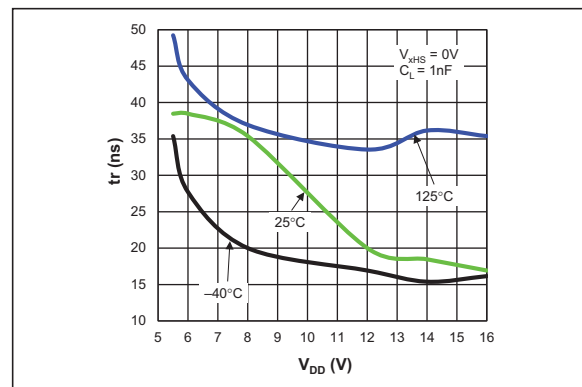


FIGURE 2-17: Output Rise Time vs. V_{DD} Voltage.

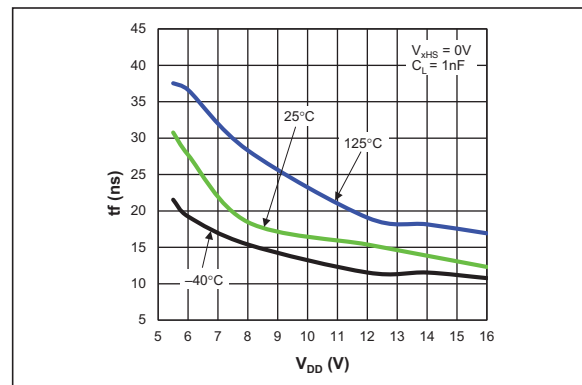


FIGURE 2-18: Output Fall Time vs. V_{DD} Voltage.

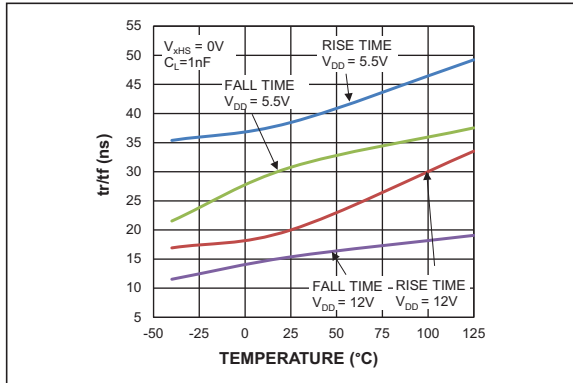


FIGURE 2-19: Rise/Fall Time vs. Temperature.

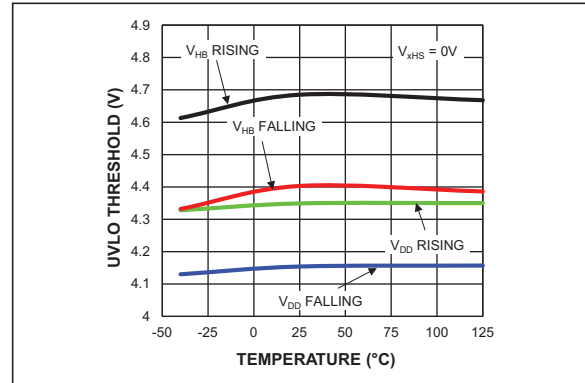


FIGURE 2-22: V_{DD}/V_{HB} UVLO vs. Temperature.

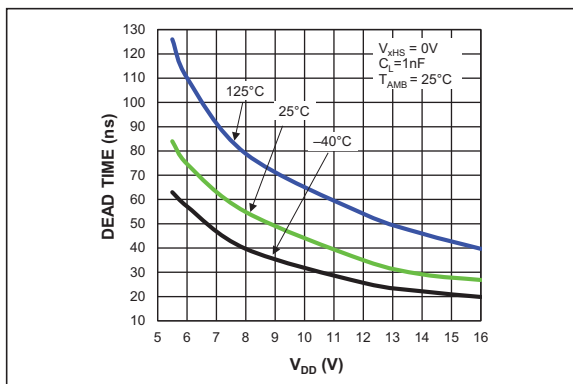


FIGURE 2-20: Dead Time vs. V_{DD} Voltage.

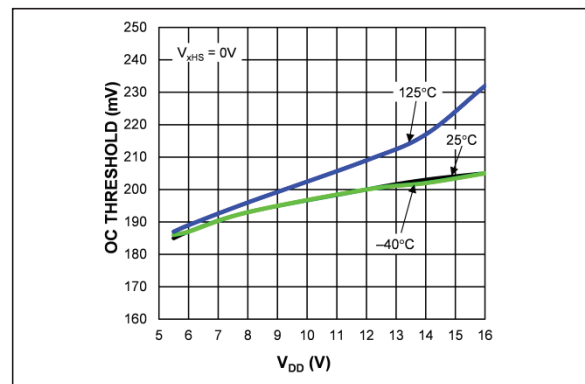


FIGURE 2-23: Overcurrent Threshold vs. V_{DD} Voltage.

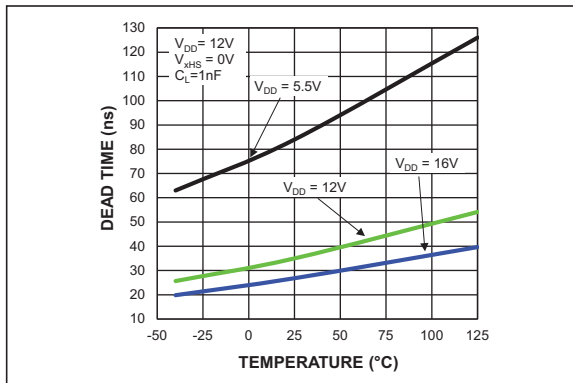


FIGURE 2-21: Dead Time vs. Temperature.

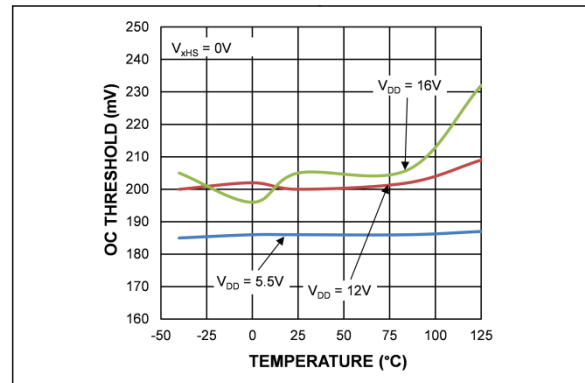


FIGURE 2-24: Overcurrent Threshold vs. Temperature.

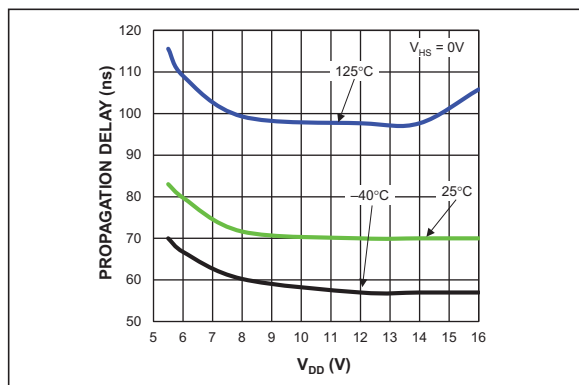


FIGURE 2-25: Overcurrent Propagation Delay vs. V_{DD} Voltage.

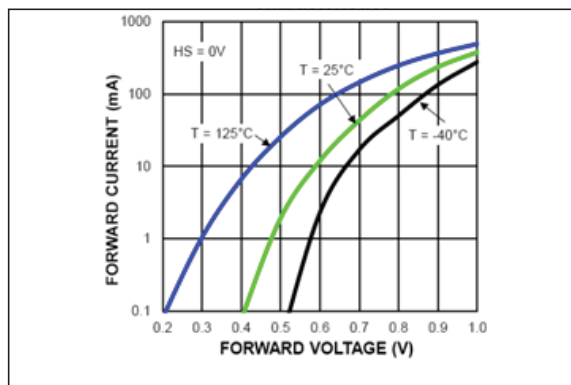


FIGURE 2-28: Bootstrap Diode I-V Characteristics.

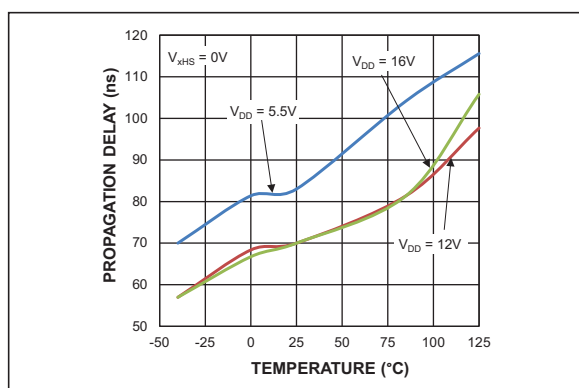


FIGURE 2-26: Overcurrent Propagation Delay vs. Temperature.

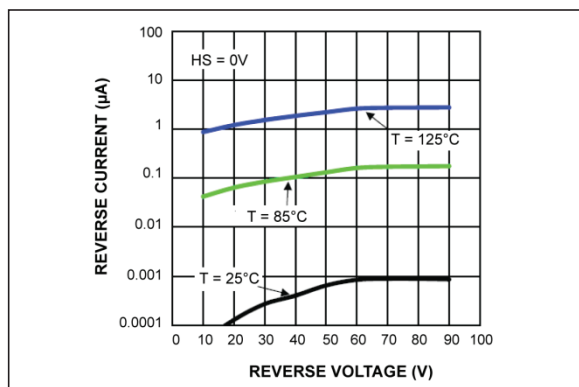


FIGURE 2-27: Bootstrap Diode Reverse Current.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#) and [Table 3-2](#).

TABLE 3-1: QFN PIN FUNCTION TABLE

Pin Number QFN	Pin Name		Description
	MIC4607-1	MIC4607-2	
1	BHI	BPWM	High-side input (-1) or PWM input (-2) for Phase B.
2	ALI	NC	Low-side input (-1) or no connect (-2) for Phase A.
3	AHI	APWM	High-side input (-1) or PWM input (-2) for Phase A.
4	EN	EN	Active-high enable input. High input enables all outputs and initiates normal operation. Low input shuts down device into a low LQ mode.
5	FLT/	FLT/	Open-Drain. FLT/ pin goes low when outputs are latched off due to an overcurrent event. Must be pulled-up to an external voltage with a resistor.
6	BHB	BHB	Phase B High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and BHS. An on-board bootstrap diode is connected from V_{DD} to BHB.
7	BHO	BHO	Phase B High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
8	BHS	BHS	Phase B High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
9	BLO	BLO	Phase B Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
10	NC	NC	No Connect.
11	ILIM-	ILIM-	Differential Current-Limit Input. Connect to most negative end of the external current-sense resistor.
12	VSS	VSS	Power Ground for Phase A and Phase B.
13	ILIM+	ILIM+	Differential Current-Limit Input. Connect to most positive end of the external current-sense resistor.
14	ALO	ALO	Phase A Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
15	AHS	AHS	Phase A High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
16	AHO	AHO	Phase A High Side Drive Output. Connect to the gate of the external high-side power MOSFET.
17	AHB	AHB	Phase A High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and AHS. An on-board bootstrap diode is connected from V_{DD} to AHB.
18	VDD	VDD	Input Supply for Gate Drivers and Internal Logic/Control Circuitry. Decouple this pin to V_{SS} with a minimum 2.2 μ F ceramic capacitor.
19	DLY	DLY	Fault Delay. Connect an external capacitor from this pin to ground to increase the current-limit reset delay. Leave open for minimum delay. Do not externally drive this pin.
20	VSS	VSS	Phase C Power and Control Circuitry Ground.
21	CLO	CLO	Phase C Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
22	CHS	CHS	Phase C High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.

MIC4607

TABLE 3-1: QFN PIN FUNCTION TABLE (CONTINUED)

Pin Number QFN	Pin Name		Description
	MIC4607-1	MIC4607-2	
23	CHO	CHO	Phase C High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
24	CHB	CHB	Phase C High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and CHS. An on-board bootstrap diode is connected from VDD to CHB.
25	NC	NC	No Connect.
26	CLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase C.
27	CHI	CPWM	High-Side Input (-1) or PWM Input (-2) for Phase C.
28	BLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase B.
EP	ePad	ePad	Exposed Heatsink Pad: Connect to GND for best thermal performance.

TABLE 3-2: TSSOP PIN FUNCTION TABLE

Pin Number TSSOP	Pin Name		Description
	MIC4607-1	MIC4607-2	
1	NC	NC	No Connect.
2	CLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase C.
3	CHI	CPWM	High-Side Input (-1) or PWM Input (-2) for Phase C.
4	BLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase B.
5	BHI	BPWM	High-side input (-1) or PWM input (-2) for Phase B.
6	ALI	NC	Low-side input (-1) or no connect (-2) for Phase A.
7	AHI	APWM	High-side input (-1) or PWM input (-2) for Phase A.
8	EN	EN	Active-high enable input. High input enables all outputs and initiates normal operation. Low input shuts down device into a low LQ mode.
9	FLT/	FLT/	Open-Drain. FLT/ pin goes low when outputs are latched off due to an overcurrent event. Must be pulled-up to an external voltage with a resistor.
10	BHB	BHB	Phase B High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and BHS. An on-board bootstrap diode is connected from VDD to BHB.
11	BHO	BHO	Phase B High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
12	BHS	BHS	Phase B High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
13	BLO	BLO	Phase B Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
14	ILIM-	ILIM-	Differential Current-Limit Input. Connect to most negative end of the external current-sense resistor.
15	VSS	VSS	Power Ground for Phase A and Phase B.
16	ILIM+	ILIM+	Differential Current-Limit Input. Connect to most positive end of the external current-sense resistor.
17	ALO	ALO	Phase A Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.

TABLE 3-2: TSSOP PIN FUNCTION TABLE (CONTINUED)

Pin Number TSSOP	Pin Name		Description
	MIC4607-1	MIC4607-2	
18	AHS	AHS	Phase A High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
19	AHO	AHO	Phase A High Side Drive Output. Connect to the gate of the external high-side power MOSFET.
20	AHB	AHB	Phase A High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and AHS. An on-board bootstrap diode is connected from V_{DD} to AHB.
21	VDD	VDD	Input Supply for Gate Drivers and Internal Logic/Control Circuitry. Decouple this pin to V_{SS} with a minimum 2.2 μ F ceramic capacitor.
22	DLY	DLY	Fault Delay. Connect an external capacitor from this pin to ground to increase the current-limit reset delay. Leave open for minimum delay. Do not externally drive this pin.
23	VSS	VSS	Phase C Power and Control Circuitry Ground.
24	CLO	CLO	Phase C Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
25	CHS	CHS	Phase C High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
26	CHO	CHO	Phase C High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
27	CHB	CHB	Phase C High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and CHS. An on-board bootstrap diode is connected from V_{DD} to CHB.
28	NC	NC	No Connect.

4.0 TIMING DIAGRAMS

4.1 Non-Overlapping LI/HI Input Mode (MIC4607-1)

In non-overlapping LI/HI input mode, enough delay is added between the xLI and xHI inputs to allow xHS to be low before xLI is pulled high and similarly xLO is low before xHI goes high.

xHO goes high with a high signal on xHI after a typical delay of 35 ns (t_{HPLH}). xHI going low drives xHO low also with typical delay of 35 ns (t_{HPLH}).

Likewise, xLI going high forces xLO high after typical delay of 35 ns (t_{LPLH}) and xLO follows low transition of xLI after typical delay of 35 ns (t_{LPHL}).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

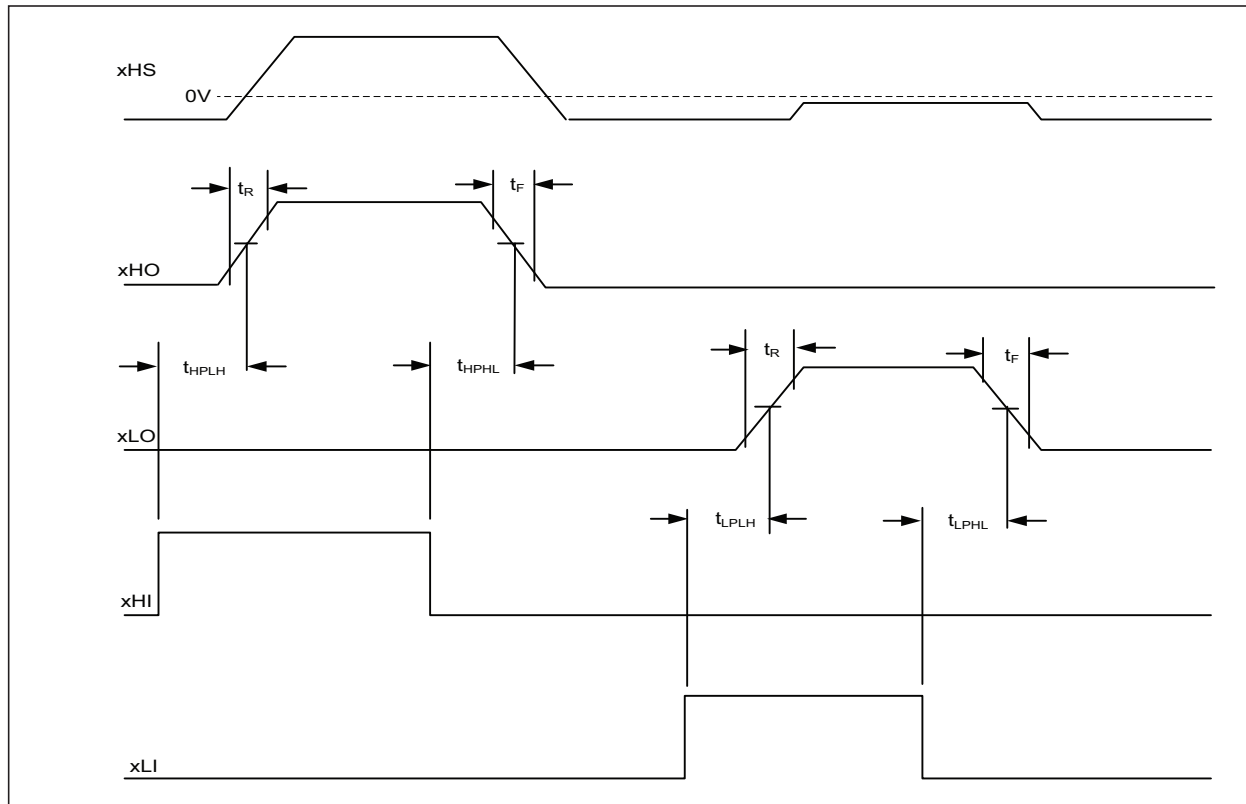


FIGURE 4-1: Separate Non-Overlapping LI/HI Input Mode (MIC4607-1).

Note 1: All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

2: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

4.2 Overlapping LI/HI Input Mode (MIC4607-1)

When xLI/xHI input high signals overlap, xLO/xHO output states are determined by the first output to be turned on. That is, if xLI goes high (ON), while xHO is high, xHO stays high until xHI goes low at which point, after a delay of t_{HOFF} and when $xHS < 2.2V$, xLO goes high with a delay of t_{LOON} . Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xHI edge delayed by a typical 250 ns will set

“HS latch” allowing xLO to go high.

If xHS falls very fast, xLO will be held low by a 35 ns delay gated by HI going low. Conversely, xHI going high (ON) when xLO is high has no effect on outputs until xLI is pulled low (off) and xLO falls to $< 1.9V$. Delay from xLI going low to xLO falling is t_{LOFF} and delay from $xLO < 1.9V$ to xHO being on is t_{HOON} .

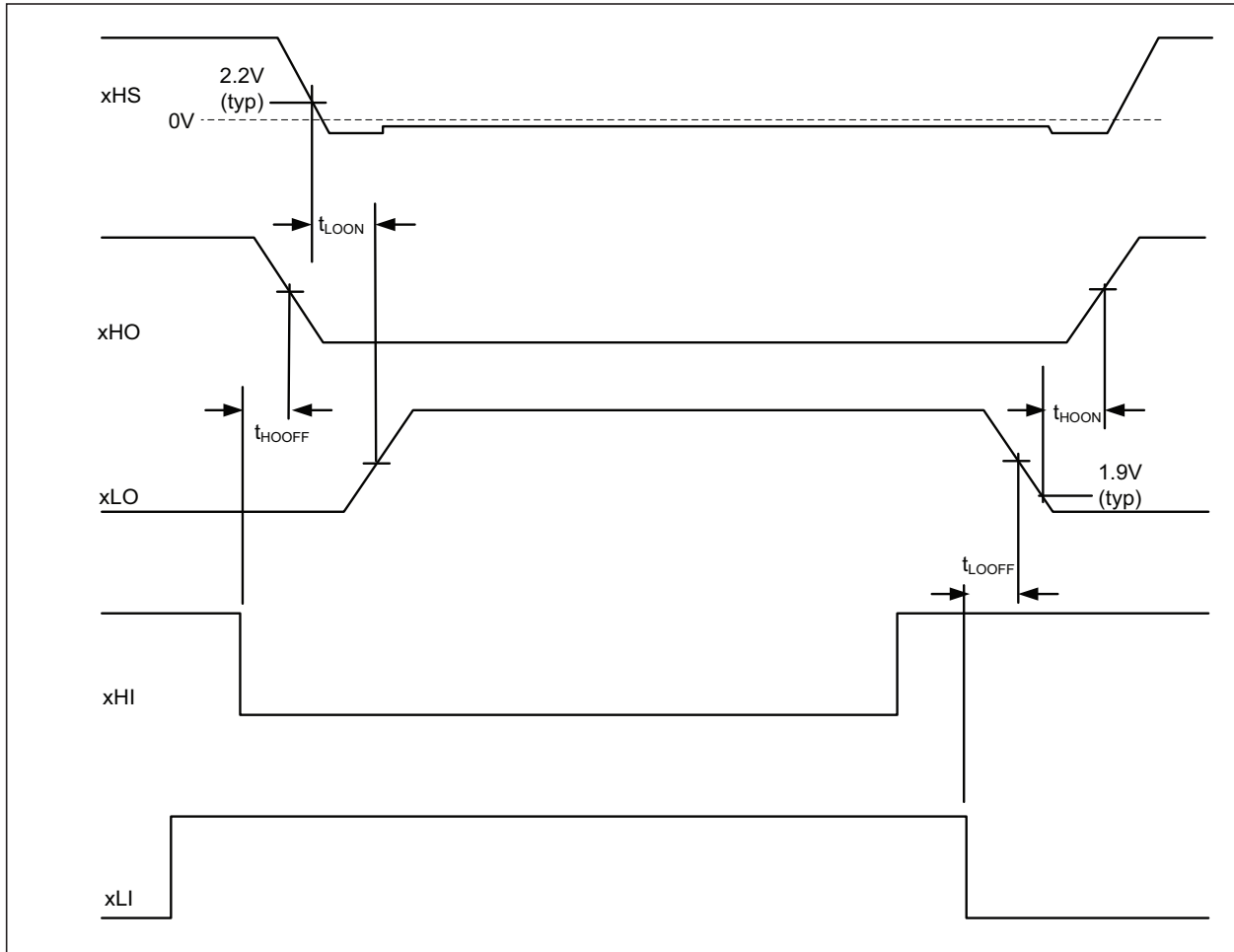


FIGURE 4-2: Separate Overlapping LI/HI Input Mode (MIC4607-1).

4.3 PWM Input Mode (MIC4607-2)

A low going xPWM signal applied to the MIC4607-2 causes xHO to go low, typically 35ns (t_{HOFF}) after the xPWM input goes low, at which point the switch node, xHS, falls (1-2).

When xHS reaches 2.2V (V_{SWTH}), the external high-side MOSFET is deemed off and xLO goes high, typically within 35 ns (t_{LOON}) (3-4). xHS falling below 2.2V sets a latch that can only be reset by xPWM going high. This design prevents ringing on xHS from causing an indeterminate xLO state. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xPWM edge delayed by 250 ns will set "HS latch" allowing xLO to go high.

A 35 ns delay gated by xPWM going low can determine the time to xLO going high for fast falling HS designs. xPWM going high forces xLO low in typically 35ns (t_{LOOFF}) (5-6).

When xLO reaches 1.9V (V_{LOOFF}), the low-side MOSFET is deemed off and xHO is allowed to go high. The delay between these two points is typically 35 ns (t_{HOON}) (7-8).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

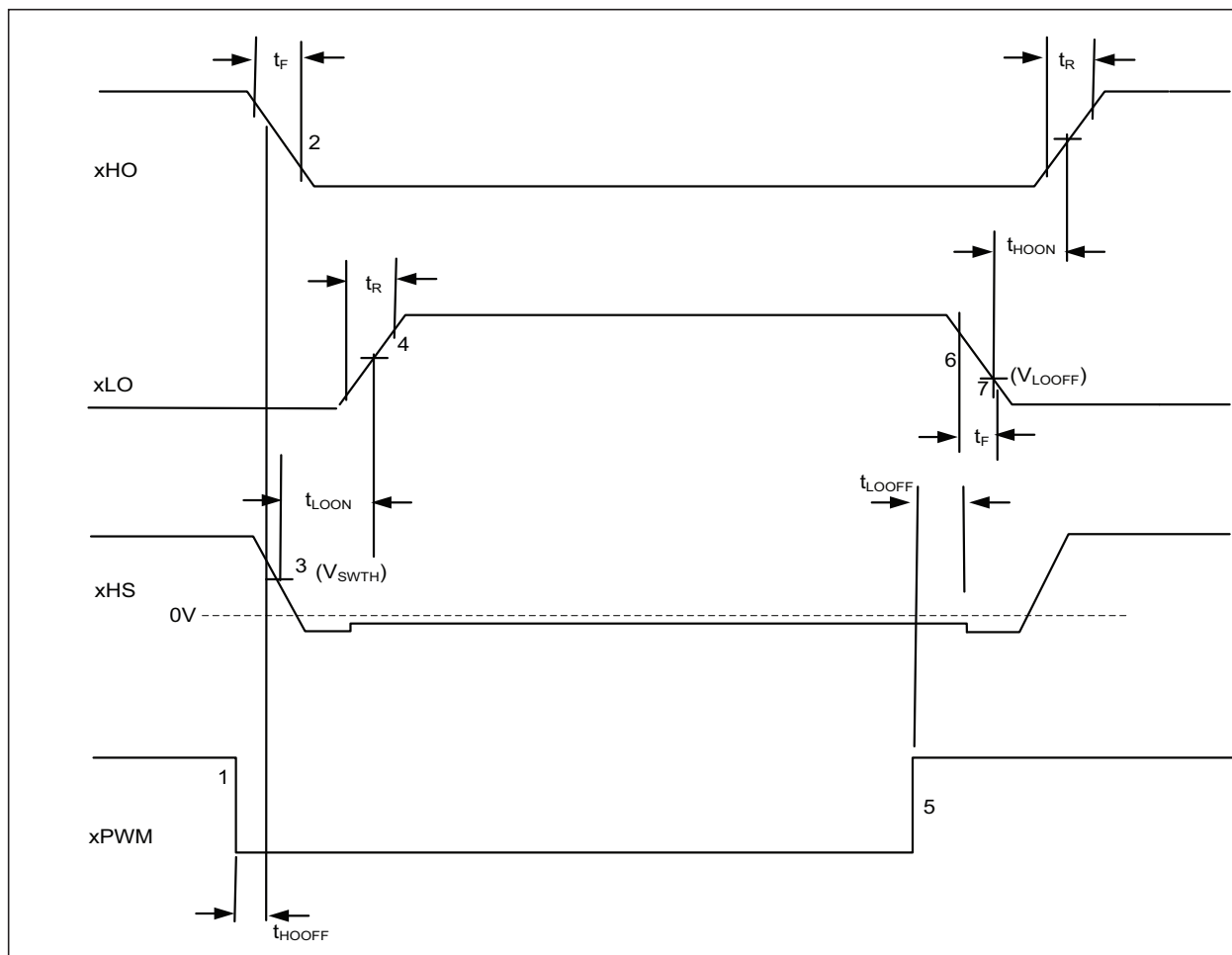


FIGURE 4-3: PWM Mode (MIC4607-2).

4.4 Overcurrent Timing Diagram

The motor current is sensed in an external resistor that is connected between the low-side MOSFET's source pins and ground. If the sense resistor voltage exceeds the rising overcurrent threshold (typically 0.2V), all LO and HO outputs are latched off and the FLT/ pin is pulled low. Once the outputs are latched off, an internal current source (typically 0.44 μ A) begins to charge up the external C_{DLY} capacitor. The outputs remain latched off and all xLI/xHI (or xPWM) input signals are ignored until the voltage on the C_{DLY} capacitor rises

above the V_{DLY+} threshold (typically 1.5V), which resets the latch on the first rising edge of any LI input of the MIC4607-1 (or falling edge on any PWM input for the MIC4607-2).

Once this occurs, the C_{DLY} capacitor is discharged, the FLT/ pin returns to a high impedance state and all outputs will respond to their respective input signals.

On startup, the current limit latch is reset during a rising V_{DD} or a rising EN pin voltage to assure normal operation.

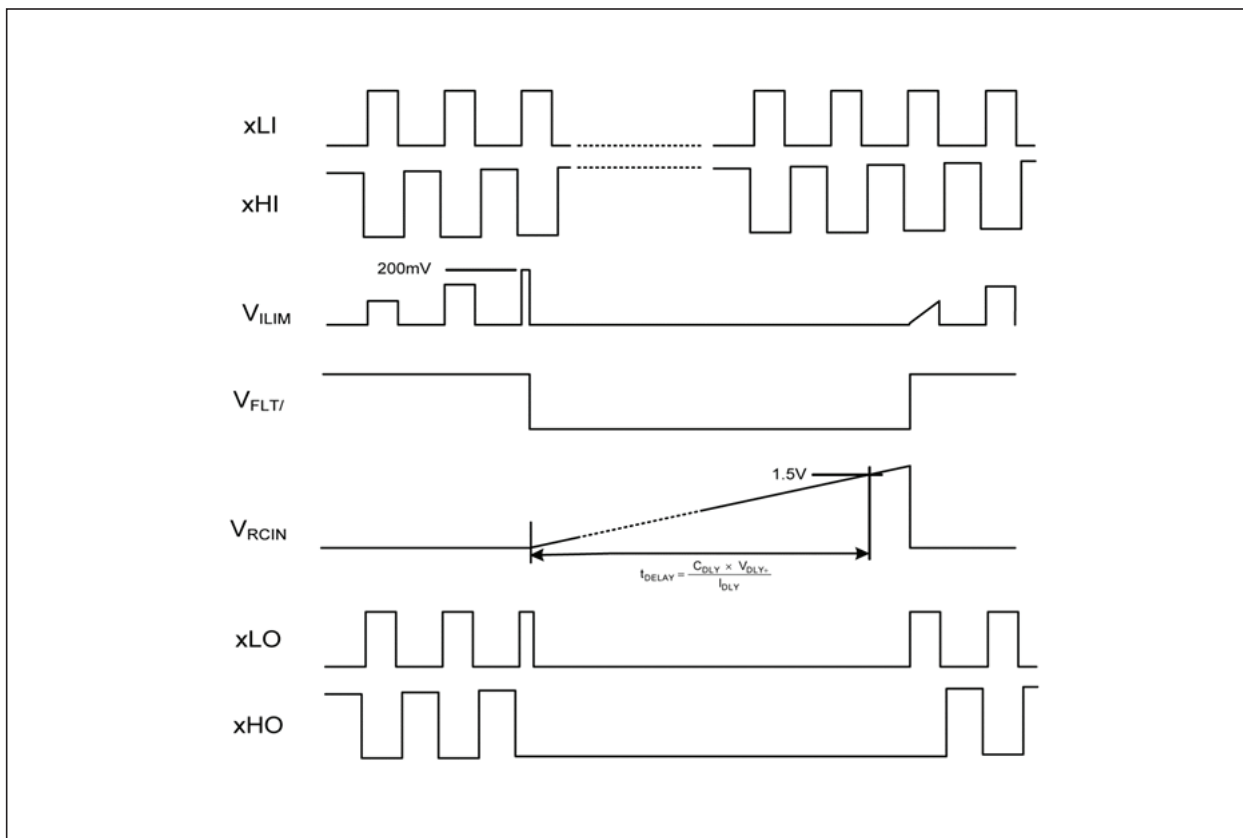


FIGURE 4-4: Overcurrent Timing Diagram.

the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the AHO pin turns on, the voltage across capacitor C_B is applied to the gate of the high-side external MOSFET. As the high-side MOSFET turns on, voltage on the AHS pin rises with the source of the high-side MOSFET until it reaches V_{IN} . As the AHS and AHB pins rise, the internal diode is reverse biased, preventing capacitor C_B from discharging. During this time, the high-side MOSFET is kept ON by the voltage across capacitor C_B .

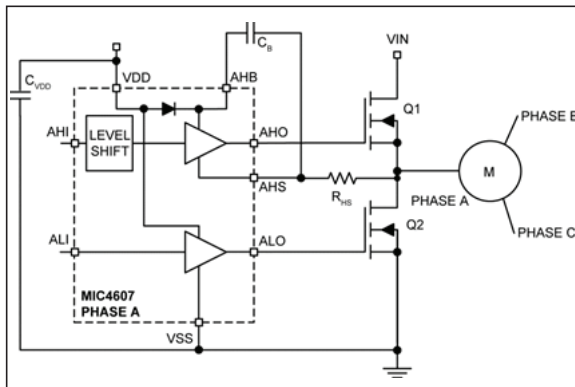


FIGURE 5-3: MIC4607 Motor Driver Example.

5.6 Programmable Gate Drive

The MIC4607 offers programmable gate drive, meaning the MOSFET gate drive (gate-to-source voltage) equals the V_{DD} voltage. This feature offers designers flexibility in selecting the proper MOSFETs for a given application. Different MOSFETs require different V_{GS} characteristics for optimum $R_{DS(ON)}$ performance. Typically, the higher the gate voltage (up to 16V), the lower the $R_{DS(ON)}$ achieved. For example, as shown in Figure 5-4, a NTMSF4899NF MOSFET can be driven to the ON state with a gate voltage of 5.5V but $R_{DS(ON)}$ is 5.2 m Ω . If driven to 10V, $R_{DS(ON)}$ is 4.1 m Ω —a decrease of 20%.

In low-current applications, the losses due to $R_{DS(ON)}$ are minimal, but in high-current motor drive applications such as power tools, the difference in $R_{DS(ON)}$ can lower the efficiency, reducing run time.

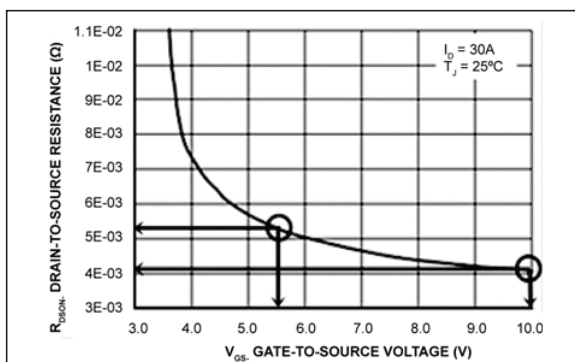


FIGURE 5-4: MOSFET $R_{DS(ON)}$ vs. V_{GS} .

5.7 Overcurrent Protection Circuitry

The MIC4607 provides overcurrent protection for the motor driver circuitry. It consists of:

- A comparator that senses the voltage across a current-sense resistor
- A latch and timer that keep all gate drivers off during a fault
- An open-drain pin that pulls low during the fault.

If an overcurrent condition is detected, the FLT/ pin is pulled low and the gate drive outputs are latched off for a time that is determined by the DLY pin circuitry. After the delay circuitry times out, a high-going edge on any of the LI pins (for the MIC4607-1 version) or a low-going edge on any of the PWM pins (for the MIC4607-2 version) is required to reset the latch, de-assert the FLT/ pin and allow the gate drive outputs to switch.

For additional information, refer to the [Timing Diagrams](#) section as well as the [Functional Diagram](#) section.

5.7.1 ILIM

The ILIM+ and ILIM- pins provide a Kelvin-sensed circuit that monitors the voltage across an external current sense resistor. This resistor is typically connected between the source pins of all three low-side MOSFETs and power ground. If the peak voltage across this resistor exceeds the V_{ILIM+} threshold, it will cause all six outputs to latch off. Both pins should be shorted to V_{SS} ground if the overcurrent features is not used.

5.7.2 DLY

A capacitor connected to the DLY pin determines the amount of time the gate drive outputs are latched off before they can be restarted.

During normal operation, the DLY pin is held low by an internal MOSFET. After an overcurrent condition is detected, the MOSFET turns off and the external capacitor is charged up by an internal current source. The outputs remain latched off until the DLY pin voltage reaches the V_{DLY+} threshold (typically 1.5V).

The delay time can be approximately calculated using Equation 5-1.

EQUATION 5-1:

$$t_{DLY} = \frac{C_{DLY} \times V_{DLY+}}{I_{DLY}}$$

5.7.3 FLT/

This open-drain output is pulled low while the gate drive outputs are latched off after an over-current condition. It will de-assert once the DLY pin has reached the V_{DLY+} threshold and a rising edge occurs on any LI pin (for the MIC4607-1) or a falling edge on any PWM pin (MIC4607-2).

During normal operation, the internal pull-down MOS-FET of the pin is high impedance. A pull-up resistor must be connected to this pin.

MIC4607

turn-off. The xLO driver turns on after a short delay (t_{LOON}). Once the xLO driver is turned on, it is latched on until the xPWM signal goes high. This prevents any ringing or oscillations on the switch node or xHS pin from turning off the xLO driver. If the xPWM pin goes low and the voltage on the xHS pin does not cross the V_{SWTH} threshold, the xLO pin will be forced high after a short delay (t_{SWTO}), ensuring proper operation.

The internal logic circuits also ensure a “first on” priority at the inputs. If the xHO output is high, the xLI pin is inhibited. A high signal or noise glitch on the xLI pin has no effect on the xHO or xLO outputs until the xHI pin goes low. Similarly, xLO being high holds xHO low until xLI and xLO are low.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width can result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead-time circuit in the MIC4607 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti-shoot-through circuit's control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

The scope photo in Figure 6-4 shows the dead time (<20 ns) between the high- and low-side MOSFET transitions as the low-side driver switches off while the high-side driver transitions from off to on.

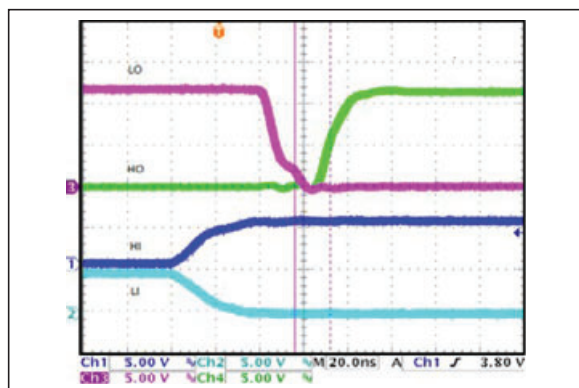


FIGURE 6-4: Adaptive Dead-Time LO (LOW) to HO (HIGH).

Table 6-1 contains truth tables for the MIC4607-1 (independent TTL inputs) and Table 6-2 is for the MIC4607-2 (PWM inputs) that details the “first on” priority as well as the failsafe delay (t_{SWTO}).

TABLE 6-1: MIC4607-1 TRUTH TABLE

xLI	xHI	xLO	xHO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	xHO will not go HIGH until xLO falls below 1.9V.
1	0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	1	X	X	First ON stays on until input of same goes LOW.

TABLE 6-2: MIC4607-2 TRUTH TABLE

xPWM	xLO	xHO	Comments
0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	0	1	xHO will not go HIGH until xLO falls below 1.9V.

6.2 HS Pin Clamp

A resistor/diode clamp between the switching node and the HS pin is necessary to clamp large negative glitches or pulses on the HS pin.

Figure 6-5 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the three phase motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side MOSFET is conducting during the on-time state, current flows into the motor. After the high-side MOSFET turns off, but before the low-side MOSFET turns on, current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current, and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and a diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recommended. If the HS pin voltage exceeds 0.7V, a diode between the xHS pin and ground is recommended. The diode reverse

voltage rating must be greater than the high-voltage input supply (V_{IN}). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

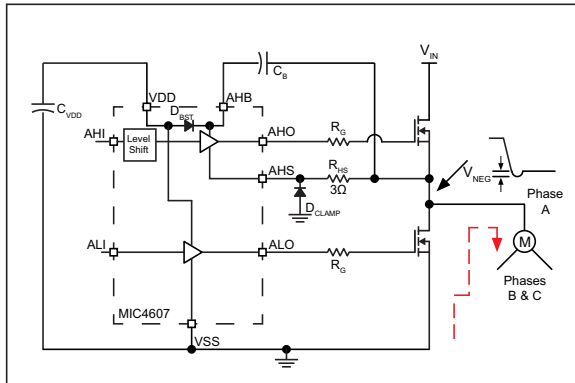


FIGURE 6-5: Negative HS Pin Voltage.

6.3 Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

6.4 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the bootstrap capacitor (C_B) multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by [Equation 6-1](#).

EQUATION 6-1:

$$I_{F(AVE)} = Q_{GATE} \times f_S$$

Where:

Q_{GATE} Total gate charge at $V_{HB} - V_{HS}$.
 f_S Gate drive switching frequency.

The average power dissipated by the forward voltage drop of the diode equals:

EQUATION 6-2:

$$P_{diode_{FWD}} = I_{F(AVE)} \times V_F$$

Where:

V_F Diode forward voltage drop.

There are three phases in the MIC4607. The power dissipation for each of the bootstrap diodes must be calculated and summed to obtain the total bootstrap diode power dissipation for the package.

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 3 μA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1 mW and can be ignored.

An optional external bootstrap diode may be used instead of the internal diode ([Figure 6-6](#)). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the V_{DD} supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated with the formula in [Equation 6-3](#):

EQUATION 6-3:

$$P_{diode_{REV}} = I_R \times V_{REV} \times (1 - D)$$

Where:

I_R Reverse current flow at V_{REV} and T_J .
 V_{REV} Diode reverse voltage.
 D Duty cycle ($t_{ON} \times f_S$).

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.

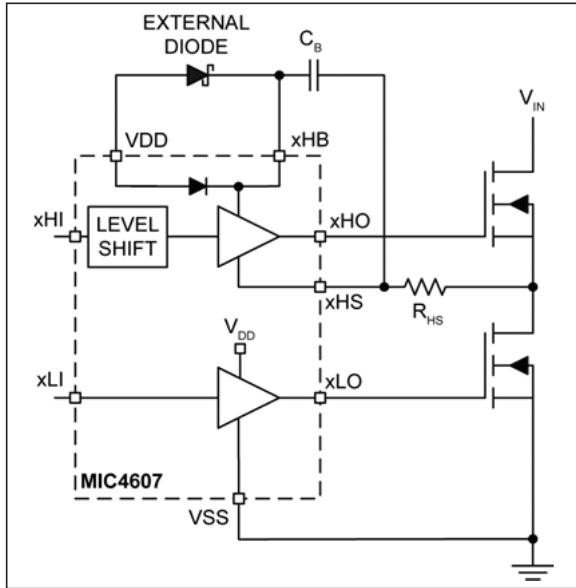


FIGURE 6-6: Optional External Bootstrap Diode.

6.5 Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 6-7 shows a simplified equivalent circuit of the MIC4607 driving an external high-side MOSFET.

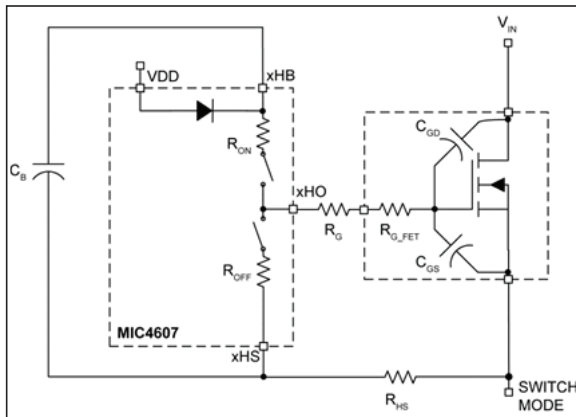


FIGURE 6-7: MIC4607 Driving an External High-Side MOSFET.

6.5.1 DISSIPATION DURING THE EXTERNAL MOSFET TURN-ON

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON} , R_G and R_{G_FET} . R_{ON} is the on resistance of the upper driver MOSFET in the MIC4607. R_G is the series resistor (if any) between the driver and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET and is typically listed in the power

MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET} .

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with I_D , V_{GS} , and V_{DS} . Fortunately, most power MOSFET specifications include a typical graph of total gate charge versus V_{GS} . Figure 6-8 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5 nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

EQUATION 6-4:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^2$$

Where:

C_{ISS} Total gate capacitance of the MOSFET.

but

EQUATION 6-5:

$$Q = C \times V$$

so,

EQUATION 6-6:

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

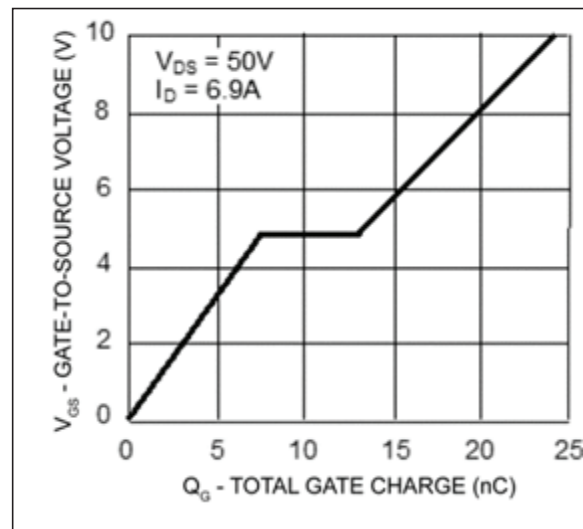


FIGURE 6-8: Typical Gate Charge vs. V_{GS} .

The same energy is dissipated by R_{OFF} , R_G , and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF} , the total energy and power dissipated by the resistive drive elements is:

EQUATION 6-7:

$$E_{DRIVER} = Q_G \times V_{GS}$$

Where:

E_{DRIVER} Energy dissipated per switching cycle

and

EQUATION 6-8:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:

P_{DRIVER} Power dissipated per switching cycle

Q_G Total gate charge at V_{GS}

V_{GS} Gate-to-source voltage on MOSFET

f_S Switching freq. of the gate drive circuit

6.6 Supply Current Power Dissipation

Power is dissipated in the input and control sections of the MIC4607, even if there is no external load. Current is still drawn from the V_{DD} and H_B pins for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The V_{DD} and V_{HB} currents are proportional to operating frequency and the V_{DD} and V_{HB} voltages. The [Typical Performance Curves](#) show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4607 due to supply current is:

EQUATION 6-9:

$$P_{diss_SUPPLY} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB}$$

Values for I_{DD} and I_{HB} are found in the EC table and the typical characteristics graphs.

6.7 Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4607 is equal to the power dissipation caused by driving the external MOSFETs, the supply currents and the internal bootstrap diodes.

EQUATION 6-10:

$$P_{diss_TOTAL} = P_{diss_SUPPLY} + P_{diss_DRIVE} + P_{DIODE}$$

The power dissipated in the driver equals the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET} . Letting $R_{ON} = R_{OFF}$, the power dissipated in the driver due to driving the external MOSFET is:

EQUATION 6-11:

$$P_{diss_DRIVER} = P_{DRIVER} \times \frac{R_{ON}}{R_{ON} + R_G + R_{G_FET}}$$

There are six MOSFETs driven by the MIC4607. The power dissipation for each of the drivers must be calculated and summed to obtain the total driver diode power dissipation for the package.

In some cases, the high-side FET of one phase may be pulsed at a frequency, f_S , while the low-side FET of the other phase is kept continuously on. Since the MOSFET gate is capacitive, there is no driver power if the FET is not switched. The operation of all driver outputs must be considered to accurately calculate power dissipation.

The die temperature can be calculated after the total power dissipation is known.

EQUATION 6-12:

$$T_J = T_A + P_{diss_TOTAL} \times \theta_{JA}$$

Where:

T_A Maximum ambient temperature

T_J Junction temperature

P_{diss_TOTAL} Total power dissipation of MIC4607

θ_{JA} Thermal resistance from junction to ambient air

6.8 Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

6.9 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side (V_{DD}) and high-side (xHB) supply pins. These capacitors supply the charge necessary to drive the

external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from xHB to xHS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1 μF is required for C_B (xHB to xHS capacitors) and 1 μF for the V_{DD} capacitor, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the V_{DD} and V_{SS} pins. The bypass capacitor (C_B) for the xHB supply pin must be located as close as possible between the xHB and xHS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the “[Grounding, Component Placement and Circuit Layout](#)” sub-section for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

EQUATION 6-13:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}}$$

Where:

Q_{GATE} Total gate charge at V_{HB} .
 ΔV_{HB} Voltage drop at the HB pin.

If the high-side MOSFET is not switched but held in an on state, the voltage in the bootstrap capacitor will drop due to leakage current that flows from the HB pin to ground. This current is specified in the [Electrical Characteristics](#) table. In this case, the value of C_B is calculated as:

EQUATION 6-14:

$$C_B \geq \frac{I_{HBS} \times t_{ON}}{\Delta V_{HB}}$$

Where:

I_{HBS} Maximum xHB pin leakage current.
 t_{ON} Maximum high-side FET on-time.

The larger value of C_B from [Equation 6-13](#) or [Equation 6-14](#) should be used.

6.10 Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4607 driver require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

[Figure 6-9](#) shows the critical current paths of the high- and low-side driver when their outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B . Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the xHB pin and out the xHO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B . The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor C_B must be placed close to the xHB and xHS pins. This capacitor not only provides all the energy for turn-on but it must also keep xHB pin noise and ripple low for proper operation of the high-side drive circuitry.

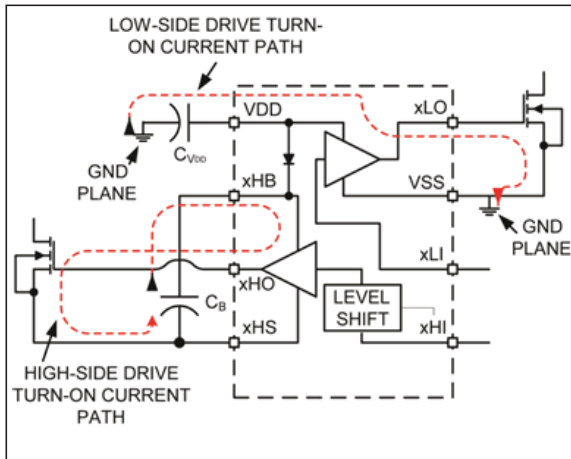


FIGURE 6-9: Turn-On Current Paths.

Figure 6-10 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B .

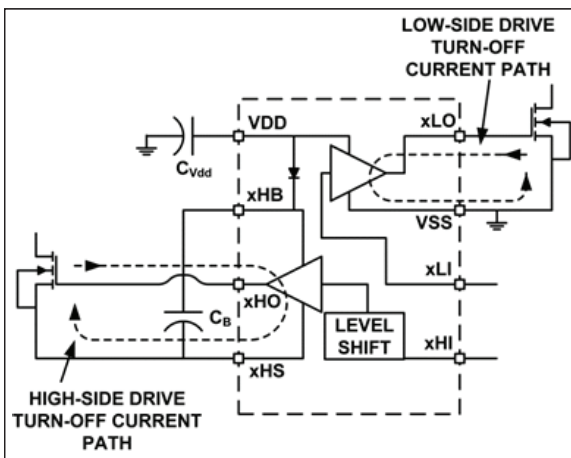


FIGURE 6-10: Turn-Off Current Paths.

A current-sense resistor senses the peak motor current. The voltage across this resistor is monitored by the OC circuit in the MIC4607, which provides overcurrent protection for the application. The 120V rating of the MIC5281 series of LDOs provide input surge voltage protection, while regulating the battery voltage down to 3.3V and 10V to 12V for the microcontroller and gate driver respectively. This circuit can also be used for power tool applications, where the battery voltage carries high-voltage peaks and surges.

Figure 7-3 illustrates an off-line motor application. Adding an off-line power supply to the front end allow the MIC4607 to be used in applications such as blenders and other small white goods as well as ceiling fan applications. The circuit consists of an MIC38C44 based AC/DC power supply, that is used to generate 24 VDC to power a BLDC motor. The MIC4607 drives the six MOSFETs that provide power to the motor.

The MIC4607 can also be used in low and mid-voltage inverter applications. [Figure 7-4](#) shows how power generated by a spinning (or breaking) motor can be used to generate DC power to a load or provide power for battery-charging applications.



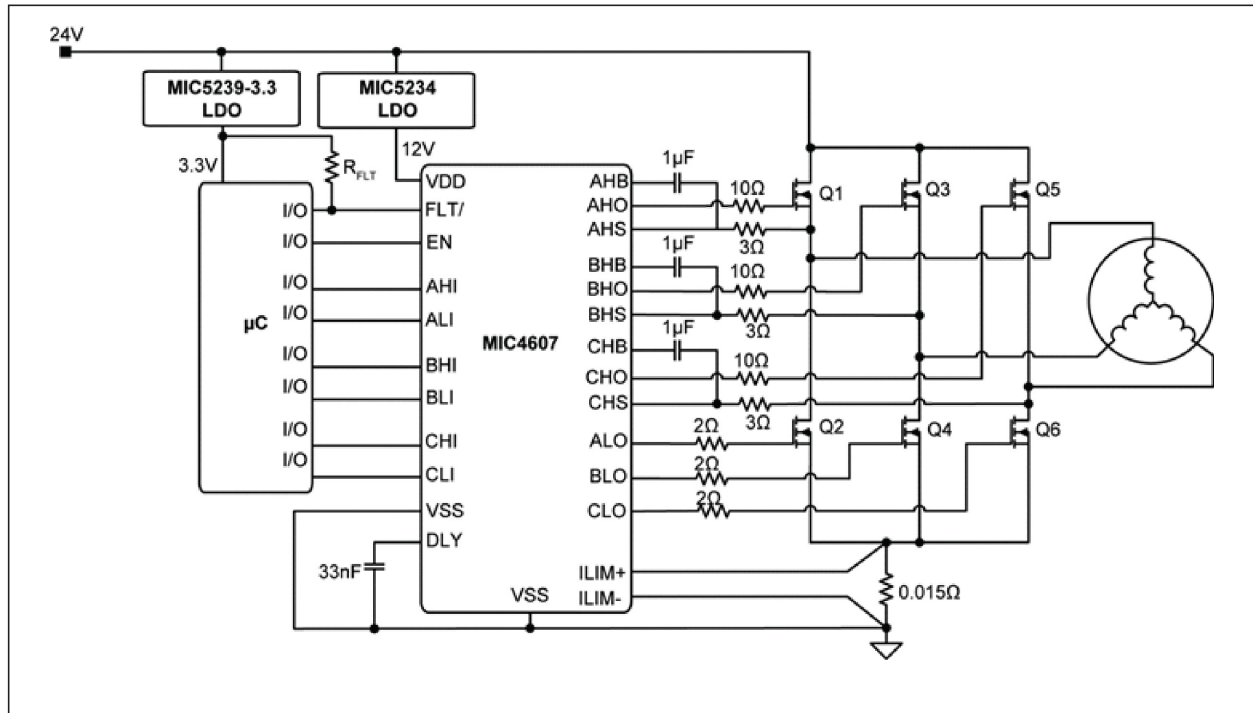


FIGURE 7-2: Industrial Motor Driver.

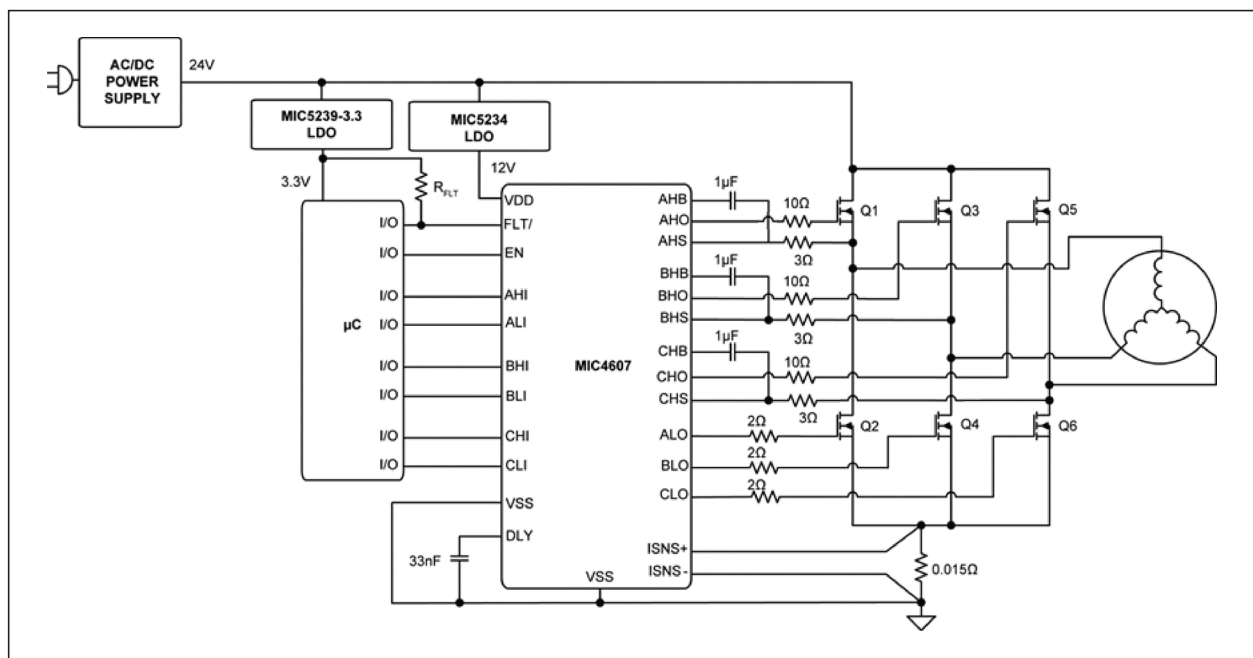


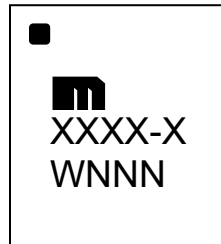
FIGURE 7-3: Blender Motor Drive Application Diagram.



8.0 PACKAGING INFORMATION

8.1 Package Marking Information

24-lead VQFN*



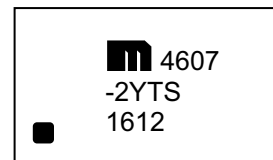
Example



28-lead TSSOP*



Example



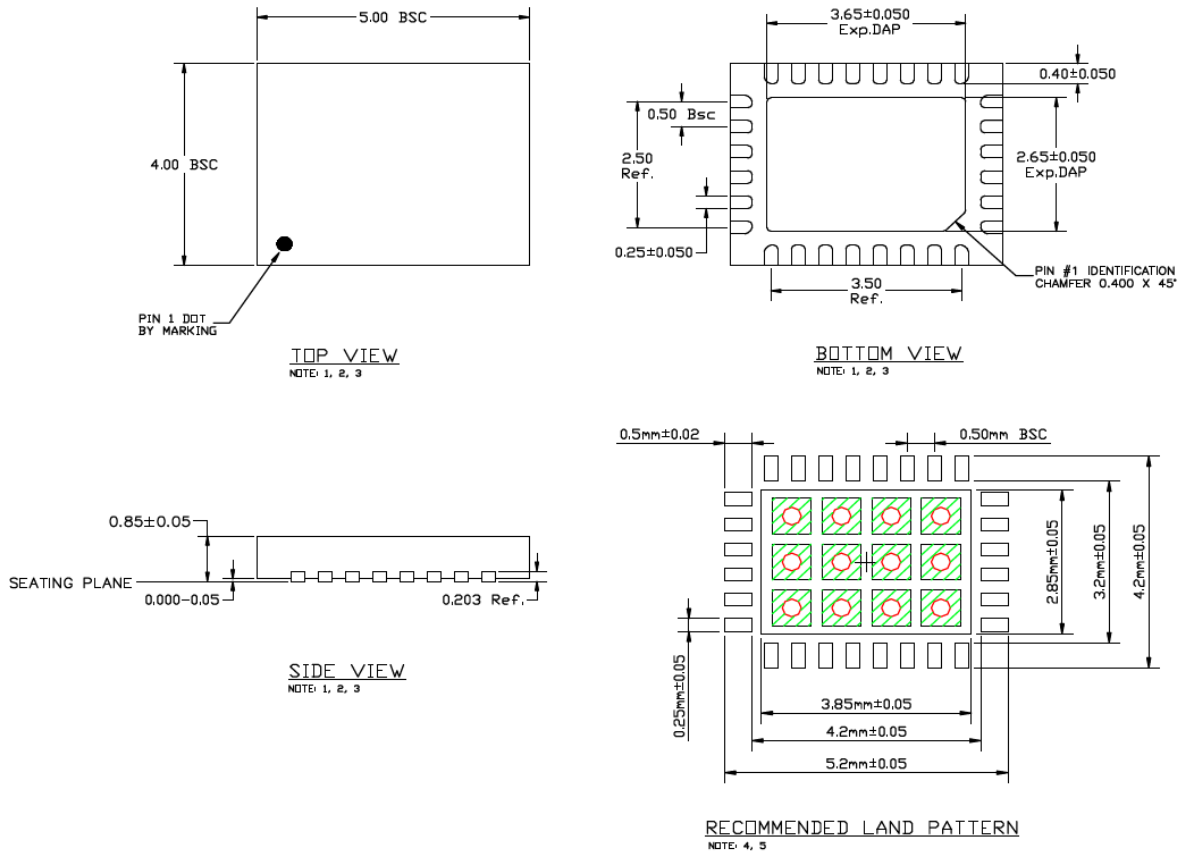
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (¯) and/or Overbar (¯) symbol may not be to scale.	

28-Lead QFN Package Outline and Recommended Land Pattern

TITLE

28 LEAD QFN 4x5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN45-28LD-PL-1	UNIT	MM
Lead Frame	Copper Alloy	Lead Finish	Matte Tin



NOTE:

1. MAX PACKAGE WARPAGE IS 0.05mm
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 0.91mm Pitch.
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.71mmx0.71mm IN SIZE. 0.20mm Gap.

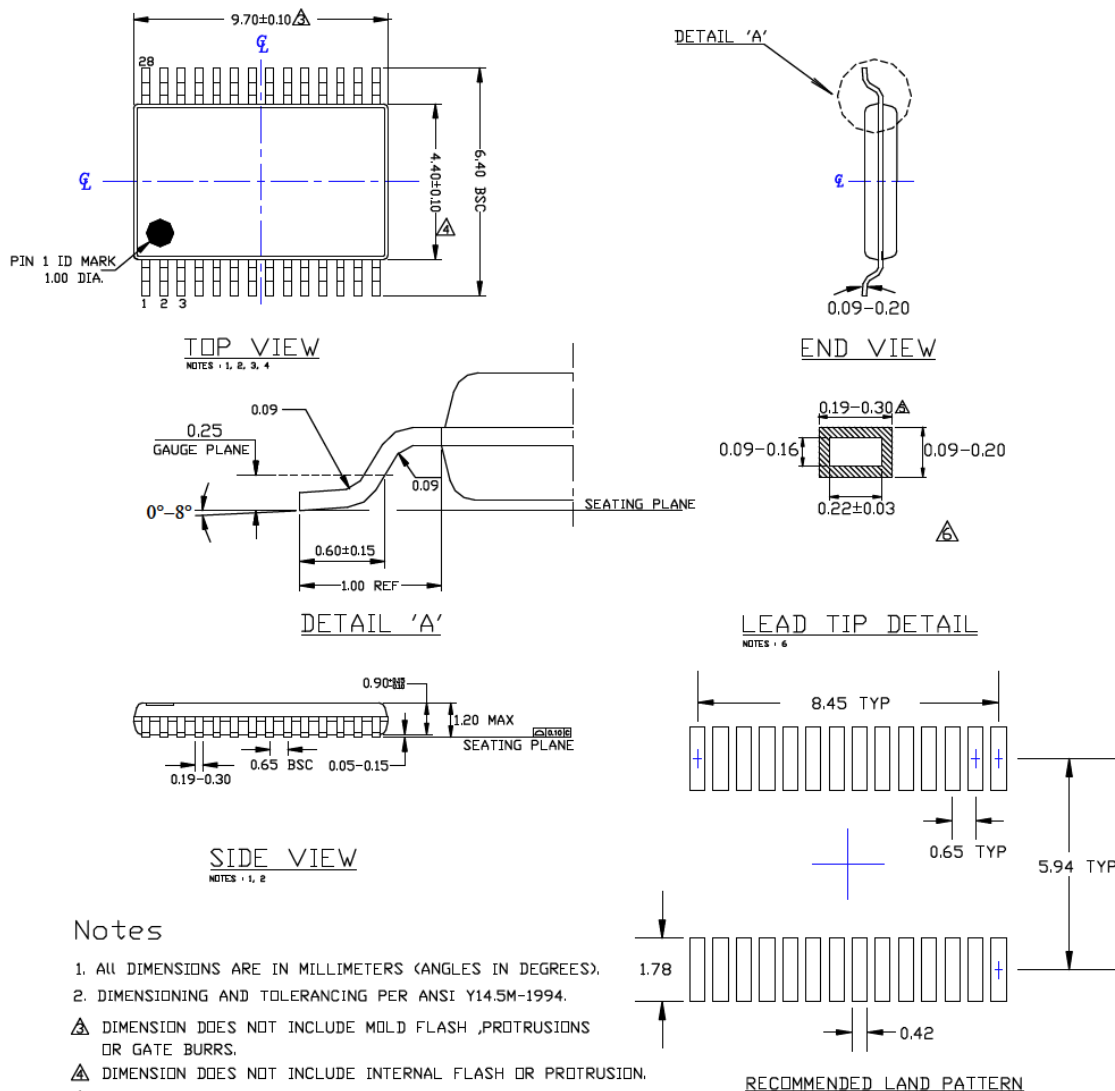
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

28-Lead TSSOP Package Outline and Recommended Land Pattern

TITLE

28 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOP-28LD-PL-1	UNIT	MM [INCH]
-----------	-----------------	------	-----------



Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
- △ DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 - △ DIMENSION DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
 - △ DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 - △ CROSS SECTION TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2016)

- Converted Micrel document MIC4607 to Microchip data sheet template DS20005610A.
- Minor text changes throughout.

Revision B (January 2018)

- Replaced [Figure 6-5](#) with a corrected version.
- Updated values in [Absolute Maximum Ratings †](#), [\(Note 2\)](#) and [Operational Characteristics ††](#), [\(Note 2\)](#) sections.

Revision C (August 2018)

- AEC-Q100 qualification.

Revision D (April 2019)

- Removed statement 'Qualified According to AEC-Q100' from [Features](#).
- Remove statement 'Automotive BLDC Motor Applications' from [Applications](#).

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>		<u>-X</u>	<u>X</u>	<u>XX</u>	<u>-</u>	<u>XX</u>
Device		Input Option	Junction Temperature Range	Package		Media Type
Device:		MIC4607: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection				
Input Option:		1 = Dual Inputs 2 = Single PWM Input				
Temperature Range:		Y = -40°C to +125°C (RoHS Compliant)				
Package:		ML = 28-lead 4x5 QFN TS = 28-lead 5.0x4.4 TSSOP				
Media Type:		T5 = 500/Reel TR = 5000/Reel QFN (ML) Package = 2500/Reel TSSOP (TS) Package <blank>=50/Tube TSSOP (TS) Package				
Examples:		<p>a) MIC4607-1YML-T5: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Dual Inputs, -40°C to +125°C Temperature Range, 28-Pin QFN, 500/Reel.</p> <p>b) MIC4607-1YML-TR: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Dual Inputs, -40°C to +125°C Temp. Range, 28-Pin QFN, 5000/Reel.</p> <p>c) MIC4607-1YTS: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Dual Inputs, -40°C to +125°C Temp. Range, 28-Pin TSSOP, 500/Reel.</p> <p>d) MIC4607-1YTS-T5: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Dual Inputs, -40°C to +125°C Temp. Range, 28-Pin TSSOP, 500/Reel.</p> <p>e) MIC4607-1YTS-TR: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Dual Inputs, -40°C to +125°C Temp. Range, 28-Pin TSSOP, 2500/Reel.</p> <p>f) MIC4607-2YML-T5: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Single PWM Input, -40°C to +125°C Temp. Range, 28-Pin TSSOP, 500/Reel.</p> <p>g) MIC4607-2YML-TR: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Single PWM Input, -40°C to +125°C Temp. Range, 28-Pin TSSOP, 2500/Reel.</p> <p>h) MIC4607-2YTS: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Dual Inputs, -40°C to +125°C Temp. Range, 28-Pin TSSOP, 50/Tube</p>				

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