MX852EB0027

Ultra-Low Jitter XTAL Oscillator with Fanout

Features

- Generates Five Output Clocks
- Frequency and Output Logic:
  - 100 MHz HCSL x 5
- Integrated Quartz Crystal for Frequency Reference
- Typical Phase Noise:
  - 118 fs (Integration Range: 1.875 MHz to 20 MHz)
  - 254 fs (Integration Range: 12 kHz to 20 MHz)
- Complete Ultra-Low Jitter Clocking Solution
- OE on Bank 1 and Bank 2
- 2.5V or 3.3V Operating Voltage Range
- ±50 ppm Total Stability
- –40°C to +85°C Temperature Range
- 38-Pin 5 mm x 7 mm LGA Package

Applications

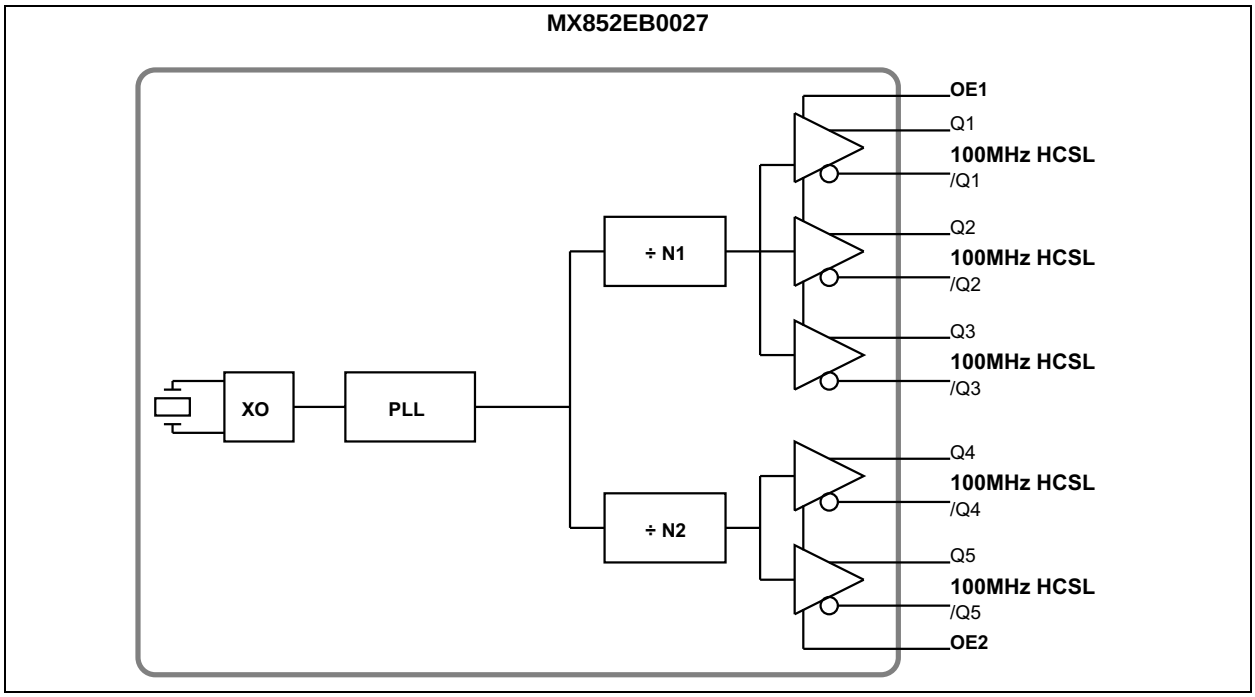
- PCI Express
- Storage

General Description

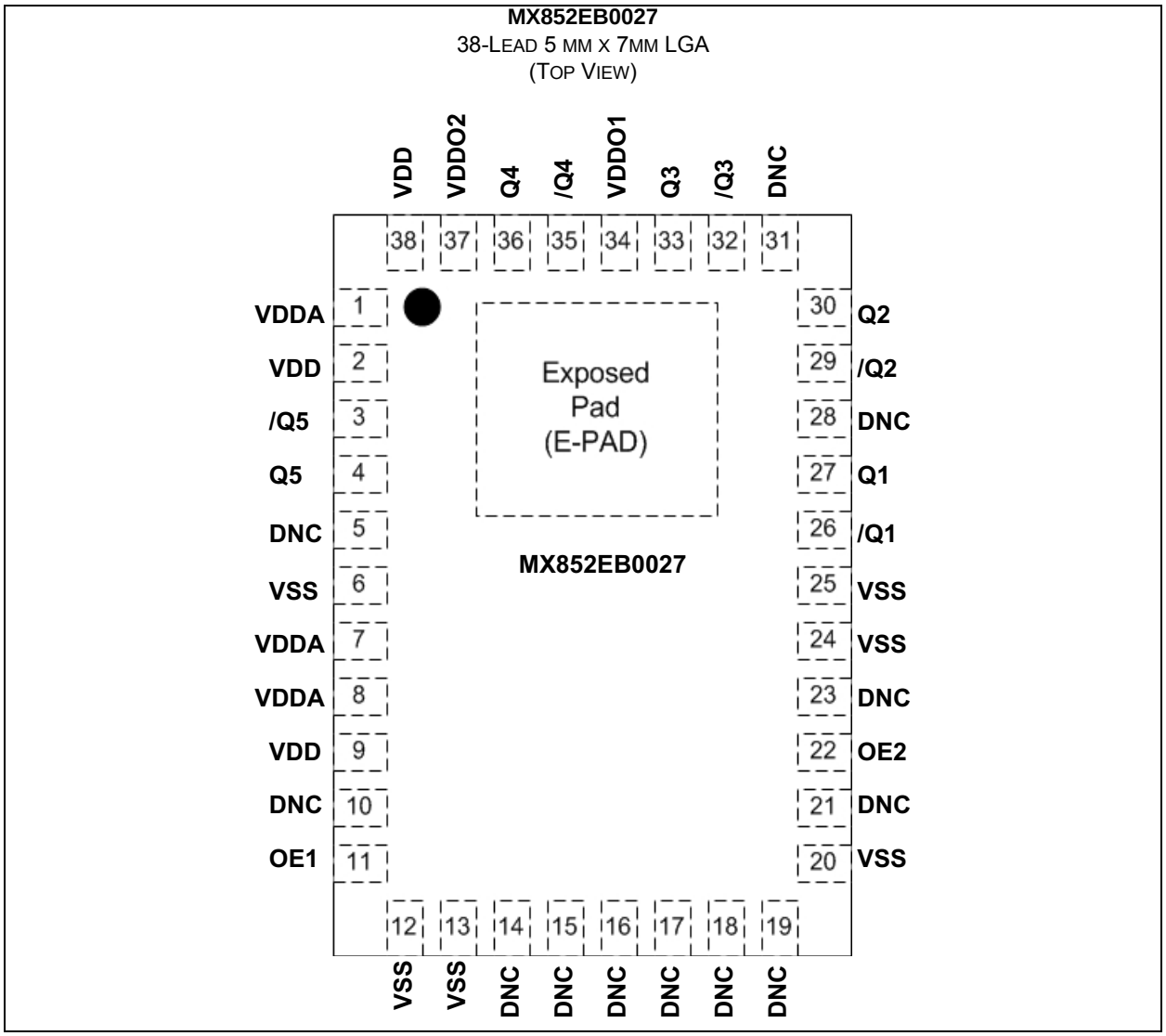
The MX852EB0027 clock management IC (CMIC) is a member of the ClockWorks® FUSION family of devices that integrates the crystal, synthesizer, and fanout buffers in a single 5 mm x 7 mm LGA package.

Integrating the entire clock chain delivers 200 fs typical phase noise performance, including fanout and crosstalk. The device operates from a 2.5V or 3.3V power supply.

Block Diagram



Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DDA}, V_{DD}, V_{DDOx}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD}+0.5V
ESD Human Body Model Rating ..... 2 kV
ESD Machine Model Rating 200V

Operating Ratings ‡

Supply Voltage (V_{DDOx}, V_{DD}, V_{DDA}) ..... +2.375V to +3.465V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{DD} = V_{DDA} = V_{DDO1} = V_{DDO2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$;
$V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO1} = V_{DDO2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$; $T_A = –40°C$ to $+85°C$, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
2.5V Operating Voltage	V_{DDx}	2.375	2.5	2.625	V	—
3.3V Operating Voltage		3.135	3.3	3.465		—
Core Supply Current	I_{DD}	—	—	204	mA	Outputs not loaded.
Output Frequency	f_O	—	100	—	MHz	Bank 1 and Bank 2
Frequency Stability	$f_{STABILITY}$	—	—	±20	ppm	Note 2, Frequency stability over temperature
		—	—	±50		Total stability
Start-Up Time	t_{START}	—	—	20	ms	—
Output-to-Output Skew	t_{SKEW}	—	—	50	ps	Note 3
Output Rise/Fall Time	t_r/t_f	150	300	450	ps	20% - 80%, HCSL output
Output Duty Cycle	ODC	48	50	52	%	<350 MHz output frequencies
RMS Phase Noise 100 MHz HCSL	$t_{jit(Ø)}$	—	254	—	fs	Integration range (12 kHz to 20 MHz)
		—	118	—		Integration range (1.5 MHz to 20 MHz)
		—	260	—		Integration range (12 kHz to 40 MHz)
Period Jitter		—	1.6	—	ps	Peak-to-peak (E5001A, 100 Hz to 40 MHz)
		—	135	—	fs	RMS (E5001A, 100 Hz to 40 MHz)
		—	5	10	ps	Peak-to-peak (10k Samples, DSA80000B)

Note 1: The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics table after thermal equilibrium has been established.

2: Inclusive of temperature drift, aging, initial accuracy, shock, and vibration. Operating temperature range dependent on part number configuration.

3: Skew between output buffers. Measured at the output differential crossing points. Applies to outputs at the same supply voltage using same output format.

TABLE 1-2: LVCMOS INPUTS DC ELECTRICAL CHARACTERISTICS (OE1, OE2)(Note 1)

Electrical Characteristics: $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = –40°C$ to $+85°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2	—	V_{DD}+ 0.3	V	—
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	—
Input High Current	I_{IH}	—	—	150	µA	$V_{DD} = V_{IN} = 3.465V$
Input Low Current	I_{IL}	–150	—	—	µA	$V_{DD} = 3.465V$, $V_{IN} = 0V$

Note 1: The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics table after thermal equilibrium has been established.

TABLE 1-3: HCSL DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V_{DD} = V_{DDO1} = V_{DDO2} = 3.3V ±5% or 2.5V ±5%;
V_{DD} = 3.3V ±5%, V_{DDO1} = V_{DDO2} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{SS}

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	640	700	850	mV	—
Output Low Voltage	V_{OL}	–150	0	27	mV	—
Crossing Point Voltage	V_{CROSS}	250	350	550	mV	—

Note 1: The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics table after thermal equilibrium has been established.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature	T_A	–40	—	+85	°C	—
Package Thermal Resistance						
Thermal Resistance 38-Ld LGA	θ_{JA}	—	38.5	—	°C/W	Still Air

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Pin Level	Description
1, 7, 8	VDDA	PWR	—	Analog Power Supply
2, 9, 38	VDD	PWR	—	Power Supply
3, 4	/Q5, Q5	O, Diff	HCSL	Bank 2 Clock Output Frequency = 100 MHz
5, 14, 15, 16, 17, 18, 19, 21, 23, 28, 31	DNC	—	—	Do not connect anything to these pins.
6, 24, 25, ePAD	VSS (Exposed Pad)	PWR	—	Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
10	DNC	—	—	Do not connect.
11	OE1	I, SE	LVCMOS	Output Enable, Bank 1 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45 kΩ pull-up.
12, 13, 20	VSS	PWR	—	Crystal Ground
22	OE2	I, SE	LVCMOS	Output Enable, Bank 2 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45 kΩ pull-up.
26, 27	/Q1, Q1	O, Diff	HCSL	Bank 1 Clock Output Frequency = 100 MHz
29, 30	/Q2, Q2	O, Diff	HCSL	Bank 1 Clock Output Frequency = 100 MHz
32, 33	/Q3, Q3	O, Diff	HCSL	Bank 1 Clock Output Frequency = 100 MHz
34	VDDO1	PWR	—	Power Supply for the outputs on Bank 1
35, 36	/Q4, Q4	O, Diff	HCSL	Bank 2 Clock Output Frequency = 100 MHz
37	VDDO2	PWR	—	Power Supply for the outputs on Bank 2

3.0 APPLICATION INFORMATION

3.1 Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin and start a 50Ω trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50Ω traces.

For EMI reasons, it is better to use a balanced differential design. LVDS can be AC-coupled or DC-coupled to its termination.

3.2 Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7 nF below) between the V_{DD} and V_{SS} pins, as close as possible to those pins and on the same side of the PCB as the IC. The shorter the physical path from V_{DD} to the capacitor and back from the capacitor to V_{SS}, the more effective the decoupling. Use one 4.7 nF capacitor for each V_{DD} pin.

The impedance value of the Ferrite Bead (FB) needs to be between 80Ω and 240Ω with a saturation current ≥250 mA.

The V_{DDO1} and V_{DDO2} pins connect directly to the V_{DD} plane. All V_{DD} pins connect to V_{DD} after the power supply filter.

4.0 POWER SUPPLY FILTERING RECOMMENDATIONS

Preferred filtering, using a Microchip MIC94325 Ripple Block, is shown in Figure 4-1.

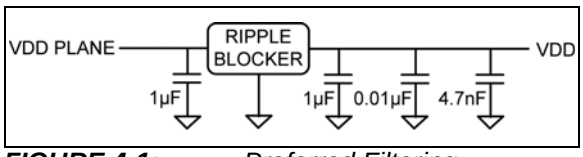


FIGURE 4-1: *Preferred Filtering.*

Figure 4-2 shows an alternative, traditional filter, using a ferrite bead.

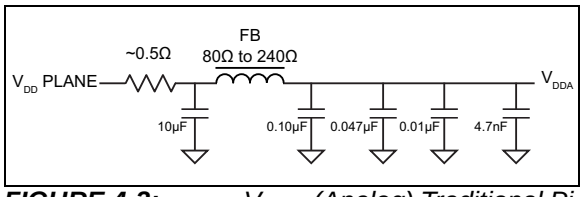


FIGURE 4-2: *V_{DDA} (Analog) Traditional Pi Filter.*

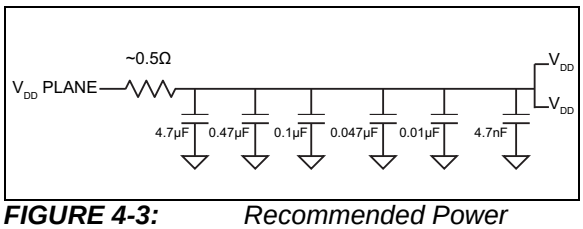


FIGURE 4-3: *Recommended Power Supply Filtering.*

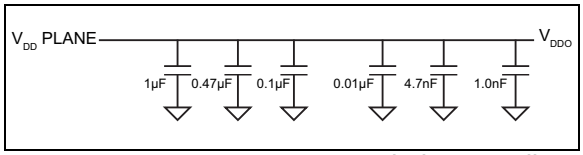


FIGURE 4-4: *Recommended Decoupling for Each V_{DDO}.*

5.0 TIMING DIAGRAMS

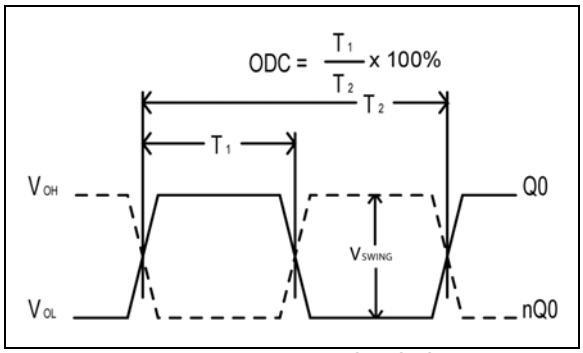


FIGURE 5-1: *Duty Cycle Timing.*

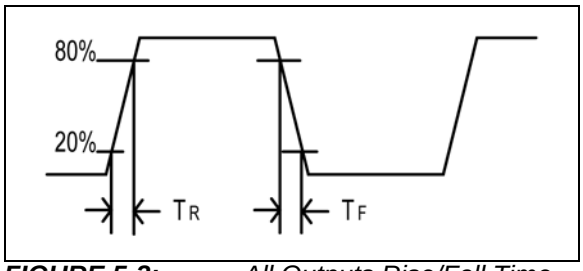


FIGURE 5-2: *All Outputs Rise/Fall Time.*

6.0 RMS PHASE/NOISE/JITTER

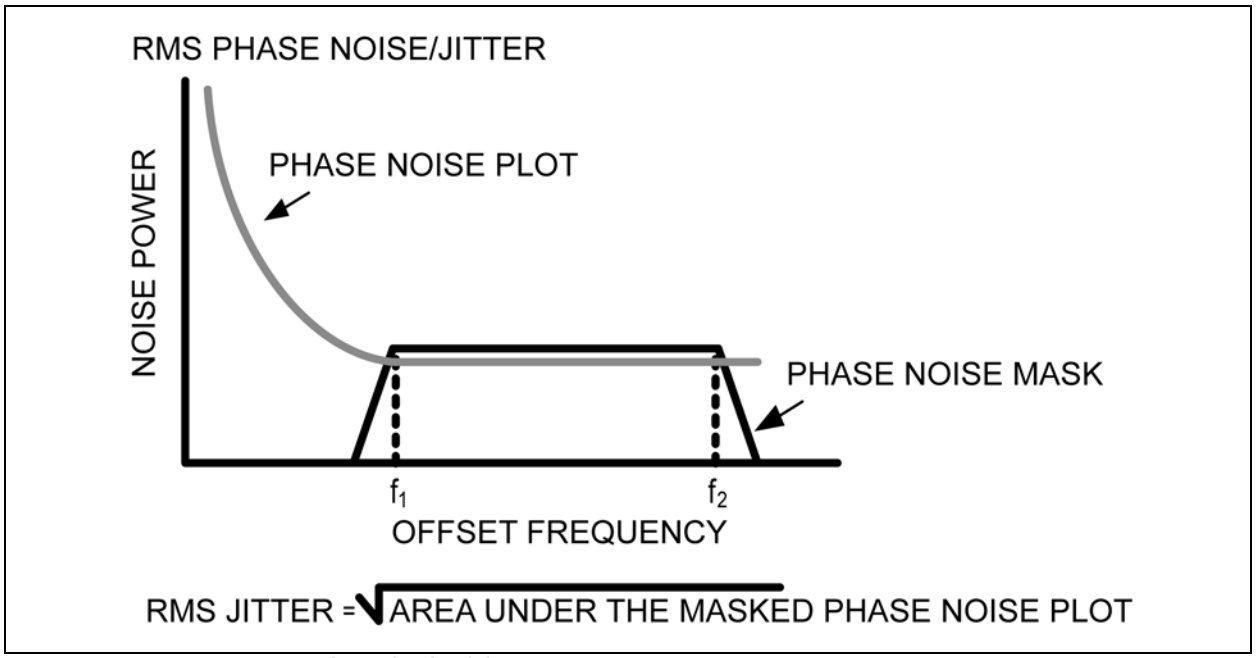


FIGURE 6-1: *RMS Phase/Noise/Jitter.*

7.0 OUTPUT TERMINATION

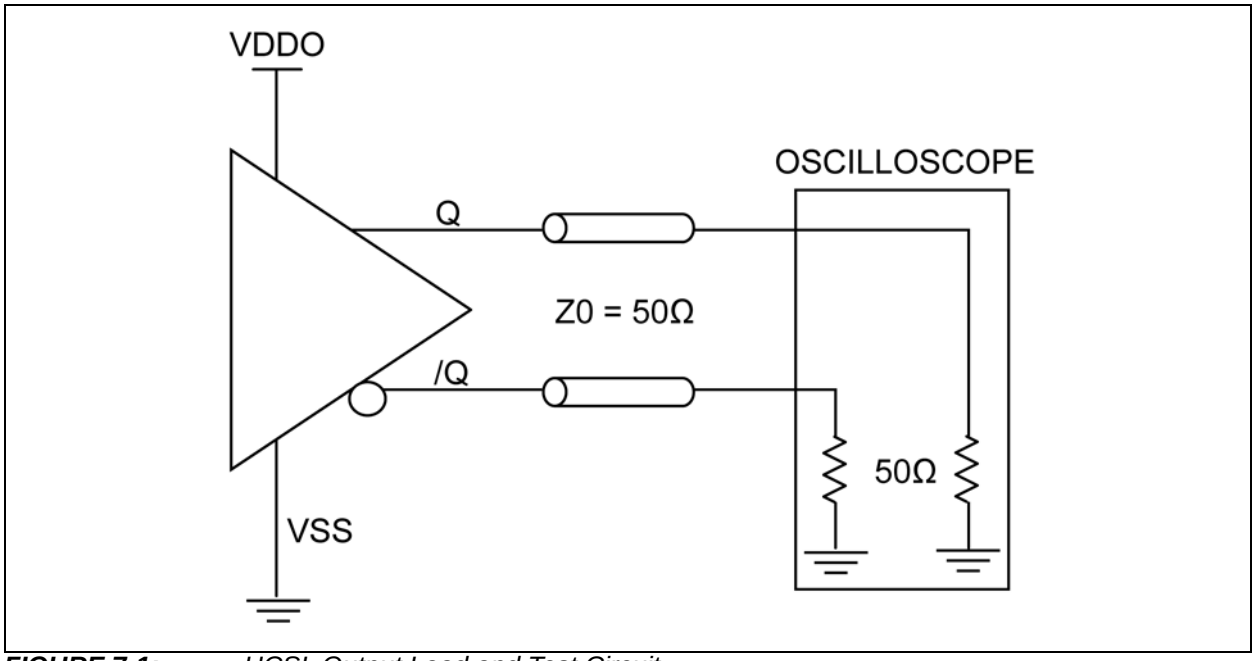


FIGURE 7-1: *HCSL Output Load and Test Circuit.*

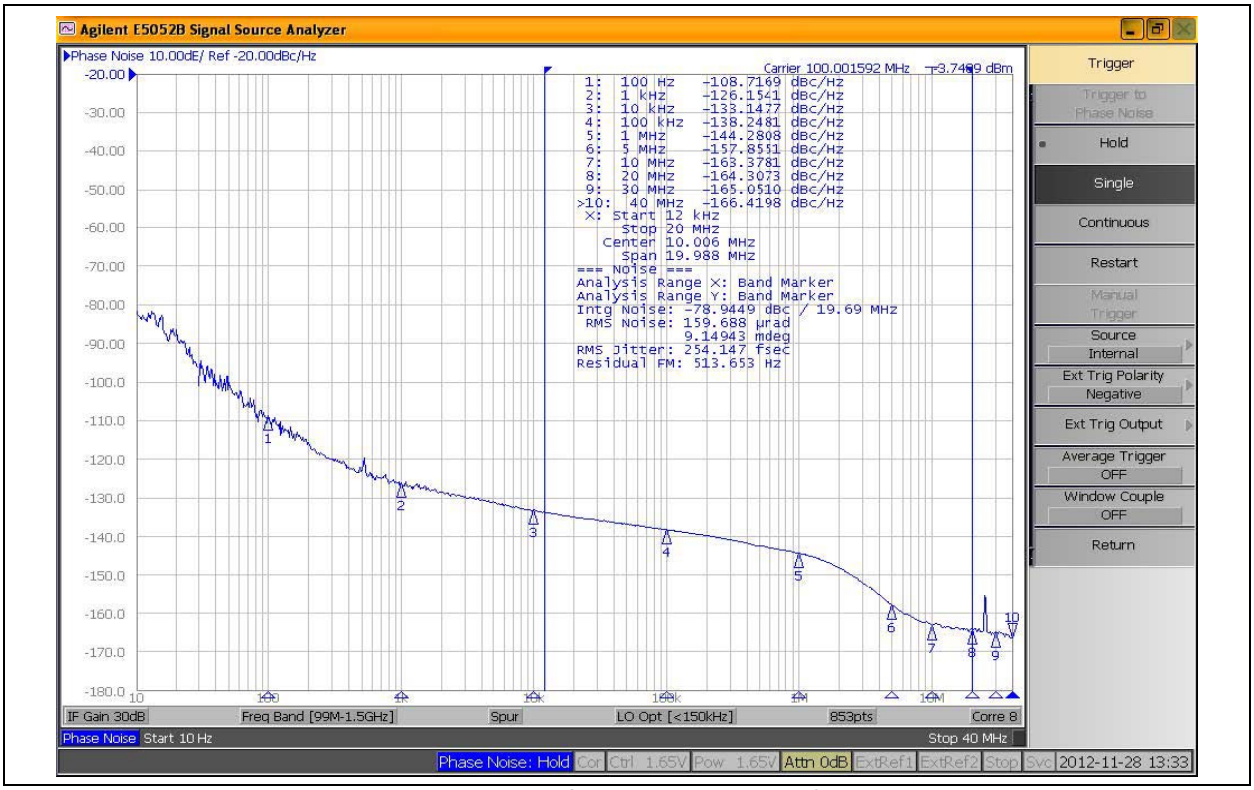


FIGURE 7-2: *100 MHz HCSL Output, 12 kHz to 20 MHz, 254 fs*

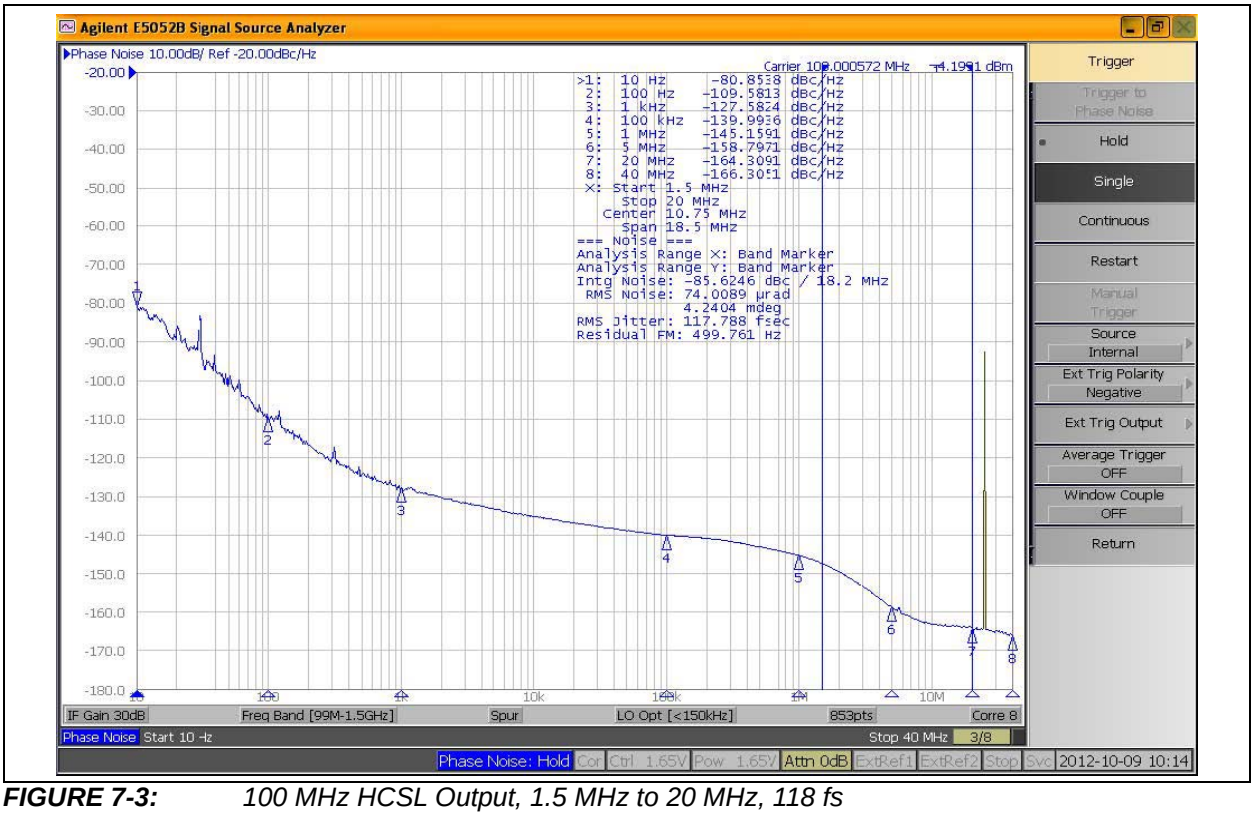


FIGURE 7-3: *100 MHz HCSL Output, 1.5 MHz to 20 MHz, 118 fs*

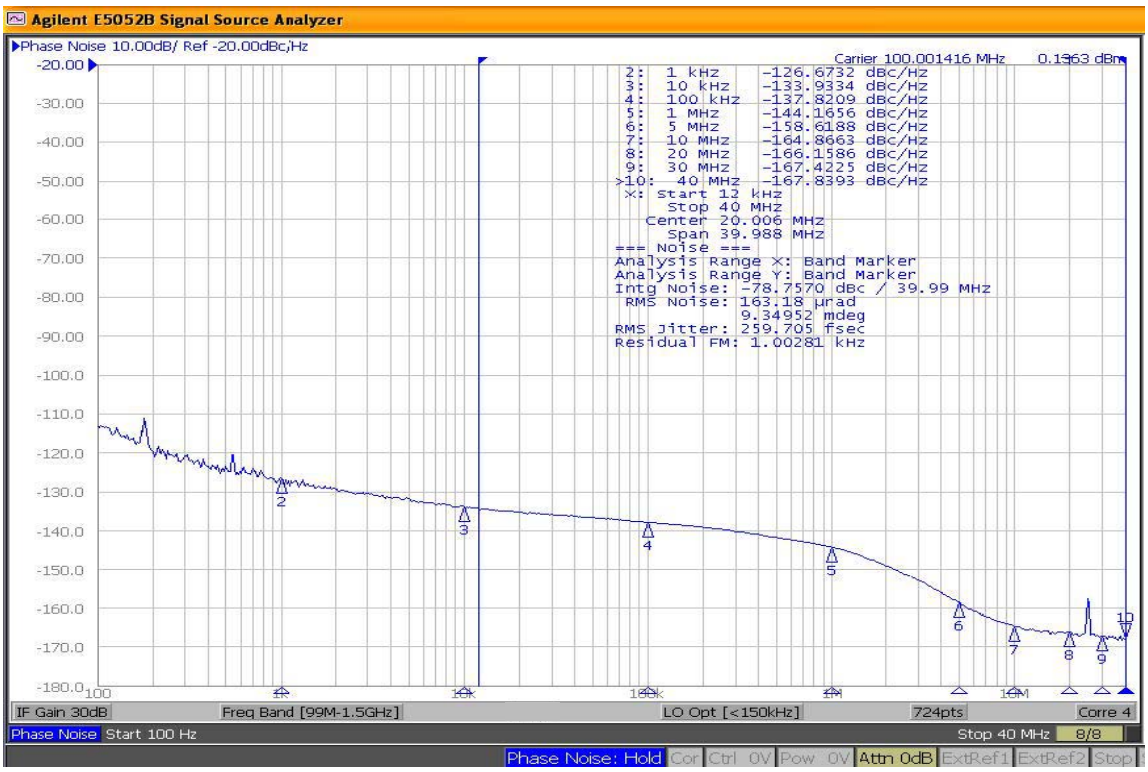


FIGURE 7-4: *100 MHz HCSL Output, 12 kHz to 40 MHz, 260 fs*

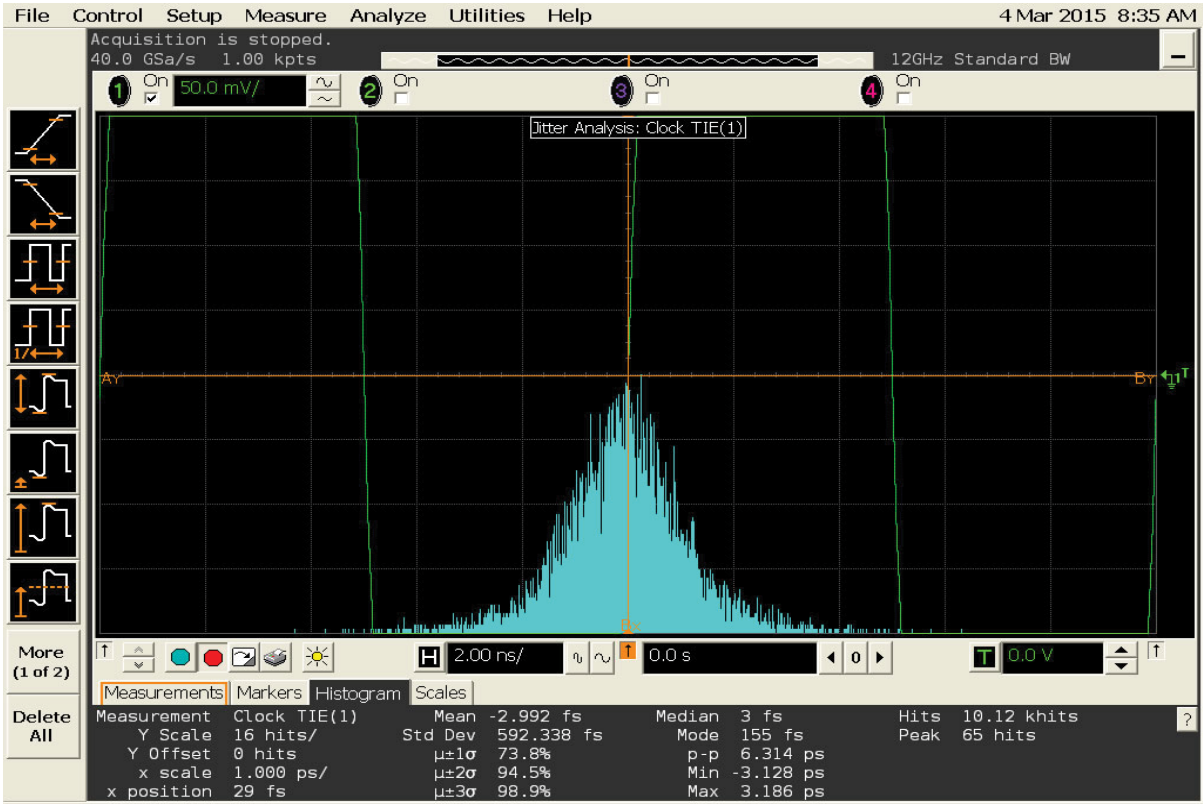


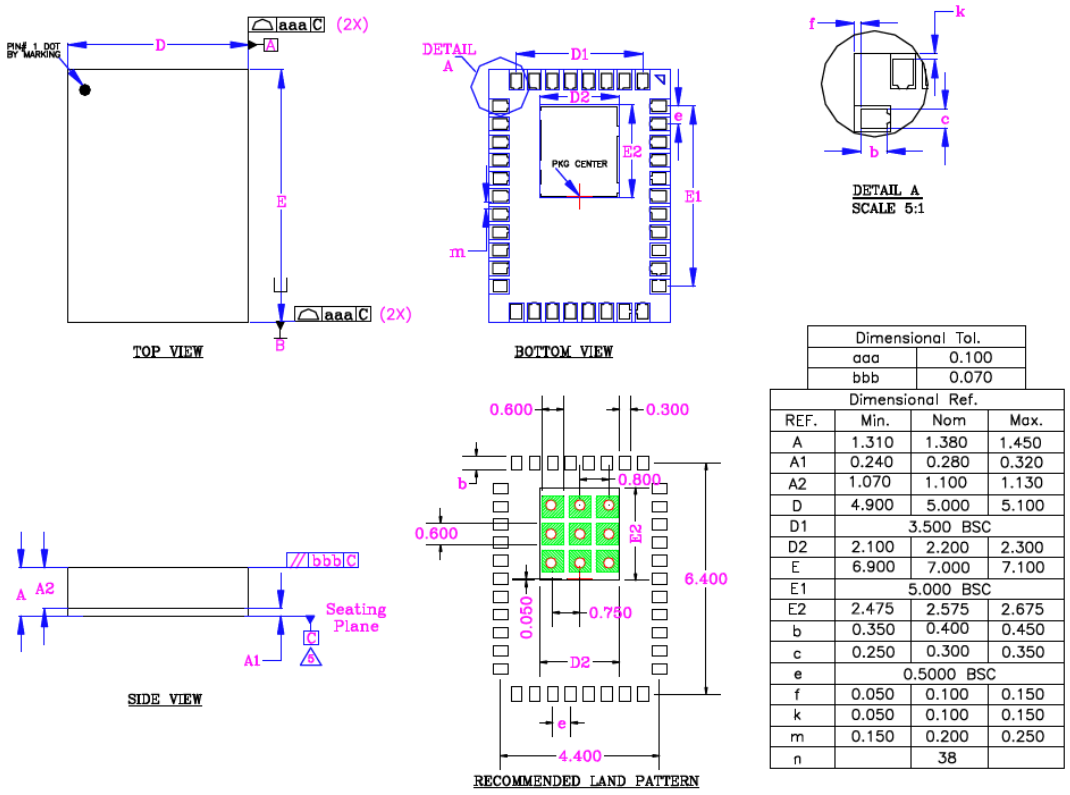
FIGURE 7-5: *TIE Jitter (10k Samples).*

8.0 PACKAGING INFORMATION

38-Lead LGA Package Outline and Recommended Land Pattern

TITLE
38 LEAD LGA 7x5 mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	LGA75-38LD-PL-1	UNIT	MM



Dimensional Tol.	
aaa	0.100
bbb	0.070

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.310	1.380	1.450
A1	0.240	0.280	0.320
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1		3.500 BSC	
D2	2.100	2.200	2.300
E	6.900	7.000	7.100
E1		5.000 BSC	
E2	2.475	2.575	2.675
b	0.350	0.400	0.450
c	0.250	0.300	0.350
e		0.5000 BSC	
f	0.050	0.100	0.150
k	0.050	0.100	0.150
m	0.150	0.200	0.250
n		38	

Notes:
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. 'e' represents the basic LGA pitch
4. 'n' is the maximum no. of Land for a specified Package.
5. Package warp shall be 0.050 max.
6. Substrate base is BT Resin
7. The Pin#1 corner must be identified on top side only.
8. Reference JEDEC Spec M0-220.
9. Red circles in land pattern indicate thermal via. Size should be 0.30mm in diameter. Pitch is 0.80mm and connected to GND for maximum thermal performance.
10. Green rectangles (SHADED AREA) indicate solder stencil opening on exposed pad area. Size is 0.60x0.60mm. Pitch is 0.75mm
11. Land Pattern Tolerance is ±0.02mm.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document MX852EB0027 to Microchip data sheet DS20005749A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–	XX
Device		Media Type

Device:	MX852EB0027:	Ultra-Low Jitter 5 HCSL Output Oscillator at 100 MHz
Media Type:	(blank)=	43/Tube
	TR =	1,000/Reel

Examples:

a) MX852EB0027: Ultra-Low Jitter 5 HCSL Output Oscillator at 100 MHz, 43/Tube

b) MX852EB0027-TR: Ultra-Low Jitter 5 HCSL Output Oscillator at 100 MHz, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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