

## Battery-Backed SPI Real-Time Clock/Calendar with Enhanced Features

### Device Selection Table

| Part Number | EEPROM (Kbits) | Protected EEPROM |
|-------------|----------------|------------------|
| MCP795W10   | 1              | Blank            |
| MCP795W20   | 2              | Blank            |
| MCP795W11   | 1              | EUI-48™          |
| MCP795W21   | 2              | EUI-48™          |
| MCP795W12   | 1              | EUI-64™          |
| MCP795W22   | 2              | EUI-64™          |

### Timekeeping Features

- Real-Time Clock/Calendar (RTCC):
  - Hours, minutes, seconds, hundredth of seconds, day of week, date, month, year
  - Leap year compensated to 2399
  - 12/24-hour modes
- Oscillator for 32.768 kHz Crystals:
  - Optimized for 6-9 pF crystals
- On-Chip Digital Trimming/Calibration:
  - ±1 ppm resolution
  - ±259 ppm range
- Dual Programmable Alarms
- Clock Output Function with Selectable Frequency
- Power-Fail Timestamp:
  - Time logged on switchover to and from Battery mode

### Low-Power Features

- Wide Voltage Range:
  - Operating voltage range of 1.8V to 3.6V
  - Backup voltage range of 1.3V to 3.6V
- Low Typical Timekeeping Current:
  - Operating from VCC: 1.2 µA at 3.0V
  - Operating from VBAT: 1.0 µA at 3.0V
- Automatic Switchover to Battery Backup

### Enhanced Features

- Programmable Watchdog Timer:
  - Dedicated output pin
  - Cleared via SPI bus or EVHS input
- Dual Configurable Event Detect Modules:
  - High-Speed Digital Event Detect for programmable pulse count detection
  - Low-Speed Event Detect for programmable switch debouncing

### User Memory

- 64-Byte Battery-Backed SRAM
- 1 Kbit or 2 Kbit EEPROM:
  - Software write-protect
  - Page write up to 8 bytes
  - Endurance: 1M erase/write cycles
- 128-Bit Protected EEPROM Area:
  - Robust write unlock sequence
  - EUI-48™ MAC address (MCP795WX1)
  - EUI-64™ MAC address (MCP795WX2)

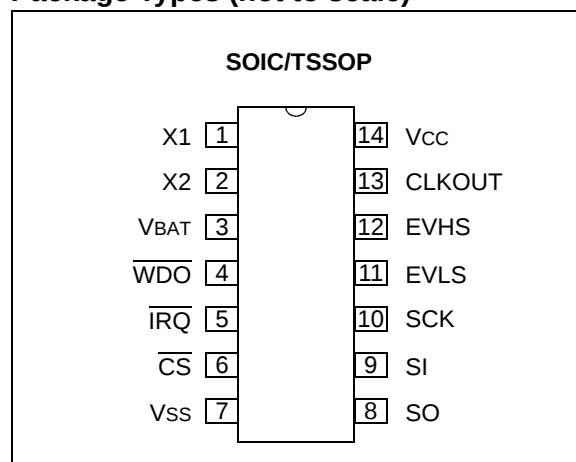
### Operating Ranges

- SPI Serial Interface:
  - SPI clock rate up to 5 MHz
- Temperature Range:
  - Industrial (I): -40°C to +85°C

### Packages

- 14-Lead SOIC and TSSOP

### Package Types (not to scale)



# MCP795W1X/MCP795W2X

## Description

The MCP795WXX Real-Time Clock/Calendar (RTCC) tracks time using internal counters for hours, minutes, seconds, hundredth of seconds, days, months, years and day of week. Alarms can be configured on all counters up to and including months. For usage and configuration, the MCP795WXX supports SPI communications up to 5 MHz.

The MCP795WXX is designed to operate using a 32.768 kHz tuning fork crystal with external crystal load capacitors. On-chip digital trimming can be used to adjust for frequency variance caused by crystal tolerance and temperature.

SRAM and timekeeping circuitry are powered from the backup supply when main power is lost, allowing the device to maintain accurate time and the SRAM contents. The times when the device switches over to the backup supply and when primary power returns are both logged by the power-fail timestamp.

The MCP795WXX features 128 bits of EEPROM which is only writable after an unlock sequence, making it ideal for storing a unique ID or other critical information.

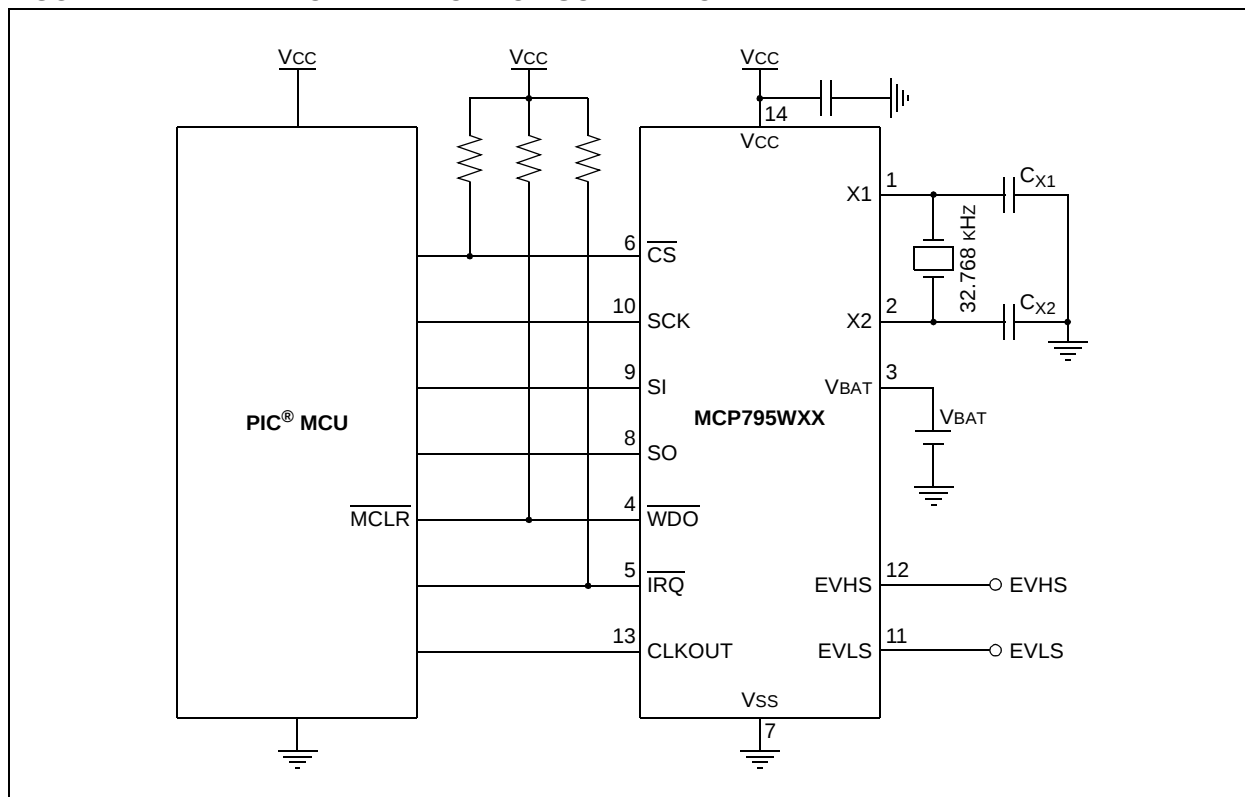
The MCP795WX1 and MCP795WX2 are preprogrammed with EUI-48 and EUI-64 addresses, respectively. Custom programming is also available.

Two event detect modules are included on the MCP795WXX. The high-speed event detect module will generate an interrupt after a programmable number of pulses have been detected. The low-speed event detect module can be used to debounce mechanical switches and includes a selectable debounce period.

The MCP795WXX also features an integrated Watchdog Timer peripheral. This allows applications to improve system robustness by moving this functionality outside of the microcontroller.

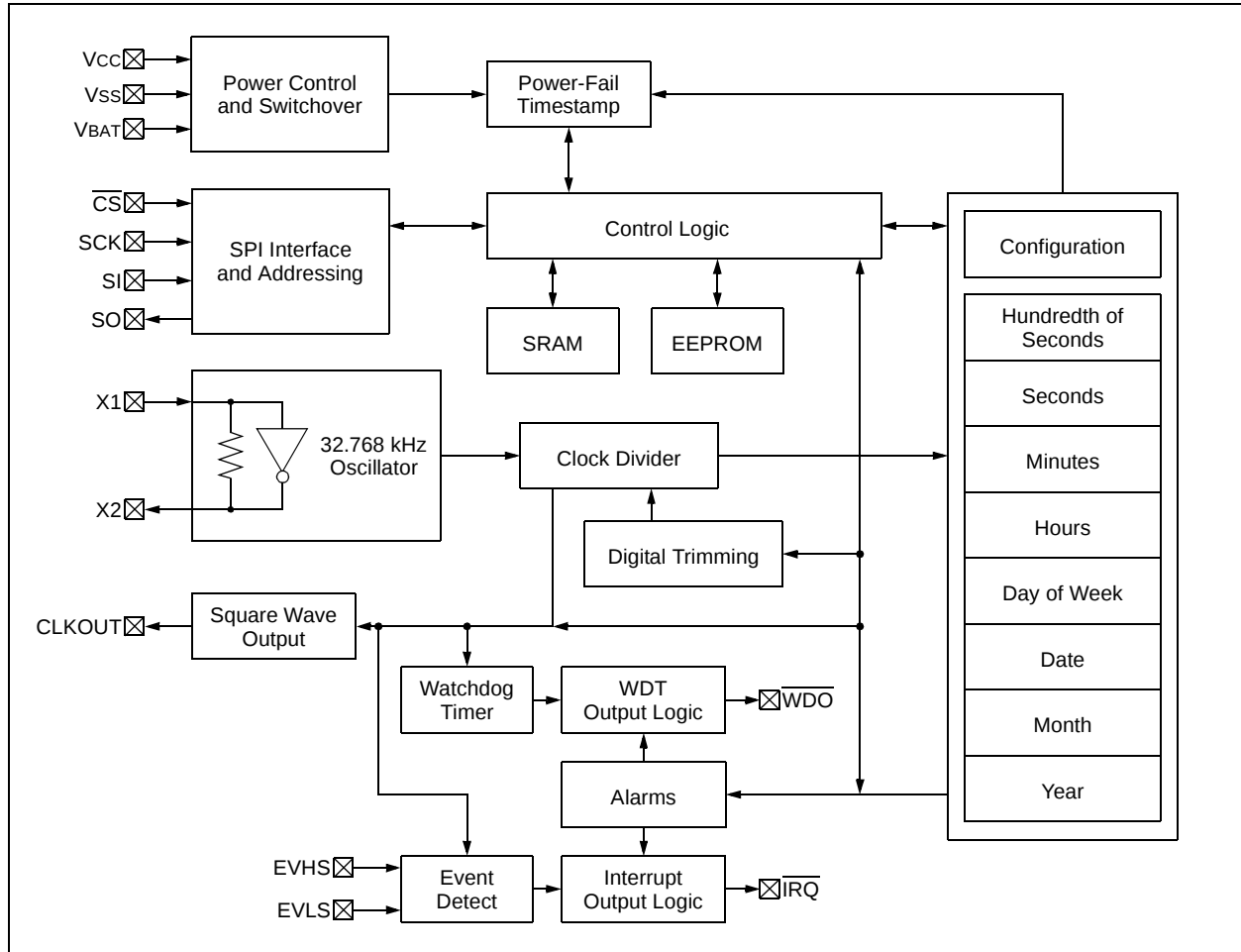
The MCP795WXX has versatile output options. There is a dedicated pin for outputting a selectable frequency square wave or for use as a general purpose output. Additionally, the alarms can be assigned to either the Watchdog Timer interrupt output or the event detect interrupt output.

FIGURE 1-1: TYPICAL APPLICATION SCHEMATIC



# MCP795W1X/MCP795W2X

**FIGURE 1-2: BLOCK DIAGRAM**



# MCP795W1X/MCP795W2X

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings <sup>(†)</sup>

|                                                     |                                |
|-----------------------------------------------------|--------------------------------|
| V <sub>CC</sub> .....                               | 6.5V                           |
| All inputs and outputs w.r.t. V <sub>SS</sub> ..... | -0.6V to V <sub>CC</sub> +1.0V |
| Storage temperature .....                           | -65°C to +150°C                |
| Ambient temperature under bias.....                 | -40°C to +85°C                 |
| ESD protection on all pins.....                     | 4 kV                           |

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| DC CHARACTERISTICS |                      |                                                            | Electrical Characteristics:<br>Industrial (I):      T <sub>A</sub> = -40°C to +85°C      V <sub>CC</sub> = 1.8V to 3.6V |                     |                     |       |                                                                                                  |
|--------------------|----------------------|------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|-------|--------------------------------------------------------------------------------------------------|
| Param. No.         | Sym.                 | Characteristic                                             | Min.                                                                                                                    | Typ. <sup>(2)</sup> | Max.                | Units | Test Conditions                                                                                  |
| D1                 | V <sub>IH</sub>      | High-Level Input Voltage                                   | 0.7 V <sub>CC</sub>                                                                                                     | —                   | V <sub>CC</sub> + 1 | V     |                                                                                                  |
| D2                 | V <sub>IL</sub>      | Low-Level Input Voltage                                    | -0.3                                                                                                                    | —                   | 0.3V <sub>CC</sub>  | V     | V <sub>CC</sub> ≥ 2.5V                                                                           |
|                    |                      |                                                            | -0.3                                                                                                                    | —                   | 0.2V <sub>CC</sub>  |       | V <sub>CC</sub> < 2.5V                                                                           |
| D3                 | V <sub>OL</sub>      | Low-Level Output Voltage                                   | —                                                                                                                       | —                   | 0.4                 | V     | I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 2.5V                                                 |
|                    |                      |                                                            | —                                                                                                                       | —                   | 0.2                 |       | I <sub>OL</sub> = 1.0 mA, V <sub>CC</sub> < 2.5V                                                 |
| D4                 | V <sub>OH</sub>      | High-Level Output Voltage                                  | V <sub>CC</sub> - 0.5                                                                                                   | —                   | —                   | V     | I <sub>OH</sub> = -400 μA                                                                        |
| D5                 | I <sub>LI</sub>      | Input Leakage Current                                      | —                                                                                                                       | —                   | ±1                  | μA    | $\overline{\text{CS}}$ = V <sub>CC</sub> , V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>  |
| D6                 | I <sub>LO</sub>      | Output Leakage Current                                     | —                                                                                                                       | —                   | ±1                  | μA    | $\overline{\text{CS}}$ = V <sub>CC</sub> , V <sub>OUT</sub> = V <sub>SS</sub> or V <sub>CC</sub> |
| D7                 | C <sub>INT</sub>     | Pin Capacitance<br>(all inputs and outputs)                | —                                                                                                                       | —                   | 7                   | pF    | V <sub>CC</sub> = 3.6V ( <b>Note 1</b> )<br>T <sub>A</sub> = 25°C, f = 1 MHz                     |
| D8                 | C <sub>OSC</sub>     | Oscillator Pin Capacitance<br>(X1, X2 pins)                | —                                                                                                                       | 3                   | —                   | pF    | <b>Note 1</b>                                                                                    |
| D9                 | IC <sub>CEERD</sub>  | EEPROM Operating Current                                   | —                                                                                                                       | —                   | 3                   | mA    | V <sub>CC</sub> = 3.6V, F <sub>CLK</sub> = 5 MHz<br>SO = Open                                    |
|                    | IC <sub>CEEWR</sub>  |                                                            |                                                                                                                         |                     | 5                   | mA    | V <sub>CC</sub> = 3.6V                                                                           |
| D10                | IC <sub>CREAD</sub>  | SRAM/RTCC Operating Current                                | —                                                                                                                       | —                   | 3                   | mA    | V <sub>CC</sub> = 3.6V, F <sub>CLK</sub> = 5 MHz<br>SO = Open                                    |
|                    | IC <sub>CWRITE</sub> |                                                            |                                                                                                                         |                     | 3                   | mA    | V <sub>CC</sub> = 3.6V, F <sub>CLK</sub> = 5 MHz                                                 |
| D11                | IC <sub>CDAT</sub>   | V <sub>CC</sub> Data Retention Current<br>(oscillator off) | —                                                                                                                       | —                   | 1                   | μA    | V <sub>CC</sub> = 3.6V                                                                           |

**Note 1:** This parameter is not tested but ensured by characterization.

**2:** Typical measurements taken at room temperature.

# MCP795W1X/MCP795W2X

| DC CHARACTERISTICS (Continued) |         |                                              | Electrical Characteristics:                                                                                  |                     |      |               |                                                                                                                     |
|--------------------------------|---------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------|---------------------|------|---------------|---------------------------------------------------------------------------------------------------------------------|
|                                |         |                                              | Industrial (I): $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{CC} = 1.8\text{V}$ to $3.6\text{V}$ |                     |      |               |                                                                                                                     |
| Param. No.                     | Sym.    | Characteristic                               | Min.                                                                                                         | Typ. <sup>(2)</sup> | Max. | Units         | Test Conditions                                                                                                     |
| D12                            | ICCT    | Timekeeping Current                          | —                                                                                                            | —                   | 1.2  | $\mu\text{A}$ | $V_{CC} = 1.8\text{V}$ , $\overline{\text{CS}} = V_{CC}$ , $\text{EVHS} = V_{SS}$ , $\text{EVLS} = V_{SS}$ (Note 1) |
|                                |         |                                              | —                                                                                                            | 1.2                 | 1.8  | $\mu\text{A}$ | $V_{CC} = 3.0\text{V}$ , $\overline{\text{CS}} = V_{CC}$ , $\text{EVHS} = V_{SS}$ , $\text{EVLS} = V_{SS}$ (Note 1) |
|                                |         |                                              | —                                                                                                            | —                   | 2.6  | $\mu\text{A}$ | $V_{CC} = 3.6\text{V}$ , $\overline{\text{CS}} = V_{CC}$ , $\text{EVHS} = V_{SS}$ , $\text{EVLS} = V_{SS}$ (Note 1) |
| D13                            | VTRIP   | Power-Fail Switchover Voltage                | 1.3                                                                                                          | 1.5                 | 1.7  | V             |                                                                                                                     |
| D14                            | VBAT    | Backup Supply Voltage Range                  | 1.3                                                                                                          | —                   | 3.6  | V             |                                                                                                                     |
| D15                            | IBATT   | Timekeeping Backup Current                   | —                                                                                                            | —                   | 850  | nA            | $V_{BAT} = 1.3\text{V}$ , $V_{CC} = V_{SS}$ (Note 1)                                                                |
|                                |         |                                              | —                                                                                                            | 1000                | 1200 | nA            | $V_{BAT} = 3.0\text{V}$ , $V_{CC} = V_{SS}$ (Note 1)                                                                |
|                                |         |                                              | —                                                                                                            | —                   | 2300 | nA            | $V_{BAT} = 3.6\text{V}$ , $V_{CC} = V_{SS}$ (Note 1)                                                                |
| D16                            | IBATDAT | VBAT Data-Retention Current (oscillator off) | —                                                                                                            | —                   | 850  | nA            | $V_{BAT} = 3.6\text{V}$ , $V_{CC} = V_{SS}$                                                                         |

**Note 1:** This parameter is not tested but ensured by characterization.

**2:** Typical measurements taken at room temperature.

# MCP795W1X/MCP795W2X

**TABLE 1-2: AC CHARACTERISTICS**

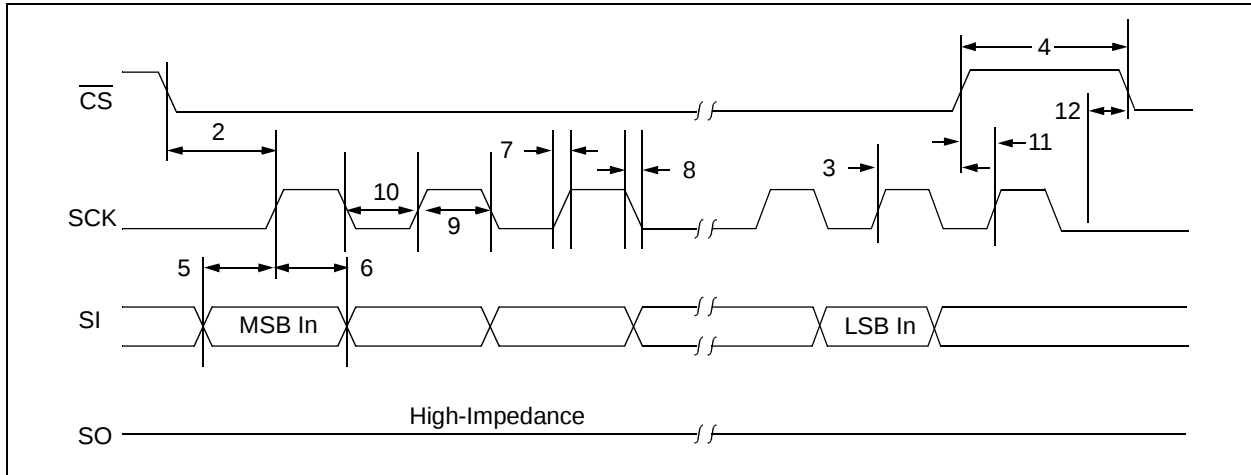
| AC CHARACTERISTICS |       |                                     | Electrical Characteristics:<br>Industrial (I): $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{CC} = 1.8\text{V}$ to $3.6\text{V}$ |        |      |               |                                                                    |
|--------------------|-------|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|--------|------|---------------|--------------------------------------------------------------------|
| Param. No.         | Sym.  | Characteristic                      | Min.                                                                                                                                        | Typ.   | Max. | Units         | Test Conditions                                                    |
| 1                  | FCLK  | Clock Frequency                     | —                                                                                                                                           | —      | 5    | MHz           | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | —                                                                                                                                           | —      | 3    | MHz           | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 2                  | TCSS  | $\overline{\text{CS}}$ Setup Time   | 100                                                                                                                                         | —      | —    | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | 150                                                                                                                                         | —      | —    | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 3                  | TCSH  | $\overline{\text{CS}}$ Hold Time    | 100                                                                                                                                         | —      | —    | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | 150                                                                                                                                         | —      | —    | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 4                  | TCSD  | $\overline{\text{CS}}$ Disable Time | 50                                                                                                                                          | —      | —    | ns            |                                                                    |
| 5                  | TSU   | Data Setup Time                     | 20                                                                                                                                          | —      | —    | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | 30                                                                                                                                          | —      | —    | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 6                  | THD   | Data Hold Time                      | 40                                                                                                                                          | —      | —    | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | 50                                                                                                                                          | —      | —    | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 7                  | TR    | SCK Rise Time                       | —                                                                                                                                           | —      | 100  | ns            | Note 1                                                             |
| 8                  | TF    | SCK Fall Time                       | —                                                                                                                                           | —      | 100  | ns            | Note 1                                                             |
| 9                  | THI   | Clock High Time                     | 100                                                                                                                                         | —      | —    | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | 150                                                                                                                                         | —      | —    | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 10                 | TLO   | Clock Low Time                      | 100                                                                                                                                         | —      | —    | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | 150                                                                                                                                         | —      | —    | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 11                 | TCLD  | Clock Delay Time                    | 50                                                                                                                                          | —      | —    | ns            |                                                                    |
| 12                 | TCLE  | Clock Enable Time                   | 50                                                                                                                                          | —      | —    | ns            |                                                                    |
| 13                 | TV    | Output Valid from Clock Low         | —                                                                                                                                           | —      | 100  | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$                            |
|                    |       |                                     | —                                                                                                                                           | —      | 160  | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$                            |
| 14                 | THO   | Output Hold Time                    | 0                                                                                                                                           | —      | —    | ns            | Note 1                                                             |
|                    |       |                                     | —                                                                                                                                           | —      | —    | ns            |                                                                    |
| 15                 | TDIS  | Output Disable Time                 | —                                                                                                                                           | —      | 80   | ns            | $2.5\text{V} \leq V_{CC} < 3.6\text{V}$ (Note 1)                   |
|                    |       |                                     | —                                                                                                                                           | —      | 160  | ns            | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$ (Note 1)                   |
| 16                 | TWC   | Internal Write Cycle Time           | —                                                                                                                                           | —      | 5    | ms            | Note 2                                                             |
| 17                 | TFVCC | VCC Fall Time                       | 300                                                                                                                                         | —      | —    | $\mu\text{s}$ | Note 1                                                             |
| 18                 | TRVCC | VCC Rise Time                       | 0                                                                                                                                           | —      | —    | $\mu\text{s}$ | Note 1                                                             |
| 19                 | FOSC  | Oscillator Frequency                | —                                                                                                                                           | 32.768 | —    | kHz           |                                                                    |
| 20                 | TOSF  | Oscillator Timeout Period           | —                                                                                                                                           | 1      | —    | ms            | Note 1                                                             |
| 21                 |       | Endurance                           | 1M                                                                                                                                          | —      | —    | E/W cycles    | Page Mode, $25^{\circ}\text{C}$<br>$V_{CC} = 3.6\text{V}$ (Note 1) |

**Note 1:** This parameter is not tested but ensured by characterization.

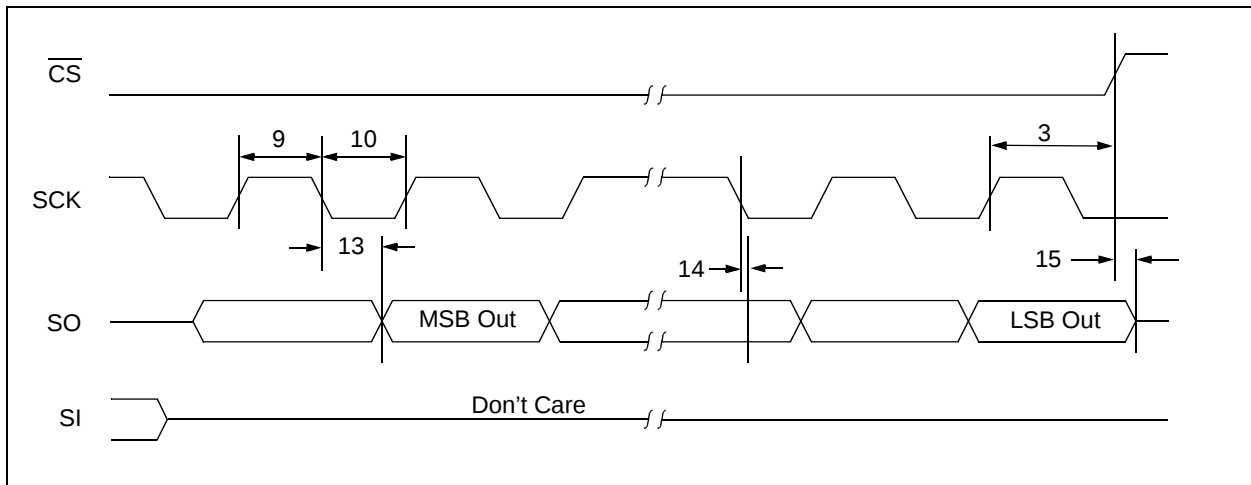
**2:** Twc begins on the rising edge of  $\overline{\text{CS}}$  after a valid write sequence and ends when the internal write cycle is complete.

# MCP795W1X/MCP795W2X

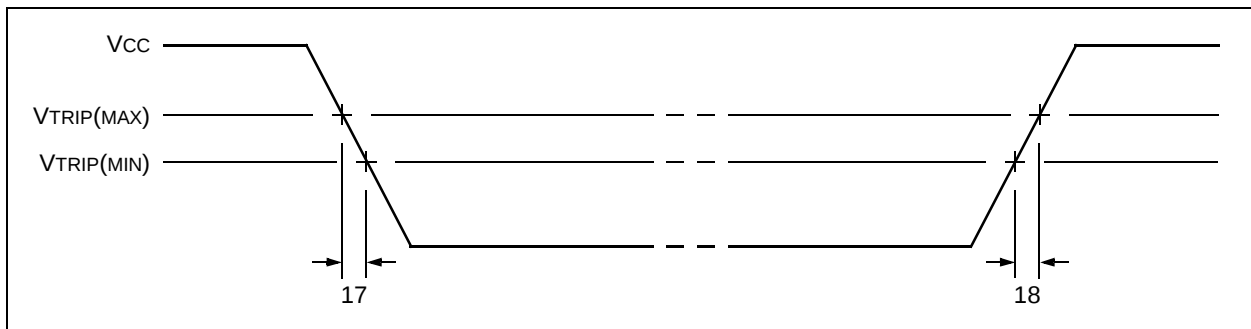
**FIGURE 1-1: SERIAL INPUT TIMING**



**FIGURE 1-2: SERIAL OUTPUT TIMING**



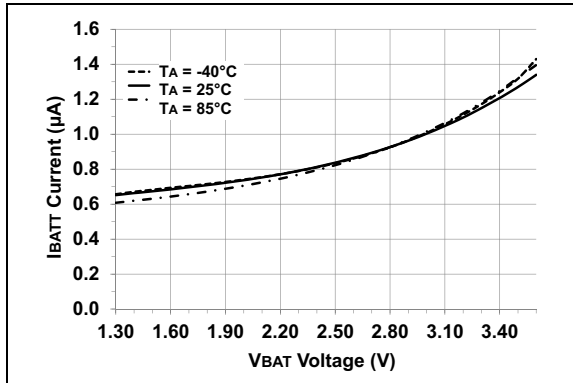
**FIGURE 1-3: POWER SUPPLY TRANSITION TIMING**



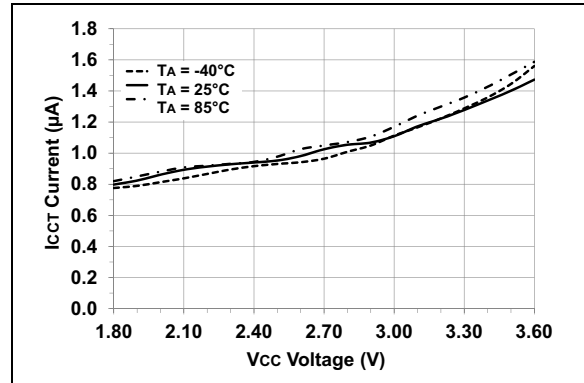
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data represented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 2-1: TIMEKEEPING BACKUP CURRENT VS. BACKUP SUPPLY VOLTAGE**



**FIGURE 2-2: TIMEKEEPING CURRENT VS. SUPPLY VOLTAGE**



## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

| Name                    | 14-pin SOIC | 14-pin TSSOP | Pin Function                                    |
|-------------------------|-------------|--------------|-------------------------------------------------|
| X1                      | 1           | 1            | Quartz Crystal Input, External Oscillator Input |
| X2                      | 2           | 2            | Quartz Crystal Output                           |
| VBAT                    | 3           | 3            | Battery Backup Supply Input                     |
| $\overline{\text{WDO}}$ | 4           | 4            | Watchdog Output                                 |
| $\overline{\text{IRQ}}$ | 5           | 5            | Interrupt Output                                |
| $\overline{\text{CS}}$  | 6           | 6            | Chip Select Input                               |
| VSS                     | 7           | 7            | Ground                                          |
| SO                      | 8           | 8            | Serial Data Output                              |
| SI                      | 9           | 9            | Serial Data Input                               |
| SCK                     | 10          | 10           | Serial Clock Input                              |
| EVHS                    | 11          | 11           | High-Speed Event Detect Input                   |
| EVLS                    | 12          | 12           | Low-Speed Event Detect Input                    |
| CLKOUT                  | 13          | 13           | Square Wave Clock Output                        |
| VCC                     | 14          | 14           | Primary Power Supply                            |

### 3.1 Chip Select ( $\overline{\text{CS}}$ )

A low level on this pin selects the device, whereas a high level deselects the device. A nonvolatile memory programming cycle which is already initiated or in progress will be completed, regardless of the  $\overline{\text{CS}}$  input signal. When the device is deselected, SO goes into the high-impedance state, allowing multiple parts to share the same SPI bus. After power-up, a high-to-low transition on CS is required prior to any sequence being initiated.

### 3.2 Serial Clock (SCK)

This pin is used to synchronize the communication between a master and the MCP795WXX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

### 3.3 Serial Input (SI)

This pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

### 3.4 Serial Output (SO)

This pin is used to transfer data out of the MCP795WXX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

### 3.5 Oscillator Input/Output (X1, X2)

These pins are used as the connections for an external 32.768 kHz quartz crystal and load capacitors. X1 is the crystal oscillator input and X2 is the output. The MCP795WXX is designed to allow for the use of external load capacitors in order to provide additional flexibility when choosing external crystals. The MCP795WXX is optimized for crystals with a specified load capacitance of 6-9 pF.

X1 also serves as the external clock input when the MCP795WXX is configured to use an external oscillator.

### 3.6 Watchdog Output ( $\overline{\text{WDO}}$ )

This is an output pin for the Watchdog Timer and, optionally, the alarms. During normal operation, the pin remains high. If a Watchdog Timer overflow occurs, the pin outputs a low pulse. The width of the pulse is user-selectable.

If an alarm output is assigned to the  $\overline{\text{WDO}}$  pin, then the pin will output a low pulse when the alarm triggers.

The  $\overline{\text{WDO}}$  pin is an open-drain output and requires a pull-up resistor to VCC (typically 10 k $\Omega$ ). This pin may be left floating if not used.

## 3.7 Interrupt Output ( $\overline{\text{IRQ}}$ )

This is an output pin for the event detect modules and, optionally, the alarms. If an event is detected by either module, then this pin will output a low signal until the interrupt flag has been cleared.

If an alarm output is assigned to the  $\overline{\text{IRQ}}$  pin, then the pin will output a low signal when the alarm triggers. The pin will remain low until the alarm interrupt flag has been cleared.

The  $\overline{\text{IRQ}}$  pin is an open-drain output and requires a pull-up resistor to VCC or VBAT (typically 10 k $\Omega$ ). This pin may be left floating if not used.

## 3.8 Square Wave Clock Output (CLKOUT)

This is the output pin for the square wave output function. This pin may be left floating if not used.

## 3.9 High-Speed Event Detect Input (EVHS)

This pin is used as the input for the high-speed event detect module.

If the high-speed event detect module is not being used, the EVHS pin should be connected to VCC or VSS.

## 3.10 Low-Speed Event Detect Input (EVLS)

This pin is used as the input for the low-speed event detect module.

If the low-speed event detect module is not being used, the EVLS pin should be connected to VCC or VSS.

## 3.11 Backup Supply (VBAT)

This is the input for a backup supply to maintain the RTCC and SRAM registers during the time when VCC is unavailable.

Power should be applied to VCC before VBAT.

If the battery backup feature is not being used, the VBAT pin should be connected to VSS.

## 4.0 SPI BUS OPERATION

The MCP795WXX is designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

The MCP795WXX contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The  $\overline{CS}$  pin must be low for the entire operation.

Table 4-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after  $\overline{CS}$  goes low.

**TABLE 4-1: INSTRUCTION SET SUMMARY**

| Instruction Name | Instruction Format | Description                                                                 |
|------------------|--------------------|-----------------------------------------------------------------------------|
| EEREAD           | 0000 0011          | Read data from EEPROM array beginning at selected address                   |
| EEWRITE          | 0000 0010          | Write data to EEPROM array beginning at selected address                    |
| EEWRDI           | 0000 0100          | Reset the write enable latch (disable write operations)                     |
| EEWREN           | 0000 0110          | Set the write enable latch (enable write operations)                        |
| SRREAD           | 0000 0101          | Read STATUS register                                                        |
| SRWRITE          | 0000 0001          | Write STATUS register                                                       |
| READ             | 0001 0011          | Read data from RTCC/SRAM array beginning at selected address                |
| WRITE            | 0001 0010          | Write data to RTCC/SRAM array beginning at selected address                 |
| UNLOCK           | 0001 0100          | Unlock the protected EEPROM block for a write operation                     |
| IDWRITE          | 0011 0010          | Write data to the protected EEPROM block beginning at selected address      |
| IDREAD           | 0011 0011          | Read data from the protected EEPROM block beginning at the selected address |
| CLRWDT           | 0100 0100          | Clear Watchdog Timer                                                        |
| CLRRAM           | 0101 0100          | Clear all SRAM data to '0'                                                  |

## 5.0 FUNCTIONAL DESCRIPTION

The MCP795WXX is a highly-integrated Real-Time Clock/Calendar (RTCC). Using an on-board, low-power oscillator, the current time is maintained in hundredths of seconds, seconds, minutes, hours, day of week, date, month, and year. The MCP795WXX also features 64 bytes of general purpose SRAM, either 2 Kbits (MCP795W2X) or 1 Kbit (MCP795W1X) of EEPROM, and 16 bytes of protected EEPROM. Two alarm modules allow interrupts to be generated at specific times with flexible comparison options. Digital trimming can be used to compensate for inaccuracies inherent with crystals. Using the backup supply input and an integrated power switch, the MCP795WXX will automatically switch to backup power when primary power is unavailable, allowing the current time and the SRAM contents to be maintained. The timestamp module captures the time when primary power is lost and when it is restored. The Watchdog Timer module can be used to reset an application that has become unresponsive. The high-speed event detect module can be used to detect pulse signals recovered from communication links, while the low-speed event detect module can be used to debounce switches and detect button presses.

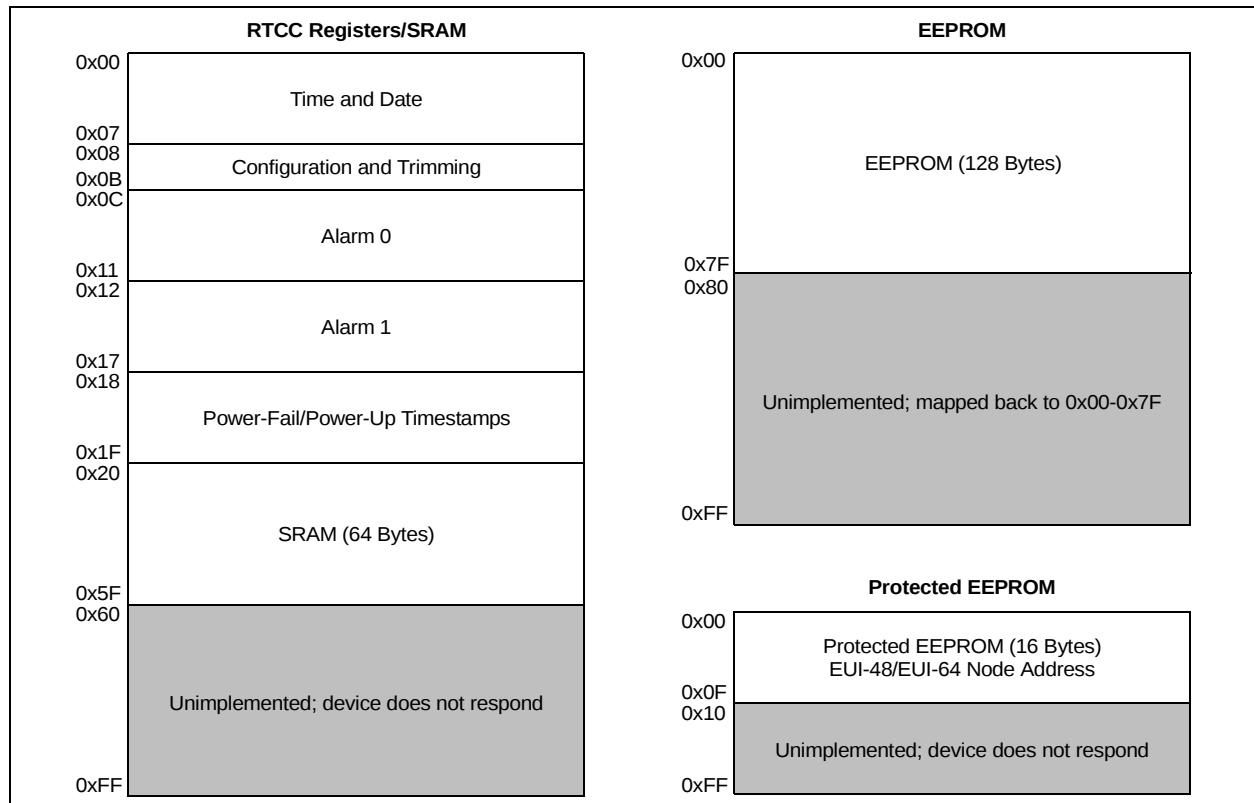
The RTCC configuration and STATUS registers are used to access all of the modules featured on the MCP795WXX.

## 5.1 Memory Organization

The MCP795WXX features four different blocks of memory: the RTCC registers, general purpose SRAM, 2 Kbit EEPROM (1 Kbit for the MCP795W1X) with software write-protect, and protected EEPROM. The RTCC registers and SRAM share the same address space and are accessed through the READ and WRITE instructions. The EEPROM region is accessed using the EEREAD and EEWRITE instructions, and the protected EEPROM is accessed using the IDREAD and IDWRITE instructions. Unused locations are not accessible. The MCP795WXX will not respond if the address is out of range, as shown in the shaded region of the memory maps in [Figure 5-1](#) and [Figure 5-2](#).

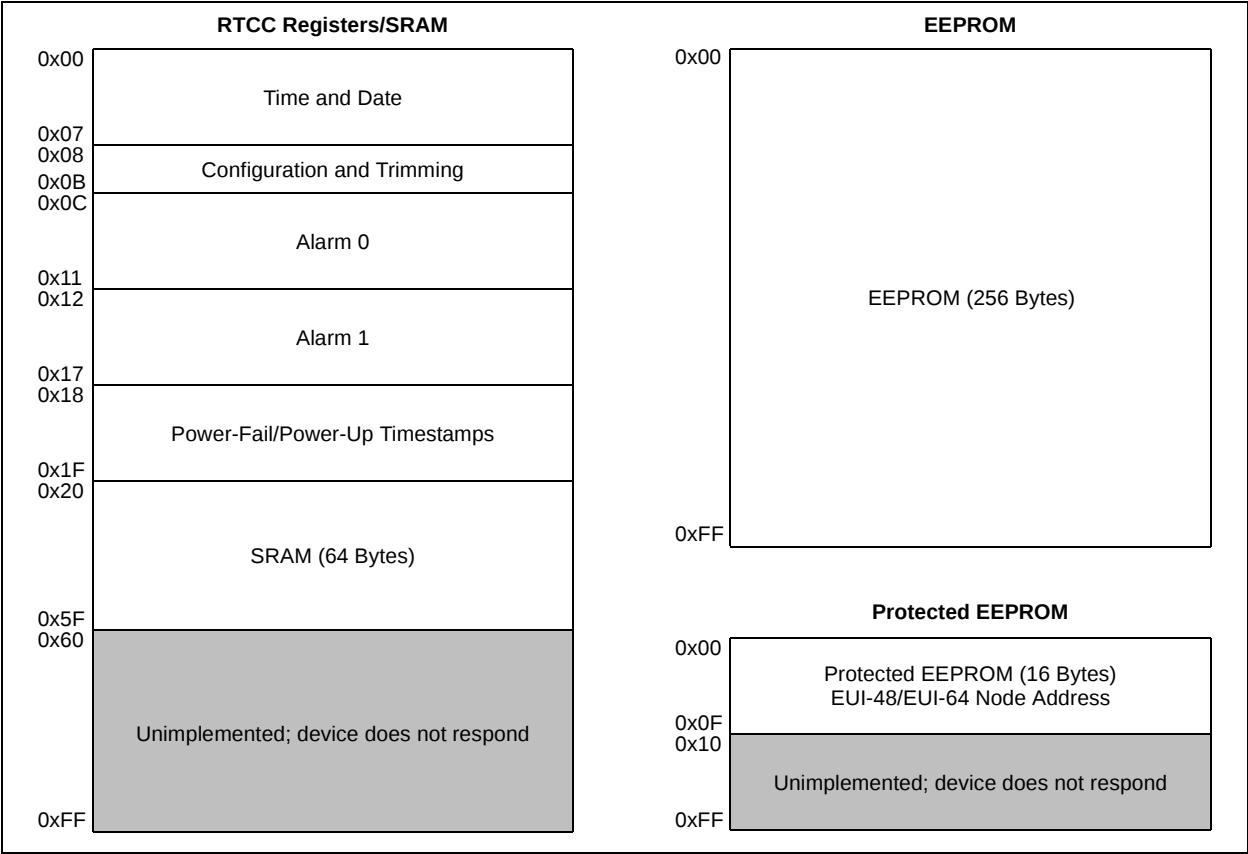
The RTCC registers are contained in addresses 0x00-0x1F. [Table 5-1](#) shows the detailed RTCC register map. There are 64 bytes of user-accessible SRAM, located in the address range 0x20-0x5F. The SRAM is a separate block from the RTCC registers. All RTCC registers and SRAM locations are maintained while operating from backup power.

**FIGURE 5-1: MEMORY MAP FOR MCP795W1X**



# MCP795W1X/MCP795W2X

**FIGURE 5-2: MEMORY MAP FOR MCP795W2X**



# MCP795W1X/MCP795W2X

**TABLE 5-1: DETAILED RTCC REGISTER MAP**

| Addr.                                        | Register Name | Bit 7    | Bit 6                | Bit 5           | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
|----------------------------------------------|---------------|----------|----------------------|-----------------|----------|----------|----------|----------|----------|
| <b>Section 5.3 “Timekeeping”</b>             |               |          |                      |                 |          |          |          |          |          |
| 00h                                          | RTCHSEC       | HSECTEN3 | HSECTEN2             | HSECTEN1        | HSECTEN0 | HSECONE3 | HSECONE2 | HSECONE1 | HSECONE0 |
| 01h                                          | RTCSEC        | ST       | SECTEN2              | SECTEN1         | SECTEN0  | SECONE3  | SECONE2  | SECONE1  | SECONE0  |
| 02h                                          | RTCMIN        | —        | MINTEN2              | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  |
| 03h                                          | RTCHOUR       | TRIMSIGN | 12/24                | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   |
| 04h                                          | RTCWKDAY      | —        | —                    | OSCRUN          | PWRFAIL  | VBATEN   | WKDAY2   | WKDAY1   | WKDAY0   |
| 05h                                          | RTCDATE       | —        | —                    | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| 06h                                          | RTCMTH        | —        | —                    | LPYR            | MHTTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  |
| 07h                                          | RTCYEAR       | YRTEN3   | YRTEN2               | YRTEN1          | YRTEN0   | YRONE3   | YRONE2   | YRONE1   | YRONE0   |
| 08h                                          | CONTROL       | OUT      | SQWEN                | ALM1EN          | ALM0EN   | EXTOSC   | CRSTRIM  | SQWFS1   | SQWFS0   |
| 09h                                          | OSCTRIM       | TRIMVAL7 | TRIMVAL6             | TRIMVAL5        | TRIMVAL4 | TRIMVAL3 | TRIMVAL2 | TRIMVAL1 | TRIMVAL0 |
| <b>Section 5.5 “Watchdog Timer”</b>          |               |          |                      |                 |          |          |          |          |          |
| 0Ah                                          | WDTCON        | WDTEN    | WDTIF                | WDTDLYEN        | WDTPWS   | WDTPS3   | WDTPS2   | WDTPS1   | WDTPS0   |
| <b>Section 5.6 “Event Detection”</b>         |               |          |                      |                 |          |          |          |          |          |
| 0Bh                                          | EVDTCN        | EVHIF    | EVLIF                | EVHEN           | EVLEN    | EVWDTEN  | EVLPS    | EVHCS1   | EVHCS0   |
| <b>Section 5.4 “Alarms”</b>                  |               |          |                      |                 |          |          |          |          |          |
| 0Ch                                          | ALM0SEC       | —        | SECTEN2              | SECTEN1         | SECTEN0  | SECONE3  | SECONE2  | SECONE1  | SECONE0  |
| 0Dh                                          | ALM0MIN       | —        | MINTEN2              | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  |
| 0Eh                                          | ALM0HOUR      | —        | 12/24 <sup>(2)</sup> | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   |
| 0Fh                                          | ALM0WKDAY     | ALM0PIN  | ALM0MSK2             | ALM0MSK1        | ALM0MSK0 | ALM0IF   | WKDAY2   | WKDAY1   | WKDAY0   |
| 10h                                          | ALM0DATE      | —        | —                    | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| 11h                                          | ALM0MTH       | —        | —                    | —               | MHTTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  |
| <b>Section 5.4 “Alarms”</b>                  |               |          |                      |                 |          |          |          |          |          |
| 12h                                          | ALM1HSEC      | HSECTEN3 | HSECTEN2             | HSECTEN1        | HSECTEN0 | HSECONE3 | HSECONE2 | HSECONE1 | HSECONE0 |
| 13h                                          | ALM1SEC       | —        | SECTEN2              | SECTEN1         | SECTEN0  | SECONE3  | SECONE2  | SECONE1  | SECONE0  |
| 14h                                          | ALM1MIN       | —        | MINTEN2              | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  |
| 15h                                          | ALM1HOUR      | —        | 12/24 <sup>(2)</sup> | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   |
| 16h                                          | ALM1WKDAY     | ALM1PIN  | ALM1MSK2             | ALM1MSK1        | ALM1MSK0 | ALM1IF   | WKDAY2   | WKDAY1   | WKDAY0   |
| 17h                                          | ALM1DATE      | —        | —                    | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| <b>Section 5.10.1 “Power-Fail Timestamp”</b> |               |          |                      |                 |          |          |          |          |          |
| <b>Power-Down Timestamp</b>                  |               |          |                      |                 |          |          |          |          |          |
| 18h                                          | PWRDNMIN      | —        | MINTEN2              | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  |
| 19h                                          | PWRDNHOUR     | —        | 12/24                | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   |
| 1Ah                                          | PWRDNDATE     | —        | —                    | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| 1Bh                                          | PWRDNMTH      | WKDAY2   | WKDAY1               | WKDAY0          | MHTTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  |
| <b>Power-Up Timestamp</b>                    |               |          |                      |                 |          |          |          |          |          |
| 1Ch                                          | PWRUPMIN      | —        | MINTEN2              | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  |
| 1Dh                                          | PWRUPHOUR     | —        | 12/24                | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   |
| 1Eh                                          | PWRUPDATE     | —        | —                    | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| 1Fh                                          | PWRUPMTH      | WKDAY2   | WKDAY1               | WKDAY0          | MHTTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  |

**Note 1:** Grey areas are unimplemented.

**2:** The 12/24 bits in the ALMxHOUR registers are read-only and reflect the value of the 12/24 bit in the RTCHOUR register.

## 5.2 Oscillator Configurations

The MCP795WXX can be operated in two different oscillator configurations: using an external crystal or using an external clock input.

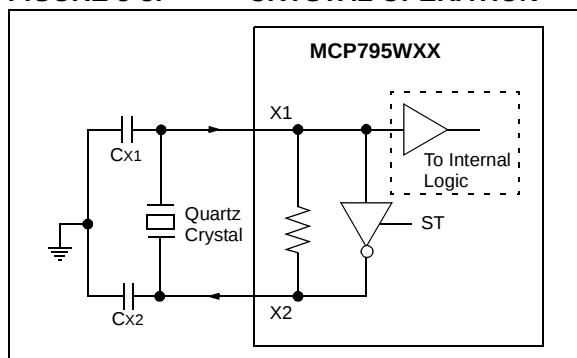
### 5.2.1 EXTERNAL CRYSTAL

The crystal oscillator circuit on the MCP795WXX is designed to operate with a standard 32.768 kHz tuning fork crystal and matching external load capacitors.

By using external load capacitors, the MCP795WXX allows for a wide selection of crystals. Suitable crystals have a load capacitance ( $C_L$ ) of 6-9 pF. Crystals with a load capacitance of 12.5 pF are not recommended.

Figure 5-3 shows the pin connections when using an external crystal.

**FIGURE 5-3: CRYSTAL OPERATION**



**Note 1:** The ST bit must be set to enable the crystal oscillator circuit.

**2:** Always verify oscillator performance over the voltage and temperature range that is expected for the application.

#### 5.2.1.1 Choosing Load Capacitors

$C_L$  is the effective load capacitance as seen by the crystal, and includes the physical load capacitors, pin capacitance, and stray board capacitance. Equation 5-1 can be used to calculate  $C_L$ .

$C_{X1}$  and  $C_{X2}$  are the external load capacitors. They must be chosen to match the selected crystal's specified load capacitance.

**Note:** If the load capacitance is not correctly matched to the chosen crystal's specified value, the crystal may give a frequency outside of the crystal manufacturer's specifications.

### EQUATION 5-1: LOAD CAPACITANCE CALCULATION

$$C_L = \frac{C_{X1} \times C_{X2}}{C_{X1} + C_{X2}} + C_{STRAY}$$

Where:

$C_L$  = Effective load capacitance

$C_{X1}$  = Capacitor value on X1 +  $C_{OSC}$

$C_{X2}$  = Capacitor value on X2 +  $C_{OSC}$

$C_{STRAY}$  = PCB stray capacitance

#### 5.2.1.2 Layout Considerations

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

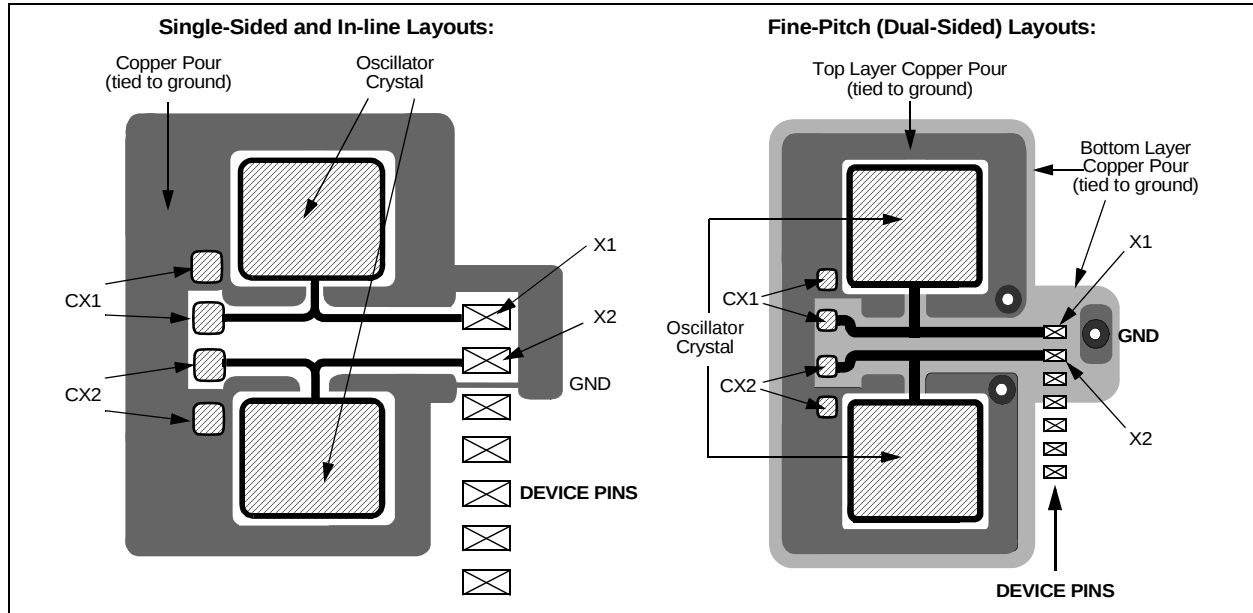
Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to VSS. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 5-4. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate website ([www.microchip.com](http://www.microchip.com)):

- AN1365, "Recommended Usage of Microchip Serial RTCC Devices"
- AN1519, "Recommended Crystals for Microchip Stand-Alone Real-Time Clock Calendar Devices"

**FIGURE 5-4: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT**

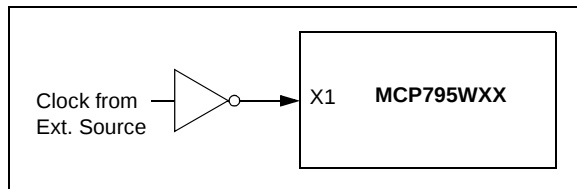


## 5.2.2 EXTERNAL CLOCK INPUT

A 32.768 kHz external clock source can be connected to the X1 pin (Figure 5-5). When using this configuration, the X2 pin should be left floating.

**Note:** The EXTOSC bit must be set to enable an external clock source.

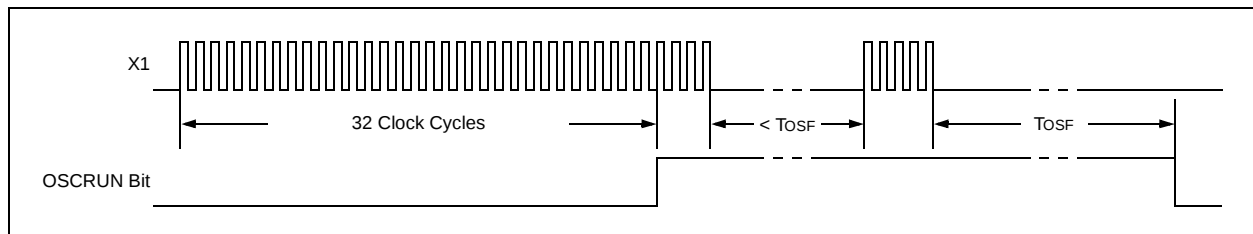
**FIGURE 5-5: EXTERNAL CLOCK INPUT OPERATION**



## 5.2.3 OSCILLATOR FAILURE STATUS

The MCP795WXX features an oscillator failure flag, OSCRUN, that indicates whether or not the oscillator is running. The OSCRUN bit is automatically set after 32 oscillator cycles are detected. If no oscillator cycles are detected for more than  $T_{OSF}$ , then the OSCRUN bit is automatically cleared (Figure 5-6). This can occur if the oscillator is stopped by clearing the ST bit or due to oscillator failure.

**FIGURE 5-6: OSCILLATOR FAILURE STATUS TIMING DIAGRAM**



**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH OSCILLATOR CONFIGURATION**

| Name     | Bit 7 | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   | Register on Page |
|----------|-------|---------|---------|---------|---------|---------|---------|---------|------------------|
| RTCSEC   | ST    | SECTEN2 | SECTEN1 | SECTEN0 | SECONE3 | SECONE2 | SECONE1 | SECONE0 | 18               |
| RTCWKDAY | —     | —       | OSCRUN  | PWRFAIL | VBATEN  | WKDAY2  | WKDAY1  | WKDAY0  | 20               |
| CONTROL  | OUT   | SQWEN   | ALM1EN  | ALM0EN  | EXTOSC  | CRSTRIM | SQWFS1  | SQWFS0  | 35               |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by oscillator configuration.

## 5.3 Timekeeping

The MCP795WXX maintains the current time and date using an external 32.768 kHz crystal or clock source. Separate registers are used for tracking hundredths of seconds, seconds, minutes, hours, day of week, date, month, and year. The MCP795WXX automatically adjusts for months with less than 31 days and compensates for leap years from 2001 to 2399. The year is stored as a two-digit value.

Both 12-hour and 24-hour time formats are supported and are selected using the 12/24 bit.

The day of week value counts from 1 to 7, increments at midnight, and the representation is user-defined (i.e., the MCP795WXX does not require 1 to equal Sunday, etc.).

All time and date values are stored in the registers as binary-coded decimal (BCD) values. The MCP795WXX will continue to maintain the time and date while operating off the backup supply.

When reading from the timekeeping registers, the registers are buffered to prevent errors due to rollover of counters. The following events cause the buffers to be updated:

- When a read is initiated from the RTCC registers (addresses 0x00 to 0x1F)
- During an RTCC register read operation, when the register address rolls over from 0x1F to 0x00

The timekeeping registers should be read in a single operation to utilize the on-board buffers and avoid rollover issues.

**Note 1:** Loading invalid values into the time and date registers will result in undefined operation.

- 2:** To avoid rollover issues when loading new time and date values, the oscillator/clock input should be disabled by clearing the ST bit for External Crystal mode and the EXTOSC bit for External Clock Input mode. After waiting for the OSCRUN bit to clear, the new values can be loaded and the ST or EXTOSC bit can then be re-enabled.

### 5.3.1 DIGIT CARRY RULES

The following list explains which timer values cause a digit carry when there is a rollover:

- Time of day: from 11:59:59.99 PM to 12:00:00.00 AM (12-hour mode) or 23:59:59.99 to 00:00:00.00 (24-hour mode), with a carry to the Date and Weekday fields
- Date: carries to the Month field according to [Table 5-3](#)
- Weekday: from 7 to 1 with no carry
- Month: from 12/31 to 01/01 with a carry to the Year field
- Year: from 99 to 00 with no carry

**TABLE 5-3: DAY TO MONTH ROLLOVER SCHEDULE**

| Month | Name      | Maximum Date            |
|-------|-----------|-------------------------|
| 01    | January   | 31                      |
| 02    | February  | 28 or 29 <sup>(1)</sup> |
| 03    | March     | 31                      |
| 04    | April     | 30                      |
| 05    | May       | 31                      |
| 06    | June      | 30                      |
| 07    | July      | 31                      |
| 08    | August    | 31                      |
| 09    | September | 30                      |
| 10    | October   | 31                      |
| 11    | November  | 30                      |
| 12    | December  | 31                      |

**Note 1:** 29 during leap years, otherwise 28.

### 5.3.2 GENERATING HUNDREDTH OF SECONDS

A special algorithm is required to accurately generate hundredth of seconds. The circuitry utilizes the 4.096 kHz clock signal and counts 41 clock pulses each for 24 increments of the hundredth of seconds count. The circuitry then counts 40 clock pulses for the next increment of the hundredth of second count. This results in every 25 hundredth of seconds increments equaling exactly 250 ms. Long term, the hundredth of seconds frequency will average the desired 100 Hz, while jitter is minimized short term.

**EQUATION 5-2: HUNDREDTH OF SECONDS GENERATION**

$$\frac{(41 \text{ clocks} \cdot 24 \text{ counts}) + (40 \text{ clocks} \cdot 1 \text{ count})}{4,096 \text{ Hz}} = 250 \text{ ms}$$

# MCP795W1X/MCP795W2X

## REGISTER 5-1: RTCHSEC: TIMEKEEPING HUNDREDTH OF SECONDS VALUE REGISTER (ADDRESS 0x00)

| R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| HSECTEN3 | HSECTEN2 | HSECTEN1 | HSECTEN0 | HSECONE3 | HSECONE2 | HSECONE1 | HSECONE0 |
| bit 7    |          |          |          |          |          |          | bit 0    |

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is clear      x = Bit is unknown

bit 7-4      **HSECTEN<3:0>**: Binary-Coded Decimal Value of Hundredth of Second's Tens Digit  
 Contains a value from 0 to 9

bit 3-0      **HSECONE<3:0>**: Binary-Coded Decimal Value of Hundredth of Second's Ones Digit  
 Contains a value from 0 to 9

## REGISTER 5-2: RTCSEC: TIMEKEEPING SECONDS VALUE REGISTER (ADDRESS 0x01)

| R/W-0 | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   |
|-------|---------|---------|---------|---------|---------|---------|---------|
| ST    | SECTEN2 | SECTEN1 | SECTEN0 | SECONE3 | SECONE2 | SECONE1 | SECONE0 |
| bit 7 |         |         |         |         |         |         | bit 0   |

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is clear      x = Bit is unknown

bit 7      **ST**: Start Oscillator bit  
 1 = Oscillator enabled  
 0 = Oscillator disabled

bit 6-4      **SECTEN<2:0>**: Binary-Coded Decimal Value of Second's Tens Digit  
 Contains a value from 0 to 5

bit 3-0      **SECONE<3:0>**: Binary-Coded Decimal Value of Second's Ones Digit  
 Contains a value from 0 to 9

## REGISTER 5-3: RTCMIN: TIMEKEEPING MINUTES VALUE REGISTER (ADDRESS 0x02)

| U-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   |
|-------|---------|---------|---------|---------|---------|---------|---------|
| —     | MINTEN2 | MINTEN1 | MINTEN0 | MINONE3 | MINONE2 | MINONE1 | MINONE0 |
| bit 7 |         |         |         |         |         |         | bit 0   |

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is clear      x = Bit is unknown

bit 7      **Unimplemented**: Read as '0'

bit 6-4      **MINTEN<2:0>**: Binary-Coded Decimal Value of Minute's Tens Digit  
 Contains a value from 0 to 5

bit 3-0      **MINONE<3:0>**: Binary-Coded Decimal Value of Minute's Ones Digit  
 Contains a value from 0 to 9

# MCP795W1X/MCP795W2X

## REGISTER 5-4: RTCHOUR: TIMEKEEPING HOURS VALUE REGISTER (ADDRESS 0x03)

| R/W-0    | R/W-0 | R/W-0           | R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-0  |
|----------|-------|-----------------|--------|--------|--------|--------|--------|
| TRIMSIGN | 12/24 | AM/PM<br>HRTEN1 | HRTEN0 | HRONE3 | HRONE2 | HRONE1 | HRONE0 |
| bit 7    |       |                 |        |        |        |        | bit 0  |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

### If 12/24 = 1 (12-hour format):

- bit 7 **TRIMSIGN:** Trim Sign bit  
1 = Add clocks to correct for slow time  
0 = Subtract clocks to correct for fast time
- bit 6 **12/24:** 12 or 24 Hour Time Format bit  
1 = 12-hour format  
0 = 24-hour format
- bit 5 **AM/PM:** AM/PM Indicator bit  
1 = PM  
0 = AM
- bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit  
Contains a value from 0 to 1
- bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit  
Contains a value from 0 to 9

### If 12/24 = 0 (24-hour format):

- bit 7 **TRIMSIGN:** Trim Sign bit  
1 = Add clocks to correct for slow time  
0 = Subtract clocks to correct for fast time
- bit 6 **12/24:** 12 or 24 Hour Time Format bit  
1 = 12-hour format  
0 = 24-hour format
- bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit  
Contains a value from 0 to 2.
- bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit  
Contains a value from 0 to 9

# MCP795W1X/MCP795W2X

## REGISTER 5-5: RTCWKDAY: TIMEKEEPING WEEKDAY VALUE REGISTER (ADDRESS 0x04)

| U-0   | U-0 | R-0    | R/W-0   | R/W-0  | R/W-0  | R/W-0  | R/W-1  |
|-------|-----|--------|---------|--------|--------|--------|--------|
| —     | —   | OSCRUN | PWRFAIL | VBATEN | WKDAY2 | WKDAY1 | WKDAY0 |
| bit 7 |     |        |         |        |        |        | bit 0  |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

bit 7-6                      **Unimplemented:** Read as '0'

bit 5                      **OSCRUN:** Oscillator Status bit  
                                  1 = Oscillator is enabled and running  
                                  0 = Oscillator has stopped or has been disabled

bit 4                      **PWRFAIL:** Power Failure Status bit<sup>(1,2)</sup>  
                                  1 = Primary power was lost and the power-fail timestamp registers have been loaded (must be cleared in software). Clearing this bit resets the power-fail timestamp registers to '0'.  
                                  0 = Primary power has not been lost

bit 3                      **VBATEN:** External Battery Backup Supply (VBAT) Enable bit  
                                  1 = VBAT input is enabled  
                                  0 = VBAT input is disabled

bit 2-0                      **WKDAY<2:0>:** Binary-Coded Decimal Value of Day of Week  
                                  Contains a value from 1 to 7. The representation is user-defined.

- Note 1:** The PWRFAIL bit must be cleared to log new timestamp data. This is to ensure previous timestamp data is not lost.
- 2:** The PWRFAIL bit can be cleared by writing a '0'. Once cleared, the PWRFAIL bit cannot be written to a '1' in software.

## REGISTER 5-6: RTCDATE: TIMEKEEPING DATE VALUE REGISTER (ADDRESS 0x05)

| U-0   | U-0 | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-1    |
|-------|-----|----------|----------|----------|----------|----------|----------|
| —     | —   | DATETEN1 | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| bit 7 |     |          |          |          |          |          | bit 0    |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

bit 7-6                      **Unimplemented:** Read as '0'

bit 5-4                      **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit  
                                  Contains a value from 0 to 3

bit 3-0                      **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit  
                                  Contains a value from 0 to 9

# MCP795W1X/MCP795W2X

**REGISTER 5-7: RTCMTH: TIMEKEEPING MONTH VALUE REGISTER (ADDRESS 0x06)**

| U-0   | U-0 | R-0  | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-1   |
|-------|-----|------|---------|---------|---------|---------|---------|
| —     | —   | LPYR | MHTTEN0 | MTHONE3 | MTHONE2 | MTHONE1 | MTHONE0 |
| bit 7 |     |      |         |         |         |         | bit 0   |

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

- bit 7-6                      **Unimplemented:** Read as '0'
- bit 5                      **LPYR:** Leap Year bit  
                                  1 = Year is a leap year  
                                  0 = Year is not a leap year
- bit 4                      **MHTTEN0:** Binary-Coded Decimal Value of Month's Tens Digit  
                                  Contains a value of 0 or 1
- bit 3-0                      **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit  
                                  Contains a value from 0 to 9

**REGISTER 5-8: RTCYEAR: TIMEKEEPING YEAR VALUE REGISTER (ADDRESS 0x07)**

| R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-1  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| YRTEN3 | YRTEN2 | YRTEN1 | YRTEN0 | YRONE3 | YRONE2 | YRONE1 | YRONE0 |
| bit 7  |        |        |        |        |        |        | bit 0  |

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

- bit 7-4                      **YRTEN<3:0>:** Binary-Coded Decimal Value of Year's Tens Digit  
                                  Contains a value from 0 to 9
- bit 3-0                      **YRONE<3:0>:** Binary-Coded Decimal Value of Year's Ones Digit  
                                  Contains a value from 0 to 9

**TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMEKEEPING**

| Name     | Bit 7    | Bit 6    | Bit 5           | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Register on Page |
|----------|----------|----------|-----------------|----------|----------|----------|----------|----------|------------------|
| RTCHSEC  | HSECTEN3 | HSECTEN2 | HSECTEN1        | HSECTEN0 | HSECONE3 | HSECONE2 | HSECONE1 | HSECONE0 | 18               |
| RTCSEC   | ST       | SECTEN2  | SECTEN1         | SECTEN0  | SECONE3  | SECONE2  | SECONE1  | SECONE0  | 18               |
| RTCMIN   | —        | MINTEN2  | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  | 18               |
| RTCHOUR  | TRIMSIGN | 12/24    | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   | 19               |
| RTCWKDAY | —        | —        | OSCRUN          | PWRFAIL  | VBATEN   | WKDAY2   | WKDAY1   | WKDAY0   | 20               |
| RTCDATE  | —        | —        | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 | 20               |
| RCMTH    | —        | —        | LPYR            | MHTTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  | 21               |
| RCYEAR   | YRTEN3   | YRTEN2   | YRTEN1          | YRTEN0   | YRONE3   | YRONE2   | YRONE1   | YRONE0   | 21               |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used in timekeeping.

## 5.4 Alarms

The MCP795WXX features two independent alarms. Each alarm can be used to either generate an interrupt at a specific time in the future, or to generate a periodic interrupt every second (Alarm 1 only), minute, hour, day, day of week, or month.

There is a separate interrupt flag, ALMxIF, for each alarm. The interrupt flags are set by hardware when the chosen alarm mask condition matches (Table 5-5 and Table 5-6). The interrupt flags must be cleared in software.

Each alarm can independently be assigned to either the  $\overline{\text{IRQ}}$  pin or the  $\overline{\text{WDO}}$  pin by configuring the ALMxPIN bits. Refer to Section 5.8 “Interrupt Outputs” for details. The alarm interrupt output is available while operating from the backup power supply, regardless of the output pin assignments.

All time and date values are stored in the registers as binary-coded decimal (BCD) values.

**Note:** Throughout this section, references to the register and bit names for the alarm modules are referred to generically by the use of ‘x’ in place of the specific module number. Thus, “ALMxSEC” might refer to the seconds register for Alarm 0 or Alarm 1.

TABLE 5-6: ALARM 1 MASKS

| ALM1MSK<2:0> | Alarm 1 Asserts on Match of                    |
|--------------|------------------------------------------------|
| 000          | Seconds                                        |
| 001          | Minutes                                        |
| 010          | Hours                                          |
| 011          | Day of Week                                    |
| 100          | Date                                           |
| 101          | Hundredth of Seconds                           |
| 110          | Reserved                                       |
| 111          | Seconds, Minutes, Hours, Day of Week, and Date |

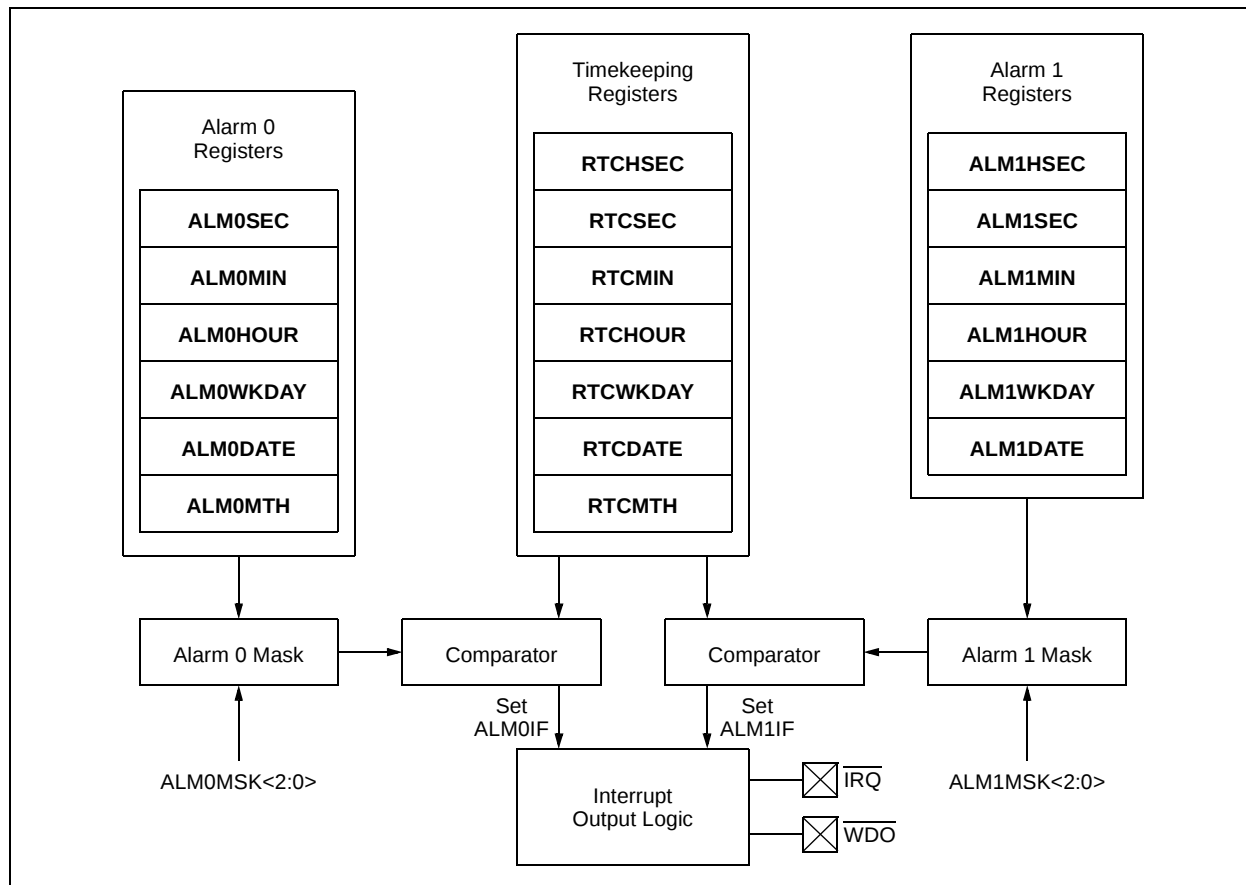
**Note 1:** The alarm interrupt flags must be cleared by the user.

**2:** Loading invalid values into the alarm registers will result in undefined operation.

TABLE 5-5: ALARM 0 MASKS

| ALM0MSK<2:0> | Alarm 0 Asserts on Match of                           |
|--------------|-------------------------------------------------------|
| 000          | Seconds                                               |
| 001          | Minutes                                               |
| 010          | Hours                                                 |
| 011          | Day of Week                                           |
| 100          | Date                                                  |
| 101          | Reserved                                              |
| 110          | Reserved                                              |
| 111          | Seconds, Minutes, Hours, Day of Week, Date, and Month |

**FIGURE 5-7: ALARM BLOCK DIAGRAM**



## 5.4.1 CONFIGURING THE ALARM

In order to configure the alarm modules, the following steps need to be performed:

1. Load the timekeeping registers and enable the oscillator.
2. Configure the ALMxMSK<2:0> bits to select the desired alarm mask.
3. Set or clear the ALMxPIN bit according to the desired output pin assignment.
4. Ensure the ALMxIF flag is cleared.
5. Based on the selected alarm mask, load the alarm match value into the appropriate register(s).
6. Enable the alarm module by setting the ALMxEN bit.

# MCP795W1X/MCP795W2X

## REGISTER 5-9: ALM1HSEC: ALARM 1 HUNDREDTHS OF SECONDS VALUE REGISTER (ADDRESS 0x12)

| R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| HSECTEN3 | HSECTEN2 | HSECTEN1 | HSECTEN0 | HSECONE3 | HSECONE2 | HSECONE1 | HSECONE0 |
| bit 7    |          |          |          |          |          |          | bit 0    |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

bit 7-4 **HSECTEN<3:0>**: Binary-Coded Decimal Value of Hundredth of Second's Tens Digit  
Contains a value from 0 to 9

bit 3-0 **HSECONE<3:0>**: Binary-Coded Decimal Value of Hundredth of Second's Ones Digit  
Contains a value from 0 to 9

**Note 1:** Hundredth of seconds matching is only available on Alarm 1.

## REGISTER 5-10: ALMxSEC: ALARM 0/1 SECONDS VALUE REGISTER (ADDRESSES 0x0C/0x13)

| U-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   |
|-------|---------|---------|---------|---------|---------|---------|---------|
| —     | SECTEN2 | SECTEN1 | SECTEN0 | SECONE3 | SECONE2 | SECONE1 | SECONE0 |
| bit 7 |         |         |         |         |         |         | bit 0   |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>**: Binary-Coded Decimal Value of Second's Tens Digit  
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>**: Binary-Coded Decimal Value of Second's Ones Digit  
Contains a value from 0 to 9

# MCP795W1X/MCP795W2X

## REGISTER 5-11: ALMxMIN: ALARM 0/1 MINUTES VALUE REGISTER (ADDRESSES 0x0D/0x14)

| U-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   |
|-------|---------|---------|---------|---------|---------|---------|---------|
| —     | MINTEN2 | MINTEN1 | MINTEN0 | MINONE3 | MINONE2 | MINONE1 | MINONE0 |
| bit 7 |         |         |         |         |         |         | bit 0   |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute's Tens Digit  
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute's Ones Digit  
Contains a value from 0 to 9

## REGISTER 5-12: ALMxHOUR: ALARM 0/1 HOURS VALUE REGISTER (ADDRESSES 0x0E/0x15)

| U-0   | R-0   | R/W-0           | R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-0  |
|-------|-------|-----------------|--------|--------|--------|--------|--------|
| —     | 12/24 | AM/PM<br>HRTEN1 | HRTEN0 | HRONE3 | HRONE2 | HRONE1 | HRONE0 |
| bit 7 |       |                 |        |        |        |        | bit 0  |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

### If 12/24 = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/24:** 12 or 24 Hour Time Format bit<sup>(1)</sup>  
1 = 12-hour format  
0 = 24-hour format

bit 5 **AM/PM:** AM/PM Indicator bit  
1 = PM  
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit  
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit  
Contains a value from 0 to 9

### If 12/24 = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/24:** 12 or 24 Hour Time Format bit<sup>(1)</sup>  
1 = 12-hour format  
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit  
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit  
Contains a value from 0 to 9

**Note 1:** This bit is read-only and reflects the value of the 12/24 bit in the RTCHOUR register.

# MCP795W1X/MCP795W2X

**REGISTER 5-13: ALMxWKDAY: ALARM 0/1 WEEKDAY VALUE REGISTER (ADDRESSES 0x0F/0x16)**

| R/W-0   | R/W-0    | R/W-0    | R/W-0    | R/W-0  | R/W-0  | R/W-0  | R/W-1  |
|---------|----------|----------|----------|--------|--------|--------|--------|
| ALMxPIN | ALMxMSK2 | ALMxMSK1 | ALMxMSK0 | ALMxIF | WKDAY2 | WKDAY1 | WKDAY0 |
| bit 7   |          |          |          |        |        |        | bit 0  |

**Legend:**

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is clear  
x = Bit is unknown

- bit 7 **ALMxPIN:** Alarm Interrupt Output Pin Assignment bit  
1 = Alarm output is assigned to WDO  
0 = Alarm output is assigned to IRQ
- bit 6-4 **ALMxMSK<2:0>:** Alarm Mask bits  
000 = Seconds match  
001 = Minutes match  
010 = Hours match (logic takes into account 12-/24-hour operation)  
011 = Day of week match  
100 = Date match  
101 = Hundredth of Seconds<sup>(1)</sup>  
110 = Reserved; do not use  
111 = Seconds, Minutes, Hour, Day of Week, Date and Month<sup>(2)</sup>
- bit 3 **ALMxIF:** Alarm Interrupt Flag bit<sup>(3)</sup>  
1 = Alarm match occurred (must be cleared in software)  
0 = Alarm match did not occur
- bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits  
Contains a value from 1 to 7. The representation is user-defined.

- Note 1:** Hundredth of seconds matching is available on Alarm 1 only. This setting is reserved on Alarm 0.  
**2:** Month matching is available on Alarm 0 only.  
**3:** The ALMxIF bit can be cleared by writing a '0'. Once cleared, the ALMxIF bit cannot be written to a '1' in software.

**REGISTER 5-14: ALMxDATE: ALARM 0/1 DATE VALUE REGISTER (ADDRESSES 0x10/0x17)**

| U-0   | U-0 | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-1    |
|-------|-----|----------|----------|----------|----------|----------|----------|
| —     | —   | DATETEN1 | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| bit 7 |     |          |          |          |          |          | bit 0    |

**Legend:**

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is clear  
x = Bit is unknown

- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit  
Contains a value from 0 to 3
- bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit  
Contains a value from 0 to 9

# MCP795W1X/MCP795W2X

**REGISTER 5-15: ALM0MTH: ALARM 0 MONTH VALUE REGISTER (ADDRESS 0x11)**

|       |     |     |         |         |         |         |         |
|-------|-----|-----|---------|---------|---------|---------|---------|
| U-0   | U-0 | U-0 | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-1   |
| —     | —   | —   | MTHTEN0 | MTHONE3 | MTHONE2 | MTHONE1 | MTHONE0 |
| bit 7 |     |     |         |         |         |         | bit 0   |

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

bit 7-5                      **Unimplemented:** Read as '0'  
 bit 4                      **MTHTEN0:** Binary-Coded Decimal Value of Month's Tens Digit  
                               Contains a value of 0 or 1  
 bit 3-0                      **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit  
                               Contains a value from 0 to 9

**Note 1:** Month matching is only available on Alarm 0.

**TABLE 5-7: SUMMARY OF REGISTERS ASSOCIATED WITH ALARMS**

| Name      | Bit 7    | Bit 6    | Bit 5           | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Register on Page   |
|-----------|----------|----------|-----------------|----------|----------|----------|----------|----------|--------------------|
| ALM0SEC   | —        | SECTEN2  | SECTEN1         | SECTEN0  | SECONE3  | SECONE2  | SECONE1  | SECONE0  | <a href="#">24</a> |
| ALM0MIN   | —        | MINTEN2  | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  | <a href="#">25</a> |
| ALM0HOUR  | —        | 12/24    | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   | <a href="#">25</a> |
| ALM0WKDAY | ALM0PIN  | ALM0MSK2 | ALM0MSK1        | ALM0MSK0 | ALM0IF   | WKDAY2   | WKDAY1   | WKDAY0   | <a href="#">26</a> |
| ALM0DATE  | —        | —        | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 | <a href="#">26</a> |
| ALM0MTH   | —        | —        | —               | MTHTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  | <a href="#">27</a> |
| ALM1HSEC  | HSECTEN3 | HSECTEN2 | HSECTEN1        | HSECTEN0 | HSECONE3 | HSECONE2 | HSECONE1 | HSECONE0 | <a href="#">24</a> |
| ALM1SEC   | —        | SECTEN2  | SECTEN1         | SECTEN0  | SECONE3  | SECONE2  | SECONE1  | SECONE0  | <a href="#">24</a> |
| ALM1MIN   | —        | MINTEN2  | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  | <a href="#">25</a> |
| ALM1HOUR  | —        | 12/24    | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   | <a href="#">25</a> |
| ALM1WKDAY | ALM1PIN  | ALM1MSK2 | ALM1MSK1        | ALM1MSK0 | ALM1IF   | WKDAY2   | WKDAY1   | WKDAY0   | <a href="#">26</a> |
| ALM1DATE  | —        | —        | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 | <a href="#">26</a> |
| CONTROL   | OUT      | SQWEN    | ALM1EN          | ALM0EN   | EXTOSC   | CRSTRIM  | SQWFS1   | SQWFS0   | <a href="#">35</a> |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by alarms.

## 5.5 Watchdog Timer

The MCP795WXX features a Watchdog Timer (WDT) module that can be used to enhance the robustness of an application. The WDT continuously counts up toward a specified time-out period. During normal operation, the application would clear the WDT before it times out. However, if a failure occurs, the application would not clear the WDT, causing it to time out, set the WDTIF interrupt flag, and assert the  $\overline{\text{WDO}}$  pin low for a specified pulse width. This can then be used to reset the application and recover from the failure.

The WDT time-out period can be configured by setting the WDTPS<3:0> bits according to Table 5-8. Setting the WDTDLLEN bit will enable a 64-second nominal start-up delay. With this enabled, every time the WDT is restarted or cleared, the WDT will wait for 64 seconds before starting the time-out period.

Once the WDTIF flag has been set due to a WDT time-out, the WDTIF flag must be cleared to restart the WDT.

The WDT is driven by the oscillator. If the oscillator is not running, then the WDT time-out will not occur.

**Note 1:** The WDT time-out period should only be changed while the WDT module is disabled.

**TABLE 5-8: WATCHDOG TIMER TIME-OUT PERIOD SELECTION**

| WDTPS<3:0> | Time-out Period (Fosc Cycles) | Nominal Time-out Period <sup>(1)</sup> |
|------------|-------------------------------|----------------------------------------|
| 0000       | 32 cycles                     | 977 $\mu\text{s}$                      |
| 0001       | 512 cycles                    | 15.6 ms                                |
| 0010       | 2,048 cycles                  | 62.5 ms                                |
| 0011       | 4,096 cycles                  | 125 ms                                 |
| 0100       | 32,768 cycles                 | 1 second                               |
| 0101       | 524,288 cycles                | 16 seconds                             |
| 0110       | 1,048,576 cycles              | 32 seconds                             |
| 0111       | 2,097,152 cycles              | 64 seconds                             |
| 1xxx       | Reserved                      |                                        |

**Note 1:** Nominal period assumes Fosc is 32.768 kHz.

### 5.5.1 WATCHDOG TIMER INTERRUPT OUTPUT

When the WDT times out, the WDTIF interrupt flag gets set and the  $\overline{\text{WDO}}$  pin is asserted low for a short pulse. The width of the pulse is determined by the WDTWPS bit according to Table 5-9.

The WDT interrupt output will operate regardless of whether or not either alarm module interrupt output is assigned to the  $\overline{\text{WDO}}$  pin. See Section 5.8.2 “WDO Interrupt Output” for additional details.

**TABLE 5-9: WATCHDOG TIMER OUTPUT PULSE WIDTH SELECTION**

| WDTWPS | Pulse Width (Fosc Cycles) | Nominal Pulse Width <sup>(1)</sup> |
|--------|---------------------------|------------------------------------|
| 0      | 4 cycles                  | 122 $\mu\text{s}$                  |
| 1      | 4,096 cycles              | 125 ms                             |

**Note 1:** Nominal period assumes Fosc is 32.768 kHz.

### 5.5.2 CONFIGURING THE WATCHDOG TIMER

In order to configure the WDT module, the following steps need to be performed:

1. Enable the oscillator.
2. Configure the WDTPS<3:0> bits to select the desired time-out period.
3. If desired, set the WDTDLLEN bit to enable the 64-second start-up delay.
4. Configure the WDTWPS bit to select the desired output pulse width.
5. Ensure the WDTIF flag is cleared.
6. Enable the WDT module by setting the WDTEN bit.

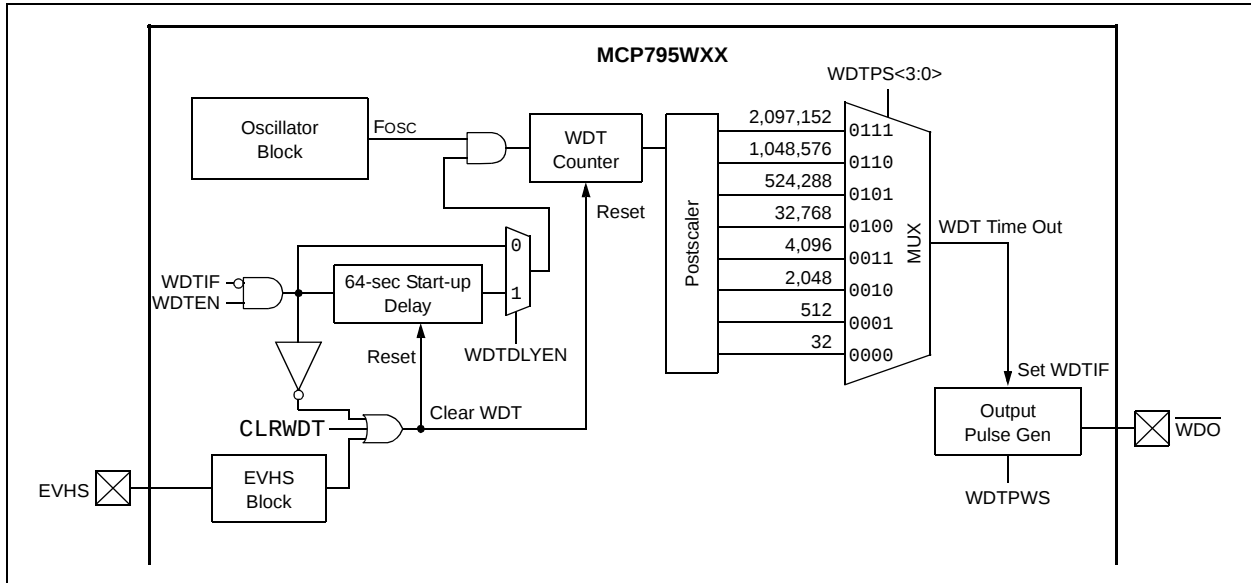
### 5.5.3 CLEARING THE WATCHDOG TIMER

The WDT must be cleared before the time-out period occurs in order to prevent it from timing out. The WDT can be cleared using any of the following methods:

1. Executing a CLRWDT instruction.
2. Toggling the EVHS pin with the EVWDTEN bit set.
3. Disabling/re-enabling the WDT module.
4. Clearing the WDTIF flag after it has been set.

# MCP795W1X/MCP795W2X

FIGURE 5-8: WATCHDOG TIMER BLOCK DIAGRAM



# MCP795W1X/MCP795W2X

**REGISTER 5-16: WDTCON: WATCHDOG TIMER CONTROL REGISTER (ADDRESS 0x0A)**

| R/W-0 | R/W-0 | R/W-0    | R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-0  |
|-------|-------|----------|--------|--------|--------|--------|--------|
| WDTEN | WDTIF | WDTDLLEN | WDTPWS | WDTPS3 | WDTPS2 | WDTPS1 | WDTPS0 |
| bit 7 |       |          |        |        |        |        | bit 0  |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

- bit 7      **WDTEN:** Watchdog Timer Enable bit<sup>(1)</sup>  
             1 = Watchdog Timer enabled  
             0 = Watchdog Timer disabled
- bit 6      **WDTIF:** Watchdog Timer Interrupt Flag bit  
             1 = Watchdog Timer has timed out (must be cleared in software)  
             0 = Watchdog Timer has not timed out
- bit 5      **WDTDLLEN:** Watchdog Timer Delay Enable bit  
             1 = Enable 2,097,152 oscillator cycle (64-second nominal) start-up delay before time-out period begins after WDT is reset  
             0 = Disable start-up delay
- bit 4      **WDTPWS:** Watchdog Timer Output Pulse Width Select bit  
             1 = 4,096 oscillator cycles (125 ms nominal)  
             0 = 4 oscillator cycles (122 µs nominal)
- bit 3-0    **WDTPS<3:0>:** Watchdog Timer Time-out Period Select bits  
             0000 = 32 oscillator cycles (977 µs nominal)  
             0001 = 512 oscillator cycles (15.6 ms nominal)  
             0010 = 2,048 oscillator cycles (62.5 ms nominal)  
             0011 = 4,096 oscillator cycles (125 ms nominal)  
             0100 = 32,768 oscillator cycles (1 second nominal)  
             0101 = 524,288 oscillator cycles (16 second nominal)  
             0110 = 1,048,576 oscillator cycles (32 second nominal)  
             0111 = 2,097,152 oscillator cycles (64 second nominal)  
             1xxx = Reserved; do not use

**Note 1:** The WDTEN bit is automatically cleared when operating from the backup power supply.

**TABLE 5-10: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER**

| Name   | Bit 7 | Bit 6 | Bit 5    | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Register on Page |
|--------|-------|-------|----------|--------|--------|--------|--------|--------|------------------|
| WDTCON | WDTEN | WDTIF | WDTDLLEN | WDTPWS | WDTPS3 | WDTPS2 | WDTPS1 | WDTPS0 | 30               |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used in Watchdog Timer configuration.

## 5.6 Event Detection

The MCP795WXX features two separate event detection modules: a high-speed event detect and a low-speed event detect. The high-speed event detect can be used to detect signal preambles, while the low-speed event detect is meant for debouncing mechanical switches.

The event detection modules are not available while operating from the backup power supply.

### 5.6.1 HIGH-SPEED EVENT DETECT

The high-speed event detect module is designed to detect a series of digital transitions (both low-to-high and high-to-low) on the EVHS input, and then generate an interrupt. The number of transitions required to occur is determined by the EVHCS<1:0> bits as shown in [Table 5-11](#). Once the specified number of transitions have occurred, the EVHIF interrupt flag is set and the IRQ pin is asserted low.

The high-speed event detect has a time-out period of 8,192 oscillator cycles (250 ms nominal assuming a 32.768 kHz clock frequency).

If the total number of transitions specified by the EVHCS<1:0> bits do not occur within the time-out period, then the transition count will be reset and counting will start over ([Figure 5-10](#)). The time-out period is driven by the oscillator. If the oscillator is not running, then the time-out will not occur.

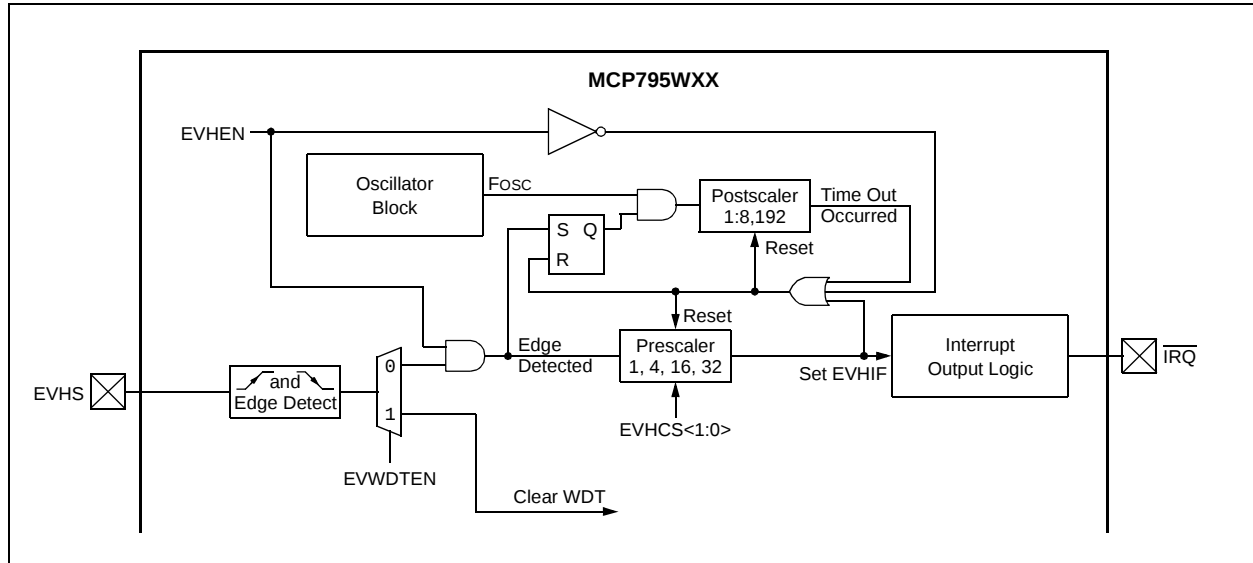
**TABLE 5-11: HIGH-SPEED EVENT COUNT SELECTION**

| EVHCS<1:0> | Required Transitions for Interrupt |
|------------|------------------------------------|
| 00         | 1                                  |
| 01         | 4                                  |
| 10         | 16                                 |
| 11         | 32                                 |

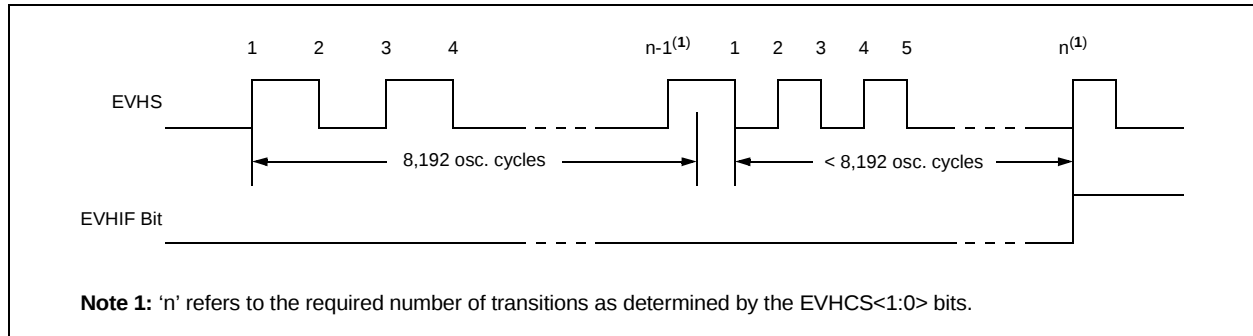
#### 5.6.1.1 Clearing the WDT Using EVHS

The EVHS input can also be used to clear the Watchdog Timer on both low-to-high and high-to-low transitions by setting the EVWDTEN bit. Note that when this bit is set, the high-speed event detect module is disabled and the EVHEN bit is ignored.

**FIGURE 5-9: HIGH-SPEED EVENT DETECT BLOCK DIAGRAM**



**FIGURE 5-10: HIGH-SPEED EVENT DETECT WAVEFORM EXAMPLE**



## 5.6.1.2 Configuring High-Speed Event Detect

In order to configure the high-speed event detect module, the following steps need to be performed:

1. Enable the oscillator.
2. Configure the EVHCS<1:0> bits to select the desired number of transitions.
3. Ensure the EVWDTEN bit is cleared.
4. Ensure the EVHIF flag is cleared.
5. Enable the high-speed event detect module by setting the EVHEN bit.

## 5.6.2 LOW-SPEED EVENT DETECT

The low-speed event detect module is designed to interface directly with mechanical switches to provide a debounced signal. The debounce period is selectable through the EVLPS bit as shown in [Table 5-12](#). Low speed events occur when the EVLS input toggles and remains stable for the selected debounce period.

After a transition on the EVLS input, the MCP795WXX will begin counting the debounce period. Either a high-to-low or a low-to-high transition will initiate counting. Once the debounce period has expired, the EVLIF flag is set and the  $\overline{\text{IRQ}}$  pin is asserted low ([Figure 5-12](#)). If the EVLS input returns to its original level before the debounce period expires, then counting is aborted and the EVLIF flag will not be set.

The low-speed event detect module is driven by the oscillator. If the oscillator is not running, then the debounce period will not expire and the EVLIF flag will not be set.

**TABLE 5-12: LOW-SPEED EVENT DEBOUNCE PERIOD SELECTION**

| EVLPS | Debounce Period (Fosc Cycles) | Nominal Debounce Period <sup>(1)</sup> |
|-------|-------------------------------|----------------------------------------|
| 0     | 1,024 cycles                  | 31.25 ms                               |
| 1     | 16,384 cycles                 | 500 ms                                 |

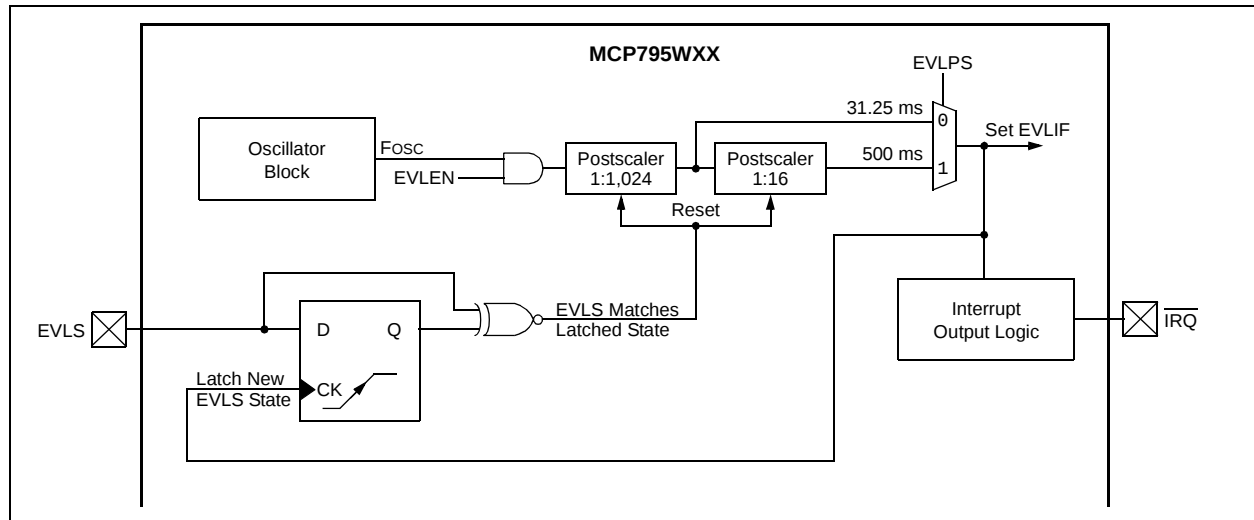
**Note 1:** Nominal period assumes Fosc is 32.768 kHz.

## 5.6.2.1 Configuring Low-Speed Event Detect

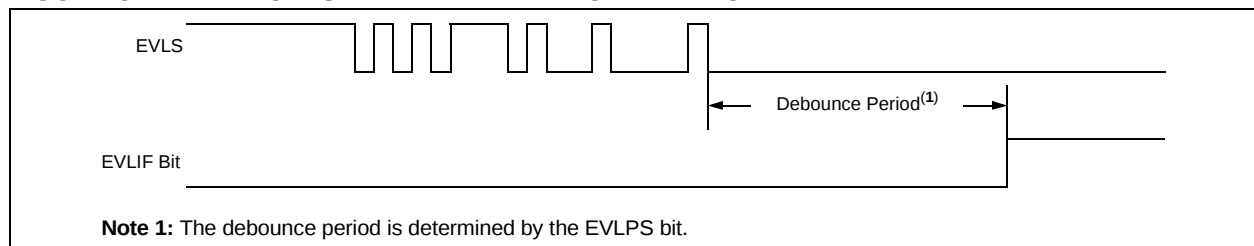
In order to configure the low-speed event detect module, the following steps need to be performed:

1. Enable the oscillator.
2. Configure the EVLPS bit to select the desired debounce period.
3. Ensure the EVLIF flag is cleared.
4. Enable the low-speed event detect module by setting the EVLEN bit.

**FIGURE 5-11: LOW-SPEED EVENT DETECT BLOCK DIAGRAM**



**FIGURE 5-12: LOW-SPEED EVENT DETECT WAVEFORM EXAMPLE**



# MCP795W1X/MCP795W2X

**REGISTER 5-17: EVDTCON: EVENT DETECT CONTROL REGISTER (ADDRESS 0x0B)**

|       |       |       |       |         |       |        |        |
|-------|-------|-------|-------|---------|-------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0   | R/W-0 | R/W-0  | R/W-0  |
| EVHIF | EVLIF | EVHEN | EVLEN | EVWDTEN | EVLPS | EVHCS1 | EVHCS0 |
| bit 7 |       |       |       |         |       |        | bit 0  |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

|         |                                                                                                                                                                                                                                                                      |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 7   | <b>EVHIF:</b> High-Speed Event Detect Interrupt Flag bit<br>1 = High-speed event detection occurred (must be cleared in software)<br>0 = High-speed event detection did not occur                                                                                    |
| bit 6   | <b>EVLIF:</b> Low-Speed Event Detect Interrupt Flag bit<br>1 = Low-speed event detection occurred (must be cleared in software)<br>0 = Low-speed event detection did not occur                                                                                       |
| bit 5   | <b>EVHEN:</b> High-Speed Event Detect Module Enable bit<br><u>If EVWDTEN = 0:</u><br>1 = High-Speed Event Detect enabled<br>0 = High-Speed Event Detect disabled<br><u>If EVWDTEN = 1:</u><br>Unused.                                                                |
| bit 4   | <b>EVLEN:</b> Low-Speed Event Detect Module Enable bit<br>1 = Low-Speed Event Detect enabled<br>0 = Low-Speed Event Detect disabled                                                                                                                                  |
| bit 3   | <b>EVWDTEN:</b> EVHS Input WDT Clear Enable bit<br>1 = Enable Watchdog Timer clear on EVHS input transition. Disables high-speed event detect module.<br>0 = Disable EVHS input clearing Watchdog Timer.                                                             |
| bit 2   | <b>EVLPS:</b> Low-Speed Event Detect Debounce Period Select bit<br>1 = 16,384 oscillator cycles (500 ms nominal)<br>0 = 1,024 oscillator cycles (31.25 ms nominal)                                                                                                   |
| bit 1-0 | <b>EVHCS&lt;1:0&gt;:</b> High-Speed Event Detect Transition Count Select bits<br>Selects how many transitions must occur on the EVHS input before an interrupt is triggered<br>00 = 1 transition<br>01 = 4 transitions<br>10 = 16 transitions<br>11 = 32 transitions |

**TABLE 5-13: SUMMARY OF REGISTERS ASSOCIATED WITH EVENT DETECTION**

| Name    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3   | Bit 2 | Bit 1  | Bit 0  | Register on Page |
|---------|-------|-------|-------|-------|---------|-------|--------|--------|------------------|
| EVDTCON | EVHIF | EVLIF | EVHEN | EVLEN | EVWDTEN | EVLPS | EVHCS1 | EVHCS0 | 33               |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used in event detect configuration.

## 5.7 Clock Output

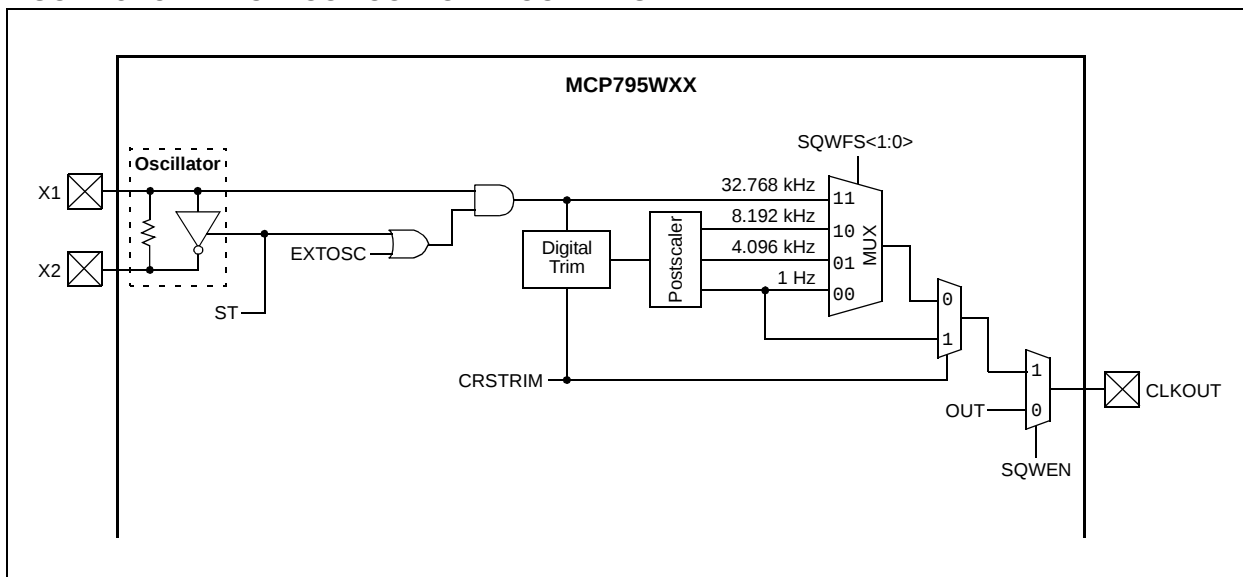
The MCP795WXX features Square Wave Clock Output and General Purpose Output modes through the CLKOUT pin. If the SQWEN bit is set, then CLKOUT operates in Square Wave Clock Output mode. Otherwise, CLKOUT operates in General Purpose Output mode (Table 5-14).

The CLKOUT pin is disabled while operating from the backup power supply.

TABLE 5-14: CLKOUT OUTPUT MODES

| SQWEN | OUT | Mode                     |
|-------|-----|--------------------------|
| 0     | 0   | Logic Low Output         |
| 0     | 1   | Logic High Output        |
| 1     | x   | Square Wave Clock Output |

FIGURE 5-13: CLKOUT OUTPUT BLOCK DIAGRAM



### 5.7.1 SQUARE WAVE OUTPUT MODE

The MCP795WXX can be configured to generate a square wave clock signal on CLKOUT. The input clock frequency, Fosc, is divided according to the SQWFS<1:0> bits as shown in Table 5-15.

The square wave output is not available when operating from the backup power supply.

**Note:** All of the clock output rates are affected by digital trimming except for the 1:1 postscaler value (SQWFS<1:0> = 11).

### 5.7.2 GENERAL PURPOSE OUTPUT MODE

If the square wave clock output is disabled, CLKOUT acts as a general purpose output. The output logic level is controlled by the OUT bit.

The general purpose output is not available when operating from the backup power supply.

TABLE 5-15: CLOCK OUTPUT RATES

| SQWFS<1:0> | Postscaler | Nominal Frequency |
|------------|------------|-------------------|
| 00         | 1:32,768   | 1 Hz              |
| 01         | 1:8        | 4.096 kHz         |
| 10         | 1:4        | 8.192 kHz         |
| 11         | 1:1        | 32.768 kHz        |

**Note 1:** Nominal frequency assumes Fosc is 32.768 kHz.

# MCP795W1X/MCP795W2X

**REGISTER 5-18: CONTROL: RTCC CONTROL REGISTER (ADDRESS 0x08)**

| R/W-1 | R/W-0 | R/W-0  | R/W-0  | R/W-0  | R/W-0   | R/W-0  | R/W-0  |
|-------|-------|--------|--------|--------|---------|--------|--------|
| OUT   | SQWEN | ALM1EN | ALM0EN | EXTOSC | CRSTRIM | SQWFS1 | SQWFS0 |
| bit 7 |       |        |        |        |         |        | bit 0  |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

|         |                                                                                                                                                                                                                                                                                                                                                       |
|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 7   | <b>OUT:</b> Logic Level for General Purpose Output<br><u>Square Wave Clock Output Mode (SQWEN = 1):</u><br>Unused.<br><u>General Purpose Output Mode (SQWEN = 0):</u><br>1 = CLKOUT signal level is logic high<br>0 = CLKOUT signal level is logic low                                                                                                |
| bit 6   | <b>SQWEN:</b> Square Wave Output Enable bit<br>1 = Enable Square Wave Clock Output mode<br>0 = Disable Square Wave Clock Output mode                                                                                                                                                                                                                  |
| bit 5   | <b>ALM1EN:</b> Alarm 1 Module Enable bit<br>1 = Alarm 1 enabled<br>0 = Alarm 1 disabled                                                                                                                                                                                                                                                               |
| bit 4   | <b>ALM0EN:</b> Alarm 0 Module Enable bit<br>1 = Alarm 0 enabled<br>0 = Alarm 0 disabled                                                                                                                                                                                                                                                               |
| bit 3   | <b>EXTOSC:</b> External Oscillator Input bit<br>1 = Enable X1 pin to be driven by external 32.768 kHz source<br>0 = Disable external 32.768 kHz input                                                                                                                                                                                                 |
| bit 2   | <b>CRSTRIM:</b> Coarse Trim Mode Enable bit<br>Coarse Trim mode results in the MCP795WXX applying digital trimming every second.<br>1 = Enable Coarse Trim mode. If SQWEN = 1, CLKOUT will output trimmed 1 Hz <sup>(1)</sup> nominal clock signal.<br>0 = Disable Coarse Trim mode<br>See <a href="#">Section 5.9 “Digital Trimming”</a> for details |
| bit 1-0 | <b>SQWFS&lt;1:0&gt;:</b> Square Wave Clock Output Frequency Select bits<br><u>If SQWEN = 1 and CRSTRIM = 0:</u><br>Selects frequency of clock output on CLKOUT<br>00 = 1 Hz <sup>(1)</sup><br>01 = 4.096 kHz <sup>(1)</sup><br>10 = 8.192 kHz <sup>(1)</sup><br>11 = 32.768 kHz<br><u>If SQWEN = 0 or CRSTRIM = 1:</u><br>Unused.                     |

**Note 1:** The 8.192 kHz, 4.096 kHz, and 1 Hz square wave clock output frequencies are affected by digital trimming.

**TABLE 5-16: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK OUTPUT CONFIGURATION**

| Name    | Bit 7 | Bit 6 | Bit 5  | Bit 4  | Bit 3  | Bit 2   | Bit 1  | Bit 0  | Register on Page   |
|---------|-------|-------|--------|--------|--------|---------|--------|--------|--------------------|
| CONTROL | OUT   | SQWEN | ALM1EN | ALM0EN | EXTOSC | CRSTRIM | SQWFS1 | SQWFS0 | <a href="#">35</a> |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used in clock output configuration.

## 5.8 Interrupt Outputs

The MCP795WXX features interrupt outputs for the alarm and event detect modules. The alarm interrupt output can be assigned to either the  $\overline{\text{IRQ}}$  pin or the  $\overline{\text{WDO}}$  pin, based on the setting of the ALMxPIN bit for each alarm module. Setting ALMxPIN to a '1' assigns the associated alarm module to the  $\overline{\text{WDO}}$  pin and clearing ALMxPIN to a '0' assigns the module to the  $\overline{\text{IRQ}}$  pin. The event detect modules are always assigned to the  $\overline{\text{IRQ}}$  pin.

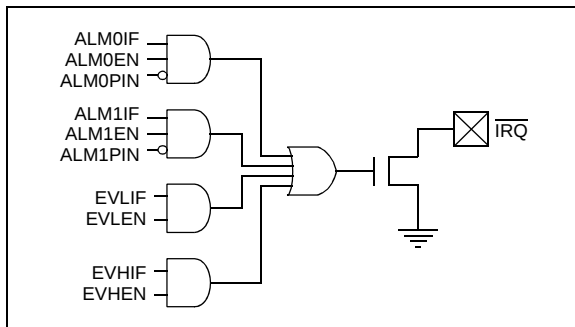
Both the  $\overline{\text{IRQ}}$  and the  $\overline{\text{WDO}}$  pins are active-low.

### 5.8.1 $\overline{\text{IRQ}}$ INTERRUPT OUTPUT

The interrupt outputs of modules that are enabled and assigned to the  $\overline{\text{IRQ}}$  pin are OR'd together. If any of the interrupt flags are set, then the  $\overline{\text{IRQ}}$  pin will assert low. In order to deassert the  $\overline{\text{IRQ}}$  pin, all of the assigned interrupt flags must be cleared or the modules must be disabled.

The  $\overline{\text{IRQ}}$  interrupt output is available when operating from the backup power supply.

**FIGURE 5-14:  $\overline{\text{IRQ}}$  OUTPUT BLOCK DIAGRAM**



### 5.8.2 $\overline{\text{WDO}}$ INTERRUPT OUTPUT

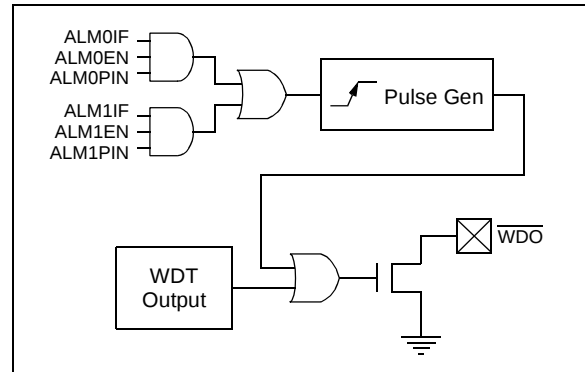
If an alarm module is enabled and assigned to the  $\overline{\text{WDO}}$  pin, then when the alarm triggers and the interrupt flag, ALMxIF, is set, the  $\overline{\text{WDO}}$  pin will be asserted low for 8 oscillator cycles (244  $\mu\text{s}$  nominal assuming a 32.768 kHz clock frequency) and then deasserted again. The ALMxIF flag must then be cleared to rearm the  $\overline{\text{WDO}}$  output and allow it to trigger again upon the next alarm interrupt.

If both alarm modules are enabled and assigned to the  $\overline{\text{WDO}}$  pin, then either module can trigger the  $\overline{\text{WDO}}$  output pulse. However, both ALMxIF flags must be cleared for the  $\overline{\text{WDO}}$  output to trigger upon the next alarm interrupt.

The Watchdog Timer output on the  $\overline{\text{WDO}}$  pin is independent of the alarm modules and will occur regardless of the state of the alarm modules and their interrupt flags.

The  $\overline{\text{WDO}}$  interrupt output is available when operating from the backup power supply.

**FIGURE 5-15:  $\overline{\text{WDO}}$  OUTPUT BLOCK DIAGRAM**



**TABLE 5-17: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT OUTPUT CONFIGURATION**

| Name      | Bit 7   | Bit 6    | Bit 5    | Bit 4    | Bit 3   | Bit 2   | Bit 1  | Bit 0  | Register on Page |
|-----------|---------|----------|----------|----------|---------|---------|--------|--------|------------------|
| EVDTCON   | EVHIF   | EVLIF    | EVHEN    | EVLEN    | EVWDTEN | EVLPS   | EVHCS1 | EVHCS0 | TBD              |
| ALM0WKDAY | ALM0PIN | ALM0MSK2 | ALM0MSK1 | ALM0MSK0 | ALM0IF  | WKDAY2  | WKDAY1 | WKDAY0 | 26               |
| ALM1WKDAY | ALM1PIN | ALM1MSK2 | ALM1MSK1 | ALM1MSK0 | ALM1IF  | WKDAY2  | WKDAY1 | WKDAY0 | 26               |
| CONTROL   | OUT     | SQWEN    | ALM1EN   | ALM0EN   | EXTOSC  | CRSTRIM | SQWFS1 | SQWFS0 | 35               |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used in interrupt output configuration.

## 5.9 Digital Trimming

The MCP795WXX features digital trimming to correct for inaccuracies of the external crystal or clock source, up to roughly  $\pm 259$  ppm when CRSTRIM = 0. In addition to compensating for intrinsic inaccuracies in the clock, this feature can also be used to correct for error due to temperature variation. This can enable the user to achieve high levels of accuracy across a wide temperature operating range.

Digital trimming consists of the MCP795WXX periodically adding or subtracting clock cycles, resulting in small adjustments in the internal timing.

The adjustment occurs once per minute when CRSTRIM = 0. The TRIMSIGN bit specifies whether to add cycles or to subtract them. The TRIMVAL<7:0> bits are used to specify by how many clock cycles to adjust. Each step in the TRIMVAL<7:0> value equates to adding or subtracting two clock pulses to or from the 32.768 kHz clock signal. This results in a correction of roughly 1.017 ppm per step when CRSTRIM = 0. Setting TRIMVAL<7:0> to 0x00 disables digital trimming.

Digital trimming also occurs while operating off the backup supply.

### REGISTER 5-19: OSCTRIM: OSCILLATOR DIGITAL TRIM REGISTER (ADDRESS 0x09)

| R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| TRIMVAL7 | TRIMVAL6 | TRIMVAL5 | TRIMVAL4 | TRIMVAL3 | TRIMVAL2 | TRIMVAL1 | TRIMVAL0 |
| bit 7    |          |          |          |          |          |          | bit 0    |

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

bit 7-0

**TRIMVAL<7:0>:** Oscillator Trim Value bits

When CRSTRIM = 0:

11111111 = Add or subtract 510 clock cycles every minute

11111110 = Add or subtract 508 clock cycles every minute

•

•

•

00000010 = Add or subtract 4 clock cycles every minute

00000001 = Add or subtract 2 clock cycles every minute

00000000 = Disable digital trimming

When CRSTRIM = 1:

11111111 = Add or subtract 510 clock cycles every second

11111110 = Add or subtract 508 clock cycles every second

•

•

•

00000010 = Add or subtract 4 clock cycles every second

00000001 = Add or subtract 2 clock cycles every second

00000000 = Disable digital trimming

## 5.9.1 CALIBRATION

In order to perform calibration, the number of error clock pulses per minute must be found and the corresponding trim value must be loaded into TRIMVAL<7:0>.

There are two methods for determining the trim value. The first method involves measuring an output frequency directly and calculating the deviation from ideal. The second method involves observing the number of seconds gained or lost over a period of time.

Once the OSCTRIM register has been loaded, digital trimming will automatically occur every minute (CRSTRIM = 0).

### 5.9.1.1 Calibration by Measuring Frequency

To calibrate the MCP795WXX by measuring the output frequency, perform the following steps:

1. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
2. Ensure TRIMVAL<7:0> is reset to 0x00.
3. Select an output frequency by setting SQWFS<1:0>.
4. Set SQWEN to enable the square wave output.
5. Measure the resulting output frequency using a calibrated measurement tool, such as a frequency counter.
6. Calculate the number of error clocks per minute (see Equation 5-3).

#### EQUATION 5-3: CALCULATING TRIM VALUE FROM MEASURED FREQUENCY

$$\text{TRIMVAL}<7:0> = \frac{(F_{\text{IDEAL}} - F_{\text{MEAS}}) \cdot \frac{32768}{F_{\text{IDEAL}}} \cdot 60}{2}$$

Where:

$F_{\text{IDEAL}}$  = Ideal frequency based on SQWFS<1:0>  
 $F_{\text{MEAS}}$  = Measured frequency

- If the number of error clocks per minute is negative, then the oscillator is *faster* than ideal and the TRIMSIGN bit must be cleared.
  - If the number of error clocks per minute is positive, then the oscillator is *slower* than ideal and the TRIMSIGN bit must be set.
7. Load the correct value into TRIMVAL<7:0>.

**Note:** Using a lower output frequency and/or averaging the measured frequency over a number of clock pulses will reduce the effects of jitter and improve accuracy.

### 5.9.1.2 Calibration by Observing Time Deviation

To calibrate the MCP795WXX by observing the deviation over time, perform the following steps:

1. Ensure TRIMVAL<7:0> is reset to 0x00.
2. Load the timekeeping registers to synchronize the MCP795WXX with a known-accurate reference time.
3. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
4. Observe how many seconds are gained or lost over a period of time (larger time periods offer more accuracy).
5. Calculate the PPM deviation (see Equation 5-4).

#### EQUATION 5-4: CALCULATING ERROR PPM

$$\text{PPM} = \frac{\text{SecDeviation}}{\text{ExpectedSec}} \cdot 1000000$$

Where:

$\text{ExpectedSec}$  = Number of seconds in chosen period  
 $\text{SecDeviation}$  = Number of seconds gained or lost

- If the MCP795WXX has gained time relative to the reference clock, then the oscillator is *faster* than ideal and the TRIMSIGN bit must be cleared.
  - If the MCP795WXX has lost time relative to the reference clock, then the oscillator is *slower* than ideal and the TRIMSIGN bit must be set.
6. Calculate the trim value (see Equation 5-5).

#### EQUATION 5-5: CALCULATING TRIM VALUE FROM ERROR PPM

$$\text{TRIMVAL}<7:0> = \frac{\text{PPM} \cdot 32768 \cdot 60}{1000000 \cdot 2}$$

7. Load the correct value into TRIMVAL<7:0>.

**Note 1:** Choosing a longer time period for observing deviation will improve accuracy.

**2:** Large temperature variations during the observation period can skew results.

# MCP795W1X/MCP795W2X

## 5.9.2 COARSE TRIM MODE

When CRSTRIM = 1, Coarse Trim mode is enabled. While in this mode, the MCP795WXX will apply trimming every second. If SQWEN is set, the CLKOUT pin will output a trimmed 1 Hz nominal clock signal.

Because trimming is applied every second rather than every minute, each step of the TRIMVAL<7:0> value has a larger effect on the resulting time deviation and output clock frequency.

By monitoring the CLKOUT output frequency while in this mode, the user can easily observe the TRIMVAL<7:0> value affecting the clock timing.

- Note 1:** The 1 Hz Coarse Trim mode square wave output is not available while operating from the backup power supply.
- 2:** With Coarse Trim mode enabled, the TRIMVAL<7:0> value has a larger effect on timing. Leaving the mode enabled during normal operation will likely result in inaccurate time.

**TABLE 5-18: SUMMARY OF REGISTERS ASSOCIATED WITH DIGITAL TRIMMING**

| Name    | Bit 7    | Bit 6    | Bit 5           | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Register on Page |
|---------|----------|----------|-----------------|----------|----------|----------|----------|----------|------------------|
| RTCHOUR | TRIMSIGN | 12/24    | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   | 19               |
| CONTROL | OUT      | SQWEN    | ALM1EN          | ALM0EN   | EXTOSC   | CRSTRIM  | SQWFS1   | SQWFS0   | 35               |
| OSCTRIM | TRIMVAL7 | TRIMVAL6 | TRIMVAL5        | TRIMVAL4 | TRIMVAL3 | TRIMVAL2 | TRIMVAL1 | TRIMVAL0 | 37               |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by digital trimming.

## 5.10 Battery Backup

The MCP795WXX features a backup power supply input (VBAT) that can be used to provide power to the timekeeping circuitry, RTCC registers, and SRAM while primary power is unavailable. The MCP795WXX will automatically switch to backup power when VCC falls below VTRIP, and back to VCC when it is above VTRIP.

The VBATEN bit must be set to enable the VBAT input.

The following functionality is maintained while operating on backup power:

- Timekeeping
- Alarms
- Alarm Outputs
- Digital Trimming
- RTCC Register and SRAM Contents

The following features are not available while operating on backup power:

- SPI Communication
- Watchdog Timer
- Event Detect
- Square Wave Clock Output
- General Purpose Output

**Note:** The Watchdog Timer is automatically disabled when primary power is lost and is not automatically re-enabled when power is restored.

### 5.10.1 POWER-FAIL TIMESTAMP

The MCP795WXX includes a power-fail timestamp module that stores the minutes, hours, date, and month when primary power is lost and when it is restored (Figure 5-16). The PWRFAIL bit is also set to indicate that a power failure occurred.

**Note:** Throughout this section, references to the register and bit names for the Power-Fail Timestamp module are referred to generically by the use of 'x' in place of the specific module name. Thus, "PWRxxMIN" might refer to the minutes register for power-down or power-up.

To utilize the power-fail timestamp feature, a backup power supply must be available with the VBAT input enabled, and the oscillator should also be running to ensure accurate functionality.

**Note 1:** The PWRFAIL bit must be cleared to log new timestamp data. This is to ensure previous timestamp data is not lost.

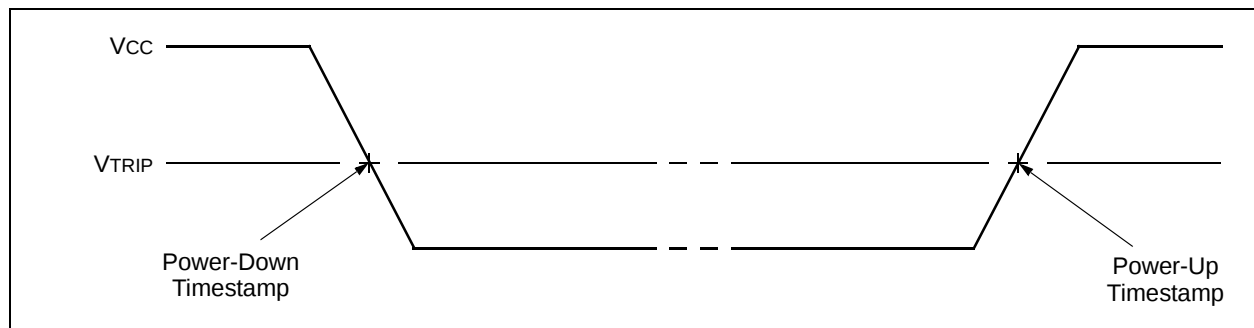
**2:** Clearing the PWRFAIL bit will clear all timestamp registers.

#### 5.10.1.1 Configuring Battery Backup

In order to configure the battery backup feature, the following steps need to be performed:

1. Enable the oscillator.
2. Wait for the OSCRUN bit to be set, indicating the oscillator has started.
3. Enable battery backup by setting the VBATEN bit.

**FIGURE 5-16: POWER-FAIL TIMESTAMP TIMING**



# MCP795W1X/MCP795W2X

## REGISTER 5-20: PWRxxMIN: POWER-DOWN/POWER-UP TIMESTAMP MINUTES VALUE REGISTER (ADDRESSES 0x18/0x1C)

| U-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   |
|-------|---------|---------|---------|---------|---------|---------|---------|
| —     | MINTEN2 | MINTEN1 | MINTEN0 | MINONE3 | MINONE2 | MINONE1 | MINONE0 |
| bit 7 |         |         |         |         |         |         | bit 0   |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

bit 7                      **Unimplemented:** Read as '0'  
 bit 6-4                      **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute's Tens Digit  
                                     Contains a value from 0 to 5  
 bit 3-0                      **MINONE<3:0>:** Binary-Coded Decimal Value of Minute's Ones Digit  
                                     Contains a value from 0 to 9

## REGISTER 5-21: PWRxxHOUR: POWER-DOWN/POWER-UP TIMESTAMP HOURS VALUE REGISTER (ADDRESSES 0x19/0x1D)

| U-0   | R/W-0 | R/W-0           | R/W-0  | R/W-0  | R/W-0  | R/W-0  | R/W-0  |
|-------|-------|-----------------|--------|--------|--------|--------|--------|
| —     | 12/24 | AM/PM<br>HRTEN1 | HRTEN0 | HRONE3 | HRONE2 | HRONE1 | HRONE0 |
| bit 7 |       |                 |        |        |        |        | bit 0  |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

### If 12/24 = 1 (12-hour format):

bit 7                      **Unimplemented:** Read as '0'  
 bit 6                      **12/24:** 12 or 24 Hour Time Format bit  
                                     1 = 12-hour format  
                                     0 = 24-hour format  
 bit 5                      **AM/PM:** AM/PM Indicator bit  
                                     1 = PM  
                                     0 = AM  
 bit 4                      **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit  
                                     Contains a value from 0 to 1  
 bit 3-0                      **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit  
                                     Contains a value from 0 to 9

### If 12/24 = 0 (24-hour format):

bit 7                      **Unimplemented:** Read as '0'  
 bit 6                      **12/24:** 12 or 24 Hour Time Format bit  
                                     1 = 12-hour format  
                                     0 = 24-hour format  
 bit 5-4                      **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit  
                                     Contains a value from 0 to 2.  
 bit 3-0                      **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit  
                                     Contains a value from 0 to 9

# MCP795W1X/MCP795W2X

## REGISTER 5-22: PWRxxDATE: POWER-DOWN/POWER-UP TIMESTAMP DATE VALUE REGISTER (ADDRESSES 0x1A/0x1E)

|       |     |          |          |          |          |          |          |
|-------|-----|----------|----------|----------|----------|----------|----------|
| U-0   | U-0 | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    | R/W-0    |
| —     | —   | DATETEN1 | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 |
| bit 7 |     |          |          |          |          |          | bit 0    |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

- bit 7-6                      **Unimplemented:** Read as '0'  
 bit 5-4                      **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit  
                                  Contains a value from 0 to 3  
 bit 3-0                      **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit  
                                  Contains a value from 0 to 9

## REGISTER 5-23: PWRxxMTH: POWER-DOWN/POWER-UP TIMESTAMP MONTH VALUE REGISTER (ADDRESSES 0x1B/0x1F)

|        |        |        |         |         |         |         |         |
|--------|--------|--------|---------|---------|---------|---------|---------|
| R/W-0  | R/W-0  | R/W-0  | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   |
| WKDAY2 | WKDAY1 | WKDAY0 | MTHTEN0 | MTHONE3 | MTHONE2 | MTHONE1 | MTHONE0 |
| bit 7  |        |        |         |         |         |         | bit 0   |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is clear                      x = Bit is unknown

- bit 7-5                      **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits  
                                  Contains a value from 1 to 7. The representation is user-defined.  
 bit 4                      **MTHTEN0:** Binary-Coded Decimal Value of Month's Ones Digit  
                                  Contains a value of 0 or 1  
 bit 3-0                      **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit  
                                  Contains a value from 0 to 9

## TABLE 5-19: SUMMARY OF REGISTERS ASSOCIATED WITH BATTERY BACKUP

| Name       | Bit 7  | Bit 6   | Bit 5           | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Register on Page |
|------------|--------|---------|-----------------|----------|----------|----------|----------|----------|------------------|
| RTCWKDAY   | —      | —       | OSCRUN          | PWRFAIL  | VBATEN   | WKDAY2   | WKDAY1   | WKDAY0   | 20               |
| PWRDNMIN   | —      | MINTEN2 | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  | 41               |
| PWRDNDHOUR | —      | 12/24   | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   | 41               |
| PWRDNDATE  | —      | —       | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 | 42               |
| PWRDNMTH   | WKDAY2 | WKDAY1  | WKDAY0          | MTHTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  | 42               |
| PWRUPMIN   | —      | MINTEN2 | MINTEN1         | MINTEN0  | MINONE3  | MINONE2  | MINONE1  | MINONE0  | 41               |
| PWRUPHOUR  | —      | 12/24   | AM/PM<br>HRTEN1 | HRTEN0   | HRONE3   | HRONE2   | HRONE1   | HRONE0   | 41               |
| PWRUPDATE  | —      | —       | DATETEN1        | DATETEN0 | DATEONE3 | DATEONE2 | DATEONE1 | DATEONE0 | 42               |
| PWRUPMTH   | WKDAY2 | WKDAY1  | WKDAY0          | MTHTEN0  | MTHONE3  | MTHONE2  | MTHONE1  | MTHONE0  | 42               |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used with battery backup.

## 6.0 ON-BOARD MEMORY

The MCP795W2X has 2 Kbits (256 bytes) of EEPROM, while the MCP795W1X has 1 Kbit (128 bytes) of EEPROM. In addition, the devices have 16 bytes of protected EEPROM for storing crucial information, and 64 bytes of SRAM for general purpose usage. The SRAM is retained when the primary power supply is removed if a backup supply is present and enabled. Since the EEPROM is nonvolatile, it does not require a supply for data retention.

Although the SRAM is a separate block from the RTCC registers, they are accessed using the same instructions, READ and WRITE. The EEPROM is accessed using the EEREAD and EEWRITE instructions, and the protected EEPROM is accessed using the IDREAD and IDWRITE instructions. RTCC and SRAM can be accessed for reads or writes immediately after starting an EEPROM write cycle.

### 6.1 SRAM/RTCC Registers

The RTCC registers are located at addresses 0x00 to 0x1F, and the SRAM is located at addresses 0x20 to 0x5F. The SRAM can be accessed while the RTCC registers are being internally updated. The SRAM is not initialized by a Power-on Reset (POR).

Neither the RTCC registers nor the SRAM can be accessed when the device is operating off the backup power supply.

#### 6.1.1 SRAM/RTCC REGISTER WRITE SEQUENCE

The device is selected by pulling  $\overline{CS}$  low. The 8-bit WRITE instruction is transmitted to the MCP795WXX followed by an 8-bit address. Next, the data to be written is transmitted.

There is no limit to the number of bytes that can be written in a single command. However, because the RTCC registers and SRAM are separate blocks, writing past the end of each block will cause the internal Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

Each data byte is latched into memory as it is received. Once all data bytes have been transmitted,  $\overline{CS}$  is driven high to end the operation (Figure 6-1).

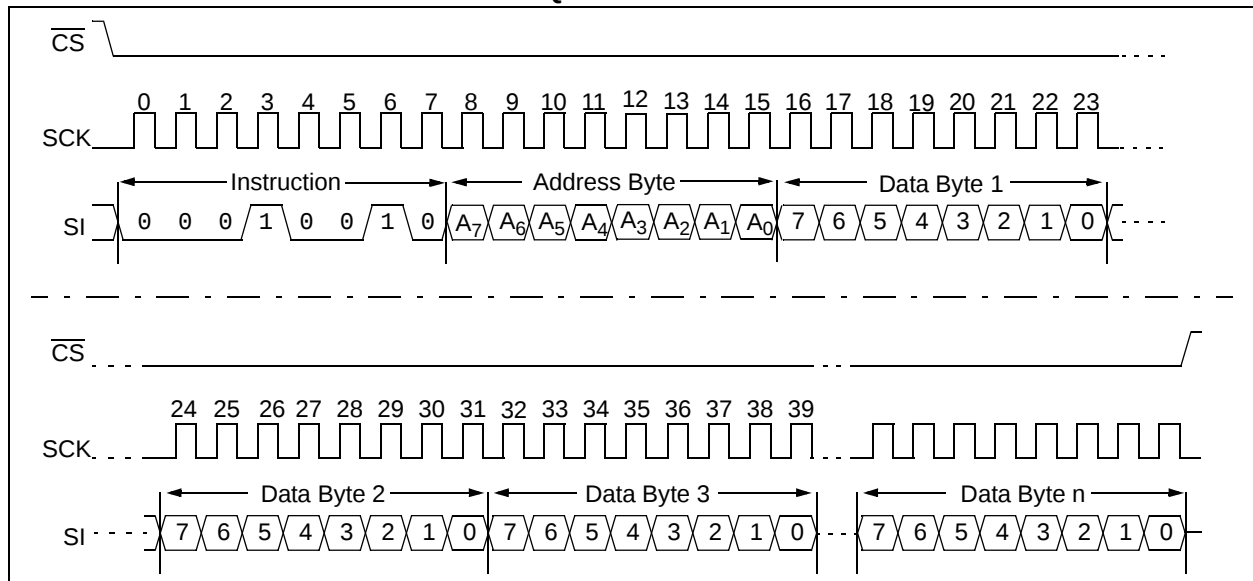
#### 6.1.2 SRAM/RTCC REGISTER READ SEQUENCE

The device is selected by pulling  $\overline{CS}$  low. The 8-bit READ instruction is transmitted to the MCP795WXX followed by an 8-bit address.

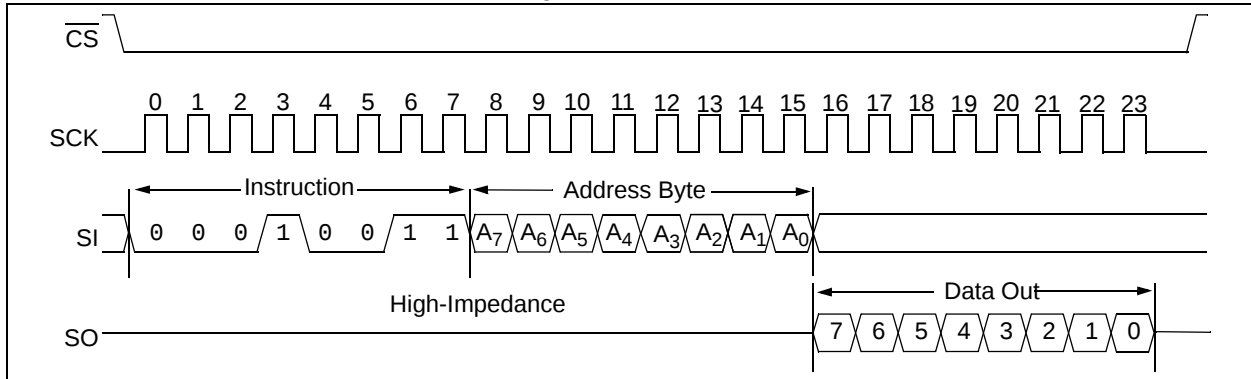
After the READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. The Address Pointer allows the entire memory block to be serially read during one operation. The read operation is terminated by driving  $\overline{CS}$  high (Figure 6-2).

Because the RTCC registers and SRAM are separate blocks, reading past the end of each block will cause the Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

**FIGURE 6-1: SRAM/RTCC WRITE SEQUENCE**



**FIGURE 6-2: SRAM/RTCC READ SEQUENCE**

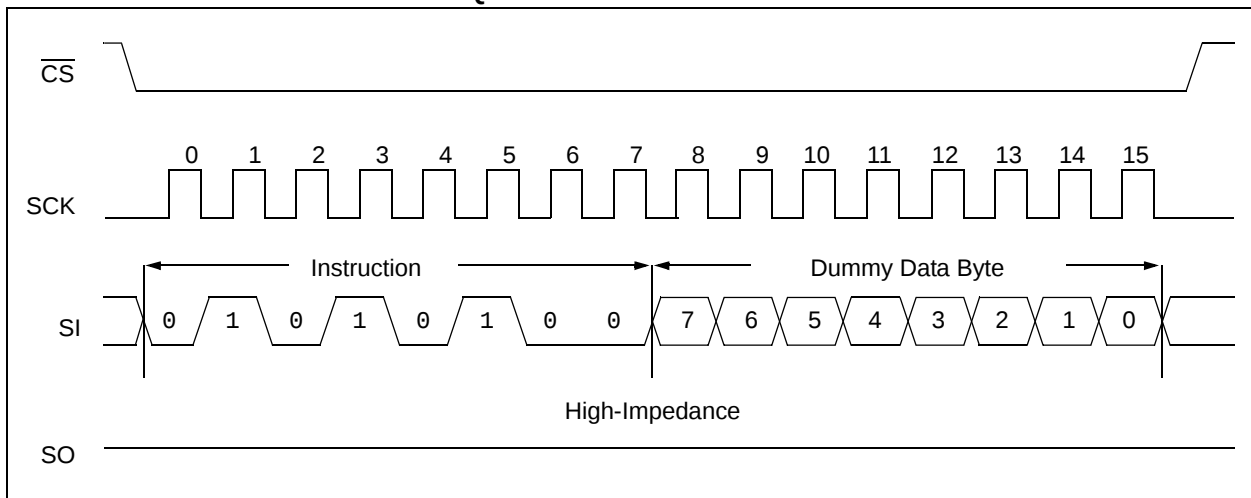


## 6.1.3 CLEAR SRAM INSTRUCTION

The CLRRAM instruction can be used to quickly clear the contents of SRAM to 0x00. The RTCC registers are not affected.

The device is selected by pulling  $\overline{CS}$  low. The 8-bit CLRRAM instruction is transmitted to the MCP795WXX followed by an 8-bit dummy data byte.  $\overline{CS}$  is driven high to end the operation (Figure 6-3). The value of the data byte is ignored.

**FIGURE 6-3: CLEAR SRAM SEQUENCE**



# MCP795W1X/MCP795W2X

## 6.2 STATUS Register

The STATUS register contains the BP<1:0>, WEL and WIP bits. The STATUS register is accessed using the SRREAD and SRWRITE instructions.

The Block Protection (BP<1:0>) bits are used to set the block write protection for the EEPROM array according to Table 6-1. These bits are set by the user issuing the SRWRITE instruction. These bits are nonvolatile.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the nonvolatile memory, when set to a '0', the latch prohibits writes to the nonvolatile memory. The state of this bit can be updated via the EEWREN or EEWRDI instructions. This bit is read-only.

The WIP bit indicates whether the MCP795WXX is busy with a nonvolatile memory write operation. When set to a '1', a write is in progress. When set to a '0', no write is in progress. This bit is read-only.

**TABLE 6-1: BLOCK PROTECTION**

| BP1 | BP0 | Array Addresses Write-Protected                         |
|-----|-----|---------------------------------------------------------|
| 0   | 0   | None                                                    |
| 0   | 1   | Upper 1/4<br>60h-7Fh (MCP795W1X)<br>C0h-FFh (MCP795W2X) |
| 1   | 0   | Upper 1/2<br>40h-7Fh (MCP795W1X)<br>80h-FFh (MCP795W2X) |
| 1   | 1   | All                                                     |

**REGISTER 6-1: STATUS: EEPROM WRITE PROTECTION REGISTER**

|       |     |     |     |       |     |     |     |
|-------|-----|-----|-----|-------|-----|-----|-----|
| U-0   | U-0 | U-0 | U-0 | R/W   | R/W | R-0 | R-0 |
| —     | —   | —   | —   | BP1   | BP0 | WEL | WIP |
| bit 7 |     |     |     | bit 0 |     |     |     |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is clear

x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **BP<1:0>:** EEPROM Array Block Protection bits  
Selects which EEPROM region is write-protected  
00 = None  
01 = Upper 1/4  
10 = Upper 1/2  
11 = All

bit 1 **WEL:** Write Enable Latch bit  
Indicates whether or not nonvolatile memory writes are enabled. It is automatically cleared at the end of a nonvolatile memory write cycle.  
0 = Writes to nonvolatile memory are not enabled  
1 = Writes to nonvolatile memory are enabled

bit 0 **WIP:** Write-In-Process bit  
Indicates whether or not a nonvolatile memory write cycle is in process  
0 = Nonvolatile write cycle is not in process  
1 = Nonvolatile write cycle is in process

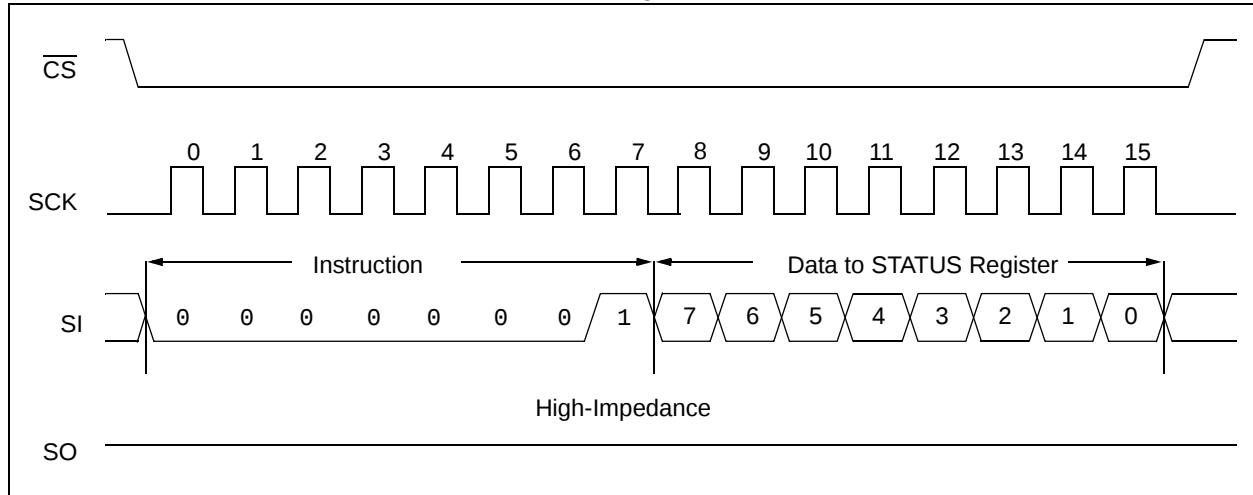
### 6.2.1 STATUS REGISTER WRITE SEQUENCE

The Write Status Register instruction (SRWRITE) allows the user to write to the nonvolatile bits in the STATUS register.

Prior to any attempt to write data to the STATUS register, the write enable latch must be set by issuing the EEWREN instruction. This is done by setting CS low and then clocking out the proper instruction into the MCP795WXX.

After all eight bits of the instruction are transmitted,  $\overline{\text{CS}}$  must be driven high to set the write enable latch. If the write operation is initiated immediately after the EEWREN instruction without  $\overline{\text{CS}}$  driven high, data will not be written to the array since the write enable latch was not properly set. The device is selected by pulling  $\overline{\text{CS}}$  low. The 8-bit SRWRITE instruction is transmitted to the MCP795WXX followed by the 8-bit data byte.  $\overline{\text{CS}}$  is driven high to end the operation and initiate the nonvolatile write cycle (Figure 6-4).

**FIGURE 6-4: WRITE STATUS REGISTER SEQUENCE**

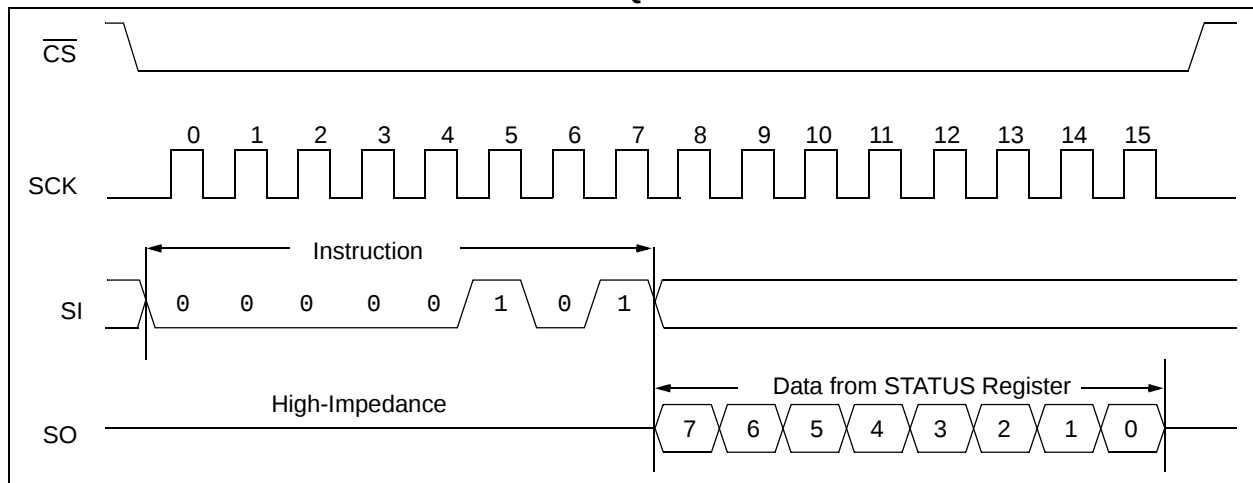


## 6.2.2 STATUS REGISTER READ SEQUENCE

The Read Status Register instruction (SRREAD) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. This allows the user to poll the WIP bit to determine when a write cycle is complete.

The device is selected by pulling  $\overline{CS}$  low. The 8-bit SRREAD instruction is transmitted to the MCP795WXX. The STATUS register value is then shifted out on the SO pin. The read operation is terminated by driving  $\overline{CS}$  high (Figure 6-5).

**FIGURE 6-5: READ STATUS REGISTER SEQUENCE**



## 6.3 EEPROM

The MCP795W2X features 2 Kbits of EEPROM, and the MCP795W1X features 1 Kbit of EEPROM. It is organized in 8-byte pages with software write protection configurable through the STATUS register.

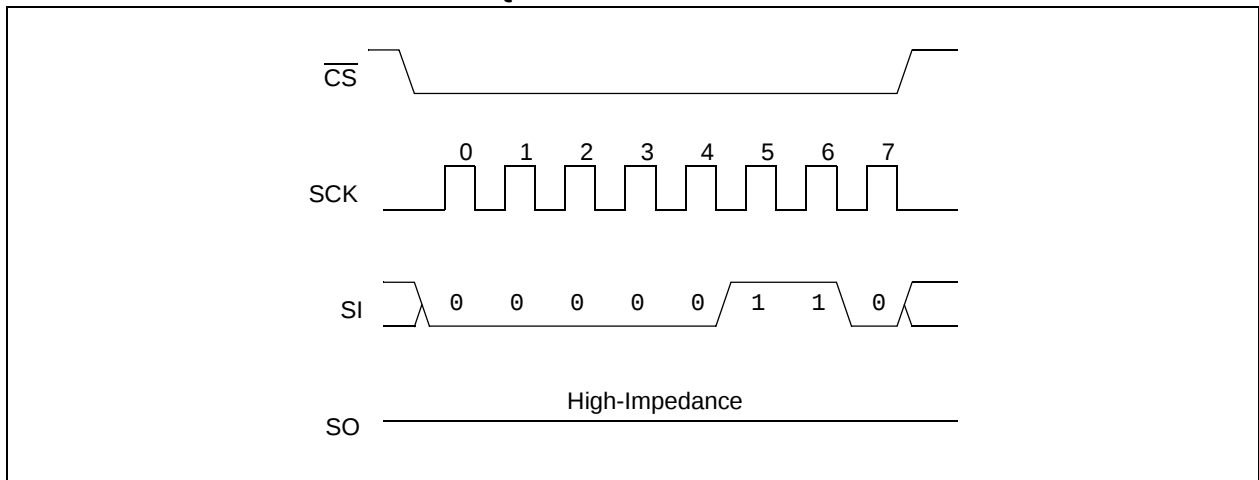
### 6.3.1 WRITE ENABLE AND WRITE DISABLE

The MCP795WXX contains a write enable latch. This latch must be set before any write operation will be completed internally. The EEWREN instruction will set the latch, and the EEWRDI instruction will reset the latch.

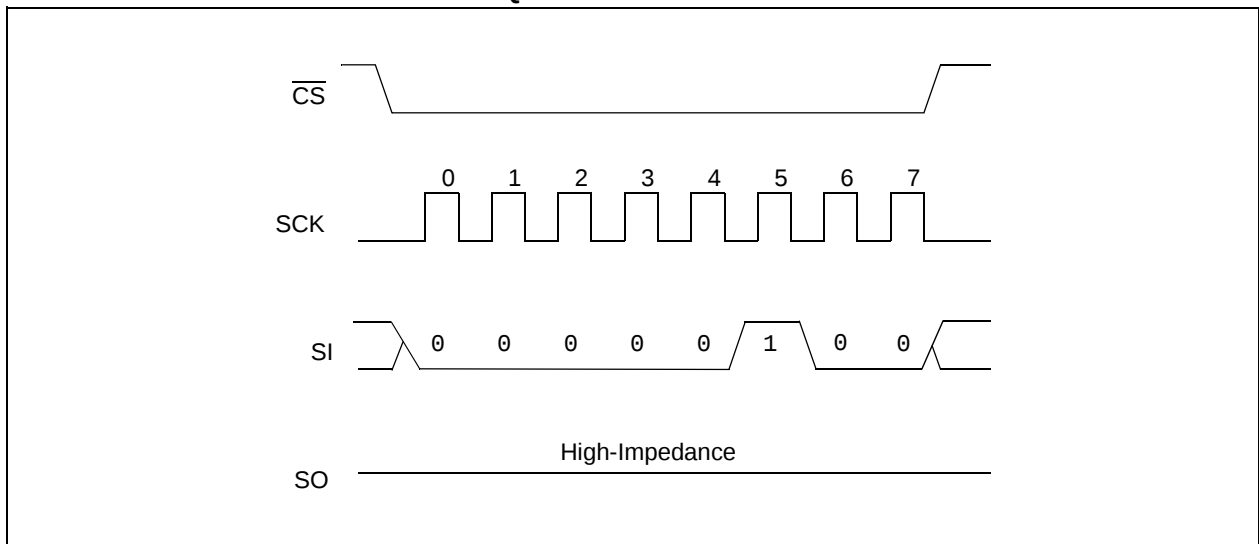
The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- EEWRITE instruction successfully executed
- SRWRITE instruction successfully executed
- IDWRITE instruction successfully executed
- Unlock sequence for protected EEPROM not followed correctly

**FIGURE 6-6: WRITE ENABLE SEQUENCE**



**FIGURE 6-7: WRITE DISABLE SEQUENCE**



## 6.3.2 EEPROM READ SEQUENCE

The device is selected by pulling  $\overline{CS}$  low. The 8-bit EEREAD instruction is transmitted to the MCP795WXX followed by an 8-bit address. See Figure 6-8 for more details.

After the correct EEREAD instruction and address are sent, the data stored in the EEPROM at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 00h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the  $\overline{CS}$  pin (Figure 6-8).

## 6.3.3 EEPROM WRITE SEQUENCE

Prior to any attempt to write data to the MCP795WXX EEPROM, the write enable latch must be set by issuing the EEWREN instruction. This is done by setting  $\overline{CS}$  low and then clocking out the proper instruction into the MCP795WXX. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must be driven high to set the write enable latch. If the write operation is initiated immediately after the EEWREN instruction without  $\overline{CS}$  driven high, data will not be written to the array since the write enable latch was not properly set.

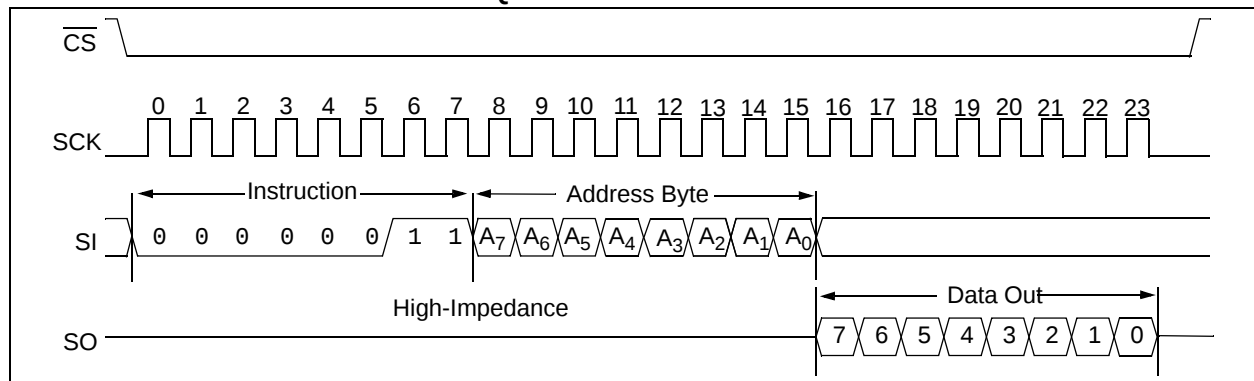
After setting the write enable latch, the user may proceed by driving  $\overline{CS}$  low, issuing an EEWRITE instruction, followed by the address, and then the data to be written. Up to eight bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Additionally, a page address begins with XXXX x000 and ends with XXXX x111. If the internal address counter reaches XXXX x111 and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and over-write any data that previously existed in those locations.

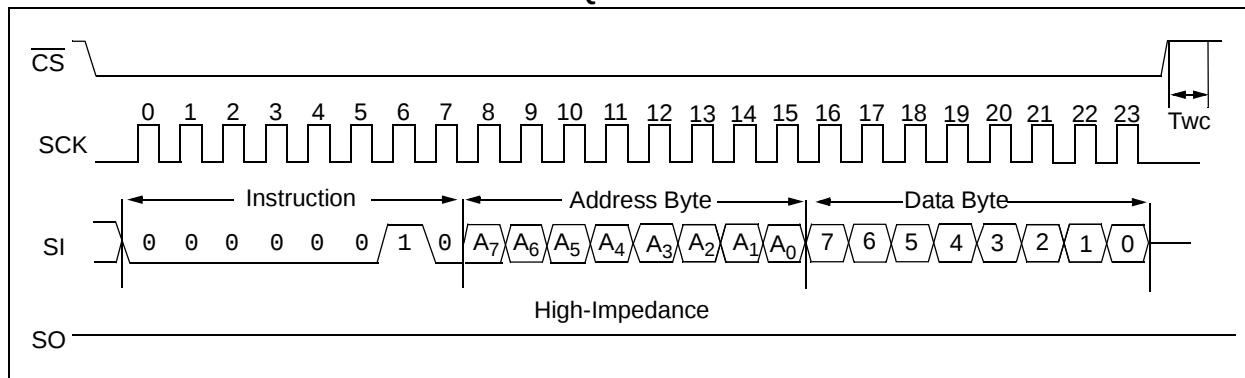
**Note:** EEPROM write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size – 1. If an EEWRITE command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent EEPROM write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the  $\overline{CS}$  must be brought high after the Least Significant bit (D0) of the  $n^{th}$  data byte has been clocked in. If  $\overline{CS}$  is driven high at any other time, the write operation will not be completed. Refer to Figure 6-9 and Figure 6-10 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits. Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

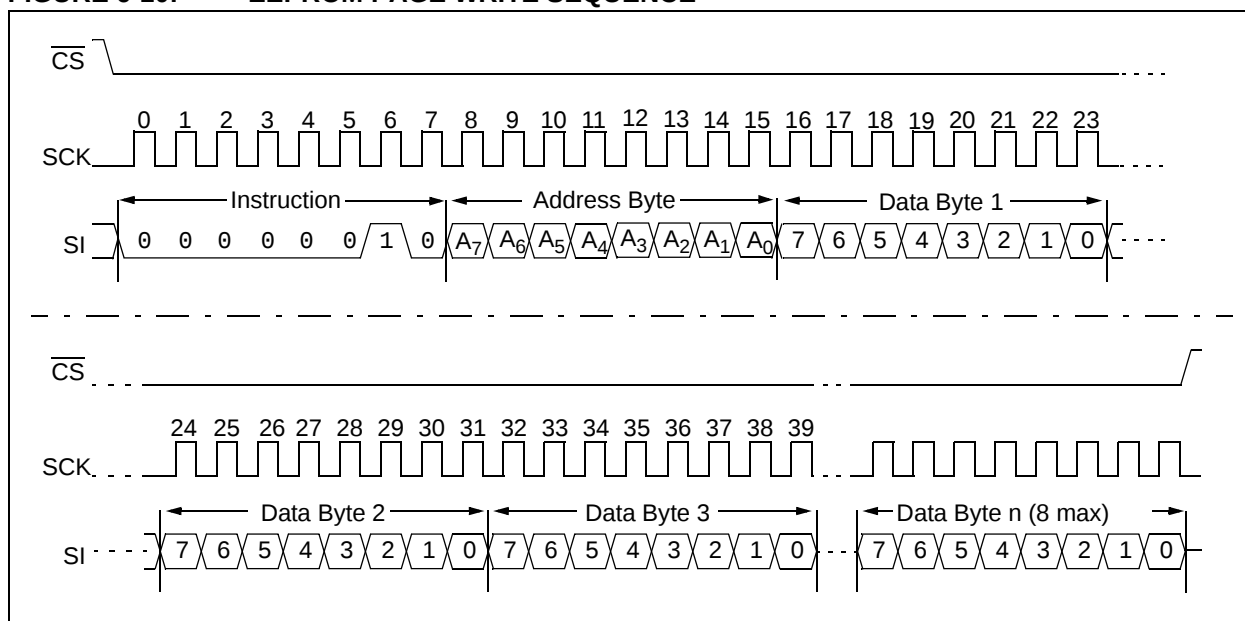
**FIGURE 6-8: EEPROM READ SEQUENCE**



**FIGURE 6-9: EEPROM BYTE WRITE SEQUENCE**



**FIGURE 6-10: EEPROM PAGE WRITE SEQUENCE**



## 6.4 Protected EEPROM

The MCP795WXX features a 128-bit protected EEPROM block, organized as two 8-byte pages, that requires a special unlock sequence to be followed in order to write to the memory. The protected EEPROM can be used for storing crucial information such as a unique serial number. The MCP795WX1 and MCP795WX2 include an EUJ-48 and EUJ-64 node address, respectively, preprogrammed into the protected EEPROM block. Custom programming is also available.

The protected EEPROM block is located at addresses 0x00 to 0x0F and is accessed using the IDREAD and IDWRITE instructions.

**Note:** Attempts to access addresses outside of 0x00 to 0x0F will result in the MCP795WXX ignoring the instruction.

### 6.4.1 PROTECTED EEPROM READ SEQUENCE

The device is selected by pulling  $\overline{CS}$  low. The 8-bit IDREAD instruction is transmitted to the MCP795WXX followed by an 8-bit address. See Figure 6-11 for more details.

After the correct IDREAD instruction and address are sent, the data stored in the protected EEPROM at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 00h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the CS pin.

## 6.4.2 PROTECTED EEPROM UNLOCK SEQUENCE

The protected EEPROM block requires a special unlock sequence to prevent unintended writes, utilizing the UNLOCK instruction.

Before performing the unlock sequence, the WEL bit must first be set by executing an EEWREN instruction (see [Section 6.3.1 “Write Enable and Write Disable”](#) for details).

To unlock the block, the following sequence must be followed after setting the WEL bit:

1. Execute an UNLOCK instruction with a data byte of 0x55
2. Execute an UNLOCK instruction with a data byte of 0xAA
3. Write the desired data bytes to the protected EEPROM using the IDWRITE instruction

[Figure 6-12](#) illustrates the sequence.

**Note 1:** Diverging from any step of the unlock sequence may result in the EEPROM remaining locked, the write operation being ignored, and the WEL bit being reset.

**2:** Unlocking the EEPROM is not required in order to read from the memory.

An entire protected EEPROM page does not have to be written in a single operation. However, the block is locked after each write operation and must be unlocked again to start a new Write command.

## 6.4.3 PROTECTED EEPROM WRITE SEQUENCE

Prior to any attempt to write data to the MCP795WXX protected EEPROM block, the write enable latch must be set by issuing the EEWREN instruction, and then the protected EEPROM unlock sequence must be performed. The EEWREN instruction is issued by setting  $\overline{CS}$  low and then clocking out the proper instruction into the MCP795WXX. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must be driven high to set the write enable latch.

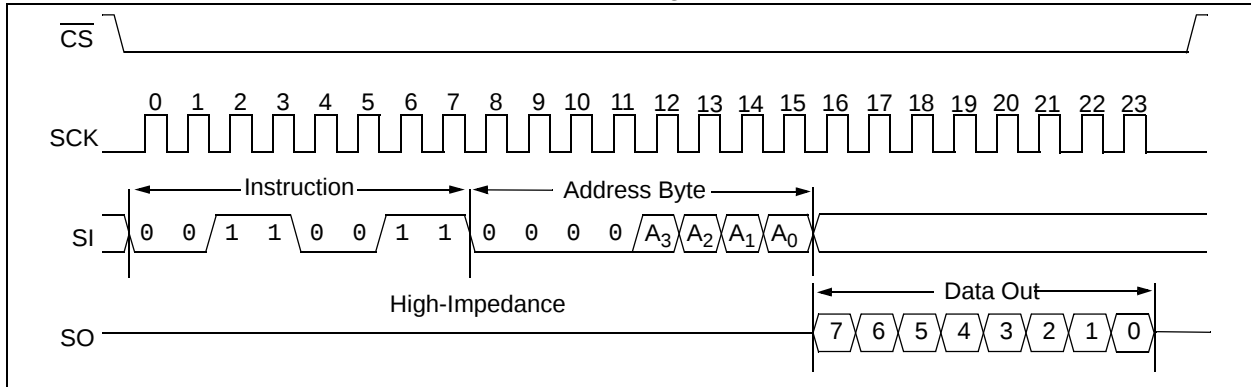
After setting the write enable latch and performing the unlock sequence, the user may proceed by driving  $\overline{CS}$  low, issuing an IDWRITE instruction, followed by the address, and then the data to be written. Up to 8 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with XXXX x000 and ends with XXXX x111. If the internal address counter reaches XXXX x111 and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and over-write any data that previously existed in those locations.

**Note:** Protected EEPROM write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and, end at addresses that are integer multiples of page size – 1. If an IDWRITE command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent protected EEPROM write operations that would attempt to cross a page boundary.

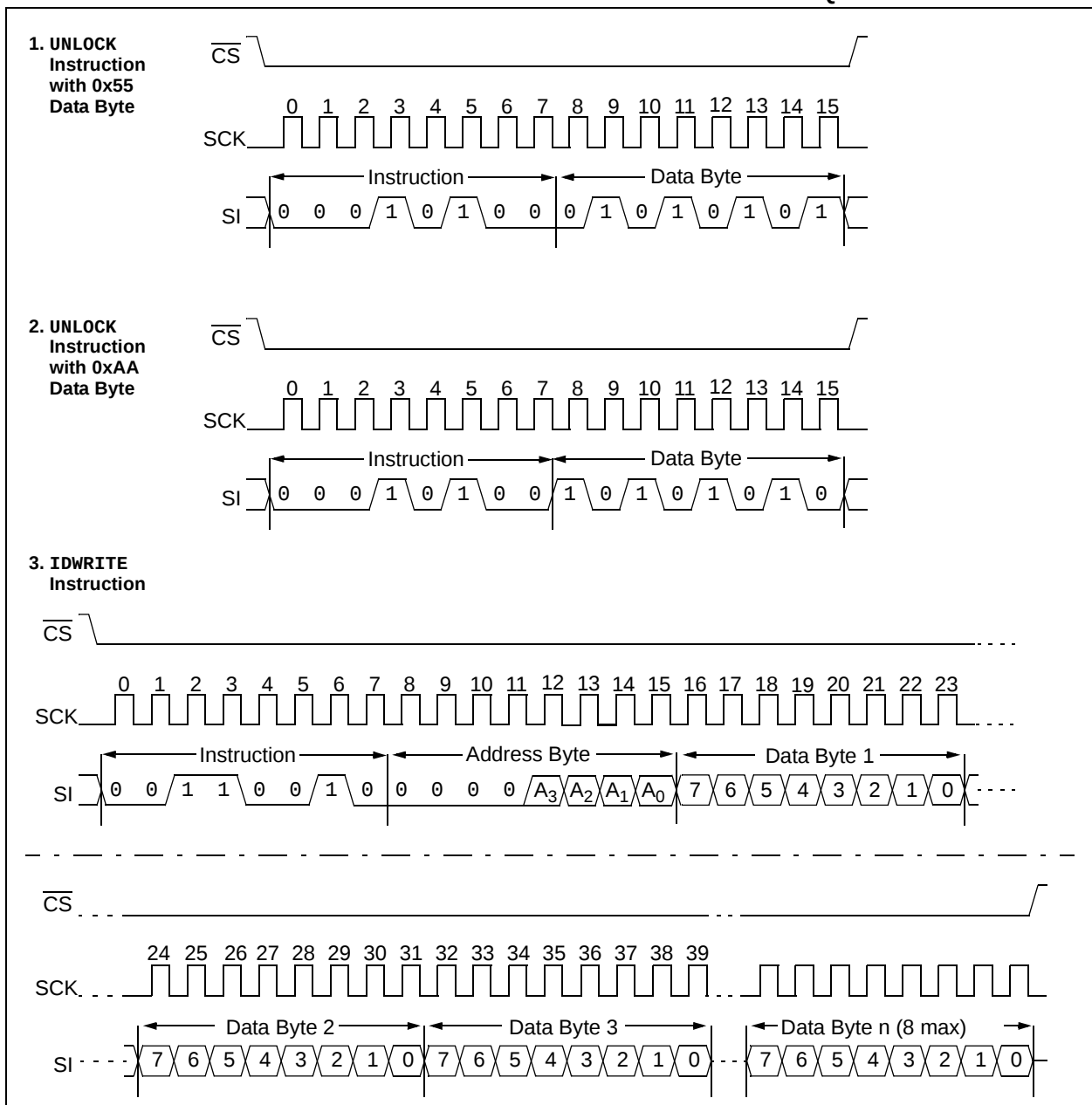
For the data to be actually written to the array, the  $\overline{CS}$  must be brought high after the Least Significant bit (D0) of the  $n^{th}$  data byte has been clocked in. If  $\overline{CS}$  is driven high at any other time, the write operation will not be completed. Refer to [Figure 6-12](#) for more detailed illustrations on the page write sequence. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits. Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

If an attempt is made to write to an address outside of the 0x00 to 0x0F range, the MCP795WXX will not execute the WRITE instruction, no data will be written, and the device will immediately accept a new command.

**FIGURE 6-11: PROTECTED EEPROM READ SEQUENCE**



**FIGURE 6-12: PROTECTED EEPROM UNLOCK AND PAGE WRITE SEQUENCE**



## 6.5 Preprogrammed EUI-48 or EUI-64 Node Address

The MCP795WX1 and MCP795WX2 are programmed at the factory with a globally unique node address stored in the protected EEPROM block.

### 6.5.1 EUI-48 NODE ADDRESS (MCP795WX1)

The 6-byte EUI-48™ node address value of the MCP795WX1 is stored in protected EEPROM locations 0x02 through 0x07, as shown in [Figure 6-13](#). The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining three bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

#### 6.5.1.1 Organizationally Unique Identifiers (OUIs)

Each OUI provides roughly 16M ( $2^{24}$ ) addresses. Once the address pool for an OUI is exhausted, Microchip will acquire a new OUI from IEEE to use for programming this model. For more information on past and current OUIs see “*Organizationally Unique Identifiers For Preprogrammed EUI-48 and EUI-64 Address Devices*” Technical Brief (DS90003187).

**Note:** The OUI will change as addresses are exhausted. Customers are not guaranteed to receive a specific OUI and should design their application to accept new OUIs as they are introduced.

### 6.5.1.2 EUI-64 Support Using the MCP795WX1

The preprogrammed EUI-48 node address of the MCP795WX1 can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFF between the OUI and the Extension Identifier, as shown below.

**Note:** As an alternative, the MCP795WX2 features an EUI-64 node address that can be used in EUI-64 applications directly without the need for encapsulation, thereby simplifying system software. See [Section 6.5.2 “EUI-64 Node Address \(MCP795WX2\)”](#) for details.

### 6.5.2 EUI-64 NODE ADDRESS (MCP795WX2)

The 8-byte EUI-64™ node address value of the MCP795WX2 is stored in array locations 0x00 through 0x07, as shown in [Figure 6-14](#). The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority.

The remaining five bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 64-bit value.

**Note:** In conformance with IEEE guidelines, Microchip will not use the values 0xFFFF and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values are specifically reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

**FIGURE 6-13: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (MCP795WX1)**

|               |                                           |     |     |                             |     |     |
|---------------|-------------------------------------------|-----|-----|-----------------------------|-----|-----|
| Description   | 24-bit Organizationally Unique Identifier |     |     | 24-bit Extension Identifier |     |     |
|               | 00h                                       | 04h | A3h | 12h                         | 34h | 56h |
| Data          |                                           |     |     |                             |     |     |
| Array Address | 02h                                       |     |     | 07h                         |     |     |

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Corresponding EUI-64™ Node Address After Encapsulation: 00-04-A3-FF-FE-12-34-56

FIGURE 6-14: EUI-64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (MCP795WX2)

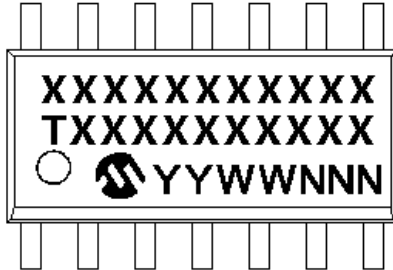
|                                                             |                                           |     |     |                             |     |     |     |     |
|-------------------------------------------------------------|-------------------------------------------|-----|-----|-----------------------------|-----|-----|-----|-----|
| Description                                                 | 24-bit Organizationally Unique Identifier |     |     | 40-bit Extension Identifier |     |     |     |     |
|                                                             | 00h                                       | 04h | A3h | 12h                         | 34h | 56h | 78h | 90h |
| Data                                                        |                                           |     |     |                             |     |     |     |     |
| Array Address                                               | 00h                                       |     |     | 07h                         |     |     |     |     |
| Corresponding EUI-64™ Node Address: 00-04-A3-12-34-56-78-90 |                                           |     |     |                             |     |     |     |     |

# MCP795W1X/MCP795W2X

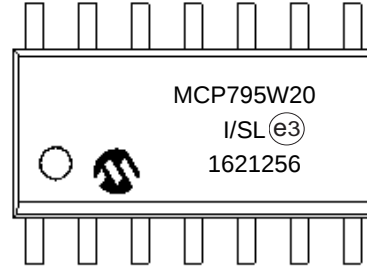
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

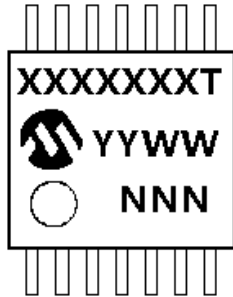
14-Lead SOIC (3.90 mm)



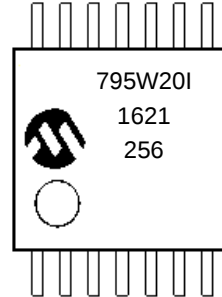
Example



14-Lead TSSOP



Example



| Part Number | 1st Line Marking Codes |         |
|-------------|------------------------|---------|
|             | SOIC                   | TSSOP   |
| MCP795W20   | MCP795W20              | 795W20T |
| MCP795W10   | MCP795W10              | 795W10T |
| MCP795W21   | MCP795W21              | 795W21T |
| MCP795W11   | MCP795W11              | 795W11T |
| MCP795W22   | MCP795W22              | 795W22T |
| MCP795W12   | MCP795W12              | 795W12T |

**Note:** T = Temperature grade

|                |        |                                                                                                               |
|----------------|--------|---------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X | Customer-specific information                                                                                 |
|                | Y      | Year code (last digit of calendar year)                                                                       |
|                | YY     | Year code (last 2 digits of calendar year)                                                                    |
|                | WW     | Week code (week of January 1 is week '01')                                                                    |
|                | NNN    | Alphanumeric traceability code                                                                                |
|                |        | JEDEC® designator for Matte Tin (Sn)                                                                          |
|                | *      | This package is RoHS compliant. The JEDEC designator () can be found on the outer packaging for this package. |

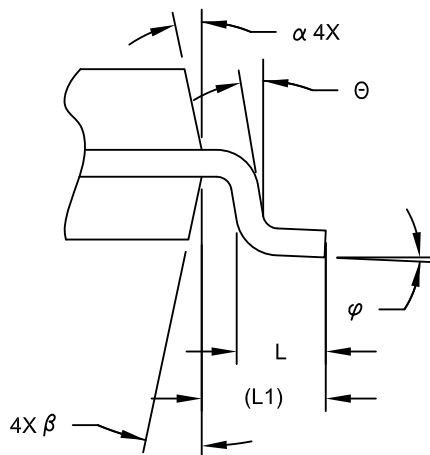
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.



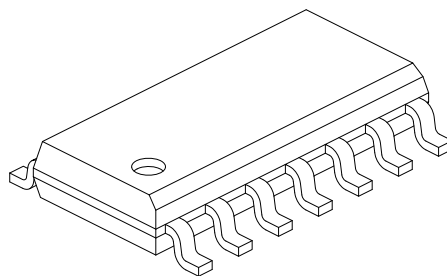
# MCP795W1X/MCP795W2X

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



VIEW C



|                          |    | Units | MILLIMETERS |     |      |
|--------------------------|----|-------|-------------|-----|------|
| Dimension Limits         |    |       | MIN         | NOM | MAX  |
| Number of Pins           | N  |       | 14          |     |      |
| Pitch                    | e  |       | 1.27 BSC    |     |      |
| Overall Height           | A  |       | -           | -   | 1.75 |
| Molded Package Thickness | A2 |       | 1.25        | -   | -    |
| Standoff §               | A1 |       | 0.10        | -   | 0.25 |
| Overall Width            | E  |       | 6.00 BSC    |     |      |
| Molded Package Width     | E1 |       | 3.90 BSC    |     |      |
| Overall Length           | D  |       | 8.65 BSC    |     |      |
| Chamfer (Optional)       | h  |       | 0.25        | -   | 0.50 |
| Foot Length              | L  |       | 0.40        | -   | 1.27 |
| Footprint                | L1 |       | 1.04 REF    |     |      |
| Lead Angle               | Θ  |       | 0°          | -   | -    |
| Foot Angle               | φ  |       | 0°          | -   | 8°   |
| Lead Thickness           | c  |       | 0.10        | -   | 0.25 |
| Lead Width               | b  |       | 0.31        | -   | 0.51 |
| Mold Draft Angle Top     | α  |       | 5°          | -   | 15°  |
| Mold Draft Angle Bottom  | β  |       | 5°          | -   | 15°  |

### Notes:

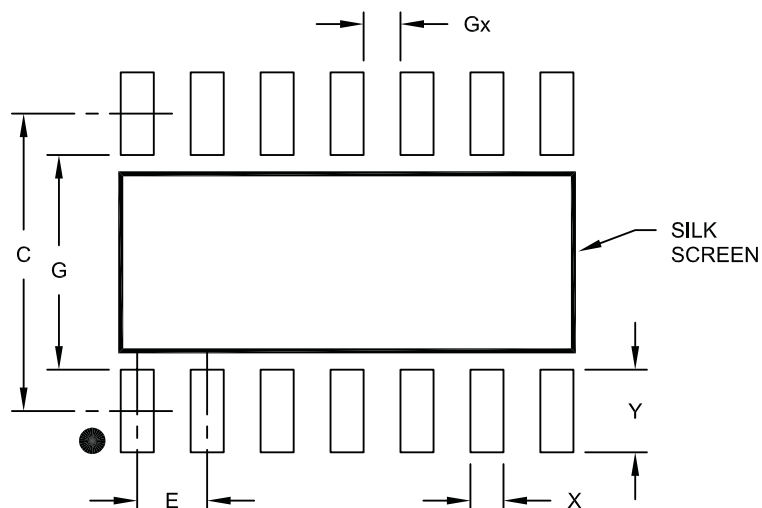
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
  - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

# MCP795W1X/MCP795W2X

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units                 |    | MILLIMETERS |      |      |
|-----------------------|----|-------------|------|------|
| Dimension Limits      |    | MIN         | NOM  | MAX  |
| Contact Pitch         | E  | 1.27 BSC    |      |      |
| Contact Pad Spacing   | C  |             | 5.40 |      |
| Contact Pad Width     | X  |             |      | 0.60 |
| Contact Pad Length    | Y  |             |      | 1.50 |
| Distance Between Pads | Gx | 0.67        |      |      |
| Distance Between Pads | G  | 3.90        |      |      |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

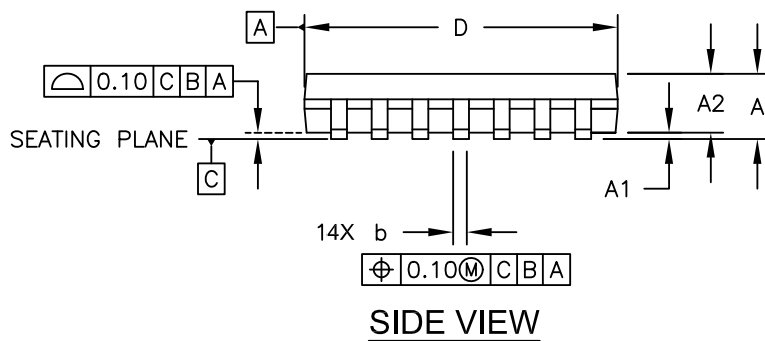
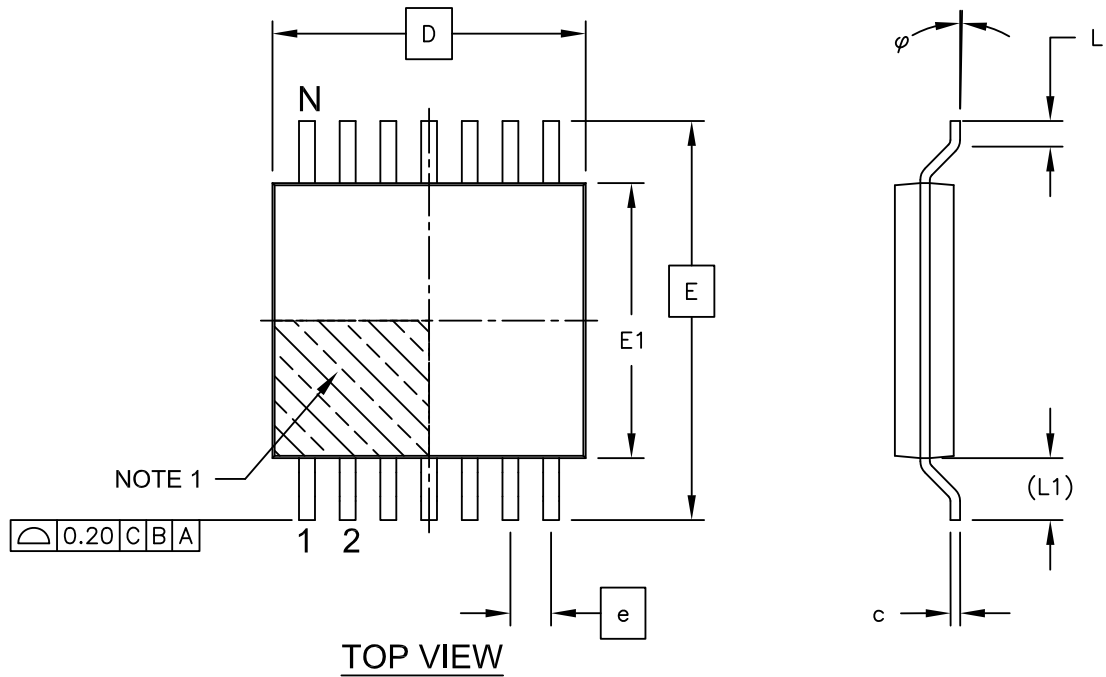
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

# MCP795W1X/MCP795W2X

## 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

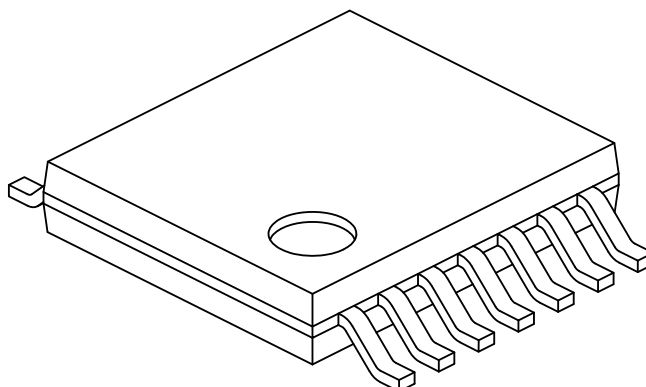


Microchip Technology Drawing C04-087C Sheet 1 of 2

# MCP795W1X/MCP795W2X

## 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                    |           | MILLIMETERS |      |      |
|--------------------------|-----------|-------------|------|------|
| Dimension Limits         |           | MIN         | NOM  | MAX  |
| Number of Pins           | N         | 14          |      |      |
| Pitch                    | e         | 0.65 BSC    |      |      |
| Overall Height           | A         | -           | -    | 1.20 |
| Molded Package Thickness | A2        | 0.80        | 1.00 | 1.05 |
| Standoff                 | A1        | 0.05        | -    | 0.15 |
| Overall Width            | E         | 6.40 BSC    |      |      |
| Molded Package Width     | E1        | 4.30        | 4.40 | 4.50 |
| Molded Package Length    | D         | 4.90        | 5.00 | 5.10 |
| Foot Length              | L         | 0.45        | 0.60 | 0.75 |
| Footprint                | (L1)      | 1.00 REF    |      |      |
| Foot Angle               | $\varphi$ | 0°          | -    | 8°   |
| Lead Thickness           | c         | 0.09        | -    | 0.20 |
| Lead Width               | b         | 0.19        | -    | 0.30 |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M

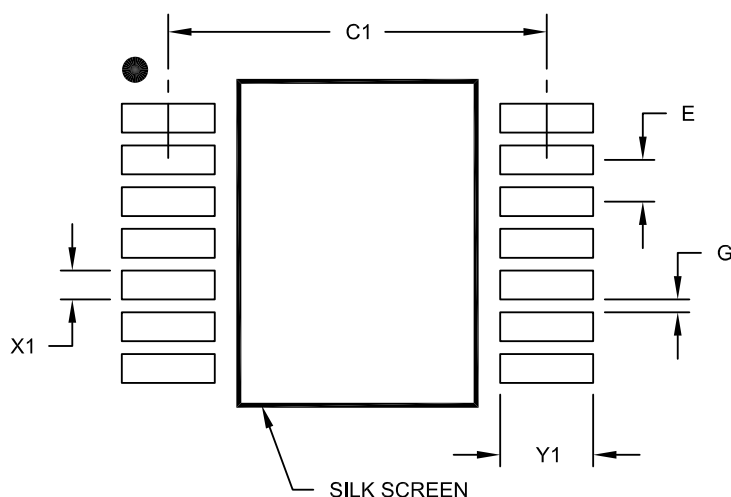
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

# MCP795W1X/MCP795W2X

## 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units                    |    | MILLIMETERS |      |      |
|--------------------------|----|-------------|------|------|
| Dimension Limits         |    | MIN         | NOM  | MAX  |
| Contact Pitch            | E  | 0.65 BSC    |      |      |
| Contact Pad Spacing      | C1 |             | 5.90 |      |
| Contact Pad Width (X14)  | X1 |             |      | 0.45 |
| Contact Pad Length (X14) | Y1 |             |      | 1.45 |
| Distance Between Pads    | G  | 0.20        |      |      |

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

# MCP795W1X/MCP795W2X

## APPENDIX A: REVISION HISTORY

### Revision A (11/2011)

Initial release of this document.

### Revision B (03/2012)

Added detailed descriptions for Registers.

### Revision C (06/2012)

Revised data sheet for 3V operation.

### Revision D (06/2016)

Removed preliminary status; Updated overall content for improved clarity; Added detailed descriptions of registers; Expanded descriptions of peripheral features; Updated block diagram and application schematic; Defined names for all bits and registers, and renamed the bits shown in [Table 1](#) for clarification; Renamed the DC characteristics shown in [Table 2](#) for clarification.

TABLE -1: BIT NAME CHANGES

| Old Bit Name | New Bit Name |
|--------------|--------------|
| CALSGN       | TRIMSIGN     |
| OSCON        | OSCRUN       |
| VBAT         | PWRFAIL      |
| LP           | LPYR         |
| SQWE         | SQWEN        |
| ALM0         | ALM0EN       |
| ALM1         | ALM1EN       |
| RS0          | SQWFS0       |
| RS1          | SQWFS1       |
| RS2          | CRSTRIM      |
| CALIBRATION  | TRIMVAL<7:0> |
| WDEL         | WDTDLLEN     |
| WDTPLS       | WDTPWS       |
| WD<3:0>      | WDTPS<3:0>   |
| EVEN0        | EVLEN        |
| EVEN1        | EVHEN        |
| EVWDT        | EVWDTEN      |
| EVLDB        | EVLPS        |
| EVHS<1:0>    | EVHCS<1:0>   |
| ALM0C<2:0>   | ALM0MSK<2:0> |
| ALM1C<2:0>   | ALM1MSK<2:0> |

TABLE -2: DC CHARACTERISTIC NAME CHANGES

| Old Name          | Old Symbol | New Name                                    | New Symbol |
|-------------------|------------|---------------------------------------------|------------|
| Operating Current | Icc Read   | EEPROM Operating Current                    | ICCEERD    |
|                   | IDD Write  |                                             | ICCEEWR    |
| VBAT Current      | IBAT       | Timekeeping Backup Current                  | IBATT      |
| Standby Current   | ICCS       | Vcc Data Retention Current (oscillator off) | ICCDAT     |

### Revision E (02/2018)

Added detailed description of OUIs.

NOTES:

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**Technical support is available through the website at: <http://microchip.com/support>**

NOTES:

# MCP795W1X/MCP795W2X

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office. Not every possible ordering combination is listed below.

| <u>PART NO.</u>                                                                            | <u>X</u>       | <u>X</u>         | <u>[X]<sup>(1)</sup></u> -                              | <u>X</u>    | <u>/XX</u> |
|--------------------------------------------------------------------------------------------|----------------|------------------|---------------------------------------------------------|-------------|------------|
| Device                                                                                     | EEPROM Density | Protected EEPROM | Tape & Reel Option                                      | Temp. Range | Package    |
| <b>Device:</b> MCP795W 1.8V - 3.6V SPI Serial RTCC with Watchdog Timer and Event Detection |                |                  |                                                         |             |            |
| <b>EEPROM Density:</b>                                                                     | 1              | =                | 1 Kbit EEPROM                                           |             |            |
|                                                                                            | 2              | =                | 2 Kbit EEPROM                                           |             |            |
| <b>Protected EEPROM:</b>                                                                   | 0              | =                | Blank                                                   |             |            |
|                                                                                            | 1              | =                | Preprogrammed EUI-48™ address                           |             |            |
|                                                                                            | 2              | =                | Preprogrammed EUI-64™ address                           |             |            |
| <b>Tape &amp; Reel Option:</b>                                                             | Blank          | =                | Tube                                                    |             |            |
|                                                                                            | T              | =                | Tape & Reel                                             |             |            |
| <b>Temperature Range:</b>                                                                  | I              | =                | -40°C to +85°C                                          |             |            |
| <b>Package:</b>                                                                            | SL             | =                | 14-Lead Plastic Small Outline (3.90 mm body)            |             |            |
|                                                                                            | ST             | =                | 14-Lead Plastic Thin Shrink Small Outline (4.4 mm body) |             |            |

**Examples:**  
a) MCP795W20-I/SL: 2 Kbit EEPROM, Industrial Temperature, SOIC Package.  
b) MCP795W10-I/ST: 1 Kbit EEPROM, Industrial Temperature, TSSOP Package.  
c) MCP795W21-I/SL: 2 Kbit EEPROM, Preprogrammed EUI-48™ address, Industrial Temperature, SOIC Package.  
d) MCP795W22-I/ST: 2 Kbit EEPROM, Preprogrammed EUI-64™ address, Industrial Temperature, TSSOP Package.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

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