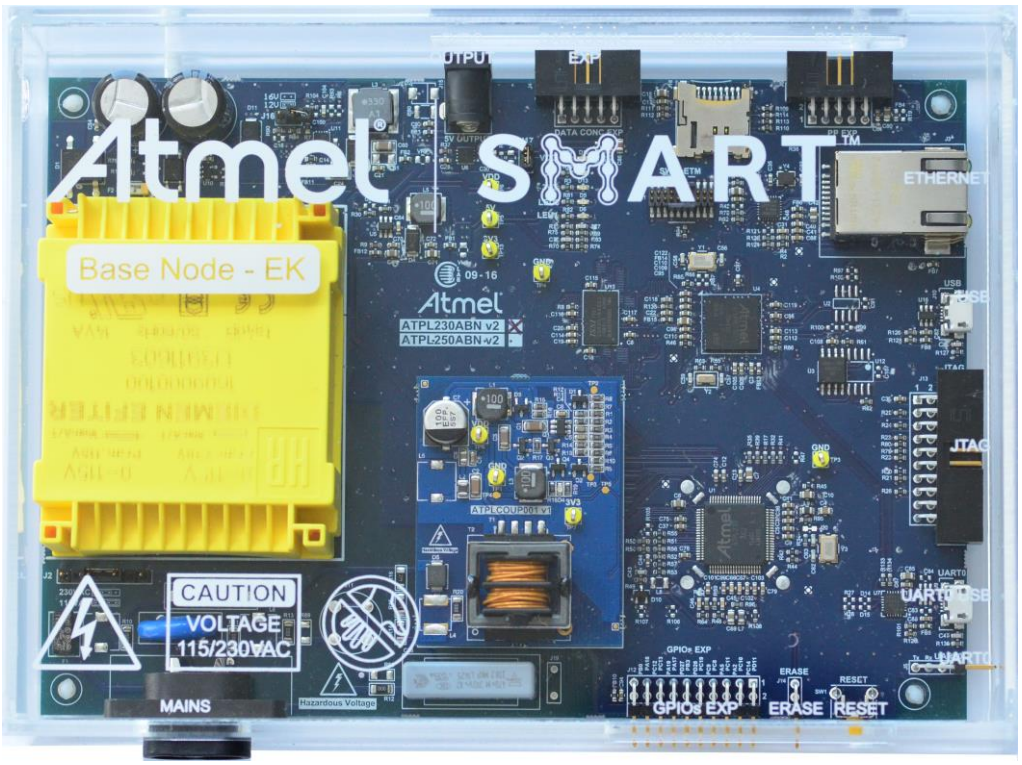
ATPL250A

PANCoordinator-EK Kit User Manual

USER GUIDE



Introduction

This PANCoordinator Evaluation Kit (EK) comprises all necessary resources to develop a complete G3-PLC PANCoordinator. It implements an Atmel® Cortex™-M7 device acting as MCU host, combined with ATPL250A modem for PLC (Power Line Communication). ATPL250A is a power line communications base band transceiver, compliant with the PHY layer of G3-PLC specification.

G3-PLC is a mature, consolidated and worldwide accepted standard for OFDM-based power line communications, with focus on providing Smart Grid services over electricity distribution networks.

This guide describes how to use the kit and get start with it.

Contents

- Welcome letter introducing the evaluation kit and its contents.
- Boards:
  - One ATPL250ABNv2 board.
  - One ATPLCOUP007v2.5 coupling board (CEN-A frequency band).
  - One ATPLCOUP002v2 coupling board (ARIB frequency band).
  - One ATPLCOUP006v2 coupling board (FCC frequency band).
- Cables:
  - One micro A/B-type USB cable.
  - One power cord cable IEC320-C8.
- Jumpers:
  - One voltage jumper with pitch 5.08 mm.
  - One erase jumper with pitch 2.54mm.

Features

- ATPL250A is a compact and high-efficient device for a wide range of Smart Grid applications such as Smart Metering (Smart Meters and Data Concentrators), Lighting, Industrial/Home Automation, Home and Building Energy Management Systems, Solar Energy and Plug-in Hybrid Electric Vehicle (PHEV) Charging Stations.
- ATPL250A G3-PLC device includes enhanced features such as additional robust modes and frequency band extension.
- ATPL250A has been conceived to be bundled with an external Atmel MCU. ATPL250ABN PAN Coordinator board mounts the ATPL250A transceiver and a SAME70 ARM Cortex M7 microcontroller. This development board provides a full featured platform to develop a complete communications system based on Power Line Communication technology, providing support for:
  - PLC band characterization.
  - Noise level measurement.
  - Sensitivity level measurement.
  - Maximum reachable distance.
  - Power consumption.
  - Check PLC performance in different bands (CENELEC, FCC, ARIB) setting different PLC coupling boards (provided with this evaluation kit).
  - The EK board can be supplied with universal 115-230 V_{AC} 50-60 Hz power input.
  - The EK boards include a JTAG interface for MCU debugging and programming purposes, a UART for debugging purposes, as well as Ethernet connectivity.

- Software application examples available based on G3-PLC Stack:
  - Atmel provides an Atmel G3-PLC PHY layer library which is used by the external MCU to take control of ATPL250A PHY layer device. Three G3-PLC PHY layer example projects are provided with the kit.
  - Atmel G3 Stack (ADP + MAC + PHY) for PAN Coordinator with some user applications is provided with the EK.

Table of Contents

Icon Key Identifiers

 TIP	Useful Tips and Techniques
 INFO	Delivers Contextual Information About a Specific Topic
 IMPORTANT	Note to Quality and Performance
 TO DO	Objectives to be Completed
 EXECUTE	Actions to be Executed Out of the Target
 RESULT	The Expected Result of an Assignment Step
 CAUTION	Procedure Which Can Result in Minor Equipment Damage
 WARNING	Procedure With Potential Equipment Damage
 DANGER	Procedure With Imminent Equipment Destruction

1. Evaluation Kit Specifications

1.1 Safety recommendations

These development boards must be only used by expert technicians. ATPL250ABN is directly powered from mains grid, so hazardous voltage (100/230V_{AC}) is present on the board. To avoid user access to dangerous parts, ATPL250ABN must always be used within its enclosure. All required connectors and configuration jumpers are easily accessible without electrical shock risk.

A normal use of ATPL250ABN does not require removing the enclosure cover. If this action is necessary, it must be performed by qualified staff after being sure that mains connection has been previously removed. Be careful it is only for indoor use.

This development board does not have any switch on mains connection to switch on or off it. It must always be connected to an easy accessible mains socket.

Do not connect any probe to high voltage sections if the board is not isolated from the mains supply to avoid damaging of measurement instruments.

Coupling boards' kits are shipped in a protective anti-static package. The boards system must not be subjected to high electrostatic discharge.

We strongly recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example) without enclosure. Avoid touching the component pins or any other metallic element on the board.

ATPL250ABN is a CE mark product which passes EN60950-1 safety standard, EN50065-1, EN50065-2-3, EN50065-7 EMC and FCC (as current carrier system) standards. It also satisfies Pb-Free and ROHS directive.

ATMEL does not assume responsibility for the consequences arising from any improper use of this board.

Boards' kits are intended for further engineering, development, demonstration, or evaluation purposes only. It is not a finished product except as may be otherwise noted on the board/kit.

1.2 Electrical characteristics

This section shows the electrical characteristics of the kit's boards. See the following tables:

Table 1-1. Power Supply Requirements.

Parameter	Condition	Min.	Typ.	Max.	Unit
AC mains Voltage Range		100	115/230	250	V_{AC}
Mains Frequency			50/60		Hz
Maximum Input Current				200(1)	mA
Isolation Voltage	ACDC power supply and PLC coupling transformer			3000	V_{AC}

Note that the ATPL250ABN can be supplied either with $100V_{AC}$ or $230V_{AC}$ by setting the proper jumpers (pitch = 5.08mm) in the voltage selector, J2, as depicted in the Figure 7-10. By default, voltage jumper is set for $230V_{AC}$. For more information about power supply, see section 3.5.1.

Note: 1. This maximum input current is measured in the worst case situation, so that, when board is supplied with a minimum input voltage,$100V_{AC}$, and the worst consumption conditions. That is when it emits against very low impedance in higher frequency band and it is supplying an extra board through the DC jack J15.

Table 1-2. Power Supply Requirements.

Parameter	Condition	Min.	Typ.	Max.	Unit
TX Power Consumption	FW: PHY TX Test Console Application Low Impedance Load (PRIME LISN). Measured on V_{DD} (16V) DCDC output.		3523(1)		mW
	FW: PHY TX Test Console Application High Impedance Load (CISPR LISN). Measured on V_{DD} (16V) DCDC output.		2280(1)		mW
RX Power Consumption	Measured on 3.3V LDO output		664(1)		mW

Note: 1. These measurements were taken with a non-optimized FW (the PHY TX Test Console project included in the kit with a default configuration in TX mode and RX mode) from a power consumption point of view and they highly depend on the architecture and efficiency of the power supplies. These measurements correspond to the whole PCBA design and not only to ATPL250A and ATSAME70 devices. All PCB peripherals are supplied, i.e. ATPLCOUP007 coupling board emitting in CENELEC-A band. Refer to Atmel ATPL250A and ATSAME70 datasheets for an optimized power consumption measurement result.

2. Evaluation Kit Overview

ATPL250ABN is the name of the development board included in this PAN Coordinator EK. It implements an ATPL250A analog front end for PLC, supporting G3-PLC, which has been designed to be controlled by an external Atmel MCU. In this case, Atmel | Smart SAME70 is the device driving ATPL250A PLC analog front end.

This document describes how to start working with the Atmel PANCoordinator-EK. A complete description of PC tools, software examples and hardware are provided in this EK.

2.1 Design support

To make it faster and easier for you to evaluate, prototype, develop and program with Atmel products, we offer a variety of design resources, including development tools, software, boards, kits and documentation.

For any technical support request, please refer to our Design Support webpage: http://www.atmel.com/design-support/.

There any user can search the Atmel knowledge base to find tips, help topics, and answers to common questions. In case that the obtained information is not helpful any user can *Open a Support Case* indicating a description of the case, product information, etc.

2.2 PANCoordinator-EK contents

PANCoordinator-EK contents –documentation, software and tools- are available online in https://secure.atmel.com/. To download this information you need a *myAtmel* account, please access to www.atmel.com/myAtmel and create your own account After that, please contact with plc@atmel.com, specifying your myAtmel user name, your company name and email, and request access to the specific evaluation kit you have acquired. **Please do not hesitate to visit our web site to get the last kit updates**.

myAtmel EK contents are:

1. A welcome letter, *PANCoordinator-EK_WL*, introducing the EK and its contents.
2. PANCoordinator-EK Kit User Manual, *doc43106*.
3. *Hardware* folder:
    a. ATPL250A datasheet, *doc43079*.
    b. Hardware application notes: PLC coupling reference designs, crystal selection guidelines, layout recommendations, critical design guidelines, etc.
    c. EK schemes, PCB layouts, gerbers and BOM files of ATPL250ABN, ATPLCOUP002, ATPLCOUP006 and ATPLCOUP007 boards.
4. *Software* folder:
    a. *G3_va.b.c* folder, contains five projects for several IDE tools, IAR, Atmel Studio and Keil µVision to work in both frequency bands, CENELEC-A, ARIB and FCC bands, see *g3.workspace.same70q21_atpl250abn_v2.zip* file:
        - *Apps_Phy_Tester_Tool*. This application configures G3-PLC PHY layer and its serial interface to communicate with Atmel PLC PHY Tester Tool to send and receive PLC messages from/to the PLC line and check the PLC transmission/reception processes between ATPL250ABN boards. Atmel PLC PHY Tester tool for PC is available in the *PCTools* folder.
        - *Apps_Phy_Tx_Test_Console*. This application lets the user to configure a proper set up to perform both EMC emissions and immunity tests on ATPL250ABN board. These tests are based on the use of G3 PHY layer with a terminal console firmware that eases the configuration of several transmission parameters such as modulation, frame data length and time interval between frames.

- *Apps_Phy_Sniffer_Tool*. This application configures G3 PHY layer to monitor the PLC data traffic on ATPL250ABN board and sends via serial communication this traffic to the ATPL Multiprotocol Sniffer tool. This tool can be downloaded from the *PCTools* folder. Every coupling board is intended to be used in their corresponding frequency bands only. By default, sniffer project is compiled for ATPLCOUP007 board. This means that only G3 CENELEC band-A is supported.
- *APPS_DLMS_EMU_COORD_APP*. The DLMS Emulator application is an example using the Atmel G3-PLC stack and show how the G3 API should be used. This application is provided for Coordinator. Application configure the ATPL250ABN board as G3 Coordinator. A Device node is required, it is configured with DLMS Emulation capabilities and simulate the data exchange between the G3 Coordinator and the Device(s). The Device responds dummy DLMS messages after receiving data requests from the Coordinator.
- *APPS_ADP_MAC_SERIALIZED_APP*. The ADP and MAC serialization is an application example that bring you access to the ADP, MAC and Bootstrap API through a serial connection. This application could be useful for users that want to make intensive test for the stack or want to run the upper layers in other CPU.

b. Common software documentation folder. It contains some user guides as the description of the Atmel G3 firmware stack, doc43081. Document describes in detail all layers from the Atmel G3 implementation as well as configuration options provided, target platforms, default architecture and the provided solutions by Atmel.

c. Evaluation License Agreement document.

5. *PCTools* folder:

a. Atmel PLC PHY Tester, PC tool used to monitor point to point PLC transmissions between Atmel boards.

b. ATPL Multiprotocol Sniffer, PC tool to monitor data traffic in G3-PLC networks using an Atmel board as sniffer.

c. SAM-ICE™ Drivers. Users may need to install this driver the first time the SAM-ICE is connected to the PC.

d. USB Drivers (Silicon USB drivers). Users may need to install these drivers the first time the ATPL250ABN board is connected to the host PC by means of a serial USB connection.

We recommend installing the evaluation kit contents in the root C:\ to avoid problems with very long paths.

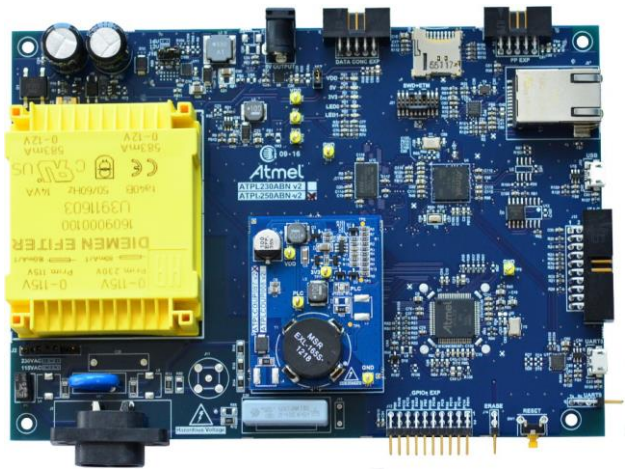
Unpack and inspect the kit carefully. Contact your local Atmel distributor, should you have any issues concerning the contents of the kit.

The ATPL250ABN board with the ATPLCOUP007 are encapsulated with methacrylate enclosures and shipped in protective anti-static foam. The two coupling boards, ATPLCOUP002 and ATPLCOUP006, are shipped in shielded bags.

The boards must not be subject to high electrostatic discharge. We recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments. Avoid touching the components pins or any other metallic elements on the board.

Figure 2-1. Packed Atmel PANCoordinator-EK.

Figure 2-2. ATPL250ABN PAN Coordinator board and with ATPLCOUP007.



ATPL250ABN board is provided with an example application preprogrammed, the G3-PLC PHY Tester project for SAM4E70Q21. After installing the Atmel PLC PHY Tester PC Tool in your PC, users can interface with the device and start exploring its capabilities, for example, checking the point to point PLC transmissions between the two Atmel boards. Please refer to chapter 7.2 for further information.

Take into account that the PANCoordinator-EK provides one coupling board for CENELEC-A band, Figure 2-3, set over the ATPL250ABN board. In addition to the ATPLCOUP007 board, evaluation kit adds one coupling boards for FCC bands, Figure 2-4. And another coupling board for ARIB bands, Figure 2-5.

Depending on the coupling board set in ATPL250ABN board and the PHY configuration parameters selected in the software project you will send and receive PLC messages in the proper PLC band. So that, with ATPLCOUP007 board only lets you send and receive PLC messages in CENELEC-A band. And with ATPLCOUP002 and ATPLCOUP006 board in ARIB or FCC bands respectively.

Figure 2-3. ATPLCOUP007 Coupling board.

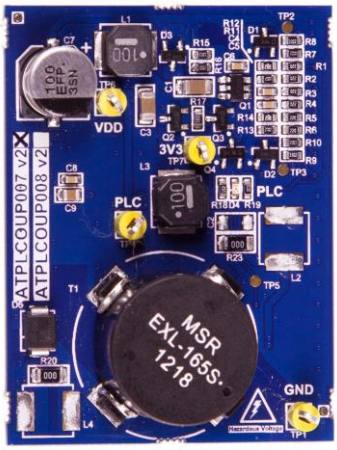
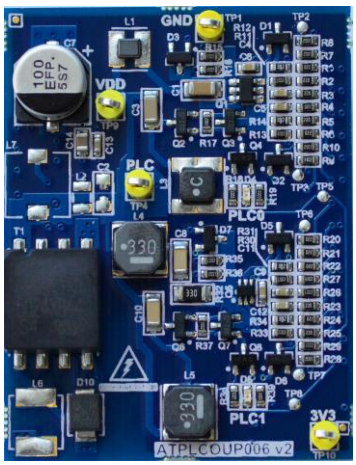


Figure 2-4. ATPLCOUP002 Coupling board.

Figure 2-5. ATPLCOUP006 Coupling board.



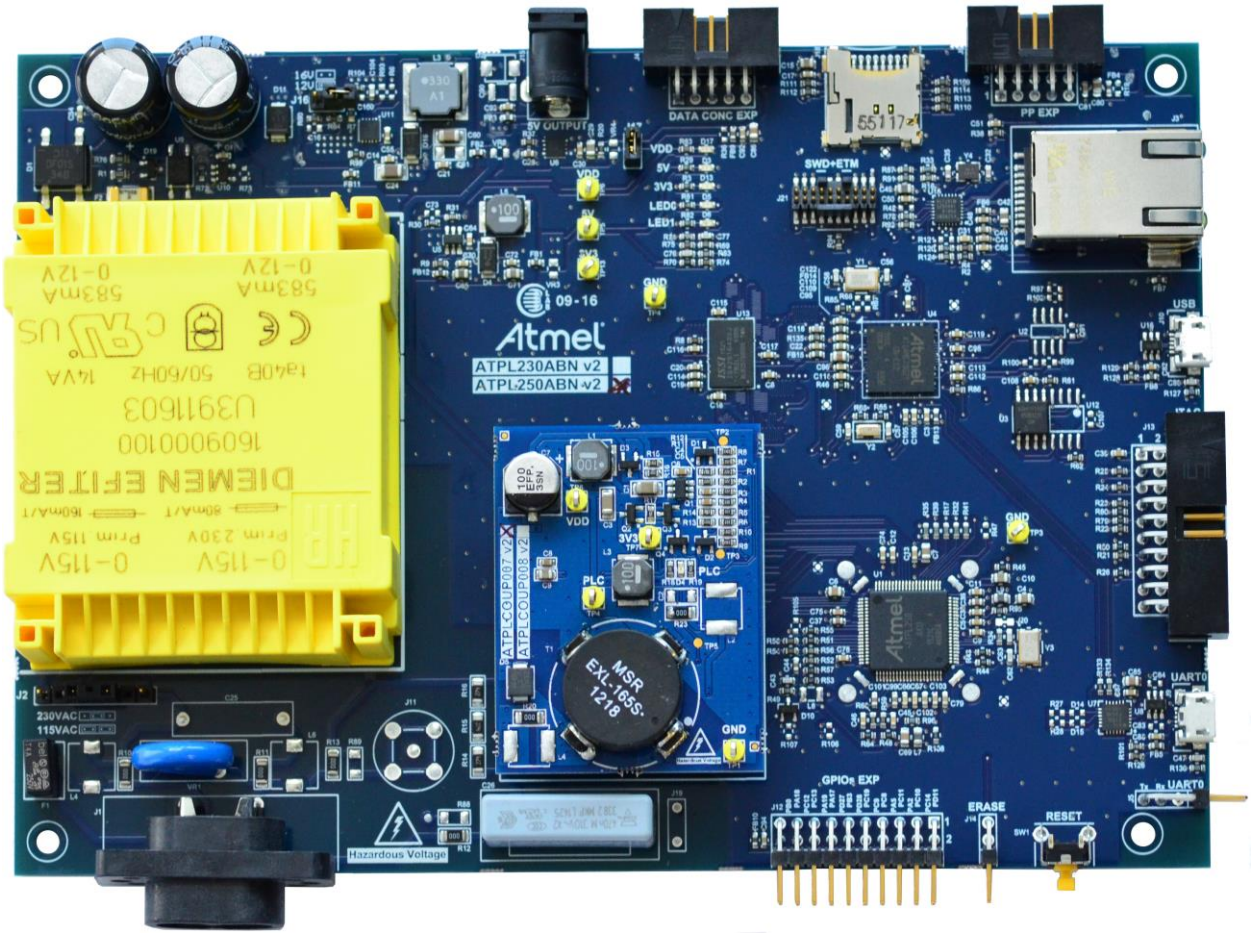
3. ATPL250ABN Hardware

3.1 Overview

This section summarizes the Atmel ATPL250ABN board design. It introduces system-level concepts, such as power supply, MCU, PLC coupling, memories, peripherals and interface board.

ATPL250ABN is a PAN Coordinator development board based on the ATPL250A, G3-PLC transceiver, and on the SAME70 ARM Cortex M7 microcontroller. ATPL250ABN PAN Coordinator board provides a platform to develop a complete communications system over G3-PLC technology.

Figure 3-1. ATPL250ABNv2 PAN Coordinator board.



3.2 Features

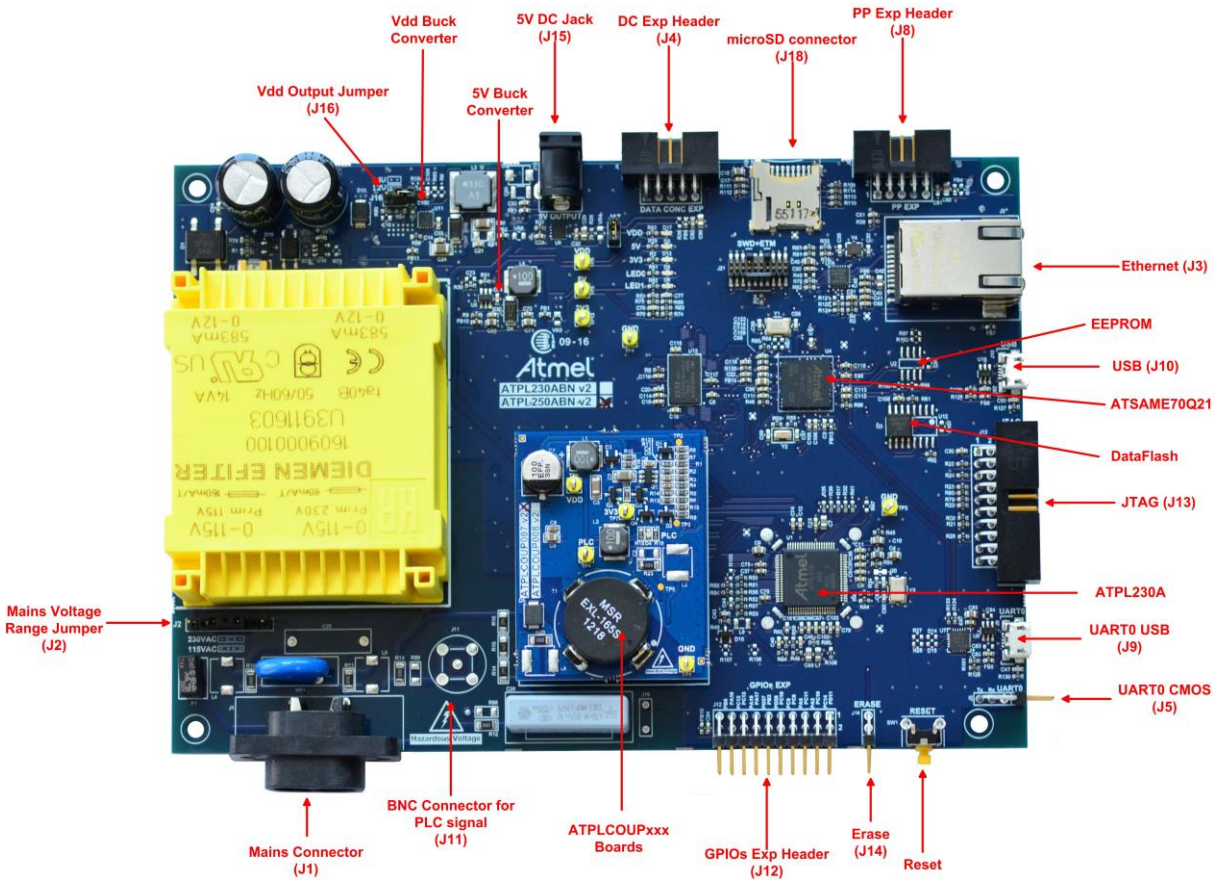
The ATPL250ABNv2 board includes the following features:

- Power supply:
  - Non switched ACDC isolated power supply: 100-230V_{AC}, 50-60Hz.
  - 5 volts rail is accessible by means of a DC Jack connector (J15).
  - Selectable 12/16 V_{DD} power supply.
- ATPL250A G3-PLC Transceiver:
  - Implements G3 CENELEC-A, FCC and ARIB profiles (ITU-T G.9903, June 2014).
  - Power Line Carrier modem for 50 and 60 Hz mains.

  - G3-PLC coherent and continuous amplitude tracking in signal reception.
  - Automatic Gain Control (AGC).
  - Zero cross detection.
  - Embedded PLC Analog Front End (AFE), requires only external discrete high efficient Class D Line Driver for signal injection.
- Support to G3-PLC coupling boards ATPLCOUP*xxx.*
- Mains zero-crossing detector circuit.
- SAME70Q21 MCU ARM Cortex-M7:
  - Core
    - ARM Cortex-M7 at up to 300 MHz.
    - 16 Kbytes of ICache and 16 Kbytes of DCache with Error Code Correction (ECC).
    - Memory Protection Unit (MPU) with 16 zones.
    - Simple- and double-precision HW Floating Point Unit (FPU).
    - DSP Instructions, Thumb®-2 Instruction Set.
    - Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU).
  - Memories
    - 2048 Kbytes Embedded Flash.
    - 384 Kbytes Embedded SRAM.
    - Tightly Coupled Memory (TCM) interface with four configurations (disabled, 2 x 32 Kbytes, 2 x 64 Kbytes, and 2 x 128 Kbytes).
    - 16 Kbytes ROM with embedded Boot Loader routines (UART0, USB) and IAP routines.
    - 16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, NOR and NAND Flash.
    - 16-bit SDRAM Controller.
  - Cryptography
    - True Random Number Generator (TRNG).
    - AES: 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications.
    - Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.
- External Memories:
  - 4Mx16-bit SDRAM.
  - 32-Mbit SPI Data Flash.
  - TWI EEPROM (do not populate).
  - microSD card connector.
- Peripherals:
  - MCU 24 MHz crystal oscillator.
  - MCU 32.768 kHz crystal oscillator.
  - V_{DD} and 5V Voltage monitor.
  - Reset button.
  - User's LEDs.
  - Chip erase.
- Interface:
  - JTAG debugging port.
  - Embedded Trace Module (ETM).

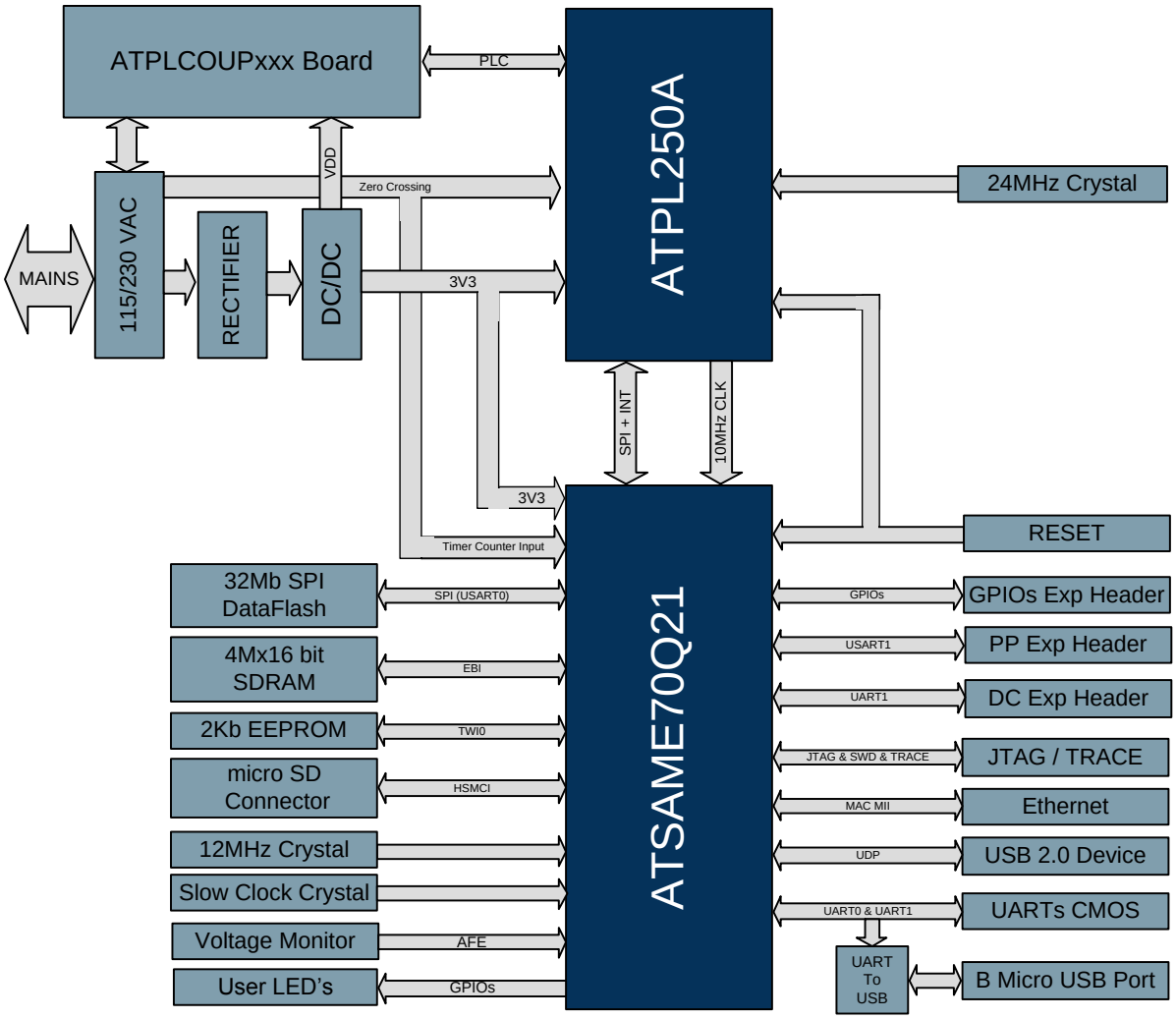
- High Speed USB 2.0 Device.
- Xplained PRO Master/Slave Interface.
- UARTs over USB and CMOS levels.
- Ethernet 10/100 Mbps.
- Poly-phase Base Node extension header.
- Data Concentrator extension header.
- GPIOs extension header.

Figure 3-2. ATPL250ABNv2 PAN Coordinator board overview.



3.3 Block diagram

Figure 3-3. ATPL250ABNv2 Block diagram.



3.4 Mechanical and user considerations

This development board is directly powered from mains grid, so hazardous voltage is present on the board. To avoid user access to dangerous parts, ATPL250ABN must always be used in its enclosure. All required connectors and configuration jumpers are easily accessible without removing the enclosure cover.

A normal use of the ATPL250ABN does not require removing the enclosure cover. If this action is necessary, it must be performed by qualified staff being sure that mains connection has been previously removed.

ATPL250ABN is a CE mark product which passes EN60950-1 safety standard and EN50065-1, EN50065-2-3, EN50065-7 EMC and FCC (as current carrier system) standards. It also satisfies Pb-Free and ROHS directive.

ATPL250ABN supply voltage is taken from mains grid (100/230V_{AC}, 50-60Hz), J1 connector.

ATPL250ABN dimensions are 178mm x 124mm x 30mm (LxWxH) and the enclosure dimensions are 191mm x 140mm x 48mm (LxWxH).

The operating temperature range is about -10 to 85ºC.

3.5 Hardware description

In this section the modules of the ATPL250ABNv2 board are described. Take into account that the board's BOM; is not a final design, so they include devices that could be no necessary in the customer designs once the design has been optimized.

Hardware files are contained in the Hardware folder: ".\Hardware\HW_SCH&PCB\ATPL250ABNv2".

3.5.1 Power supply

ATPL250ABN board can be powered either with $100V_{AC}$ or $230V_{AC}$ by setting the proper jumpers in the voltage selector (J2, Figure A-2). J1 IEC-320-C8 connector allows cable connection to mains grid. This design uses an encapsulated transformer (T1, Figure A-2) plus a full bridge rectifier (D1, Figure A-2) to obtain a DC voltage without increasing noise in PLC frequency bands (42 to 472 kHz), as may occur with switched ACDC power supplies. F1 and VR1 are used as protective devices in the equipment input and F2 protects the transformer output against over current situations.

By default, the voltage jumpers' configuration is for $230V_{AC}$. See Figure 7-10.

The maximum transformer output power of 14VA is oversized compared to the maximum current consumption of ATPL250ABN when it is used as a G3-PLC PAN Coordinator. However, this design is intended to power up other development kits which may have considerable power consumption if they include components such TFT displays.

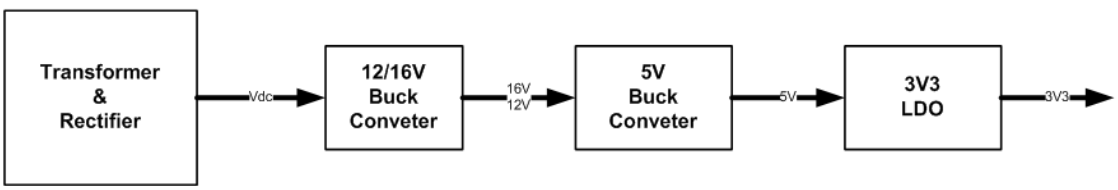
The "V_{DC}" voltage rail is used as input power of a high switching frequency buck converter (U11, Figure A-2) to generate the regulated DC voltage "V_{DD}", which is used to power the class D amplifier of the PLC coupling circuit. The output level of the buck converter is selectable between 12V and 16V by means of jumper J16. Refer to the application note "PLC Coupling Reference Designs" doc43052 to know how the jumper J16 must be configured depending on the PLC coupling board which is being used.

A second buck converter (U12, Figure A-2) also with switching frequency above the highest PLC frequency band is used to generate a regulated 5V voltage rail. Despite 5V is not used by any device on ATPL250ABN board, it may be useful to power other Atmel evaluation kits to form more complex PLC reference designs, such as data concentrators. The DC Jack connector J15 (J15, Figure A-10) can be used to connect other board to 5V.

Finally on the power supply chain scheme, a low dropout (LDO) regulator (U13, Figure A-2) is used to generate the 3V3 voltage rail required by ATPL250A and the MCU. The current consumption from 3V3 voltage rail can be measured connecting an ammeter in the placeholder of jumper J17.

Other 1.2V voltage levels are generated by the embedded LDOs on ATPL250A and ATSAME70Q21 respectively. For a more detailed information about these LDOs, refer to ATPL250A and ATSAME70Q21 datasheets.

Figure 3-4. Power supply diagram.



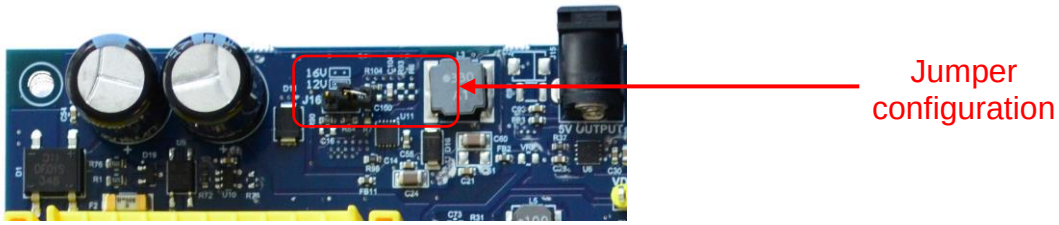
Switching frequency of DCDC buck converters used in this evaluation kit has been chosen to be higher than maximum PLC frequency band supported by ATPL250A device.

We recommend characterizing the potential impact of the selected SMPS for customer designs on the G3-PLC frequency band transmission.

V_{DD} could be two different voltages, 16 volts or 12 volts, depending on the jumper position. If the jumper is not placed, the voltage V_{DD} is 16 volts. If the jumper is placed in J16, V_{DD} is 12 volts. By default, the board has a jumper, so board provides 12 volts. These different voltages are used to supply the PLC coupling driver board.

Be careful with the V_{DD} voltage selected, because the PLC coupling driver board ATPLCOUP*XXX* could be damaged. Please check the features of these boards to select the operation voltage.

Figure 3-5. V_{DD} selection in ATPL250ABN board.



The following test points and LEDs allow to check that these power supplies are operating properly (see Figure A-2):

- V_{DD}: TP6 and green LED D17.
- 5V: TP5 and green LED D3.
- 3V3: TP13 and green LED D13.
- GND: TP3 & TP4.

3.5.2 Zero crossing detector

Phase identification is an important feature of devices that are connected to a smart grid network, such as smart meters. A typical implementation is based on measuring the time difference between a specific PLC frame reception and the last zero crossing event of the mains single-phase to which the device is connected.

Figure A-2 shows the zero crossing detection circuit, U10, used in ATPL250ABN board, which allows discerning between rising and falling edges of the mains voltage. The output signal of the detection circuit “VNR” is connected to a specific input of the ATPL250A and a synchronization algorithm is applied in order to obtain an accurate measurement of the time between PLC frame reception and zero crossing events.

The “VNR” signal is also connected to a timer counter input pin of the ATSAME70Q21 in order to have also information about zero crossing events on the microcontroller side.

It is important to note that in products that do not require galvanic isolation between primary and secondary circuits and the digital reference ground is connected to either line or neutral, a simple zenner diode with proper current limiting resistors, which considerably reduce the BOM cost, can be used instead of the circuit mounted in ATPL250ABN.

3.5.3 SAME70Q21 Flash microcontroller

3.5.3.1 SAME70Q21 Overview

The Atmel SAME70Q21 Flash microcontroller is based on the high-performance 32-bit ARM Cortex-M7 RISC processor and includes a floating point unit (FPU). It operates at a maximum speed of 300 MHz and

features 2048 Kbytes of Flash and 384 Kbytes of multiport SRAM, which guarantees a minimum access latency. The on-chip SRAM can be configured as Tightly Coupled Memory (TCM) or system memory.

The SAME70 offers a rich set of advanced connectivity peripherals including a 10/100 Mbps Ethernet MAC supporting IEEE 1588, 802.1Qbb, 802.3az, 802.1AS and 802.1Qav. With a simple- and double-precision HW FPU, advanced analog features, as well as a full set of timing and control functions, the SAME70 is the ideal solution for industrial automation, home and building control, machine-to-machine communications, automotive aftermarket and energy management applications.

Furthermore, the peripheral set of SAME70 includes a high-speed USB device port with embedded transceiver, a high-speed MCI for SDIO/SD/MMC, 16-bit SDRAM interface, 16-bit external bus interface featuring a static memory controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 12-bit ITU-R BT.601/656 Image Sensor Interface (ISI), hardware acceleration for AES256, three USARTs, five UARTs, three TWIs, three SPIs, as well as two 4-channel PWM, four three-channel 16-bit Timers with quadrature decoder logic support, one RTC, Analog Front End interfaces (12-bit ADC, DAC, MUX and PGA), one 12-bit DAC (2-ch) and an analog comparator.

3.5.3.2 SAME70Q21 Clocking

Besides the embedded RC oscillators of ATSAME70Q21, two crystal oscillators are assembled on ATPL250ABN board to obtain a more precise and stable system clock reference, Y1 of 12 MHz and Y2, (Figure A-3). Furthermore, a 24MHz clock signal generated by the PLC transceiver ATPL250A is used by default as clock input by configuring the high frequency oscillator of ATSAME70Q21 in bypass mode. This configuration allows reducing the overall BOM cost (12MHz crystal oscillator is not required) while keeping a stable clock input signal.

A slow clock crystal oscillator of 32.768 kHz (Y2, Figure A-3) is used as SAME70 can be used as calendar and time base counter.

3.5.4 ATPL250A PLC Transceiver

3.5.4.1 ATPL250A Overview

Atmel ATPL250A (U1, Figure A-7) is a power line communications modem, compliant with the PHY layer of G3-PLC specification. G3-PLC is an open standard technology used for Smart Grid applications like Smart Metering, Industrial Lighting and Automation, Home Automation, Street Lighting, Solar Energy and PHEV Charging Stations.

ATPL250A G3-PLC device includes enhanced features such as additional robust modes and frequency band extension. ATPL250A is able to operate in independently selectable transmission bands up to 472 kHz.

ATPL250A has been conceived to be bundled with an ATMEL MCU running the Physical Layer API and being controlled by means of a serial synchronous communication interface (SPI).

Please refer to ATPL250A datasheet on the Atmel website or in doc43079 for a detailed description.

3.5.4.2 ATPL250A Clocking

ATPL250A requires a 24MHz crystal oscillator (Y3, Figure A-7). And SAME70Q21 requires a 12 MHz crystal oscillator (Y1, Figure A-7).

The 24MHz clock signal could be used as internal reference time of the PLC modem, ATPL250A, and also to generate a 12MHz. So, it could be connected the output clock signal (CLKOUT) of ATPL250A like an input clock (CLKIN) of SAME70Q21 when ATPL250A is configured in bypass mode. In this way, only one high frequency crystal oscillator is required. For this option that is mounted by default in the board, R85 is soldered but R67 and R68 are not populated, and remember that ATPL250A must be configured properly.

Clocking item is widely detailed in the datasheet, doc43079.

3.5.5 PLC Coupling

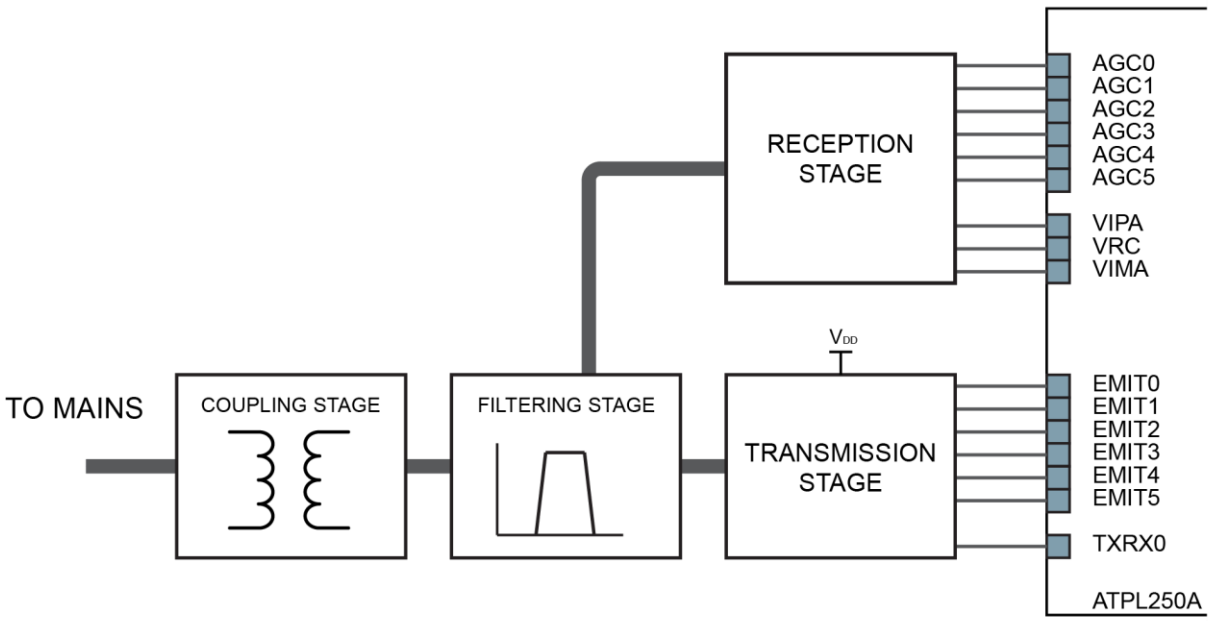
Atmel PLC technology is purely digital and does not require external DAC/ADC, thus simplifying the external required circuitry. Generally Atmel PLC coupling reference designs make use of few passive components plus a Class D amplification stage for transmission.

Figure A-8 and Figure A-9 show external components required by ATPL250A for PLC reception and transmission respectively.

PLC coupling reference design is composed by the same sub-circuits:

- Coupling Stage.
- Reception Stage.
- Transmission Stage.
- Filtering Stage.

Figure 3-6. PLC Coupling example.



3.5.5.1 Coupling stage

The coupling stage blocks the DC component of the line to/from which the signal is injected / received (i.e.: 50/60 Hz of the mains). This is carried out by a high voltage capacitor (C26, Figure A-8). Coupling stage could also voltage isolate the coupling circuitry from the external world by means of a 1:1 PLC transformer. Capacitor is laying out in ATPL250ABN. The optional PLC transformer is included in ATPLCOUP007 board (voltage isolated), see section 4.

Footprint of BNC connector (J11, Figure A-8) is included in the board, but is not mounted by default. Removing the R12 and R13 and soldering R88 and R89 resistors, the PLC coupling signal can be isolated from the mains grid and that connector allows performing measurements of transmitted and received PLC signal without side effects (noise) coming from the grid.

3.5.5.2 Reception stage

The reception stage adapts the received analog signal to be properly captured by the internal reception chain. Reception circuit is independent of the PLC frequency band which is being used. It basically consists on:

- Single-pole low pass filter (RC Filter), R49 & C43, Figure A-9.

- Automatic Gain Control (AGC) circuit. The AGC circuit avoids distortion (set of resistors used to attenuate the incoming PLC signal) on the received signal that may arise when the input signal is high enough to polarize the protective diodes in direct region (D10, Figure A-9).
- Driver of the internal ADC. The driver to the internal ADC comprises a couple of resistors (DC biasing resistors, R59 and R60) and a couple of capacitors (DC decoupling capacitors, C45 and C46). This driver provides a DC component and adapts the received signal to be properly converted by the internal reception chain.

3.5.5.3 Transmission stage

The transmission stage adapts the EMIT signals and amplifies them if required (Figure A-8). It can be composed by:

- Driver: A group of resistors which adapt the EMIT signals to either control the Class-D amplifier or to be filtered by the next stage.
- Amplifier: If required, a Class-D amplifier which generates a square waveform from 0 to V_{DD} is included.
- Bias and protection: A couple of resistors and a couple of Schottky barrier diodes provide a DC component and provide protection from received disturbances.

Transmission stage shall be always followed by a filtering stage.

3.5.5.4 Filtering stage

The filtering stage is composed by band-pass filters which have been designed to achieve high performance in field deployments complying at the same time with the proper normative and standards.

The in-band flat response filtering stage does not distort the injected signal, reduces spurious emission to the limits set by the corresponding regulation and blocks potential interferences from other transmission frequency bands.

The filtering stage has three aims:

- Band-pass filtering of high frequency components of the square waveform generated by the transmission stage.
- Adapt Input/Output impedances for optimal reception/transmissions. This is controlled by TXRX signals.
- And, in some cases, Band-pass filtering for received signals.

When the system is intended to be connected to a physical frequency band with high voltage or which is not electrically referenced to the same point then the filtering stage must be always followed by a coupling stage.

These components are not implemented on ATPL250ABN board because are dependent on the application parameters such frequency band transmission. A set of boards known as ATPLCOUP*xxx* have been design by to support multiple transmission options supported by ATPL250A. PANCoordinator-EK includes ATPLCOUP007, ATPLCOUP002 and ATPLCOUP006 boards which are described in chapters 4, 5 and 6 respectively. Other coupling boards have been designed. The Application Note, doc43052, provides a complete description of Atmel PLC Coupling Reference Designs available.

3.5.5.5 ATPLCOUP boards

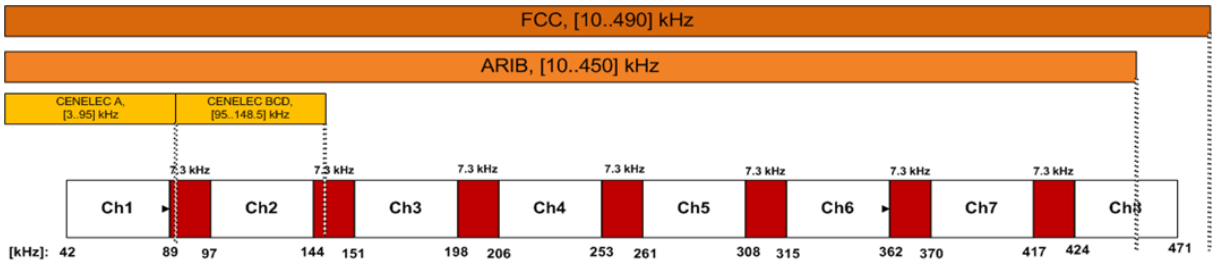
Table 3-1 summarizes the main characteristics of currently available PLC coupling reference designs. Please refer to Atmel doc43052 for a complete description of ATPLCOUP boards.

This technology only allows one frequency band active at a time.

Table 3-1. ATPLCOUP boards.

Board Name	Frequency Band	Branch	Electrical Isolation	CENELEC Band	ARIB	FCC
ATPLCOUP002	152-405 kHz	Double	Yes	-	X	-
ATPLCOUP006	152-489 kHz	Double	Yes	-	-	X
ATPLCOUP007	35-91 kHz	Single	Yes	A	-	-
ATPLCOUP008	35-91 kHz	Single	No	A	-	-

Figure 3-7. FCC & ARIB bands.



3.5.6 Peripherals

These peripherals are not necessary to implement a G3-PLC design, they are included to show some features of the ATPL250A for a customer designs.

3.5.6.1 SDRAM

The amount of data to be managed by a PAN Coordinator device typically exceeds the embedded SRAM density of ATSAME70Q21 (384kB). To overcome this limitation, an external SDRAM with 4Mx16-bit density is used in ATPL250ABN to support a big quantity of connected devices.

3.5.6.2 Data Flash

A 4MB SPI serial DataFlash is used to extend the non-volatile memory capability of ATSAME70Q21 (1MB).

Two different packages (U3 and U12, Figure A-4) are used in ATPL250ABN board to support the pinout of both the Adesto (former Atmel) family of DataFlash memories and standard serial flash products. Since both packages use the same chip select signal, only one device can be assembled simultaneously.

3.5.6.3 EEPROM

ATPL250ABN board includes the possibility to mount a serial EEPROM memory connected by Two Wires Interface, TWI, (U2, Figure A-4) with the SAME70. This device is not assembled by default. Please refer to AT24Cxx datasheet for a further description on Atmel's website.

3.5.6.4 microSD card connector

The high speed multimedia card interface (HSMCI) peripheral of ATSAME70Q21 supports the SD memory card specification V2.0. A microSD card connector with card detection switch is used in ATPL250ABN board. The card detection feature can be implemented by means of a GPIO with interrupt capability.

3.5.6.5 Voltage Monitor

Two ports (PB2 and PD30) of the ATSAME70Q21 analog front end module are used to monitor the V_{DD} and 5V voltage rails through external voltage divisors, as shown in Figure A-3.

The voltage monitor circuit allows the implementation of multiple applications such as:

- Detection of fault conditions.
- Detection of low power mode entering conditions.
- Detection of wake-up situations.
- Measuring of PLC power amplifier voltage value.

The selected ports for the voltage monitor circuit can also be used as input of the analog comparator in ATSAME70Q21.

3.5.6.6 Reset

Besides the reset conditions managed by the reset controller peripheral of the ATSAME70Q21, such as power-on-reset and brown-out monitor, two other reset sources are added at PCB level in ATPL250ABN:

- User controller reset switch button (SW1).
- The “NRST_CONC” signal on the data concentrator expansion connector, which allows resetting the base node reference design when it is used in data concentrator topologies.

The input/output “NRST” pin of ATSAME70Q21 is connected to the “PLL_INIT” input reset pin of the ATPL250A. Therefore, all reset conditions commented above, generate also a complete reset of the PLC transceiver. It is important to note that a reset event on “PLL_INIT” disables the “CLKOUT” output pin and, in case the ATSAME70Q21 is using this clock signal as the external clock input in bypass mode, a reset condition may lead to a loss of master clock on the microcontroller if a proper configuration is not applied by firmware. The firmware releases provided by Atmel for the base node reference design take this condition into account.

In addition to the complete reset of the PLC transceiver generated by an assertion of the “PLL_INIT” input, the “ARST” and “SRST” input reset signals allow also resetting the ATPL250A but in each of these cases without disabling the external clock on “CLKOUT” pin. Therefore, no special configurations have to be considered on the microcontroller side related to the clock system configuration. “ARST” and “SRST” are managed by the GPIOs PE1 and PE2 respectively in ATPL250ABN board.

3.5.6.7 Chip Erase

The 1x2 right angle pin-header J14 marked as “ERASE” (see Figure A-3) is connected to the SAME70 chip erase pin (PB12) and 3V3. This header can be used to erase the ATSAME70Q21 flash memory by placing a jumper on the header and pressing the reset switch button. After a while, the erase jumper should be removed and the PCBA must be turn off and turn on by disconnecting and connecting it again to the mains grid (flash erasing takes only 200ms).

3.5.6.8 User LEDs

The board incorporates two user LEDs (LED0 & LED1), green and red (D5 & D6, Figure A-3), connected to GPIOs PA21 and PA22 respectively of the SAME70Q21.

3.5.7 Interface Ports

3.5.7.1 ATSAME70Q21 JTAG/SWD Debug Port

The ATSAME70Q21 JTAG/SWD interface is available in a standard 20 pins male right angle header for debugging and programming purposes.

Please, refer to ATSAME70Q21 datasheet for a more detailed description of the debug port. It is important to note that JTAG is only available for boundary scan manufacturing test purposes.

3.5.7.2 Embedded Trace Module (ETM)

The Embedded Trace Macrocell (ETM) is a real-time trace module which delivers unrivalled instruction trace capture in an area far smaller than traditional trace units, enabling the SAME70 MCU to implement full instruction trace.

The ETM depends on the Trace Port Interface Unit (TPIU) to export data out of the system. The TPIU features the following pins:

- TRACECLK is the data stream synchronization signal
- TRACED0-TRACED3

ATPL250ABN implements a CoreSight™ 20, 20-pin, 50-mil keyed connector (pin seven is removed). Besides the TPIU signals, the CoreSight connector features also a Serial Wire Debug (SWD) interface.

Considering that the TPIU signals of the ATSAME70Q21 are multiplexed with the GMAC Ethernet RMII interface, it is not possible to use the ETM if the Ethernet port is enabled. Furthermore, if ETM is used, it is important to keep the Ethernet PHY IC in reset mode (GPIO PD31 must be asserted low) to avoid signal collisions.

3.5.7.3 High-speed USB Device 2.0

The ATPL250ABN has a micro-USB receptacle connected to the high-speed USB device 2.0 module of ATSAME70Q21. To be able to detect when a USB host is attached to ATPL250ABN board, a GPIO (PC17) is used to detect the VBUS voltage on the connector. The 5V voltage rail provided by the USB host is not used in ATPL250ABN rather than for detection purpose.

3.5.7.4 Debug UART

The UART0 of ATSAME70Q21 is connected to a CP2105 UART to USB 2.0 bridge to ease PC connectivity for debugging purposes. The firmware projects provided by Atmel to ease the evaluation of the G3 PHY-layer performance are based on serial interface through UART0.

As shown in Figure A-5, the UART to USB bridge CP2105 is powered from the 3.3V LDO on ATPL250ABN rather than from the 5V voltage rail of the USB connection. Therefore, ATPL250ABN board has to be connected to mains if the debugging UART is going to be used.

UART0 signals in CMOS levels are also available in the 3-pins right angle header J5.

3.5.7.5 Ethernet

The ATSAME70Q21 has a built in 10/100 Mbps Ethernet IEEE® 802.3 MAC with a RMII interface that connects to a Micrel KSZ8081RNA PHY-layer transceiver. The Ethernet input and output differential pairs of the PHY-layer transceiver are directly connected to a RJ45 Ethernet connector with embedded isolating signal transformers.

Refer to Figure A-6 for a complete view of the Ethernet PHY-layer transceiver design.

3.5.7.6 Poly-Phase Expansion Header

The 10-pin dual row male header J8 contains the USART transmission and reception signals of ATSAME70Q21 USART1 and two extra GPIOs. This expansion header is intended to cover poly-phase PLC base node reference designs in combination with other Atmel evaluation boards.

3.5.7.7 Data Concentrator Expansion Header

The 10-pin dual row male header J4 contains the UART transmission and reception signals of ATSAME70Q21 UART1 and two extra GPIOs. Furthermore, as commented in section 3.5.6.6, a reset input of ATPL250ABN board is available as well. This expansion header is intended to cover data concentrator reference designs in combination with other Atmel evaluation boards.

3.5.7.8 GPIOs Expansion Header

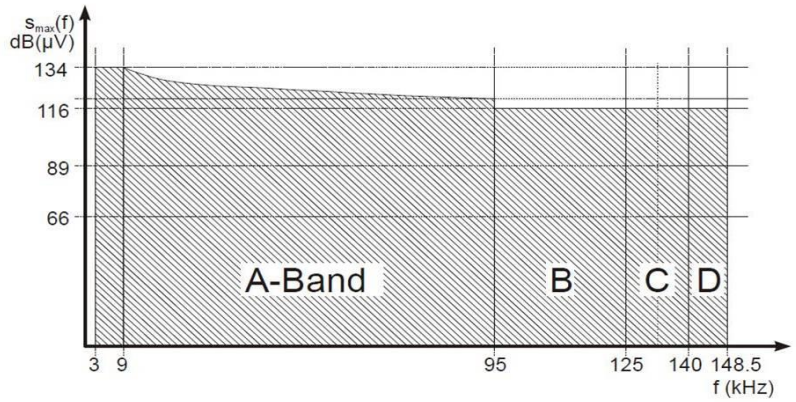
The 2.54mm pitch right-angle header J12 offers access to the I/O ports of the microcontroller that are not used within the ATPL250ABN board. Refer to ATSAME70Q21 datasheet for a description of the peripheral functionality available of each GPIO.

4. ATPLCOUP007 Hardware

4.1 Overview

ATPLCOUP007 is a PLC coupling board designed to communicate in CENELEC-A band, especially in G3-PLC band, from 35 to 91 kHz. ATPLCOUP007 mounts a single branch with voltage isolation from mains to the PLC coupling driver board. The goal of this design is provided to the customers with a cost optimized performance transmission board in CENELEC-A band for G3-PLC. This board is set by default in the ATPL250ABN board of the PANCoordinator-EK.

Figure 4-1. CENELEC bands.

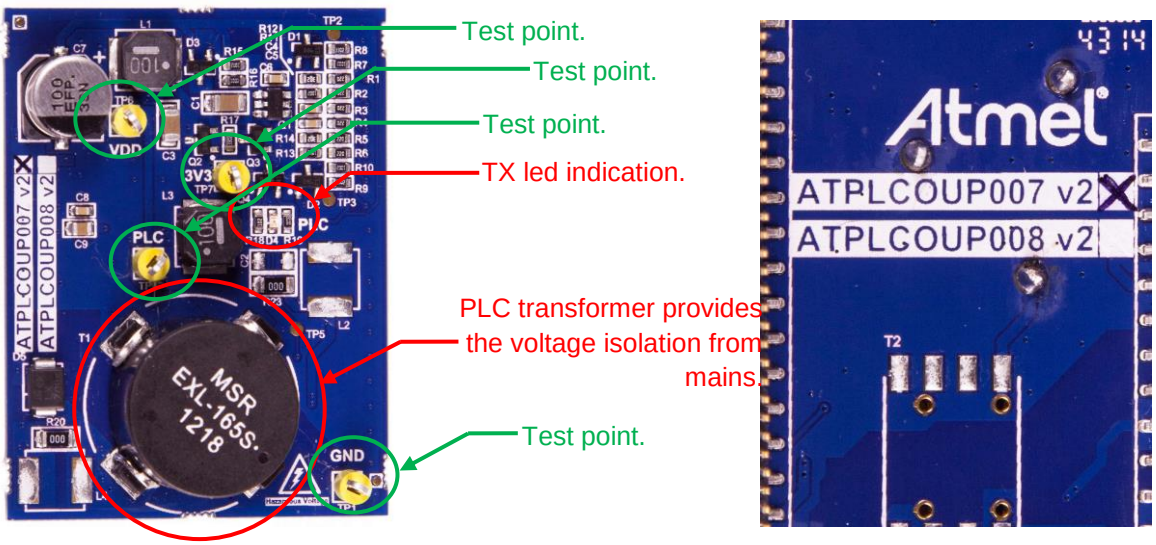


4.2 Features

The ATPLCOUP007v2.5 board includes the following features:

- Specially designed to communicate in CENELEC-A frequency band (35 – 91 kHz).
- Voltage Isolation from mains with a transformer, *MSR EXL-165S-LT*, soldered in top layer board.
- Single branch:
  - Low impedance optimized.

Figure 4-2. ATPLCOUP007v2.5 PLC Coupling board (top view).



4.3 Mechanical and user considerations

ATPLCOUP007 is delivered with the PANCoordinator-EK. Board-to-board SMD connectors, J1 and J2, are used to connect the ATPLCOUP007 into connectors J6 and J7 of ATPL250ABN board (Figure A-8). These J1 and J2 connectors are in bottom layer of ATPLCOUP007 and they have the following part numbers:

- J1: SAMTEC FTR-130-54-L-S.
- J2: SAMTEC FTR-124-54-L-S.

The ATPLCOUP007 board is directly powered from mains grid, so hazardous voltage is present on the board. To avoid user access to dangerous parts, ATPLCOUP007 must always be used in its enclosure.

ATPLCOUP007 is a CE mark product that passes EN 50065-1, EN 50065-2-3 and EN 50065-7 EMC standards. It also satisfies Pb-Free and ROHS directive.

ATPLCOUP007 dimensions are 51.5mm x 39.5mm x 18mm (LxWxH).

The operating temperature range is about -40 to 85ºC.

4.4 Hardware description

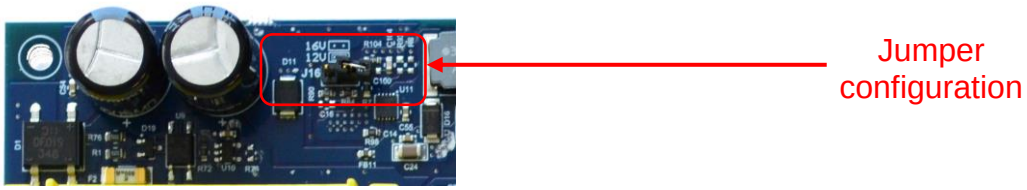
Hardware files are contained in the Hardware folder: *".\Hardware\HW_SCH&PCB\ATPLCOUP007v2.5"*.

ATPLCOUP007 is an isolated reference design which provides a full performance PLC coupling reference design in terms of output signal level over a wide range of load impedance values while complying with EN50065-1, EN50065-2-3 and EN50065-7 normative. It supports the frequency band between 35 and 91 kHz of CENELEC-A band.

ATPLCOUP007 is composed of only one transmission branch (single branch) which filtering stage has a flat band pass response with typical field impedances. It involves a cost optimization in the BOM. For more information, see PLC coupling reference designs document, doc43052.

Take into account that, when ATPLCOUP007 is connected to ATPL250ABN, V_{DD} voltage must be **12 volts** to avoid damaging the coupling board, so jumper in J16 must be **set** (see section 3.5.1 and Figure A-2). By default, the jumper is placed in J16.

Figure 4-3. V_{DD} selection in ATPL250ABN board.

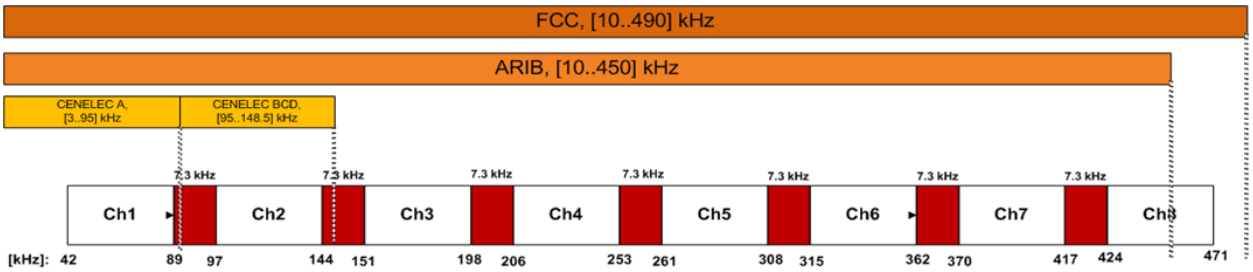


5. ATPLCOUP002 Hardware

5.1 Overview

ATPLCOUP002 is a PLC coupling board designed to communicate in ARIB and FCC bands, especially in bands from 152 to 405 kHz. ATPLCOUP002 mounts a double branch with voltage isolation from mains to the PLC coupling driver board. The goal of this design is provided to the customers with a full performance transmission board in ARIB bands. This board is not set by default in the ATPL250ABN board of the PANCoordinator-EK.

Figure 5-1. FCC and ARIB bands.

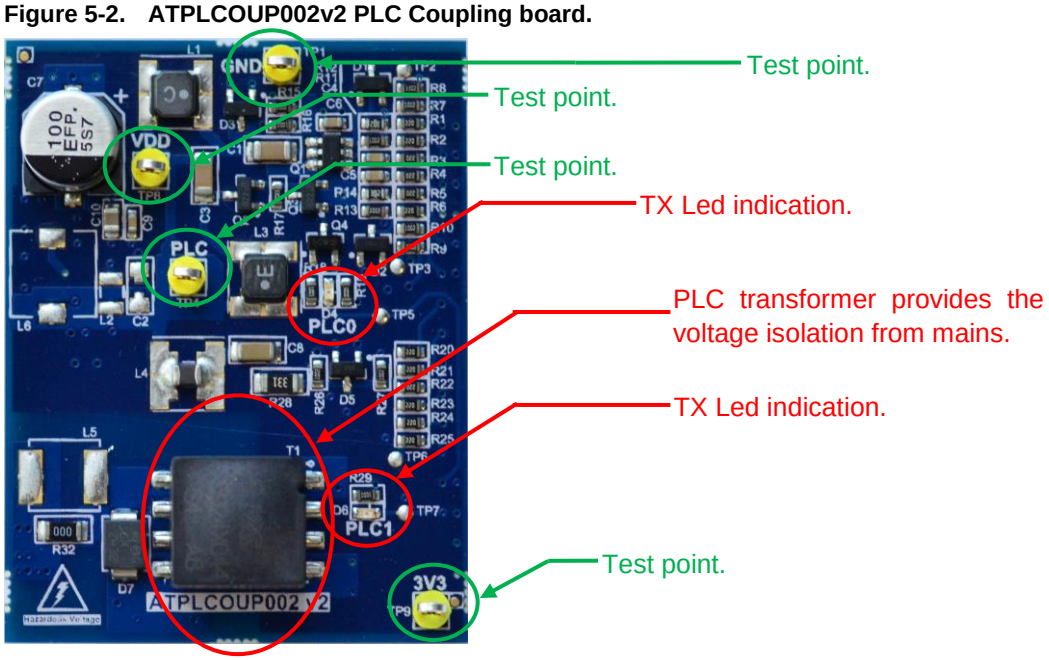


5.2 Features

The ATPLCOUP002v2 board includes the following features (see Figure 5-2):

- G3 FCC/ARIB bands (152 – 405 kHz).
- Double-branch design:
  - Low impedance optimized.
  - High impedance optimized.
- Voltage Isolation from mains with a transformer, *VAC T60403K5024X044*, soldered in top layer board.

Figure 5-2. ATPLCOUP002v2 PLC Coupling board.



5.3 Mechanical and user considerations

ATPLCOUP002 is delivered with the PANCoordinator-EK. Board-to-board SMD connectors, J1 and J2, are used to connect the ATPLCOUP002 into connectors J6 and J7 of ATPL250ABN board (Figure A-8). These J1 and J2 connectors are in bottom layer of ATPLCOUP002 and they have the following part numbers:

- J1: SAMTEC FTR-130-54-L-S.
- J2: SAMTEC FTR-124-54-L-S.

The ATPLCOUP002 board is directly powered from mains grid, so hazardous voltage is present on the board. To avoid user access to dangerous parts, ATPLCOUP002 must always be used in its enclosure.

ATPLCOUP002 is a CE mark product that passes EN 50065-1, EN 50065-2-3, EN 50065-7 EMC and STD-T84v1.0 (ARIB) standards. It also satisfies Pb-Free and ROHS directive.

ATPLCOUP002 dimensions are 51.5mm x 39.5mm x 18mm (LxWxH).

The operating temperature range is about -40 to 85ºC.

5.4 Hardware description

Hardware files are contained in the Hardware folder: *".\Hardware\HW_SCH&PCB\ATPLCOUP002v2"*.

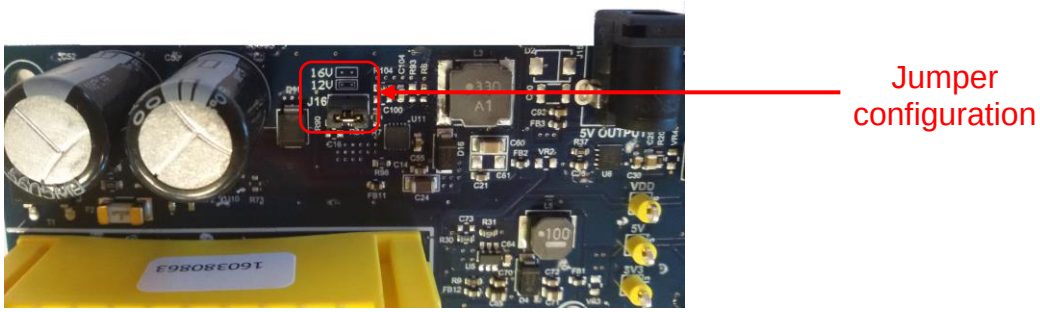
ATPLCOUP002v2 board is a PLC coupling driver board with double branch design and galvanic voltage isolation. ATPLCOUP002 has been designed to transmit in ARIB and FCC bands, especially in bands from 260 to 417 kHz.

It has a good performance in terms of transmitted frequency band power over a range of load impedance values complying with ARIB standard (sections 3.2 and 3.3 of the standard), see ARIB normative. ATPLCOUP002 is composed of two transmission branches which only differ on the filtering stage. A 12V power supply voltage for the class-D amplifier is recommended to be used with ATPLCOUP002.

For more information, see PLC coupling reference designs document, doc43052.

Take into account that, when ATPLCOUP002 is connected to ATPL250ABN, V_{DD} voltage must be **12 volts** to avoid damaging the coupling board, so jumper in J20 must be **set** (see section 3.5.1 and Figure A-2). By default, the jumper is placed in J16.

Figure 5-3. V_{DD} selection in ATPL250ABN board.

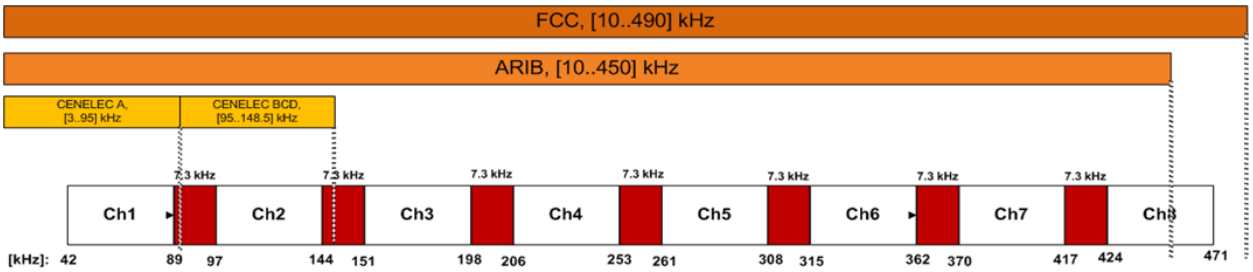


6. ATPLCOUP006 Hardware

6.1 Overview

ATPLCOUP006 is a PLC coupling board designed to communicate in ARIB and FCC bands, especially in G3 bands from 152 to 489 kHz. ATPLCOUP006 mounts a double branch with voltage isolation from mains to the PLC coupling driver board. The goal of this design is provided to the customers with a full performance transmission board in FCC band. This board is not set by default in the ATPL250ABN board of the PANCoordinator-EK.

Figure 6-1. FCC and ARIB bands.

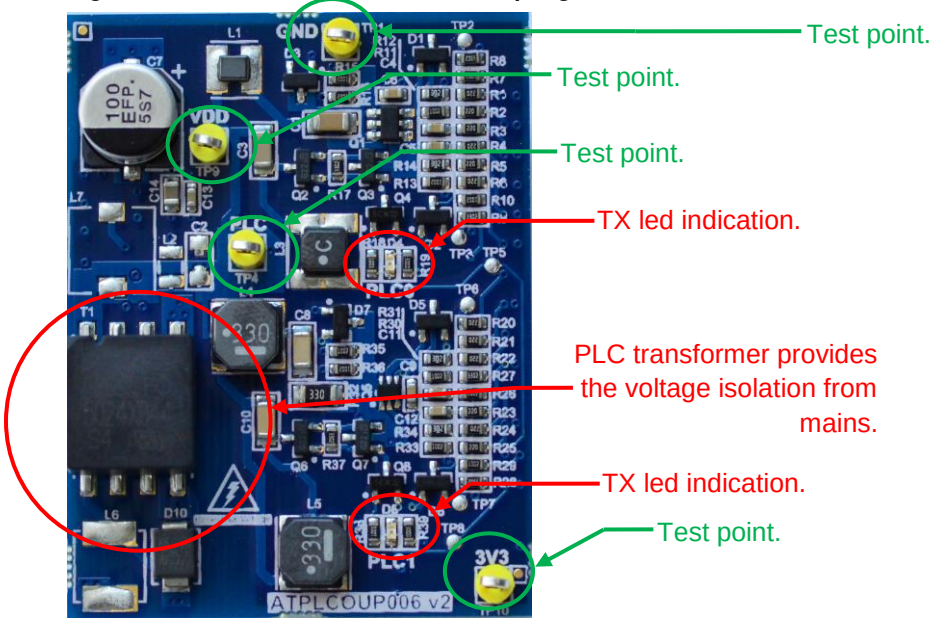


6.2 Features

The ATPLCOUP006v2 board includes the following features:

- Specially designed to communicate in ARIB and FCC frequency bands (152 – 489 kHz).
- Voltage Isolation from mains with a transformer, *VAC T60403K5024X044*, soldered in top layer board.
- Double branch, each one for a range of impedances:
  - Low impedance optimized.
  - High impedance optimized.

Figure 6-2. ATPLCOUP006v2 PLC coupling board.



6.3 Mechanical and user considerations

ATPLCOUP006 is delivered with the PANCoordinator-EK. Board-to-board SMD connectors, J1 and J2, are used to connect the ATPLCOUP006 into connectors J6 and J7 of ATPL250ABN board (Figure A-8). These J1 and J2 connectors are in bottom layer of ATPLCOUP006 and they have the following part numbers:

- J1: SAMTEC FTR-130-54-L-S.
- J2: SAMTEC FTR-124-54-L-S.

The ATPLCOUP006 board is directly powered from mains grid, so hazardous voltage is present on the board. To avoid user access to dangerous parts, ATPLCOUP006 must always be used in its enclosure.

ATPLCOUP006 is a CE mark product that passes EN 50065-1, EN 50065-2-3, EN 50065-7 EMC and FCC (as current carrier system) standards. It also satisfies Pb-Free and ROHS directive.

ATPLCOUP006 dimensions are 51.5mm x 39.5mm x 18mm (LxWxH).

The operating temperature range is about -40 to 85ºC.

6.4 Hardware description

Hardware files are contained in the Hardware folder: *".\Hardware\HW_SCH&PCB\ATPLCOUP006v2"*.

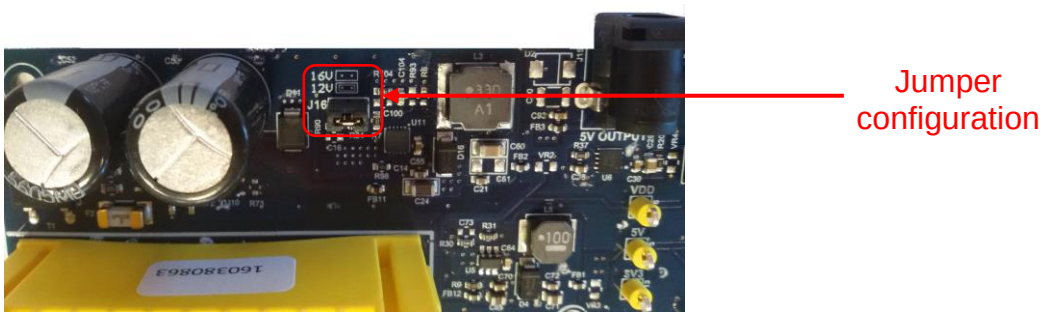
ATPLCOUP006v2 board is a PLC coupling driver board with double branch design and galvanic voltage isolation. ATPLCOUP006 has been designed to transmit in ARIB and FCC band, especially in bands from 151 to 472 kHz.

It has a good performance in terms of transmitted frequency band power over a range of load impedance values complying with FCC standard as current carrier system, see FCC normative. ATPLCOUP006 is composed of two transmission branches which only differ on the filtering stage. A 12V power supply voltage for the class-D amplifier is recommended to be used with ATPLCOUP006.

For more information, see PLC coupling reference designs document, doc43052.

Take into account that, when ATPLCOUP006 is connected to ATPL250ABN, V_{DD} voltage must be **12 volts** to avoid damaging the coupling board, so jumper in J20 must be **set** (see section 3.5.1 and Figure A-2). By default, the jumper is placed in J16.

Figure 6-3. V_{DD} selection in ATPL250ABN board.



7. PAN Coordinator Evaluation Kit: Getting started

The purpose of this chapter is to provide an introduction to the Atmel PANCoordinator-EK and its functionalities.

First of all, the software is presented to create, build, program and debug your application using the appropriate IDE tools (section 7.1).

Chapter 7.2 describes a simple PLC application to check PLC performance in a point-to-point connection (PHY layer example).

Chapter 7.3 describes the PHY TX Test Console application, which lets you configure a proper setup to perform both EMC emissions and immunity tests on ATPL250ABN board.

Chapter 7.4 describes the G3 PHY Sniffer project, which, is able to monitor data traffic on the G3-PLC network.

Chapter 7.5 describes the Atmel G3-PLC Stack and we present you the structure of a G3-PLC project.

Chapter 7.6 explains the setup and operations required to create a smart PLC network using the included G3 PAN Coordinator example. This network communicates by means of G3-PLC.

Note: The software described in this manual is under the Atmel`s *Evaluation License Agreement.pdf* document, available in the Software folder.

7.1 Introduction to the embedded system

The purpose of this section is to guide new users through the initial settings of IAR Embedded Workbench, Atmel Studio (AS) or Keil µVision, and compile a G3 project. The section shows setup of a G3 project to generate a debug target that can be loaded into the microcontroller.

Kit projects are supported by IAR 7.70, µVision 5.14 or AS 6.2 versions or above. From this point on, it is assumed that a working copy of this IDE is installed in your computer. The IAR's homepage, http://www.iar.com, is a suitable source to download (i.e.: 30-day time-limited evaluation license). In the Atmel's homepage, http://www.atmel.com, is suitable for downloading the Atmel Studio (free download). Visit http://www.keil.com/ to get a MDK-Lite version.

7.1.1 IAR Embedded Workbench

IAR Embedded Workbench is a high-performance C/C++ compiler assembler, linker, librarian, text editor, project manager, and C-SPY® Debugger in an integrated development environment for applications based on 8-, 16-, and 32-bit microcontrollers. IAR Embedded Workbench is compatible with other ARM EABI compliant compilers and supports the SAM4C core family (example projects are developed only for 7.70 versions or above).

7.1.2 Keil µVision

µVision is a window-based software development platform that combines a robust and modern editor with a project manager and makes facility tool. It integrates all the tools needed to develop embedded applications including a C/C++ compiler, macro assembler, linker/locator, and a HEX file generator.

µVision offers a Build Mode for creating applications and a Debug Mode for debugging applications. Applications can be debugged with the integrated µVision Simulator or directly on hardware.

PLC example projects are developed only for µVision 5.14 versions or above.

7.1.3 Atmel Studio 6

Atmel Studio is the integrated development platform (IDP) for developing and debugging Atmel ARM Cortex-M and Atmel AVR® microcontroller (MCU) based applications. The Atmel Studio IDP gives you a

seamless and easy-to-use environment to write, build and debug your applications written in C/C++ or assembly code.

Atmel Studio 6 is free of charge and is integrated with the Atmel Software Framework (ASF) — a large library of free source code with 1,600 ARM and AVR project examples. ASF strengthens the IDP by providing, in the same environment, access to ready-to-use code that minimizes much of the low-level design required for projects. Use the IDP for our wide variety of AVR and ARM Cortex-M processor-based MCUs, including our broadened portfolio of Atmel SAM3 ARM Cortex-M3 and M4 Flash devices.

We recommend download and installing the last version of Atmel Studio. You can download all versions from the following link:

http://www.atmel.com/tools/STUDIOARCHIVE.aspx.

7.1.4 Atmel SAM-ICE JTAG Probe

Atmel SAM-ICE (a dedicated Atmel J-Link version) is a USB-powered JTAG emulator supporting Atmel ARM-based microcontrollers.

Atmel SAM-ICE is a JTAG emulator designed for Atmel SAMA5, SAM3, SAM4, SAM7 and SAM9 ARM core-based microcontrollers, including the Thumb® mode. It supports download speeds up to 720 Kbytes per second and maximum JTAG speeds up to 12 MHz. It also supports Serial Wire Debug (SWD) and Serial Wire Viewer (SWV) from SAM-ICE hardware V6.

SAM-ICE support is integrated in most professional integrated development environments (IDEs) such as IAR, Keil and many others.

More details are available here: http://www.atmel.com/tools/ATMELSAM-ICE.aspx.

Figure 7-1. Atmel SAM-ICE JTAG.

This evaluation kit does not provide an Atmel SAM-ICE.

To use Segger tools with Atmel Studio, download Atmel's latest USB driver driver-atmel-bundle-7.0.712.exe from the following link: https://gallery.atmel.com/Products/Details/07bf16c1-444f-4ac8-8f40-9d4005575dca or take it from the PCTools folder: ".*PCTools\SAM-ICE_Drivers*". And install the file.

7.1.5 J-Link / SAM-ICE JTAG Probe Software & Documentation Pack

The J-Link / SAM-ICE JTAG software and documentation pack includes:

- GDB Server - Support for GDB and other debuggers using the same protocol. GUI & command line version.

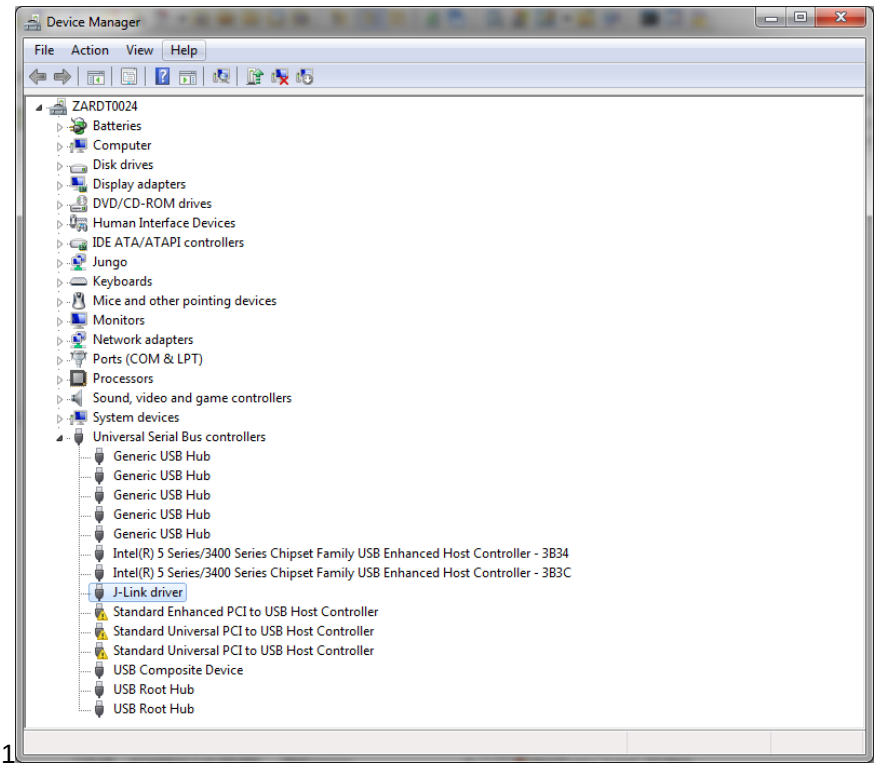
- J-Link Configurator - Free utility to manage a various number of J-Links connected to the PC via USB or Ethernet.
- J-Link Commander - Simple command line utility, primarily for diagnostics and trouble shooting.
- J-Link Remote Server - Free utility which provides the possibility to use J-Link / J-Trace remotely via TCP/IP.
- SWO Viewer - Free tool which shows terminal output of the target performed via SWO pin.
- J-Mem - Memory viewer.
- J-Link DLL Updater - Allows updating 3rd party applications which use the J-Link DLL.
- Free flash programming utilities - Simple command line utilities which allow programming a bin file into the internal/external flash memory of popular evaluation boards.
- USB driver (Includes driver for J-Links with CDC functionality).
- Manuals: UM08001 (J-Link User Guide), UM08003 (J-Flash User Guide), UM08004 (RDI User Guide), UM08005 (GDB Server User Guide) and UM08007 (Flasher ARM User Guide).
- Release notes for J-Link DLL, J-Flash and J-Link RDI DLL.
- J-Flash, including sample projects for most popular evaluation boards.
- J-Link RDI – Support for ARM RDI standard. Makes J-Link compatible with RDI compliant debuggers.

Installing the software will automatically install the J-Link USB drivers. It also allows the update of applications that use the J-Link DLL.

The last version of the driver for the SAM-ICE JTAG Probe can be downloaded from the http://www.segger.com website using the following link: http://www.segger.com/jlink-software.html. The package for Windows, *Setup_JLinkARM_V496b.zip***,** is located in the following folder: *".\PCTools\SAM-ICE Driver"*.

Once drivers have been installed you may verify the driver installation by consulting the Windows® device manager. If the driver is installed and your SAM-ICE is connected to your computer, the device manager should list the J-Link driver as a node below "Universal Serial Bus controllers" as shown in the following screenshot.

Figure 7-2. Device manager.



1

7.1.6 Atmel Software Framework (ASF)

The Atmel Software Framework (ASF) is a collection of embedded software for the Atmel Flash MCUs: megaAVR, AVR XMEGA, AVR UC3 and SAM devices.

It simplifies the use of our microcontrollers by providing an abstraction to the hardware and high-value middleware. ASF is designed to be used for evaluation, prototyping, design and production phases. The intention of ASF is to provide a rich set of proven drivers and code modules developed by Atmel experts to reduce customer design-time. It simplifies the usage of microcontrollers, providing an abstraction to the hardware and high-value middleware.

ASF is integrated in the Atmel Studio IDE with a graphical user interface or available as standalone for GCC, IAR compilers. ASF can be downloaded for free. ASF is an open-source code library designed to be used for evaluation, prototyping, design and production phases.

The Atmel Software Framework is split in six main parts, the *avr32/* directory, the *xmega/* directory, the *mega/* directory, the *common/* directory, the *sam/ directory* and the *thirdparty/* directory. These six directories represent the Atmel AVR UC3 architecture, the Atmel megaAVR, the Atmel AVR XMEGA architecture and the Atmel SAM architecture, what are common between all architectures and finally third party libraries.

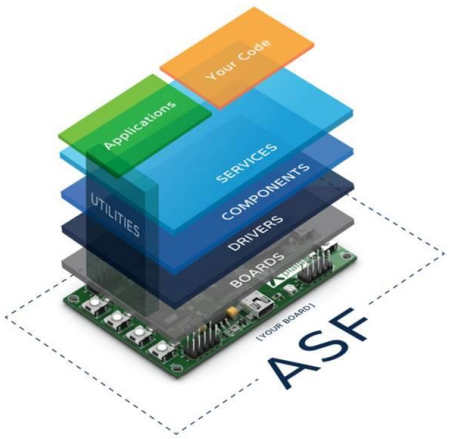
Each architecture (and the common directory) is split into several subdirectories, these directories contain the various modules; boards, drivers, components, services and utilities.

See the list below and Figure 7-3 for an overview of how the various modules are wired together:

- *Boards* contain mapping of all digital and analog peripheral to each I/O pin of Atmel's development kits.
- *Drivers* is composed of a *driver.c* and *driver.h* file that provides low level register interface functions to access a peripheral or device specific feature. The services and components will interface the drivers.

- *Components* is a module type which provides software drivers to access external hardware components such as memory (e.g. Atmel DataFlash®, SDRAM, SRAM, and NAND flash), displays, sensors, wireless, etc.
- *Services* is a module type which provides more application oriented software such as a USB classes, FAT file system, architecture optimized DSP library, graphical library, etc.
- *Utilities* provide several linker script files, common files for the build system and C/C++ files with general usage define, macros and functions.
- *Applications* provide application examples that are based on services, components and drivers modules. These applications are more high level and might have multiple dependencies into several modules.

Figure 7-3. ASF modules structures.



Download link for more information: http://www.atmel.com/tools/AVRSOFTWAREFRAMEWORK.aspx. Please do not hesitate to visit our web site to get the last library updates.

7.2 PLC application example 1 – PHY Tester

Board of the kit, by default, are programmed with the embedded PLC PHY Tester tool firmware for SAME70Q21 device, *apps_phy_tester_tool.bin*. It is an application example that shows the capabilities of the ATPL250A in a point-to-point connection (physical layer). This application requires a pair of boards and a PC tool, Atmel PLC PHY Tester tool, which has to be installed in the user's host PC to interface with the board.

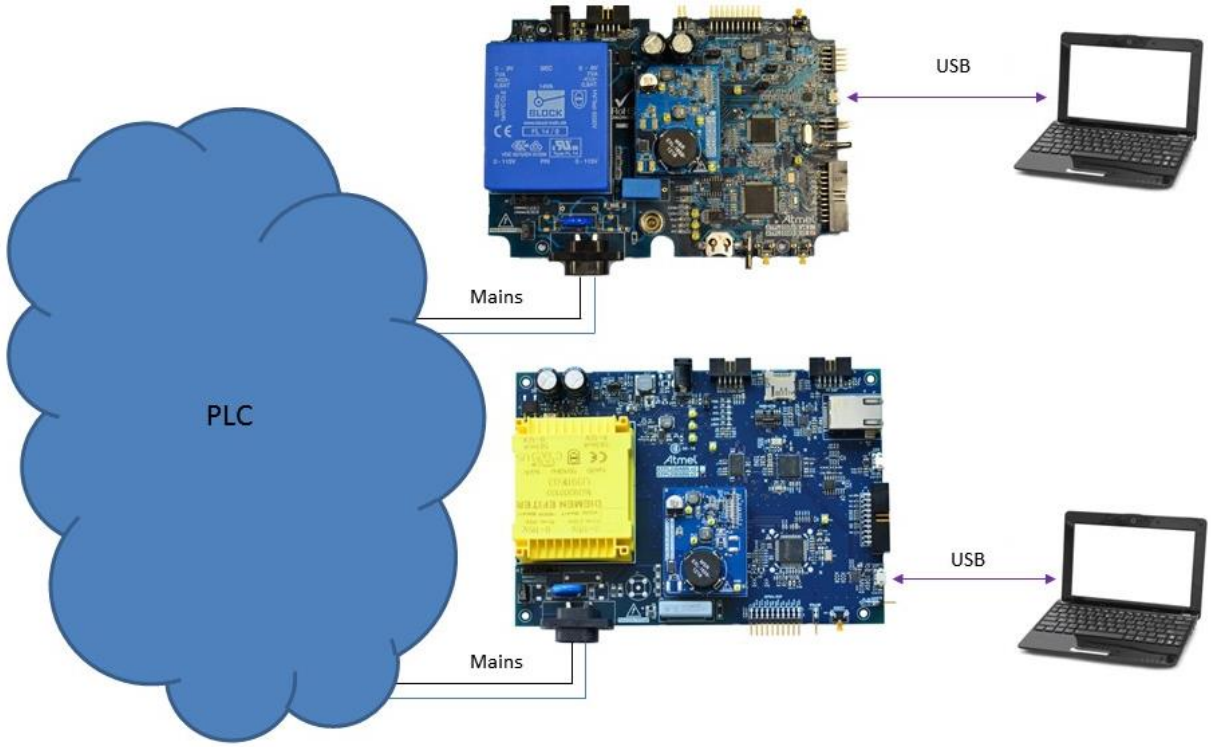
In any case, if you want to load this file again, you have to build the project *apps_phy_tester_tool* to generate the output file to program. See section 7.2.4 to know more about programming the ATPL250ABN board.

Atmel recommends to load the binary generated with the last PHY Tester Tool project released in the kit to evaluate the board with last improvements.

After installing the Atmel PLC PHY Tester tool in your PC(s), connect the two boards to the grid and to the host(s) PC(s) as shown in the following figure.

To run this example, two boards are used. So another Atmel board besides of ATPL250ABN is necessary to run this test, e. g, ATPL250AMB.

Figure 7-4. Atmel Boards connection scheme.

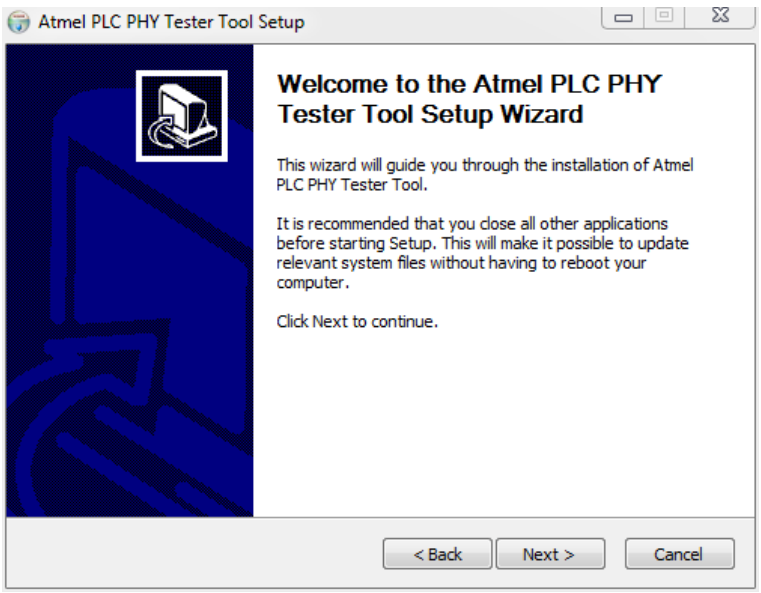


Following chapters explain to you how to install the PC tool, supply the boards, and select the UART0 to communicate with the SAME70Q21. Load the firmware and run the application.

7.2.1 Atmel PLC PHY Tester tool Installation

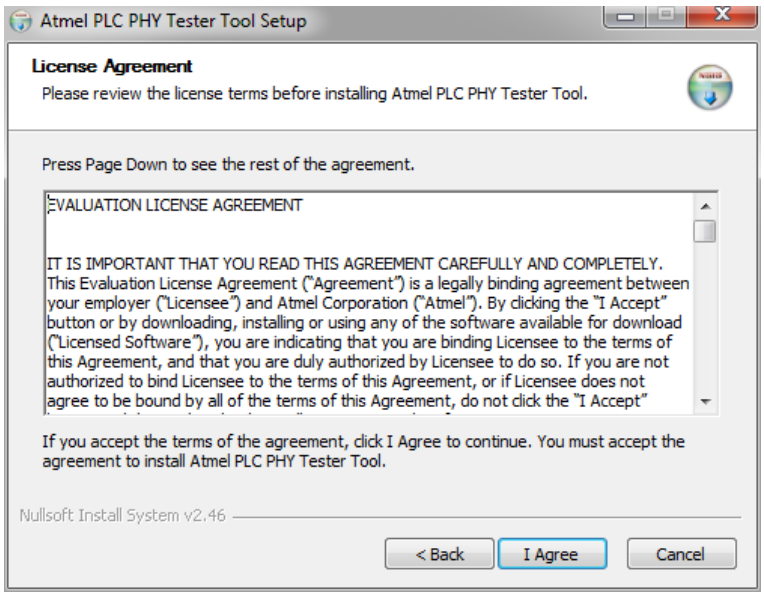
To install Atmel PLC PHY Tester tool in a Windows Operating System, execute the provided installer in the Tools folder: *".\PCTools\ATMEL_PLC_PHY_Tester\ATMEL_PLC_PHY_Tester_Tool_vX.Y.Z.exe"*, and follow the installation wizard. The installer wizard should open. To follow with the installation, click Next.

Figure 7-5. Installation process, slide 1.



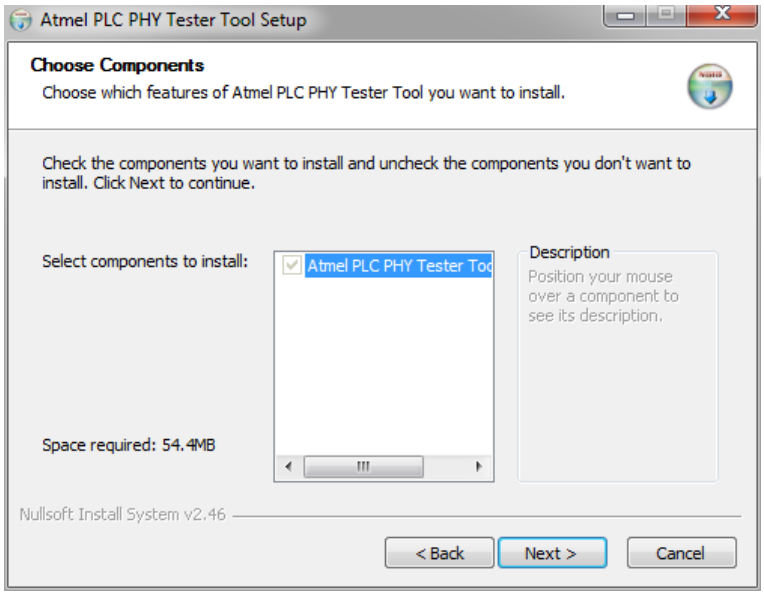
Select the users' permissions and click Next.

Figure 7-6. Installation process, slide 2.



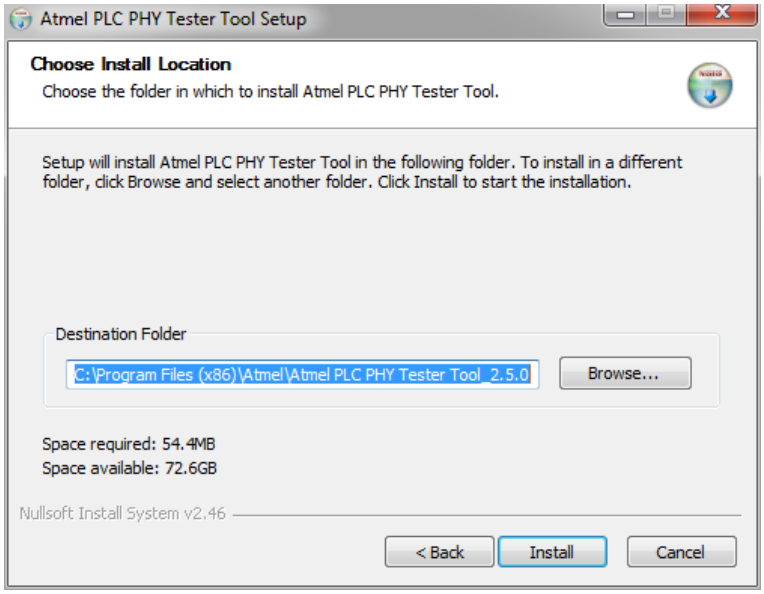
Click I Agree to continue.

Figure 7-7. Installation process, slide 3.



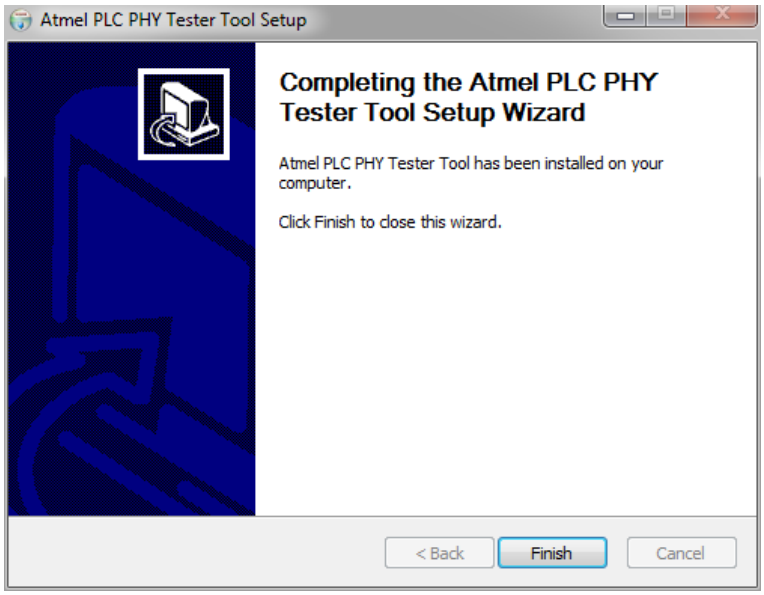
Click Next.

Figure 7-8. Installation process, slide 4.



Setup will install the program in the *Destination Folder*. To install in a different folder, click Browse and select your destination folder. Click Install.

Figure 7-9. Installation process, slide 5.



Click Finish.

Now the program is installed in your computer and a shortcut should have been created in your desktop.

Note that Atmel releases of G3-PLC versions lower than 1.2.2 run with PHY Tester PC Tool version 2.4.6. Atmel G3-PLC version 1.2.2 or above run with PHY Tester PC Tool version 2.5.0 or above.

7.2.2 Supplying the boards

Kit is provided with power cord cable in order to connect the board to the mains. Mains connector is shown below in Figure 7-10. Please connect the provided power cord cable with the kit to the *Power Cord Connector, J1,* in order to supply the board.

Figure 7-10. ATPL250ABN mains and voltage jumper selector.

Note that the ATPL250ABN board can be supplied either with $100V_{AC}$ or $230V_{AC}$ by setting the proper jumpers in the voltage selector, J2, as depicted in the Figure 7-11. By default, voltage jumper is set for $230V_{AC}$. For more information about power supply section, see section 3.5.1.

Figure 7-11. Jumper configuration for $115V_{AC}$ or $230V_{AC}$.

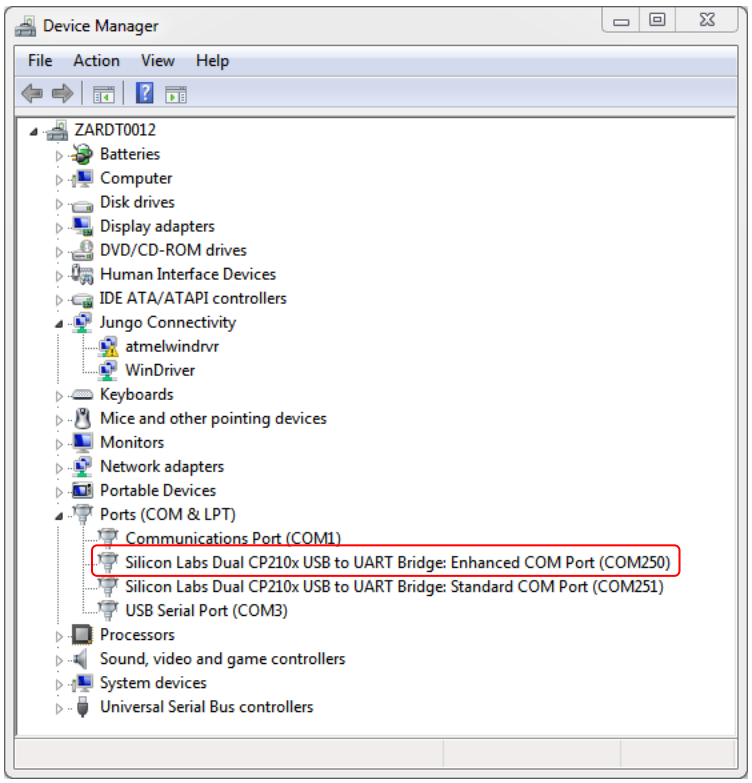
7.2.3 USB connection

By default, the programmed firmware for Atmel PHY Tester tool establishes serial communication with **UART0**. Boards have such UART0 available either by micro-B USB connector, J9, or the triple pin row CMOS connector, J16. See the Figure 3-2 and section 3.5.7.4 for more information about the USB device. PAN Coordinator Evaluation Kit is provided with one micro USB cable in order to connect the user's host(s) PC(s) with the PAN Coordinator board.

Previous to connect the USB cable to the micro-B USB connector and the host PC, supply the ATPL250ABN board. If the PC does not recognize the USB, download the USB driver from the manufacturer webpage or take it from the *PCTools* folder: ".*PCTools**USB_Drivers*". Once the driver is downloaded, unpack the driver archive to a folder on the host PC's hard-disk. Connect the USB cable to the board. The new hardware installation will recognize the new board and will guide you through the USB driver installation. When the wizard asks for the driver to install, navigate to the directory where the driver archive has been unpacked to.

Identify the new hardware in the *Windows Device Manager*. The assigned COM port number is needed when configuring the PHY Tester tool application later. See the following figure for an example of a COM port assignment.

Figure 7-12. Windows device manager.



As you can see in the figure above, the CP210x USB to UART Bridge Virtual COM Port (VCP) appears as two COM ports (Enhanced and Standard COM ports) in the Device Manager. They are assigned the lowest available COM ports for operation. In the ATPL250ABN design, the Enhanced COM port corresponds to UART0, so select the Enhanced COM Port when you use the Atmel PLC PHY Tester PC tool.

7.2.4 Programming the embedded file

To be able to develop applications, build binaries and program the firmware on the SAME70Q21 device, you can use the IAR Workbench, Keil µVision or Atmel Studio. For that, open the IDE tool used, select the PHY Tester tool project and now build it to generate the output file.

Remember that the J-Link USB drivers must have been downloaded previously from the Segger webpage (see section 7.1.5) and they depend on your operating system. In order to program the firmware on the board, set the JTAG probe, SAM-ICE, on the JTAG connector, J13 (see section about JTAG programming mode, 3.5.7.1).

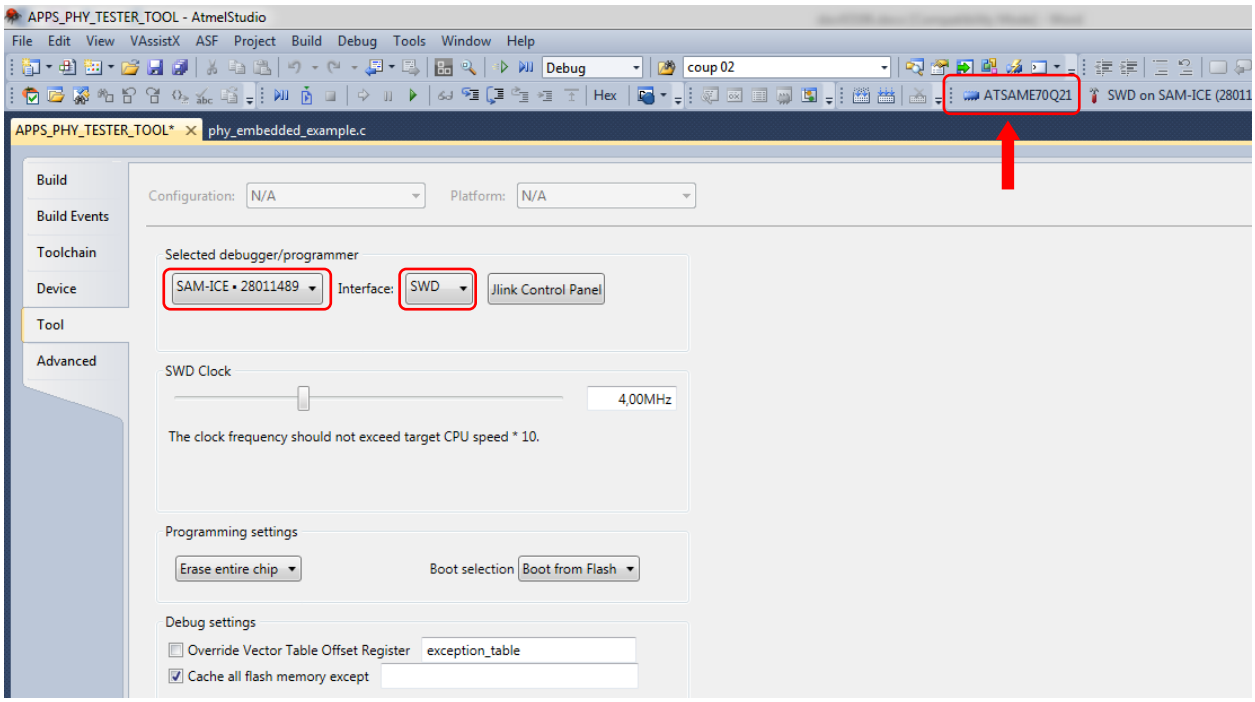
Note that kits do not provide a J-Link ARM or SAM-ICE JTAG probe in order to connect to the user's host PC and the boards to download and debug the projects.

The process to load the file should be as is explained below; in that process we use a programming tool, J-Link Tool. Remember that the J-Link USB drivers must have been downloaded previously from the Segger webpage (see section 7.1.5) and they depend on your operating system:

1. Place the JTAG connector of the J-Link or SAM-ICE in the J13, JTAG connector of the board. Check pin number 1 of J13 connector to place the cable in the right position.
2. Switch on the power supply of the board.
3. Launch the IAR, Keil or Atmel Studio and select the PHY Tester tool project. Now you can download the file to the board. Build the project *apps_phy_tester_tool.atsln* or *apps_phy_tester_tool.eww* or *apps_phy_tester_tool_flash.uvprojx* to generate the output file to program. Now you can download

the file to the board. In case of programming with Atmel Studio IDE, select the interface to SWD to download the output file. By default, JTAG option is selected. That option is found in Tool tab of Device (ATSAME70Q21) button toolbar. See the following figure.

Figure 7-13. Atmel Studio debugger/programmer settings.



Remember that, PHY Tester Tool example project is contained in the following Software folder:
".\Software\G3_va.b.c\g3.workspace.same70q21_atpl250abn_v2\thirdparty\g3\phy\atpl250\apps\phy_tester_tool\".

Note that the firmware provided for this example is only for the ATPL250ABN board. To show all features and run the application another Atmel board is required, i.e. ATPL250AMB. Which it has been programmed with the respective application, *APPS_PHY_TESTER_TOOL*. See ATPL250A-EK for more information.

PHY Tester Tool project of *G3_va.b.c* folder has been created for CENELEC-A, FCC and ARIB bands, ATPLCOUP007v2.5, ATPLCOUP006v2 and ATPLCOUP002v2 PLC coupling boards respectively. For FCC/ARIB option, select the project folder with suffix "_fcc" and open the project application, *apps_phy_tester_tool.atsln*, *apps_phy_tester_tool.eww* or *apps_phy_tester_tool_flash.uvprojx*.

After that, you can select the file *conf_project.h*, that it is located in the following project directory: *".\Software\G3_va.b.c\g3.workspace.same70q21_atpl250abn_v2\thirdparty\g3\phy\atpl250\apps\phy_tester_tool\same70q21_atpl250abn_fcc"*, find the define function to select the coupling board configuration (see Figure 7-14). Change the frequency band name to the desired and build to generate the output file.

Figure 7-14. Frequency band configuration definition.

```
49  /* Configuration constants */
50
51  // Work Band
52  #define CONF_CENELEC_A
53  //#define CONF_FCC
54  //#define CONF_ARIB
```

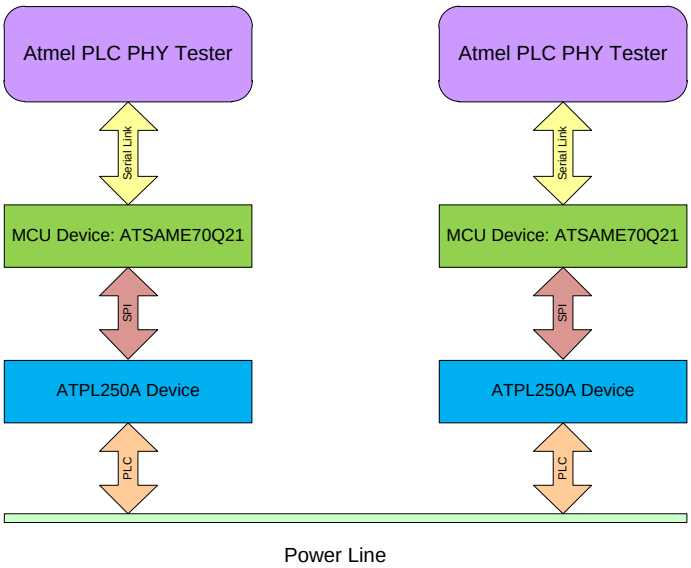
Check the Table 3-1 for the characteristics of the available *ATPLCOUPxxx* boards.

Note that Atmel releases of G3-PLC versions lower than 1.2.2 run with PHY Tester PC Tool version 2.4.6. Atmel G3-PLC version 1.2.2 or above run with PHY Tester PC Tool version 2.5.0 or above.

7.2.5 Running the PLC application example 1

The Atmel PLC PHY Tester tool is used to control the application running on the SAME70Q21+ATPL250A. As you can see in Figure 7-15, the two boards are plugged into the same power line. Users have to execute two instances of the PHY Tester tool – which has been previously installed in the host(s) PC(s) – in order to enable communication between both boards. Please note that these two instances may or may not run on the same computer.

Figure 7-15. Atmel PLC PHY Tester concept.



In order to know if the boards were programmed successfully you can check if the green led LED0, D5 is blinking. This indicates that the PHY Tester Tool application is running on SAME70Q21 device.

You must select the same coupling boards to plug in both Atmel boards. Check the coupling identifier that you can find in the coupling board.

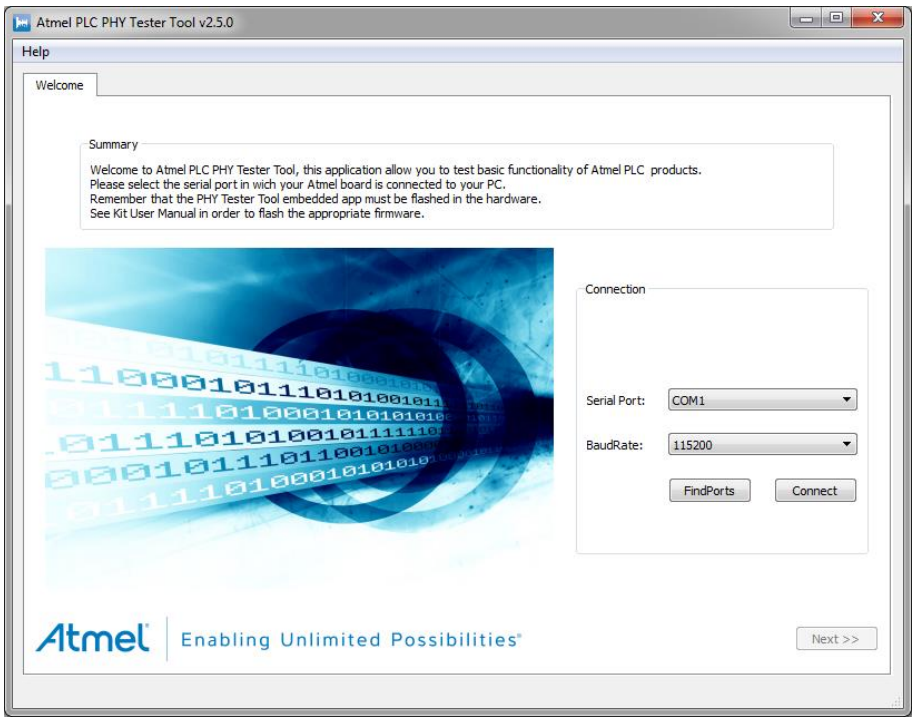
These coupling boards must be the proper one for the frequency band you want to send/receive, otherwise please remove them and connect the proper ones.

By default, ATPL250ABN board sets an ATPLCOUP007 coupling board, so V_{DD} voltage of ATPL250ABN must be 12 volts. V_{DD} can be regulated to 16 or 12 volts depending on the J16 jumper position. In this situation, jumper J16 must set. See section 3.5.1 and Figure A-2 for more information.

Other coupling boards may require different voltage for the class D amplifier (V_{DD}).

Once the application is launched, *Starting Window* will appear (see Figure 7-16).

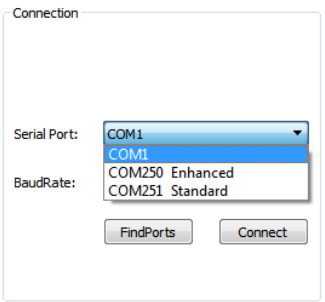
Figure 7-16. Welcome instance.



The first to do is configure the corresponding COM port for each board. In this window we select the serial connection configuration:

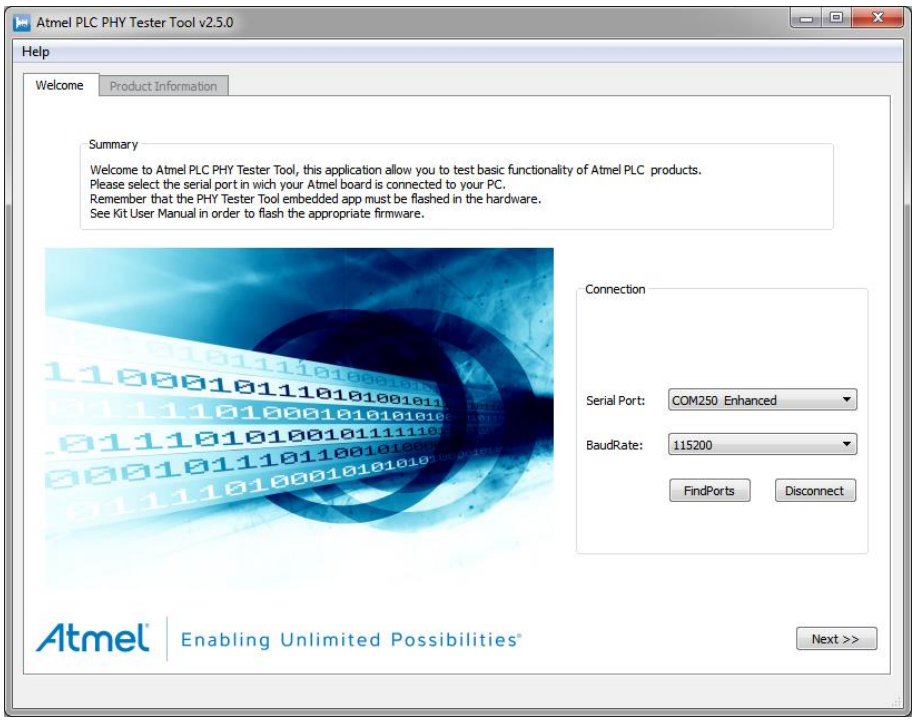
- Select in the Serial Port combo box the proper port to connect (see Figure 7-17). As it is explained in section 7.2.3, communication is by the Enhanced COM (UART0). If your COM port does not appear (see section 7.2.3), press Find Ports button.
- Select the BaudRate combo box of 115200 bauds.

Figure 7-17. Serial port selection.



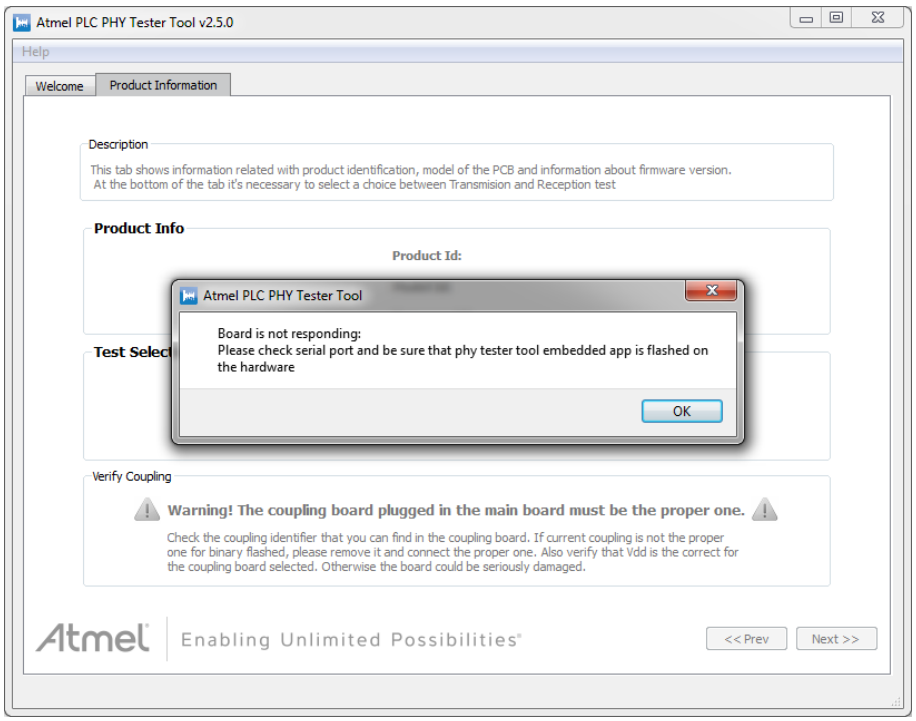
Once COM port is selected, click the Connect button. As soon as the button is clicked, the button text will change to *Connecting*. Then, the application and the board start a process of identification and, after few seconds, the button text will change to *Disconnect*. This means that the identification process has finished. A new Tab (*Product Information*) is appended to the wizard and Next button is enabled allowing the user to go to the following step of the configuration. See Figure 7-18.

Figure 7-18. Communication enabled.



In case the tool cannot establish a communication with the board, the tool shows the following error message.

Figure 7-19. Communication error.

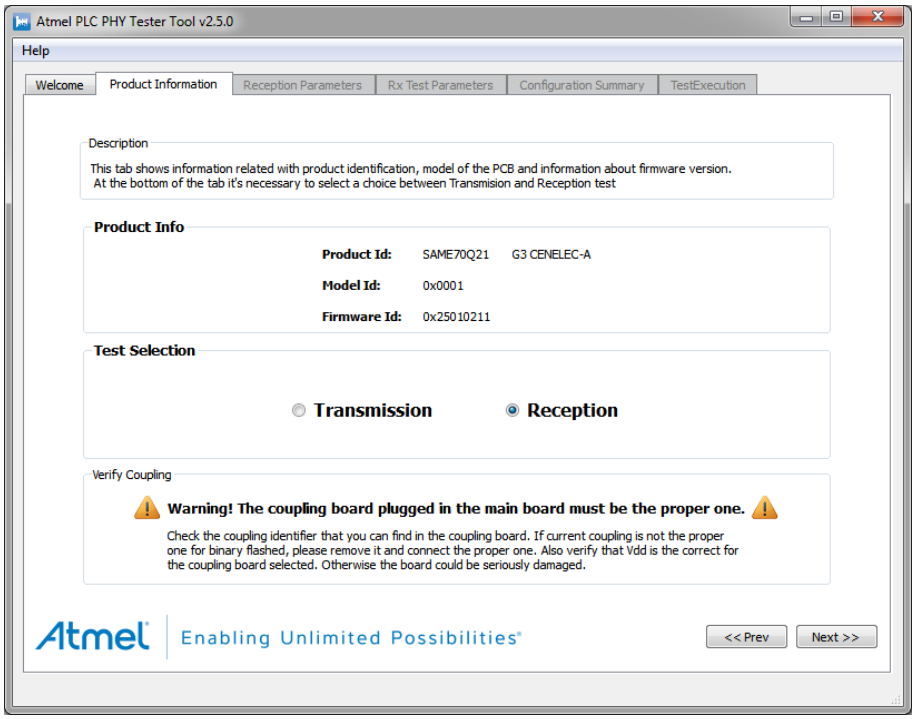


Click the OK button and press Prev button to get back to *Welcome* tab. Now press Disconnect button and check your connections. Either you have not selected the right Enhanced COM port or the board is not

supplied or the downloaded firmware is not the right. After these operations, you can retry to establish the communication again between the board and the computer.

Once the communication is right, *Product Information* tab of the PHY Tester tool is shown below in Figure 7-20.

Figure 7-20. Product Information tab of the Atmel PLC PHY Tester tool.



The *Product Information* Tab shows basic information of the type of board connected to, and also asks the user to select the kind of test to be performed.

The showed information is related to the physical layer implemented in the firmware of the board:

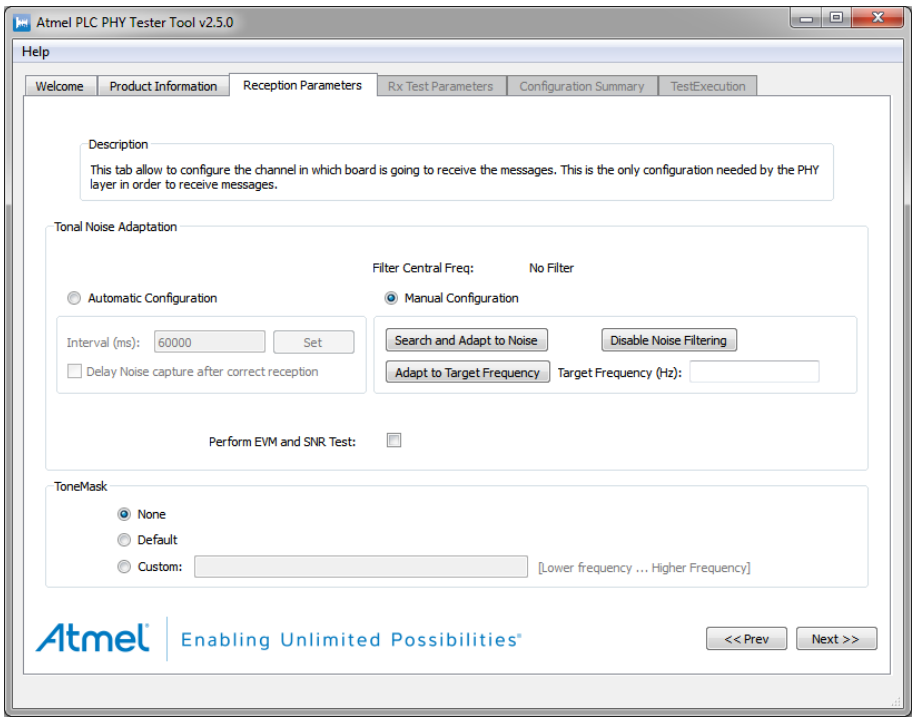
- **Product ID:** it shows a text string that identifies the Atmel PLC product (platform).
- **Model ID:** It is a 16-bit unsigned integer that identifies the model of the board.
- **Firmware ID:** It is a 32-bit unsigned integer that identifies the physical layer firmware running in the board.

Now the user has to do a selection depending on whether the user selects transmission or reception test, different tabs are added. For reception tests, "*Reception Parameters*" and "*Rx Test Parameters*" tabs are added. For transmission tests, "*Transmission Parameters*" and "*Tx Test Parameters*" tabs are added. Finally, independently of the kind of selected test, two more tabs are added: "*Configuration Summary*" and "*Test Execution*".

Note the warning message displayed before to continue, check the proper voltage to use (V_{DD} selection, see section 3.5.1).

First, we will describe the process to configure a board as receptor and after that we will describe how to configure the other board as emitter. Selecting the *Reception* option and clicking the Next button, a tab appears as the following image (Figure 7-21).

Figure 7-21. Reception Parameters tab.



In Reception Parameters tab you can select the tonal noise adaptation and the tone mask feature.

- Tonal noise adaptation. PHY layer is able to detect tonal noise and configure some input filters in order to cancel this noise. User can select two modes, *Manual* and *Automatic*.
  - Automatic Configuration. Hardware is performing noise captures every fixed interval (configurable). After each capture the hardware selects the proper filtering for the noise detected. User can configure to only perform the noise captures when hardware is not receiving. This option is activated by means of *Delay noise capture after correct reception* checkbox.
  - Manual Configuration. In this mode the hardware only performs noise analysis when user press Search and Adapt to Noise button. The user is also able to indicate the frequency where tonal noise is present and the firmware will configure the filters for this noise by means of Adapt to target frequency button. Finally user can disable noise adaptation using Disable Noise Filtering button.
- Tone mask. It allows to disable carriers for each symbol as G3 specification says. An array of 0 and 1 is shown when selecting *Custom* mode, there was a digit for each carrier in the current band plan (CENELEC-A = 36; FCC = 72; ARIB= 54), 1 means carrier disabled and 0 means carrier not disabled. *Default* option configures the PHY layer to disable the carriers specified in G3 interoperability tests for each band plan. If you do not use the tone mask feature select *None.*

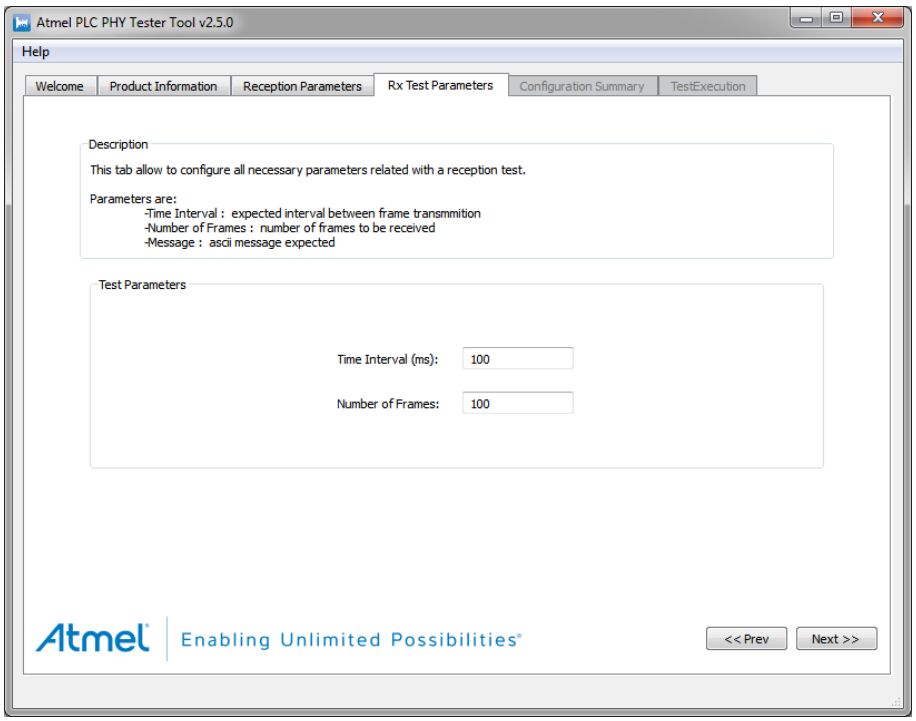
Click the Next button to continue.

The next tab shows the *RX Test Parameters*, see Figure 7-22. This tab is where the following reception test parameters are configured:

- Time Interval (milliseconds): expected interval between frame transmissions.
- Number of Frames: number of frames to be received.
- Message: ASCII message expected.

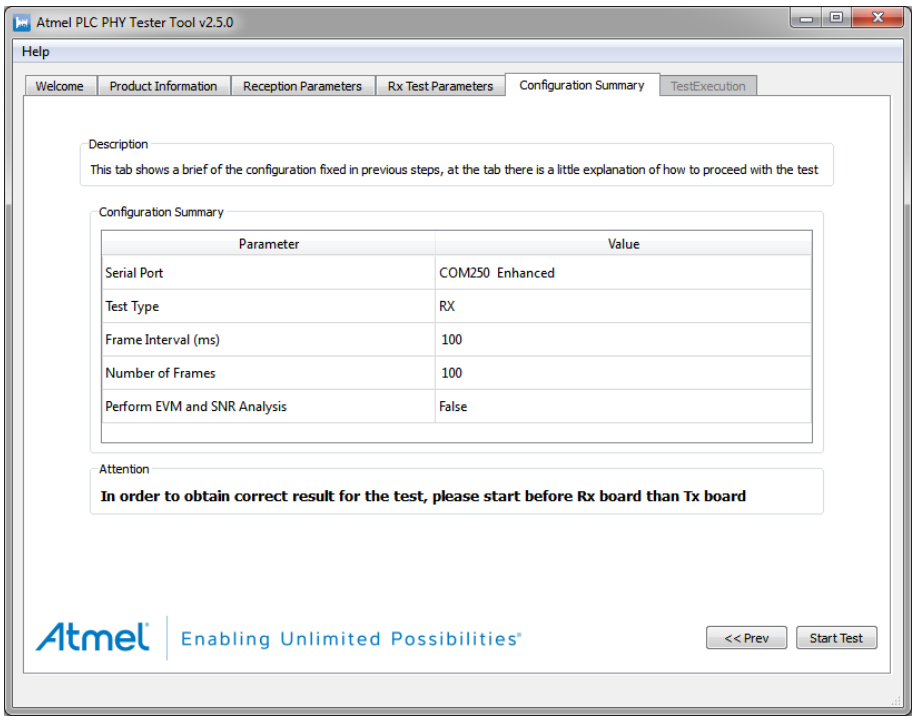
Default parameters (100ms and 100 frames) are selected.

Figure 7-22. RX test parameters.



Default parameters are selected. Click the Next button to continue.

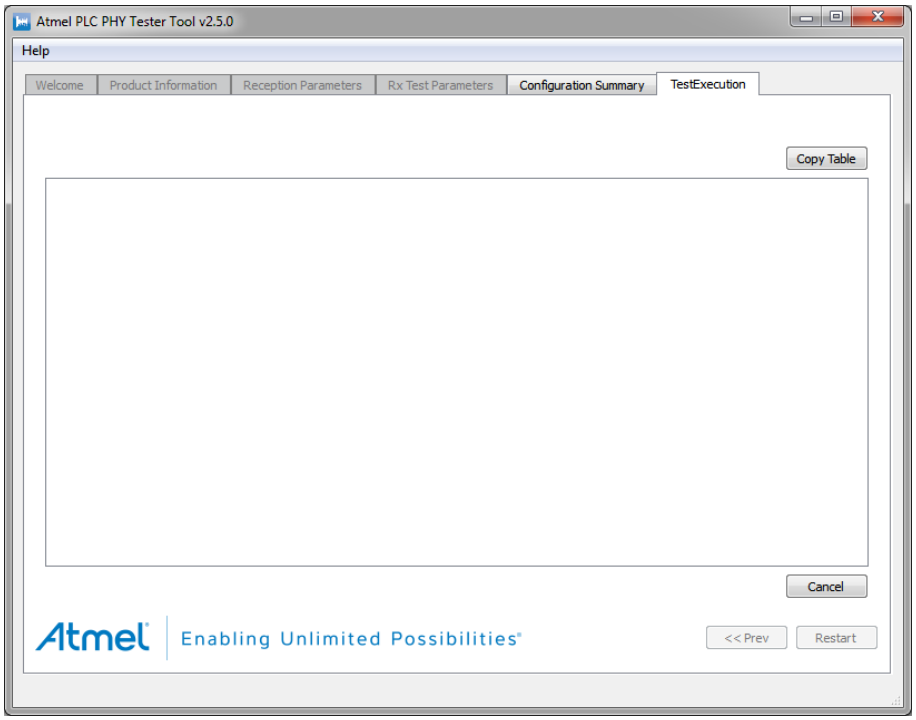
Figure 7-23. Configuration Summary tab.



The previous figure, *Configuration Summary* tab, shows a table where all the configuration parameters and their selected values are listed. It is recommended to check that all values correspond to the desired configuration before to continue.

To start the process, click the Start Test button. A new tab is enabled, at first the table is empty because any frame has been received. Note that there is a timeout to wait the frame reception.

Figure 7-24. Test Execution tab.



Once the receiver board has been configured, the emitter board must be configured. Launch another Atmel PLC PHY Tester tool and once the transmission board is supplied and USB cable connected, configure the corresponding COM port for the board in the window *Starting Window*.

Once COM port is selected, click the Connect button. As soon as the button is clicked, the button text will change to *Connecting*. Then, the application and the board start a process of identification and, after few seconds, the button text will change to *Disconnect*. This means that the identification process has finished. Press Next button.

A new Tab (*Product Information*) is appended to the wizard and click the Next button. This time we select in *Product Information* tab, the Transmission process (Figure 7-25). Press Next button to continue.

Figure 7-25. Transmission option selection.

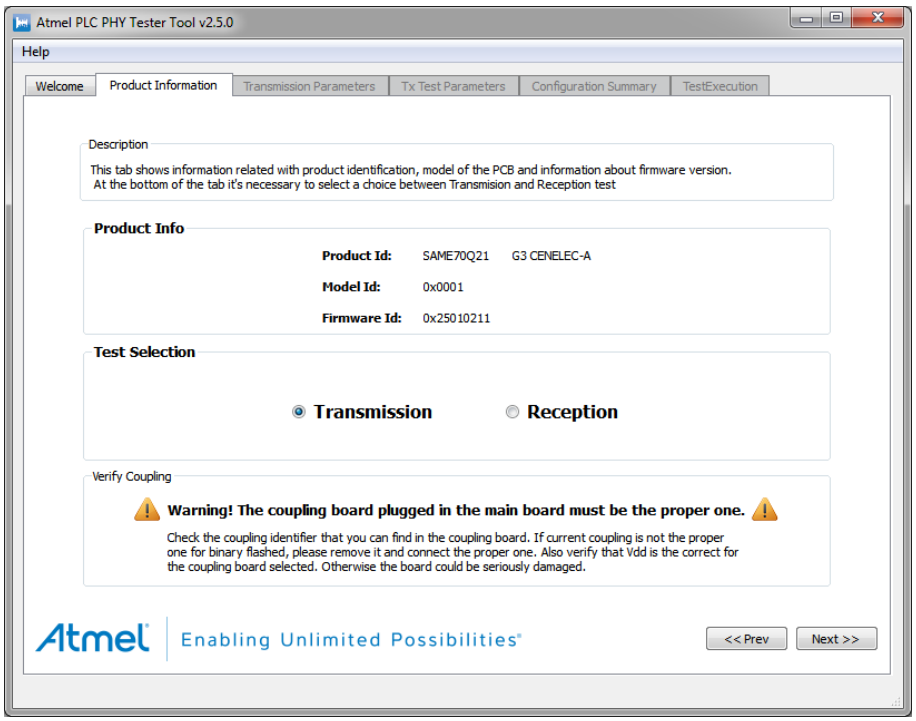
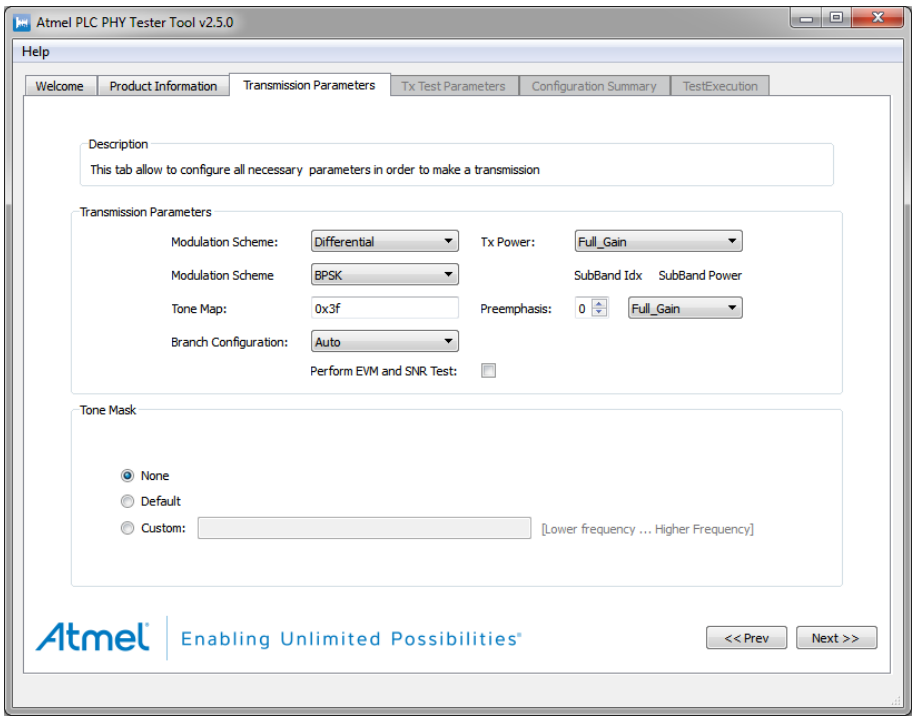


Figure 7-26. Transmission Parameters tab.



The *Transmission Parameters* tab appears (Figure 7-26) that allows you to configure the PLC coupling board plugged and the transmission parameters:

- Modulation Scheme. Allow to configure differential or coherent modulation scheme.
- Modulation Type. Allow to select between BPSK, QPSK, 8PSK and robust BPSK.

- Tone Map. Allow disabling sub-bands, it is dependant of bandplan selected. Each band is activated or deactivated setting to “1“ or “0“ in the corresponding bit of the hex array. The different sub-bands are ordered in the hex array from least significant bit (lower frequency sub-band) to most significant bit (higher frequency sub-band). For example, in CENELEC-A bandplan 0x01 represents a tone map where only lower sub-band is active, as well as 0x20 is the tone map corresponding to a tone map with only the higher sub-band active.
- Reed Solomon 2nd Block. This feature is only available for FCC and ARIB bandplans compiled firmware, it allows introducing a second RS block as G3-PLC specification tells.
- TX Power. Allow to decrease the transmission power in steps of 3 dB.
- Branch Configuration. You can select the impedance branch transmission.
- Preemphasis. Allow to introduce an attenuation for each sub-band.

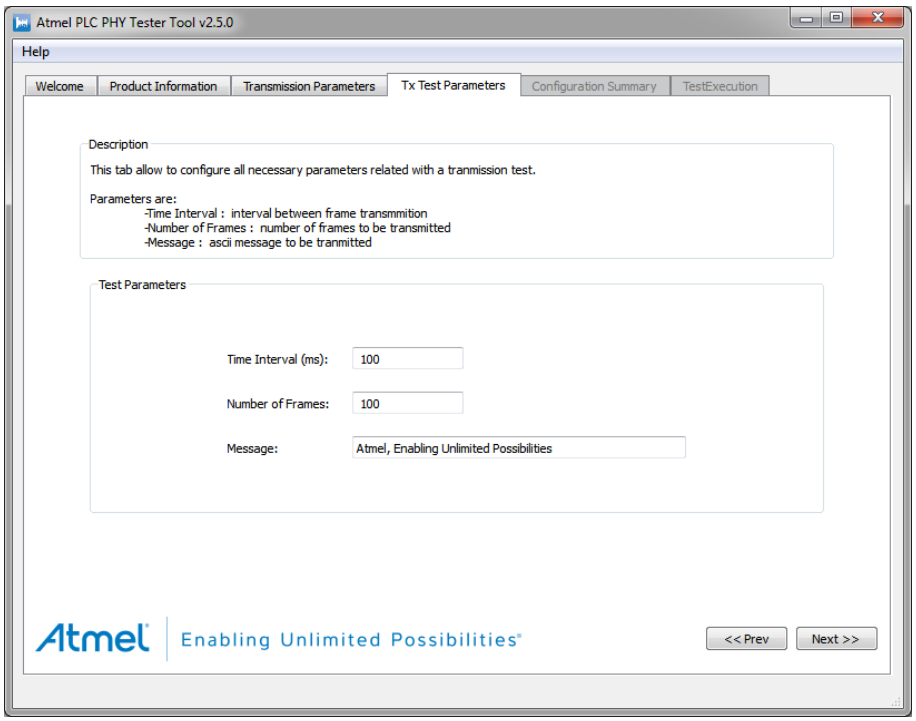
Note the warning message displayed before to continue, check the proper voltage to use (V_{DD} selection, see section 3.5.1). In this example, we select (Figure 7-26) the following transmission values:

- Modulation Scheme. We select *Differential*.
- Modulation Type. We select *BPSK*.
- Tone Map. We select *0x3f*.
- Branch Configuration. We select *Auto*.
- TX Power. We select *Full_Gain*.
- Preemphasis. We select *0* and *Full_Gain*.

You can select the tone mask feature. It allows to disable carriers for each symbol as G3 specification tells. So if you want a tone with null amplitude select *Default* option for the tone mask parameter specified for Cenelec-A (36), FCC (72) and ARIB (54). Or *Custom* if you want to select other range frequencies. If you do not use the tone mask feature select *None*.

Click the Next button to continue.

Figure 7-27. TX Test Parameters tab.



Previous figure (Figure 7-27) shows the *TX Test Parameters* tab. This tab is where transmission test parameters are configured:

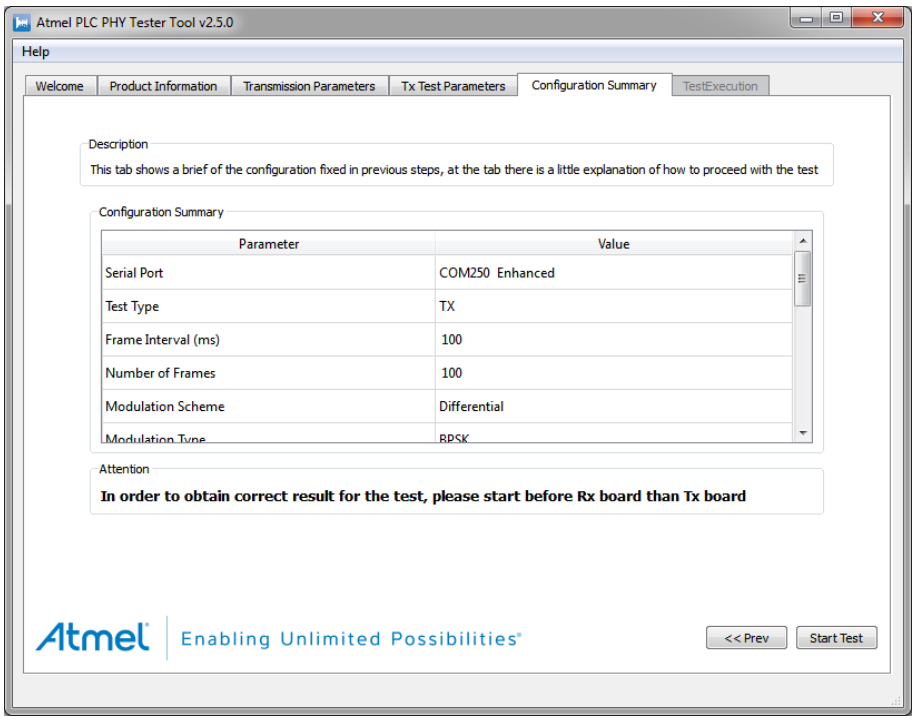
- Time Interval (milliseconds): desired interval between frame transmissions.
- Number of Frames: number of frames to be transmitted.
- Message: ASCII message to be transmitted.

These parameters **must match** the reception test parameters (Figure 7-22) for the test to be successful.

Default parameters are selected. Click the Next button to continue.

The next tab shows a table where all the configuration parameters and their selected values are listed. It is recommended to check that all values correspond to the desired configuration before continue.

Figure 7-28. Configuration Summary tab.



To start the process, click the Start Test button. A new tab, *Test Executions* (reports of TX process), will appear with the frame sent and the TX result of the transmission process.

Now you can observe the transmission and reception process in both *Test Executions* windows. If messages are different, the receiver will not recognize them as a valid. If the configured interval and number of frames are different, the statistics computed at the end of the test may be inaccurate. In both board's displays the transmitted/received messages are showed.

During the transmission process the TX led of the coupling board is toggled. You can use it to check if the PLC messages are sent.

When all frames are sent, both *Test Executions* windows show some statistics. See the following figures.

Figure 7-29. Transmission test result.

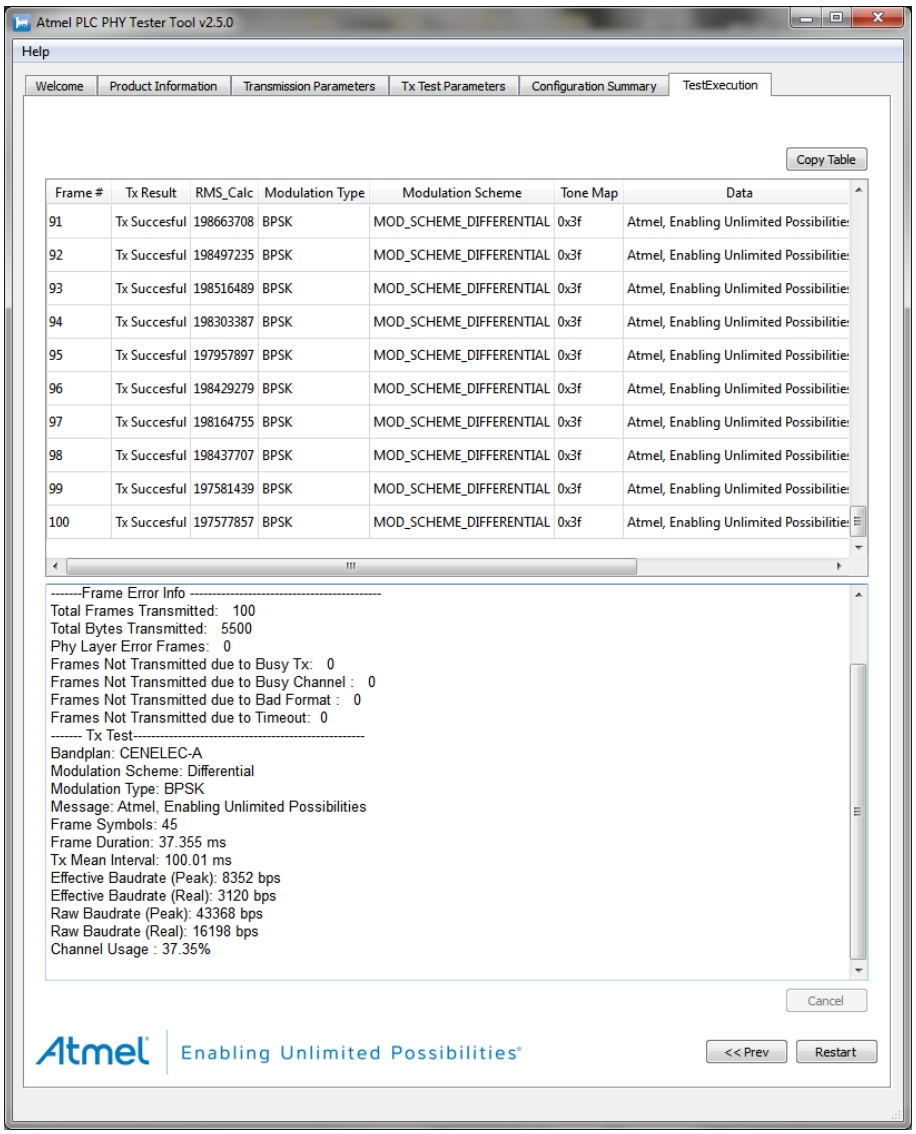
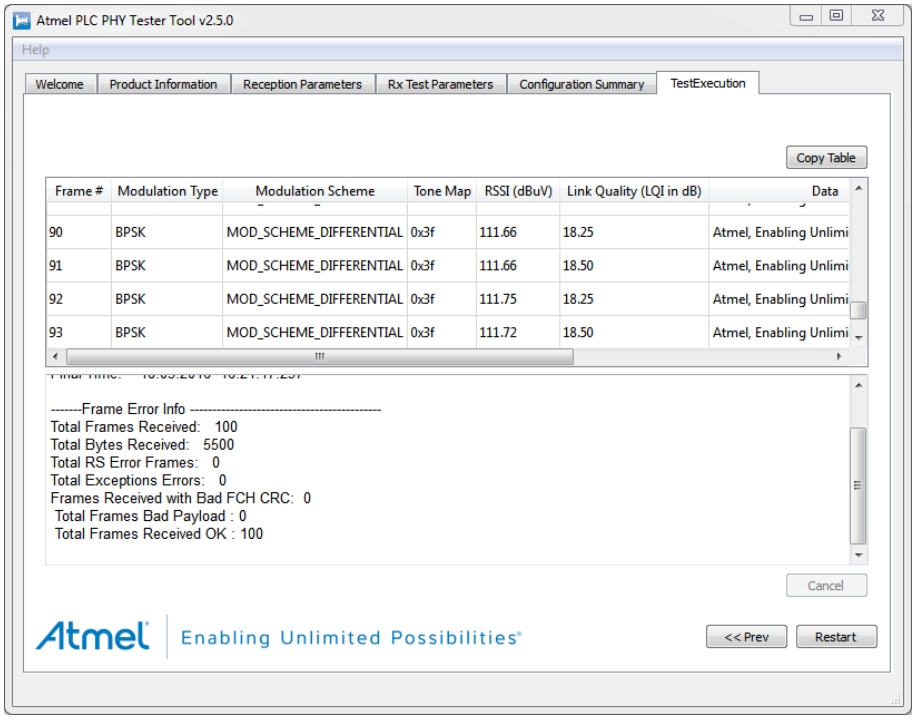


Figure 7-30. Reception test result.



While tests are executing, a row is added to the top table with information about the frame currently transmitted/received. The columns that contain these tables are the following.

Table 7-1. Transmission/Reception parameters showed in columns.

Transmission parameters showed		Reception parameters showed	
Parameter	**Description**	**Parameter**	**Description**
Frame #	It indicates the number of frame transmitted. It is useful to track the test progress.	Frame #	It indicates the number of frame received. It is useful to track the test progress.
Tx Result	It indicates the result of transmission. If an error occurs, a descriptive text will appear.	Modulation Scheme	It indicates if modulation scheme is differential or coherent.
Modulation Scheme	It indicates if modulation scheme is differential or coherent.	Modulation Type	It indicates the type of modulation: BPSK, QPSK, 8PSK or BPSK_ROBO.
Modulation Type	It indicates the type of modulation: BPSK, QPSK, 8PSK or BPSK_ROBO.	Tone Map	It indicates active sub-bands in the frame.
Tone Map	It indicates active sub-bands in the frame.	RSSI	It indicates the strength of the signal received in dBuV.
Data	It shows the message transmitted in ASCII format.	LQI	It is a parameter that indicates the mean SNR per carrier (dB).
Tx Interval	It is the interval of time between the transmission of the current frame and the previous one.	Data	It is the received info in ASCII format.
		Rx Interval	It is the interval of time between the reception of the current frame and the previous one.

Transmission parameters showed		Reception parameters showed	
		Payload Integrity	It shows if the content of the frame is correct or not.

After all frames have been transmitted/received, or the test has been cancelled, at the bottom of the tab it will appear a text box with information about the test. First of all, it will appear information about starting and ending time, this information is measured by the PC application.

After that, there is a section of information called *Frame Error* information that shows information about transmitted/received frames and possible errors. Finally another section shows a resume of the transmission/reception tests, this information contains much information as modulation scheme, message length, total frame received,… that is pretty straight forward but other fields must be explained. For that, please refer to the tool's embedded help (in the menu bar).

Once the values have been received, you can copy all values to check and analyze them by your own, clicking Copy Table button on the instances, the reception and transmission.

Click the Restart button to start the test again. It does first in the reception instance to avoid "lose" some frames.

The same TX/RX processes could be done using another ATPL coupling board. For that, after power down the ATPL250ABN, remove the ATPLCOUP007 board and set the new coupling board. Take into account that the new coupling board could require to set the jumper in J16 connector of the ATPL250BN board. Check the characteristics of the available ATPLCOUP boards. And even, you have to download over ATPL250ABN boards a new firmware build for the new coupling board in which the coupling board configuration has been changed (see Figure 7-14).

For further information about the tool, please refer to the tool's embedded help (in the menu bar).

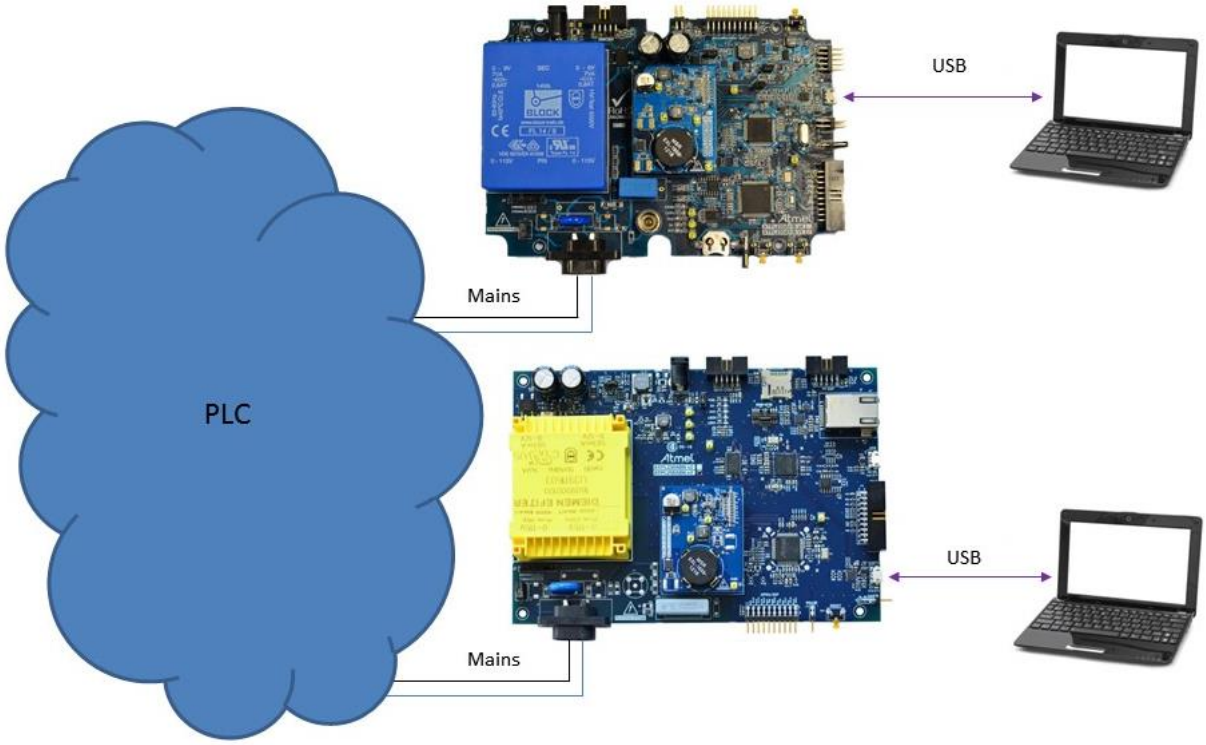
7.3 PLC application example 2 – PHY TX Test Console

This example explains how to use the project application called *APPS_PHY_TX_TEST_CONSOLE*. This application lets the user to configure a proper setup to perform both EMC emissions and immunity tests for ATPL250ABN board. These tests are based on the use of G3 PHY layer with a terminal console firmware (*apps_phy_tx_test_console.bin*) that eases the configuration of several transmission parameters such as modulation, frame data length and time interval between frames.

To run this example, two boards are used. So another Atmel board besides of ATPL250ABN is necessary to run this test, e. g, ATPL250AMB.

Following chapters explain to you how to supply the board, select the UART to communicate with the ATSAME70Q21, load the firmware and run the application. The setup is shown in the following figure.

Figure 7-31. Boards connection scheme.



7.3.1 Supplying the boards

Please refer to 7.2.2 in order to know how to supply the ATPL250ABN board.

7.3.2 USB connection

This application uses the UART1 of ATSAME70Q21 device. This UART is available in the Data Concentrator Expansion, J4, that connector is a 10-pin dual row male header. Please refer to 3.5.7.7 in order to know the description of the connector.

Atmel propose to use a USB to TTL serial cable which provides connectivity between USB (PC) and serial interfaces (board), e. g. TTL-232R-3V3-WE cable of FTDI.

Connect the USB to TTL serial cable to the host PC. If PC doesn't recognize the USB, download a USB driver from the USB cable manufacturer's web site. Once the driver is downloaded, unpack the driver archive to a folder on the host PC's hard-disk. Then, assign this new driver from Windows Device Manager.

7.3.3 Programming the embedded file

We have commented in section 7.2.4 the way to program a board.

Open the IDE tool used, Keil, Atmel Studio or IAR Embedded Workbench. Select the PHY sniffer tool project, *apps_phy_tx_test_console.atsln*, *apps_phy_tx_test_console.eww*, *apps_phy_tx_test_console_flash.uvprojx*, and now build it to generate the output file.

Remember that the J-Link USB drivers must have been downloaded previously from the Segger webpage (see section 7.1.5) and they depend on your operating system. In order to program the firmware on the board, set the JTAG probe, SAM-ICE, on the JTAG connector, J13 (see section about JTAG programming mode, 3.5.7.1).

Note that kits do not provide a J-Link ARM or SAM-ICE JTAG probe in order to connect to the user's host PC and the boards to download and debug the projects.

In case of programming with Atmel Studio IDE, select the interface to SWD to download the output file. By default, JTAG option is selected. That option is found in Tool tab of Device (ATSAME70Q21) button toolbar. See the Figure 7-13.

Remember that, PHY TX Test Console example project is contained in the following Software folder:
".\Software\G3_va.b.c\g3.workspace.same70q21_atpl250abn_v2\thirdparty\g3\phy\atpl250\apps\phy_tx_test_console\".

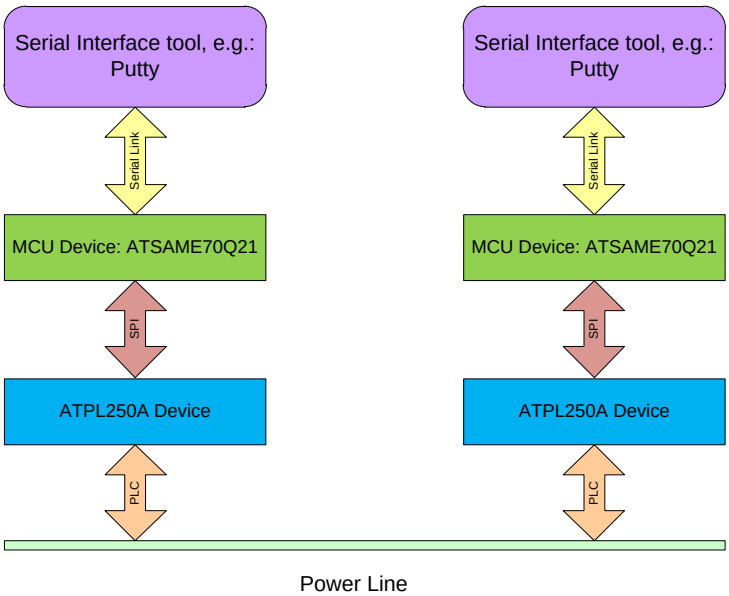
PHY TX Test Console project of *G3_va.b.c* folder has been created for CENELEC-A, FCC and ARIB bands, ATPLCOUP007v2.5, ATPLCOUP006v2 and ATPLCOUP002v2 PLC coupling boards. For FCC/ARIB option, select the project folder with suffix "_fcc" and open the project application, *apps_phy_tx_test_console.atsln*, *apps_phy_tx_test_console_flash.uvprojx* or *apps_phy_tx_test_console.eww*.

After that, you can select the file *conf_project.h*, that it is located in the following project directory: *"./Software\G3_va.b.c\g3.workspace.same70q21_atpl250abn_v2\thirdparty\g3\phy\atpl250\apps\phy_tx_test_console\same70q21_atpl250abn_fcc"*, find the define function to select the coupling board configuration (see Figure 7-14) and check that the frequency band name is the desired. Now, you can build project to generate the output file.

7.3.4 Running the PLC application example 2

As the PLC application example 1, boards are plugged to the mains, see Figure 7-31. Users have to execute an instance of the serial interface tool – which has been previously installed to the host PC – in order to enable communication between both boards. Please note that these two instances may or may not run on the same computer.

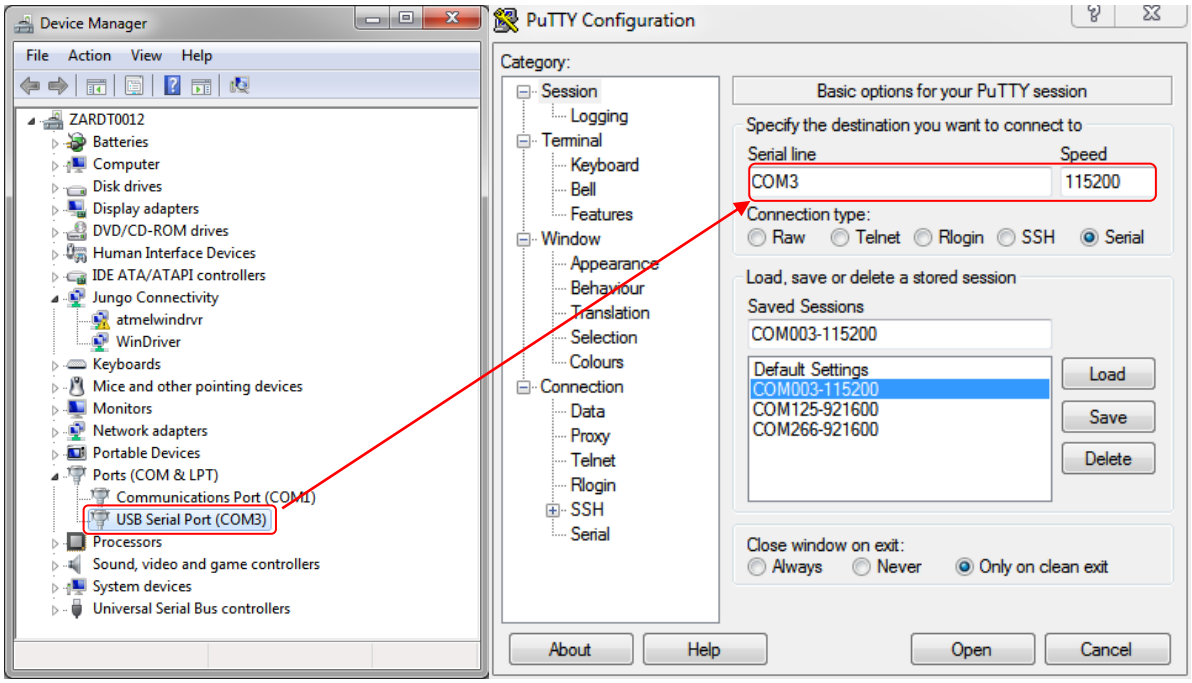
Figure 7-32. PHY TX Test Console concept.



For this example a serial interface tool is required. HyperTerminal is not installed on Windows 7. You can use a PuTTY terminal instead. Once you have the serial terminal in your computer, open *putty.exe* and

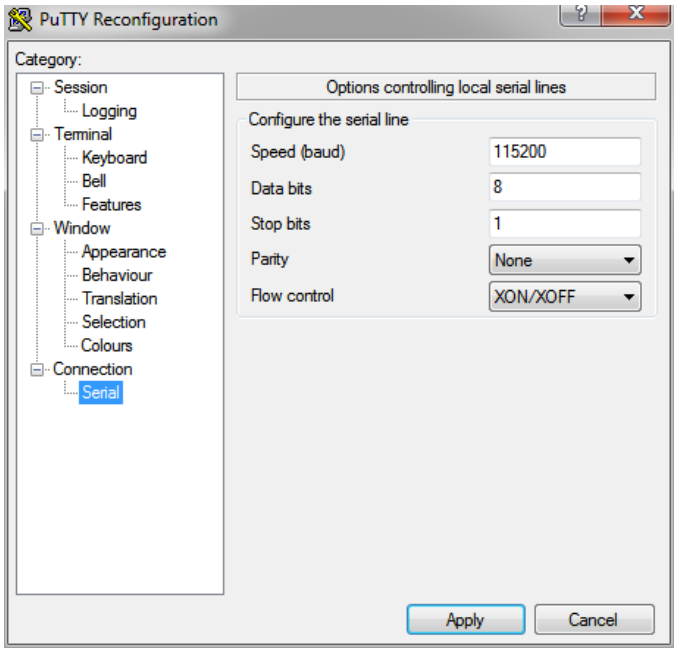
connect to the COM port number assigned to the USB cable (see Figure 7-33). As is commented in section 3.5.7.7, UART1 is available by Data Concentrator Expansion connector, J4, see Figure 3-2.

Figure 7-33. COM Port selection.



Set 115200 in the *Speed* field. In the *Serial* Category, change the *Flow Control* to None. The other fields should already be correctly configured. Finally, click Open.

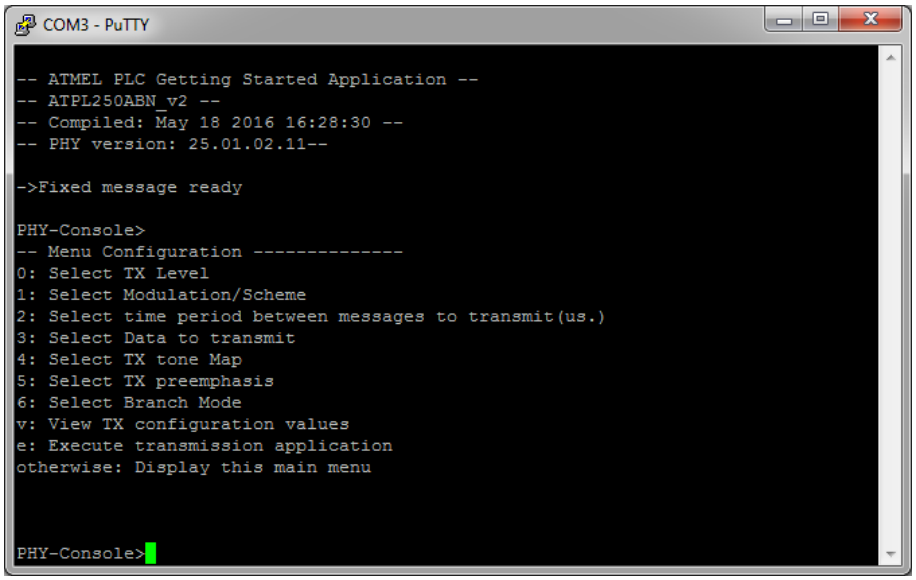
Figure 7-34. PuTTY Configuration instance.



Once board is supplied, leds LED0 and LED1 blink once at the same time, after that, green led D5, LED0, blinks quickly several times. Finally main menu is displayed (press Reset button in case board has been

supplied previously to connect USB cable) in the Terminal window and green led D5, LED0, blinks slowly indicating application is running properly.

Figure 7-35. Main menu.



The description of each field is the following:

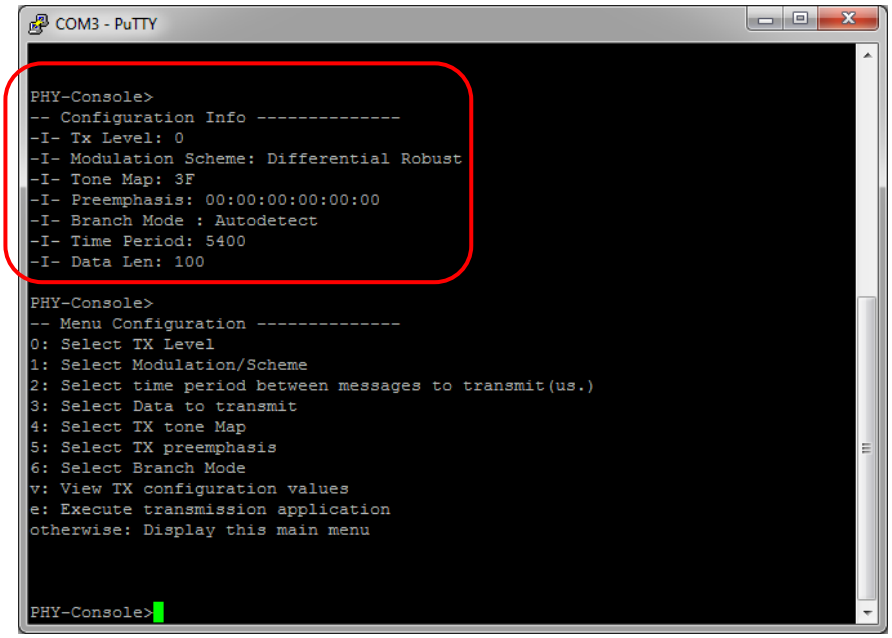
- **0: Select TX level** – 0 is 0dB of attenuation and every step increments the attenuation in 3dB. In the current firmware the maximum attenuation value is 10 (30dB). The value could be from 0 to 31 because it is defined in the G3 specification.
- **1: Select Modulation Scheme:** In this example we choose 3 that is Differential Robust.
- **2: Select time period between messages to transmit (µs).** 5400µs in this example.
- **3: Select data to transmit.** In this example we choose Random Data and 133 bytes. This value (133 bytes) is the maximum for Robust mode in CENELEC.
- **4: Select TX tone map**. 0x3F in this example.
- **5: Select TX preemphasis.** 0 in this example.
- **6: Select Branch Mode.** Autodetection in this example.
- **v: View Tx configuration values**. Press *v* key of keyboard to check default configuration.
- **e: Execute transmission application**. Press *e* key in the keyboard to begin transmission and reception mode in both boards. And press *x* key of keyboard to stop the transmission process.

Default configuration is configured for ready for EMC tests:

- TX level: 0. 0dB of attenuation.
- Modulation/Scheme: 3. It means Differential Robust.
- Data: 1. It is Random Data to transmit of 133 bytes. 133 bytes is the maximum for Robust mode in CENELEC.
- TX tone map: 0x3F.
- TX preemphasis: 0.
- Branch mode: Autodetection.
- Time period: 5400. 5400µs between messages to transmit.
- Data Len: 100 bytes

In *phy_tx_test_console.C* file are all the possible values of the parameters from main menu fields.

Figure 7-36. Default configuration menu.

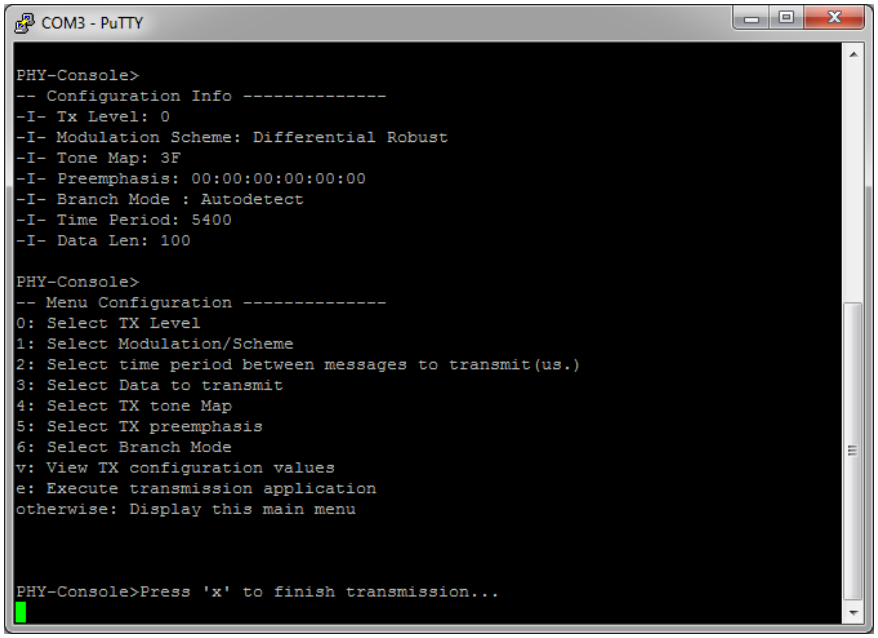


Type “e” to start the transmission and press “x” to stop the process.

Default configuration is configured for ATPLCOUP007 coupling board for differential modulation scheme in Robust mode with 133 data bytes length and 5.4 milliseconds time interval between PLC frames.

During the transmission, green led (LED0) is blinking indicating test is running. And the yellow led, PLC, on ATPLCOUP007 board blinks every time a PLC frame is sent. In the reception board, the red led (LED1) blinks in every PLC frame reception.

Figure 7-37. Transmission messages.



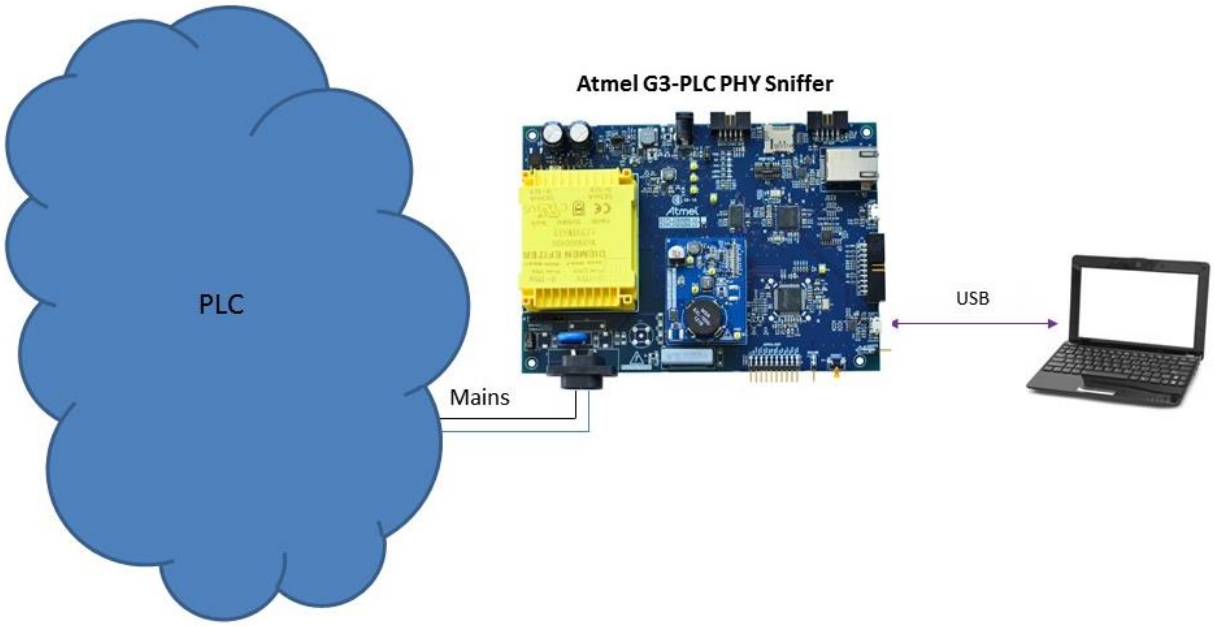
In case the configuration default has been changed, the board keeps the configuration unless power shutdown. If board is reset while keeping power supply on, it will restart the configuration mode after start-up.

7.4 PLC application example 3 – PHY Sniffer

In this example, we present you the G3 PHY Sniffer project, *APPS_PHY_SNIFFER_TOOL*. G3 PHY Sniffer project is able to monitor data traffic on the G3-PLC network by means of an ATPL250ABN board and the PC application, ATPL Multiprotocol Sniffer. For this example, only one ATPL250ABN board is required -and obviously a G3-PLC network to be tracked-.

The circuitry in the coupling boards has an influence in the reception itself. As a consequence, each coupling board is intended to be used in their corresponding frequency band(s) only. The application behaves properly when this correspondence is maintained.

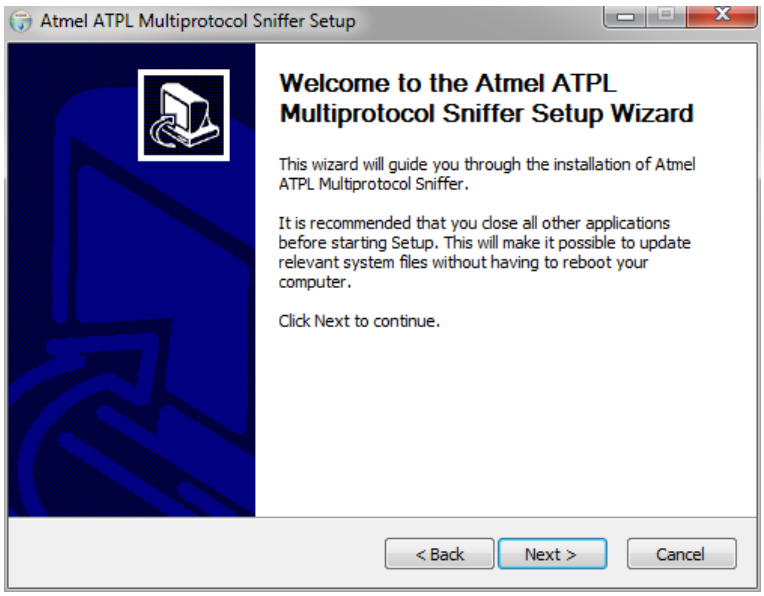
Figure 7-38. ATPL250ABN board connection scheme.



7.4.1 ATPL Multiprotocol Sniffer tool Installation

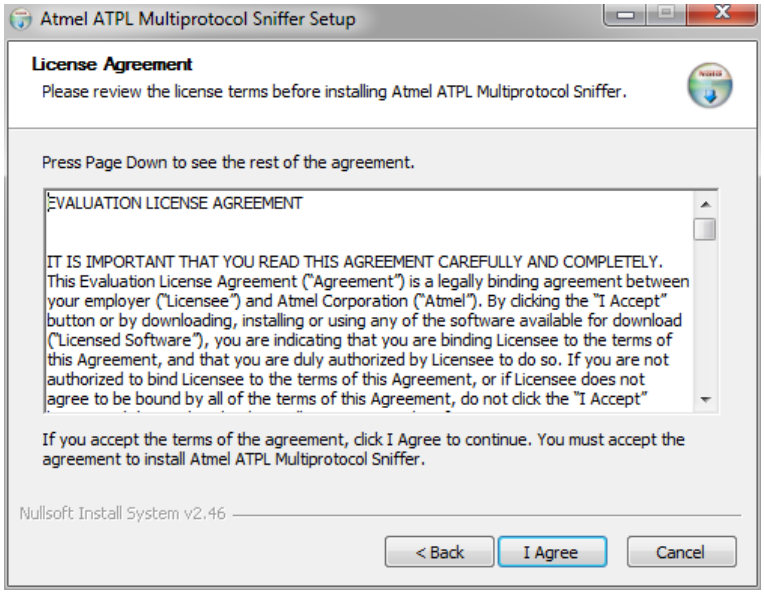
To install ATPL Multiprotocol Sniffer tool in a Windows Operating System, execute the provided installer in the PCTools folder *".\PCTools\ATPL_Multiprotocol_Sniffer\ATPL Multiprotocol Sniffer vX.Y.Z.exe"* and follow the installation wizard. The installer wizard should open. To follow the installation, click Next.

Figure 7-39. ATPL Multiprotocol Sniffer installation process, slide 1.



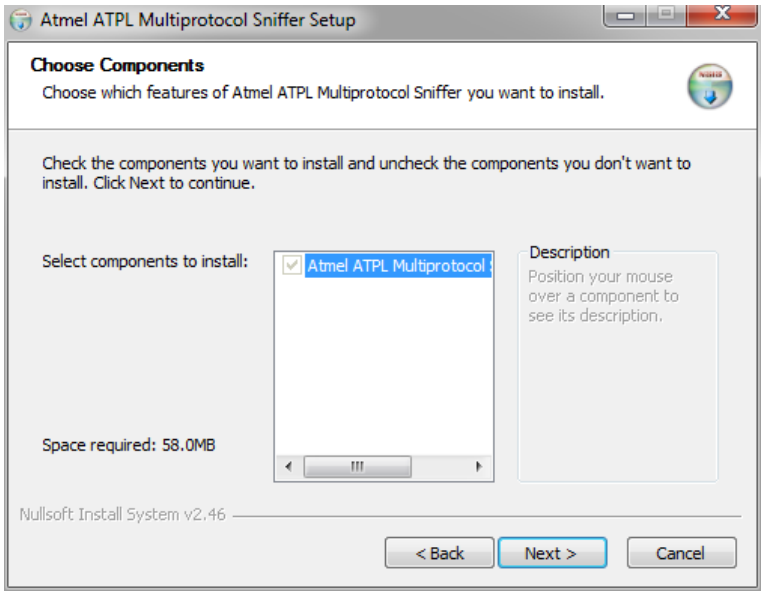
Select the users' permissions and click Next.

Figure 7-40. Installation process, slide 2.



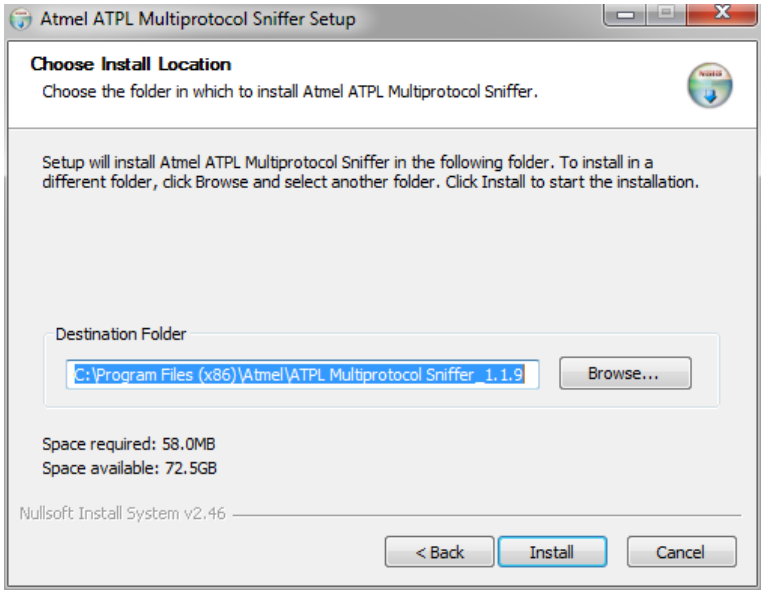
Read and accept term and conditions expressed in the End User License Agreement. Click I Agree to continue.

Figure 7-41. Installation process, slide 3.



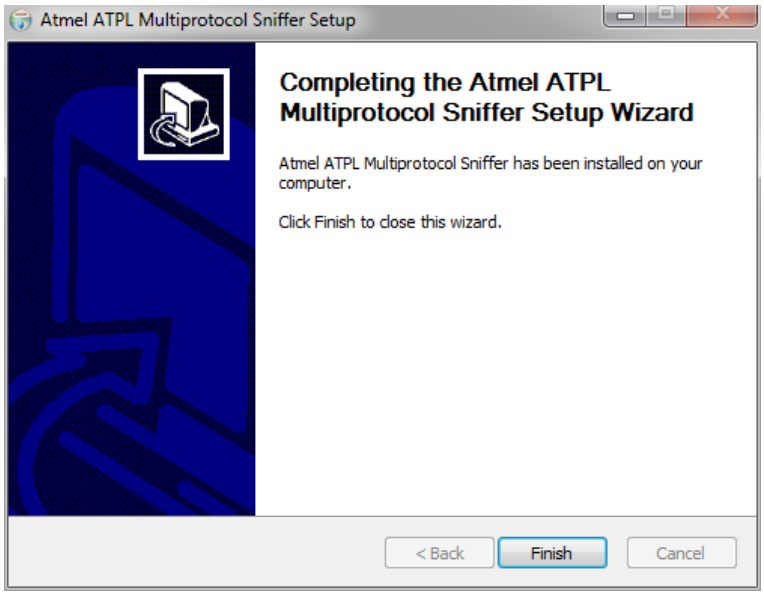
Click Next to install the component selected.

Figure 7-42. Installation process, slide 4.



Setup will install the program in the *Destination Folder*. To install in a different folder, click Browse and select your destination folder. Click Install to start the installation process.

Figure 7-43. Installation process, slide 6.



Click Finish.

Now the program is installed in your computer and a shortcut should have been created in your desktop.

7.4.2 Supplying the boards

Please refer to 7.2.2 in order to know how to supply the ATPL250ABN board.

7.4.3 USB connection

This application uses UART0, please refer to 7.2.3 in order to know how to connect the micro USB cable with the ATPL250ABN board.

7.4.4 Programming the embedded files

We have commented in section 7.2.4 the way to program a board. To program the board as PLC sniffer, process will be the same: building the IDE project and downloading into the board.

Open the IDE tool used, Keil, Atmel Studio or IAR Embedded Workbench. Select the project *apps_phy_sniffer_tool.atsln* or *apps_phy_sniffer_tool.eww* or *apps_phy_sniffer_tool_flash.uvprojx* and build it to generate the output file. Now you can download the file to the board.

To be able to develop applications, build binaries and program the firmware on the SAM4C16C device, you can use the IAR Workbench, Keil µVision or Atmel Studio.

Remember that the J-Link USB drivers must have been downloaded previously from the Segger webpage (see section 7.1.5) and they depend on your operating system.

In order to program the firmware on the board, set the JTAG probe, SAM-ICE, on the JTAG connector, J13 (see section about JTAG programming mode, 3.5.7.1).

In case of programming with Atmel Studio IDE, select the interface to SWD to download the output file. By default, JTAG option is selected. That option is found in Tool tab of Device (ATSAME70Q21) button toolbar. See the Figure 7-13.

Note that kits do not provide a J-Link ARM or SAM-ICE JTAG probe in order to connect to the user's host PC and the boards to download and debug the projects.

Remember that, PHY TX Console example project is contained in the following Software folder:
".\Software\G3_va.b.c\g3.workspace.same70q21_atpl250abn\thirdparty\g3\phy\atpl250\apps\phy_sniffer_tool".

As we commented in a previous sections, every coupling board is intended to be used in their corresponding band(s) only. By default, sniffer project is compiled for ATPLCOUP007 board. This means that only CENELEC-A frequency band is supported.

PHY Sniffer project of *G3_va.b.c* folder has been created for CENELEC-A, FCC and ARIB bands, ATPLCOUP007v2.5, ATPLCOUP006v2 and ATPLCOUP002v2 PLC coupling boards. For FCC/ARIB option, select the project folder with suffix "_fcc" and open the project application, *apps_phy_sniffer_tool.atsln*, *apps_phy_sniffer_tool.eww* or *apps_ phy_sniffer_tool_flash.uvprojx.*

After that, you can select the file *conf_project.h*, that it is located in the following project directory:

".\Software\G3_va.b.c\g3.workspace.same70q21_atpl250abn_v2\thirdparty\g3\phy\atpl250\apps\phy_sniffer\same70q21_atpl250abn_fcc", find the define function to select the coupling board configuration (see Figure 7-44). Change the frequency band name to desire and build to generate the output file.

Figure 7-44. Frequency band configuration definition.

```
/* Configuration constants */

// Work Band
#define CONF_CENELEC_A
//#define CONF_FCC
//#define CONF_ARIB
```

Check the Table 3-1 for the characteristics of the available ATPLCOUP boards.

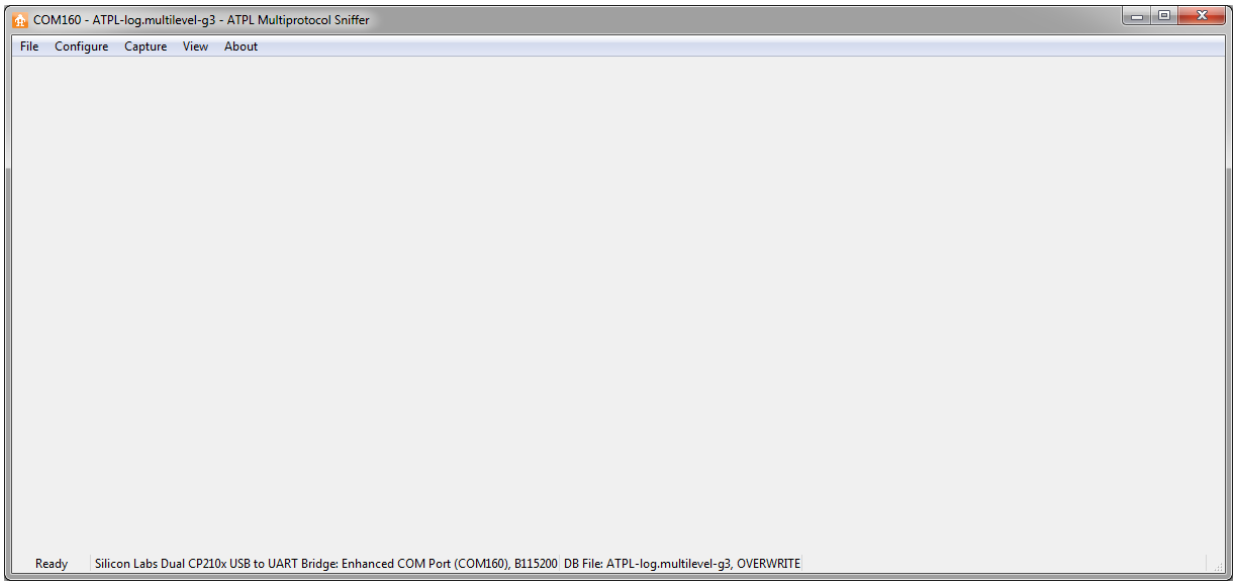
7.4.5 Running the PLC application example 3

As you can see in Figure 7-38, the sniffer board is plugged into the same power line. Users have to execute an instance of the ATPL Multiprotocol Sniffer tool – which has been previously installed in the host PC – in order to enable communication between the sniffer board and the PC. The ATPL Multiprotocol Sniffer tool is used to monitor data traffic on the network. You can also use the ATPL Multiprotocol Sniffer tool to monitor

the PLC messages which they do not belong the G3 standard then the messages will be showed in red color and without PduType.

The main window of the Sniffer PC interface is shown in Figure 7-45.

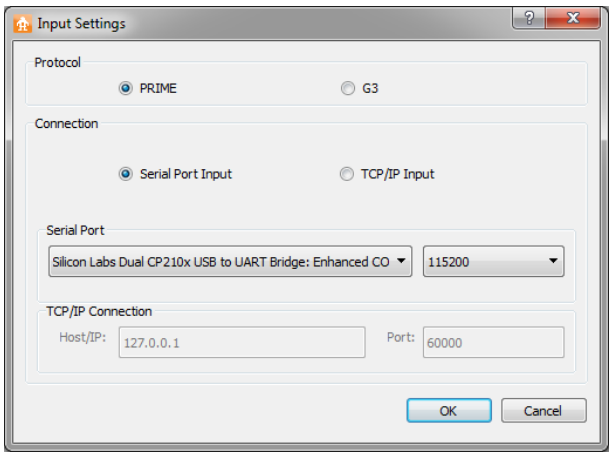
Figure 7-45. ATPL Multiprotocol Sniffer tool window.



Once the application is launched, the COM port for the board needs to be configured. The COM port selection window is available by choosing Configure>Input (Ctrl+I). A new window *Input Settings* will appear as shown in Figure 7-46.

First of all, select the Power Line Communication protocol, in this case G3. After that select the COM port and set the speed. The default port is UART0 (enhanced COM port) and the speed for this application is 115200 bauds. Also, this tool is able to connect to a remote device through the TCP/IP protocol.

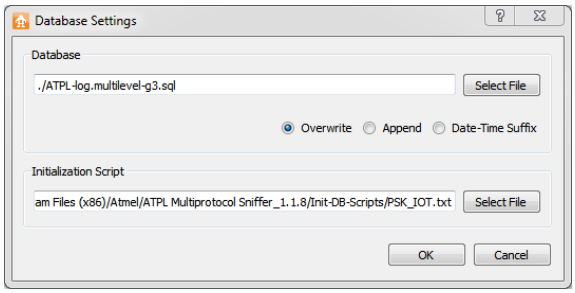
Figure 7-46. Input Settings window.



The database file to store the traffic must be configured. If output logs are required and the location to store these choose Configure>Database… (Ctrl+D). A new window *Database Settings* will appear as shown in Figure 7-47, select the file name and click OK button. Database files can hold longer logs without having to split them in pieces. Also log stored files can be opened to review the file. The three options when you create a log database depends on if you want to keep the previous data or not. And it is possible to build your own scripts (for example, in Python) to analyze the data.

Besides of the log database, there are a set of scripts supplied along the ATPL Multiprotocol Sniffer that prepares the database to be able to decode all the messages sent in the Interoperability tests defined by the G3-PLC Alliance.

Figure 7-47. Database Settings window.

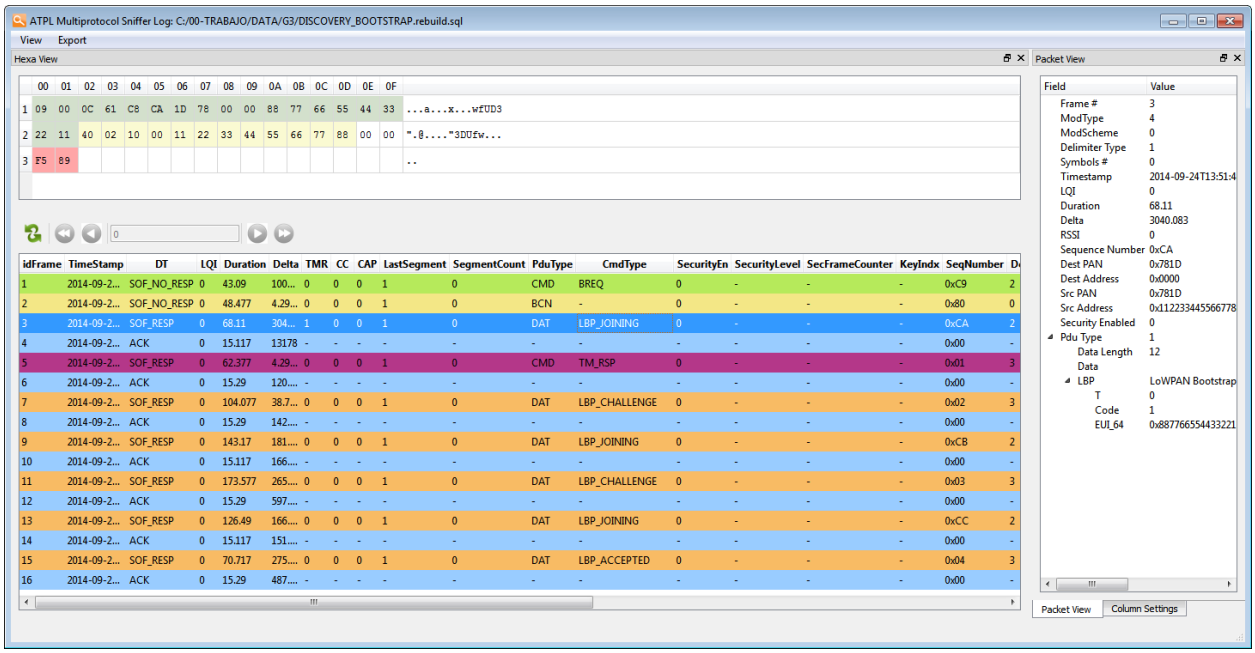


At this point, the tool is ready to start capturing data. If board is not powered, this is the point to supply it.

Click on the menu Capture>Start to begin logging data.

If tool establishes the communication with the COM port of the ATPL250ABN, the status bar at the bottom of the window will show the current setup and status of the tool. On a G3-PLC network the main window will look like as the Figure 7-48. Main window displays a table with the current log. It is updated in real time as frames are received from the hardware sniffer.

Figure 7-48. ATPL Multiprotocol Sniffer tool main window.



The capture window has a tool bar with four commands (see Figure 7-49):

- Pause command will stop the update of the scroll view, while the logging process will continue.
- To restart showing the live stream of PDUs, click Play button.

Figure 7-49. Tool bar.

Main window displays a table with the current log. It is updated in real time as frames are received from the hardware sniffer. The data shown are: idFrame, Timestamp, ModType, ModScheme, Delimiter Type, Symbols, SNR, RSSI (in db/µV), Duration, Delta, Tone Map Request, Contention Control, Channel Access Priority, Last Segment Flag, SegmentCount, PduType, CmdType, SecurityEn, SecurityLevel, SecFrameCounter, KeyIndx, SeqNumber, PanIdCompression, DestAddrMode, SrcAddrMode, DestPAN, SrcPAN, DestAddress, SrcAddress, Length, Pdu, headerLen and payloadLen.

While the PLC traffic is logged into a database, the software tries to infer the PLC network structure and status as seen by the PAN coordinator. This information is shown in several docking views. They are available on the menu View:

- Hexa view shows the hexadecimal display of the selected frame in the main view.
- Packet view shows the disassembled data of the selected frame in the main window. All the specified fields on the G3 specification are shown.
- Filter view allows selecting the frames shown in the main view table.

> To uninstall the ATPL Multiprotocol Sniffer tool from your computer, go to *Start>All Programs>ATMEL>ATPL Multiprotocol Sniffer vX.Y.Z>Uninstall*.

For further information, please refer to the tool's embedded help (in the menu bar).

7.5 Introduction to G3 Stack

PLC is a medium with such special characteristics (asymmetry, noise variation in time, etc.) that make it a hostile environment for successful communication when users are not familiar with these issues.

On the PHY level, G3-PLC is based on the OFDM modulation technique. OFDM can efficiently utilize limited bandwidth channels allowing the use of advanced channel coding techniques. This combination facilitates a very robust communication over a power line channel in presence of narrowband interference, impulsive noise and frequency selective attenuation.

OFDM supports differential modulations (DBPSK, DQPSK, and D8PSK) and coherent modulations (BPSK, QPSK, 8-PSK) and also robust modes to use in CENELEC, FCC and ARIB bandplans (10 kHz - 490 kHz). In G3-PLC, convolutional, Reed-Solomon and CRC16 coding provide redundancy bits allowing the receiver to recover lost bits caused by background and impulsive noise. And also other techniques as adaptative tone mapping, notching and modulation provide very robust power line communications.

On top of the PHY layer, the G3-PLC MAC and ADP layers provide the conditions for fast and secure communication by use of advanced routing techniques through hopping via devices in the network. The ITU-T G.9903 data link layer specification comprises these two layers:

- The MAC layer based on IEEE 802.15.4.
- The adaptation layer based on IETF RFC 4944.

In the following sections there are basic overviews of the Atmel libraries used and the description of the whole system integration (FreeRTOS, G3-PLC stack, ATPL250A and the SAME70) in a G3 project using the ASF structure.

7.5.1 FreeRTOS

FreeRTOS is a real-time kernel (or real-time scheduler) on top of which Cortex-M3/M4 microcontroller applications can be built to meet their hard real-time requirements. It allows Cortex-M3/M4 microcontroller applications to be organized as a collection of independent tasks to be executed. The kernel decides which task should be executed by examining the priority assigned to each by the application designer. In the simplest case, the application designer could assign higher priorities to tasks that implement hard real-time

requirements, and lower priorities to tasks that implement soft real-time requirements. This would ensure that hard real-time tasks are always executed ahead of soft real-time one.

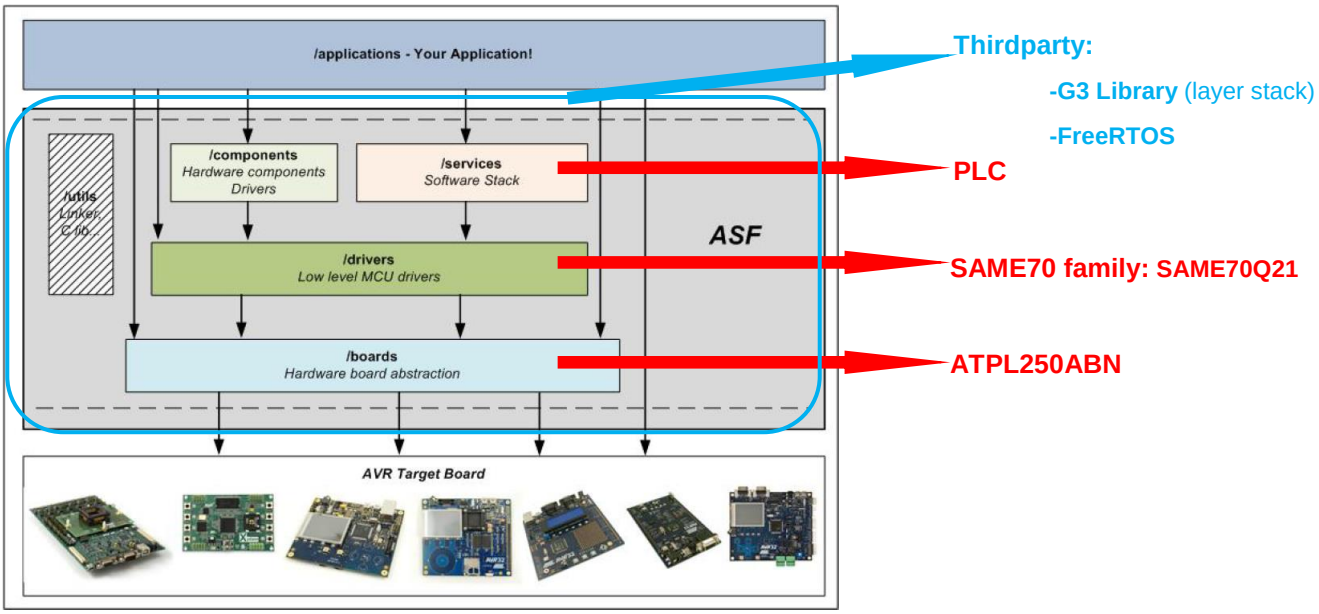
Thanks to the FreeRTOS scheduler we are able to optimize G3-PLC code and memory usage.

Please take into account that the provided RTOS support is just an example of integration of the stack in an RTOS. It is functional, but Atmel does not ensure the same reliability and performance as the microcontroller mode implementation, as the latter is the reference implementation.

7.5.2 ASF Integration

As it was explained before, ASF has a defined structure. ASF root folder contains the *common/* directory, the *sam/* directory and the *thirdparty/* directory. The components contents of thirdparty directory are showed in the following figure. That is the way to integrate the whole platform in this structure (ATPL250ABN, SAME70, PLC, G3-PLC and FreeRTOS).

Figure 7-50. SAME70 & G3 Integration in thirdparty folder.



We integrate the different parts according to the ASF structure:

- Boards: The ATPL250ABN board hardware mapping is defined here.
- Drivers: The drivers for the SAME70 Family.
- Services: We offer the PLC modem as a service.
- ThirdParty: We add in this point the G3 and FreeRTOS libraries.

Could be possible that the last version of the Atmel Software Framework provided in the web link does not coincide with the PLC libraries of the projects from the kit's Software folder.

You can check the versions of G3-PLC software provided in the kit in *g3_stack_version.h* file. Also, PHY layer version in *atpl250_version.h* file.

Take into account, previous to download futures releases of ASF, if it is supported by these kit's version boards.

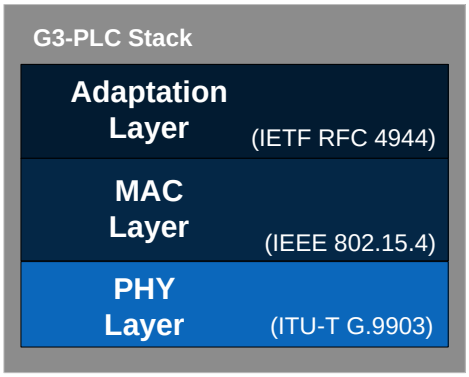
In case you do not know the ASF version downloaded in Atmel Studio, go to Help>Atmel Studio. Select in the combo box of the new window the component: *Atmel Software Framework*. After that, all the versions installed are showed.

7.5.3 Atmel G3-PLC Stack Structure

The Atmel G3 firmware stack follows a layered approach based on G3-PLC specification. The Figure 7-51 shows the G3 stack's architecture. The stack modules are from the bottom up:

- PHY Layer.
- MAC Layer.
- Adaptation Layer.

Figure 7-51. G3- PLC stack.



The Atmel G3 stack is able to run on a system with an OS (the OS Wrapper is an abstraction layer so different OSS can be used), or without it, running in microcontroller mode (mode by default).

The OS intends to transform the microcontroller-mode operation into a task-mode operation typical of operating systems. In order to do that, it creates and manages a single task where all active layers and interfaces are included. The user does not need to take care of controlling how the G3 stack is running and can create their applications normally. The current implementation of the OSS is based on FreeRTOS but the user could modify it appropriately to use any other RTOS.

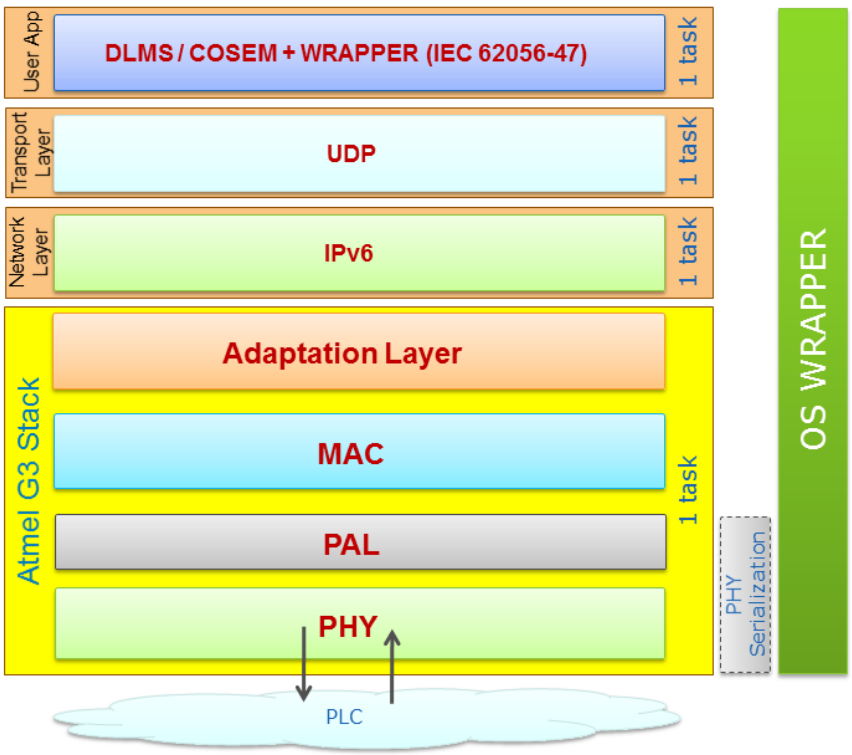
The Atmel G3 stack is according to the following architecture:

- PHY Layer. PHY layer is in charge of frame transmission and reception, this layer will be interrupt driven with events coming from PLC modem. Interrupt events will occur while transmitting and receiving frames using PLC modem. Apart from these events, PHY layer will implement entry functions in order to transmit a frame using the PLC modem, and to access the PHY Information Base (PIB) to read, write, or modify parameters.
- PAL. This layer abstracts the interface of the ATPL250A PHY Layer developed by Atmel and provides an interface compliant with the G3 PHY and MAC layers, and is in charge of communicating both layers properly. It will implement primitives to inform the MAC layer of events coming from PLC. Apart from these tasks, PAL will directly address function calls from MAC to transmit a frame to PHY layer. The same will occur with MAC calls to PLME functions, which will be directly addressed to PHY functions related to PIB access.
- MAC and Adaptation Layers. These layers will run together in 1 OS task (if OS is used), along with the PHY layer. MAC layer will access PHY layer using an intermediate PAL described above. It will implement the API defined in G3-PLC specification for the upper layer (Adaptation Layer). MAC implements the following tasks:
  - Channel access with CSMA-CA.
  - High and normal priority.

  - Segmentation of big packets.
  - Segment acknowledgement and retransmission of lost segments.
  - Network scan.
  - Transmission robustness management.
- Adaptation layer will access MAC layer below, and will implement the API defined in G3-PLC specification for the upper layer (IPv6 Layer) so any implementation of IPv6 can be used above it. ADP implements the following tasks:
  - Handles the device authentication and encryption key distribution.
  - IPv6 headers compression / decompression.
  - Fragmentation / reassembly of the IPv6 packets.
  - Controlling broadcast / multicast propagation.
  - Routing a message into the network.
  - Discovery and maintenance of the routes into the network.
- IPv6, UDP and DLMS Layers. These layers are generic and not directly related to G3-PLC protocol. These layers will run each one on a separate OS task (if OS is used), to make it possible to extract or insert any of them on the stack. Also for this purpose, each layer will provide the API defined in the corresponding standard.
- Serialization Layers. Serialization will be available on PHY layer. Serialization of PHY layer will act as the PAL layer, but communicating with a Serial Port Service, instead of the MAC. PHY Tester and PHY Sniffer projects use this serialization to communicate with the PC.

The following figure shows the architecture of the Atmel G3 software stack to be placed over the ATPL250A platform.

Figure 7-52. Atmel G3-PLC software Stack overview.



For more information about the Atmel G3 Firmware Stack see the doc43081 and the G3-PLC specification.

7.6 PLC application 4 – PLC Network

In this chapter the example proposed is used to show the capabilities of the ATPL250A in a network of smart devices. One ATPL250ABN board acts as a PAN Coordinator, i.e. the device that controls the whole network, whereas the other one, e. g. ATPL250AMB board acts as a PAN Device.

To run this example, a minimum of two boards are used. So another Atmel board besides of ATPL250ABN is necessary to run this test, e. g, ATPL250AMB.

Atmel provides a G3 PLC library with PAN Coordinator features, *APPS_DLMS_EMU_COORD_APP* application, such as creating the Network and accepting all Network Join from the Devices. This way, it is possible to build a network so data can be exchanged.

APPS_DLMS_EMU_COORD_APP and *APPS_DLMS_EMU_DEV_APP* are template applications intended to hold the application code developed by the user along with the Atmel G3-PLC Stack. So the user can integrate his application code in the firmware package delivered by Atmel. They are provided for IAR and Atmel Studio.

Following sections explain to you how to install the PC tool, select the projects, supplying the boards, select the COM ports to communicate with the SAME70Q21 and run the application.

7.6.1 Supplying the boards

Please refer to 7.2.2 in order to know how to supply the ATPL250ABN board.

7.6.2 USB connection

Please refer to 7.2.3 in order to know how to connect the micro USB cable with the ATPL250ABN board.

7.6.3 Programming the embedded files

It is commented in section 7.2.4 the way to program a board. To program the board as PAN Coordinator will be the same: building the IDE project and downloading into the board

Open the IDE tool used, Atmel Studio, Keil or IAR Embedded Workbench. Select the PAN Coordinator project, *APPS_DLMS_EMU_COORD_APP.atsln*, *APPS_DLMS_EMU_COORD_APP_FLASH.uvprojx* or *APPS_DLMS_EMU_COORD_APP.eww*, and now build it to generate the output file.

Remember that, DLMS Emulation Coordinator example project is contained in the following Software folder:
".\Software\G3_va.b.c_CENELEC\g3.workspace.same70q21_atpl250abn_v2\thirdparty\g3\apps\dlms_emu_coord_app".

Note that kits do not provide a J-Link ARM or SAM-ICE JTAG probe in order to connect to the user's host PC and the boards to download and debug the projects.

Remember that the J-Link USB drivers must have been downloaded previously from the Segger webpage (see section 7.1.5) and they depend on your operating system.

In order to program the firmware on the board, set the JTAG probe, SAM-ICE, on the JTAG connector, J13 (see section about JTAG programming mode, 3.5.7.1).

In case of programming with Atmel Studio IDE, select the interface to SWD to download the output file. By default, JTAG option is selected. That option is found in Tool tab of Device (ATSAME70Q21) button toolbar. See the Figure 7-13.

Note that the firmware provided for this example is only for Atmel PAN Coordinator, ATPL250ABN. To show all features and run the application, an Atmel PAN Device is required, i.e. ATPL250AMB. Which it must be programmed with the respective application, *APPS_DLMS_EMU_DEV_APP*. See ATPL250A-EK for more information.

G3 PAN Coordinator project of *G3_va.b.c* folder has been created for CENELEC-A, FCC and ARIB bands, ATPLCOUP007v2.5, ATPLCOUP006v2 and ATPLCOUP002v2 PLC coupling boards. For FCC/ARIB option, select the project folder with suffix "_fcc" and open the project application.

After that, you can select the file *conf_project.h*, that it is located in the following project directory:

".\Software\G3_va.b.c\g3.workspace.same70q21_atpl250abn_v2\thirdparty\g3\apps\same70q21_atpl250abn_v2_fcc", find the define function to select the coupling board configuration (see Figure 7-53). Change the frequency band name to desire and build to generate the output file.

Figure 7-53. Coupling board configuration definition.

```
/* Configuration constants */

// Work Band
#define CONF_CENELEC_A
//#define CONF_FCC
//#define CONF_ARIB
```

Check the Table 3-1 for the characteristics of the available ATPLCOUP boards.

Please, make sure all nodes (PAN Coordinator and PAN Devices) have valid and different between them EUI64 addresses. An invalid EUI64 makes a node unable to register.

7.6.3.1 Setting EUI64 number

Every device in a G3 network needs a unique EUI64 to be identified.

Every device in a G3 network needs a unique EUI64 to be identified. Mechanism to store expected sequence and EUI64 in flash memory is not provided, as it is expected to be done when flashing the device.

This EUI64 (or extended address) is stored in the variable *CONF_EXTENDED_ADDRESS[8]*, which has a default value. If more than one PAN Device is used, different Extended Address has to be configured for each one, so, change the value of the variable *CONF_EXTENDED_ADDRESS[8]* that can be found in file oss_if.c before compiling and load the project for every board.

For more information about EUI64 mechanism see doc43081.

Take into account that implementation reads the data from a reserved area in flash memory and if a certain sequence is found, default value for EUI64 is kept. So, if you want to change the EUI64 of a board, you have to execute the EUI64 script file.

J-Link Commander can also be used in script mode that allows the user to use this application for batch processing and without user interaction. When using J-Link commander in script mode, the path of a script file is passed to it. The syntax in the script file is the same as when using regular commands in J-Link commander (one line per command).

To do easier to load the EUI64, Atmel provides you a script, *writeEUI64_SAME70Q21.bat*, that lets you download the EUI64 in the right memory address position. You can find them in the following directories: *"\Software\G3_va.b.c\Scripts\EUI64"*.

writeEUI64_SAME70Q21.bat file code:

```
"c:\Program Files (x86)\SEGGER\JLink_V496b\JLink.exe"
writeEUI64_SAM4C16C.jlink
```

Edit the path to JLink.exe according to your installation folder and J-Link version.

writeEUI64_SAME70Q21.jlink file code:

```
exec device = ATSAME70Q21 //device
speed 0
r //reset
h //halt
//load bin files
loadbin eui64.bin, 0x010FFF00
r //reset
g //go
qc //quit and close
```

Eui64.bin file:

```
aa 55 11 22 33 44 55 66 77 88
```

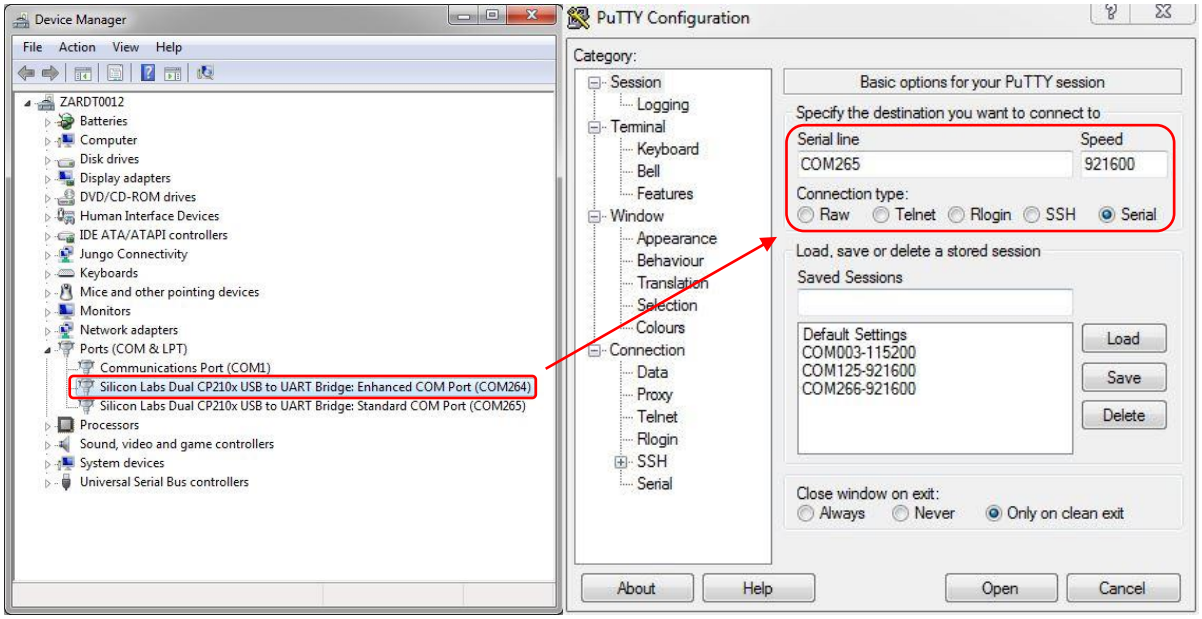
Edit the eui64.bin according to your desired EUI64 number with an HEX editor. Default number is: 1122334455667788. Add “aa55” prefix to EUI64.

7.6.4 Running the PLC application example 4

As you can see in Figure 7-54, the boards are plugged into the same power line. In this PLC example, ATPL250ABN board is the PAN Coordinator and the other ones are the PAN Devices. And users have to execute an instance of the serial interface tool – which has been previously installed to the host PC – in order to enable communication with Coordinator board. In this example, please note that it is only necessary to establish a serial connection between the board acting as a PAN Coordinator and the host PC, so only one instance is required.

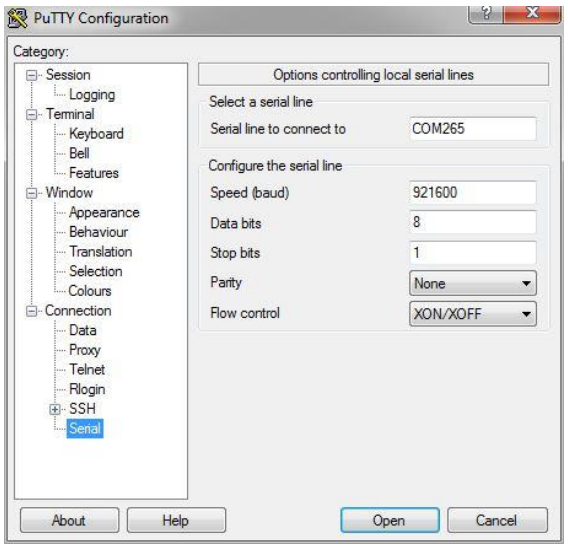
For this example a serial interface tool is required. HyperTerminal is not installed on Windows 7. You can use a PuTTY terminal instead. Once you have the serial terminal in your computer, open *putty.exe* and connect to the COM port number assigned to the micro-B USB cable (see Figure 7-54). As is commented in section 7.3.2, UART1 CMOS signals are also in the Data Concentrator Expansion connector, J4, see Figure A-10.

Figure 7-54. COM Port selection.



Set 921600 in the *Speed* field. In the *Serial* Category, change the *Flow Control* to None. The other fields should already be correctly configured. Finally, click Open.

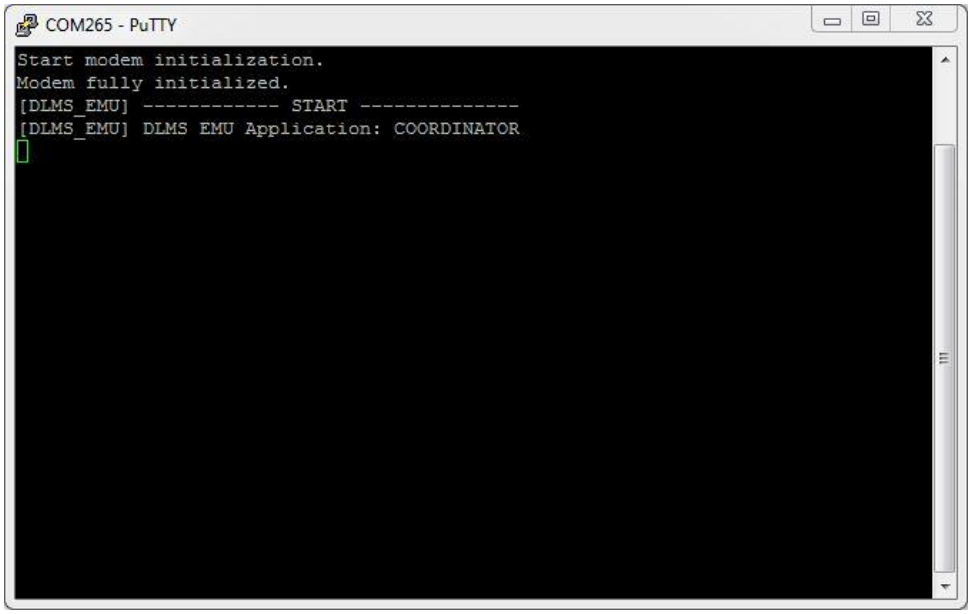
Figure 7-55. PuTTY Configuration instance.



Once the PAN Coordinator and PAN Device boards are programed and powered, the green led D5, LED0, are blinking to indicate the DLMS EMU application is running. And red led D6, LED1, flashes when receives a PLC message. Also when the PAN Coordinator and PAN Device send a PLC message, the TX led of the coupling board (ATPLCOUPxxx) is flashed. You can use these LEDs to check if the application in board is running and PLC messages are sent properly.

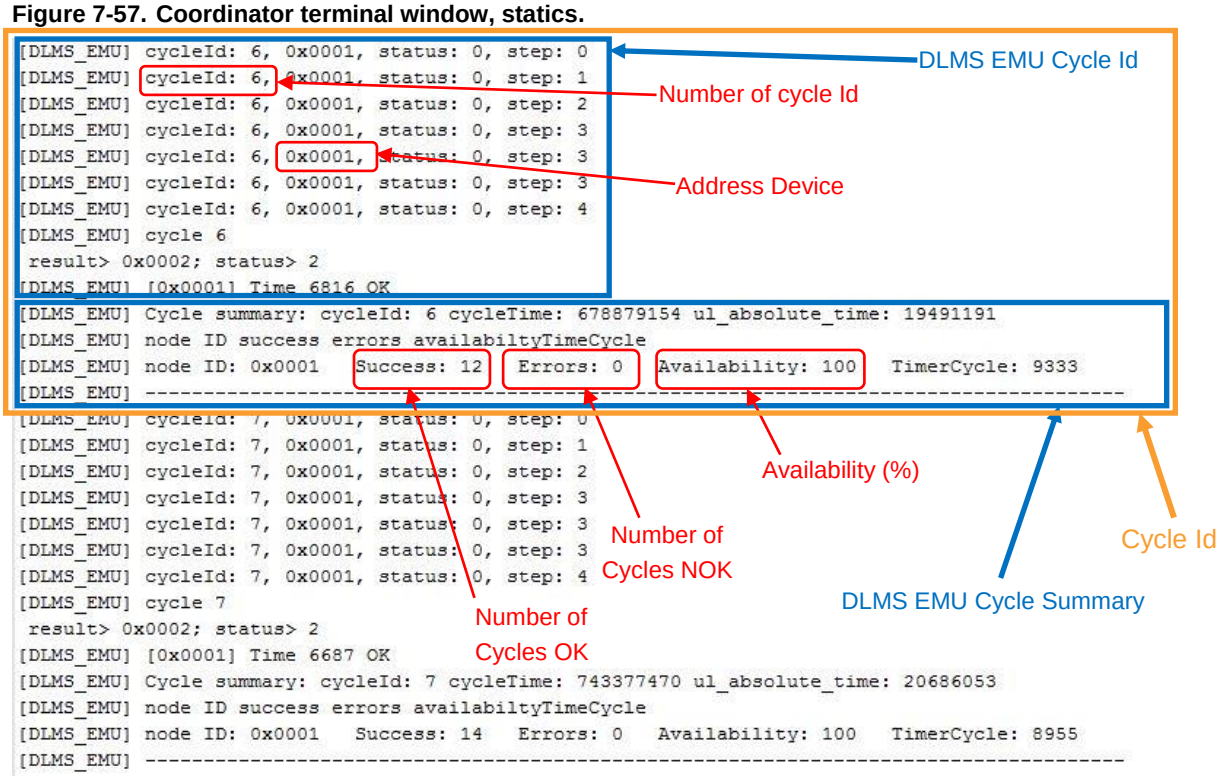
In the Terminal window, main menu is displayed (press Reset button in case board has been supplied previously to connect USB cable), see Figure 7-56. Once coordinator board has been supplied after 4 minutes (time defined in dlms_emu_coord.h) to the bootstrap process it starts the cycle process.

Figure 7-56. Coordinator terminal window, main menu.



After this point, statics will appear on the terminal, see Figure 7-57.

Figure 7-57. Coordinator terminal window, statics.



If the PAN Device is not an Atmel board, only runs the bootstrap process, due to DLMS emulation process will be ignored.

For more information about the DLMS Emulation procedure see the Atmel G3 Firmware Stack, doc43081.

8. References

[1] CENELEC, EN 50065-1. Signaling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz.

[2] FCC Part 15 Subpart B.

[3] Narrowband OFDM PLC specifications for G3-PLC networks, 2014.

[4] doc43079: ATPL250A Datasheet, 2016.

[5] doc11296: SAME70 Series Datasheet, 2016.

[6] doc43081: Atmel G3-PLC Firmware Stack User Guide, 2016.

[7] ITU G.9901: http://www.itu.int/rec/T-REC-G.9901/en.

[8] ITU G.9903: https://www.itu.int/rec/T-REC-G.9903/en.

[9] G3-PLC Alliance: http://www.g3-plc.com/.

[10] doc43052: PLC coupling reference designs, 2016.

[11] doc43088: G3 PHY Performance Verification, 2016.

Appendix A Board schemes

A.1 ATPL250ABNv2 Schemes

This section contains the schemes of the ATPL250ABN PAN Coordinator board:

- Top level scheme.
- Power supply scheme.
- SAME70.
- Memory.
- USB.
- Ethernet.
- ATPL250A.
- PLC Coupling TX.
- PLC Coupling RX.
- Connectors.
- Components location in top and bottom layers.

Figure A-1. ATPL250ABN Top level scheme.

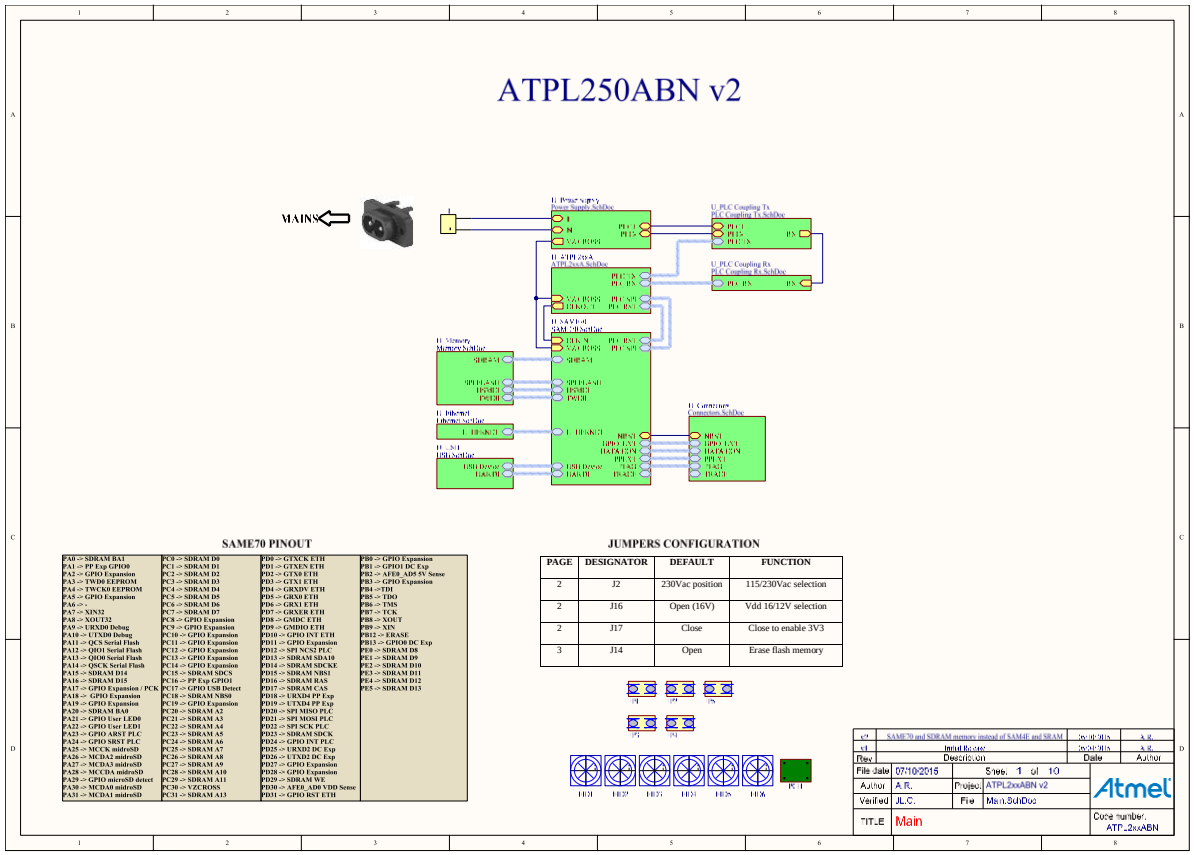


Figure A-2. ATPL250ABN Power supply scheme.

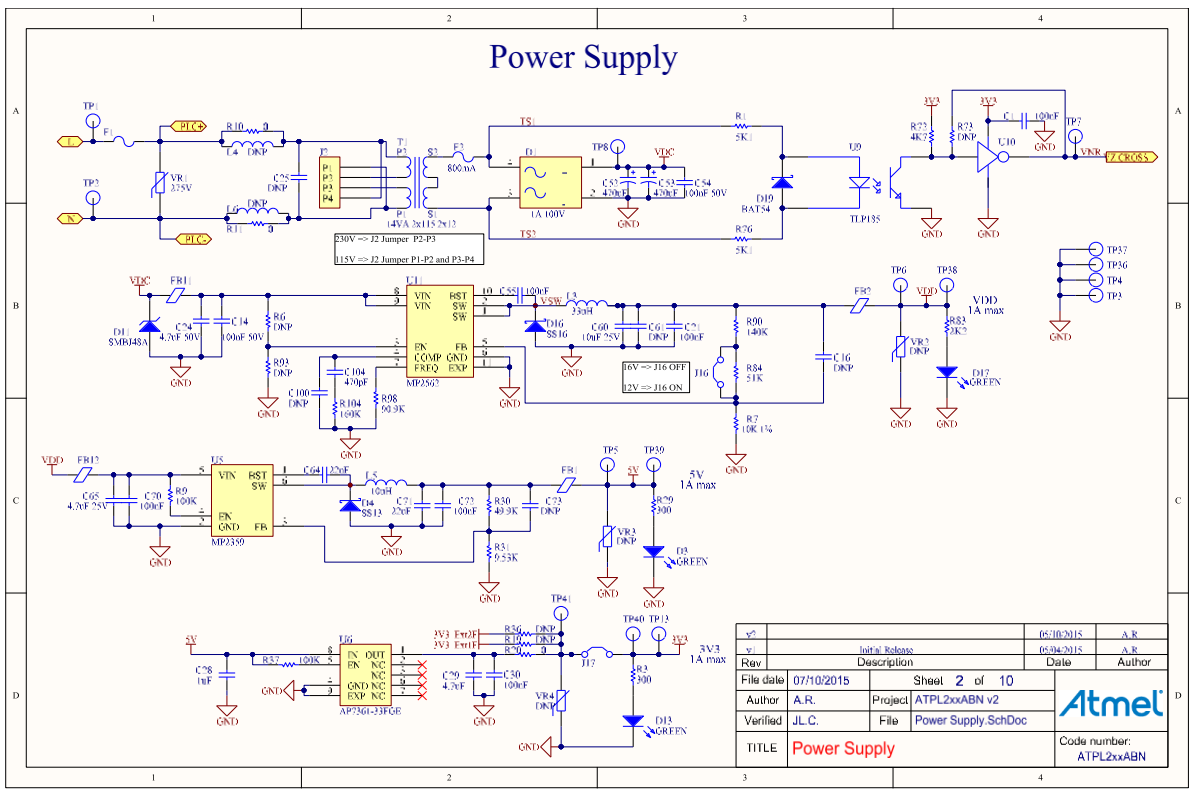


Figure A-3. SAME70Q21 scheme.

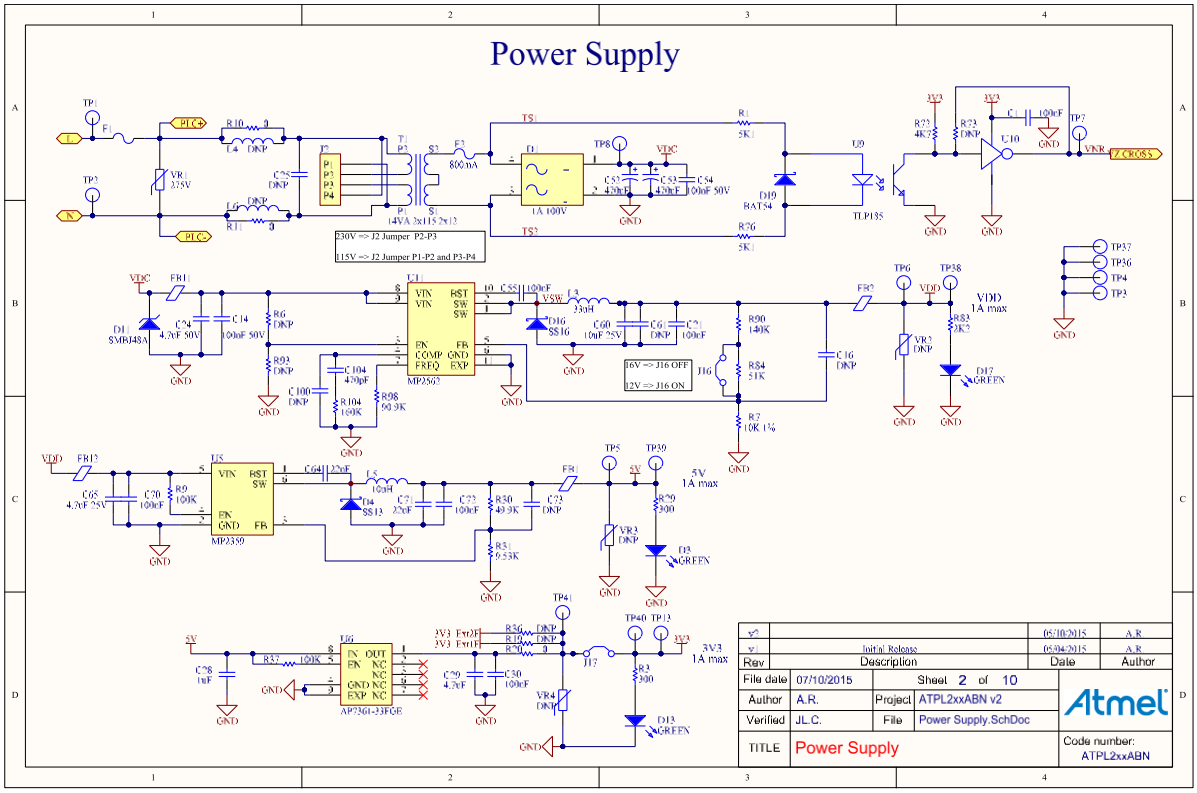


Figure A-4. ATPL250ABN Memory scheme.

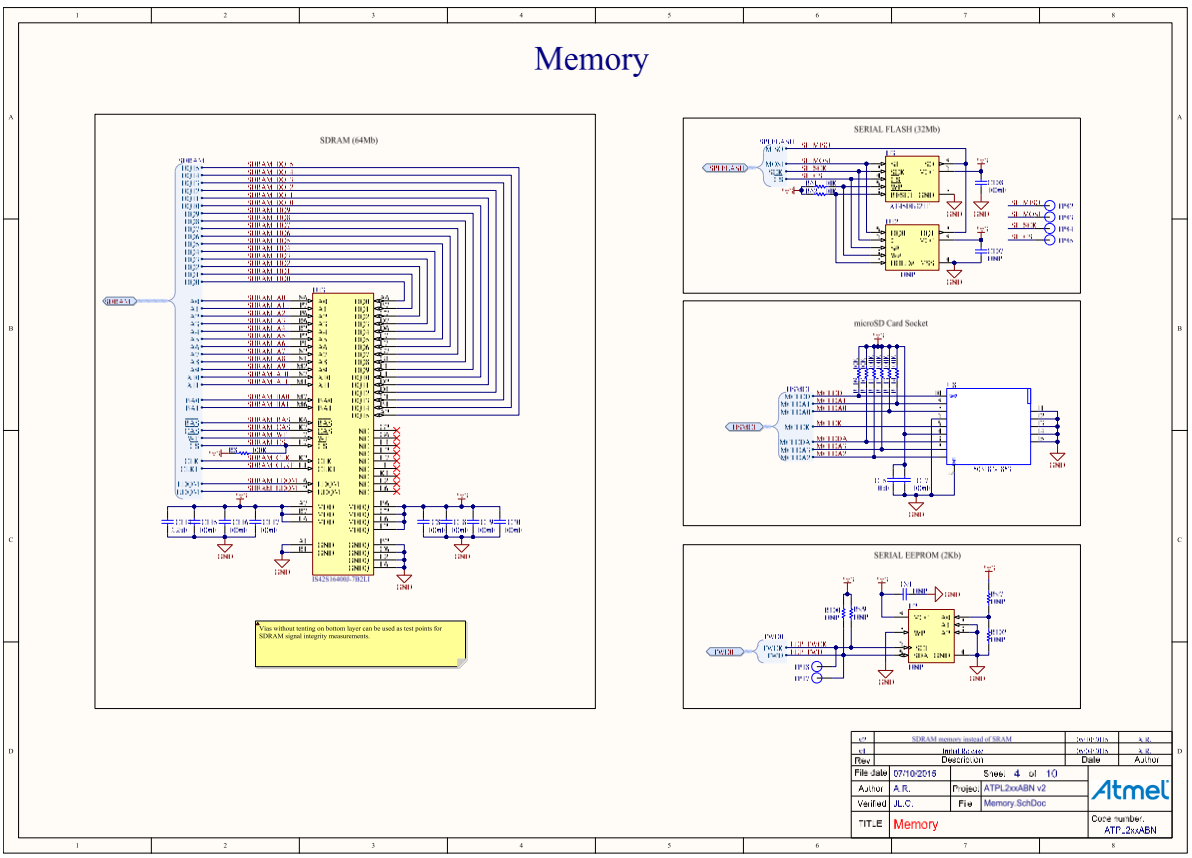


Figure A-5. ATPL250ABN USB scheme.

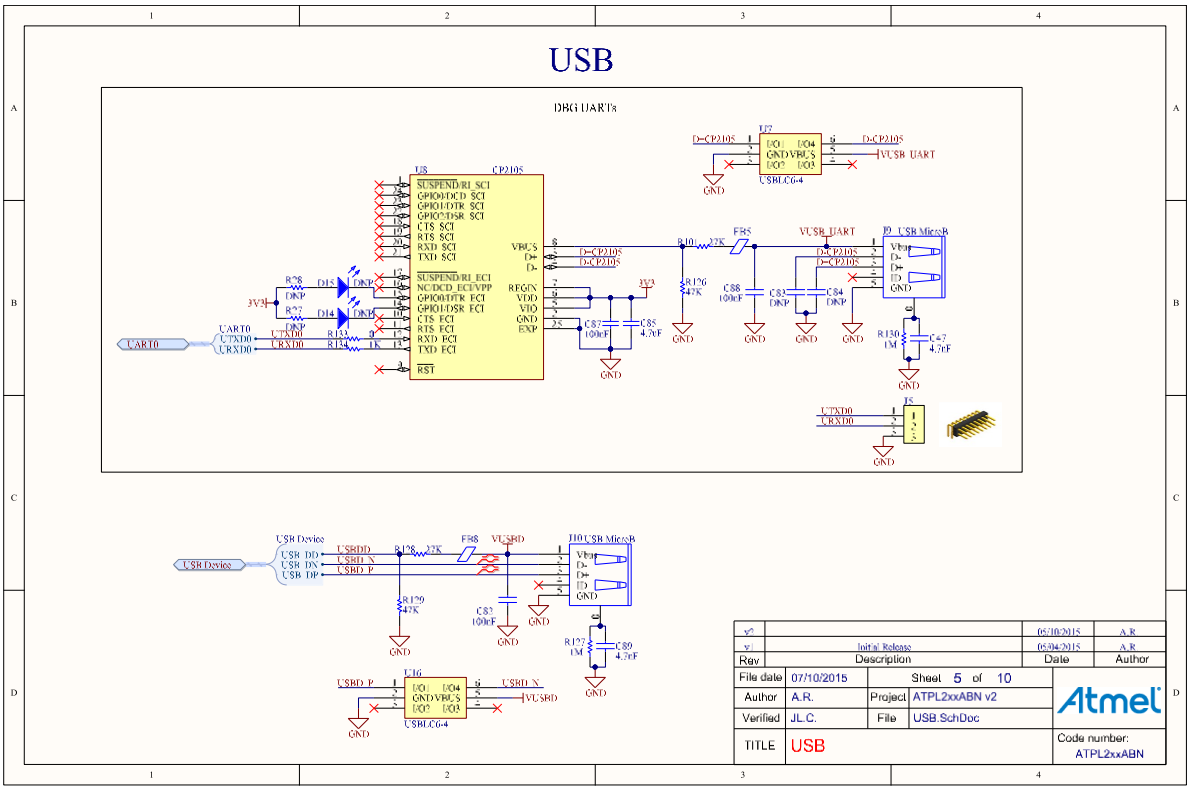


Figure A-6. ATPL250ABN Ethernet scheme.

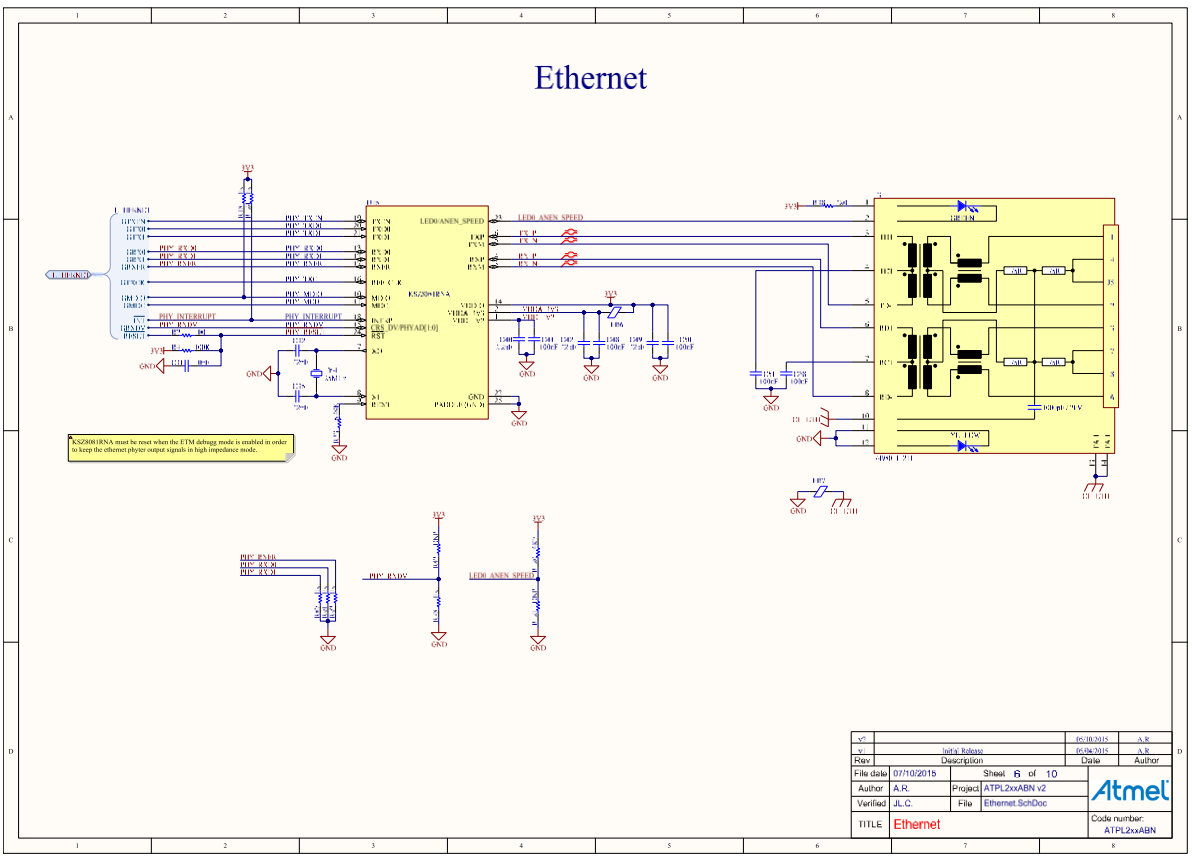


Figure A-7. ATPL250A scheme.

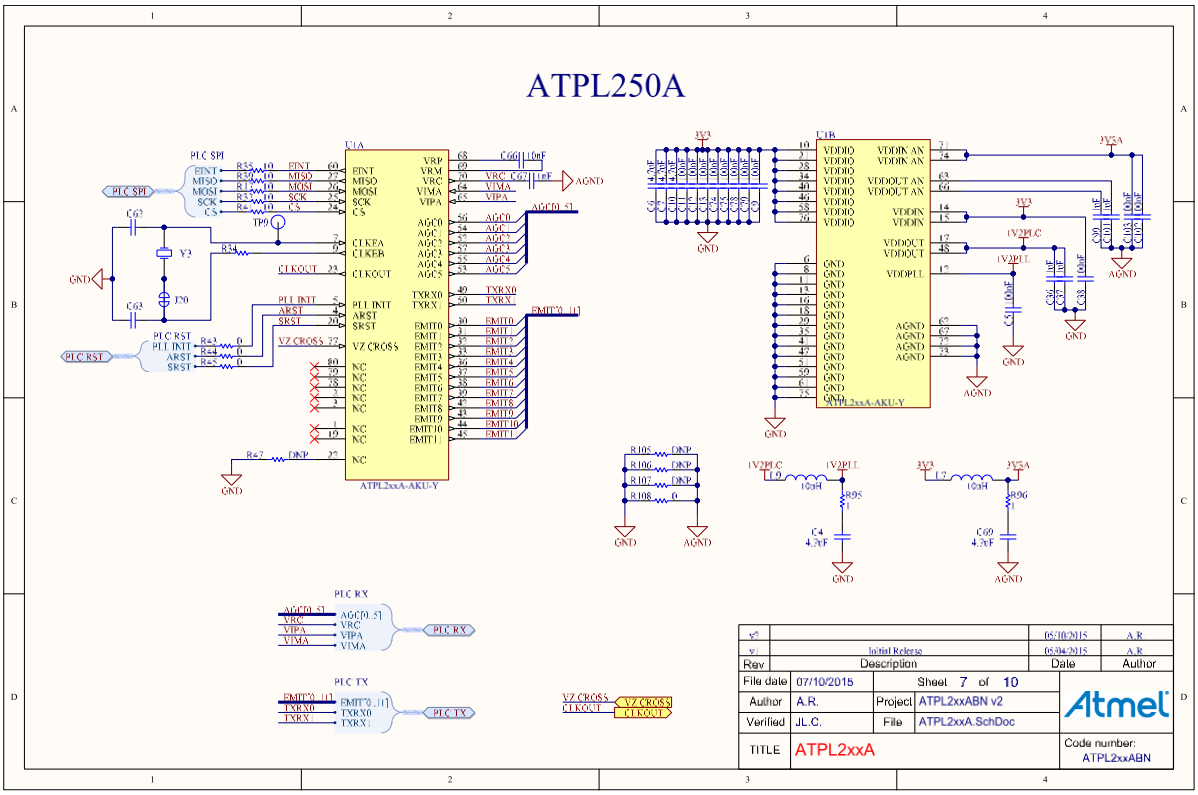


Figure A-8. ATPL250ABN PLC Coupling transmission scheme.

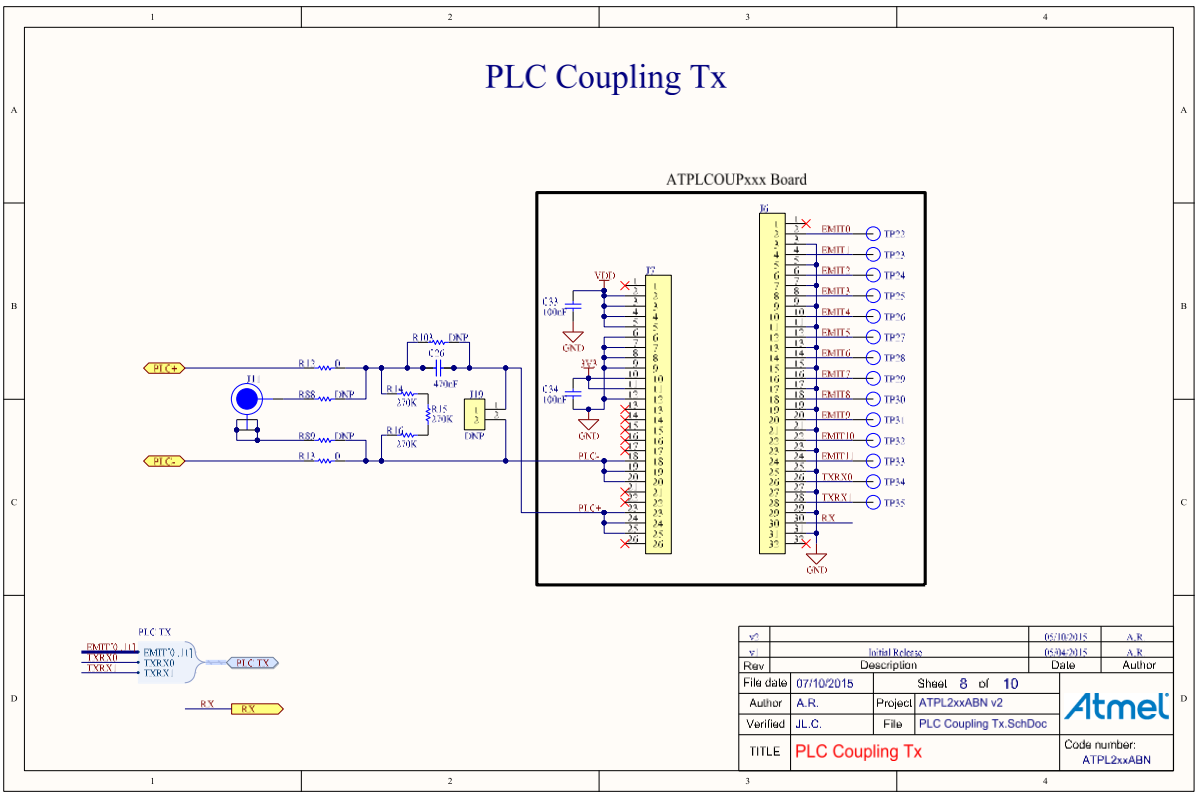


Figure A-9. ATPL250ABN PLC Coupling reception scheme.

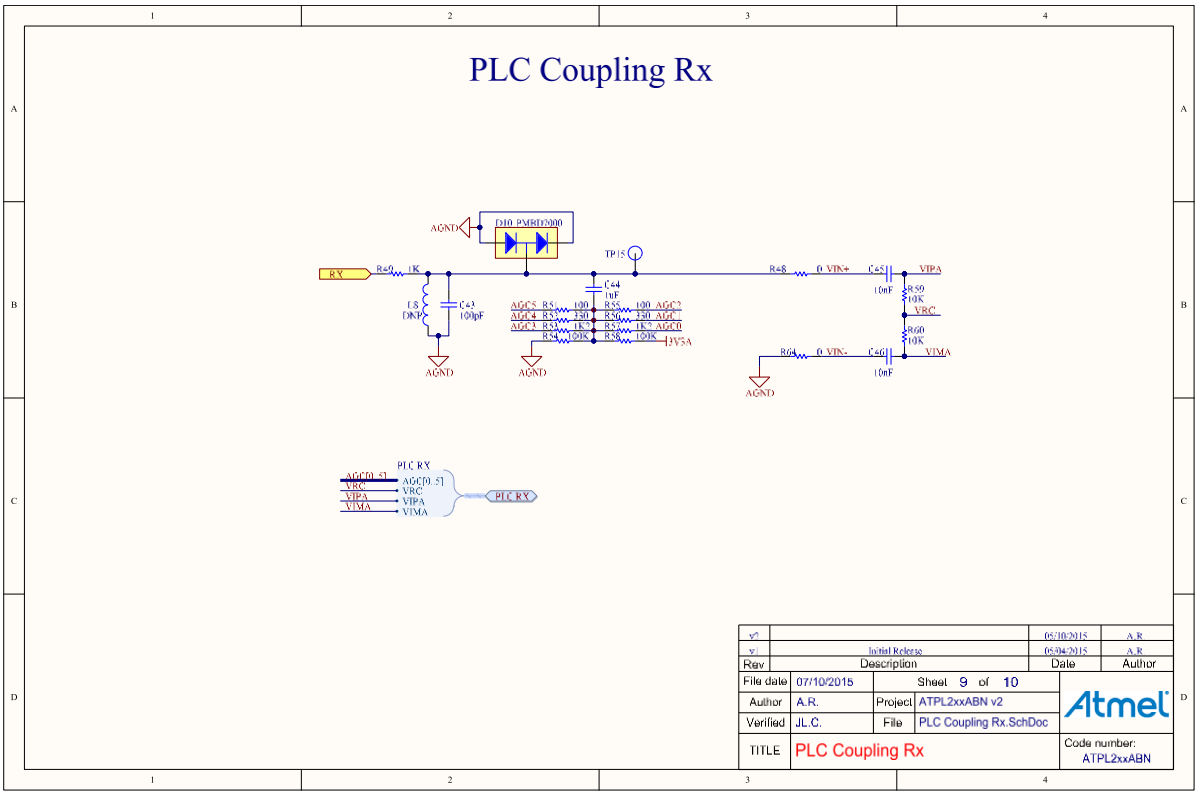


Figure A-10. ATPL250ABN Connectors.

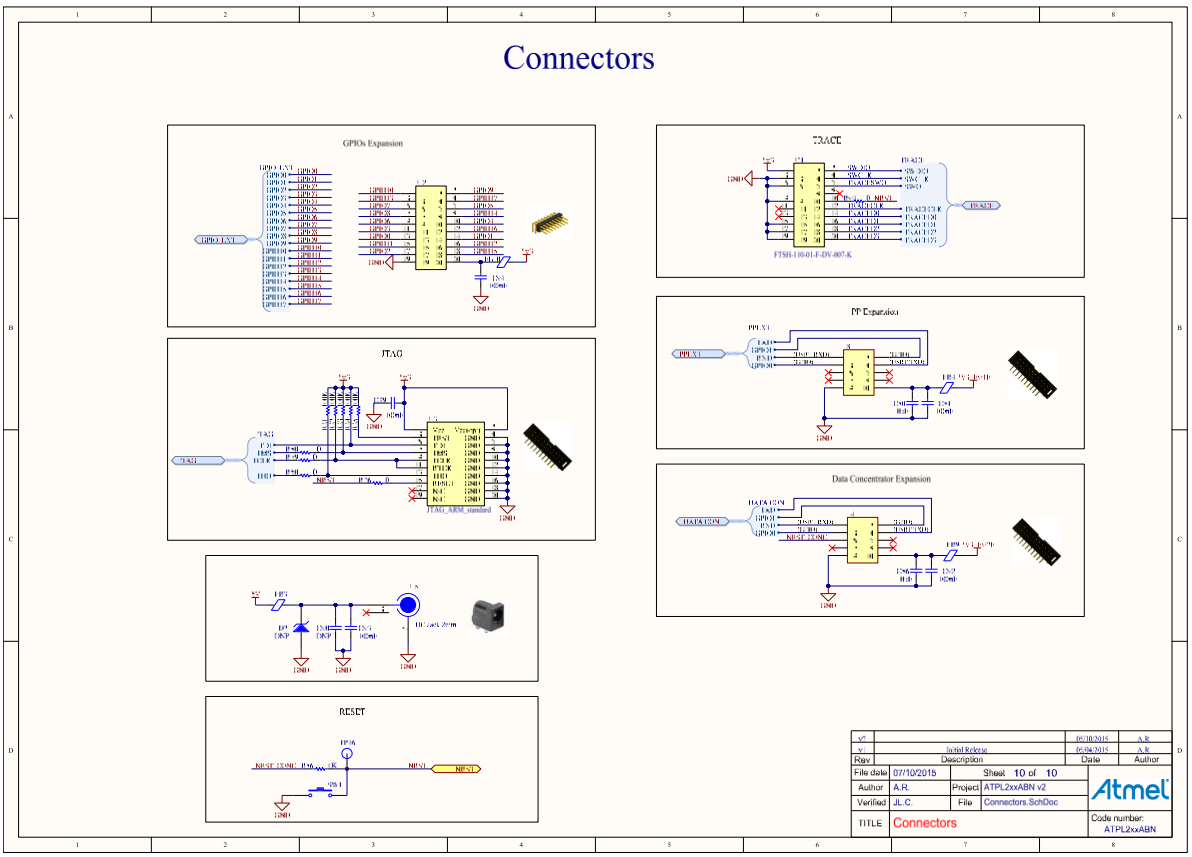


Figure A-11. ATPL250ABN components location in top layer.

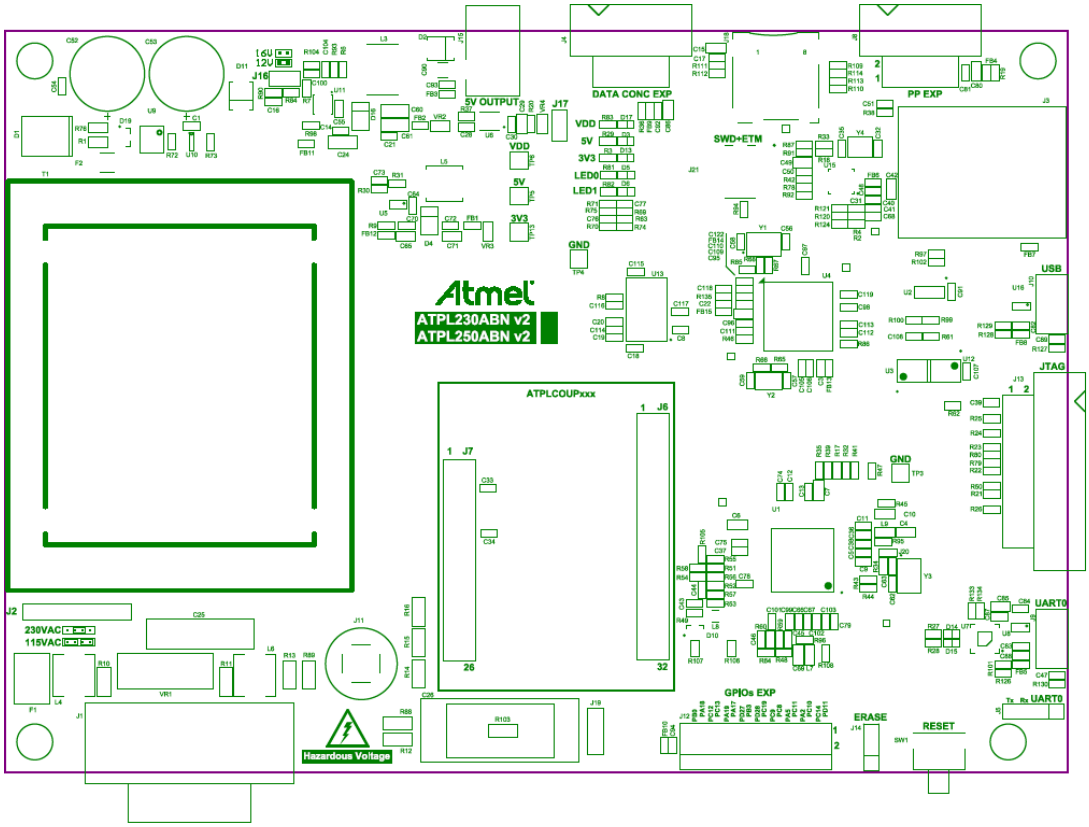


Figure A-12. ATPL250ABN components location in bottom layer.

A.2 ATPLCOUP007v2.5 schemes

This section contains the schemes of the ATPLCOUP007 board:

- PLC Coupling transmission scheme.
- Components location in top and bottom layers.

Figure A-13. ATPLCOUP007 PLC Coupling transmission scheme.

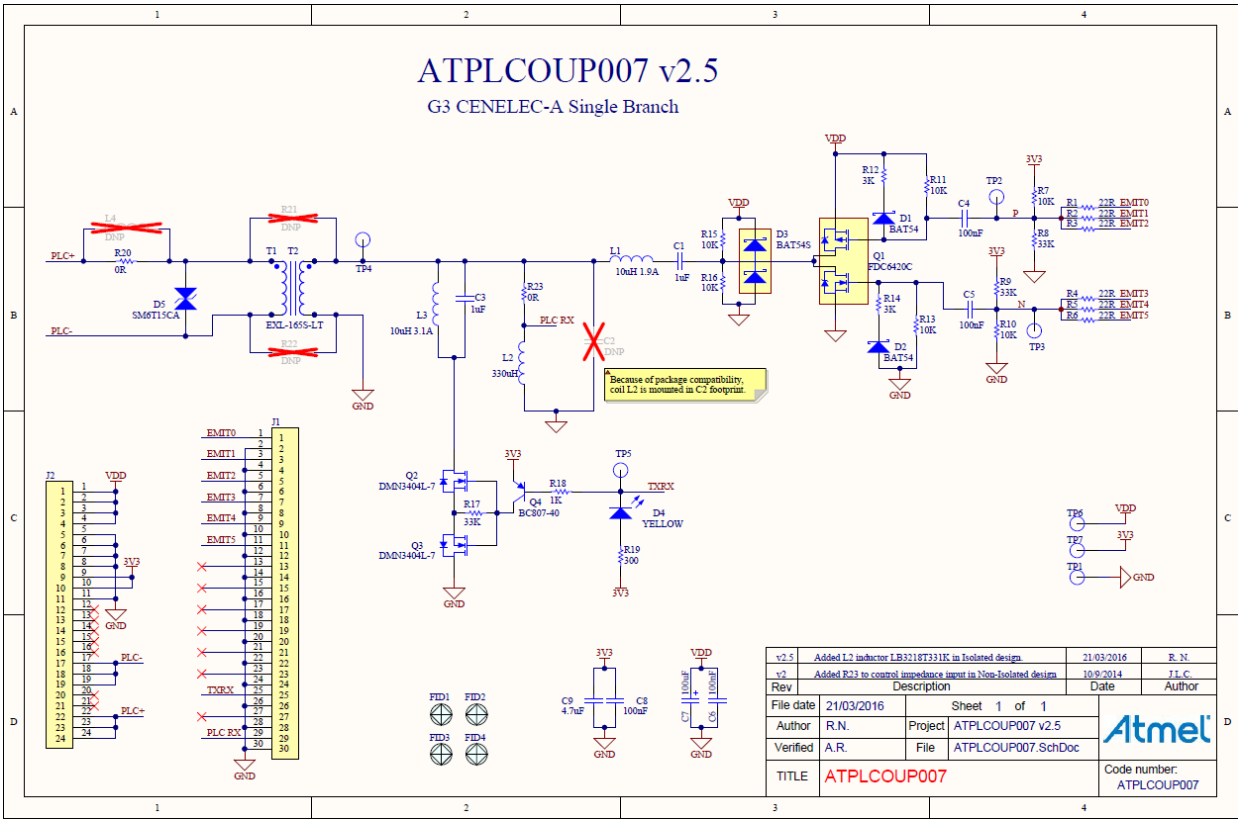
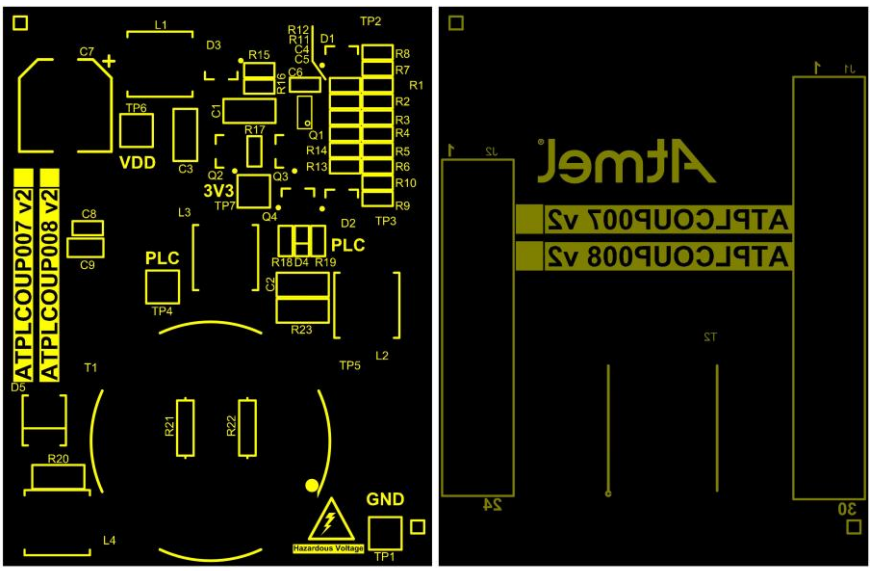


Figure A-14. ATPLCOUP007 components location in top and bottom layers.



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Revision History

Doc Rev.	Date	Comments
43106C	10/2016	Minor changes.
43106B	09/2016	Updating document according to EK contents (SW release).
43106A	06/2016	Initial document release.

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