MIC3001

FOM Management IC with Internal Calibration

Consider MIC3003 for New Designs

General Description

The MIC3001 enables the implementation of sophisticated, hot-pluggable fiber optic transceivers with intelligent laser control and an internally calibrated digital diagnostic monitoring interface per SFF-8472. It essentially integrates all non-data path functions of an SFP transceiver into a tiny (4mm × 4mm) QFN package.

A highly-configurable automatic power control (APC) circuit controls laser bias. Bias and modulation are temperature compensated using dual DACs, an on-chip temperature sensor, and NVRAM look-up tables. A programmable internal feedback resistor provides unprecedented dynamic range for APC. Controlled laser turn-on facilitates hot plugging.

An analog-to-digital converter converts the measured temperature, voltage, bias current, transmit power, and received power from analog to digital. An EEPOT provides front-end adjustment of RX power. Each parameter is compared against user-programmed warning and alarm thresholds. Analog comparators and DACs provide high-speed monitoring of received power and critical laser operating parameters. Data can be reported as either internally calibrated or externally calibrated.

An interrupt output, power-on hour meter, and data-ready bits add user friendliness beyond SFF-8472. The interrupt output and data-ready bits reduce overhead in the host system. The power-on hour meter logs operating hours using an internal real-time clock and stores the result in NVRAM.

Communication with the MIC3001 is via an industry standard 2-wire serial interface. Nonvolatile memory is provided for serial ID, configuration, and separate OEM and user scratchpad spaces. Two-level password protection guards against data corruption.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- APC or constant-current laser bias
- Turbo mode for APC loop start-up and shorter laser turn on time
- Supports multiple laser types and bias circuit topologies
- Drives external low-cost BJT for laser bias
- Integrated digital temperature sensor
- Temperature compensation of modulation, bias, and fault levels via NVRAM look-up tables
- Direct interface to SY88932, SY88982, SY89307 and other drivers
- NVRAM to support GBIC/SFP serial ID function
- User writable EEPROM scratchpad
- Diagnostic monitoring interface per SFF-8472
  - Monitors and reports critical parameters: temperature, bias current, TX and RX optical power, and supply voltage
  - S/W control and monitoring of TXFAULT, RXLOS, RATESELECT, and TXDISABLE
  - Internal or external calibration
  - EEPOT for adjusting RX power measurement
- Power-on hour meter
- Interrupt capability
- Extensive test and calibration features
- 2-wire, I^2C-compatible serial interface
- SFP MSA and SFF-8472 compliant
- 3.0V to 3.6V power supply range
- 5V-tolerant I/O
- 4mm × 4mm 24-pin QFN package

Applications

- SFF/SFP optical transceivers
- SONET/SDH transceivers and transponders
- Fibre channel transceivers
- 10Gbps transceivers
- Free space optical communications
- Proprietary optical links

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Ordering Information

Part Number	Package Type	Junction Temperature Range	Package Marking	Lead Finish
MIC3001BML	24-Pin QFN	–45°C to +105°C	3001	Sn-Pb or NiPdAu
MIC3001BMLTR[1]	24-Pin QFN	–45°C to +105°C	3001	Sn-Pb or NiPdAu
MIC3001GML	24-Pin QFN	–45°C to +105°C	3001 with Pb-Free Bar-Line Indicator	NiPdAu
MIC3001GMLTR[1]	24-Pin QFN	–45°C to +105°C	3001 with Pb-Free Bar-Line Indicator	NiPdAu

Note:

1. Tape and Reel.

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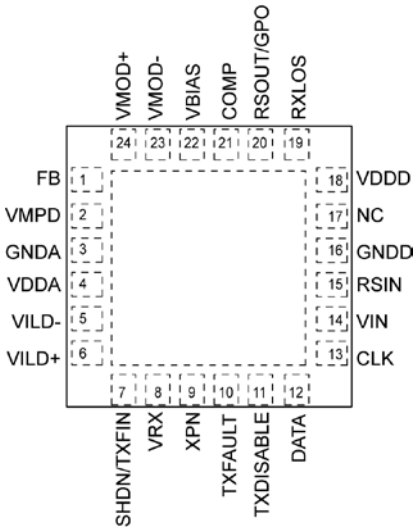
Pin Configuration



24-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	FB	Analog Input. Feedback voltage for the APC loop op-amp. Polarity and scale are programmable via the APC configuration bits. Connect to V_{BIAS} if APC is not used.
2	VMPD	Analog Input. Multiplexed A/D converter input for monitoring transmitted optical power via a monitor photodiode. In most applications, VMPD will be connected directly to FB. The input range is 0 - V_{REF} or 0 - V_{REF}/4 depending on the setting of the APC configuration bits
3	GNDA	Ground return for analog functions.
4	VDDA	Power supply input for analog functions.
5	VILD–	Analog Input. Reference terminal for the multiplexed pseudo-differential A/D converter inputs for monitoring laser bias current via a sense resistor (VILD+ is the sensing input). Tie to V_{DD} or GND to reference the voltage sensed on VILD+ to V_{DD} or GND respectively. Limited common-mode voltage range, see “Applications Information” section for more details.
6	VILD+	Analog Input. Multiplexed A/D input for monitoring laser bias current via a sense resistor (signal input); accommodates inputs referenced to V_{DD} or GND (see pin 5 description). Limited common-mode voltage range, see “Applications Information” section for more details.
7	SHDN (TXFIN)	Digital output; Programmable polarity. When used as shutdown output (SHDN), asserted at the detection of a fault condition that can be used to activate a second series transistor in the laser current path, enhancing protection against single-point failures. When programmed as TXFIN, it is an input for external fault signals to be ORed with the internal fault sources to drive TXFAULT.
8	SHDN (TXFIN)	Analog Input. Multiplexed A/D converter input for monitoring received optical power. The input range is 0 to V_{REF}. A 5-bit programmable EEPOT on this pin provides for coarse calibration and ranging of the RX power measurement.
9	XPN	Analog Input/Output. Optional connection to an external PN junction for sensing temperature at a remote location. The Zone bit in OEMCFG1 determines whether temperature is measured using the on-chip sensor or the remote PN junction.
10	TXFAULT	Digital Output; Open-Drain. A high level indicates a hardware fault impeding transmitter operation. The state of this input is always reflected in the TXFLT bit.

Pin Description

Pin Number	Pin Name	Pin Function
11	TXDISABLE	Digital Input; Active High. The transmitter is disabled when this line is high or the STXDIS bit is set. The state of this input is always reflected in the TXDIS bit.
12	DATA	Digital I/O; Open-drain. Bi-directional serial data input/output.
13	CLK	Digital Input; Serial bit clock input.
14	VIN	If bit 4 (IE) in USRCTL register is set to 0 (default), this pin is configured as analog input. If IE bit is set to 1, this pin is configured as open-drain output. Analog Input: Multiplexed A/D input for monitoring supply voltage. 0V to 5.5V input range. Open-drain output: outputs the internally generated interrupt signal /INT.
15	RSIN	Digital Input; Rate Select Input; ORed with rate select bit to determine the state of the RSOUT pin. The state of this pin is always reflected in the RSEL bit.
16	GNDD	Ground return for digital functions.
17	NC	No connection. This pin is used for test purposes and must be left unconnected.
18	VDDD	Power supply input for digital functions.
19	RXLOS	Digital Output; Active-High/Open-Drain. Indicates the loss of the received signal as indicated by a level of received optical power below the programmed RXLOS comparator threshold; may be wire-ORed with external signals. Low indicates normal operation. RXLOS is de-asserted when VRX > LOSFLTn. The LOS bit reflects the state of RXLOS whether driven by the MIC3001 or an external circuit.
20	RSOUT (GPO)	Digital Output. Open-Drain or push-pull. When used as rate select output, this output is controlled by the SRSEL bit ORed with RSIN input and is open drain only. When used as a general-purpose, non-volatile output, it is controlled by the GPO configuration bits in OEMCFG3.
21	COMP	Analog Output, compensation terminal. Connect a capacitor between this pin and GNDA or V_{DDA} with appropriate value to tune the APC loop time constant to a desirable value.
22	VBIAS	Analog Output. Buffered DAC output capable of sourcing or sinking up to 10mA under control of the APC function to drive an external transistor for laser diode D.C. bias. The output and feedback polarity are programmable to accommodate either a NPN or an PNP transistor to drive a common-anode or common-cathode laser diode.
23	VMOD–	Analog Input. Inverting terminal of VMOD buffer op-amp. Connect to V_{MOD}+ (gain = 1) or feedback resistors network to set a different gain
24	VMOD+	Analog Output. Buffered DAC output to set the modulation current on the laser driver IC. Operates with either a 0– V_{REF} or a (V_{DD}–V_{REF}) – V_{DD} output swing so as to generate either a ground-referenced or a V_{DD} referenced programmed voltage. A simple external circuit can be used to generate a programmable current for those drivers that require a current rather than a voltage input. See “Applications Information” section for more details.

Absolute Maximum Ratings[1]

Power Supply Voltage, V_{DD} ..... +3.8V
Voltage on CLK, DATA, TXFAULT, VIN, RXLOS, DISABLE, RSIN..... –0.3V to +6.0V
Voltage On Any Other Pin.....–0.3V to V_{DD}+0.3V
Power Dissipation, T_A = 85°C 1.5W
Junction Temperature (T_J) ..... 150°C
Storage Temperature (T_S)..... –65°C to +150°C
ESD Ratings[3]
Human Body Model..... 2kV
Machine Model 300V
Soldering (20sec) 260ºC

Operating Ratings[2]

Power Supply Voltage, V_{DDA}/V_{DDD} ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ... –40°C to +105°C
Package Thermal Resistance
QFN (θ_{JA})..... 43°C/W

Electrical Characteristics

For typical values, T_A = 25°C, V_{DDA} = V_{DDD} = +3.3V, unless otherwise noted. **Bold** values are guaranteed for +3.0V ≤ (V_{DDA} = V_{DDD}) ≤ 3.6V, $T_{(min)} \le T_A \le T_{(max)}$[8]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supply						
I_{DD}	Supply Current	CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE low; all DACs at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
		CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE high; FLTDAC at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
V_{POR}	Power-on Reset Voltage	All registers reset to default values; A/D conversions initiated.		2.9	2.98	V
V_{UVLO}	Under-Voltage Lockout Threshold	Note 5	2.5	2.73		V
V_{HYST}	Power-on Reset Hysteresis Voltage			170		mV
t_{POR}	Power-on Reset Time	V_{DD} > V_{POR}[4]		50		µs
V_{REF}	Reference Voltage		1.210	1.225	1.240	V
$\Delta V_{REF}/\Delta V_{DDA}$	Voltage Reference Line Regulation			1.7		mV/V
Temperature-to-Digital Converter Characteristics						
	Local Temperature Measurement Error	–40°C ≤ T_A ≤ +105°C[6]		±1	±3	°C
	Remote Temperature Measurement Error	–40°C ≤ T_A ≤ +105°C[6]		±1	±3	°C
t_{CONV}	Conversion Time	Note 4			60	ms
t_{SAMPLE}	Sample Period				100	ms
Remote Temperature Input, XPN						
I_F	Current to External Diode[4]	XPN at high level, clamped to 0.6V.		192	400	µA
		XPN at low level, clamped to 0.6V.	7	12		µA

Voltage-to-Digital Converter Characteristics (V_{RX}, V_{AUX}, V_{BIAS}, V_{MPD}, V_{ILD}±)

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Voltage Measurement Error	–40°C ≤ T_A ≤ +105°C(6)		±1	±2.0	%fs
t_{CONV}	Conversion Time	Note 4			10	ms
t_{SAMPLE}	Sample Period	Note 4			100	ms
Voltage Input, V_{IN} (Pin 14 used as an ADC Input)						
V_{IN}	Input Voltage Range	–0.3 ≤ V_{DD} ≤ 3.6V	GNDA		5.5	V
I_{LEAK}	Input Current	V_{IN} = V_{DD} or GND; V_{AUX} = V_{IN}		55		µA
C_{IN}	nput Capacitance			10		pF
Digital-to-Voltage Converter Characteristics (V_{MOD}, V_{BIAS})						
	Accuracy	–40°C ≤ T_A ≤ +105°C(6)		±1	2.0	%fs
t_{CONV}	Conversion Time	Note 4			20	ms
DNL	Differential Non-linearity Error	Note 4		±0.5	±1	LSB
Bias Current Sense Inputs, V_{ILD}+, V_{ILD}–						
V_{ILD}	Differential Input Signal Range, | V_{ILD}^+ – V_{ILD}^- |		0		V_{REF}/4	mV
I_{IN+}	V_{ILD}^+ input current				±1	µA
$I_{IN–}$	V_{ILD}^- input current	V_{ILD}^- referred to V_{DDA}		+150		µA
	| V_{ILD}^+ – V_{ILD}^- | = 0.3V	V_{ILD}^- referred to GND		-150		µA
C_{IN}	Input Capacitance			10		pF
APC Op Amp, FB, V_{BIAS}, COMP						
GBW	Gain Bandwidth Product	C_{COMP} = 20pF; Gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient(4)			1		µV/°C
V_{OUT}	Output Voltage Swing	I_{OUT} = 10mA, SRCE bit = 1	GNDA		1.25	V
		I_{OUT} = -10mA, SRCE bit = 0	V_{DDA} -1.25		V_{DDA}	V
I_{SC}	Output Short-Circuit Current			55		mA
t_{SC}	Short Circuit Withstand Time	T_J ≤ 150°C(4)				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; Gain = 1, to GND		55		dB
		C_{COMP} = 20pF; Gain = 1, to V_{DD}		40		
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF, Note 4			1	V/V
ΔV/Δt	Slew Rate	C_{COMP} = 20pF; Gain = 1		3		V/µs
ΔRFB	Internal Feedback Resistor Tolerance			±20		%
ΔRFB/Δt	Internal Feedback Resistor Temperature Coefficient			25		ppm/C
I_{START}	Laser Start-up Current Magnitude	START = 01_h		0.375		mA
		START = 02_h		0.750		mA
		START = 04_h		1.500		mA
		START = 08_h		3.000		mA
C_{IN}	Pin Capacitance			10		pF

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{MOD} Buffer Op-Amp, V_{MOD}+, V_{MOD}–						
GBW	Gain Bandwidth	C_{COMP} = 20pF; Gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient			1		µV/°C
I_{BIAS}	V_{MOD}– Input Current			±0.1	±1	µA
V_{OUT}	Output Voltage Swing	I_{OUT} = ±1mA	GNDA+75		V_{DDA}-75	mV
I_{SC}	Output Short-Circuit Current			35		mA
t_{SC}	Short Circuit Withstand Time	$T_J \le 150°C$(4)				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; Gain = 1, to GND		65		dB
		C_{COMP} = 20pF; Gain = 1, to V_{DD}		44		dB
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF			1	V/V
$\Delta V/\Delta T$	Slew Rate	C_{COMP} = 20pF; Gain = 1		1		V/µs
C_{IN}	Pin Capacitance			10		pF
Control and Status I/O, TXDISABLE, TXFAULT, RSIN, RSOUT(GPO), SHDN(TXFIN), RXLOS, /INT						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.0			V
V_{OL}	Low Output Voltage	$I_{OL} \le$ 3mA			0.3	V
V_{OH}	High Output Voltage (applies to SHDN only)	$I_{OH} \le$ 3mA			V_{DDD}–0.3	V
I_{LEAK}	Input Current				±1	µA
C_{IN}	Input Capacitance			10		pF
Transmit Optical Power Input, V_{MPD}						
V_{IN}	Input Voltage Range	Note 4	GNDA		V_{DDA}	V
V_{RX}	Input Signal Range	BIASREF=0			V_{REF}	V
		BIASREF=1	V_{DDA}–V_{REF}		V_{DDA}	V
C_{IN}	Input Capacitance	Note 4		10		pF
I_{LEAK}	Input Current				±1	µA
Received Optical Power Input, VRX, RXPOT						
	Input Voltage Range	Note 4	GNDA		V_{DDA}	V
V_{RX}	Valid Input Signal Range (ADC Input Range)		0		V_{REF}	V
$R_{RXPOT(32)}$	End-to-End Resistance	RXPOT = $1F_h$		32		KΩ
ΔRXPOT	Resistor Tolerance			±20		%
ΔRXPOT/ΔT	Resistor Temperature Coefficient			25		ppm/C
$\Delta V_{RX}/V_{RXPOT}$	Divider Ratio Accuracy	00 ≤ RXPOT ≤ $1F_h$	-5		+5	%
I_{LEAK}	Input Current	RXPOT = 0 (disconnected)			±1	µA
C_{IN}	Input Capacitance	Note 4		10		pF
I_{LEAK}	Input Current				±1	µA

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Control and Status I/O Timing, TXFAULT, TXDISABLE, RSIN, RSOUT, and RXLOS						
t_{OFF}	TXDISABLE Assert Time	From input asserted to optical output at 10% of nominal, C_{COMP} = 10nF.			**10**	µs
t_{ON}	TXDISABLE De-assert Time	From input de-asserted to optical output at 90% of nominal, C_{COMP} = 10nF.			**1**	ms
t_{INIT}	Initialization Time	From power on or transmitter enabled to optical output at 90% of nominal and TX_FAULT de-asserted.(4)			**300**	ms
t_{INIT2}	Power-on Initialization Time	From power on to APC loop enabled.			**200**	ms
t_{FAULT}	TXFAULT Assert Time	From fault condition to TXFAULT assertion.(4)			95	µs
t_{RESET}	Fault Reset Time	Length of time TXDISABLE must be asserted to reset fault condition.	**10**			µs
t_{LOSS_ON}	RXLOS Assert Time	From loss of signal to RXLOS asserted.			95	µs
t_{LOSS_OFF}	RXLOS De-assert Time	From signal acquisition to LOS de-asserted.			**100**	µs
t_{DATA}	Analog Parameter Data Ready	From power on to valid analog parameter data available.(4)			**400**	ms
t_{PROP_IN}	TXFAULT, TXDISABLE, RXLOS, RSIN Input Propagation Time	Time from input change to corresponding internal register bit set or cleared.(4)			**1**	µs
t_{PROP_OUT}	TXFAULT, RSOUT, /INT Output Propagation Time	From an internal register bit set or cleared to corresponding output change.(4)			**1**	µs
Fault Comparators						
ϕ_{FLTTMR}	Fault Suppression Timer Clock Period	Note 4	**0.475**	0.5	**0.525**	ms
	Accuracy		-3		+3	%/F.S.
t_{REJECT}	Glitch Rejection	Maximum length pulse that will not cause output to change state.(4)	4.5			µs
V_{SAT}	Saturation Detection Threshold	High level		95		%VDDA
		Low level		5		%VDDA
Power-On Hour Meter						
	Timebase Accuracy	0°C ≤ T_A ≤ +70°C(4)	**+5**		**-5**	%
		–40°C ≤ T_A ≤ +105°C	**+10**		**-10**	%
	Resolution	Note 4		10		hours
Non-Volatile (FLASH) Memory						
t_{WR}	Write Cycle Time(7)	From STOP of a one to four-byte write transaction.(4)			**13**	ms
	Data Retention		**100**			years
Endurance	Minimum Permitted Number Write Cycles		**10,000**			cycles

Serial Data I/O Pin, Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Output Voltage	I_{OL} = 3mA			**0.4**	V
		I_{OL} = 6mA			**0.6**	V
V_{IL}	Low Input Voltage				**0.8**	V
V_{IH}	High Input Voltage		**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 4		10		pF

Serial Clock Input, CLK

V_{IL}	Low Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V			**0.8**	V
V_{IH}	High Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V	**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 4		10		pF

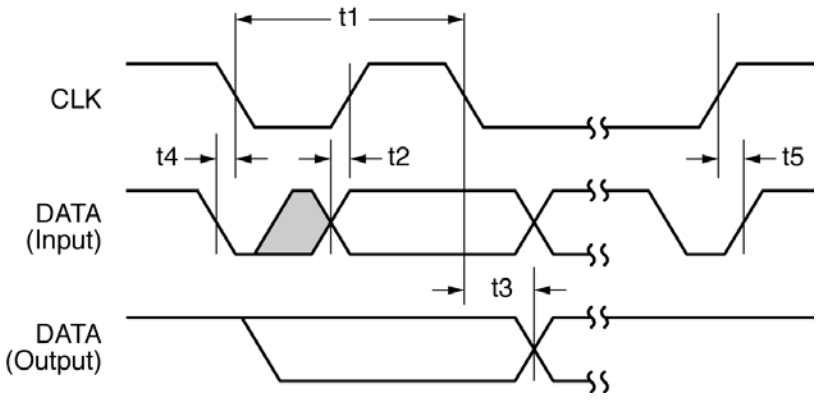
Serial Interface Timing(4)

t_1	CLK (clock) Period		**2.5**			µs
t_2	Data In Setup Time to CLK High		**100**			ns
t_3	Data Out Stable After CLK Low		**300**			ns
t_4	Data Low Setup Time to CLK Low	Start Condition	**100**			ns
t_5	Data High Hold Time After CLK High	Stop Condition	**100**			ns
t_{DATA}	Data Ready Time	From power on to completion of one set of ADC conversions; analog data available via serial interface.			**400**	ms

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling
4. precautions recommended.
5. Guaranteed by designing and/or testing of related parameters. Not 100% tested in production.
6. The MIC3000 will attempt to enter its shutdown state when V_{DD} falls below V_{UVLO}. This operation requires time to complete. If the supply voltage falls too rapidly, the operation may not be completed.
7. Does not include quantization error.
8. The MIC3001 will not respond to serial bus transactions during an EEPROM write-cycle. The host will receive a NACK during t_{WR}.
9. Final test on outgoing product is performed at T_A = +25°C.

Timing Diagram



Serial Interface Timing

Address Map

Address(s)	Field Size (Bytes)	Name	Description
0 –95	96	Serial ID defined by SEP MSA	G-P NVRAM; R/W under valid OEM password.
96 – 127	32	Vendor Specific	Vendor specific EEPROM
128 – 255	128	Reserved	Reserved for future use. G-P NVRAM; R/W under valid OEM password.

Table 1. MIC3001 Address Map, Serial Address = $A0_h$

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
00-27	0-39	40	Alarm and Warning Threshold	High/low limits for warning and alarms; writeable using OEM p/w; read-only otherwise.
28-37	40-55	16	Reserved	Reserved – do not write; reads undefined.
38-5B	56-91	36	Calibration Constants	Numerical constants for external calibration; writeable using OEM p/w; read-only otherwise.
5C-5E	92-94	3	Reserved	Reserved – do not write; reads undefined.
5F	95	1	Checksum	G-P NVRAM; writeable using OEM p/w; ready only otherwise.
60-69	96-105	10	Analog Data	Real time analog parameter data.
6A-6D	106-109	4	Reserved	Reserved – do not write; reads undefined.
6E	110	1	Control/Status Bits	Control and status bits.
6F	111	1	Reserved	Reserved – do not write; reads undefined.
70-71	112-113	2	Alarm Flags	Alarm status bits; read only.
72-73	114-115	2	Reserved	Reserved – do not write; reads undefined.
74-75	116-117	2	Warning Flags	Warning status bits; read only.
76-77	118-119	2	Reserved	Reserved – do not write; reads undefined.
78-7B	120-123	4	OEMPW	OEM password entry field.
7C-7F	124-127	4	Vendor Specific	Vendor specific. Reserved – do not write; reads undefined.
80-F7	128-247	120	User Scratchpad	User writeable EEPROM. G-P NVRAM; R/W using any valid password.
F8-F9	248-249	2	Reserved	Reserved – do not write; reads undefined.
FA	250	1	USRPWSET	User password setting; read/write using any p/w; returns zero otherwise.
FB	251	1	USRPW	Entry field for user password.
FC-FD	252-253	2	POH	Power-on hour meter result; ready only.
FE	254	1	Data Ready Flags	Data ready bits for each measured parameter; read only.
FF	255	1	User Control	End-user control and status bits.

Table 2. MIC3001 Address Map, Serial Address = $A2_h$

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
00-3F	0-63	64	APCLUTn	A.P.C temperature compensation L.U.T.
40-7F	64-127	64	MODLUTn	VMOD temperature compensation L.U.T.
80-BF	128-191	64	IFLTUT	Bias current fault threshold temperature compensation L.U.T.
C0-FF	192-255	64	EOLLUTn	Bias current high alarm threshold temperature compensation L.U.T.

Table 3. Temperature Compensation Tables, Serial Address = $A4_h$

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
00	0	40	OEMCFG0	Control/status bits
01	1	16	OEMCFG1	Control/status bits
02	2	36	OEMCFG2	Control/status bits
03	3	3	APCSET0	APC setpoint 0
04	4	1	APCSET1	APC setpoint 1
05	5	10	APCSET2	APC setpoint 2
06	6	4	MODSET	Nominal modulation DAC setpoint
07	7	1	IBFLT	Bias current fault-comparator threshold
08	8	1	TXPFLT	TX power fault threshold
09	9	2	LOSFLT	RX LOS fault-comparator threshold
0A	10	2	FLTTMR	Fault comparator masking interval timer setting
0B	11	2	FLTMSK	Fault source mask bits
0C-0F	12-15	2	OEMPWSET	Password for access to OEM areas
10	16	4	OEMCAL0	OEM calibration register 0
11	17	4	OEMCAL1	OEM calibration register 1
12	18	120	LUTINDX	Look-up table index read-back
13	19	2	RESERVED	Reserved – do not write; reads undefined.
14	20	1	APCDAC	Reads back current APC DAC setting
15	21	1	MODDAC	Reads back current modulation DAC setting
16	22	2	OEMREAD	Reads back OEM calibration data
17	23	1	LOSFLTn	LOS De-assert threshold
18	24	1	RXPOT	RXPOT tap selection
19	25	1	OEMCFG4	I START selection bits
1A-1F	26-31	6	RESERVED	Reserved – do not write; reads undefined.
20-27	32-39	8	POHDATA	Power-on hour meter scratchpad
28-47	40-71	32	RXLUT	RX power calibration look-up table
48-49	72-73	2	RESERVED	Reserved – do not write; reads undefined.
4A-57	74-87	18	CAL	Internal calibration slope/offset data
59-7D	88-125	37	RESERVED	Reserved – do not write; reads undefined.
7E-FD	126-253	128	SCRATCH	OEM scratchpad area
FE	254	1	MFG_ID	Manufacturer identification (Micrel = 42)
FF	255	1	DEV_ID	Device and die revision

Table 4. OEM Configuration Registers, Serial Address = $A6_h$

Block Diagram

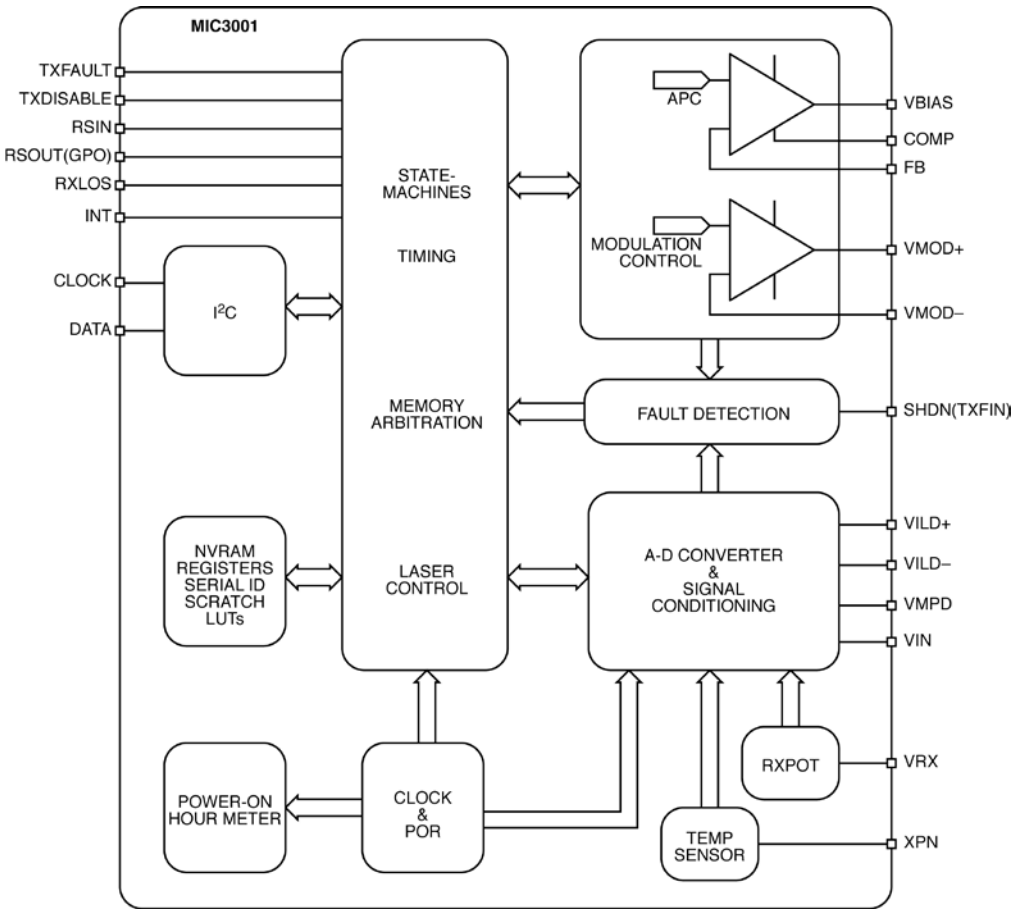


Figure 1. MIC3001 Block Diagram

MIC3000 Capability

In general, the MIC3001 is completely hardware and software backward compatible with the MIC3000. Every feature available in the MIC3000 is still present in the MIC3001. New features have, of course, been added. The following differences between the MIC3000 and MIC3001 would be evident to host software:

1. Faults do not set alarm or warning bits as in the MIC3000.
2. RXOPI at register address 69_h at serial address $x2_h$ now contains four bits of data rather then being fixed at zero as in the MIC3000.

Analog-to-Digital Converter/Signal Monitoring

A block diagram of the monitoring circuit is shown below. Each of the five analog parameters monitored by the MIC3001 are sampled in sequence. All five parameters are sampled and the results updated within the t_{CONV} internal given in the “Electrical Characteristics” section. In OEM, Mode, the channel that is normally used to measure V_{IN} may be assigned to measure the level of the V_{DDA} pin or one of five other nodes. This provides a kind of analog loopback for debug and test purposes. The V_{AUX} bits in OEMCFG0 control which voltage source is being sampled. The various V_{AUX} channels are level-shifted differently depending on the signal source, resulting in different LSB values and signal ranges. See Table 5.

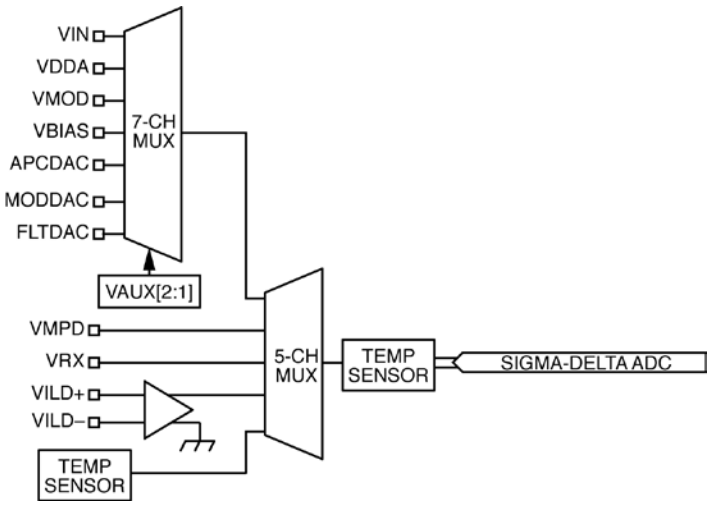


Figure 2. Analog-to-Digital Converter Block Diagram

Channel	ADC Resolution (bits)	Conditions	Input Range (V)	LSB[1]
TEMP	8		N/A	1°C
VAUX	8	See Table 6		
VMPD	8	GAIN = 0; BIASREF = 0	GNDA - V_{REF}	4.77mV
		GAIN = 0; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF})	
		GAIN = 1; BIASREF = 0	GNDA - V_{REF}/4	1.17mV
		GAIN = 1; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF}/4)	
VILD	8	VILD- = VDDA	V_{DDA} – (V_{DDA} – V_{REF})	4.77mV
		VILD- = GNDA	GNDA - V_{REF}	
VRX	12	RXPOT = 00	0 - V_{REF}	0.298mV

Table 5. A/D Input Signal Ranges and Resolutions

Note:

1. Assumes typical VREF value of 1.22V.

Channel	VAUX [2:0]	Input Range (V)	LSB[1] (mV)
V_{IN}	000 = 00_h	0.5V to 5.5V	25.6mV
V_{DDA}	0001 = 01_h	0.5V to 5.5V	25.6mV
V_{BIAS}	010 = 02_h	0.5V to 5.5V	25.6mV
V_{MOD}	011 = 03_h	0.5V to 5.5V	25.6mV
APCDAC	100 = 04_h	0V to V_{REF}	4.77mV
MODDAC	101 = 05_h	0V to V_{REF}	4.77mV
FLTDAC	110 = 06_h	0V to V_{REF}	4.77mV

Table 6. V_{AUX} Input Signal Ranges and Resolutions

Note:

1. Assumes typical V_{REF} value of 1.22V.

Internal/External Calibration

The default mode of calibration in the MIC3001 is external calibration, for which INTCAL bit (bit 0 in OEMCF3 register) is set to 0. This mode is backward compatible with MIC3000. The internal calibration mode is selected by setting INTCAL bit to 1.

A/ External Calibration

The voltage and temperature values returned by the MIC3001's A/D converter are internally calibrated. The binary values of TEMPh:TEMPl and VOLTh:VOLTl are in the format called for by SFF-8472 under Internal Calibration.

SFF-8472 calls for a set of calibration constants to be stored by the transceiver OEM at specific non-volatile memory locations, refer to SFF-8472 specifications for memory map of calibration coefficient. The MIC3001 provides the non-volatile memory required for the storage of these constants. The Digital Diagnostic Monitoring Interface specification should be consulted for full details. Slopes and offsets are stored for use with voltage, temperature, bias current, and transmitted power measurements. Coefficients for a fourth-order polynomial are provided for use with received power measurements. The host system can retrieve these constants and use them to process the measured data. Since voltage and temperature require no calibration, the corresponding slopes should generally be set to unity and the offsets to zero.

Voltage

The voltage values returned by the MIC3001's A/D converter are internally calibrated. The binary values of VOLTh:VOLTl are in the format called for by SFF-8472 under Internal Calibration. Since VINh:VINl requires no processing, the corresponding slope should be set to unity and the offset to zero.

Temperature

The temperature values returned by the MIC3001's A/D converter are internally calibrated. The binary values of TEMPh:TEMPl are in the format called for by SFF-8472 under Internal Calibration. Since TEMPh:TEMPl requires no processing, the corresponding slope should be set to unity and the offset to zero.

Bias Current

Bias current is sensed via an external sense resistor as a voltage appearing at VILD+ and VILD-. The value returned by the A/D is therefore a voltage analogous to bias current. Bias current, IBIAS, is simply VVILD/R_{SENSE}. The binary value in IBIASh (IBIASl is always zero) is related to bias current by:

$$I_{BIAS} = \frac{(0.300V)\left(\frac{IBIASh}{255}\right)}{R_{SENSE}} \quad (1)$$

The value of the least significant bit (LSB) of IBIASh is given by:

$$LSB(IBIASh) = \frac{0.300V}{255 \times R_{SENSE}} Amps = \frac{300mV}{255 \times R_{SENSE}} mA = \frac{1191\ 4}{R_{SENSE}} \mu A \quad (2)$$

Per SFF-8472, the value of the bias current LSB is 2µA. The conversion factor, "slope", needed is therefore:

$$Slope = \frac{1191.4\mu A}{2\mu A \times R_{SENSE}} = 595.7 \div R_{SENSE}$$

The tolerance of the sense resistor directly impacts the accuracy of the bias current measurement. It is recommended that the sense resistor chosen be 1% accurate or better. The offset correction, if needed, can be determined by shutting down the laser, i.e., asserting TXDISABLE, and measuring the bias current. Any non-zero result gives the offset required. The offset will be equal and opposite to the result of the "zero current" measurement.

TX Power

Transmit power is sensed via an external sense resistor as a voltage appearing at VMPD. It is assumed that this voltage is generated by a sense resistor carrying the monitor photodiode current. In most applications, the signal at VMPD will be feedback voltage on FB. The VMPD voltage may be measured relative to GND or V_{DDA} depending on the setting of the BIASREF bit in OEMCFG1. The value returned by the A/D is therefore a voltage analogous to transmit power. The binary value in TXOPh (TXOPl is always zero) is related to transmit power by:

$$P_{TX}(mW) = \frac{K \times VREF\left(\frac{TXOPh}{255}\right)}{R_{SENSE}} = \frac{K \times (1220mV)\left(\frac{TXOPh}{255}\right)}{R_{SENSE}} = \frac{K \times 4.75656 \times TXOPh}{R_{SENSE}} mW \quad (3)$$

For a given implementation, the value of RSENSE is known. It is either the value of the external resistor or the chosen value of RFB used in the application. The constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends on the monitoring photodiode responsivity and coupling efficiency.

It should be noted that the APC circuit acts to hold the transmitted power constant. The value of transmit power reported by the circuit should only vary by a small amount as long as APC is functioning correctly.

RX Power

Received power is sensed as a voltage appearing at VRX. It is assumed that this voltage is generated by a sense resistor carrying the receiver photodiode current.

$$P_{RX}(mW) = K \times VREF \times \frac{RXOPh}{255} = K \times 1220mV \times \frac{RXOPh}{255} mW \quad (4)$$

For a given implementation, the constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends on the gain and efficiencies of the components upstream. In SFF-8472 implementations, the external calibration constants can describe up to a fourth-order polynomial in case K is nonlinear.

B/ Internal Calibration

If the INTCAL bit in OEMCFG3 is set to 1 (internal calibration selected), the MIC3001 will process each piece of data coming out of the A/D converter before storing the result in memory. Linear slope/offset correction will be applied on a per-channel basis to the measured values for voltage, bias current, TX power, and RX power. Only offset correction is applied to temperature.

The user must store the appropriate slope/offset parameters in memory at the time of transceiver calibration. In the case of RX power, a look-up table is provided that implements eight-segment piecewise-linear correction. This correction may be performed as temperature compensation or as simple slope/offset correction. If static slope/offset correction for RX power is desired, the eight coefficient sets can simply be made the same. The memory maps for these coefficients are shown in Table 8 and Table 9.

The slopes allow for the correction of gain errors. Each slope coefficient is an unsigned, sixteen-bit, fixed-point binary number in the format:

[mmmmmmmm.llllllll], where m is a data bit in the most-significant byte and l is a data bit in the least significant byte (5)

Slopes are always positive. The binary point is in between the two bytes, i.e., between bits 7 and 8. This provides a numerical range of 1/256 (0.00391) to 255 in steps of 1/256. The most significant byte is always stored in memory at the lower numerical address.

The offsets correct for constant errors in the measured data. Each offset is a signed, sixteen-bit, fixed-point binary number. The bit-weights of the offsets are the same as that of the final results. In the case of temperature, the offset's least significant byte (LSB) is always zero since the MIC3001 does not deal with fractional temperature values. The sixteen bit offsets provide a numerical range of –32768 to +32767 for voltage, bias current, transmit power, and receive power. The value returned by the A/D is therefore a voltage analogous to received power. The binary value in RXOPh (RXOPl is always zero) is related to received power by:

The numerical range for the temperature offset is –32513 (–128°) to +32512 (+127°) in increments of 256 (1°). The format for offsets is:

[Smmmmmmmmllllllll], where S is the sign bit (1 = positive, 0 = negative), m is a data bit in the most-significant byte and l is a data bit in the least significant byte (6)

The most significant byte is always stored in memory at the lower numerical address.

Calibration of voltage, bias current, and TX power are performed using the following calculation:

RESULTn = ADC_RESULTn x SLOPEn + OFFSETn (7)

Calibration of temperature is performed using the following calculation:

RESULT = ADC_RESULT + OFFSET (8)

Calibration of RX power is performed using the following calculation:

RESULT = ADC_RESULT x SLOPE(m) + OFFSET(m) (9)

where m is the appropriate value from the RX power calibration look-up table.

The results of these calculations are rounded to sixteen bits in length. If the seventeenth most significant bit is a one, the result is rounded up to the next higher value. If the seventeenth most significant bit is zero, the upper sixteen bits remain unchanged. The bit-weights of the offsets are the same as that of the final results. For SFF-8472 compatible applications, these bit-weights are given in Table 7.

Parameter	Magnitude of LSB
Temperature	1.0°C(1)
Voltage	100µV
Bias Current	2µA
TX Power	0.1µW
RX Power	0.1µW

Table 7. LSB Values of Offset Coefficients

Note:

1. The LSBytes of the temperature is always zero.

Address(s)		Field Size	Name	Description
HEX	DEC			
48-49	72-73	2	RESERVED	Reserved. (There is no slope for temperature.) Do not write; reads undefined.
4A-4B	74-75	2	TOFFh:TOFFl	Temperature offset; signed fixed point; LSB is always zero; MSB is at lower physical address.
4C-4D	76-77	2	VSLPh:VSLPl	Voltage slope; unsigned fixed-point; MSB is at lower physical address.
4E-4F	78-79	2	VOFFh:VOFFl	Voltage offset; signed fixed point; MSB is at lower physical address.
50-61	80-81	2	ISLPh:ISLPl	Bias current slope; unsigned fixed-point; MSB is at lower physical address.
52-63	82-83	2	IOFFh:IOFFl	Bias current offset; signed fixed point; MSB is at lower physical address.
54-65	84-85	2	TXSLPh: TXSLPl	TX power slope; unsigned fixed-point; MSB is at lower physical address.
56-67	86-87	2	TXOFFh: TXOFFl	TX power offset; signed fixed point; MSB is at lower physical address.

Table 8. Internal Calibration Coefficient Memory Map – Part I

Address(s)		Field Size	Name	Description
HEX	DEC			
28-29	40-41	2	RXSLP0h: RXSLP0l	RX power slope 0; unsigned fixed-point; MSB is at lower physical address.
2A-2B	42-43	2	RXOFF0h: RXOFF0l	RX power offset 0; signed twos-complement; MSB is at lower physical address.
2C-2D	44-45	2	RXSLP1h: RXSLP1l	RX power slope 1; unsigned fixed-point; MSB is at lower physical address.
2E-2F	46-47	2	RXOFF1h: RXOFF1l	RX power offset 1; signed twos-complement; MSB is at lower physical address.
30-31	48-49	2	RXSLP2h: RXSLP2l	RX power slope 2; unsigned fixed-point; MSB is at lower physical address.
32-33	50-51	2	RXOFF2h: RXOFF2l	RX power offset 2; signed twos-complement; MSB is at lower physical address.
34-35	52-53	2	RXSLP3h: RXSLP3l	RX power slope 3; unsigned fixed-point; MSB is at lower physical address.
36-37	54-55	2	RXOFF3h: RXOFF3l	RX power offset 3; signed twos-complement; MSB is at lower physical address.
38-39	56-57	2	RXSLP4h: RXSLP4l	RX power slope 4; unsigned fixed-point; MSB is at lower physical address.
3A-3B	58-59	2	RXOFF4h: RXOFF4l	RX power offset 4; signed twos-complement; MSB is at lower physical address.
3C-3D	60-61	2	RXSLP5h: RXSLP5l	RX power slope 5; unsigned fixed-point; MSB is at lower physical address.
3E-3F	62-63	2	RXOFF5h: RXOFF5l	RX power offset 5; signed twos-complement; MSB is at lower physical address.
40-41	64-65	2	RXSLP6h: RXSLP6l	RX power slope 6; unsigned fixed-point; MSB is at lower physical address.
42-43	66-67	2	RXOFF6h: RXOFF6l	RX power offset 6; signed twos-complement; MSB is at lower physical address.
44-45	68-69	2	RXOFF7h: RXOFF7l	RX power slope 7; signed twos-complement; MSB is at lower physical address.
46-47	70-71	2	RXSLP7h: RXSLP7l	RX power slope 7; signed fixed-point; MSB is at lower physical address.

Table 9. Internal Calibration Coefficient Memory Map – Part II

C/ ADC Result Registers Reading

In the present revision of MIC3001, the ADC result registers should be read as 16 bit registers under internal calibration while under external calibration they should be read as 8 bit registers at the MSB address. For example, TX power should be read under internal calibration as 16 bits at address $A2_h$: 66–67 and under external calibration as 8 bits at address $A2_h$: 66_h.

RXPOT

A programmable, non-volatile digitally controlled potentiometer is provided for adjusting the gain of the receive power measurement signal chain in the analog domain. Five bits in the RXPOT register are used to set and adjust the position of potentiometer. RXPOT functions as a programmable divider or attenuator. It is adjustable in steps from 1:1 (no divider action) down to 1/32 in steps of 1/32. If RXPOT is set to zero, the divider is bypassed completely. There will be no scaling of the input signal, and the resistor network will be disconnected from the VRX pin. At all other settings of RXPOT, there will be a 32k Ω (typical) load seen on VRX.

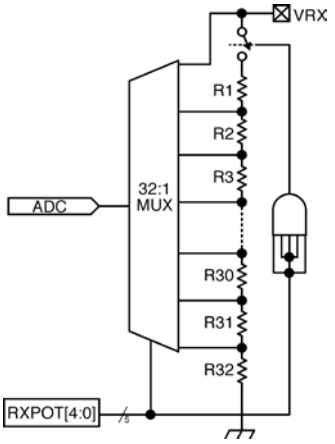


Figure 3. RXPOT Block Diagram

Laser Diode Bias Control

The MIC3001 can be configured to generate a constant bias current using electrical feedback, or regulate average transmitted optical power using a feedback signal from a monitor photodiode, see Figure 4. An operational amplifier is used to control laser bias current via the V_{BIAS} output. The VBIAS pin can drive a maximum of ±10mA. An external bipolar transistor provides current gain. The polarity of the op amp's output is programmable BIASREF in OEMCFG1 in order to accommodate either NPN or PNP transistors that drive common anode and common cathode laser, respectively. Additionally, the polarity of the feedback signal is programmable for use with either common-emitter or emitter-follower transistor circuits.

Furthermore, the reference level for the APC circuit is selectable to accommodate electrical, i.e., current feedback, or optical feedback via a monitor photodiode. Finally, any one of seven different internal feedback resistors can be selected. This internal resistor can be used alone or in parallel with an external resistor. This wide range of adjustability (50:1) accommodates a wide range of photodiode current, i.e, wide range of transmitter output power. The APC operating point can be kept near the mid-scale value of the APC DAC, insuring maximum SNR, maximum effective resolution for digital diagnostics, and the widest possible DAC adjustment range for temperature compensation, etc. See Figure 5.

The APCCAL bit in OEMCAL0 is used to turn the APC function on and off. It will be turned off in the MIC3001's default state as shipped from the factory. When APC is on, the value in the selected APCSETx register is added to the signed value taken from the APC look-up table and loaded into the V_{BIAS} DAC. When APC is off, the V_{BIAS} DAC may be written directly via the V_{BIAS} register, bypassing the look-up table entirely. This provides direct control of the laser diode bias during setup and calibration. In either case, the V_{BIAS} DAC setting is reported in the APCDAC register. The APCCFG bits determine the DACs response to higher or lower numeric values.

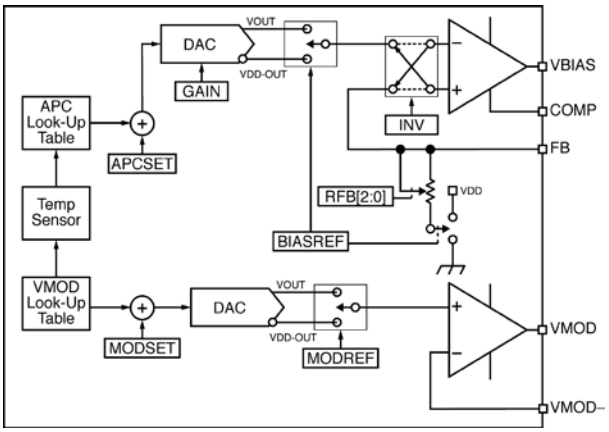


Figure 4. MIC3001 APC and Modulation Control Block Diagram

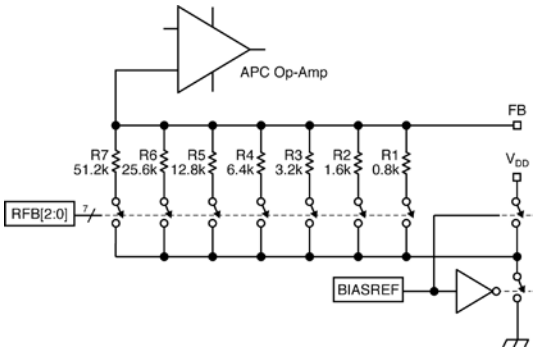


Figure 5. Programmable Feedback Resistor

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Laser Modulation Control

As shown in Figure 4, a temperature-compensated DAC is provided to set and control the laser modulation current via an external laser driver circuit. MODREF in OEMCFG0 selects whether the V_{MOD} DAC output swings up from ground or down from V_{DD}. If the laser driver requires a voltage input to set the modulation current, the MIC3001's V_{MOD} output can drive it directly. If a current input is required, a fixed resistor can be used between the driver and the V_{MOD} output. Several different configurations are possible as shown in Figure 7.

When APC is on, i.e., the APCCAL bit in OEMCAL0 is set to 0, the value corresponding to the current temperature is taken from the MODLUT look-up table, added to MODSET, and loaded into the V_{MOD} DAC. When APC is off, the value in V_{MOD} is loaded directly into the V_{MOD} DAC, bypassing the look-up table entirely. This provides for direct modulation control for setup and calibration. The MODREF bit determines the DACs response to higher or lower numeric values.

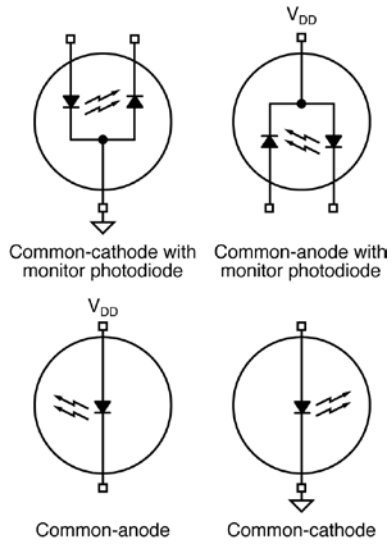
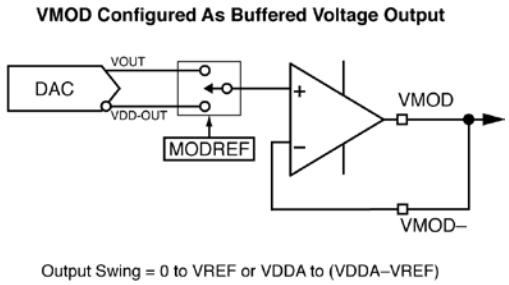


Figure 6. Transmitter Configurations Supported by MIC3001



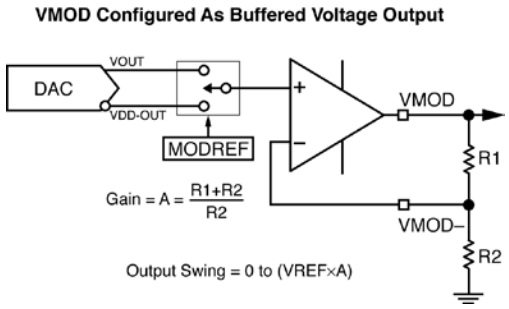


Figure 7. V_{MOD} Configured as Voltage Output with Gain

Power ON and Laser Start-Up

When power is applied, the MIC3001 initializes its internal registers and state machine. This process takes t_{POR}, about 50ms. Following t_{POR}, analog-to-digital conversions begin, serial communication is possible, and the POR bit and data ready bits may be polled. The first set of analog data will be available t_{CONV} after t_{POR}. MIC3001s are shipped from the factory with the output enable bit, OE, set to zero, off. The MIC3001's power-up default state, therefore, is APC off, V_{BIAS}, V_{MOD}, and SHDN outputs disabled. V_{BIAS}, V_{MOD}, and SHDN will be floating (high impedance) and the laser diode, if connected, will be off. Once the device is incorporated into a transceiver and properly configured, the shutdown states of SHDN, V_{BIAS} and V_{MOD} will be determined by the state of the APC configuration and OE bits. Table 10, Table 11, and Table 12 illustrate the shutdown states of the various laser control outputs versus the control bits.

Configuration Bits		Shutdown State
OE	SPOL	SHDN
0	Don't Care	Hi-Z
1	0	≈GND
1	1	≈V_{DD}

Table 10. Shutdown State of SHDN vs. Configuration Bits

Configuration Bits			V_{BIAS} Shutdown State
OE	INV	BIASREF	V_{BIAS}
0	Don't Care	Don't Care	Hi-Z
1	Don't Care	0	≈GND
1	Don't Care	1	≈V_{DD}

Table 11. Shutdown State of V_{BIAS} vs. Configuration Bits

Configuration Bits		V_{MOD} Shutdown State
OE	MODREF	V_{MOD}
0	Don't Care	Hi-Z
1	0	≈GND
1	1	≈V_{DD}

Table 12. Shutdown State of V_{MOD} vs. Configuration Bits

In order to facilitate hot-plugging, the laser diode is not turned on until t_{INIT2} after power-on. Following t_{INIT2}, and assuming TXDISABLE is not asserted, the DACs will be loaded with their initial values. Since t_{CONV} is much less than t_{INIT2}, the first set of analog data, including temperature, is available at t_{INIT2}. Temperature compensation will be applied to the DAC values if enabled. APC will begin if OE is asserted. (If the output enable bit, OE, is not set, the V_{MOD}, V_{BIAS}, and SHDN outputs will float indefinitely.) Figure 8 shows the power-up timing of the MIC3001. If TXDISABLE is asserted at power-up, the V_{MOD} and V_{BIAS} outputs will stay in their shutdown states following MIC3001 initialization. A/D conversions will begin, but the laser will remain off.

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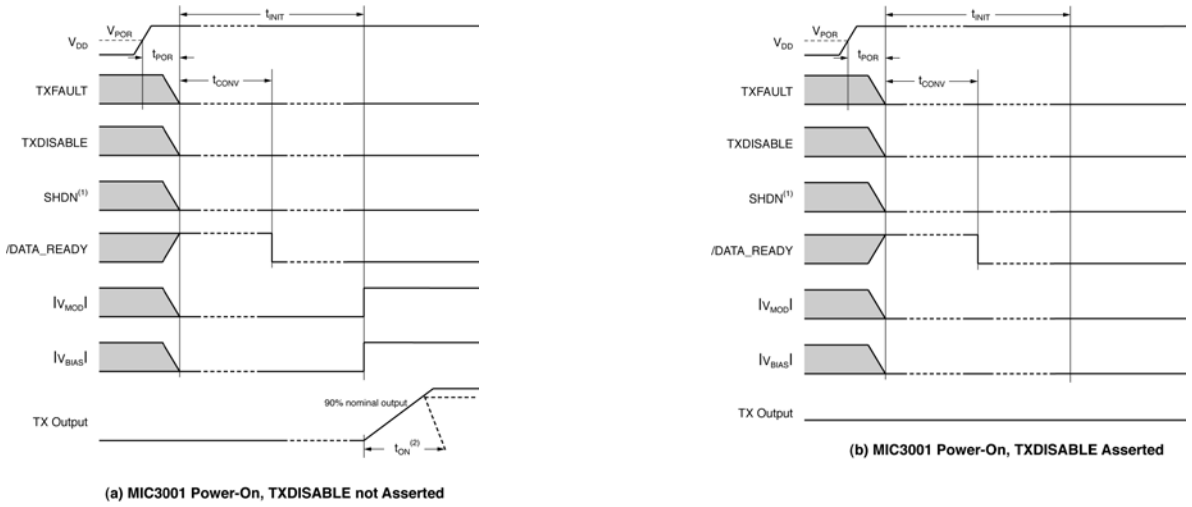


Figure 8. MIC3001 Power-On Timing (OE = 1)

Fault Comparators

In addition to detecting and reporting the events specified in SFF-8472, the MIC3001 also monitors five fault conditions: inadequate supply voltage, thermal diode faults, excessive bias current, excessive transmit power, and APC op-amp saturation. Comparators monitor these parameters in order to respond quickly to fault conditions that could indicate link failure or safety issues, see Figure 9. When a fault is detected, the laser is shut down and TXFAULT is asserted. Each fault source may be independently disabled using the FLTMSK register. FLTMSK is non-volatile, allowing faults to be masked only during calibration and testing or permanently.

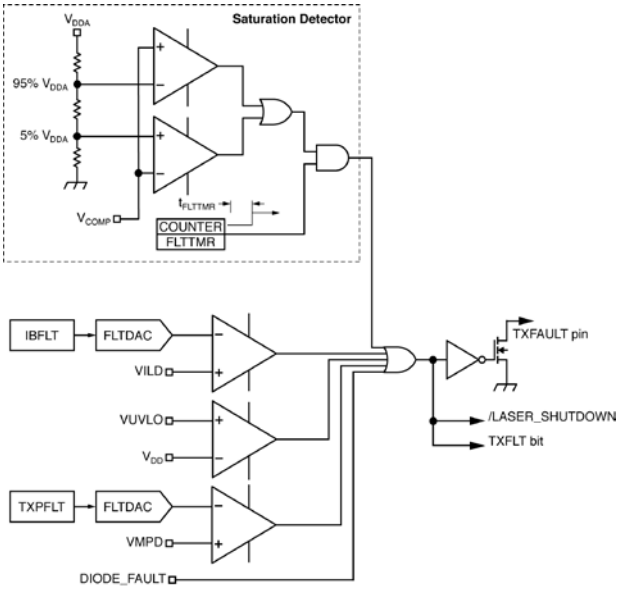


Figure 9. Fault Comparator Logic

Thermal diode faults are detected within the temperature measurement subsystem when an out-of-range signal is detected. A window comparator circuit monitors the voltage on the compensation capacitor to detect APC op-amp saturation (Figure 10). Op-amp saturation indicates that some fault has occurred in the control loop such as loss of feedback. The saturation detector is blanked for a time, tFLTTMR, following laser turn-on since the compensation voltage will essentially be zero at turn-on. The FLTTMR interval is programmable from 0.5ms to 127ms (typical) in increments of 0.5ms (fFLTTMR). Note that a saturation comparator cannot be relied upon to meet certain eye-safety standards that require 100ms response times. This is because the operation of a saturation detector is limited by the loop bandwidth, i.e., the choice of C_{COMP}. Even if the comparator itself was very fast, it would be subject to the limited slew-rate of the APC op-amp. Only the other fault comparator channels will meet <100ms timing requirements.

The MIC3001 can also except and respond to fault inputs from external devices. See “SHDN and TXFIN” section.

A similar comparator circuit monitors received signal strength and asserts RXLOS when loss-of-signal is detected (Figure 11). RXLOS will be asserted when and if VRX drops below the level programmed in LOSFLT. Hysteresis is implemented such that RXLOS will be de-asserted when VRX subsequently rises above the level programmed in LOSFLTn. The loss-of-signal comparator may be disabled completely by setting the LOSDIS bit in OEMCFG3. Once the LOS comparator is disabled, an external device may drive RXLOS. The state of the RXLOS pin is reported in the CNTRL register regardless of whether it is driven by the internal comparator or by an external device. A programmable digital-to-analog converter provides the comparator reference voltages for monitoring received signal strength, transmit power, and bias current. Glitches less than 10ms (typical) in length are rejected by

the fault comparators. Since laser bias current varies greatly with temperature, there is a temperature compensation look-up table for the bias current fault DAC value.

When a fault condition is detected, the laser will be immediately shutdown and TXFAULT will be asserted. The V_{MOD}, V_{BIAS}, and SHDN (if enabled) outputs will be driven to their shutdown state according to the state of the configuration bits. The shutdown states of V_{MOD}, V_{BIAS}, and SHDN versus the configuration bit settings are shown in Table 10, Table 11, and Table 12.

SHDN and TXFIN

SHDN and TXFIN are optional functions of pin 7. SHDN is an output function and is designed to drive a redundant safety switch in the laser current path. TXFIN is an input function and serves as an input for fault signals from external devices that must be reported to the host via TXFAULT. The SHDN function is designed for applications in which the MIC3001 is performing all APC and laser management tasks. The TXFIN function is for situations in which an external device such as a laser diode driver IC is performing laser management tasks, including fault detection.

If the TXFIN bit in OEMCFG3 is zero (the default mode), SHDN will be activated anytime the laser is supposed to be off. Thus, it will be active if 1) TXDISABLE is asserted, 2) STXDIS in CNTRL, is set, or 3) a fault is detected. SHDN is a push-pull logic output. Its polarity is programmable via the SPOL bit in OEMCFG1.

If TXFIN is set to one, pin 7 serves as an input that accepts fault signals from external devices such as laser diode driver ICs. Multiple TXFAULT signals cannot simply be wire-ORed together as they are open-drain and active high. The input polarity is programmable via the TXFPOL bit in OEMCFG3. TXFIN is logically ORed with the MIC3001's internal fault sources to produce TXFAULT and determine the value of the transmit fault bit in CNTRL. See Figure 9.

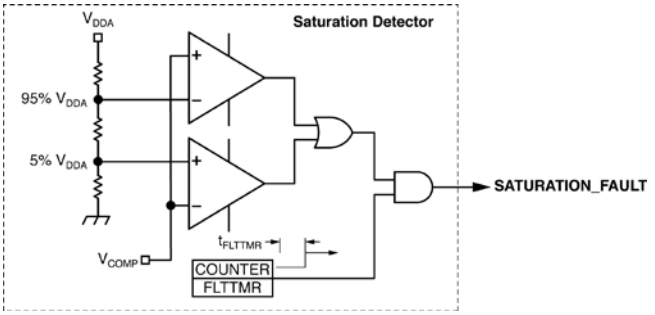


Figure 10. Saturation Detector

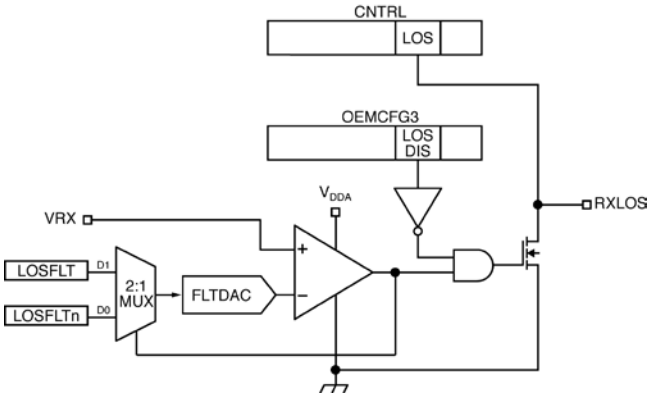


Figure 11. RXLOS Comparator Logic

Temperature Measurement

The temperature-to-digital converter for both internal and external temperature data is built around a switched current source and an eight-bit analog-to-digital converter. The temperature is calculated by measuring the forward voltage of a diode junction at two different bias current levels. An internal multiplexer directs the current source's output to either an internal or external diode junction. The value of the ZONE bit in OEMCFG1 determines whether readings are taken from the on-chip sensor or from the XPN input. The external PN junction may be embedded in an integrated circuit, or it may be a diode-connected discrete transistor. This data is also used as the input to the temperature compensation look-up tables. Each time temperature is sampled and an updated value acquired, new corrective values for IMOD and the APC setpoint are read from the corresponding tables, added to the set values, and transferred to DACs.

Diode Faults

The MIC3001 is designed to respond in a failsafe manner to hardware faults in the temperature sensing circuitry. If the connection to the sensing diode is lost or the sense line is shorted to V_{DD} or ground, the temperature data reported by the A/D converter will be forced to its full-scale value (+127°C). The diode fault flag, DFLT, will be set in OEMCFG1, TXFAULT will be asserted, and the high temperature alarm and warning flags will be set. The reported temperature will remain +127°C until the fault condition is cleared. Diode faults may be reset by toggling TXDISABLE, as with any other fault. Diode faults will not be detected at power up until the first A/D conversion cycle is completed. Diode faults are not reported while TXDISABLE is asserted.

Temperature Compensation

Since the performance characteristics of laser diodes and photodiodes change with operating temperature, the MIC3001 provides a facility for temperature compensation of the A.P.C. loop setpoint, laser modulation current, bias current fault comparator threshold, and bias current high alarm flag threshold. Temperature compensation is

performed using a look-up table (LUT) that stores values corresponding to each measured temperature over a 128°C span. Four identical tables reside at serial address A4h as summarized in Table 13. The range of temperatures spanned by the tables is programmable via the LUTOFF register. Each table entry is a signed twos complement number that is used as an offset to the parameter being compensated. The default value of all table entries is zero, giving a flat response.

The A/D converter reports a new temperature sample each t_{CONV}. This occurs at roughly 10Hz. To prevent temperature oscillation due to thermal or electrical noise, sixteen successive temperature samples are averaged together and used to index the LUTs. Temperature compensation results are therefore updated at $16xt_{CONV}$ intervals, or about 1.6 seconds. This can be expressed as shown in Equation10.

$$T_{COMPm} = \frac{T_n + T_{n+1} + T_{n+2} + \bullet\bullet\bullet T_{n+15}}{16} \quad (10)$$

Each time an updated average value is acquired, a new offset value for the APC setpoint is read from the corresponding look-up table (see Table 14) and transferred to the APC circuitry. This is illustrated in Equation 11. In a same way, new offset values are taken from similar look-up tables (see Table 15 and Table 16), added to the nominal values and transferred into the modulation and fault comparator DACs. The bias current high alarm threshold, is compensated using a fourth look-up table (see Table 17). This compensation happens internally and does not affect any host-accessible registers.

$$APCSET_m \Big|_{Table\_min \le T_{COMPm} \le Table\_max} = APCSETx + APCLUT(T_{COMPm})$$

$$APCSET_m \Big|_{T_{COMP} > Table\_max} = APCSETx + APCLUT(max)$$

$$APCSET_m \Big|_{T_{COMP} < Table\_min} = APCSETx + APCLUT(min) \quad (11)$$

If the measured temperature is greater than the maximum table value, the highest value in each table is used. If the measured temperature is less than the minimum, the minimum value is used. Hysteresis is employed to further enhance noise immunity and prevent oscillation about a table threshold. Each table entry spans two degrees C. The table index will not change unless the new temperature average results in a table index beyond the midpoint of the next entry in either direction. There is therefore 2 to 3°C of hysteresis on temperature compensation changes. The table index will never oscillate due to quantization noise as the hysteresis is much larger than ±1 ⁄2 LSB.

Byte Addresses	Function
00h–3Fh	APC Look-up Table
40h–7Fh	I_{MOD} Look-up Table
80h–BFh	IFLT Look-up Table
C0h–FFh	Bias High Alarm Look-up Table

Table 13. Temperature Compensation Look-up Tables, Serial Address I2CADR + 4_h

Register Address	Table Offset	Temperature Offset (°C)
00h	0	0
		1
01h	1	2
		3
02h	2	4
		5
•	•	•
•	•	•
•	•	•
3Eh	62	124
		125
3Fh	63	126
		127

Table 14. APC Temperature Compensation Look-Up Table, Serial Address 12C ADR+4_h

Register Address	Table Offset	Temperature Offset (°C)
40h	0	0
		1
41h	1	2
		3
42h	2	4
		5
•	•	•
•	•	•
•	•	•
7Eh	62	124
		125
7Fh	63	126
		127

Table 15. V_{MOD} Temperature Compensation Look-Up Table, Serial Address 12C ADR+4_h

Register Address	Table Offset	Temperature Offset (°C)
80h	0	0
		1
81h	1	2
		3
82h	2	4
		5
•	•	•
•	•	•
•	•	•
8Eh	62	124
		125
8Fh	63	126
		127

Table 16. I_{BIAS} Comparator Temperature Compensation Look-Up Table, Serial Address 12C ADR+4_h

Register Address	Table Offset	Temperature Offset (°C)
C0h	0	0
		1
C1h	1	2
		3
C2h	2	4
		5
•	•	•
•	•	•
•	•	•
FEh	62	124
		125
FFh	63	126
		127

Table 17. BIAS Current High Alarm Temperature Compensation Table, Serial Address 12C ADR+4_h

The LUTOFF register determines the range of measured temperatures that are actually spanned by the tables. The temperature span of the tables versus the value of LUTOFF is given in Table 18.

LUTOFF	Temperature Span t_{COMP} (min) – t_{COMP} (max)
00h	0°C to 127°C
01h	–2°C to 125°C
02h	–4°C to +123°C
•	•
•	•
•	•
0Fh	–30°C to 97°C

Table 18. Range of Temperature Compensation Table vs. LUTOFF

The internal state machine calculates a new table index each time a new average temperature value becomes available. This table index is derived from the average temperature value and LUTOFF. The table index is then converted into a table address for each of the four look-up tables. These operations can be expressed as:

$$INDEX = \left| \frac{T_{AVG(n)}}{2} \right| + LUTOFF \quad (12)$$

where TAVG(n) is the current average temperature; and

TABLE_ADDRESS=INDEX+BASE_ADDRES

where BASE_ADDRESS is the physical base address of each table, i.e., 00_h, 40_h, 80_h, or $C0_h$ (all tables reside in the I2CADR+4 page of memory).

At any given time, the current table index can be read in the LUTINDX register.

Figures 12 and 13 illustrate the operation of the temperature compensation tables.

Figure 12 is a graphical illustration of the use of the LUTOFF register to control the temperature range spanned by the temperature compensation tables. Note that, if the LUTINDX becomes greater than 63 or less than zero, the maximum or minimum table value is used, respectively. The tables do not “roll over.”

Figure 13 llustrates that the table values are used as offsets to the nominal value of the parameter in question. APCSET is used as an example, but all four tables function identically. Note that the shape and magnitude of the compensation curve do not change as the nominal value changes.

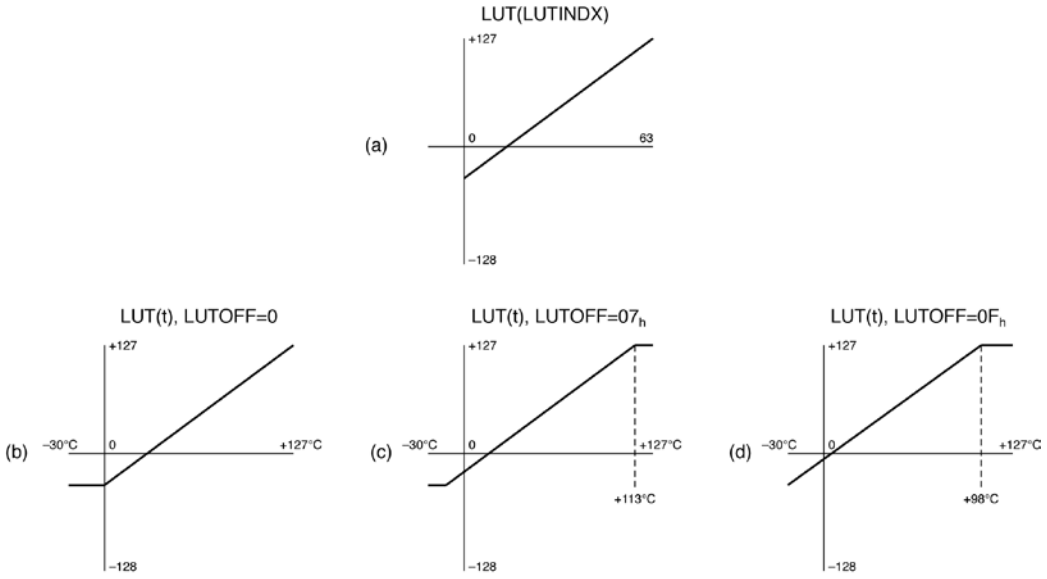


Figure 12. Examples of LUTOFF Operation

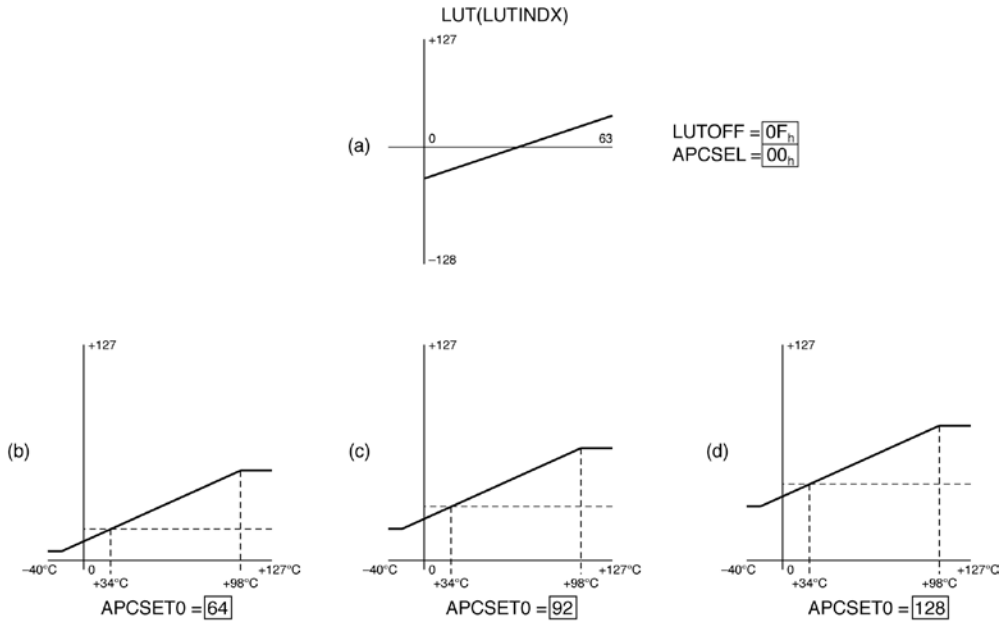


Figure 13. Temperature Compensation Examples

Alarms and Warning Flags

There are twenty different conditions that will cause the MIC3001 to set one of the bits in the WARNx or ALARMx registers. These conditions are listed in Table 19. The less critical of these events generate warning flags by setting a bit in WARN0 or WARN1. The more critical events cause bits to be set in ALARM0 or ALARM1.

An event occurs when any alarm or warning condition becomes true. Each event causes its corresponding status bit in ALARM0, ALARM1, WARN0, or WARN1 to be set. This action cannot be masked by the host. The status bit will remain set until the host reads that particular status register, a power on-off cycle occurs, or the host toggles TXDISABLE.

If TXDISABLE is asserted at any time during normal operation, A/D conversions continue. The A/D results for all parameters will continue to be reported. All events will be reported in the normal way. If they have not already been individually cleared by read operations, when TXDISABLE is de-asserted, all status registers will be cleared.

Control and Status I/O

The logic for the transceiver control and status I/O is shown schematically in Figure 14. Note that the internal drivers on RXLOS, RATE_SELECT, and TXFAULT are all open-drain. These signals may be driven either by the internal logic or external drivers connected to the corresponding MIC3001 pins. In any case, the signal level appearing at the pins of the MIC3001 will be reported in the control register status bits.

Note that the control bits for TX_DISABLE and RATE_SELECT and the status bits for TXFAULT and RXLOS do not meet the timing requirements specified in the SFP MSA or the GBIC Specification, revision 5.5 (SFF-8053) for the hardware signals. The speed of the serial interface limits the rate at which these functions can be manipulated and/or reported. The response time for the control and status bits is given in the “Electrical Characteristics” section.

Event	Condition	MIC3001 Response
Temperature high alarm	TEMP > TMAX	Set ALARM0[7]
Temperature low alarm	TEMP < TMIN	Set ALARM0[6]
Voltage high alarm	VIN > VMAX	Set ALARM0[5]
Voltage low alarm	VIN < VMIN	Set ALARM0[4]
TX bias high alarm	IBIAS > IBMAX	Set ALARM0[3]
TX bias low alarm	IBIAS < IBMIN	Set ALARM0[2]
TX power high alarm	TXOP > TXMAX	Set ALARM0[1]
TX power low alarm	TXOP < TXMIN	Set ALARM0[0]
RX power high alarm	RXOP > RXMAX	Set ALARM1[7]
RX power low alarm	RXOP < RXMIN	Set ALARM1[6]
Temperature high warning	TEMP > THIGH	Set WARN0[7]
Temperature low warning	TEMP < TLOW	Set WARN0[6]
Voltage high warning	VIN > VHIGH	Set WARN0[5]
Voltage low warning	VIN < VLOW	Set WARN0[4]
TX bias high warning	IBIAS > IBHIGH	Set WARN0[3]
TX bias low warning	IBIAS < IBLOW	Set WARN0[2]
TX power high warning	TXOP > TXHIGH	Set WARN0[1]
TX power low warning	TXOP < TXLOW	Set WARN0[0]
RX power high warning	RXOP > RXHIGH	Set WARN1[7]
RX power low warning	RXOP < RXLOW	Set WARN1[6]
Temperature high alarm	TEMP > TMAX	Set ALARM0[7]

Table 19. MIC3001 Events

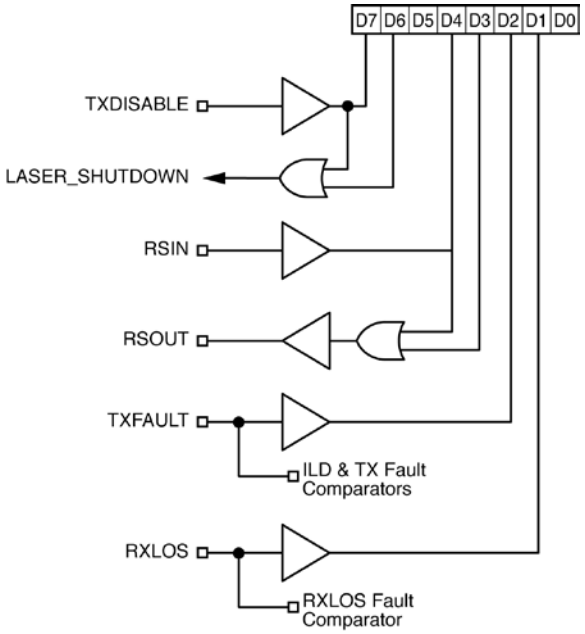


Figure 14. Control and Status I/O Logic

System Timing

The timing specifications for MIC3001 control and status I/O are given in the “Electrical Characteristics” section.

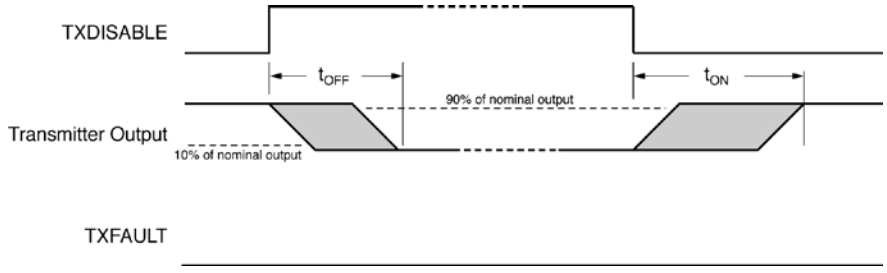


Figure 15. Transmitter ON-OFF Timing

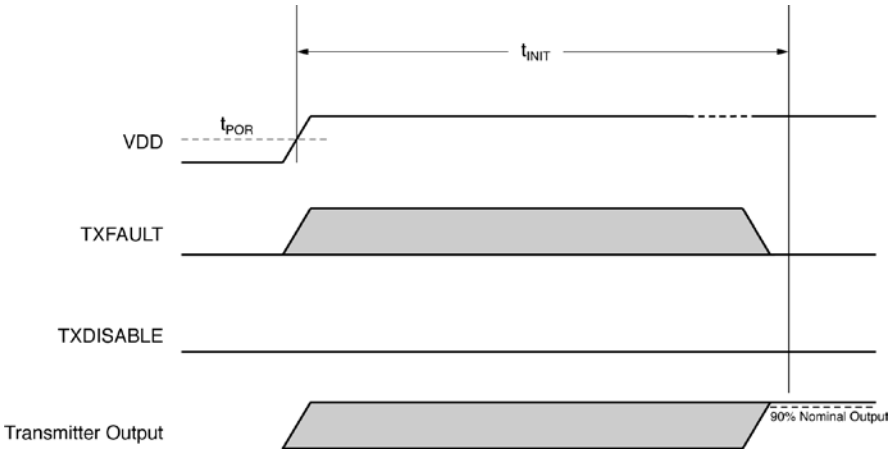


Figure 16. Initialization Timing with TXDISABLE Asserted

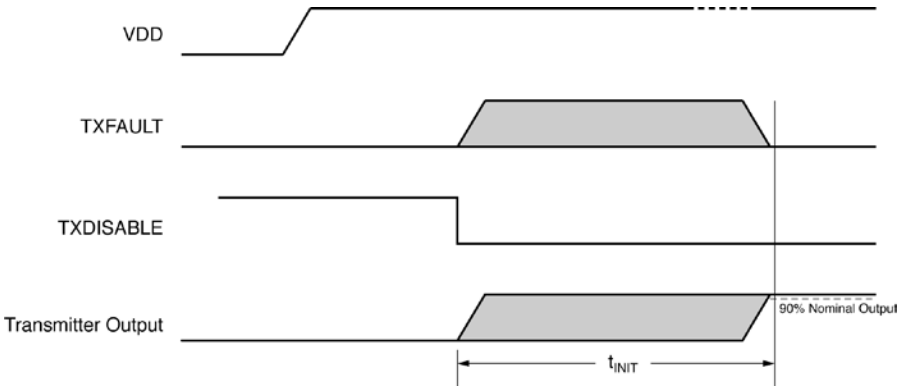


Figure 17. Initialization Timing with TXDISABLE Not Asserted

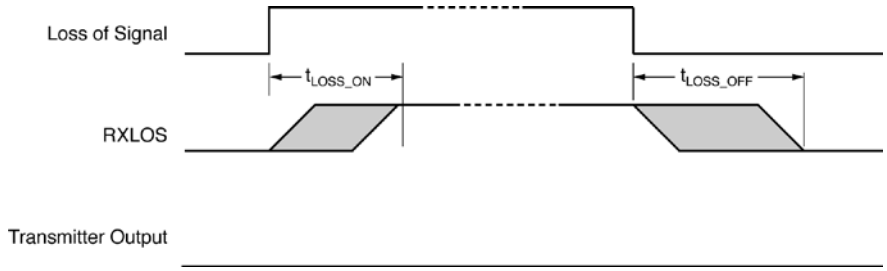


Figure 18. Loss-of-Signal (LOS) Timing

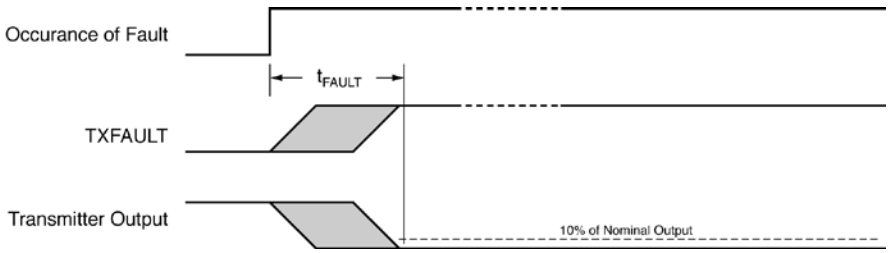


Figure 19. Transmit Fault Timing

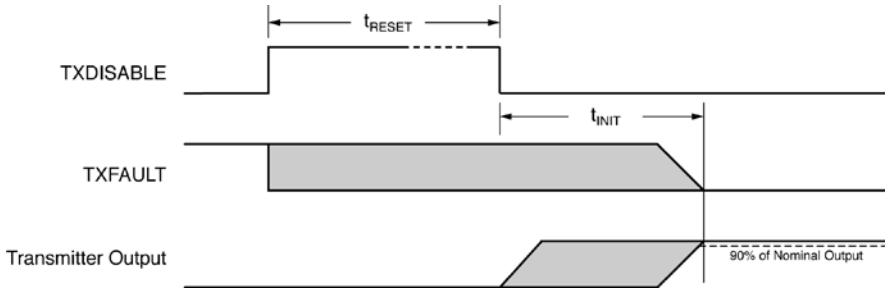


Figure 20. Successfully Clearing a Fault Condition

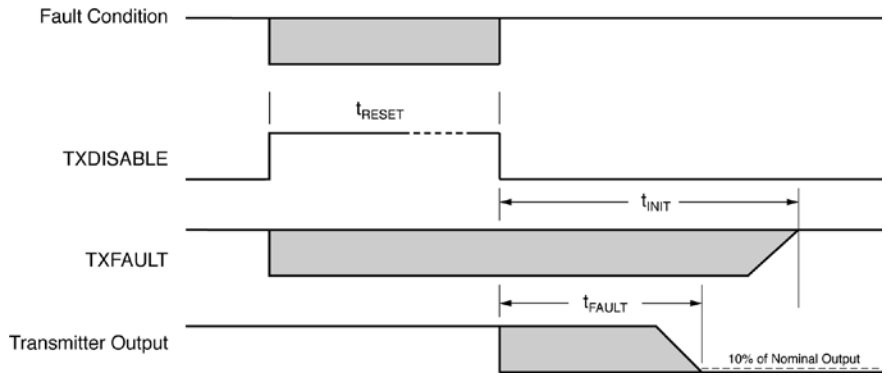


Figure 21. Unsuccessful Attempt to Clear a Fault

Warm Resets

The MIC3001 can be reset to its power-on default state during operation by setting the reset bit in OEMCFG0. When this bit is set, TXFAULT and RXLOS will be de-asserted, all registers will be restored to their normal power-on default values, and any A/D conversion in progress will be halted and the results discarded. The state of the MIC3001 following this operation is indistinguishable from a power-on reset.

Power-On Hour Meter

The Power-On Hour meter logs operating hours using an internal real-time clock and stores the result in NVRAM. The hour count is incremented at ten-hour intervals in the middle of each interval. The first increment therefore takes place five hours after power-on. Time is accumulated whenever the MIC3001 is powered. The hour meter's timebase is accurate to 5% over all MIC3001 operating conditions. The counter is capable of storing counts of more than thirty years, but is ultimately limited by the write-cycle endurance of the non-volatile memory. This implies a range of at least twenty years. Actual results will depend on the operating conditions and write-cycle endurance of the part in question.

Two registers, POHH and POHl, contain a 15-bit power-on hour measurement and an error flag, POHFLT. Great care has been taken to make the MIC3001's hour meter immune to data corruption and to insure that valid data is maintained across power cycles. The hour meter employs multiple data copies and error correction codes to maintain data validity. This data is stored in the POHDATA registers. If POHFLT is set, however, the power-on hour meter data has been corrupted and should be ignored.

It is recommended that a two-byte (or more) sequential read operation be performed on POHh and POHI to insure coherency between the two registers. These registers are accessible by the OEM using a valid OEM password. The only operation that should be performed on these registers is to clear the hour meters initial value, if necessary, at the time of product shipment. The hour meter result may be cleared by setting all eight POHDATA bytes to 00_h.

Power-On Hour Result Format		
High Byte, POHH		Low Byte, POHI
Error Flag	Elapsed Time / 10 Hours, MSBs	Elapsed Time / 10 Hours, LSBs
MSB		LSB

Table 20. Power-On Hour Meter Result Format

Test and Calibration Features

Numerous features are included in the MIC3001 to facilitate development, testing, and diagnostics. These features are available via registers in the OEM area. As shown in Table 21, these features include:

Function	Description	Control Register(s)
Analog loop-back	Provides analog visibility of op-amp and DAC outputs via the ADC	OEMCFG0
Fault comparator disable control	Disables the fault comparator	OEMCAL0
Fault comparator spin-on-channel mode	Selects a single fault comparator channel	OEMCAL0
Fault comparator output read-back	Allows host to read individual fault comparator outputs	OEMRD
RSOUT, /INT read-back	Allows host to read the state of these pins	OEMRD
Inhibit EEPROM write cycles	Speeds repetitive writes to registers backed up by NVRAM	OEMCAL0
APC calibration mode	Allows direct writes to MODDAC and APCDAC (temperature compensation not used)	OEMCAL0
Continuity checking	Forcing of RXLOS, TXFAULT, /INT	OEMCAL0
Halt A/D	Stops A/D conversions; ADC in one-shot mode	OEMCAL1
ADC idle flag	Indicates ADC status	OEMCAL1
A/D one-shot mode	Performs a single A/D conversion on the selected input channel	OEMCAL1
A/D spin-on-channel mode	Selects a single input channel	OEMCAL1
Channel selection	Selects ADC or fault comparator channel for spin-on-channel modes	OEMCAL1
LUT index read-back	Permits visibility of the LUT index calculated by the state-machine	LUTINDX
Manufacturer and device ID registers	Facilitates presence detection and version control	MFG_ID, DEV_ID

Table 21. Test and Diagnostic Features

Serial Port Operation

The MIC3001 uses standard Write_Byte, Read_Byte, and Read_Word operations for communication with its host. It also supports Page_Write and Sequential_Read transactions. The Write_Byte operation involves sending the device's slave address (with the R/W bit low to signal a write operation), followed by the address of the register to be operated upon and the data byte. The Read_Byte operation is a composite write and read operation: the host first sends the device's slave address followed by the register address, as in a write operation. A new start bit must then be sent to the MIC3001, followed by a repeat of the slave address with the R/W bit (LSB) set to the high (read) state. The data to be read from the part may then be clocked out. A Read_Word is similar, but two successive data bytes are clocked out rather than one. These protocols are shown in Figure 22 to 25.

The MIC3001 will respond to up to four sequential slave addresses depending on whether it is in OEM or User mode. A match between one of the MIC3001's addresses and the address specified in the serial bit stream must be made to initiate communication. The MIC3001 responds to slave addresses $A0_h$ and $A2_h$ in User Mode; it also responds to $A4_h$ and $A6_h$ in OEM Mode (assuming I2CADR = Ax_h).

Page Writes

To increase the speed of multi-byte writes, the MIC3001 allows up to four consecutive bytes (one page) to be written before the internal write cycle begins. The entire non-volatile memory array is organized into four-byte pages. Each page begins on a register address boundary where the last two bits of the address are 00_b. Thus the page is composed of any four consecutive bytes having the addresses $xxxxxx00_b$, $xxxxxx01_b$, $xxxxxx10_b$, and $xxxxxx11_b$.

The page write sequence begins just like a Write_Byte operation with the host sending the slave address, R/W bit low, register address, etc. After the first byte is sent the host should receive an acknowledge. Up to three more bytes can be sent in sequence. The MIC3001 will acknowledge each one and increment its internal address register in anticipation of the next byte. After the last byte is sent, the host issues a STOP. The MIC3001's internal write process then begins. If more than four bytes are sent, the MIC3001's internal address counter wraps around to the beginning of the four-byte page.

To accelerate calibration and testing, NVRAM write cycles can be disabled completely by setting the WRINH bit in OEMCAL0. Writes to registers that do not have NVRAM backup will not incur write-cycle delays when writes are inhibited. Write operations on registers that exist only in NVRAM will still incur write cycle delays.

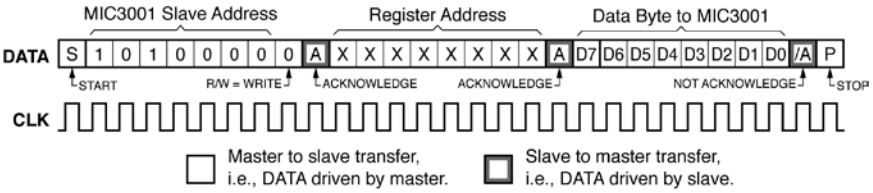


Figure 22. Write Byte Protocol

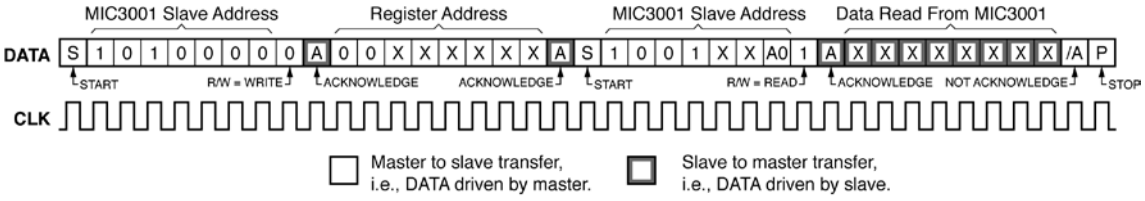


Figure 23. Read Byte Protocol

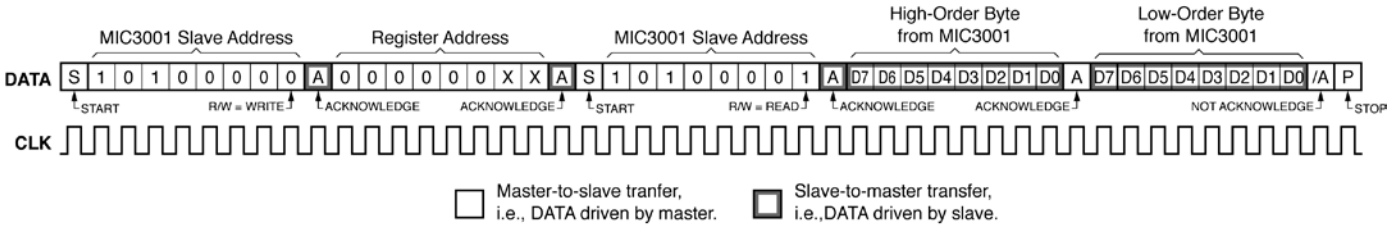


Figure 24. Read_Word Protocol

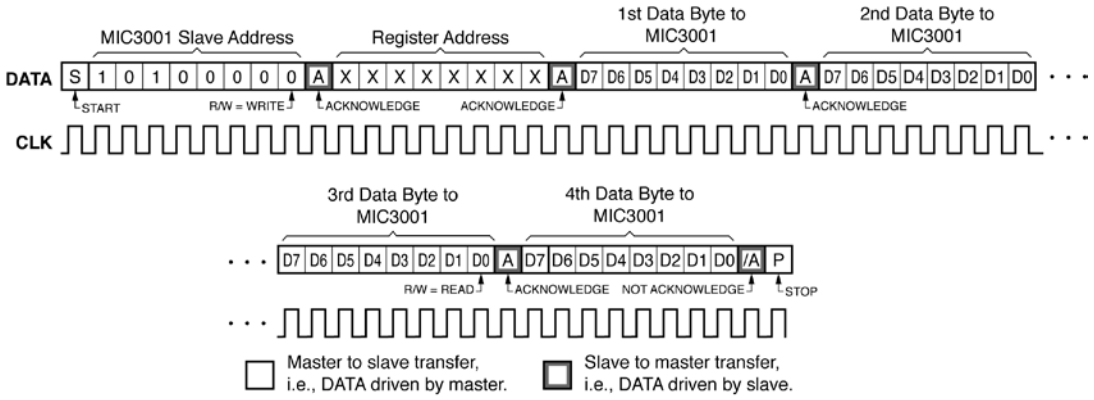


Figure 25. Four-Byte Page_White Protocol

Acknowledge Polling

The MIC3001's non-volatile memory cannot be accessed during the internal write process. To allow for maximum speed bulk writes, the MIC3001 supports acknowledge polling. The MIC3001 will not acknowledge serial bus transactions while internal writes are in progress. The host may therefore monitor for the end of the write process by periodically checking for an acknowledgement.

Write Protection and Data Security

OEM Password

A password is required to access the OEM areas of the MIC3001, specifically the non-volatile memory, look-up tables, and registers at serial addresses $A4_h$ and $A6_h$. A four-byte field, OEMPWSET, at serial address $A6_h$ is used for setting the OEM password. The OEM password is set by writing OEMPWSET with the new value. The password comparison is performed following the write to the MSB of the OEMPW, address $7B_h$ at serial address $A2_h$. **Therefore, this byte must be written last!** A four-byte burst-write sequence to address 78_h may be used as this will result in the MSB being written last. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect.

The corresponding four-byte field for password entry, OEMPW, is located at serial address $A2_h$. This field is therefore always visible to the host system. OEMPW is compared to the four-byte OEMPWSET field at serial address $A6_h$. If the two fields match, access is allowed to the OEM areas of the MIC3001 non-volatile memory at serial addresses $A4_h$ and $A6_h$. If OEMPWSET is all zeroes, no password security will exist. The value in OEMPW will be ignored. This helps prevent a deliberately unsecured MIC3001 from being inadvertently locked. Once a valid password is entered, the MIC3001 OEM areas will be accessible. The OEM areas may be re-secured by writing an incorrect password value at OEMPW, e.g., all zeroes. In all cases OEMPW must be written LSB first through MSB last. The OEM areas will be inaccessible following the final write operation to OEMPW's LSB. The OEMPW field is reset to all zeros at power on. Any values written to these locations will be readable by the host regardless of the locked/unlocked status of the device. If OEMPWSET is set to zero (00000000_h), the MIC3001 will remain unlocked regardless of the contents of the OEMPW field. This is the factory default security setting.

NOTE: A valid OEM password allows access to the OEM and user areas of the chip, i.e., the entire memory map, regardless of any user password that may be in place. Once the OEM areas are locked, the user password can provide access and write protection for the user areas.

User Password

A password is required to access the USER areas of the MIC3001, specifically the non-volatile memory at serial addresses $A0_h$ and $A2_h$. A one-byte field, USRPWSET at serial address $A2_h$ is used for setting the USER password. USRPWSET is compared to the USRPW field at serial address $A2_h$. If the two fields match, access is allowed to the USER areas of the MIC3001 non-volatile memory at serial addresses $A0_h$ and $A2_h$. The USER password is set by writing USRPWSET with the new value. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect.

NOTE: A valid OEM password allows access to the OEM and user areas of the chip, i.e., the entire memory map, regardless of any user password that may be in place. Once the OEM areas are locked, the user password can provide access and write protection for the user areas. If a valid OEM password is in place, the user password will have no effect.

Detailed Register Descriptions

Note: Serial bus addresses shown assume that I2CADR = Ax_h.

Alarm Threshold Registers

Temperature High Alarm Threshold MSB (TMAXh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			00 = 00_h				
Each LSB represents one degree centigrade. This register is to be used in conjunction with TMAXl to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The value in TMAXh is compared against TEMPh. Alarm bit Ax is set if TEMPh > TMAXh.							

Temperature High Alarm Threshold LSB (TMAXh)					
D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)		
Serial Address			$A2_h$ = 1010001_b		
Byte Address			01 = 01_h		
This register is to be used in conjunction with TMAXh to yield a sixteen-bit temperature value. The value in TMAXh is compared against TEMPh. Alarm bit Ax is set if TMAXh > TEMPh. Since TEMPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.					

Temperature Low Alarm Threshold MSB (TMINh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			02 = 02_h				
Each LSB represents one degree centigrade. This register is to be used in conjunction with TMINl to yield a sixteen-bit temperature value. The value in TMINh is compared against TEMPh. Alarm bit Ax is set if TEMPh < TMINh.							

Temperature Low Alarm Threshold LSB (TMINl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			03 = 03_h				
This register is to be used in conjunction with TMINh to yield a sixteen-bit temperature value. The value in TMINh is compared against TEMPh. Alarm bit Ax is set if TEMPh < TMINh. Since TEMPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Voltage High Alarm Threshold MSB(VMAXh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0V)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			08 = 08_h				
Each LSB represents 25.6mV. This register is to be used in conjunction with VMAXl to yield a sixteen-bit value. The value in TMINh is compared against VINh. Alarm bit Ax is set if VINh > VMAXh.							

Voltage High Alarm Threshold LSB(VMAXl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0V)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			09 = 09_h				
Each LSB represents 100μV. This register is to be used in conjunction with VINh to yield a sixteen-bit value. The value in VMAXh is compared against VINh. Alarm bit Ax is set if VINh > VMAXh. Since VINl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Voltage Low Alarm Threshold MSB (VMINh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0V)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			10 = $0A_h$				
Each LSB represents 25.6mV. This register is to be used in conjunction with VMINl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in VMINh is compared against VINh. Alarm bit Ax is set if VINh<VMINh.							

Voltage Low Alarm Threshold LSB (VMINl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0V)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			11 = $0B_h$				
Each LSB represents 100μV. This register is to be used in conjunction with VINh to yield a sixteen-bit value. The value in VMINh is compared against VINh. Alarm bit Ax is set if VINh < VMINh. Since VINl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Bias Current High Alarm Threshold MSB (IMAXh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$16 = 10_h$				
This register is to be used in conjunction with IMAXl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in IMAXh is compared against ILDh. Alarm bit Ax is set if ILDh > IMAXh.							

Bias Current High Alarm Threshold LSB (IMAXl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$17 = 11_h$				
Each LSB represents 2μA. This register is to be used in conjunction with IMAXh to yield a sixteen-bit value. The value in this register is uncalibrated. The value in IMAXh is compared against ILDh. Alarm bit Ax is set if ILDh > IMAXh. Since ILDl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Bias Current Low Alarm Threshold MSB (IMINh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$18 = 12_h$				
This register is to be used in conjunction with IMINl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in IMINh is compared against ILDh. Alarm bit Ax is set if ILDh < IMINh.							

Bias Current Low Alarm Threshold LSB (IMINl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$19 = 13_h$				
Each LSB represents 2μA. This register is to be used in conjunction with IMINh to yield a sixteen-bit value. The value in this register is uncalibrated. The value in IMINh is compared against ILDh. Alarm bit Ax is set if ILDh < IMINh. Since ILDl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

TX Optical Power High Alarm MSB (TXMAXh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$24 = 18_h$				
Each LSB represents 25.6μW. This register is to be used in conjunction with TXOPl to yield a sixteen-bit value. The values in TXOPh:TXOPl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXMAXh is compared against TXOPh. Alarm bit Ax is set if TXOPh > TXMAXh.							

TX Optical Power High Alarm LSB (TXMAXl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$25 = 19_h$				
Each LSB represents 0.1μW. This register is to be used in conjunction with TXMAXh to yield a sixteen-bit value. The values in TXOPh:TXOPl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXMAXh is compared against TXOPh. Alarm bit Ax is set if TXOPh > TXMAXh. Since TXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

TX Optical Power Low Alarm MSB (TXMINh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$26 = 1A_h$				
Each LSB represents 25.6μW. This register is to be used in conjunction with TXMINl to yield a sixteen-bit value. The values in TXMINh:TMINl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXMINh is compared against TXOPh. Alarm bit Ax is set if TXOPh < TXMINh.							

TX Optical Power Low Alarm LSB (TXMINl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$27 = 1B_h$				
Each LSB represents 0.1μW. This register is to be used in conjunction with TXMINh to yield a sixteen-bit value. The values in TXOPh:TXOPl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXMINh is compared against TXOPh. Alarm bit Ax is set if TXOPh < TXMINh. Since TXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

RX Optical Power High Alarm Threshold MSB (RXMAXh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$32 = 20_h$				
Each LSB represents 25.6μW. This register is to be used in conjunction with RXMAXl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in RXMAXh is compared against RXOPh. Alarm bit Ax is set if RXOPh > RXMAXh.							

RX Optical Power High Alarm Threshold LSB (RXMAXl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$33 = 21_h$				
Each LSB represents 0.1μW. This register is to be used in conjunction with RXMAXh to yield a sixteen-bit value. The values in RXMAXh:RXMAXl are in an unsigned binary format. The value in this register is uncalibrated. The value in RXMAXh is compared against RXOPh. Alarm bit Ax is set if RXOPh > RXMAXh. Since RXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

RX Optical Power Low Alarm Threshold MSB (RMINh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			34 = 22h				
Each LSB represents 25.6μW. This register is to be used in conjunction with RXMINl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in RXMINh is compared against RXOPh. Alarm bit Ax is set if RXOPh < RXMINh.							

RX Optical Power Low Alarm Threshold LSB (RMINl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$35 = 23_h$				
Each LSB represents 0.1μW. This register is to be used in conjunction with RXMINh to yield a sixteen-bit value. The values in RXMINh:RXMINl are in an unsigned binary format. The value in this register is uncalibrated. The value in RXMINh is compared against RXOPh. Alarm bit Ax is set if RXOPh < RXMINh. Since RXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Warning Threshold Registers

Temperature High Warning Threshold MSB (THIGHh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			04 = 04_h				
Each LSB represents one degree centigrade. This register is to be used in conjunction with THIGHl to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The value in THIGHh is compared against TEMPh. Warning bit Wx is set if TEMPh > THIGHh.							

Temperature High Warning Threshold LSB (THIGHl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			05 = 05_h				
This register is to be used in conjunction with THIGHh to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The value in THIGHh is compared against TEMPh. Warning bit Wx is set if THIGHh > TEMPh. Since TEMPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Temperature Low Warning Threshold MSB (TLOWh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			06 = 06_h				
Each LSB represents one degree centigrade. This register is to be used in conjunction with TLOWl to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The value in TLOWh is compared against TEMPh. Warning bit Wx is set if TEMPh < TLOWh.							

Temperature Low Warning Threshold LSB (TLOWl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0°C)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			07 = 07_h				
This register is to be used in conjunction with TLOWh to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The value in TLOWh is compared against TEMPh. Warning bit Wx is set if TEMPh < TLOWh. Since TEMPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Voltage High Warning Threshold MSB (VHIGHh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0V)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$12 = 0C_h$				
Each LSB represents 25.6mV. This register is to be used in conjunction with VHIGHl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in VHIGHh is compared against VINh. Warning bit Wx is set if VINh > VHIGHh.							

Voltage High Warning Threshold LSB (VHIGHl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0V)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$13 = 0D_h$				
Each LSB represents 100µV. This register is to be used in conjunction with VHIGHh to yield a sixteen-bit value. The value in VHIGHh is compared against VINh. Warning bit Wx is set if VINh > VHIGHh. Since VINl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Voltage Low Warning Threshold MSB (VLOWh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0V)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$14 = 0E_h$				
Each LSB represents 25.6mV. This register is to be used in conjunction with VLOWl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in VLOWh is compared against VINh. Warning bit Wx is set if VINh < VLOWhh.							

Voltage Low Warning Threshold LSB (VLOWl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0V)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$15 = 0F_h$				
Each LSB represents 100µV. This register is to be used in conjunction with VLOWh to yield a sixteen-bit value. The value in VLOWh is compared against VINh. Warning bit Wx is set if VINh < VLOWh. Since VINl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Bias Current High Warning Threshold MSB (IHIGHh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$20 = 14_h$				
This register is to be used in conjunction with IHIGHl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in IHIGHh is compared against ILDh. Warning bit Wx is set if ILDh > IHIGHh.							

Bias Current High Warning Threshold LSB (IHIGHl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$21 = 15_h$				
Each LSB represents 2μA. This register is to be used in conjunction with IHIGHh to yield a sixteen-bit value. The value in this register is uncalibrated. The value in IHIGHh is compared against ILDh. Warning bit Wx is set if ILDh > IHIGHh. Since ILDl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Bias Current Low Warning Threshold MSB (ILOWh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$22 = 16_h$				
This register is to be used in conjunction with ILOWl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in ILOWh is compared against ILDh. Warning bit Wx is set if ILDh < ILOWh.							

Bias Current Low Warning Threshold LSB (ILOWl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (0mA)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$23 = 17_h$				
Each LSB represents 2μA. This register is to be used in conjunction with ILOWh to yield a sixteen-bit value. The value in this register is uncalibrated. The value in ILOWh is compared against ILDh. Warning bit Wx is set if ILDh < ILOWh. Since ILDl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

TX Optical Power High Warning MSB (TXHIGHh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$28 = 1C_h$				
Each LSB represents 25.6µW. This register is to be used in conjunction with TXHIGHl to yield a sixteen-bit value. The values in TXHIGHh:TXHIGHl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXHIGHh is compared against TXOPh. Warning bit Wx is set if TXOPh > TXHIGHh.							

TX Optical Power High Warning LSB (TXHIGHl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$29 = 1D_h$				
Each LSB represents 0.1µW. This register is to be used in conjunction with TXHIGHh to yield a sixteen-bit value. The values in TXHIGHh:TXHIGHl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXHIGHh is compared against TXOPh. Warning bit Wx is set if TXOPh > TXHIGHh. Since TXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning b.							

TX Optical Power Low Warning MSB (TLOWh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$30 = 1E_h$				
Each LSB represents 25.6µW. This register is to be used in conjunction with TXLOWl to yield a sixteen-bit value. The values in TXLOWh:TLOWl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXLOWh is compared against TXOPh. Warning bit Wx is set if TXOPh < TXLOWh.							

TX Optical Power Low Warning LSB (TLOWl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0mW)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$31 = 1F_h$				
Each LSB represents 0.1µW. This register is to be used in conjunction with TXLOWh to yield a sixteen-bit value. The values in TXLOWh:TXLOWl are in an unsigned binary format. The value in this register is uncalibrated. The value in TXLOWh is compared against TXOPh. Warning bit Wx is set if TXOPh < TXLOWh. Since TXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

RX Optical Power High Warning Threshold MSB (RXHIGHh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0mW)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			36 = 24_h				
Each LSB represents 25.6µW. This register is to be used in conjunction with RXHIGHl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in RXHIGHh is compared against RXOPh. Warning bit Wx is set if RXOPh > RXHIGHh.							

RX Optical Power High Warning Threshold LSB (RXHIGHl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0mW)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			37 = 25_h				
Each LSB represents 0.1µW. This register is to be used in conjunction with RXHIGHh to yield a sixteen-bit value. The values in RXHIGHh:RXHIGHl are in an unsigned binary format. The value in this register is uncalibrated. The value in RXHIGHh is compared against RXOPh. Warning bit Wx is set if RXOPh > RXHIGHh. Since RXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

RX Optical Power Low Warning Threshold MSB (RXLOWh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0mW)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			38 = 26_h				
Each LSB represents 25.6µW. This register is to be used in conjunction with RXLOWl to yield a sixteen-bit value. The value in this register is uncalibrated. The value in RXLOWh is compared against RXOPh. Warning bit Wx is set if RXOPh < RXLOWh.							

RX Optical Power Low Warning Threshold LSB (RXLOWl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 0000_b = 00_h (0mW)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			39 = 27_h				
Each LSB represents 0.1µW. This register is to be used in conjunction with RXLOWh to yield a sixteen-bit value. The values in RXLOWh:RXLOWl are in an unsigned binary format. The value in this register is uncalibrated. The value in RXLOWh is compared against RXOPh. Warning bit Wx is set if RXOPh < RXLOWh. Since RXOPl is always zero, it is recommended that this register always be programmed to zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Checksum (CHKSUM) **Checksum of bytes 0 - 94 at serial address A2h**							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$ (0°C)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$95 = 5F_h$				
This register is provided for compliance with SFF-8472. It is implemented as general-purpose non-volatile memory. Read/write access is possible whenever a valid OEM password has been entered. CHKSUM is read-only in USER mode.							

ADC Result Registers

Temperature Result MSB (TEMPh)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			$0000\ 0000_b = 00_h$ (0°C)(1)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$96 = 60_h$				
Each LSB represents one degree centigrade. This register is to be used in conjunction with TEMPl to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section.							

Temperature Result LSB (TEMPl)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			$0000\ 0000_b = 00_h$ (0°C)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$97 = 61_h$				
This register is to be used in conjunction with TEMPh to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section. In the MIC3001 this register will always return zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Voltage MSB (VINh)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			$0000\ 0000_b = 00_h$ (0V)(2)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$98 = 62_h$				
Each LSB represents 25.6mV. This register is to be used in conjunction with VINl to yield a sixteen-bit value. The values in VINh:VINl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section.							

Voltage LSB (VINl)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			$0000\ 0000_b = 00_h$ (0V)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$99 = 63_h$				
Each LSB represents 100μV. This register is to be used in conjunction with VINh to yield a sixteen-bit value. The values in VINh:VINl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section. In the MIC3001, this register will always return zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Notes:

1. TEMPh will contain measured temperature data after the completion of one conversion.
2. VINh will contain measured data after one A/D conversion cycle.

Laser Diode Bias Current MSB (ILDh)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			0000 0000_b = 00_h (0mA)(3)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			100 = 64_h				
This register is to be used in conjunction with ILDl to yield a sixteen-bit value. The values in ILDh:ILDl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration sections.							

Laser Diode Bias Current LSB (ILDl)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			0000 0000_b = 00_h (0mA)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			101 = 65_h				
Each LSB represents 2μA. This register is to be used in conjunction with ILDh to yield a sixteen-bit value. The values in ILDh:ILDl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section. In the MIC3001, this register will always return zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Transmitted Optical Power MSB (TXOPh)(4)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			0000 0000_b = 00_h (0mW)(5)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			102 = 66_h				
Each LSB represents 25.6μW. This register is to be used in conjunction with TXOPl to yield a sixteen-bit value. The values in TXOPh:TXOPl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section.							

Transmitted Optical Power LSB (TXOPl)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			0000 0000_b = 00_h (0mW)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			103 = 67_h				
Each LSB represents 0.1μW. This register is to be used in conjunction with TXOPh to yield a sixteen-bit value. The values in TXOPh:TXOPl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section. In the MIC3001, this register will always return zero. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bitsection.							

Notes:

3. ILDh will contain measured data after one A/D conversion cycle.
4. The scale factor corresponding to the sense resistor used must be set in the configuration register.
5. TXOPh will contain measured data after one A/D conversion cycle.

Received Optical Power MSB (RXOPh)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			$0000\ 0000_b = 00_h$ (0mW)(6)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$104 = 68_h$				
Each LSB represents 25.6μW. This register is to be used in conjunction with RXOPl to yield a sixteen-bit value. The values in RXOPh:RXOPl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section.							

Received Optical Power LSB (RXOPl)							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			$0000\ 0000_b = 00_h$ (0mW)(6)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$105 = 69_h$				
Each LSB represents 0.1μW. This register is to be used in conjunction with RXOPh to yield a sixteen-bit value. The values in RXOPh:RXOPl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the coefficients provided. See the External Calibration section. This register is provided for compliance with SFF-8472. It is not used by the MIC3001 when doing threshold comparisons and setting alarm or warning bits.							

Control and Status (CNTRL)							
D[7] TXDIS read-only	D[6] STXDIS read/write	D[5] reserved	D[4] RSEL read/write	D[3] SRSEL read/write	D[2] XFLT read-only	D[1] LOS read-only	D[0] POR read-only
Default Value				$0000\ 0000_b = 00_h$			
Serial Address				$A2_h = 1010001_b$			
Byte Address				$110 = 6E_h$			

Bit(s)		Function	Operation
D[7]	TXDIS	Reflects the state of the TXDISABLE pin	1 = disabled, 0 = enabled, read only.
D[6]	STXDIS	Soft transmit disable	1 = disabled; 0 = enabled.
D[5]	D[5]	Reserved	Reserved - always write as zero.
D[4]	RSEL	Reflects the state of the RSEL pin	1 = high; 0 = low.
D[3]	SREL	Soft rate select	1 = high (2Gbps); 0 = low (1Gbps).
D[2]	TXFLT	Reflects the state of the TXFAULT pin	1 = high (fault); 0 = low (no fault).
D[1]	LOS	Loss of signal. Reflects the state of the LOS pin	1 = high (loss of signal); 0 = low (no loss of signal).
D[0]	POR	MIC3001 power-on status	0 = POR complete, analog data ready; 1 = POR in progress.

Notes:

6. RXOPh will contain measured data after one A/D conversion cycle.

Alarm Flags

Alarm Register 0 (ALARM0)							
D[7] A7 read-only	D[6] A6 read-only	D[5] A5 read-only	D[4] A4 read-only	D[3] A3 read-only	D[2] A2 read-only	D[1] A1 read-only	D[0] A1 read-only
Default Value			0000 0000_b = 00_h (no events pending)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			112 = 70_h				
The power-up default value is 00_h. Following the first A/D conversion, however, any of the bits may be set depending on the results.							

Bit(s)		Function	Operation
D[7]	A7	High temperature alarm, TEMPh > TMAXh.	1 = condition exists, 0 = normal/OK.
D[6]	A6	Low temperature alarm, TEMPh < TMINh.	1 = condition exists, 0 = normal/OK.
D[5]	A5	High voltage alarm, VINh > VMAXh.	1 = condition exists, 0 = normal/OK.
D[4]	A4	Low voltage alarm, VINh < VMINh.	1 = condition exists, 0 = normal/OK.
D[3]	A3	High laser diode bias alarm, IBIASh > IMAXh.	1 = condition exists, 0 = normal/OK.
D[2]	A2	Low laser diode bias alarm, IBIASh < IMINh.	1 = condition exists, 0 = normal/OK.
D[1]	A1	High transmit optical power alarm, TXOPh > TXMAXh.	1 = condition exists, 0 = normal/OK.
D[0]	A0	Low transmit optical power alarm, TXOPh < TXMINh.	1 = condition exists, 0 = normal/OK.

Alarm Register 1 (ALARM1)							
D[7] A15 read-only	D[6] A14 read-only	D[5] reserved	D[4] reserved	D[3] reserved	D[2] reserved	D[1] reserved	D[0] reserved
Default Value			0000 0000_b = 00_h (no events pending)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			113 = 71_h				
The power-up default value is 00_h. Following the first A/D conversion, however, any of the bits may be set depending on the results.							

Bit(s)		Function	Operation
D[7]	A15	High received power (overload) alarm, RXOPh > RXMAXh.	1 = condition exists, 0 = normal/OK.
D[6]	A14	Low received power (LOS) alarm, RXOPh < RXMINh.	1 = condition exists, 0 = normal/OK.
D[5:0]		Reserved	Reserved - always write as zero.

Warning Flags

Warning Register 0 (WARN0)							
D[7] W7 read-only	D[6] W6 read-only	D[5] W5 read-only	D[4] W4 read-only	D[3] W3 read-only	D[2] W2 read-only	D[1] W1 read-only	D[0] W1 read-only
Default Value			0000 0000_b = 00_h (no events pending)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			116 = 74_h				
The power-up default value is 00_h. Following the first A/D conversion, however, any of the bits may be set depending on the results.							

Bit(s)		Function	Operation
D[7]	W7	High temperature warning, TEMPh > THIGHh.	1 = condition exists, 0 = normal/OK.
D[6]	W6	Low temperature warning, TEMPh < TLOWh.	1 = condition exists, 0 = normal/OK.
D[5]	W5	High voltage warning, VINh > VHIGHh.	1 = condition exists, 0 = normal/OK.
D[4]	W4	Low voltage warning, VINh < VLOWh.	1 = condition exists, 0 = normal/OK.
D[3]	W3	High laser diode bias warning, IBIASh > IHIGHh.	1 = condition exists, 0 = normal/OK.
D[2]	W2	Low laser diode bias warning, IBIASh < ILOWh.	1 = condition exists, 0 = normal/OK.
D[1]	W1	High transmit optical power warning, TXOPh > TXHIGHh.	1 = condition exists, 0 = normal/OK.
D[0]	W0	Low transmit optical power warning, TXOPh < TXLOWh.	1 = condition exists, 0 = normal/OK.

Warning Register 1 (WARN1)							
D[7] W15 read-only	D[6] W14 read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Default Value			0000 0000_b = 00_h (no events pending)				
Serial Address			$A2_h$ = 1010001_b				
Byte Address			117 = 75_h				
The power-up default value is 00_h. Following the first A/D conversion, however, any of the bits may be set depending on the results.							

Bit(s)		Function	Operation
D[7]	W15	Received power high warning, RXOPh > RXHIGHh.	1 = condition exists, 0 = normal/OK.
D[6]	W14	Received power low warning, RXOPh < RXMINh.	1 = condition exists, 0 = normal/OK.
D[5:0]		Reserved	Reserved - always write as zero.

OEM Password Entry (OEMPW)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$ (reset to zero at power-on)				
Serial Address			$A2_h = 1010001_b$				
Byte Address			120 – 123 = 78_h - $7B_h$ (MSB is $7B_h$)				
This four-byte field is for entry of the password required to access the OEM area of the MIC3001's memory and registers. A valid OEM password will also permit access to the user areas of memory. The byte at address 123 ($7B_h$) is the most significant byte. This field is compared to the four-byte OEMPWSET field at serial address A6h, bytes 12 to 15. If the two fields match, access is allowed to the OEM areas of the MIC3001 non-volatile memory at serial addresses $A4_h$ and $A6_h$. The OEM password is set by writing the new value into OEMPWSET. The password comparison is performed following the write to the MSB, address $7B_h$. This byte must be written last! A four-byte burst-write sequence to address 78_h may be used as this will result in the MSB being written last. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect. This field is reset to all zeros at power on. Any values written to these locations will be readable by the host regardless of the locked/unlocked status of the device. If OEMPWSET is set to zero (00000000_h), the MIC3001 will remain unlocked regardless of the contents of the OEMPW field. This is the factory default security setting.								

Byte	**Weight**
3	OEM Password Entry, Most Significant Byte (Address = 7Bh)
2	OEM Password Entry, 2nd Most Significant Byte (Address = 7Ah)
1	OEM Password Entry, 2nd Least Significant Byte (Address = 79h)
0	OEM Password Entry, Least Significant Byte (Address = 78h)

USER Password Setting (USRPWSET)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$				
Serial Address			$A2_h = 1010001_b$				
Byte Address			250 = FA_h				
This register is for setting the password required to access the USER area of the MIC3001's memory and registers. This field is compared to the USRPW field at serial address $A2_h$, byte 251. If the two fields match, access is allowed to the USER areas of the MIC3001 non-volatile memory at serial addresses A0h and A2h. If a valid USER password has not been entered, writes to the serial ID fields, USRCTRL, and the user scratchpad areas of $A0_h$ and $A2_h$ will not be allowed, and USRPWSET will be unreadable (returns all zeroes). A USER password is set by writing the new value into USRPWSET. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect. This register is non-volatile and will be maintained through power and reset cycles. A valid USER or OEM password is required for access to this register. Otherwise, this register will read as 00_h. Note: a valid OEM password overrides the USER password setting. If a valid OEM password is currently in place, the user password will have no effect.								

USER Password (USRPW)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$251 = FB_h$				
USER passwords are entered in this field. This field is compared to the USRPWSET field at serial address A2h, byte 250. If the two fields match, access is allowed to the USER areas of the MIC3001 non-volatile memory at serial addresses A0h and A2h. If a valid USER password has not been entered, writes to the serial ID fields and user scratchpad areas of A0h and A2h will not be allowed and USRPWSET will be unreadable (returns all zeroes).							

Power-On Hours MSB (POHh)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$252 = FC_h$				
The lower seven bits of this register contain the most-significant bits of the 15-bit power-on hours measurement. POHFLT is an error flag. The value in this register should be combined with the Power-on Hours, Low Byte, POHl, to yield the complete result. If POHFLT is set, the power-on hour meter data has been corrupted and should be ignored. It is recommended that a two-byte (or more) sequential read operation be performed on POHh and POHl to insure coherency between the two registers. This register is non-volatile and will be maintained through power and reset cycle.							

Bit(s)	Function	Operation
D[7]	Power-on hours fault flag	1 = fault; 0 = no fault.
D[6:0]	Power-on hours, high byte	Non-volatile.

Power-On Hours LSB (POHl)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
POH Fault Flag (POHFLT)							
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$253 = FD_h$				
This register contains the least-significant eight bits of the 15-bit power-on hours measurement. The value in this register should be combined with the Power-on Hours, High Byte, POHh, to yield the complete result. If POHFLT is set, the power-on hour meter data has been corrupted and should be ignored. It is recommended that a two-byte (or more) sequential read operation be performed on POHh and POHl to insure coherency between the two registers. This register is non-volatile and will be maintained through power and reset cycles.							

Data Ready Flags (DATARDY)							
D[7] TRDY read/write	D[6] VRDY read/write	D[5] IRDY read/write	D[4] TXRDY read/write	D[3] RXDY read/write	D[2] reserved	D[1] reserved	D[0] reserved
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$254 = FE_h$				
When the A/D conversion for a given parameter is completed and the results available to the host, the corresponding data ready flag will be set. The flag will be cleared when the host reads the corresponding result register.							

Bit(s)		Function	Operation
D[7]	TRDY	Temperature data ready flag	0 = old data; 1 = new data ready
D[6]	VRDY	Voltage data ready flag	0 = old data; 1 = new data ready
D[5]	IRDY	Bias current data ready flag	0 = old data; 1 = new data ready
D[4]	TXRDY	Transmit power data ready flag	0 = old data; 1 = new data ready
D[3]	RXRDY	Receive power data ready flag	0 = old data; 1 = new data ready
D[2:0]		Reserved	Reserved

USER Control Register (USRCTL)							
D[7] read/write	D[6] PORM read/write	D[5] PORS read/write	D[4] IE read/write	D[3] APCSEL read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0010\ 0000_b = 20_h$				
Serial Address			$A2_h = 1010001_b$				
Byte Address			$255 = FF_h$				
This register provides for control of the nominal APC setpoint and management of interrupts by the end-user. APCSEL[1:0] select which of the APC setpoint registers, APCSET0, APCSET1, or APCSET2 are used as the nominal automatic power control setpoint. IE must be set for any interrupts to occur. If PORM is set, the power-on event will generate an interrupt and warm resets using RST will not generate a POR interrupt. When a power-on interrupt occurs, assuming PORM=1, PORS will be set. PORS will be cleared and the interrupt output de-asserted when USRCTL is read by the host. If IE is set while /INT is asserted, /INT will be de-asserted. The host must still clear the various status flags by reading them. If PORM is set following the setting of PORS, PORS will remain set, and /INT will not be de-asserted, until USRCTL is read by the host. PORM, IE, and APCSEL are non-volatile and will be maintained through power and reset cycles. A valid USER password is required for access to this register.							

Bit		Function	Operation
D[7]		Reserved	Always write as zero; reads undefined.
D[6]	PORM	Power-on interrupt mask	1 = POR interrupts enabled; 0 = disabled; read/write; non-volatile.
D[5]	PORS	Power-on interrupt flag	1 = POR interrupt occurred; 0 = no POR interrupt; read-only.
D[4]	IE	Global interrupt enable	1 = enabled; 0 = disabled; read/write; non-volatile.
D[3]	APCSEL	Selects APC setpoint register	00 = APCSET0, 01 = APCSET1, 10 = APCSET2; 11 = reserved; read/write; non-volatile.
D[2:0]		Reserved	Reserved

OEM Configuration Register 0 (OEMCFG0)							
D[7] RST write only	D[6] ZONE read/write	D[5] DFLT read only	D[4] OE reserved	D[3] MODREF reserved	D[2] VAUX[2] read/write	D[1] VAUX[1] read/write	D[0] VAUX[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$00 = 00_h$				
A write to OEMCFG0 will result in any A/D conversion in progress being aborted and the result discarded. The A/D will begin a new conversion sequence once the write operation is complete. All bits in OEMCFG0 are non-volatile except DFLT and RST. A valid OEM password is required for access to this register.							

Bit(s)		Function	Operation
D[7]	RST		0 = no action; 1 = reset; write-only.
D[6]	ZONE	Selects temperature zone.	0 = internal; 1 = external; non-volatile.
D[5]	DFLT	Diode fault flag.	1 = diode fault; 0 = OK.
D[4]	OE	Output enable for SHDN, V_{MOD}, and V_{BIAS}.	1 = enabled; 0 = hi-Z; non-volatile.
D[3]	MODREF	Selects whether V_{MOD} is referenced to ground or V_{DD}.	1 = V_{DD}; 0 = GND; non-volatile.
D[2:0]	VAUX[2:0]	Selects the voltage reported in VINh:VINl.	000 = V_{IN}; 001 = V_{DDA}; 010 = V_{BIAS}; 011 = V_{MOD}; 100 = APCDAC; 101 = MODDAC; 110 = FLTDAC; non-volatile

OEM Configuration Register 1 (OEMCFG1)							
D[7] INV read/write	D[6] GAIN read/write	D[5] BIASREF read/write	D[4] RFB[2] read/write	D[3] RFB[1] read/write	D[2] RFB[0] read/write	D[1] SRCE read/write	D[0] SPOL read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$1 = 01_h$				
A write to OEMCFG1 will result in any A/D conversion in progress being aborted and the result discarded. The A/D will begin a new conversion sequence once the write operation is complete. All bits in OEMCFG1 are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register.							

Bit(s)		Function	Operation
D[7]	INV	Inverts the APC op-amp inputs. When set to “0” the BIAS DAC output is connected to the “+”input and FB is connected to the “–” input of the op amp. Set to “0” to use the ADC feedback loop.	0 = emitter follower (no inversion); 1 = common emitter (inverted); read/write; non-volatile.
D[6]	GAIN	Sets the feedback voltage range by changing the APCDAC output swing; 0-V_{REF} for optical feedback, 0-V_{REF}/4 for electrical feedback.	1 = V_{REF}/4 full scale; 0 = V_{REF} full scale; read/write; non-volatile.
D[5]	BIASREF	Selects whether FB and VMPD are referenced to ground or V_{DD} and selects feedback resistor termination voltage (V_{DDA} or GNDA).	1 = V_{DD}; 0 = GND; read/write; non-volatile.
D[4:2]	RFB[2:0]	Selects internal feedback resistance. (Resistors will be terminated to V_{DDA} or GNDA according to BIASREF.)	000 = ∞; 001 = 800Ω, 010 = 1.6kΩ, 011 = 3.2kΩ, 100 = 6.4kΩ, 101 = 12.8kΩ, 110 = 25.6kΩ, 111 = 51.2kΩ; read/write; non-volatile.
D[1]	SRCE	V_{BIAS} source vs. sink drive.	1 = source (NPN), 0 = sink (PNP); read/write; non-volatile.
D[0]	SPOL	Polarity of shutdown output, SHDN, when active.	1 = high; 0 = low; read/write; non-volatile.

OEM Configuration Register 2 (OEMCFG2)							
D[7] I2CADR[3] read/write	D[6] I2CADR[2] read/write	D[5] I2CADR[1] read/write	D[4] I2CADR[0] read/write	D[3] LUTOFF read/write	D[2] LUTOFF read/write	D[1] LUTOFF read/write	D[0] LUTOFF read/write
Default Value			1010 $xxxx_b$ = xx_h (slave address = $1010xxx_b$)				
Serial Address			$A6_h$ = 1010011_b				
Byte Address			$2 = 02_h$				
CAUTION: Changes to I2CADR take effect immediately! Any accesses following a write to I2CADR must be to the newly programmed serial bus address. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles.							

Bit(s)		Function	Operation
D[7:4]	I2CADR[3:0]	Upper four MSBs of the serial bus slave address; writes take effect immediately.	Read/write; non-volatile.
D[3:0]	LUTOFF	LUT offset. LUTOFF is added to the result of the digital temperature sensor to derive the table index; writes take effect after reset.	Read/write; non-volatile.

APC Setpoint 0 (APCSET0) Automatic power control setpoint (unsigned binary) used when APCSEL[1:0] = 00							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$3 = 03_h$				
When A.P.C. is on, i.e., the APCCAL bit in OEMCAL0 is set, the value in APCSETx is added to the signed value taken from the A.P.C. look-up table and loaded into the VBIAS DAC. When A.P.C. is off, the value in APCSET is loaded directly into the VBIAS DAC, bypassing the look-up table entirely. In either case, the VBIAS DAC setting is reported in the VBIAS register. The APCCFG bits determine the DAC's response to higher or lower numeric values. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles.							

APC Setpoint 1 (APCSET1) Automatic power control setpoint (unsigned binary) used when APCSEL[1:0] = 01							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$4 = 04_h$				
When A.P.C. is on, i.e., the APCCAL bit in OEMCAL0 is set, the value in APCSETx is added to the signed value taken from the A.P.C. look-up table and loaded into the VBIAS DAC. When A.P.C. is off, the value in APCSET is loaded directly into the VBIAS DAC, bypassing the look-up table entirely. In either case, the VBIAS DAC setting is reported in the VBIAS register. The APCCFG bits determine the DAC's response to higher or lower numeric values. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles.							

APC Setpoint 2 (APCSET2) Automatic power control setpoint (unsigned binary) used when APCSEL[1:0] = 10							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$5 = 05_h$				
When A.P.C. is on, i.e., the APCCAL bit in OEMCAL0 is set, the value in APCSETx is added to the signed value taken from the A.P.C. look-up table and loaded into the VBIAS DAC. When A.P.C. is off, the value in APCSET is loaded directly into the VBIAS DAC, bypassing the look-up table entirely. In either case, the VBIAS DAC setting is reported in the VBIAS register. The APCCFG bits determine the DAC's response to higher or lower numeric values. This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register.							

Modulation DAC Setting (MODSET) Nominal V_{MOD} setpoint							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$6 = 06_h$				
When A.P.C. is on, the value corresponding to the current temperature is taken from the MODLUT look-up table, added to MODSET and loaded into the V_{MOD} DAC. This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register.							

I_{BIAS} Fault Threshold (IBFLT) Bias current fault threshold							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$7 = 07_h$				
A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. A fault is generated if the bias current is higher than IBFLT value set in this register.							

Transmit Power Fault Threshold (TXFLT)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$8 = 08_h$				
A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. A fault is generated if the Transmit power is higher than TXFLT value set in this register.							

Loss-Of-Signal Threshold (LOSFLT)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$9 = 09_h$				
A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. A fault is generated if the received power is lower than LOSFLT value set in this register.							

Byte	**Function**	**Operation**
D[7:4]	Receive loss-of-signal threshold	Read/write; non-volatile.

Fault Suppression Timer (FLTTMR) Fault suppression interval in increments of 0.5ms							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$10 = 0A_h$				
Saturation faults are suppressed for a time, t_{FLTTMR}, following laser turn-on. This avoids nuisance tripping while the APC loop starts up. The length of this interval is (FLTTMR∞0.5ms), typical. A value of zero will result in no fault suppression. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles.							

Fault Mask (FLTMSK)							
D[7] OEMIM read/write	D[6] POHE read/write	D[5] reserved	D[4] reserved	D[3] SATMSK read/write	D[2] TXMSK read/write	D[1] IAMSK read/write	D[0] DFMSK read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$11 = 0B_h$				
A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles.							

Bit		Function	Operation
D[7]	OEMIM	OEM interrupt mask bit	1 = masked; 0 = enabled; Read/write; non-volatile.
D[6]	POHE	OEM Power-on Hour Meter enable bit	1 = enabled; 0 = disabled; Read/write; non-volatile.
D[5:4]	D[5:4]	Reserved	Always write as zero; reads undefined.
D[3]	SATMSK	APC saturation fault mask bit	1 = masked; 0 = enabled; Read/write; non-volatile.
D[2]	TXMSK	High TX optical power fault mask bit	1 = masked; 0 = enabled; Read/write; non-volatile.
D[1]	IAMSK	Bias current high alarm mask bit	1 = masked; 0 = enabled; Read/write; non-volatile.
D[0]	DFMSK	Diode fault mask bit	1 = masked; 0 = enabled; Read/write; non-volatile.

OEM Password Setting (OEMPWSET)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			12 - 15 = $0F_h$ - $0F_h$; $0C_h$ = MSB				
This four-byte field is the password required for access to the OEM area of the MIC3001's memory and registers. The byte at address 250 (FA_h) is the most significant byte. This field is compared to the four-byte OEMPW field at serial address $A2_h$, byte 120 to 123. If the two fields match, access is allowed to the OEM areas of the MIC3001 non-volatile memory at serial addresses $A4_h$ and $A6_h$. The OEM password may be set by writing the new value into OEMPWSET. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect. These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register.							

Byte	Weight
3	OEM Password, Most Significant Byte
2	OEM Password, 2nd Most Significant Byte
1	OEM Password, 2nd Least Significant Byte
0	OEM Password, Least Significant Byte

OEM Calibration 0 (OEMCAL0)							
D[7] reserved	D[6] FLTDIS read/write	D[5] FSPIN read/write	D[4] WRINH read/write	D[3] APCCAL read/write	D[2] FRCINT read/write	D[1] FRCTXF read/write	D[0] FRCLOS read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$16 = 10_h$				
A valid OEM password is required for access to this register.							

Bit		Function	Operation
D[7]		Reserved	Always write as zero; reads undefined.
D[6]	FLTDIS	Fault comparator disable; inhibits output of fault comparators when set.	0 = faults enabled; 1 = disabled; Read/write.
D[5]	FSPIN	Fault comparator “spin-on-channel” mode select; do not enable ADC and FC spin-on-channel modes simultaneously.	0 = normal operation; 1 = spin on channel; Read/write.
D[4]	WRINH	Inhibit NVRAM write cycles.	0 = normal operation; 1 = inhibit writes; Read/write.
D[3]	APCCAL	Selects APC calibration mode - DACs may be controlled directly.	0 = normal mode; 1 = calibration mode; Read/write.
D[2]	FRCINT	Forces the assertion of /INT	0 = normal operation; 1 = asserted; Read/write.
D[1]	FRCTXF	Forces the assertion of TXFAULT	0 = normal operation; 1 = asserted; Read/write.
D[0]	FDCLOS	Forces the assertion of RXLOS	0 = normal operation; 1 = asserted; Read/write.

OEM Calibration 1 (OEMCAL1)							
D[7] reserved	D[6] ADSTP read/write	D[5] ADIDL read/write	D[4] 1SHOT read/write	D[3] ADSPIN read/write	D[2] SPIN[2] read/write	D[1] SPIN[1] read/write	D[0] SPIN[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$17 = 11_h$				
A valid OEM password is required for access to this register.							

Bit		Function	Operation
D[7]		Reserved	Always write as zero; reads undefined.
D[6]	ADSTP	Stop ADC Halts the analog to digital converter	0 = normal operation; 1 = stopped; Read/write.
D[5]	ADIDL	ADC idle flag	0 = busy; 1 = idle; Read/write.
D[4]	1SHOT	Triggers one-shot A/D conversion cycle	0 = normal operation; 1 = one-shot; Read/write.
D[3]	ADSPIN	Selects ADC spin-on-channel mode; do not enable ADC and FC spin-on-channel modes simultaneously	0 = normal operation; 1 = spin-on-channel; Read/write.
D[2], D[1], D[0]	SPIN[2:0]	ADC and fault comparator (FC) channel select for spin-on-channel mode; do not enable ADC and FC spin-on-channel modes simultaneously	ADC: 000 = temperature; 001 = voltage; 010 = VILD; 011 = VMPD; 100 = VRX; FC: 001 = VILD; 001 = VMPD; 010 = VRX; Read/write.

OEM Calibration 1 (OEMCAL1)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			18 = 12h				
The look-up table index is derived from the current temperature measurement and LUTOFF as follows: $INDEX = \left(\frac{T_{AVG}(\mu)}{2}\right) + LUTOFF$ where T_{AVG}(n) is the current average temperature. This register allows the current table index to be read by the host. The table base address must be added to LUTINDX to form a complete table index in physical memory. A valid OEM password is required for access to this register. Otherwise, reads are undefined.							

OEM Configuration 3 (OEMCFG3)							
D[7] LUTSEL read/write	D[6] TXFPOL read/write	D[5] GPOD read/write	D[4] GPOM read/write	D[3] GPOC read/write	D[2] TXFIN read/write	D[1] LOSDIS read/write	D[0] INTCAL read/write
Default Value			$0000\ 1000_b = 08_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$19 = 13_h$				
This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register. GPOD and GPOC are ignored when GPOM = 0. TXFPOL is ignored if TXFIN = 0.							

Bit		Function	Operation
D[7]	LUTSEL	RX power look-up table input selection bit	1 = RX power; 0 = temperature; read/write; ignored if INTCAL = 0.
D[6]	TXFPOL	TXFIN active polarity select; a fault is indicated when TXFIN = TXFPOL	0 = active-low; 1 = active-high; read/write; ignored if TXFIN = 0.
D[5]	GPOD	GPO output drive	0 = open drain; 1 = push-pull; read/write; ignored if GPOM = 0.
D[4]	GPOM	GPO/RSOUT mode select	0 = RSOUT; 1 = GPO; read/write.
D[3]	GPOC	GPO output control	0 = low; 1 = high; read/write; ignored if GPOM = 0.
D[2]	TXFIN	TXFIN mode select	0 = SHDN; 1 = TXFIN; read/write.
D[1]	LOSDIS	RXLOS comparator disable	0 = enabled; 1 = disabled; read/write.
D[0]	INTCAL	Calibration mode select	0 = external calibration; 1 = internal calibration; read/write.

BIAS DAC Setting (APCDAC) Current VBIAS Setting							
D[7] read only	D[6] read only	D[5] read only	D[4] read only	D[3] read only	D[2] read only	D[1] read only	D[0] read only
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$20 = 14_h$				
This register reflects (reads back) the value set in the APC register (APCSET0, APCSET1, or APCSET2 whichever is selected). A valid OEM password is required for access to this register.							

Modulation DAC Setting (MODDAC) Current VMOD Setting							
D[7] read only	D[6] read only	D[5] read only	D[4] read only	D[3] read only	D[2] read only	D[1] read only	D[0] read only
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$21 = 15_h$				
This register reflects (reads back) the value set in the MODSET register. A valid OEM password is required for access to this register.							

OEM Readback Register (OEMRD)							
D[7] reserved	D[6] reserved	D[5] reserved	D[4] INT read only	D[3] APCSAT read only	D[2] IBFLT read only	D[1] TXFLT read only	D[0] RSOUT read only
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$22 = 16_h$				
This register reflects (reads back) the status of the bits corresponding to the parameters defined below. A valid OEM password is required for access to this register. Otherwise, reads are undefined and writes are ignored.							

Bit		Function	Operation
D[7:5]		Reserved	Always write as zero; reads undefined.
D[4]	INT	Mirrors state of /INT but active-high; not state of physical pin!	1 = interrupt; 0 = no interrupt.
D[3]	APCSAT	APC saturation fault comparator output state	1 = fault; 0 = normal operation.
D[2]	IBFLT	State of IBIAS over-current fault comparator output	1 = fault; 0 = normal operation; read-only.
D[1]	TXFLT	State of transmit power fault comparator output	1 = fault; 0 = normal operation; read-only.
D[0]	RSOUT	State of the rate select output pin, RSOUT	1 = high; 0 = low; Read-only.

Signal Detect Threshold (LOSFLTn)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$23 = 17_h$				
This register works in conjunction with the LOSFLT register to control the operation of the loss of signal comparator. The comparator's output, RXLOS, is asserted when the input on VRX falls below the level in LOSFLT. The output will then be de-asserted when the VRX signal rises above LOSFLTn. The input signal is subject to scaling by the RXPOT. If the LOS comparator is disabled, i.e., LOSDIS = 1, this register is ignored. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles.							

RX EEPOT Tap Selection (RXPOT)							
D[7] reserved	D[6] reserved	D[5] reserved	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$24 = 18_h$				
This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers.							

Bit(s)	Function	Operation
D[7:5]	Reserved	Reserved. Always write as zero; reads undefined.
D[4:0]	RXPOT tap selection: 00000 = No divider action; POT disconnected 00001 = 31/32 00010 = 30/32 • • • 11110 = 2/32 11111 = 1/32	Read/write; non-volatile.

OEM Configuration 4 (OEMCFG4)							
D[7] reserved	D[6] reserved	D[5] reserved	D[4] reserved	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$25 = 19_h$				
This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers.							

Bit(s)	Function	Operation
D[7:5]	Reserved	Reserved. Always write as zero; reads undefined.
I_{START}[3:0]	I_{START} current level selection: 0000 = No I_{START} current 0001 - 1111 = 0.375mA x I_{START}[3:0] I_{START} is used to speed up the laser start-up after a fault accures. The charging current of the compensation cap starts from I_{START} instead of ramping up from 0.	Read/write; non-volatile.

Power-On Hour Meter Data (POHDATA)							
D[7] read/write	D[6] read/write	D[5] read/write	D[4] read/write	D[3] read/write	D[2] read/write	D[1] read/write	D[0] read/write
Default Value			0000 $0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			32-39 = 20_h - 27_h				
These registers are used for backing up the POH result during power cycles. At power-up, the POH meter selects the larger of the two values as the initial count. Incremental results are stored in alternate register pairs. The power-on hour meter may be reset or preset by writing to these registers. These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers.							

Byte	Weight
3	POHA, high-byte
2	POHA, low-byte
1	POHB, high-byte
0	POHB, low-byte

OEM Scratchpad Registers (SCRATCHn)	
Default Value	0000 $0000_b = 00_h$
Serial Address	$A6_h = 1010011_b$
Byte Address	SCRATCH0: 126 = $7E_h$ SCRATCH1: 127 = $7F_h$ SCRATCH2: 128 = 80_h ..... SCRATCH127: 253 = FD_h
The scratchpad registers are general-purpose non-volatile memory locations. They can be freely read from and written to any time the MIC3001 is in OEM mode.	

RX Power Look-up Table (RXLUTn)	
Default Value	$0000\ 0000_b = 00_h$
Serial Address	$A6_h = 1010011_b$
Byte Address	$40\text{-}71 = 28_h - 47_h$
These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers.	

Bytes	Definition
RXSLP0h	RX Slope 0, High Byte.
RXSLP0l	RX Slope 0, Low Byte.
RXOFF0h	RX Offset 0, High Byte.
RXOFF0l	RX Offset 0, Low Byte.
RXSLP1h	RX Slope 1, High Byte.
RXSLP1l	RX Slope 1, Low Byte.
RXOFF1h	RX Offset 1, High Byte.
RXOFF1l	RX Offset 1, Low Byte.
•	•
•	•
•	•
RXSLP7h	RX Slope 7, High Byte.
RXSLP7l	RX Slope 7, Low Byte.
RXOFF7h	RX Offset 7, High Byte.
RXOFF7l	RX Offset 7, Low Byte.

Calibration Constants (CALn)	
Default Value	$0000\ 0000_b = 00_h$
Serial Address	$A6_h = 1010011_b$
Byte Address	74 - 87 = 4A h - 57h
These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers.	

Bytes	Definition
TOFFh	Temperature Offset, High Byte.
TOFF0l	Temperature Offset, Low Byte. Always Reads Zero; Writes Ignored.
VSLP0h	Voltage Slope, High Byte.
VSLP0l	Voltage Slope, Low Byte.
VOFFh	Voltage Offset, High Byte.
VOFF0l	Voltage Offset, Low Byte.
ISLP0h	Bias Current Slope, High Byte.
ISLP0l	Bias Current Slope, Low Byte.
IOFFh	Bias Current Offset, High Byte.
IOFF0l	Bias Current Offset, Low Byte.
TXSLPh	TX Power Slope, High Byte.
TXSLPl	TX Power Slope, Low Byte.
TXOFFh	TX Power Offset, High Byte.
TXOFFl	TX Power Offset, Low Byte.

Manufacturer ID Register (MFG_ID) Identifies Micrel as the manufacturer of the device. Always returns 2Ah							
D[7] read only	D[6] read only	D[5] read only	D[4] read only	D[3] read only	D[2] read only	D[1] read only	D[0] read only
Default Value			$0000\ 0000_b = 00_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$32\text{-}39 = 20_h - 27_h$				
These registers are used for backing up the POH result during power cycles. At power-up, the POH meter selects the larger of the two values as the initial count. Incremental results are stored in alternate register pairs. The power-on hour meter may be reset or preset by writing to these registers. These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers.							

Bit(s)	Function	Operation
D[7:0]	Identifies Micrel as the manufacturer of the device. Always returns $2A_h$.	Read only. Always returns A_h

Device ID Register (DEV_ID)							
D[7] read only	D[6] read only	D[5] read only	D[4] read only	D[3] read only	D[2] read only	D[1] read only	D[0] read only
MIC3001 DEVICE ID always reads 0 at D[5-7] and 1 at D[4]				DIE REVISION			
Default Value			$0001\ xxxx_b = 1x_h$				
Serial Address			$A6_h = 1010011_b$				
Byte Address			$255 = FF_h$				
The value in this register, in combination with the MFG_ID register, serve to identify the MIC3001 and its revision number to software. This register is read-only.							

Applications Information

Controlling Laser Diode Bias

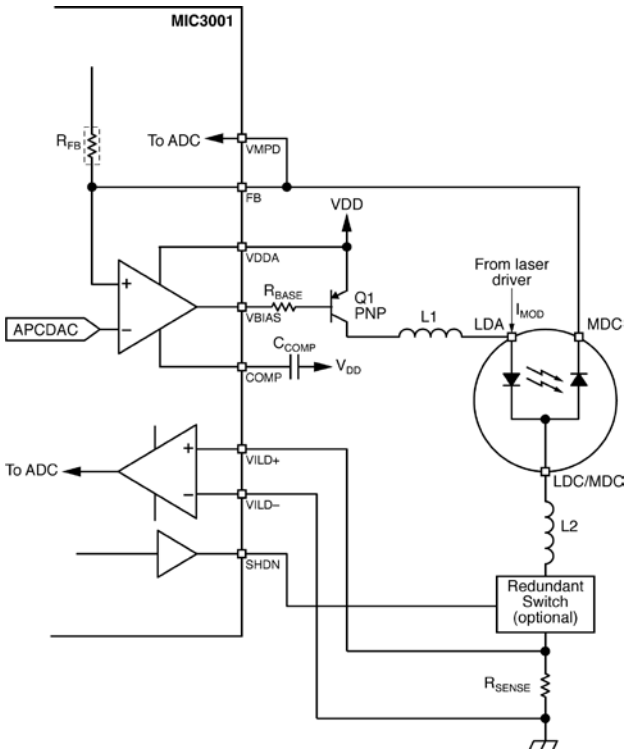


Figure 26. Example APC Circuit for Common-Cathode TOSA

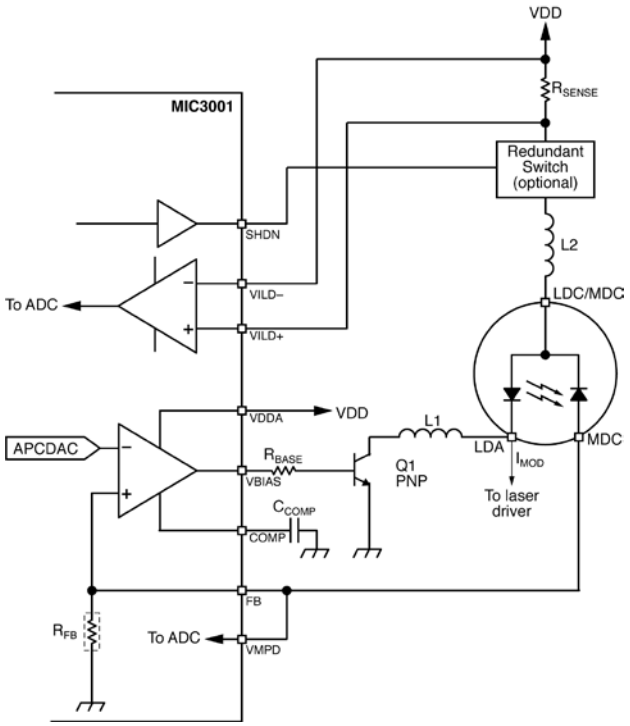


Figure 27. Example APC Circuit for Common Anode TOSA

hbwhelp@micrel.com or (408) 955-1690

Choosing C_{COMP}

The APC loop is compensated by a capacitor, C_{COMP}, connected from COMP to either V_{DDA} or GNDA. This capacitor adjusts the slew rate and bandwidth of the loop as follows:

$$SlewRate = dV / dt = \frac{I_{SLEW}}{C_{COMP}}$$

$$BW = \frac{G_M}{2\pi C_{COMP}}$$

where:

I_{SLEW} = 64µA,
G_M = 125µMho

these relationships are shown graphically in Figure 28 and Figure 29.

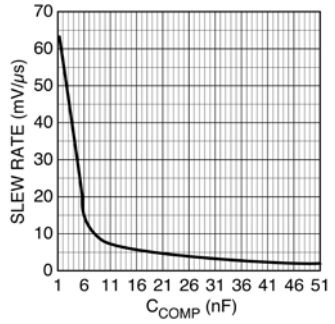


Figure 28. Slew Rate vs. C_{COMP} Value

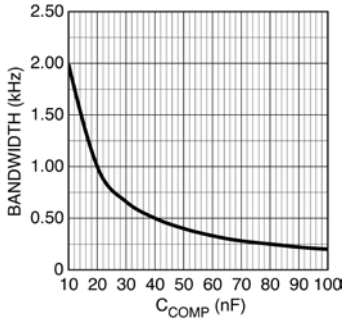


Figure 29. Open Loop Unity-Gain Bandwidth vs. C_{COMP}

The loop response should be tailored to the data rate, encoding format and maximum run-lengths, and required laser turn-on time. Higher data rates and/or shorter maximum run lengths and/or faster turn-on times call for smaller capacitors. Lower data rates and/or longer maximum run lengths and/or slower turn-on times call for larger capacitors. In order to meet the SFP/GBIC turn-on requirement of 1ms, for example, do not employ a capacitor larger than 20nF. Low ESR capacitors such as ceramics will give the best results. Excessive ESR will reduce the effectiveness of C_{COMP}. The capacitor's voltage rating must exceed V_{DDA}. Some typical values are shown in Table 22.

Application	C_{COMP} (nF)
8b/10b encoding, ≥1Gbps, t_{ON} ≤ 1ms	10
SONET ($62_b/64_b$ encoding), ≥1Gbps	22
≥155Mbps, t_{ON} ≤ 1ms	22
≥155Mbps	100

Table 22. Typical Values for C_{COMP}

While there is no theoretical upper limit on the size of C_{COMP}, it is desirable for the loop to be able to track the changes resulting from periodic temperature compensation. The typical temperature compensation update period is 1.6s. Therefore, a maximum size of 1mF is recommended. If laser turn-on time is not a factor, a value between 100nF and 1mF can be used for virtually any typical application. The tradeoff is that higher value capacitors have a larger physical size and cost.

In order to maximize the power supply rejection ratio (PSRR), C_{COMP} should be returned to GNDA when the V_{BIAS} output is sourcing current, e.g., driving an NPN transistor (SRCE bit = 1). C_{COMP} should be returned to V_{DDA} when the V_{BIAS} output is sinking current, e.g., driving a PNP transistor (SRCE bit =0).

Measuring Laser Bias Current

VILD+ and VILD– form a pair of pseudo-differential A/D inputs for measuring laser diode bias current via a sense resistor. The signal applied to these inputs is converted to a single-ended, ground-referenced signal for input into the ADC and bias current fault comparator. These inputs have limited common-mode voltage range. The full-scale differential input range is $V_{REF}/4$ or about 300mV.

Figure 26 and Figure 27 illustrate the typical implementation of this function. Note that VILD– is always connected to the circuit's reference potential: V_{DD} in the case of a common-anode transmitter optical sub-assembly (TOSA) and GND in the case of a common-cathode TOSA. Note that the monitor photodiode current will also flow in the sense resistor. This will result in a small offset in the measured bias current. The APC function will hold this term constant, so it can be corrected for in the external calibration constants. The sensing resistor could also be connected between V_{DD} and the emitter of Q1 on figure 26 or between the emitter of Q1 and GND on Figure 27.

Interfacing To Laser Drivers

In order for the MIC3001 to control the modulation current of the laser diode, an interface circuit may be required depending on the method used by the driver to set its modulation current level. Generally, most laser diode driver ICs use one of three methods:

a) A current, I_{SET}, is sourced into a pin on the driver IC. The modulation current delivered by the driver is then some fixed multiple of I_{SET}. The SY88912 is an example of this type of driver. A simple circuit

can be used to create a current source controlled by the V_{MOD} outputs. The circuit is based on an external bipolar transistor and a current sensing resistor.

b) A current, I_{SET}, is drawn out of a pin on the driver IC. The modulation current delivered by the driver is then some fixed multiple of I_{SET}. A simple circuit can be used to create a current source controlled by the V_{MOD} outputs. The circuit is based on an external bipolar transistor and a current sensing resistor.

c) A voltage, V_{SET}, is applied to a pin on the driver IC. This voltage may be referenced to GND or V_{DD}. The MIC3001's V_{MOD+} output can supply this voltage directly. If a voltage swing wider than V_{REF} is needed, gain can be applied with a pair of external resistors. The SY88932, SY88982, and SY89307 are examples of this type of driver.

SY88912 3.3V 3.2Gbps SONET/SDH Laser Driver

The modulation level of the SY88912 driver is controlled by the current sourced into the RSET pin (Type (a) above). The circuit shown in Figure 30.allows the MIC3001's V_{MOD} outputs to control the SY88912's modulation current from its minimum value, 5mA, to its maximum value, 60mA. The circuit operates as a DAC-controlled current source. The current source is formed by the V_{MOD} buffer amplifier, external transistor, and current sense resistor. The op-amp acts to force the voltage drop across RSET to be equal to the DAC output voltage.

The current, I_{SET}, through RSET is therefore regulated as

$I_{SET} = V_{MOD+}/R_{SET}$ (In this case, the DAC output and therefore the op-amp output, are referenced to V_{DDA}.) The SY88912's current gain, I_{MOD}/I_{SET}, is 23. A modulation current level of 60mA requires I_{SET} = 60mA/23 = 2.61mA; a modulation current level of 5mA requires I_{SET} = 5mA/23 = 0.217mA. R_{FLTR} and C_{FLTR} are optional and act to eliminate any noise that might be present on V_{DDA} or V_{MOD}. The values shown give a 100ms time constant. Note that the time constant is present whenever the laser is turned on or turned off. This must be taken into account when designing to system specifications such as the SFP MSA's t_{ON} and t_{OFF} requirements. The values of R_{FLTR} and/or C_{FLTR} may need to be adjusted accordingly. The impact of the filter time constant on the turn off time can be eliminated by using the MIC3001's SHDN signal to drive the SY88912's enable input, /EN.

The use of the SHDN signal is completely optional. The main benefit to using SHDN, however, is that it shuts down the driver very quickly and irrespective of the values of R_{FLTR} and C_{FLTR}. The values of R_{FLTR} and C_{FLTR} can therefore be increased, enhancing their effect without incurring any turn-off time penalty. Depending on the polarity chosen for SHDN using the SPOL bit, an inversion may be required between the MIC3001's SHDN output and the driver's /EN input. (The SHDN output may also be used to drive a redundant safety switch and the same polarity may not be appropriate for both functions.)

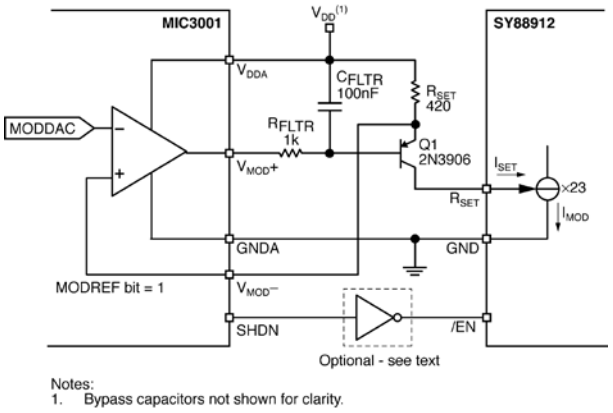


Figure 30. Controlling the SY88912

Modulation Current

For the circuit of Figure 30, the modulation current control range and corresponding DAC values are shown in Table 23 below.

DAC	V_{DDA}-V_{MOC}	I_{SET}	I_{MOD}
0	0V	0mA	0mA
19	0.091V	0.216mA	4.98mA
127	0.61V	1.45mA	33.4mA
255	1.22V	2.91mA	66.8mA

Table 23. Control Range of SY88912 Modulation Control Circuit

SY88932 3.3V 3.2Gbps SONET/SDH Laser Driver

The modulation level of the SY88932 driver is controlled by the voltage applied to the VCTRL pin (Type (c) above). The circuit shown in Figure 31 allows the MIC3001's V_{MOD} output to control the SY88932's modulation current. The circuit operates as a DAC-controlled voltage source. VCTRL is simply the DAC output voltage. See section above on SY88912 for R_{FLTR}, C_{FLTR} and SHDN.

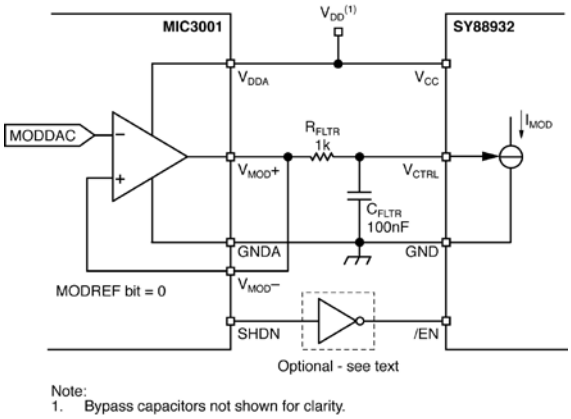
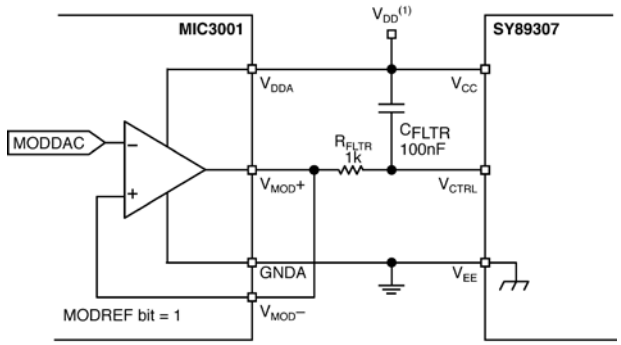


Figure 31. Controlling the SY88932 Modulation Current

SY89307 5.0V/ 3.3V 2.5Gbps VCSEL Driver

The modulation level of the SY89307 driver is controlled by the voltage applied to the VCTRL pin (Type (c) above). The circuit shown in Figure 32 allows the MIC3001's V_{MOD} output to control the SY89307's output swing. VCTRL is simply the DAC output voltage. The circuit operates as a DAC-controlled voltage source. See section above on SY88912 for R_{FLTR}, C_{FLTR}.



Note:
1. Bypass capacitors not shown for clarity.

Figure 32. Controlling the SY89307 Modulation Current

Laser Drivers Programmed via a Sink Current

The modulation level of some laser diode drivers is controlled by a current sourced out of the RSET pin (Type (b) above). The circuit shown in Figure 33 allows the MIC3001's V_{MOD} outputs to control the set current, ISET. The circuit operates as a DAC-controlled current sink. The current sink is formed by the V_{MOD} buffer amplifier, external transistor, and current sense resistor. The op-amp acts to force the voltage drop across RSET to be equal to the DAC output voltage.

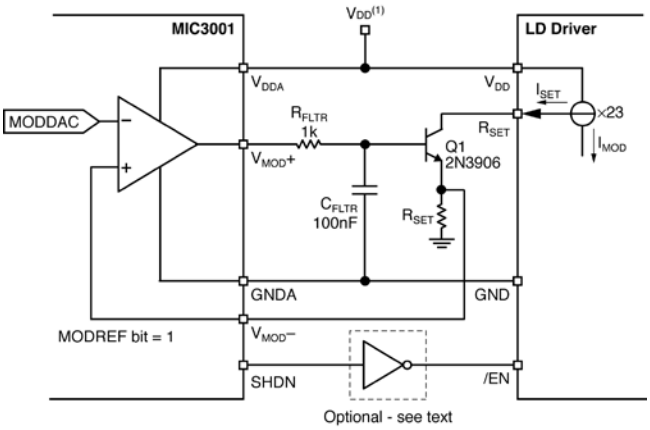
The current through R_{SET} is therefore regulated as

$I_{RSET} = V_{MOD}+/R_{SET}$. I_{SET} is given by the equation:

$$I_{SET} = \left(\frac{VMOD+}{R_{SET}}\right)\left(\frac{\beta}{1+\beta}\right) \qquad (13)$$

where b is the DC gain of Q1

The higher the gain of the transistor, the closer I_{SET} will be to the current in R_{SET}. R_{FLTR} and C_{FLTR} act to eliminate any noise that might be present on V_{DDA} or V_{MOD}. The values shown give a 100ms time constant. See section above on SY88912 for R_{FLTR}, C_{FLTR} and SHDN.



Notes:
1. Bypass capacitors not shown for clarity

Figure 33. Controlling the Modulation Current via a Sink Current

Drivers with Monitor Outputs

Laser diode driver ICs have been introduced with monitor outputs. These outputs provide ground-referred signals that mirror critical signals like laser bias current, modulation current or monitor photodiode current, an analog of transmitted power. Generally, these outputs source a current into an external resistor to generate a ground-referenced voltage. Using these outputs with the MIC3001 is straightforward since the MIC3001's VILD+/– and VMPD inputs are polarity programmable,

Shutdown Output

The shutdown output, SHDN, can be used in two ways: as an enable or on/off control for the laser driver IC, and/or to control a redundant switch in the laser current path. The redundant switch provides a means for the MIC3001 to shut off the laser current even if the bias transistor or modulator is damaged or fails. SHDN is active any time the MIC3001 shuts down the laser, i.e., if the TXDISABLE function is asserted in hardware or software, or if the fault detection circuits trigger laser shutdown. The shutdown output, SHDN, is essentially a logic output with programmable polarity. The programmable polarity allows SHDN to drive either high-side or low-side switches or active-high or active-low enable inputs without the need for external inversion circuits. If an active-low and an active-high shutdown signal are required, an external inverter will be necessary. Examples of redundant switch circuits are shown in Figure 34.

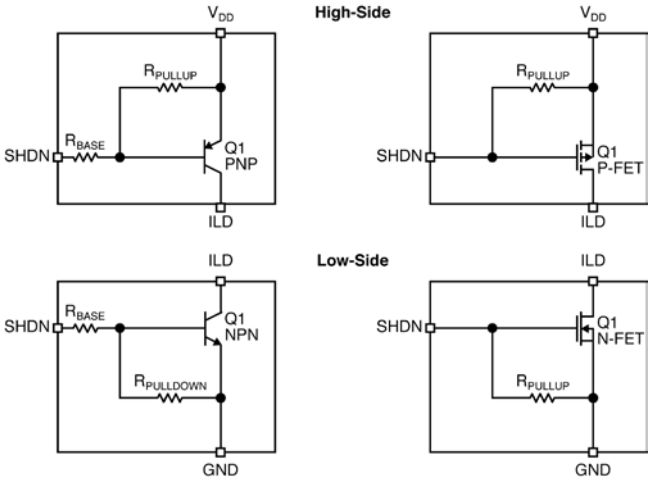


Figure 34. Redundant Switch Circuits

Temperature Sensing

The MIC3001 can measure and report its own internal temperature or the temperature of a remote PN junction or "thermal diode". In either case it is important to note that any board-mounted semiconductor device tends to track the ground plane temperature around it. The dominant thermal path to the sensor is often the ground pin. The ground pin usually connects to the lead-frame paddle on which the die is mounted. Typical semiconductor packages, being non-conductive plastic, insulate the device from the ambient air.

The advantage to using a remote sensor is that the temperature may be sensed at a specific location, such as in the proximity of the laser diode, or away from any heat sources where it will more closely track the transceiver's case temperature. The measured temperature is reported via the digital diagnostics registers and is used to index the temperature compensation tables. (Note: SFF-8472 does not specify the meaning of the reported temperature information or the location from which it is taken. This information is to be specified in the transceiver vendor's datasheet.)

Remote Sensing

For remote temperature sensing using the XPN pin, most small-signal PNP transistors with characteristics similar to the JEDEC 2N3906 will perform well as thermal diodes. Table 24 lists several examples of such parts that Micrel has tested for use with the MIC3001. Other transistors equivalent to these should also work well.

Vendor	Part Number	Package
Fairchild Semiconductor	MMBT3906	SOT-23
On Semiconductor	MMBT3906L	SOT-23
Infineon Technologies	SMBT3906/MMBT3906	SOT-23
Samsung Semiconductor	KST3906-TF	SOT-23

Table 24. Transistors Suitable for Use as Remote Diodes

Minimizing Errors

Self-Heating

One concern when measuring temperature is to avoid errors induced by self-heating. Self-heating is caused by power dissipation within the MIC3001. It is directly proportional to the internal power dissipation and the junction-to-ambient thermal resistance, θ_{JA}. The dissipation in the MIC3001 must be calculated and reduced to a temperature offset. The power dissipation, PDISS, includes the effect of quiescent current and all currents flowing into or out of any signal pins, especially V_{BIAS} and V_{MOD}. The temperature rise caused by self-heating is given by:

$$\Delta t = P_{DISS} \times \theta_{JA} \quad (14)$$

θ_{JA} is given in the "Operating Ratings" section above as 43°C/W. The possible contributors to self-heating are listed in Table 25.

The numbers given in Table 25 suggest that the power dissipation in a typical application will be no more than a few tens of milliwatts, leading to self-heating on the order of 1°C.

Description	Magnitude	Notes
Quiescent Power	I_{DD} x V_{DD}	Typically V_{DD} = 3.3V, I_{DD} = 2.7mA → 3.3V x 2.7mA = 8.91mW.
SHDN Current	I_{OL} x V_{OL}	Negligible if MOSFET is used as shutdown device.
TXFAULT Current	I_{OL} x V_{OL}	Worst case is V_{DD}^2/R_{PULLUP}; R_{PULLUP} is 4.7kΩ min. per SFP MSA → $3.3V^2/4.7k\Omega$ = 2.32mW.
V_{BIAS} Current	V_{BIAS} x I_{VBIAS} or (V_{DD}–V_{BIAS}) x I_{VBIAS}	Worst-case is V_{REF} x 10mA = 1.22V x 10mA = 12.3mW.
V_{MOD} Current	V_{MOD} x I_{VMOD} or (V_{DD}–V_{MOD}) x I_{VMOD}	Worst-case is V_{REF} x 10mA = 1.22V x 10mA = 12.3mW.
RSOUT Current	I_{OL} x V_{OL}	Only for rate-agile applications using RSIN/RSOUT.
DATA Current	I_{OL} x V_{OL} x duty_cycle	May be negligible; Depends on bus speed, pull-up current, and bus activity.
RXLOS Current	I_{OL} x V_{OL}	Worst case is V_{DD}^2/R_{PULLUP}; R_{PULLUP} is 4.7kΩ min. per SFP MSA → $3.3V^2/4.7k\Omega$ = 2.32mW.

Table 25. Contributors to Self-Heating

In any application, the best and often easiest approach is to measure performance in the final application environment. This is especially true when dealing with systems for which some temperature data may be poorly defined or unobtainable except by empirical means. If desired, the external calibration constants may be used to correct the temperature readings.

Series Resistance with External Temperature Sensor

The operation of the MIC3001 depends upon sensing the VCB-E of a diode-connected PNP transistor ("diode") at two different current levels. For remote temperature measurements, this is done using an external diode connected between XPN and ground. Since this technique relies upon measuring the relatively small voltage difference resulting from two levels of current through the external diode, any resistance in series with the external diode will cause an error in the temperature reading from the MIC3001. A good rule of thumb is this: for each ohm in series with the external transistor, there will be a 0.9°C error in the MIC3001's temperature measurement. It is not difficult to keep the series resistance well below an ohm (typically <0.1), so this will rarely be an issue.

XPN Filter Capacitor Selection

It is desirable to employ a filter capacitor between XPN and GNDA. The use of this capacitor is especially recommended in environments with a lot of high frequency noise (such as digital switching noise), or if long wires are used to connect to the remote diode. The maximum recommended total capacitance from the XPN pin to GND is 2000pF. The recommended typical capacitor is a 1000pF NP0 or C0G ceramic capacitor with a 10% tolerance. If the remote diode is to be at a distance of more than 6" to 12" from the MIC3001, using twisted pair wiring or shielded microphone cable for the connections to the diode can significantly reduce noise pickup. If using a long run of shielded cable, remember to subtract the cable's conductor-to-shield capacitance from the 2000pF maximum total capacitance.

XPN Layout Considerations

The following guidelines should be kept in mind when designing and laying out circuits using the MIC3001 and a remote thermal diode:

1. Place the MIC3001 as close to the remote diode as possible, while taking care to avoid severe noise sources such as high speed data busses, and the like.
2. Since any conductance from the various voltages on the PC board and the XPN line can induce errors, it is good practice to guard the remote diode's emitter trace with a pair of ground traces. These ground traces should be returned to the MIC3001's own ground pin. They should not be grounded at any other part of their run. However, it is highly desirable to use these guard traces to carry the diode's own ground return back to the ground pin of the MIC3001, thereby providing a Kelvin connection for the base of the diode.
3. When using the MIC3001 to sense the temperature of a processor or other device which has an integral thermal diode, connect the emitter and base of the remote sensor to the MIC3001 using the guard traces and Kelvin return shown in Figure 35. The collector of the remote diode is typically inaccessible to the user on these devices.
4. Due to the small currents involved in the

measurement of the remote diode's DVBE, it is important to adequately clean the PC board after soldering to prevent current leakage. This is most likely to show up as an issue in situations where water-soluble soldering fluxes are used.

5. In general, wider traces for the ground and T1 lines will help reduce susceptibility to radiated noise (wider traces are less inductive). Use trace widths and spacing of 10 mils wherever possible and provide a ground plane under the MIC3001 and under the connections from the MIC3001 to the remote diode. This will help guard against stray noise pickup.

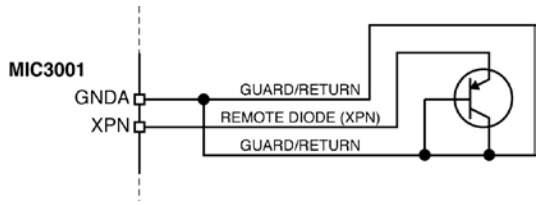


Figure 35. Guard Traces and Kelvin Return for Remote Thermal Diode

Layout Considerations

Small Form-Factor Pluggable (SFP) Transceivers

The pinout of the MIC3001 digital control and status signals was optimized for use in small form-factor pluggable (SFP MSP) optical transceivers. If the MIC3001 is mounted on the bottom of the PC board with the correct rotation, the control and status I/O can be routed to the host connector without changing the order. This is shown in Figure 36.

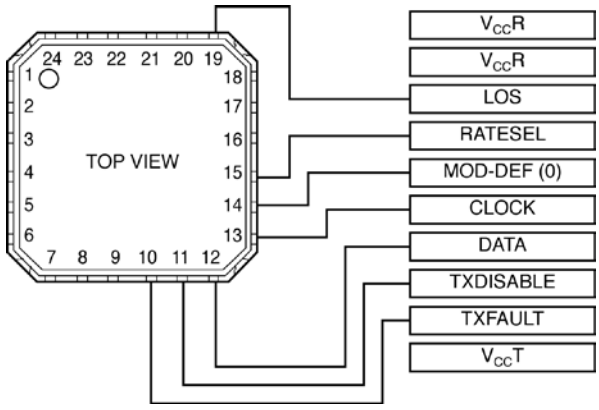


Figure 36. Typical SFP Control and Status I/O Signal Routing (not to scale)

Power Supplies

The MIC3001 has separate power supply and ground pins for both the analog and digital supplies. This helps prevent digital switching noise from corrupting the analog functions. The individual supply and ground pins are not isolated from one another inside the IC. Separate analog and digital power and ground planes are NOT required on the PCB. Having one of each plane (power and ground) is certainly good practice, however. If dedicated power and ground layers are not available, care should be taken to route the digital supply and return currents back to the supply separate from the analog supply connections. A schematic of this approach is shown in Figure 37. Each supply should be bypassed as close to the IC as possible with 0.01µF capacitor (Low ESR capacitors such as ceramics are preferred.) as shown. This assumes that bulk capacitance is already present upstream. If no other filter capacitance is present nearby, a 1µF filter capacitor should be added in parallel to the 0.01µF capacitor.

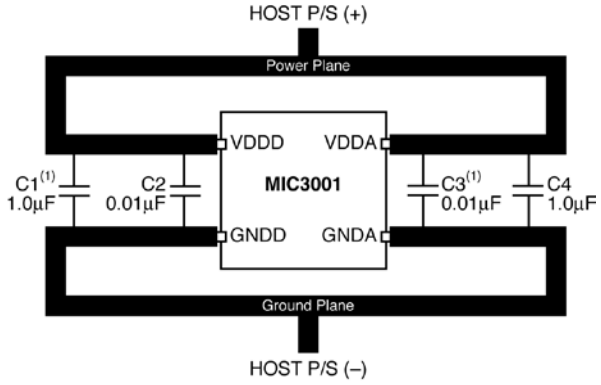


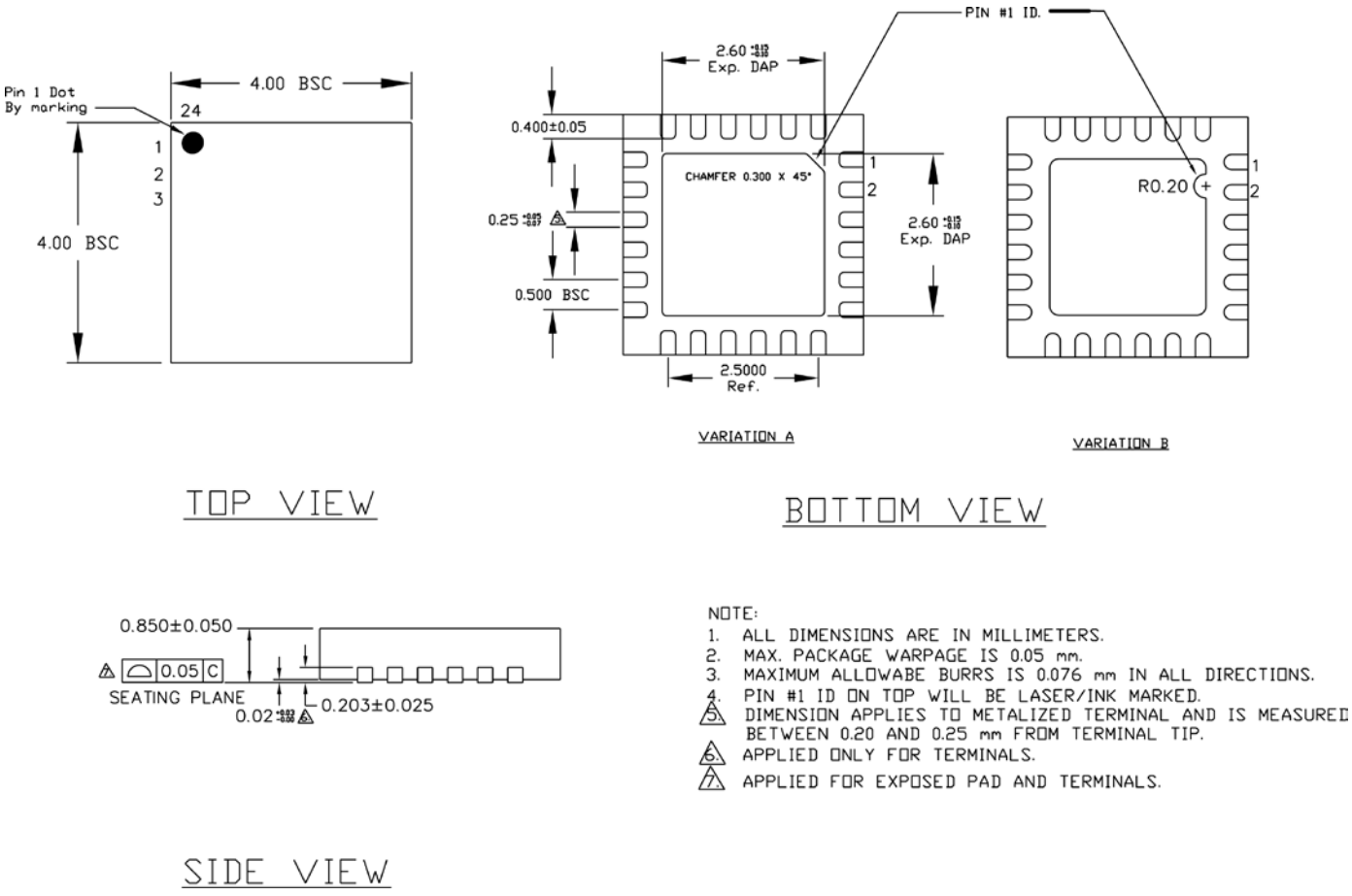
Figure 37. Power Supply Routing and Bypassing

Using the MIC3001 In a 5V System

It is fairly straightforward to use the MIC3001 in a system powered from a 5V rail. In these systems, the laser diode driver IC will usually be powered from the 5V rail. A small linear regulator, such as Micrel's MIC5213, can be used to generate a 3.3V power supply rail if one does not otherwise exist in the system. All of the MIC3001's digital I/O's except for RSOUT are 5V tolerant and may be pulled up to 5.5V regardless of the MIC3001's supply voltage. They can be connected directly to a 5V host. The MIC5213 is ideal, as it is capable of supplying up to 80mA, is in a tiny SC-70 package, and is stable with small ceramic output capacitors.

The laser diode driver interface will be unchanged in most cases. Ground referred voltages and currents can be generated the same way as with 3.3V-powerd drivers. The exception is drivers that are controlled by a voltage referenced to V_{DD} such as the SY89307. The MIC3001's V_{BIAS} or V_{MOD} output will be referenced to its own 3.3V power supply whereas the driver's input will be referenced to its 5V power supply. The solution is a simple level-shifting circuit that converts the V_{BIAS}/V_{MOD} output into a current and then into a V_{DD}-referenced voltage.

Package Information



24-Pin QFN

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