



MIC2285A

8MHz PWM Synchronous Buck Regulator with LDO Standby Mode

General Description

The Micrel MIC2285A is a high efficiency 8MHz PWM synchronous buck (step-down) regulator that features a LOWQ® LDO standby mode that draws only 20µA of quiescent current. The MIC2285A allows an ultra-low noise, small size, and high efficiency solution for portable power applications.

In PWM mode, the MIC2285A operates with a constant frequency 8MHz PWM control. Under light load conditions, such as in system sleep or standby modes, the PWM switching operation can be disabled to reduce switching losses. In this light load LOWQ® mode, the LDO maintains the output voltage and draws only 18µA of quiescent current. The LDO mode of operation saves battery life while not introducing spurious noise and high ripple as experienced with pulse skipping or bursting mode regulators.

The MIC2285A operates from 2.7V to 5.5V input and features internal power MOSFETs that can supply up to 600mA output current in PWM mode. It can operate with a maximum duty cycle of 100% for use in low-dropout conditions.

The MIC2285A is available in the 10-pin 2mm x 2mm Thin MLF® package with a junction operating range from -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

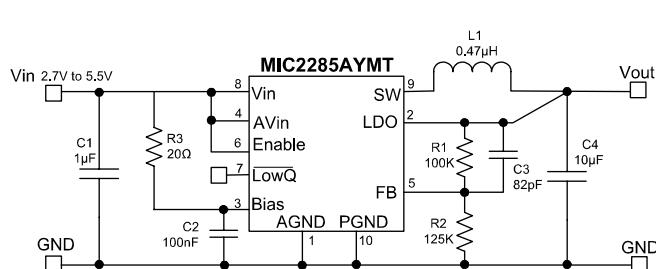
Features

- 2.7 to 5.5V supply/input voltage
- Light load LOWQ® LDO mode
 - 20µA quiescent current
 - Low noise, 75µVrms
- 8MHz PWM mode
 - Output current to 600mA
 - >90% efficiency
 - 100% maximum duty cycle
- Adjustable output voltage option down to 1V
 - Fixed output voltage options available
- Ultra-fast transient response
- Requires only a 0.47µH inductor
- **Enables sub 0.55mm profile solution**
- Fully integrated MOSFET switches
- Micropower shutdown
- Thermal shutdown and current limit protection
- 10-pin 2mm x 2mm x 0.55mm MLF® package
- -40°C to +125°C junction temperature range

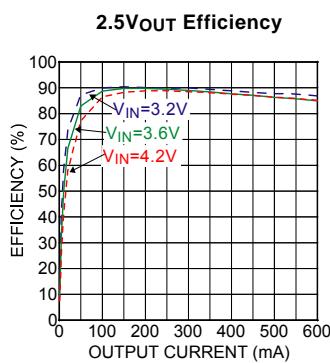
Applications

- Cellular phones
- PDAs
- USB peripherals

Typical Application



Adjustable Output Buck Regulator with LOWQ® Mode



LOWQ is a registered trademark of Micrel, Inc.
MLF and MicroLeadFrame are registered trademarks of Amkor Technology, Inc.

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Ordering Information

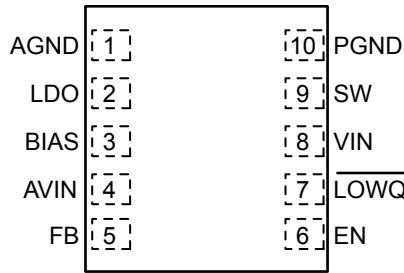
| Part Number | Marking | Output Voltage* | Junction Temperature Range | Package | Lead Finish |
|-------------|---------|-----------------|----------------------------|----------------------|-------------|
| MIC2285AYMT | WPA | Adj. | -40° to +125°C | 10-Pin 2x2 Thin MLF® | Pb-free |

Note

* For other voltage options available, please contact Micrel Marketing for details.

MLF® is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



10-Pin 2mm x 2mm Thin MLF® (MT)

Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|----------|---|
| 1 | AGND | Analog (signal) Ground. |
| 2 | LDO | LDO Output (Output): Connect to V_{OUT} for LDO mode operation. |
| 3 | BIAS | Internal circuit bias supply. Must be decoupled to signal ground with a $0.1\mu F$ capacitor and should not be loaded. |
| 4 | AVIN | Analog Supply Voltage (Input): Supply voltage for the analog control circuitry and LDO input power. Requires bypass capacitor to GND. |
| 5 | FB | Feedback. Input to the error amplifier. For the Adjustable option, connect to the external resistor divider network to set the output voltage. For fixed output voltage options, connect to V_{OUT} and an internal resistor network sets the output voltage. |
| 6 | EN | Enable (Input). Logic low will shut down the device, reducing the quiescent current to less than $5\mu A$. |
| 7 | LOWQ | Enable LDO Mode (Input): Logic low enables the internal LDO and disables the PWM operation. Logic high enables the PWM mode and disables the LDO mode. |
| 8 | VIN | Supply Voltage (Input): Supply voltage for the internal switches and drivers. |
| 9 | SW | Switch (Output): Internal power MOSFET output switches. |
| 10 | PGND | Power Ground. |

Absolute Maximum Ratings⁽¹⁾

| | |
|--|-------------------|
| Supply Voltage (V_{IN}) | +6V |
| Output Switch Voltage (V_{SW}) | +6V |
| Output Switch Current (I_{SW}) | 2A |
| Logic Input Voltage (V_{EN}, V_{LOWQ}) | -0.3V to V_{IN} |
| Storage Temperature (T_s) | -60°C to +150°C |
| ESD Rating ⁽³⁾ | 3kV |

Operating Ratings⁽²⁾

| | |
|--|-------------------|
| Supply Voltage (V_{IN}) | +2.7V to +5.5V |
| Logic Input Voltage (V_{EN}, V_{LOWQ}) | -0.3V to V_{IN} |
| Junction Temperature (T_J) | -40°C to +125°C |
| Junction Thermal Resistance 2x2 MLF-10L (θ_{JA}) | 60°C/W |

Electrical Characteristics⁽⁴⁾

$V_{IN} = V_{EN} = V_{LOWQ} = 3.6V$; $L = 0.47\mu H$; $C_{OUT} = 10\mu F$; $T_A = 25^\circ C$, unless noted. **Bold** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$

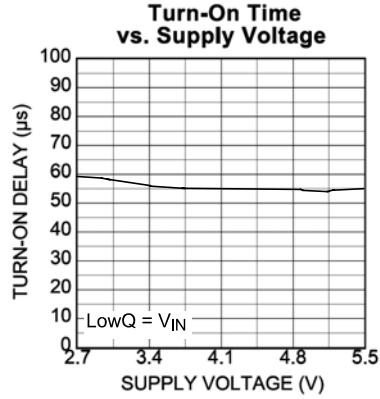
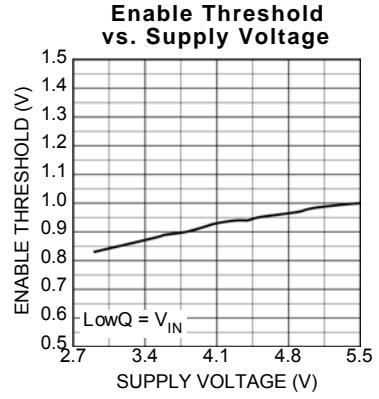
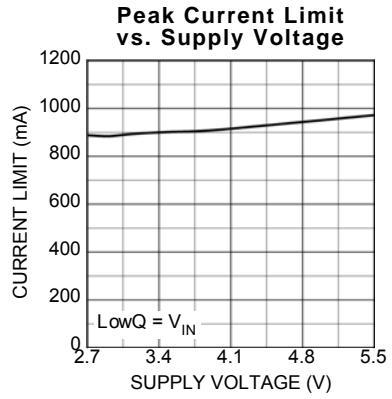
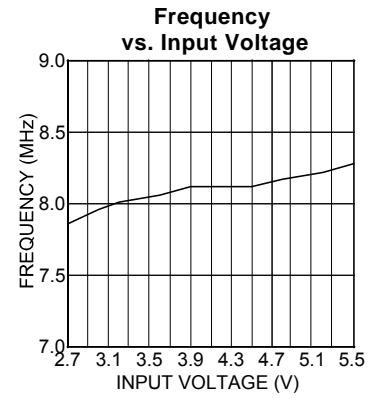
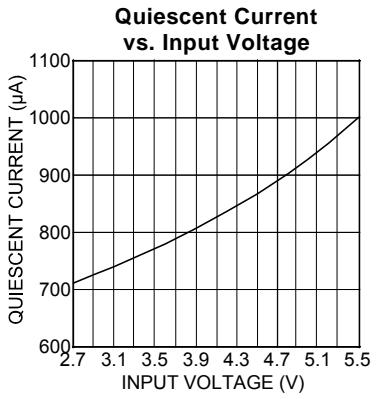
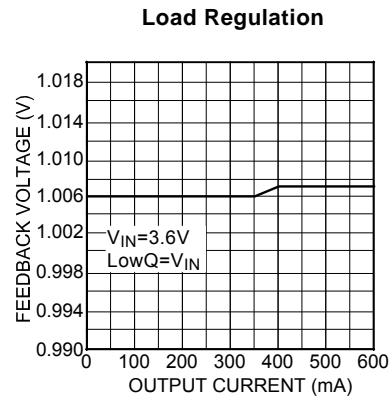
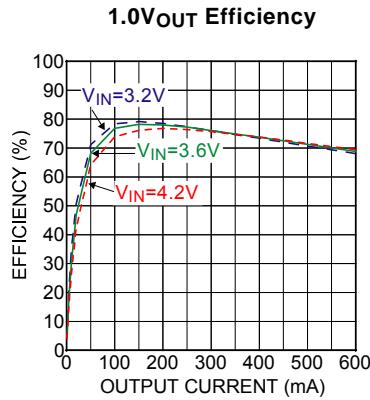
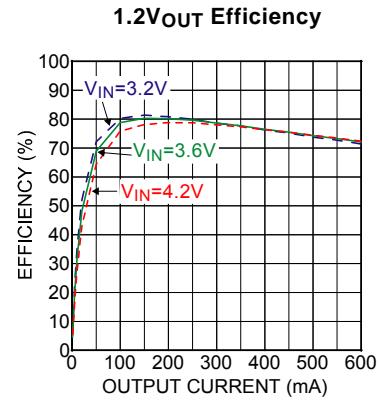
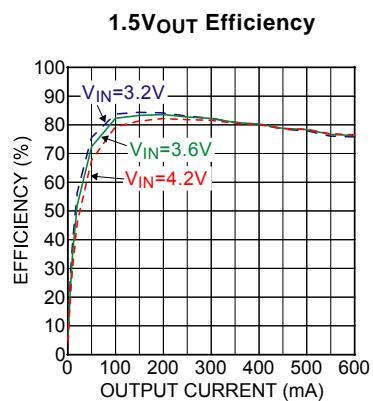
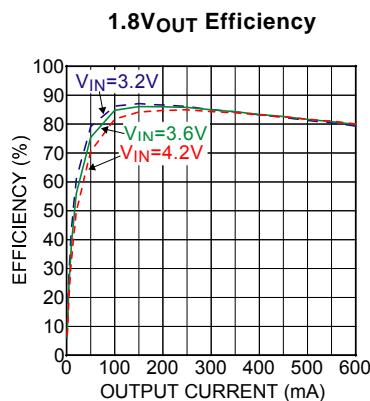
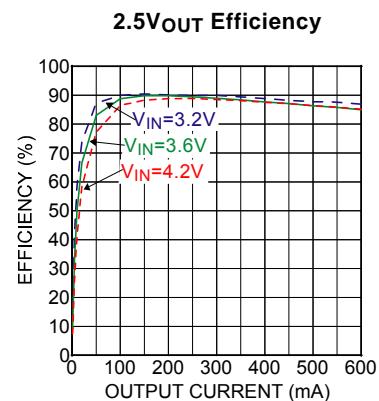
| Parameter | Condition | Min | Typ | Max | Units |
|--|--|---------------------|------------|---------------------|-------|
| Supply Voltage Range | | 2.7 | | 5.5 | V |
| Under-Voltage Lockout Threshold | (turn-on) | 2.45 | 2.55 | 2.65 | V |
| UVLO Hysteresis | | | 100 | | mV |
| Quiescent Current, PWM mode | $V_{FB} = 0.9 * V_{NOM}$ (not switching) | | 790 | 900 | µA |
| Quiescent Current, LDO mode | $V_{LOWQ} = 0V; I_{OUT} = 0mA$ | | 20 | 29 | µA |
| Shutdown Current | $V_{EN} = 0V$ | | 0.01 | 5 | µA |
| [Adjustable] Feedback Voltage | ±1% ±2% (over temperature) | 0.99 0.98 | 1 | 1.01 1.02 | V |
| [Fixed Output] Voltages | Nominal V_{OUT} tolerance | -1 -2 | | +1 +2 | % |
| FB pin input current | | | 1 | | nA |
| Current Limit in PWM Mode | $V_{FB} = 0.9 * V_{NOM}$ | 0.75 | 1 | 1.85 | A |
| Output Voltage Line Regulation | $V_{OUT} > 2V; V_{IN} = V_{OUT} + 300mV$ to 5.5V; $I_{LOAD} = 100mA$ $V_{OUT} < 2V; V_{IN} = 2.7V$ to 5.5V; $I_{LOAD} = 100mA$ | | 0.13 | | % |
| Output Voltage Load Regulation, PWM Mode | $20mA < I_{LOAD} < 300mA$ | | 0.2 | 0.8 | % |
| Output Voltage Load Regulation, LDO Mode | $100\mu A < I_{LOAD} < 50mA$ $V_{LOWQ} = 0V$ | | 0.5 | 1 | % |
| Maximum Duty Cycle | $V_{FB} \leq 0.4V$ | 100 | | | % |
| PWM Switch ON-Resistance | $I_{SW} = 50mA \quad V_{FB} = 0.7V_{FB_NOM}$ (High Side Switch) $I_{SW} = -50mA \quad V_{FB} = 1.1V_{FB_NOM}$ (Low Side Switch) | | 0.4 0.4 | | Ω |
| Oscillator Frequency | | 7.2 | 8 | 8.8 | MHz |
| LOWQ Threshold Voltage | | 0.5 | 0.85 | 1.3 | V |
| LOWQ Input Current | | | 0.1 | 2 | µA |
| Enable Threshold | | 0.5 | 0.85 | 1.3 | V |
| Enable Input Current | | | 0.1 | 2 | µA |
| LDO Dropout Voltage | $I_{OUT} = 50mA$ Note 5 | | 110 | | mV |

| Parameter | Condition | Min | Typ | Max | Units |
|-----------------------------|---|-----|-----|-----|---------------|
| Output Voltage Noise | LOWQ = 0V; $C_{OUT} = 10\mu F$, 10Hz to 100kHz | | 75 | | μV_{rms} |
| LDO Current Limit | LOWQ = 0V; $V_{OUT} = 0V$ (LDO Mode) | 60 | 120 | | mA |
| Over-Temperature Shutdown | | | 160 | | $^{\circ}C$ |
| Over-Temperature Hysteresis | | | 20 | | $^{\circ}C$ |

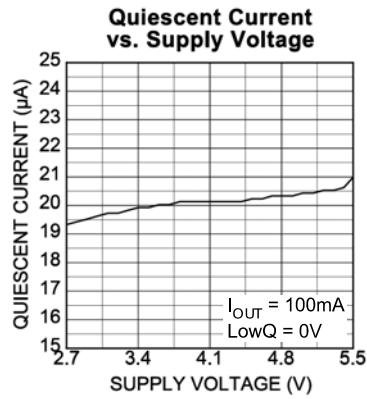
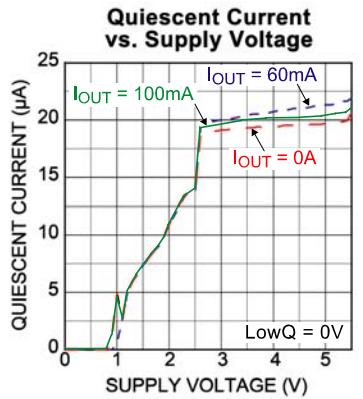
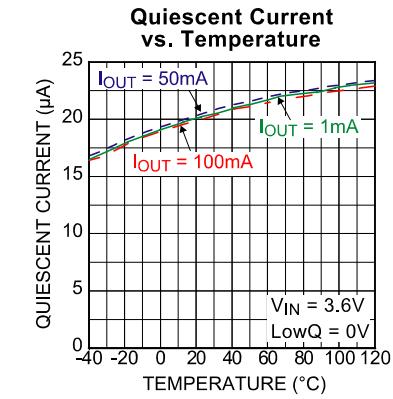
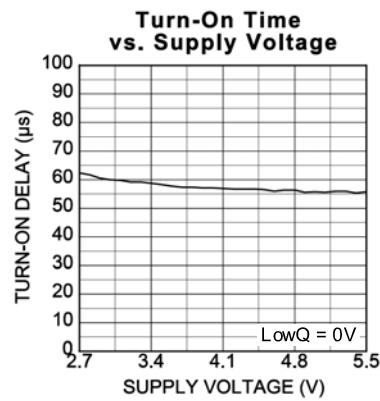
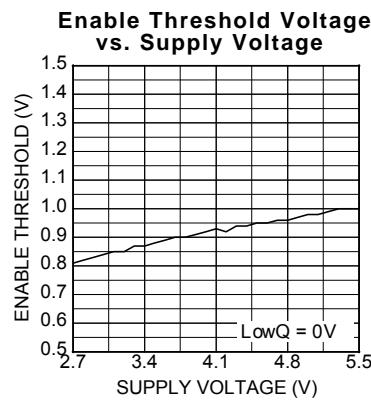
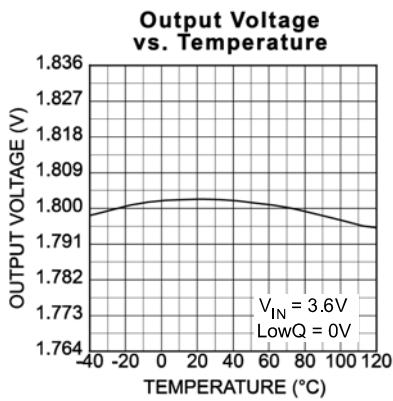
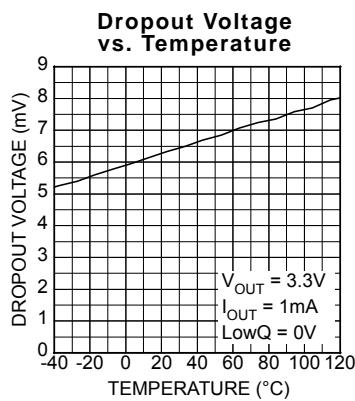
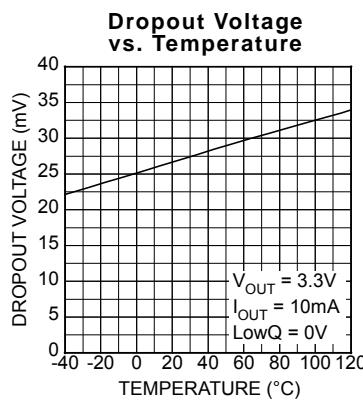
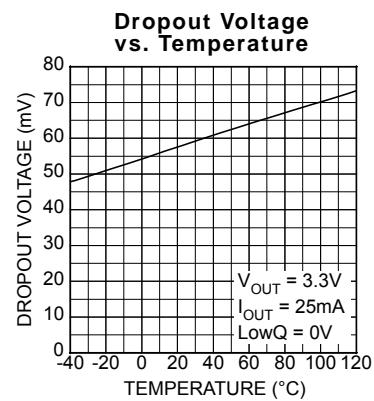
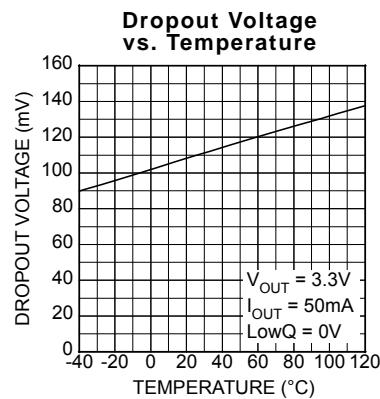
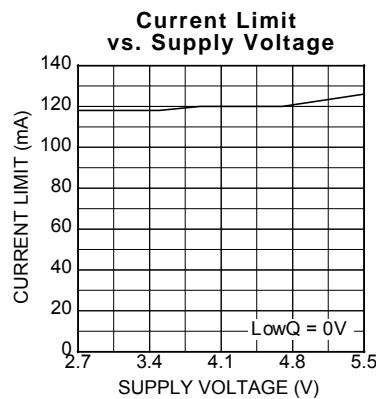
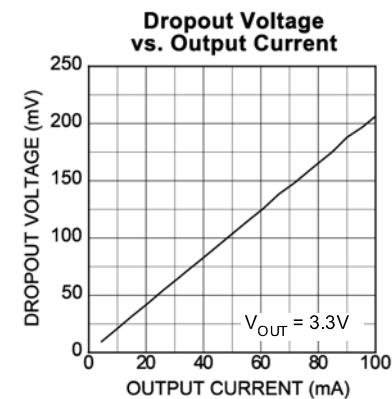
Notes

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model: $1.5k\Omega$ in series with $100pF$.
4. Specification for packaged product only.
5. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value that is initially measured at a 1V differential. For outputs below 2.7V, the dropout voltage is the input-to-output voltage differential with a minimum input voltage of 2.7V.

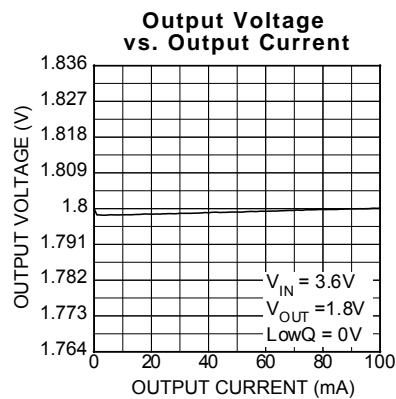
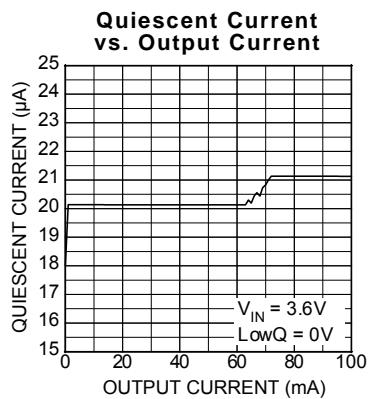
Typical Characteristics – PWM Mode



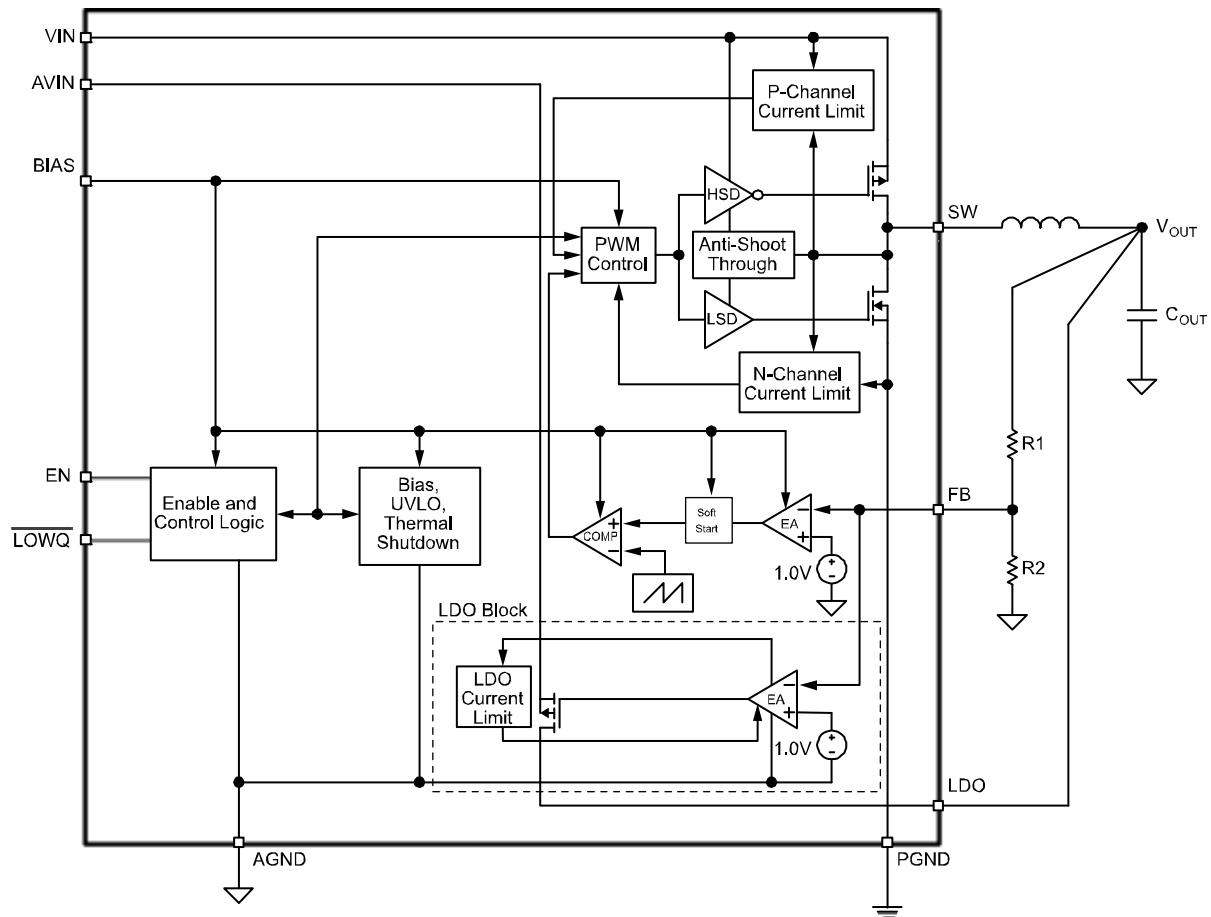
Typical Characteristics - LDO Mode



Typical Characteristics – LDO Mode (cont.)

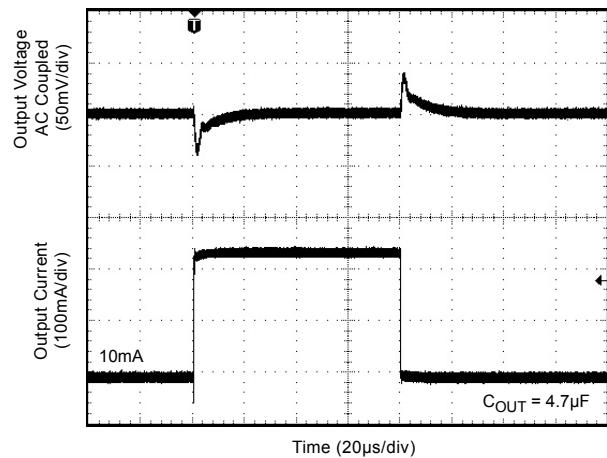
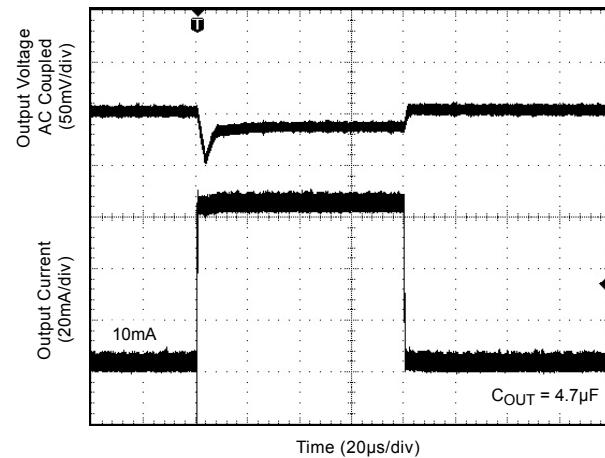
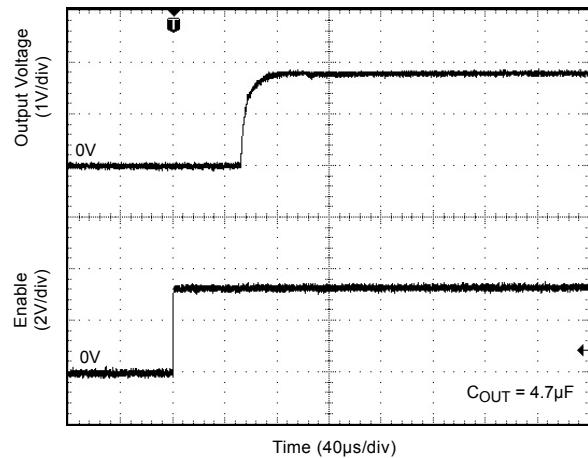
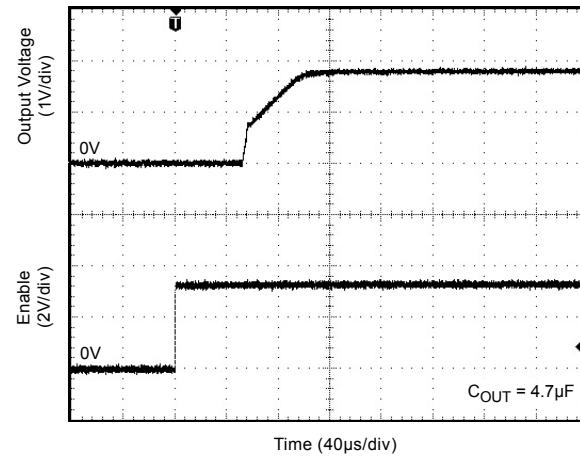


Functional Diagram



MIC2285A Block Diagram

Functional Characteristics

Load Transient PWM Mode**Load Transient LDO Mode****Enable Transient PWM Mode****Enable Transient LDO Mode**

Functional Description

VIN

VIN provides power to the MOSFETs for the switch mode regulator section, along with the current limiting sensing. Due to the high switching speeds, a $1\mu\text{F}$ capacitor is recommended close to VIN and the power ground (PGND) pin for bypassing. Please refer to layout recommendations.

AVIN

Analog V_{IN} (AVIN) provides power to the LDO section. AVIN and VIN must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by VIN is reduced before reaching AVIN.

LDO

The LDO pin is the output of the linear regulator and should be connected to the output. In LOWQ mode ($LOWQ < 1.5\text{V}$), the LDO provides the output voltage. In PWM mode ($LOWQ > 1.5\text{V}$), the LDO pin is high impedance.

EN

The enable pin provides a logic level control of the output. In the off state, supply current of the device is greatly reduced (typically $<1\mu\text{A}$). Also, in the off state, the output drive is placed in a "tri-stated" condition, where both the high side P-channel MOSFET and the low-side N-channel are in an "off" or non-conducting state. Do not drive the enable pin above the supply voltage.

LOWQ

The LOWQ pin provides a logic level control between the internal PWM mode and the low noise linear regulator mode. With LOWQ pulled low ($<0.5\text{V}$), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical I_Q of $20\mu\text{A}$. In linear (LDO) mode, the output can deliver 60mA of current to the output. By placing LOWQ high ($>1.5\text{V}$), this transitions the device into a constant frequency PWM buck regulator mode. This allows the device the ability to efficiently deliver up to 500mA of output current at the same output voltage.

BIAS

The BIAS pin supplies the power to the internal power to the control and reference circuitry. The bias is powered from the input voltage through an RC lowpass filter. The RC lowpass filter frequency must

$$\text{be } \geq \frac{1}{2\pi(20.5\Omega)(100\text{nF})}.$$

FB

The feedback pin (FB) provides the control path to control the output. For adjustable versions, a resistor divider connecting the feedback to the output is used to adjust the desired output voltage. The output voltage is calculated as follows:

$$V_{OUT} = V_{REF} \times \left(\frac{R1}{R2} + 1 \right)$$

Where V_{REF} is equal to 1.0V .

A feedforward capacitor is recommended for most designs using the adjustable output voltage option. To reduce battery current draw, a 100K feedback resistor is recommended from the output to the FB pin (R1). Also, a feedforward capacitor should be connected between the output and feedback (across R1). The large resistor value and the parasitic capacitance of the FB pin can cause a high frequency pole that can reduce the overall system phase margin. By placing a feedforward capacitor, these effects can be significantly reduced. Typically, an 82pF small ceramic capacitor is recommended.

SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible and separate from the Analog ground (AGND) loop. Refer to the layout considerations for more details.

AGND

Signal ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power ground (PGND) loop. Refer to the layout considerations for more details.

Applications Information

The MIC2285A is a 500mA PWM power supply that utilizes a LOWQ light load mode to maximize battery efficiency in light load conditions. This is achieved with a LOWQ control pin that when pulled low, shuts down all the biasing and drive current for the PWM regulator, drawing only 18 μ A of operating current. This allows the output to be regulated through the LDO output, capable of providing 60mA of output current. This method has the advantage of producing a clean, low current, ultra-low noise output in LOWQ mode. During LOWQ mode, the SW node becomes high impedance, blocking current flow. Other methods of reducing quiescent current, such as pulse frequency modulation (PFM), or bursting techniques, create large amplitude, low frequency ripple voltages that can be detrimental to system operation.

When more than 60mA is required, the LOWQ pin can be forced high, causing the MIC2285A to enter PWM mode. In this case, the LDO output makes a "hand-off" to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off allowing up to 600mA of current to be efficiently supplied through the PWM output to the load.

Input Capacitor

A minimum 1 μ F ceramic is recommended on the VIN pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

A minimum 1 μ F is recommended close to the VIN and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to layout recommendation section of data sheet for proper layout of the input capacitor.

Output Capacitor

The MIC2285A is optimized for a 10 μ F output capacitor. A larger value can be used to improve transient response. The MIC2285A utilizes type III internal compensation and utilizes an internal high frequency zero to compensate for the double pole roll off of the LC filter. For this reason, larger output capacitors can create instabilities. X5R or X7R dielectrics are recommended for the output capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

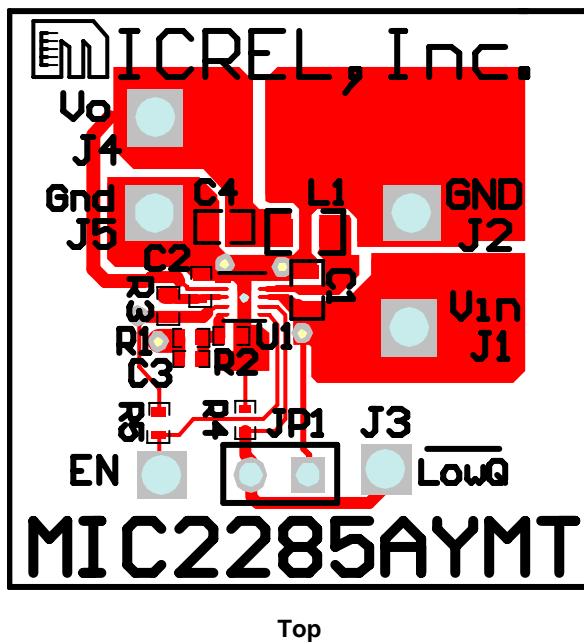
In addition to a 10 μ F, a small 10nF is recommended close to the load for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL.

Inductor Selection

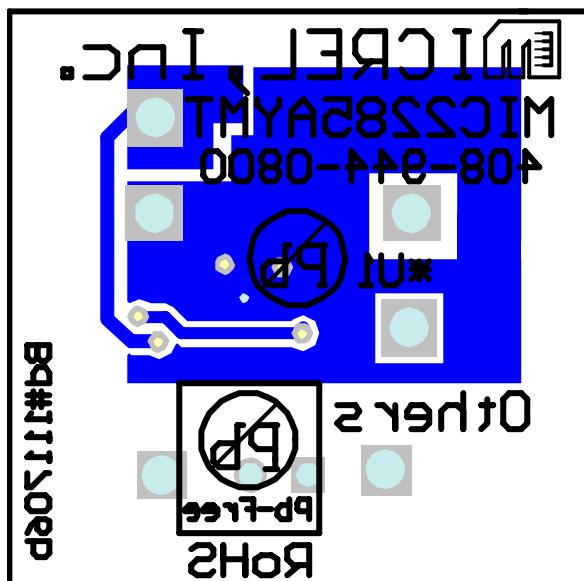
The MIC2285A is designed for use with a 0.47 μ H inductor. Proper selection should ensure that the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

$$I_{PK} = I_{OUT} + \frac{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{2 \times f \times L}$$

Layout Recommendation



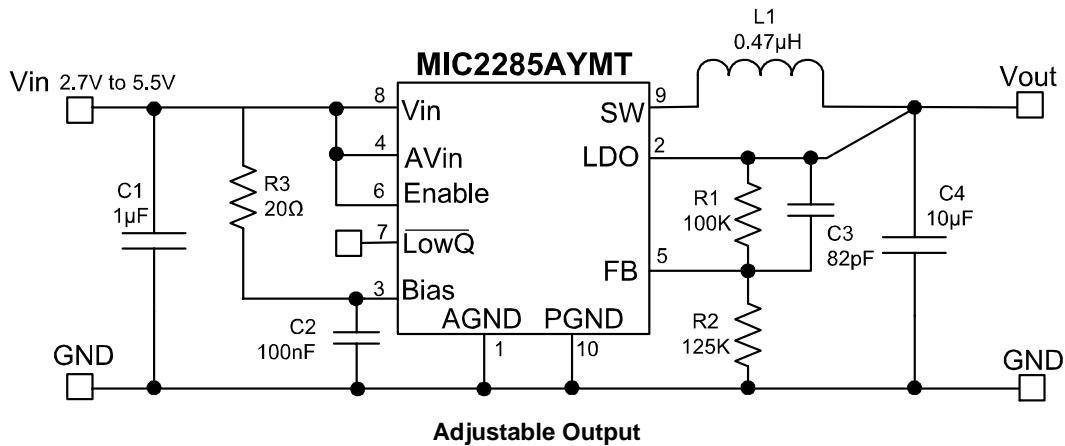
Top



Bottom

Note

The above figures demonstrate the recommended layout for the MIC2285A adjustable option.



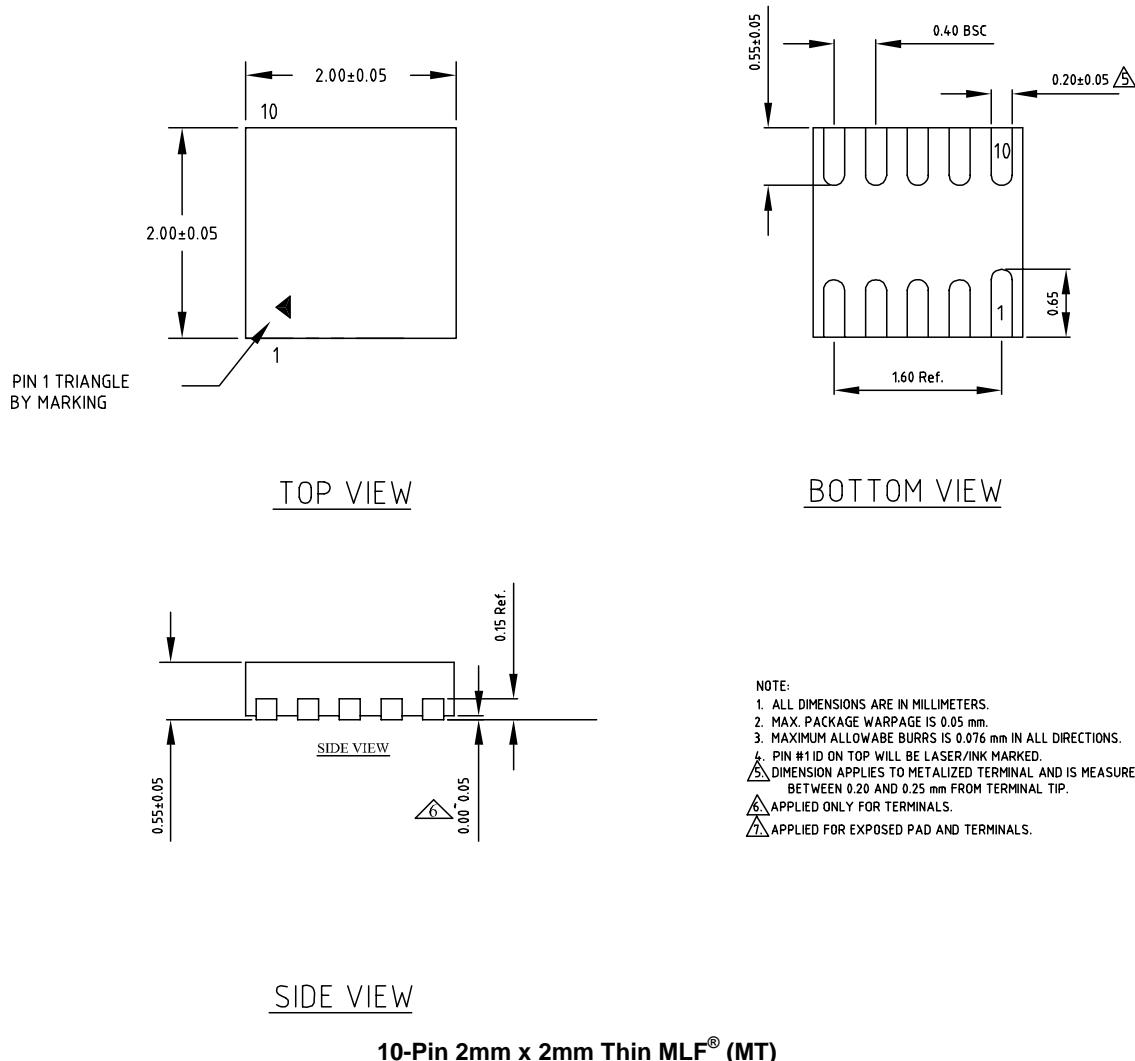
Bill of Materials

| Item | Part Number | Manufacturer | Description | Qty |
|------|--------------------|-----------------------------|--|-----|
| C1 | 06036D105MAT2 | AVX ⁽¹⁾ | | |
| | GRM185R60J105KE21D | Murata ⁽²⁾ | 1μF Ceramic Capacitor X5R, 6.3V 0603 | 1 |
| C2 | 0201ZD103MAT2 | AVX ⁽¹⁾ | | |
| | GRM033R10J103KA01D | Murata ⁽²⁾ | 10nF Ceramic Capacitor, 6.3V 0201 | 1 |
| C3 | VJ0402A101KXAA | Vishay ⁽³⁾ | 100pF Ceramic Capacitor | 1 |
| C4 | | AVX ⁽¹⁾ | | |
| | | Murata ⁽²⁾ | 10μF Ceramic Capacitor X5R, 6.3V 0603 | 1 |
| | LQM21PNR47M00 | Murata ⁽²⁾ | 0.47μH Inductor, 120mΩ 2.0mm x 1.25mm x 0.5mm | |
| L1 | | Murata ⁽²⁾ | 0.47μH Inductor, 97mΩ 3.2mm x 2.5mm x 1.55mm | 1 |
| | | Sumida ⁽⁴⁾ | 0.47μH Inductor, 94mΩ 3.2mm x 3.2mm x 1.55mm | |
| R1 | CRCW04021002F | Vishay-Dale ⁽³⁾ | 100kΩ 1% 0402 Resistor | 1 |
| R2 | CRCW04026652F | Vishay-Dale ⁽³⁾ | 66.5kΩ 1% 0402 Resistor for 2.5V _{OUT} | 1 |
| | CRCW04021243F | Vishay-Dale ⁽³⁾ | 124kΩ 1% 0402 Resistor for 1.8V _{OUT} | |
| | CRCW04022003F | Vishay-Dale ⁽³⁾ | 200kΩ 1% 0402 Resistor for 1.5V _{OUT} | |
| | CRCW04024023F | Vishay-Dale ⁽³⁾ | 402kΩ 1% 0402 Resistor for 1.2V _{OUT} | |
| | | | Open for 1.0V _{OUT} | |
| R3 | CRCW040220R5F | Vishay ⁽³⁾ | 20Ω 1% 0402 Resistor | 1 |
| U1 | MIC2285AYMT | Micrel⁽⁵⁾ | 8MHz Synchronous Buck Regulator with LOWQ® Mode | 1 |

Notes:

1. AVX: www.avxcorp.com
2. Murata: www.murata.com
3. Vishay: www.vishay.com
4. Sumida: www.sumida.com
5. **Micrel, Inc.:** www.micrel.com

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