
Keyboard and Embedded Controller for Notebook PC

Features

- 3.3V Operation with 5V Tolerant Buffers on PS/2 pins
- ACPI 1.0/2.0 PC99/PC2001 Compliant
- LPC Interface with Clock Run Support
 - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
 - 15 Direct IRQs
 - ACPI SCI Interface
 - nSMI output and supporting PM registers
 - Shadowed write only registers
- Internal 64K SRAM
 - Loaded at VCC1 power from the HOST/8051 SPI Memory Interface
 - Provides 64KB of 8051 program space
 - 32k-Byte region shared with 8051 data space
- HOST/8051 SPI Memory Interface
 - 3-pin Full Duplex serial communication interface.
 - Two Chip Select Pins
 - Fully 8051 Controlled
 - Hardware Support for two SPI Flash Configurations:
 - Switched SPI Flash Configuration
 - Parallel Shared SPI Flash Configuration
- Two Power Planes
 - Low Standby Current in Sleep Mode
- ACPI Embedded Controller Interface
- Configuration Register Set Compatible with ISA Plug-and-Play Standard (Version 1.0a)
- High-Performance Embedded 8051 Keyboard and System Controller
 - Provides System Power Management
 - System Watch Dog Timer (WDT)
 - 8042 Style Host Interface
 - Supports Interrupt and Polling Access
 - 1024 Boot /ROM
 - 256 Bytes Data RAM
 - On-Chip Memory-Mapped Control Registers
 - Access to VCC0 Backed Registers
 - Up to 18x8 Keyboard Scan Matrix
 - Two 16-Bit Timer/Counters
 - Integrated Full-Duplex Serial Port Interface
 - Seventy-Three 8051 Interrupt Sources
- Thirty-Two 8-Bit, Host/8051 Mailbox Registers
- Sixty-Four Maskable Hardware Wake-Up Events
- Fast GATEA20
- Fast CPU_RESET
- Multiple Clock Sources and Operating Frequencies
- IDLE and SLEEP Modes
- Accurate Fail-Safe Ring Oscillator
 - Single Clock source for most 8051 and SIO functions
 - Provides 2% frequency accuracy
 - Lock Bit provides status
- Integrated Standby Power Reset Generator
 - VCC1_RST# output
- VCC0 Backed Resources
 - 16 Byte VCC0 Backed Registers
 - VCC0 Backed Status Register
 - 32.768KHz-input clock
 - <2μA Standby Current (typ)
- Two 8584-Style I²C/SMBus Controllers
 - 8051 Controlled Logic Allows I²C/SMBus Master or Slave Operation
 - I²C/SMBus Controllers are Fully Operational on Standby Power
 - 2 Sets of Dedicated Pins per I²C/SMBus Controller
- Four independent Hardware Driven PS/2 Ports
- 48 General Purpose I/O Pins
 - Maskable Hardware Wake-Event Capable
 - Programmable Open-Drain/Push-Pull Outputs
- 7 General-Purpose Outputs
- Four Programmable Pulse-Width Modulator Outputs
 - Independent Clock Rates
 - 6-Bit Duty Cycle Granularity
 - Operational in both Full on and Standby modes
- Consumer Infrared Receiver for Vista (CIRV)
 - Consumer Infrared Remote Control Receiver Interface
 - Support of all common CIR formats in S0 power state, per Vista standard mechanism.

- Hardware matching of Microsoft Remote input frames, with PME Wake (S3/S4/S5 power states).
- Programmable High-Speed Synchronous Communications Engine (SCE) with a 32-Byte FIFO and Programmable Threshold
- LED Control for Activity Indication
- Dual Fan Tachometer Inputs
- Debug Port (UART)
 - High-Speed 16550A-Compatible UART with 16-Byte Send/Receive FIFOs
 - Programmable Baud Rate Generator
 - Relocatable to 480 Different Base I/O Addresses
 - 15 IRQ Options
- BC-Link Interconnection Bus
 - Combined High Speed/Low Speed Bus Master Controller
- General Purpose Analog to Digital Converter (GP-ADC)
 - 10-bit conversion precision
 - 10-bit conversion per channel is completed in 10.91us
 - 4 ADC general purpose channels
 - Channel 0 has a 5 volt tolerant input
 - 10-bit Conversion with 3.22 mV resolution
 - 0 to 3.3 VDC Conversion Range
 - Channel 1, 2, & 3 has a 3.3 volt tolerant input with a 10-bit, 3.22 mV resolution
 - Optional continuous sampling at a programmable rate
 - Integral Non-Linearity of ± 0.5 LSB; Dynamic Non-Linearity of ± 0.5 LSB

Description

The MEC1308 is a 128-pin 3.3V LPC-based ACPI 2.0 and PC99/PC2001 compliant Notebook I/O Controller. See Figure 1, "MEC1308 Block Diagram".

The MEC1308 incorporates a high-performance 8051-based keyboard and system controller with internal 64k byte RAM; a 1K byte Boot ROM, and 16-bytes battery backed registers. The 64K RAM is loaded via HOST/8051 SPI Memory Interface. The HOST/8051 SPI Memory Interface can be configured in Switched SPI Flash Configuration or Parallel Shared SPI Flash Configuration.

The MEC1308 has four PS/2 ports; an 16C550A-compatible 2 pin UART for Debug Port; a Consumer Infra-red Receiver for Vista (CIRV), two 8584-style I²C/SMBus controllers with two selectable ports per controller; a Serial IRQ peripheral agent interface; an ACPI Embedded Controller Interface; forty-eight General Purpose I/O pins and seven General Purpose Outputs; four independently programmable pulse width modulators; dual fan control through the implementation of two fan tachometer input pins; hardware monitoring of a PWM input and maskable hardware wake-up events; one BC-Link Combined High Speed/Low Speed Bus Master Controller; 4 channel Analog to Digital Converter.

The MEC1308 has two separate power planes to provide "instant on" and system power management functions. Additionally, the MEC1308 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. Wake-up events and ACPI-related functions are supported through the SCI Interface.

The MEC1308 supports the ISA Plug-and-Play Standard (Version 1.0a) and provides all the functionality for current Windows O/S's. The I/O Address and Hardware IRQ of each logical device in the MEC1308 may be reprogrammed through the internal configuration registers. There are 480 I/O address location options and 15 IRQs for each logical device.

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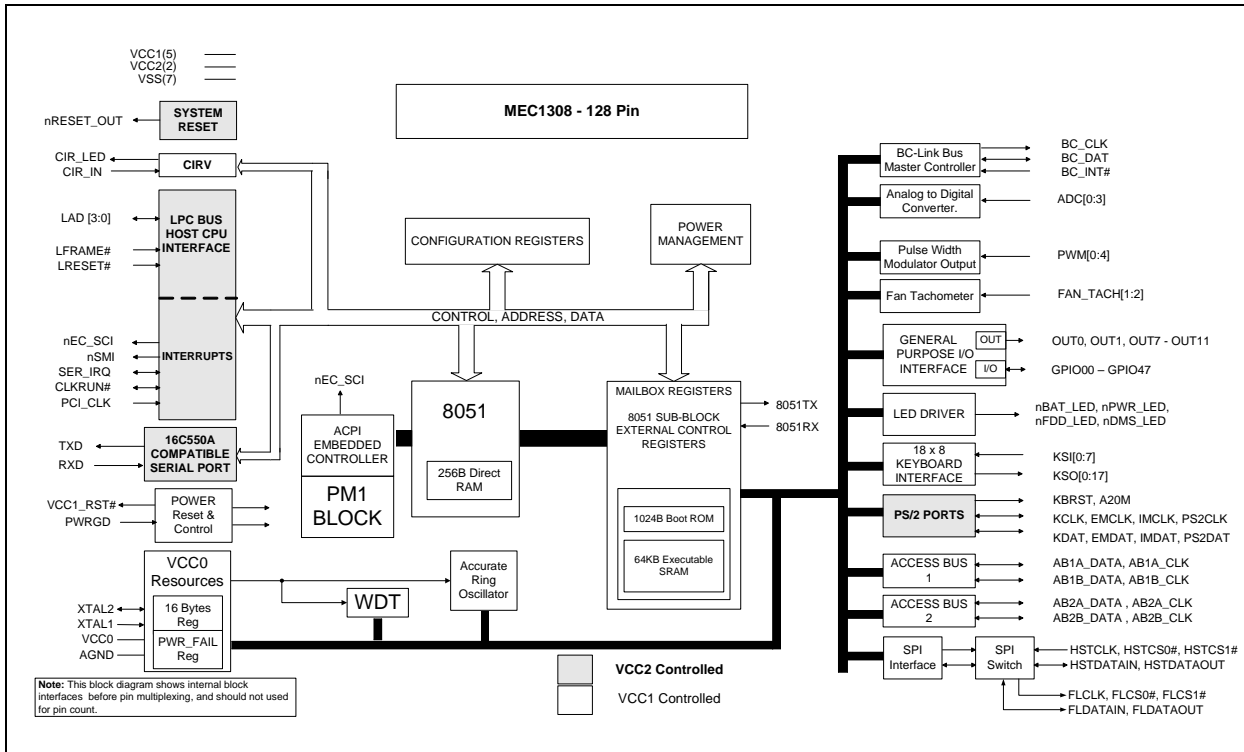
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MEC1308

BLOCK DIAGRAM

FIGURE 1: MEC1308 BLOCK DIAGRAM



PACKAGE OUTLINES

FIGURE 2: 128-PIN VTQFP PACKAGE

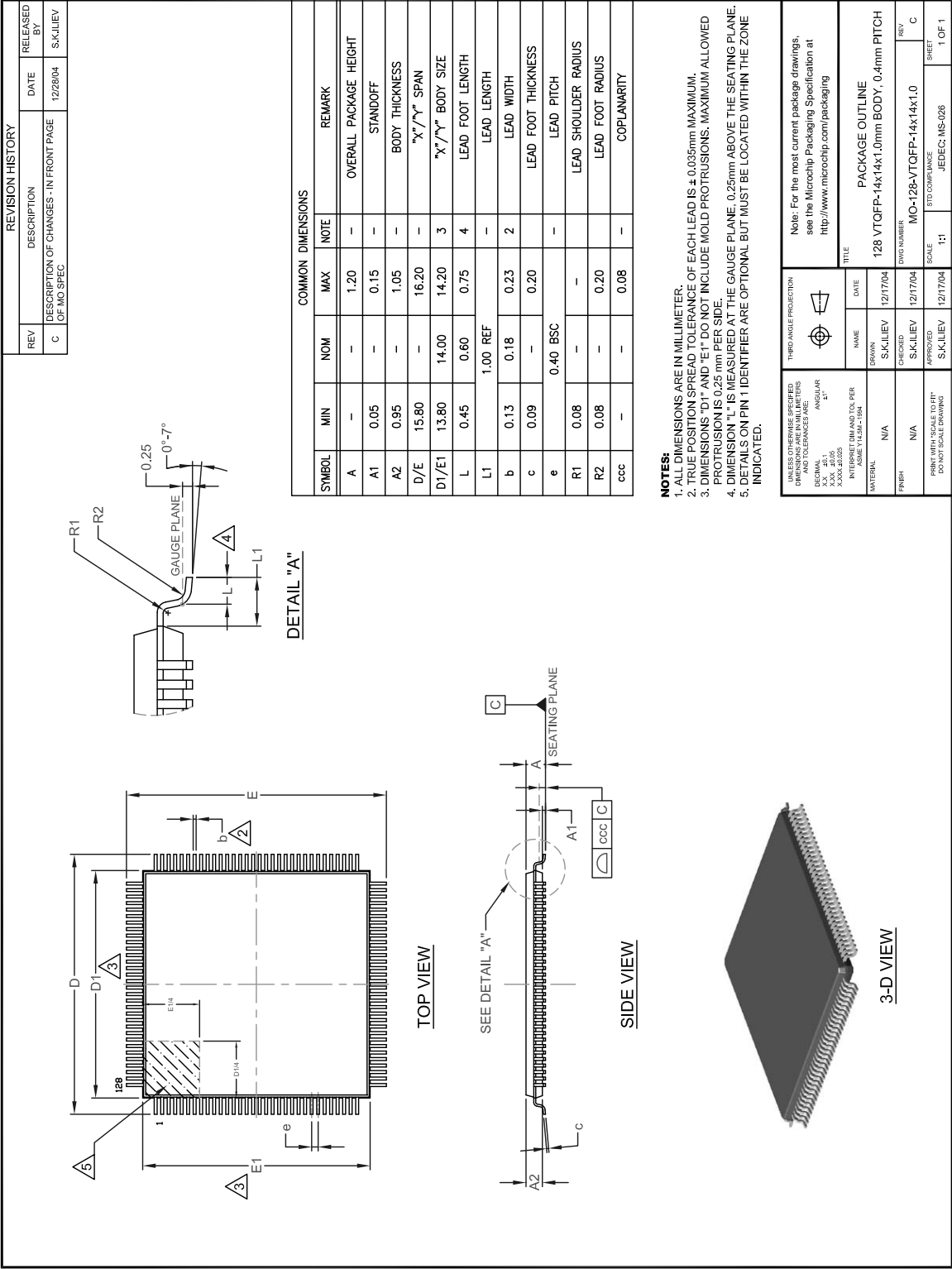
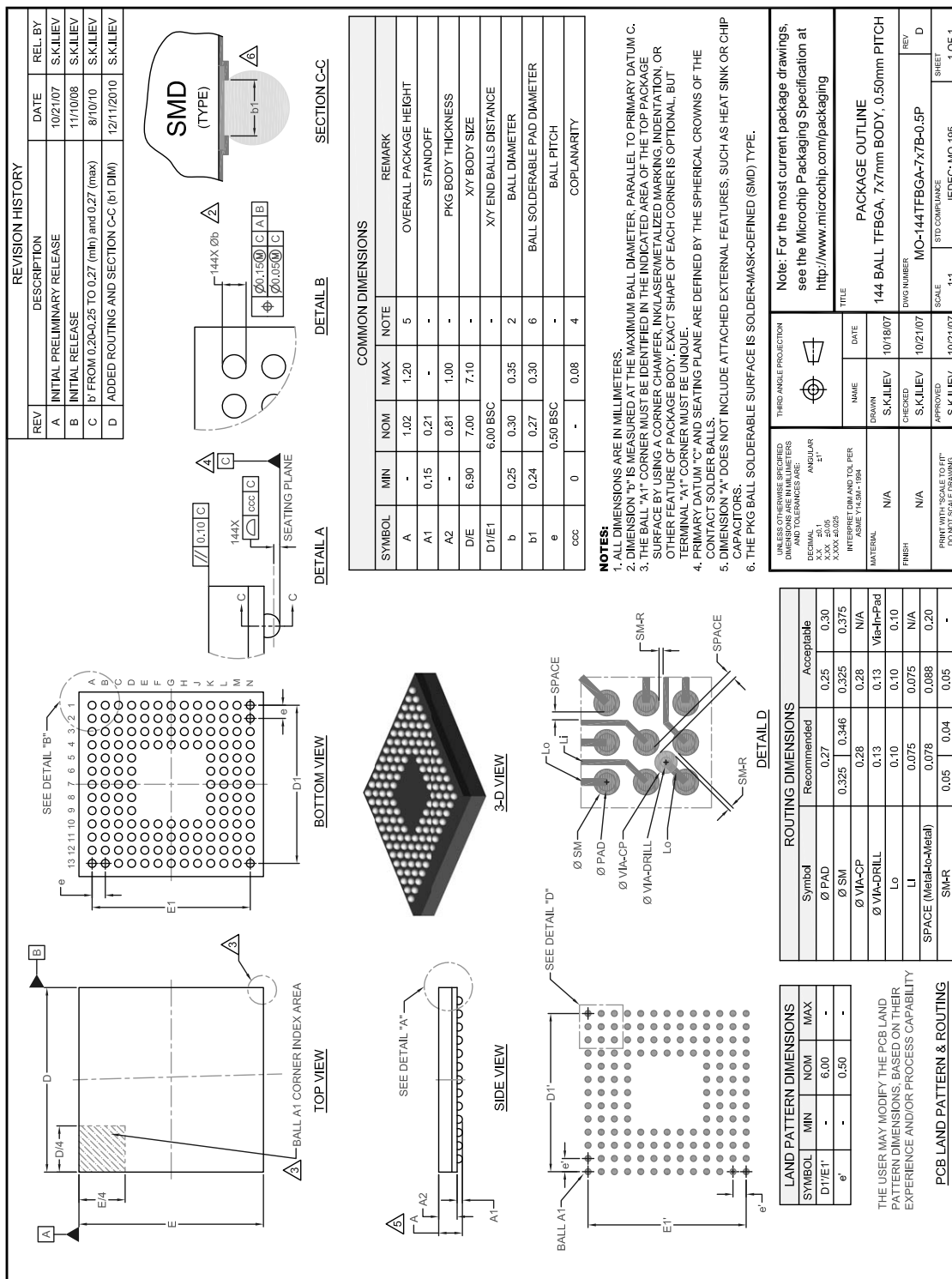


FIGURE 3: 144 BALL TFBGA PACKAGE



APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001753A (05-21-14)	Document release	

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