Synchronous Ethernet Packet Clock Network Synchronizer

Features

- Up to four independent clock channels
- Fully compliant to EEC (G.8262), SEC (G.813), GR-253 SMC and GR-1244 Stratum 3/3E
- Excellent jitter performance of 180 fs rms in the 12 KHz to 20 MHz band meeting jitter requirements for 10G/40G and 100G PHYs
- Three programmable ultra-low jitter synthesizers generate any frequency from 0.5Hz to 900MHz
- One programmable general purpose synthesizer generates any clock from 0.5 Hz to 180 MHz
- 6 differential (CML) or 12 single ended (CMOS) ultra-low jitter outputs plus two general purpose CMOS outputs
- Accepts up to 10 LVPECL/LVDS/HCSL/LVCMOS inputs
- Up to four programmable digital PLLs/NCOs with loop bandwidth from 0.1 mHz to 470 Hz synchronize to any clock rate from 0.5 Hz to 900 MHz

Ordering Information

ZL30601LDG6*	100 Pin aQFN	Trays
ZL30602LDG6*	100 Pin aQFN	Trays
ZL30603LDG6*	100 Pin aQFN	Trays
ZL30604LDG6*	100 Pin aQFN	Trays

*Pb Free Tin/Silver/Copper

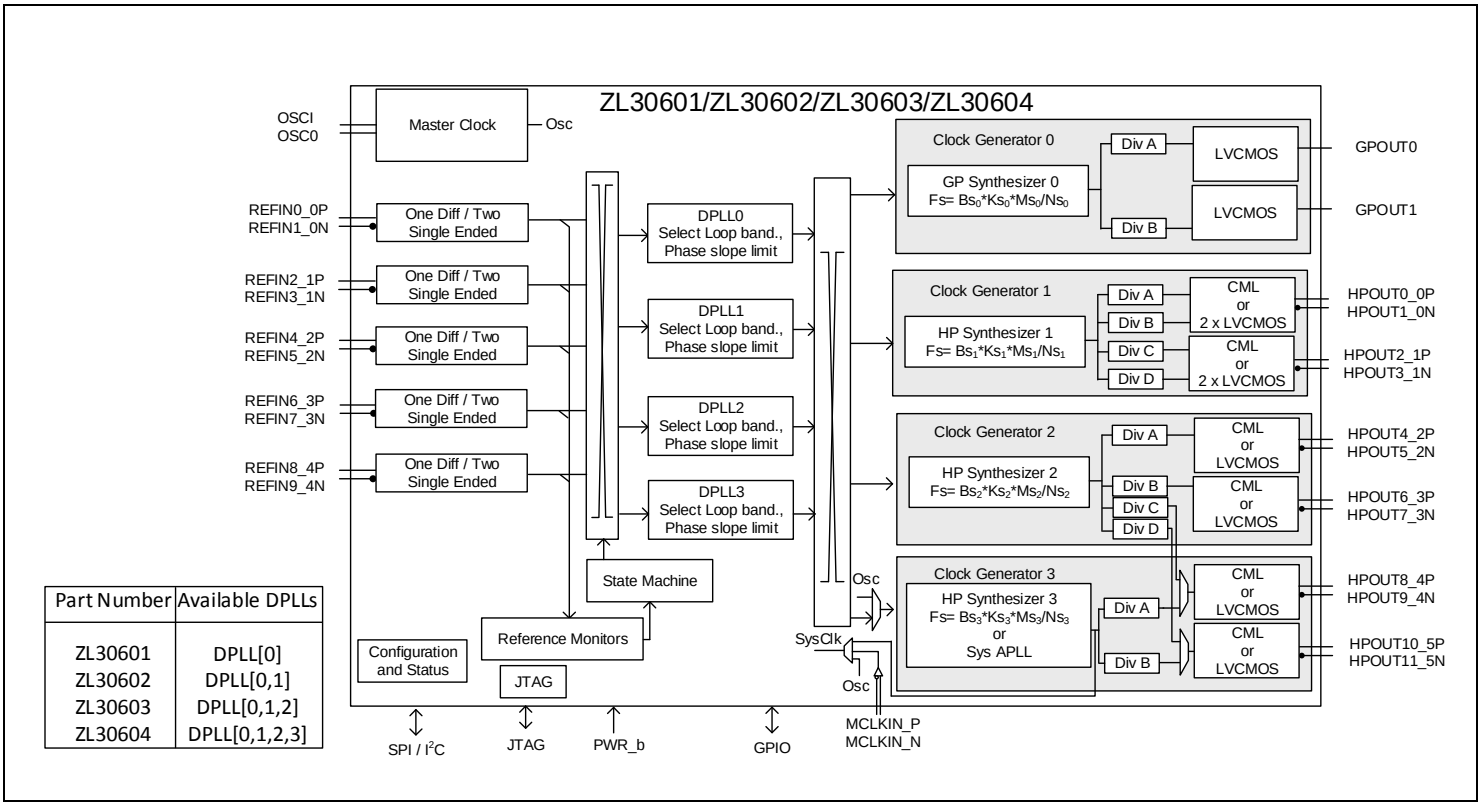
Package size: 10 x 10 mm

-40°C to +85°C

- Automatic hitless reference switching and digital holdover on reference fail with initial holdover accuracy better than 0.1 ppb
- Any input reference can be fed with clock, sync (frame pulse), clock /sync pair or clock modulated with sync pulse (embedded PPS ePPS and embedded PP2S ePP2S)

Applications

- Synchronous Ethernet/Sonet/SDH timing and line cards
- Wireless Backhaul
- Wireless Base stations
- Test Equipment



Part Number	Available DPLLs
ZL30601	DPLL[0]
ZL30602	DPLL[0,1]
ZL30603	DPLL[0,1,2]
ZL30604	DPLL[0,1,2,3]

Figure 1. Functional Block Diagram

2 Feature List

2.1 General features

- Up to four independent clock channels
- Operates from a single crystal resonator or clock oscillator
  - Supports split XO mode for low-frequency stability TCXO/OCXO with ultra-low jitter clock outputs
- Configurable from SPI/I2C bus or from pre-configured flash memory

2.2 Electrical Clock Inputs

- Accepts up to 10 LVCMOS or 5 LVDS/HCSL/LVPECL/CML inputs
- Frequencies from 0.5 Hz to 180 MHz for LVCMOS
- Frequencies from 0.5 Hz to 900 MHz for LVDS/HCSL/LVPECL/CML
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities.
  - Each input reference has its own set of monitors which can be independently programmed.
  - Loss of signal (LOS)
  - Single Cycle Monitor (Triggers on glitches or variation in duty-cycle)
  - Coarse Frequency Monitor
  - Precise Frequency Monitor
- Locks to gapped clocks

2.3 Electrical Clock Input-Output Special Formats

- Supports 64 kHz composite clocks with external glue logic
- Supports embedded pulse per second (ePPS) single wire for carrying high-speed clock & 1PPS
- Supports REF-SYNC pair, a combination of a high speed clock reference and a frame pulse sync pair
- Each output can generate clock, sync pulse, embedded pulse per second (ePPS) or embedded pulse per 2 seconds (ePP2S)
  - Clock modulated sync feature helps in reducing number of clock lines on backplane and in addition provides equal delay for both clock and sync signals.

2.4 Electrical Clock Engine

- Digital PLLs filter jitter from 0.1 mHz up to 470 Hz
- Multiple modes of operation
  - Freerun
  - Forced holdover
  - Forced reference
  - Automatic
  - NCO
- Internal state machine automatically controls state
  - Locked
  - Acquiring
  - Holdover
- Support for fast lock with lock times in seconds
- Support for hitless reference switching
- Internal, per DPLL, time of day counters maintaining full 48-bit seconds and 32-bit nanoseconds aligned to 1PPS rollover
- Holdover better than 0.01 ppb
- Full rate conversion between input and output clock frequencies
- Supports ITU-T G.823, G.824 and G.8261 for 2048 Kbit/s and 1544 Kbit/s interfaces
- Supports G.781 SETS

2.5 Electrical Clock Engine: Industry Specifications

- Support for wide variety of Equipment Clock specifications
  - SyncE
    - ITU-T G.8262 option 1 EEC (Europe/China)
    - ITU-T G.8262 option 2 (USA)
  - SONET/SDH
    - ITU-T G.813 option 1 SEC (Europe/China)
    - ITU-T G.813 option 2 (USA)
    - ANSI T1.105/Telcordia GR-253 Stratum 3 for SONET
    - Telcordia GR-253 SMC
  - PDH
    - ITU-T G.812 Type I SSU
    - ITU-T G.812 Type II, ANSI T1.101/Telcordia GR-1244 Stratum 2 (without optional freq monitoring at 16 ppb)
    - ITU-T G.812 Type III, ANSI T1.101/Telcordia GR-1244 Stratum 3E
    - ANSI T1.101/Telcordia GR-1244 Stratum 3
    - ANSI T1.101/Telcordia GR-1244 Stratum 4E/4

2.6 Electrical Clock Generation

- Four programmable synthesizers
- Precision Synthesizers
  - Each ultra-low jitter output can be independently set to be differential (CML) or two CMOS
  - Six CML outputs
    - Generate clock rates from 0.5 Hz to 900 MHz
    - Jitter performance of 180 fs rms (12 KHz – 20 MHz)
    - Meets OC-192, STM-64, 1 GbE & 10 GbE interface jitter requirements
  - Twelve LVCMOS outputs
    - Generate clock rates from 0.5 Hz to 180 MHz
    - Jitter performance of 290 fs rms (12 kHz – 20 MHz)
- General Synthesizer
  - Two LVCMOS outputs
  - Generate clock rates from 1 Hz to 180 MHz
  - Jitter performance of 17 ps rms (12 kHz – 20 MHz)
- Programmable output advancement/delay to accommodate trace delays or compensate for system routing paths
- Each output has its own power supply pin which can be hooked to 3.3V, 2.5V or 1.8V supplies. Outputs may be disabled to save power

3 Application

The only difference between ZL30601/ZL30602/ZL30603/ZL30604 is the number of DPLLs. The least significant digit in the part number assigns the number of available DPLLs.

3.1 Applications Examples

- ITU-T G.8262 System Timing Cards which support 1 GbE and 10 GbE interfaces
- Telcordia GR-253 Carrier Grade SONET/SDH Stratum 3 System Timing Cards
- System Timing Cards which supports ITU-T G.781 SETS (SDH Equipment Timing Source)
- Integrated basestation reference synchronization for air interfaces for
- GSM, WCDMA, TD-SCDMA, LTE and LTE-A
- FDD or TDD mobile technology
- femtocells, small cells (residential, urban, rural, enterprise), picocells and macrocells
- Mobile Backhaul NID, cell-site router, edge switch/router, microwave or access aggregation node
- EPON/GPON OLT and ONU/OLT
- DSLAM and RT-DSLAM
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fiber Channel, XAUI

3.2 Physical Layer – Chassis Architecture

Block diagram of a traditional shelf based system.is shown in Figure 2**Error! Reference source not found.**. ZL30601/ZL30602/ZL30603/ZL30604 can be used in systems with timing redundancy as shown in Figure 2. These systems have dual timing cards—Active and Redundant—and number of line cards. All synchronous devices on line cards are locked to Active timing card. If the Active timing card fails, all line cards will switch to the clock provided by the Redundant timing card. To facilitate seamless transition, the redundant clock has to be replica of the active one—has to be locked in frequency and phase. This is achieved by locking redundant card to the Active card.
During the timing card rearrangements, the Redundant card will first go into holdover to avoid tracking input from the failed card and then it will lock to the same reference the active card was lock to—GPS in our example—as long as the GPS reference is good.

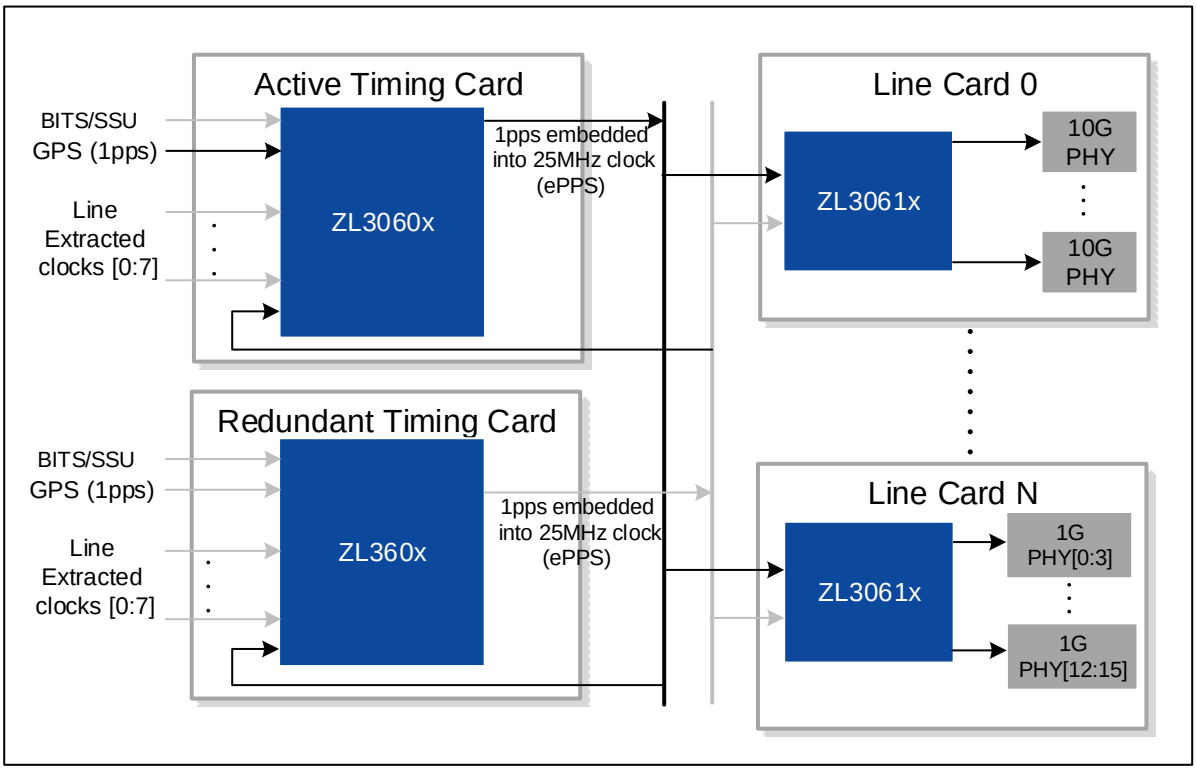


Figure 2. System with timing redundancy

4 Product Family

There are several devices within the ZL30601/602/603/604 family. They are differentiated by the number of DPLL, as shown in

Table 1 · ZL3060x Product Family

Product Number	Number of DPLL Channels	Number of Synthesizers
ZL30601	1	4
ZL30602	2	4
ZL30603	3	4
ZL30604	4	4

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