SST11LF04

4.9-5.9 GHz High-Linearity, High-Efficiency Front-end Module

FEATURES

- Input/output ports internally matched to 50Ω and DC decoupled
- Package available
  - 16-contact X2QFN – 2.5mm x 2.5mm x 0.4mm (max)
- Devices are RoHS compliant

Transmitter Chain

- Operating voltage 3.0V to 5.0V
- Gain:
  - Typically 30 dB gain across 4.9-5.9 GHz at 3.3V
- Typical linear output power at 3.3V:
  - Meets 802.11a OFDM ACPR requirement up to 21 dBm
  - Meets 802.11ac spectrum mask requirement up to 20 dBm
  - 3.0% dynamic EVM up to 18 dBm for 802.11a, 54 Mbps
  - 1.75% dynamic EVM up to 16 dBm for 802.11ac, MCS9, 80 MHz
- Operating current for 802.11a/n/ac applications
  - 270 mA @ P_{OUT} = 18 dBm for 802.11a at 3.3V
- I_{PEN}: 6 mA
- Idle current: 210 mA I_{CQ}
- Low shut-down current: ~2 µA
- High-speed power-up/down
  - Turn on/off time (10%–90%) <400 ns
- Limited variation over temperature
  - ~1 dB gain/power variation between -40°C to +85°C
- Excellent on-chip power detection
  - Load and temperature insensitive
  - >20 dB dynamic range on-chip power detection

Receiver Chain

- Gain:
  - Typically 12 dB gain across 4.9-5.9 GHz
- Noise figure
  - Typically 2.95 dB across 4.9-5.9 GHz
- LNA bypass loss
  - Typically 8 dB

Applications

- WLAN–IEEE 802.11a/n/ac
- WAVE(IEEE 802.11p)
- Home RF
- Cordless phones
- 5 GHz ISM wireless equipment

PRODUCT DESCRIPTION

SST11LF04 is a 4.9-5.9 GHz Front-end Module (FEM) designed in compliance with IEEE 802.11a/n/p/ac applications. Based on GaAs pHEMT/HBT technology, it combines a high-performance Power Amplifier (PA), a low-noise amplifier (LNA) and an antenna Tx/Rx switch (SW). The input/output RF ports are single-ended and internally matched to 50 Ω. These RF ports are DC decoupled, and require no external DC-blocking capacitors or matching components. This helps reduce the system board Bill of Materials (BOM) cost.

There are two functional components to the FEM: the Transmitter (TX) chain and the Receiver (RX) chain.

The TX chain includes a high-efficiency PA based on the InGaP/GaAs HBT technology. At 3.3V, the transmitter typically provides 30 dB gain and provides 802.11a spectrum mask compliance at 21 dBm. The TX chain has excellent linearity, typically 3% dynamic EVM at 18 dBm output power, with 802.11a, 54 Mbps operation and requires only 270 mA DC current. It also provides up to 16 dBm output power with 1.75% dynamic EVM using 802.11ac MCS9, 80 MHz modulation. SST11LF04 transmitter features a high-speed power-up/-down control with low current (total I_{PEN} ~6 mA).

SST11LF04 has an excellent on-chip, single-ended power detector that is stable over temperature and insensitive to output VSWR. This detector features a wide dynamic-range (20 dB) with dB-wise linear operation, thus providing a reliable solution to board-level power control.

The Rx chain provides typically 12 dB gain with 2.95 dB noise figure. With the LNA bypassed, the receiver loss is typically 8 dB with P1dB>20 dBm.

SST11LF04 is offered in a16-contact X2QFN package. See Figure 2-1 for pin assignments and Table 2-1 for pin descriptions.

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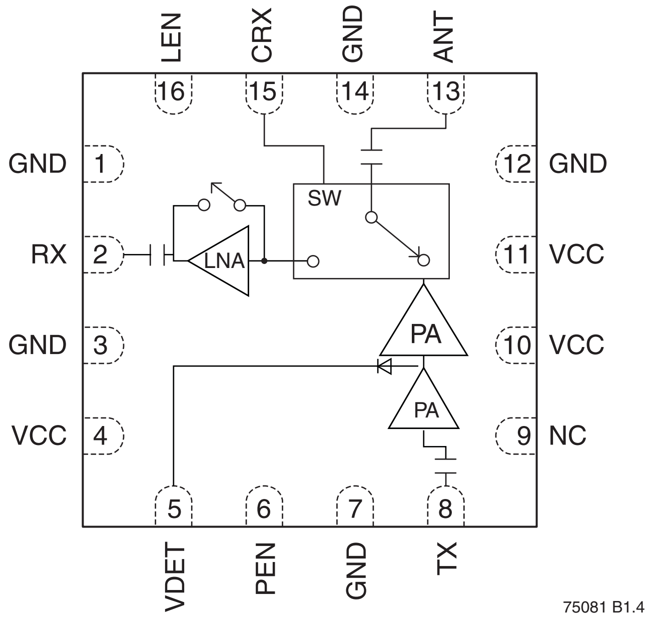
1.0 FUNCTIONAL BLOCKS

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN ASSIGNMENTS

FIGURE 2-1: PIN ASSIGNMENTS FOR 16-CONTACT X2QFN

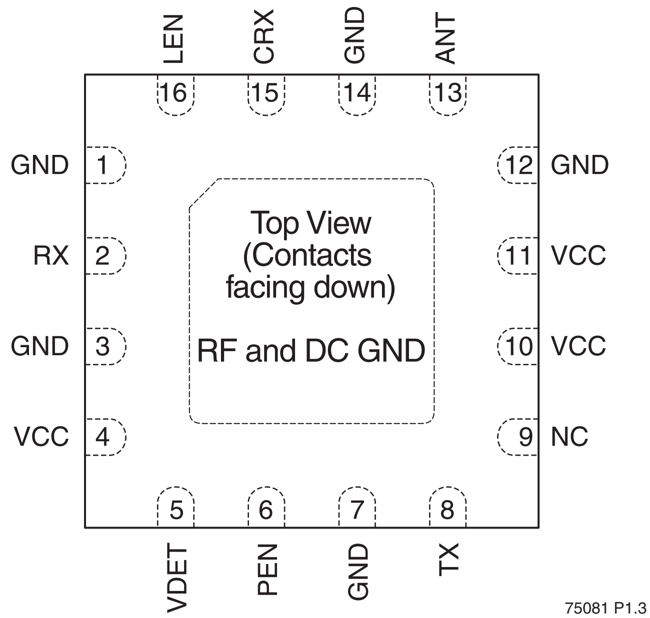


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin No.	Pin Name	Type[1]	Function
GND	1	Ground		Ground pad
RX	2		O	LNA output
GND	3	Ground		Ground pad
VCC	4	Power Supply	PWR	Supply Voltage
VDET	5		O	Detector output voltage
PEN	6		I	PA enable
GND	7	Ground		Ground pad
TX	8		I	RF transmit input
NC	9			No Connection
VCC	10	Power Supply	PWR	Supply voltage
VCC	11	Power Supply	PWR	Supply voltage
GND	12	Ground		Ground pad
ANT	13		I/O	Antenna
GND	14			Ground pad
CRX	15		I	Switch control pin voltage
LEN	16		I	LNA Enable

1. I=Input, O=Output

3.0 ELECTRICAL SPECIFICATIONS

The DC and RF specifications for the power amplifier are specified below. Refer to Table 3-2 for the DC voltage and current specifications.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Tx input power to pin 8 (TX)[1] . . . . +5 dBm
Rx input power to pin 13 (ANT with LNA ON) . . . . +5 dBm
Average Tx output power from pin 13 (ANT)[2] . . . . +22 dBm
Supply Voltage at pins 4, 10, and 11 (V_{CC}) . . . . +5.2V
PA enable voltage to pin 6 (PEN) . . . . +3.6V
DC supply current (I_{CC})[3] . . . . 400 mA
Operating Temperature (T_A) . . . . -40ºC to +85ºC
Storage Temperature (T_{STG}) . . . . -40ºC to +120ºC
Maximum Junction Temperature (T_J) . . . . +150ºC
Surface Mount Solder Reflow Temperature . . . . 260°C for 10 seconds

1. At 5.0V bias, the RF-input power must be less than 5 dBm while operating into a maximum antenna port VSWR of 6:1. At 5.5V bias, the maximum VSWR is 2:1 with a maximum input-RF power of 5 dBm.
2. Never measure with CW source. Pulsed single-tone source with <50% duty cycle is recommended. Exceeding the maximum rating of average output power could cause permanent damage to the device.
3. Measured with 100% duty cycle 54 Mbps 802.11a OFDM Signal

TABLE 3-1: OPERATING RANGE

Range	Ambient Temp	V_{CC}
Industrial	-40°C to +85°C	3.0V to 5.5V

TABLE 3-2: DC ELECTRICAL CHARACTERISTICS AT 25°C FOR TX CHAIN

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{CC}	Supply Voltage at pins 4, 10, and 11	3.0	3.3	5.5	V
V_{PEN}	Tx PA Enable Voltage		2.95		V
I_{CQ}	Tx Idle current for 802.11a to meet EVM ~3% @ 17 dBm		210		mA
I_{CC}	Tx Supply Current for 11a OFDM 54 Mbps signal, P_{OUT} = 18 dBm, 3.3 V V_{CC}		270		mA
I_{CC}	Rx Supply Current (with LNA ON)		11		mA
I_{PEN}	I_{PEN} PA Enable Control Current		6		mA

TABLE 3-3: TX CHAIN RF CHARACTERISTICS AT 25°C V_{CC} = 3.3V, PEN = 2.95V

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range	4.9		5.9	GHz
Linearity,	Output Power with <3% dynamic EVM, 802.11a @ 54 Mbps OFDM		18		dBm
	Output Power level <1.75% dynamic EVM, 802.11ac MCS9, 80 MHz BW		16		dBm
G	Gain over band	24	30		dB
RL_{IN}	Input return loss at TX port	6	11		dB
V_{DET}	Power detector output voltage range, 0-20 dBm	0.3		0.95	V
2f, 3f, 4f, 5f	Harmonics at 17 dBm			-30	dBm/ MHz

TABLE 3-4: RECEIVER CHAIN RF CHARACTERISTICS AT 25°C, V_{CC} = 3.3V

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range	4.9		5.9	GHz
G	Gain, with LNA ON		12		dB
NF	Noise figure, with LNA ON		2.95		dB
IP1dB	Input P1dB, with LNA ON		-6		dBm
Loss	LNA bypassed		8		dB
RL_{IN}	Input return loss at Antenna port with LNA		12		dB

TABLE 3-5: CONTROL VOLTAGES[1]

Function	PEN	CRX	LEN
Transmit mode	3.0V	0	0
Receive mode, LNA on	0	3.0	3.0
Receive mode, LNA bypass	0	3.0	0
OFF	0	0	0

1. No other operating modes are allowed

4.0 TYPICAL TRANSMITTER PERFORMANCE CHARACTERISTICS

Test Conditions: V_{CC} = 3.3V, T_A = 25°C, PEN = 3.0V, 802.11a 54 Mbps OFM Modulation Unless otherwise specified

FIGURE 4-1: TRANSMITTER S-PARAMETER

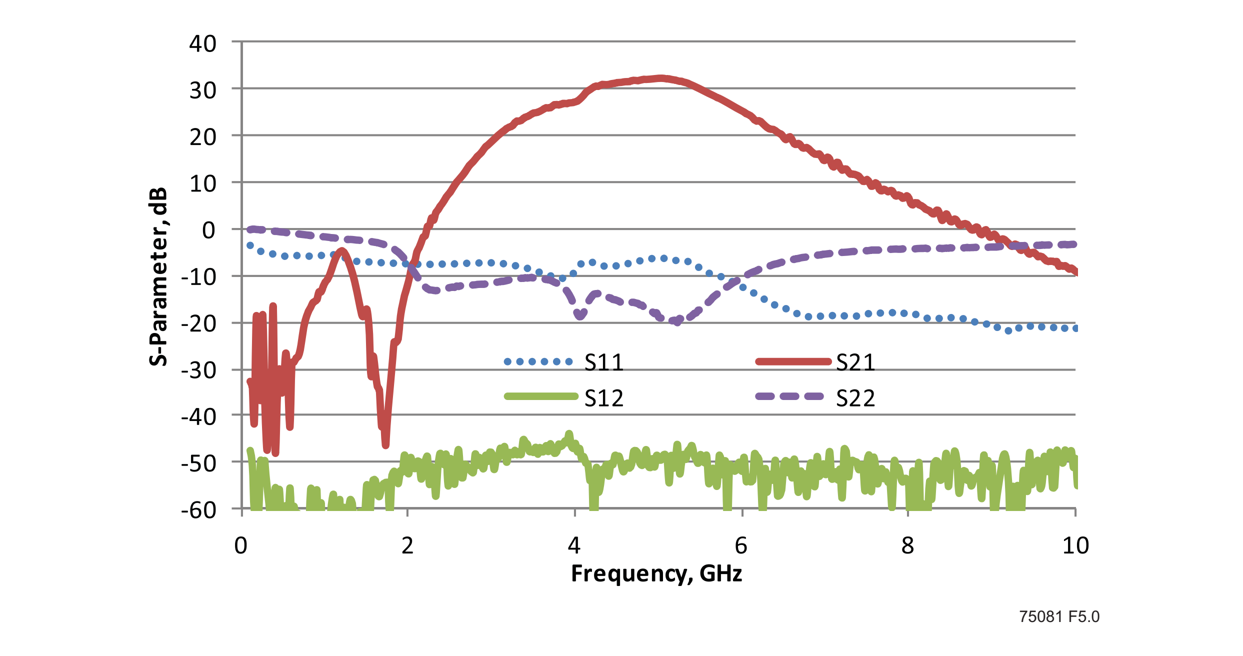


FIGURE 4-2: EVM VERSUS OUTPUT POWER, 802.11a 54 Mbps, 100% DUTY CYCLE

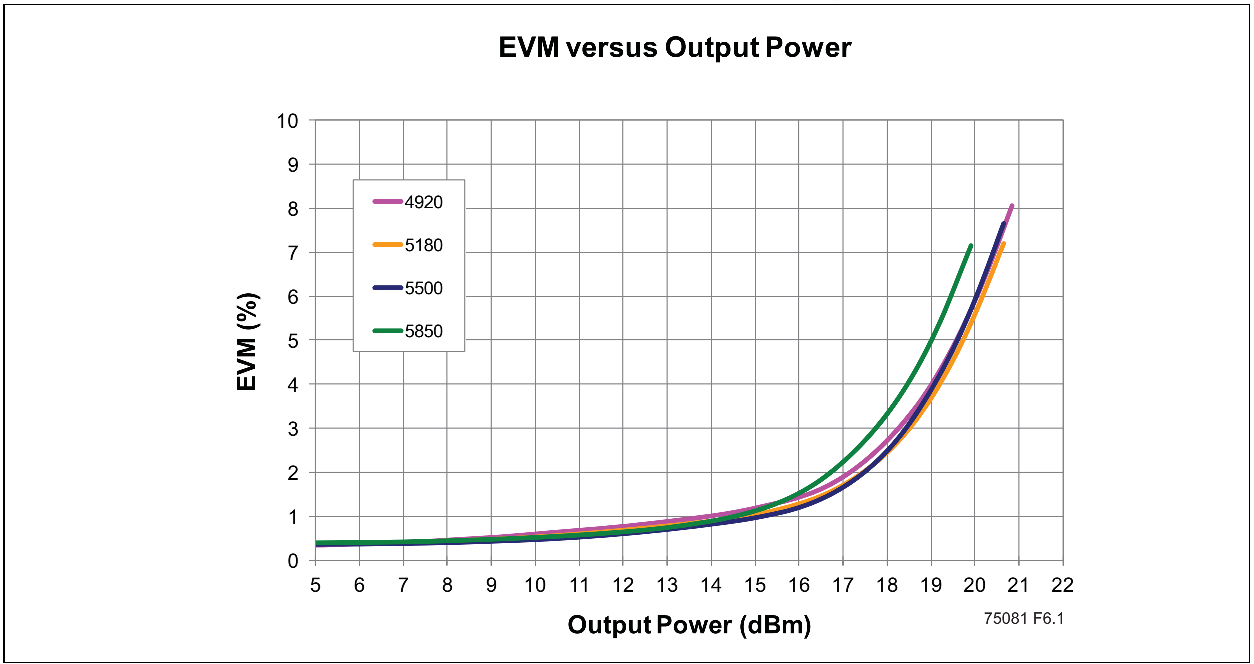


FIGURE 4-3: DYNAMIC EVM VERSUS OUTPUT POWER, 802.11ac, MCS9, 80 MHz, 60 µS PULSE, 75% DUTY CYCLE

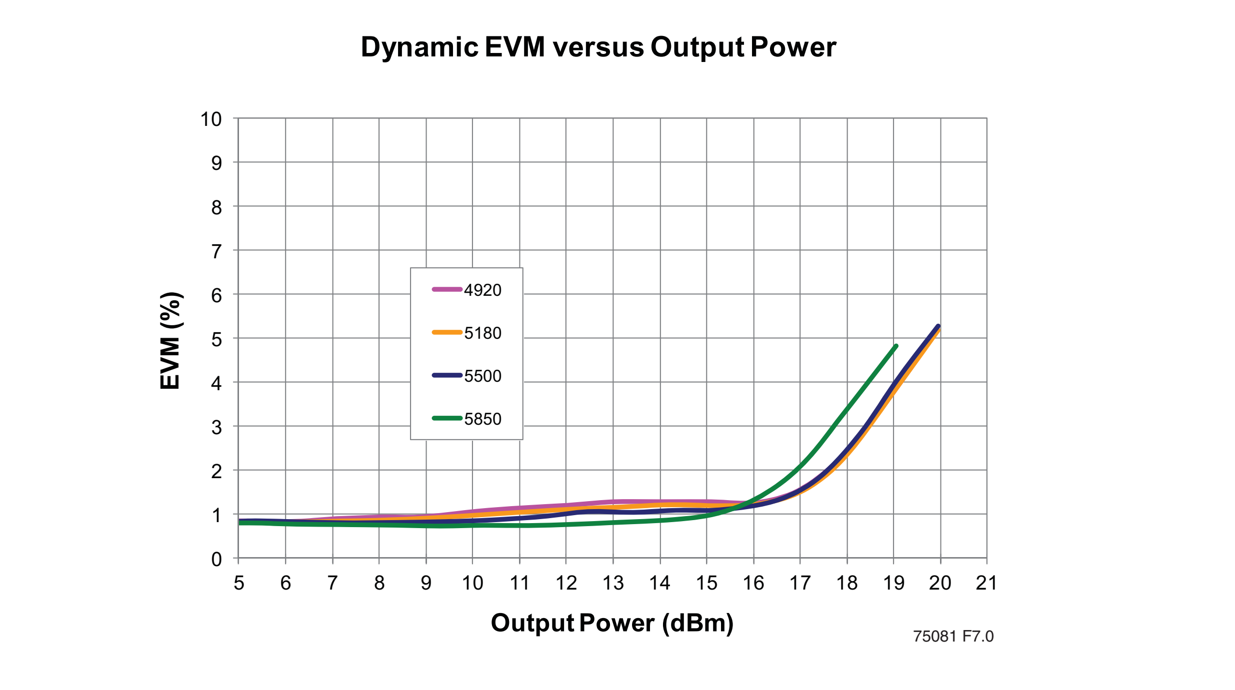


FIGURE 4-4: DC SUPPLY CURRENT VERSUS OUTPUT POWER 802.11a, 54 Mbps, 100% DUTY CYCLE

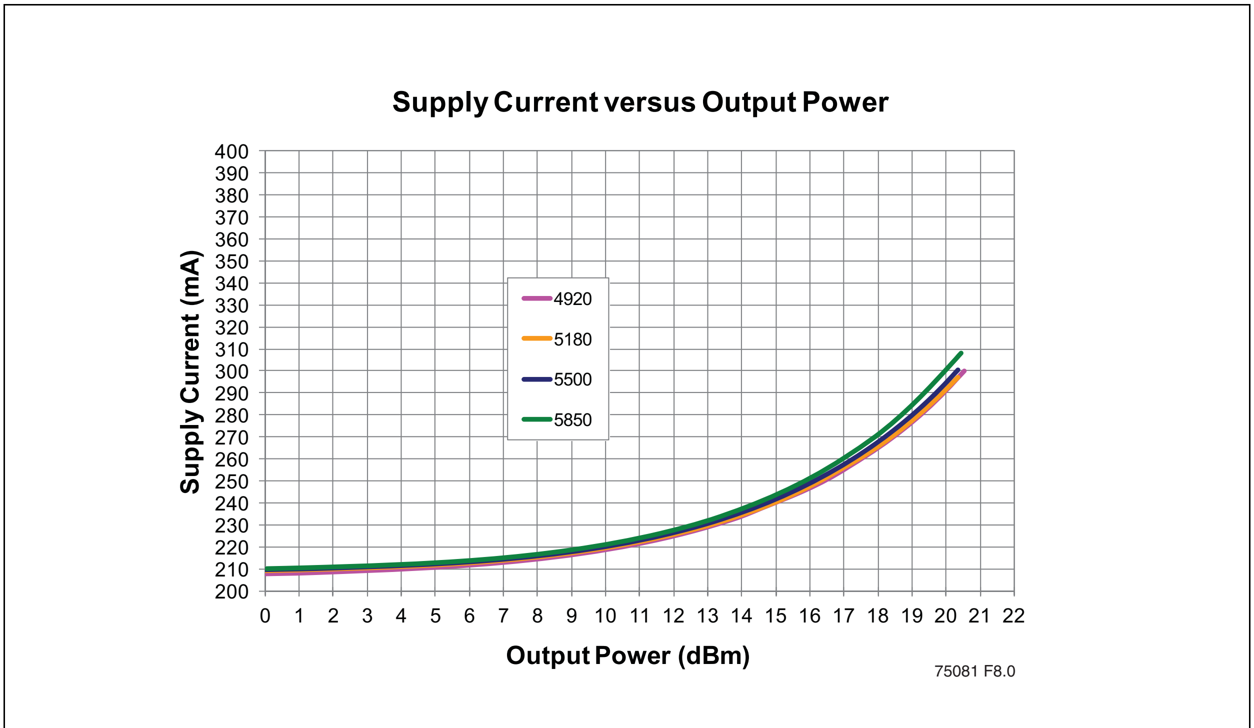


FIGURE 4-5: INSTANTANEOUS SUPPLY CURRENT VERSUS OUTPUT POWER, 802.11ac, MCS9, 80 MHz, 60 µS PULSE, 75% DUTY CYCLE

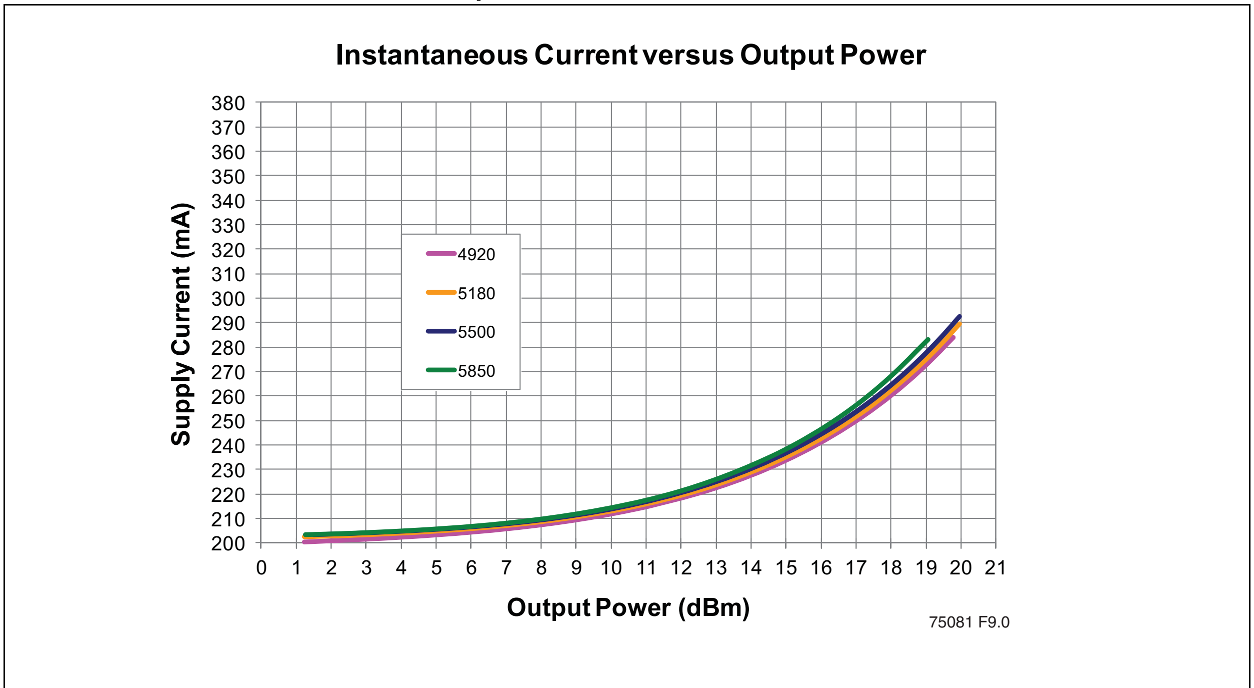


FIGURE 4-6: POWER GAIN VS OUTPUT POWER 802.11a, 54 Mbps, 100% DUTY CYCLE

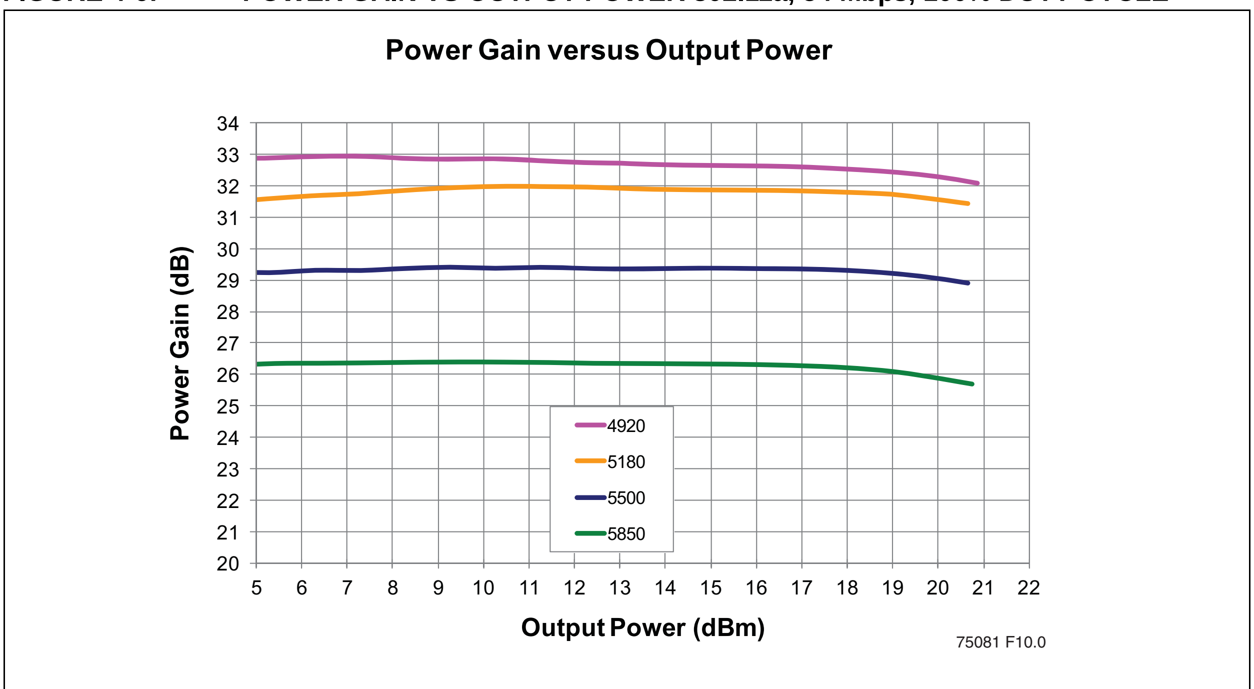
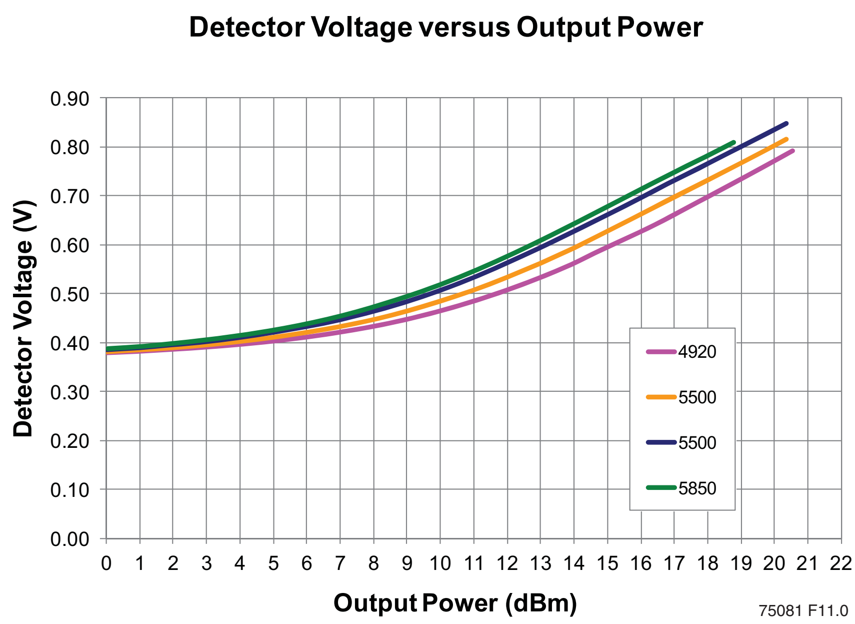


FIGURE 4-7: DETECTOR VOLTAGE VERSUS OUTPUT POWER 802.11a, 54 Mbps, 100% DUTY CYCLE



5.0 TYPICAL RECEIVER PERFORMANCE CHARACTERISTICS

Test Conditions: V_{CC} = 3.3V, T_A = 25°C, PEN = 0 LEN=3.0V CRX= 3.0V, small signal measurements unless otherwise specified

FIGURE 5-1: RECEIVER S-PARAMETER

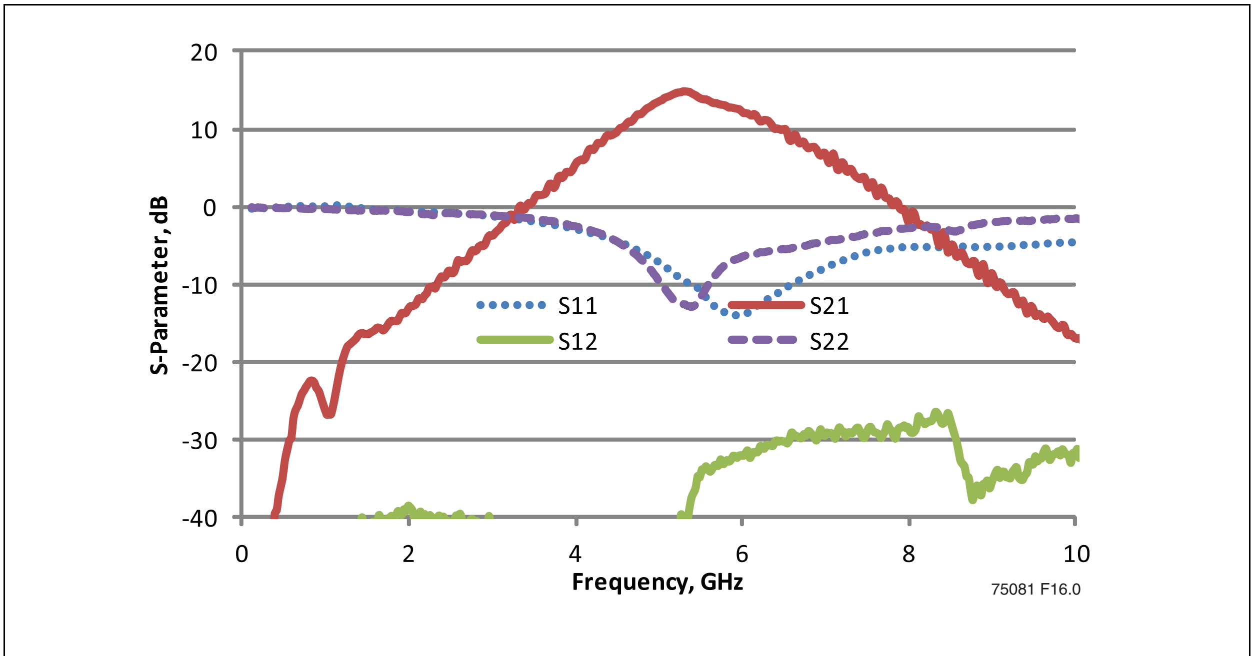
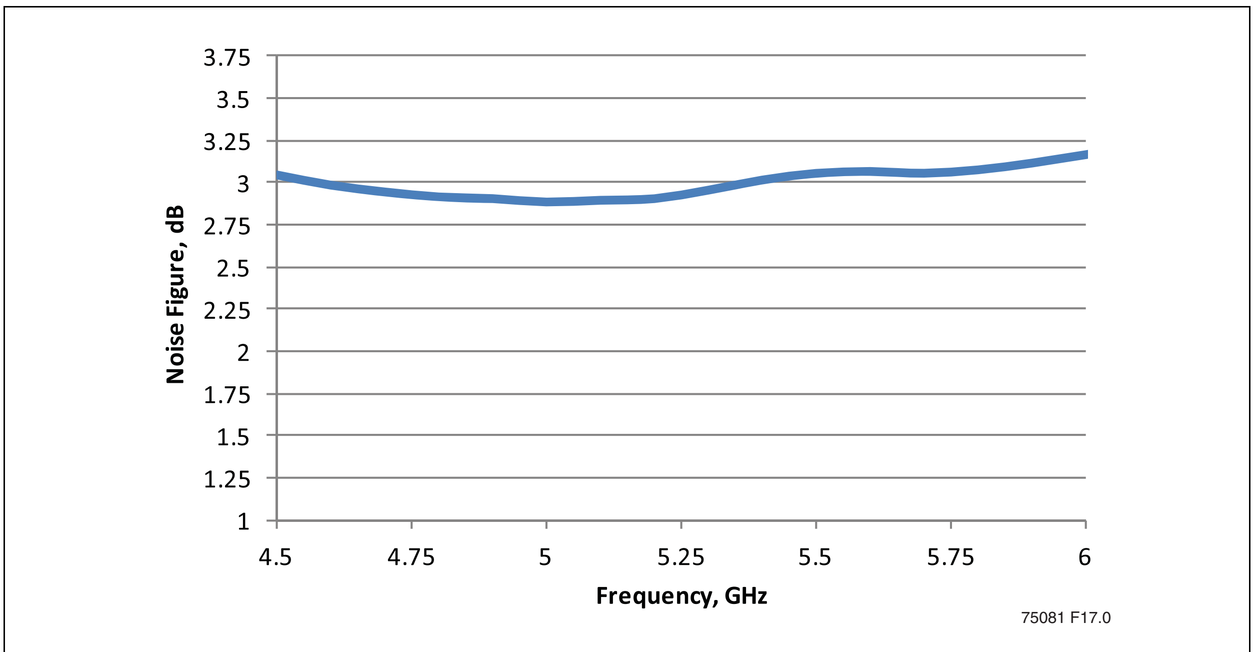
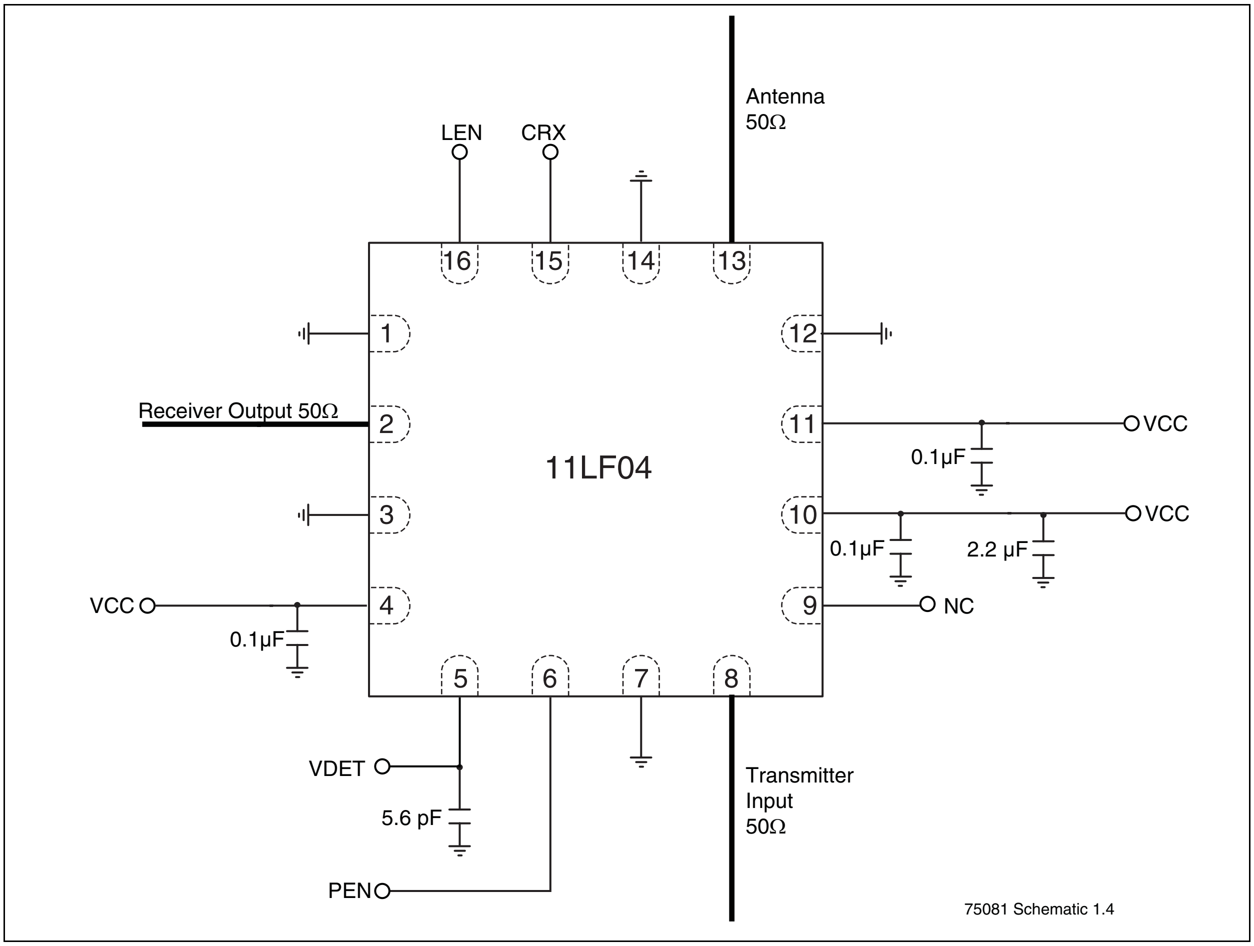


FIGURE 5-2: RECEIVER NOISE FIGURE



6.0 APPLICATION SCHEMATIC

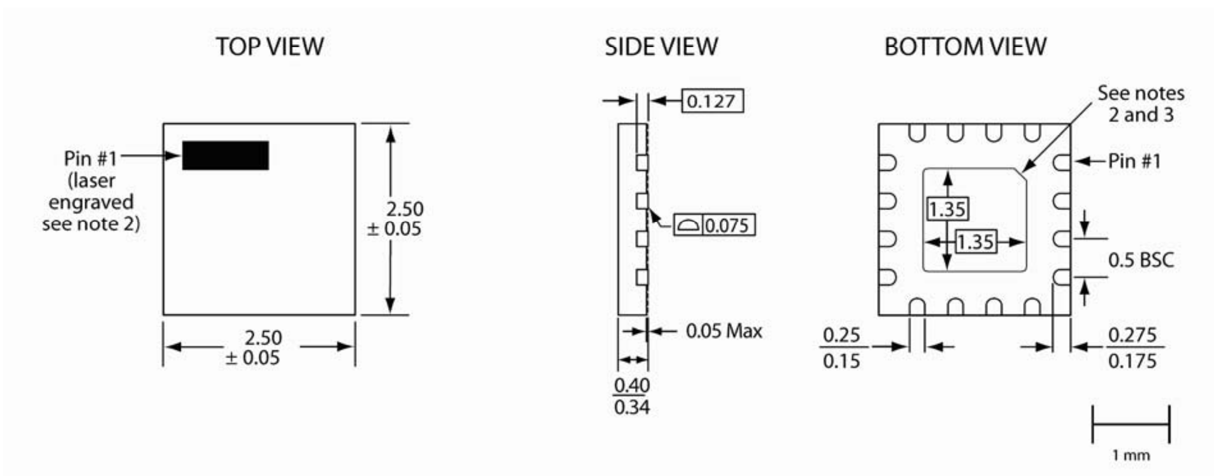
FIGURE 6-1: TYPICAL SCHEMATIC



7.0 PACKAGE INFORMATION

16-Lead Super-Thin Quad Flatpack No-Leads (Q3CE/F) - 2.5x2.5 mm Body [X2QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



16-x2qfn-2.5x2.5-Q3C-2.0

Note:

1. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
2. The topside pin #1 indicator is laser engraved; its approximate shape and location is as shown.
3. The external paddle is electrically connected to the die back-side and to VSS.
   This paddle must be soldered to the PC board; it is required to connect this paddle to the VSS of the unit.
   Connection of this paddle to any other voltage potential will result in shorts and electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

Microchip Technology Drawing C04-14017A Sheet 1 of 1

Note: The topside Pin #1 indicator can either be a circle or a bar.

TABLE 7-1: REVISION HISTORY

Revision	Description	Date
A	• Initial release of data sheet	Dec 2013
B	• Updated Figure 1-1 on page 3, Figure 2-1 on page 4, and Figure 6-1 on page 12,	Oct 2014

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PART NO.	XXX
Device	Package

Device:	SST11LF04	= 5 GHz, 802.11ac, Front-end Module
Package:	Q3CE	= X2QFN (2.5mm x 2.5mm), 0.4 max thickness 16-contact
Evaluation Kit Flag	K	= Evaluation Kit

Valid Combinations:

SST11LF04-Q3CE
SST11LF04-Q3CE-K

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