DSC2211FL2-E0018

Crystal-less™ Configurable Clock Generator

General Description

The DSC2211FL2-E0018 is a programmable, high performance dual LVCMOS output oscillator utilizing Micrel's proven silicon MEMS technology to provide excellent jitter and stability while incorporating high output frequency flexibility and drive strength control.

The DSC2211FL2-E0018 allows the user to independently modify the frequency of each output and LVCMOS drive strength using SPI interface.

The user can also select from two pre-programmed default output frequencies using the frequency select pin.

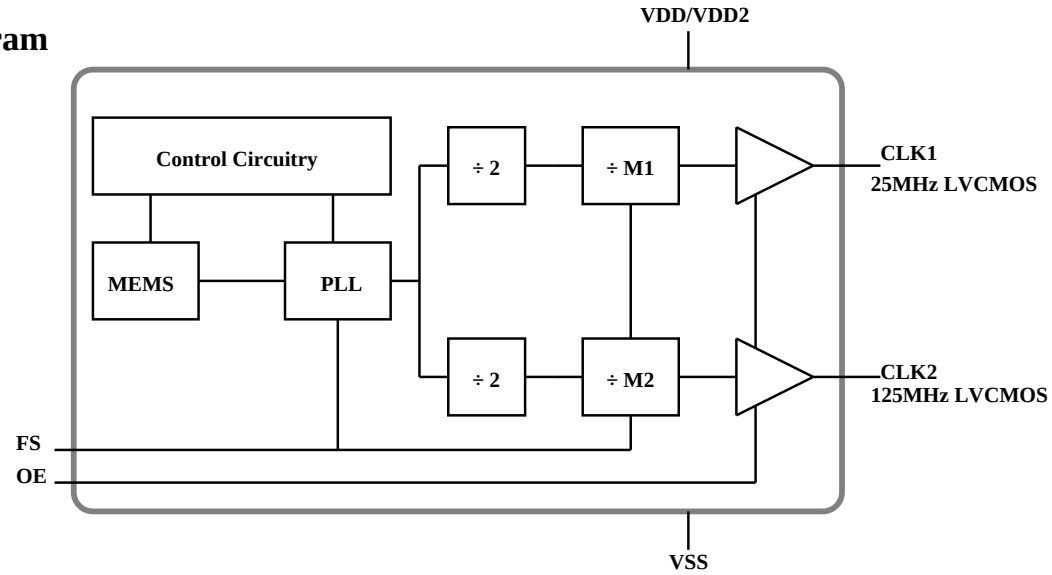
Applications

- Consumer Electronics
- Storage Area Networks
  - SATA, SAS, Fibre Channel
- Passive Optical Networks
  - EPON, 10G-EPON, GPON, 10G-GPON
- Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express
- Automotive

Features

- Frequency and output formats:
  - LVCMOS
    25/27MHz
  - LVCMOS
    125/24MHz
- Low RMS phase jitter: <1ps (typ)
- ±25ppm frequency stability
- -40°C to +105°C ext. industrial temperature range
- High supply noise rejection: -50dBc
- SPI programmable frequency and drive
- Excellent shock & vibration immunity
  - Qualified to MIL-STD-883
- High reliability
  - 20x better MTF than quartz oscillators
- Supply range of 2.25 to 3.6V
- AEC-Q100 automotive qualified
- 14-pin 3.2mm x 2.5mm QFN package

Block Diagram

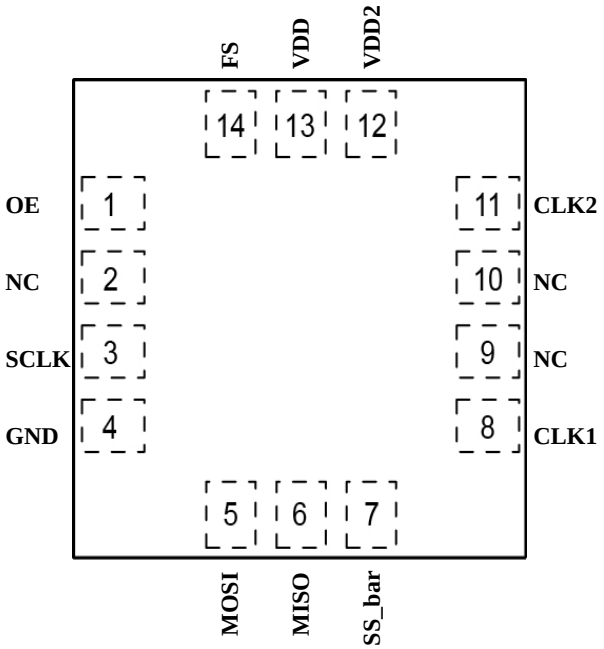


Ordering Information

Ordering Part Number	Industrial Temperature Range	Shipping	Package
DSC2211FL2-E0018	-40°C to +105°C	Tube	14-pin 3.2mm x 2.5mm QFN
DSC2211FL2-E0018T	-40°C to +105°C	Tape and Reel	14-pin 3.2mm x 2.5mm QFN

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



14-pin 3.2mm x 2.5mm QFN

Pin Description

Pin Number	Pin Name	Pin Type	Pin Function
1	OE	I	Enables outputs when high and disables outputs when low
2	NC		Leave unconnected or connect to ground
3	SCLK	I	SPI serial clock from master to slave
4	GND	PWR	Ground
5	MOSI		SPI serial data from master to slave
6	MISO	O	SPI serial data from slave to master
7	SS_bar	I	SPI slave select (active low)
8	CLK1	O	LVCMOS output
9	NC		Leave unconnected or connect to ground
10	NC		Leave unconnected or connect to ground
11	CLK2	O	LVCMOS output
12	VDD2	PWR	Power supply for LVCMOS output CLK2, 1.65V to 3.6V (VDD2 ≤ VDD)
13	VDD	PWR	Power supply
14	FS	I	Frequency select pin, see Table 2 for details

Operational Description

The DSC2211FL2-E0018 is a dual output LVCMOS oscillator consisting of a MEMS resonator and a supporting PLL IC. The two LVCMOS outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL. DSC2211FL2-E0018 allows for easy programming of theoutput frequencies using SPI interface. Upon power-up, the output frequencies are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for two different default frequency pairs. The control pin (FS) selects the initial pair. Once the device is powered up, a new output frequency pair can be programmed using SPI pins. Programming details are provided in the Programming Guide.

The DSC2211FL2-E0018 has independent control of the output voltage levels of the two outputs. The high voltage level of CLK1 is equal to the main supply voltage, VDD (pin 13). VDD2 (pin 12) sets the high voltage level of CLK2. VDD2 must be equal to or less than VDD at all times to insure proper operation. VDD2 can be as low as 1.65V. When OE (pin 1) is floated or connected to VDD, the DSC2211FL2-E0018 is in operational mode. Driving OE to ground will disable both output drivers (hi-impedance mode).

DSC2211FL2-E0018 has programmable output drive strength, which can be controlled via SPI.

Table 1 displays typical rise / fall times for the output with a 15pF load capacitance as a function of these control bits at VDD = 3.3V and room temperature.

	Output Drive Strength Bits [OXS2, OXS1, OXS0] - Default is [111] - X = 1 for CLK1, and 2 for CLK2							
	000	001	010	011	100	101	110	**111**
tr (ns)	2.1	1.7	1.6	1.4	1.3	1.3	1.2	**1.1**
tf (ns)	2.5	2.4	2.4	2	1.8	1.6	1.3	**1.3**

Table 1. Rise/Fall Times for Drive Strengths

Output Clock Frequencies

Frequency select bits are weakly tied high so if left unconnected the default setting will be [1] and the device will output the associated frequency highlighted in bold.

Freq (MHz)	**Freq Select Bit [FS] - Default is [1]**	
	0	**1**
CLK1	27	**25**
CLK2	24	**125**

Table 2. Pin-Selectable Output Frequencies

Absolute Maximum Ratings

Item	**Min.**	**Max.**	**Units**	**Condition**
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	VDD + 0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

1000+ years of data retention on internal memory

Specifications (Unless specified otherwise: T = 25°C, max LVCMOS drive strength)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage[1]	VDD		2.25		3.6	V
Supply Voltage (CLK2)[1]	VDD2		1.65		3.6	V
Supply Current	IDD	OE pin low - outputs are disabled		21	23	mA
Supply Current[2]	IDD	OE pin high - outputs are enabled CL = 15pF, F01 = F02 = 125MHz		32		mA
Frequency Stability	△F	Includes frequency variation due to initial tolerance, temp. and power supply voltage			±25	ppm
Aging	△F	First year (@ 25°C)			±5	ppm
Startup Time[3]	tSU	T = 25°C			5	ms
Input Logic Levels Input Logic High Input Logic Low	 VIH VIL		 0.75 x VDD -		 - 0.25 x VDD	 V
Output Disable Time[4]	tDA				5	ns
Output Enable Time	tEN				20	ns
Pull-Up Resistor[2]		Pull-up exists on all digital IO		40		kOhms
LVCMOS Outputs						
Output Logic Levels Output Logic High Output Logic Low	 VOH VOL	I = ±6mA	 0.9 x VDD -		 - 0.1 x VDD	V
Output Transition Time[4] Rise Time Fall Time	 tR tF	 20% to 80% CL = 15pF		 1.1 1.4	 2 2	 ns
Frequency	CLK1 CLK2	[FS] = [1]		25 125		MHz
Output Duty Cycle	SYM		45		55	%
Period Jitter[5]	JPER	F01 = F02 = 125MHz		3		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz		0.3 0.38 1.7	 2	psRMS

Notes:

1. Pin 12 VDD2, and pin 13 VDD should be filtered with 0.1uF capacitors.
2. Output is enabled if OE pin is floated or not connected.
3. tSU is time to 100ppm stable output frequency after VDD is applied and outputs are enabled.
4. Output Waveform and Test Circuit figures below define the parameters.
5. Period Jitter includes crosstalk from adjacent output.

Nominal Performance Parameters (Unless specified otherwise: T = 25°C, VDD = 3.3V)

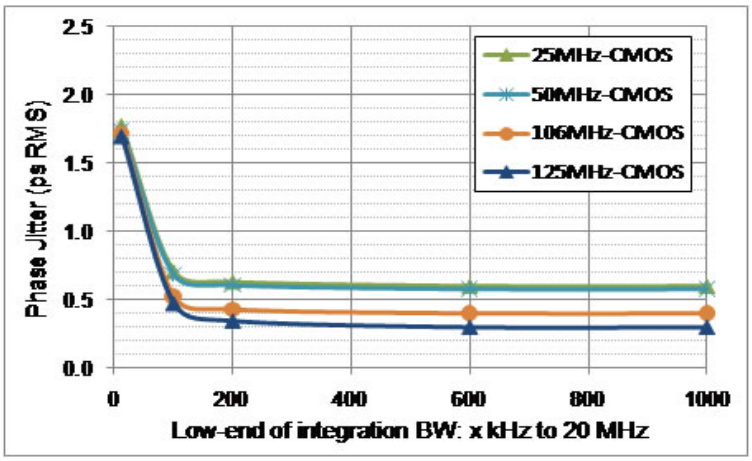


Figure 1. LVCMOS Phase Jitter (integrated phase noise)

LVCMOS Output Waveform

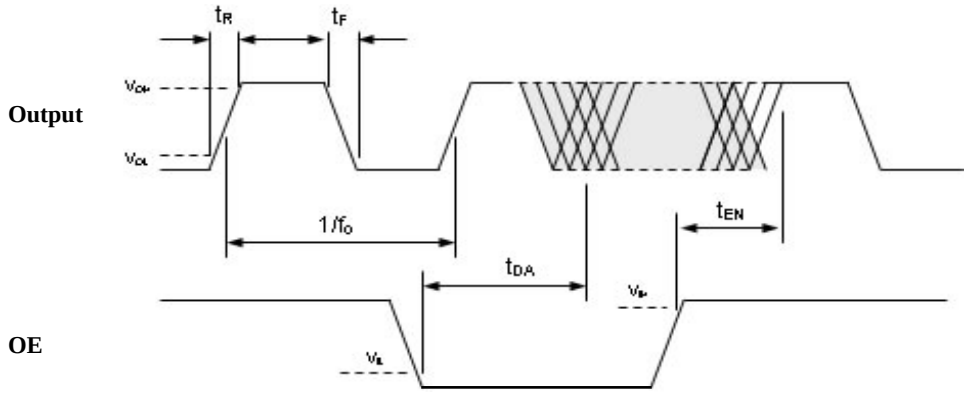


Figure 2. LVCMOS Output Waveform

MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec Max.
Preheat Time 150°C to 200°C	60 - 180 sec
Time maintained above 217°C	60 - 150 sec
Peak Temperature	255 - 260°C
Time within 5°C of actual Peak	20 - 40 sec
Ramp-Down Rate	6°C/sec Max.
Time 25°C to Peak Temperature	8 min Max.

Solder Reflow Profile

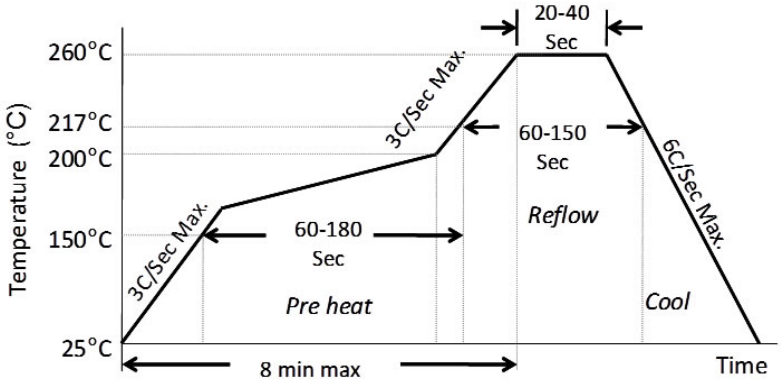
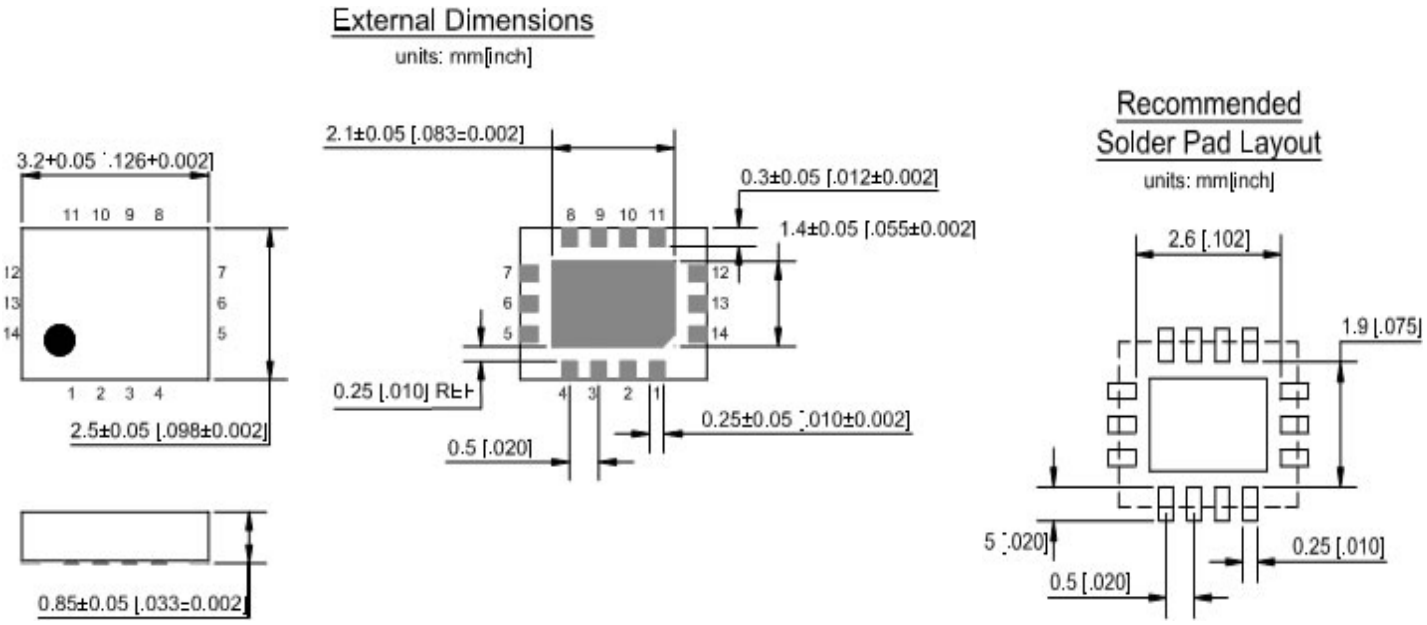


Figure 3. Solder Reflow Profile

Package Information[7]



3.2mm x 2.5mm 14 Lead Plastic Package

Notes:

6. Connect the exposed die paddle to ground.
7. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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Microchip:

DSC2211FL2-E0018T DSC2211FL2-E0018