Le9662
Dual Subscriber Line Interface Circuit
miSLIC™ Series
Data Sheet

Document ID# 146852 Version 4 February 2015

Features

- **Economical, fifth-generation line interface solution for VoIP processors and SoCs**
- **Dual Channel Architecture**
- **Single port 4-wire interface control (ZSI)**
  - Compatible with numerous VoIP processors and SoC solutions
  - Less expensive isolation than multi-port control
  - Simplifies board routing
- **VoicePath SDK and VP-API-II Software available to implement FXS functions**
- **VeriVoice Professional Test Suite Software**
  - Comprehensive subscriber loop testing, including *Telcordia GR-909-CORE / TIA-1063* diagnostic testing
  - Industry leading advanced test software
- **VeriVoice Manufacturing Test Package (VVMT)**
  - Facilitates factory testing and calibration of assembled boards
- **Low cost, Energy Efficient Shared Switching Regulator Architectures**
  - Dual Output power supplies
  - Integrated battery switches
  - Up to 70 V_{RMS} open circuit ringing with 5 REN load
- **Low cost, 2-Layer PCB Reference Designs**
- **Complete Wideband BORSCHT functionality**
- **Worldwide Programmability**
- **Per channel Narrowband or Wideband operation**

Applications

- **DSL Residential Gateways and Integrated Access Devices (IADs)**
- **Cable Embedded Multimedia Terminal Adapters (eMTAs)**
- **PON Single Family Units (SFU)**
- **Fiber-to-the-premise (FTTX) solutions**

Ordering1 Information

Device OPN	Device Type	Package	Packing
Le9662WQCT	SLIC, BBABS/FBABS	56-pin QFN	Tape&Reel
Le9662WQC	SLIC, BBABS/FBABS	56-pin QFN	Tray

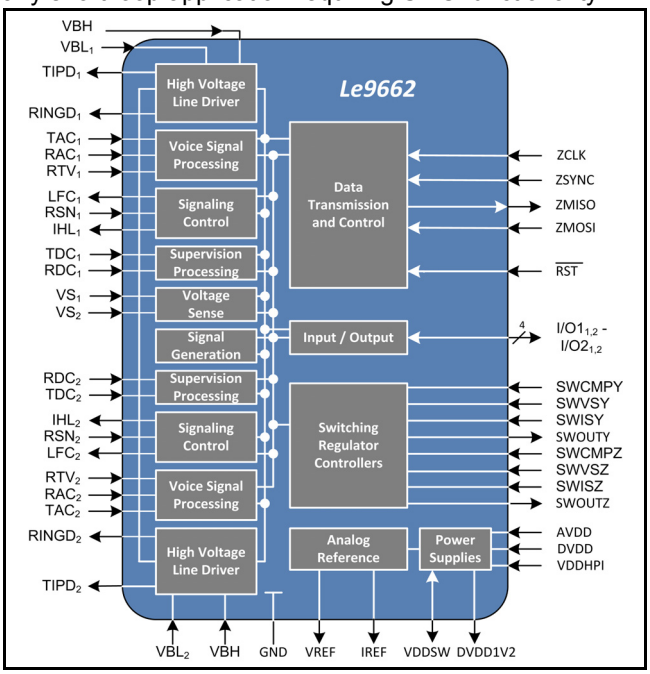
These Green packages meet RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

Description

The miSLIC™ Line Circuits together with a VoIP processor or SoC, provides an economical turn-key solution for derived voice applications. The miSLIC devices are controlled by a VoIP processor or SoC through a simple, single serial interface.

The dual channel Le9662 miSLIC device uses energy efficient shared power supply topologies for reduced BOM cost. The Le9662 can be configured for patent-pending shared Buck-Boost Automatic Battery Switching (BBABS) or for shared Flyback ABS (FBABS) operation. Ringing and system power management are supported to limit the peak power requirements of each telephone line FXS port. The dual channel Le9662 features wideband clarity and complete BORSCHT functionality.

Manufacturing self test and subscriber line diagnostics are available features. All AC, DC, and power parameters are programmable making the Le9662 device suitable for any short loop application requiring SLIC functionality.



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1.0 miSLIC™ Series Solution Overview

The fifth-generation *miSLIC* line interface solution consists of *a miSLIC* device, *VoicePath API-II (VP-API-II)* Software, and *Profiles* Data Structures. To support the *miSLIC* device, Microsemi offers comprehensive software and hardware collateral packages, including 2-layer printed circuit board reference designs.

The *VoicePath API-II (VP-API-II)* software initializes each FXS port coefficient data containing application or country-specific AC and DC parameters, ringing and other signaling characteristics, and configures the switching power supply. *VP-API-II* resides on the customer's VoIP processor or SoC and provides high-level control over the telephony functions. *VP-API-II* offers a seamless migration between products utilizing its common software architecture and interfaces with the Microsemi *VeriVoice Professional Test Suite Software*.

A *Microsoft*® *Windows*® GUI (Graphical User Interface) application, *VoicePath Profile Wizard (VP Profile Wizard)*, allows the user to select the operating parameters of the FXS channels and to automatically generate the sets of data structures, called *Profiles*, that are required by the *VP-API-II* for integration with the VoIP host software.

1.1 Le9662 Shared Battery miSLIC Device

The Le9662 miSLIC device implements a dual channel, universal telephone line interface with a ZSI serial digital interface. All AC, DC, and signaling parameters are fully programmable via the ZSI interface.

The Le9662 features integrated switching controllers that drive external components to generate the high voltages necessary for efficiently powering and ringing analog telephones. The high performance architecture permits high efficiency in all operating states and corresponding low power consumption. The switching regulator circuit can be configured for shared Flyback Automatic Battery Switching (FBABS) or the patent-pending shared inverting Buck-Boost Automatic Battery Switching (BBABS). FBABS operation supports high voltage ringing and large ringing loads while requiring a minimal number of external components. BBABS provides similar performance but with lower ringing voltages and extremely low cost components. Refer to "Switching Regulator Controllers" on page 21 for more information on the circuits.

The Le9662 utilizes the *VeriVoice Professional Test Suite Software* to resolve line circuit faults and to provide line diagnostics. The integrated digital access to line information such as AC and DC line voltages and Metallic or Longitudinal currents is crucial for remote applications where dedicated test hardware is not cost effective.

Additionally, the *VeriVoice Manufacturing Software (VVMT)* package provides test functions intended to facilitate factory testing, eliminating the need for expensive external test equipment.

Figure 2 shows a high-level solution diagram with a *Le9662* device, *VP-API-II* and *Profiles*.

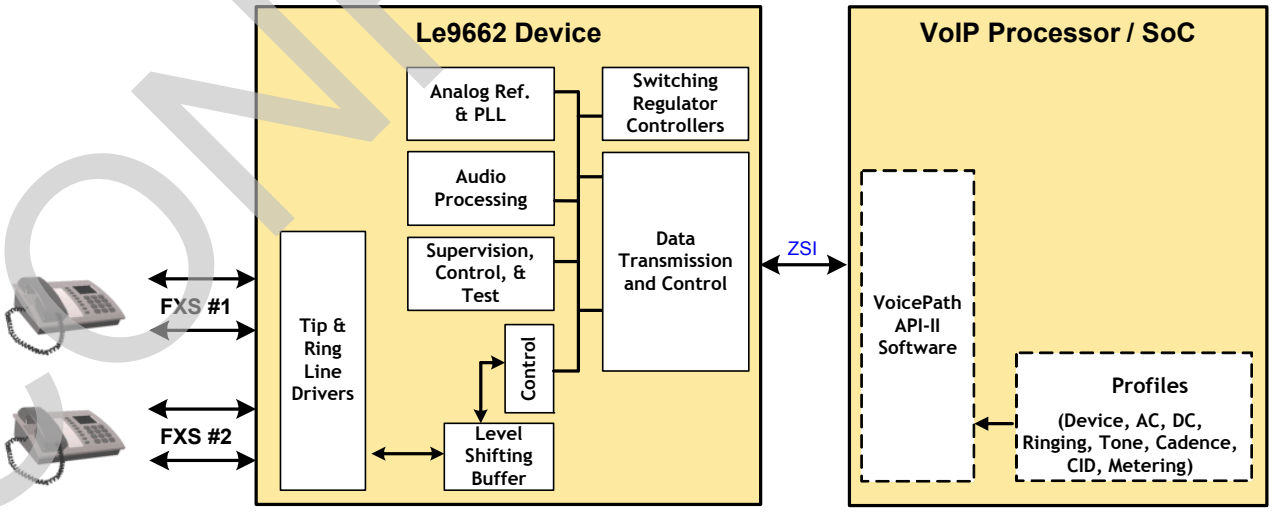


Figure 2 - Le9662 Dual Channel Solution Diagram

2.0 Le9662 Shared Battery miSLIC™ Device Overview and Block Diagram

Le9662 features:

- Performs all Battery feed, Ringing, Signaling, Coding, Hybrid and Test (BORSCHT) functions
- Single chip solution provides high voltage line driving, digital signal processing, and high voltage power generation for two lines
- Wideband 150 Hz – 6.8 kHz and Narrowband 200 Hz – 3.4 kHz codec modes
  - Compliant with Cable Labs *PacketCable High Definition Voice Specification PKT-SP-HDV-104-120823*
- Exceeds *Telcordia® GR-909-CORE* transmission requirements
- Single hardware design meets worldwide requirements through software programming of:
  - Ringing waveform, frequency and amplitude
  - DC loop-feed characteristics and current limit
  - Loop-supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and ring trip filters
  - Two-wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains and equalization
  - Digital I/O pins
  - A-law/µ-law and linear coding selection
  - Switching power supply
- Supports loop-start and ground-start signaling
- On-hook transmission
- Power/service denial mode
- Smooth polarity reversal
- Supports wink function
- Metering generation with envelope shaping
  - Programmable frequency and duration
- Internal Test Termination
- Compatible with inexpensive protection networks
- Self-contained ringing generation and control
  - Programmable ringing cadencing
  - Internal battery-backed balanced sinusoidal or trapezoidal
  - Integrated ring trip filter and software, manual or automatic ring trip mode
- Flexible tone generation
  - Call progress tone generation
  - DTMF tone generation
  - Universal Caller ID generation (FSK and DTMF signaling)
  - Howler tone generation with *VP-API-II*
- Integrated switching regulator controller
  - Generates batteries for each line
  - Energy efficient in all states
  - Low idle-power per line
  - Line-feed characteristics independent of battery voltage
- *VeriVoice Professional Test Suite Software*
  - Monitors two-wire interface voltages and currents for subscriber line diagnostics
  - Integrated self-test features
- *VeriVoice Manufacturing Test Package*
- Supported by *VoicePath SDK* and *VP-API-II*
- Monitors and drives Tip & Ring independently
- Built-in voice-path test modes
- Small physical size in 8x8 mm, 56-pin QFN
- -40°C to +85°C operation
- Low-Power Idle Mode (LPIM)
  - Voltage-based off-hook detection
- Supervision ADC for advanced testing
  - Monitors up to 5 signals in multiplexed mode, such as V_{TIP}, V_{RING}, I_M, I_L, & VBAT
  - Two pins for sensing external voltages ranging from -180 V to +60 V
- Simultaneous ground key / DC fault detection
- Over current monitoring and blanking
- Hook and ground key detection with hysteresis and calibrated thresholds
- On-chip timer functions
- Tone generators with frequency modulation capability for compliance with *BT*, *NTT*, and *Austel* special Howler tone requirements
- ZSI Interface requires fewer serial interface signals to the host
  - Less expensive system isolation cost
  - Supports communication with host processors at 1.8 V, 2.5 V or 3.3 V

- Low BOM cost:
  - Compatible with 2-layer PCB designs
  - Direct FET driver (FBABS)
  - Small value/size/cost switcher output and SLIC capacitors
  - No external diodes for protecting SLIC against positive surges
- Comprehensive device calibration capabilities
  - Short calibration time
  - No need to generate voltages to the Tip/Ring interface
  - Longitudinal operating point calibration
  - Programmable loop current dependent overhead

2.1 Le9662 Device Block Diagram

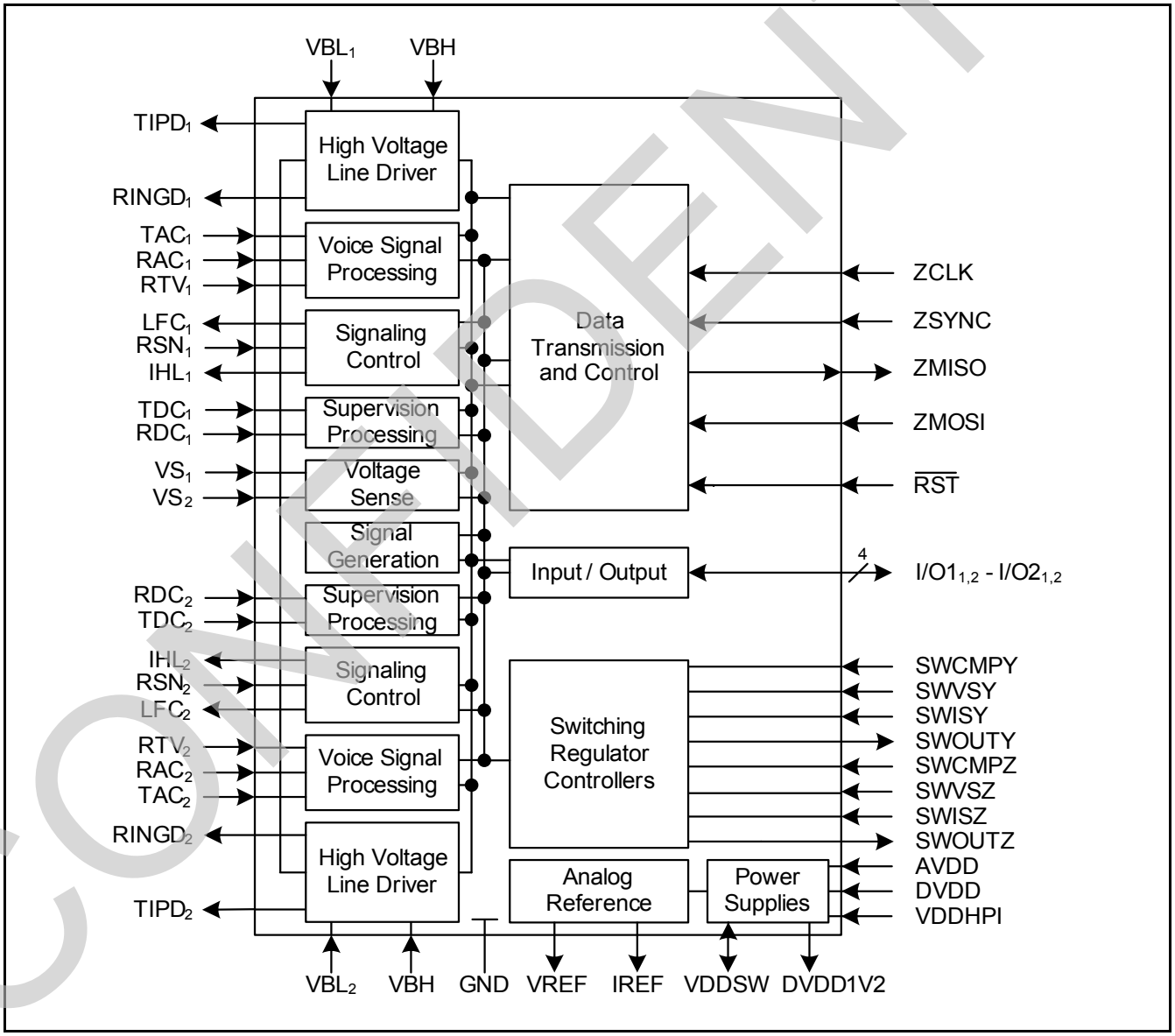


Figure 3 - Le9662 Device Block Diagram

3.0 Functional Description

3.1 Host Port Interface

The Le9662 device features a host port interface for communicating with VoIP processors and SoCs using the ZSI interface.

The host interface is supported by a 4-wire interface called ZSI (see Figure 4.) The ZSI interface must be supported by the host processor or by a PCM/SPI to ZSI bus translator device such as the Le88004.

This interface supports separate PCM and control channels based on the level of the ZCLK. For receive signals (ZSYNC, ZMOSI) PCM data is valid when ZCLK is high and control data is valid when ZCLK is low. For the transmit ZMISO, PCM data is valid when ZCLK is low and control data valid when ZCLK is high. The control data is framed byte by byte in a similar way to the separate MPI interface on the VoicePort family of products. Chip select status is carried on the ZSYNC signal and requires a chip select off time of at least one clock period. Interrupt status (INT) is communicated on the ZMISO control channel whenever the previous ZSYNC CS status is low. This is achieved by XORing the DX data with the active high INT status.

The ZCLK rate can be 1.024 MHz, 1.536 MHz, 2.048 MHz, 3.072 MHz, 4.096 MHz, 6.144 MHz, or 8.192 MHz. The Le9662 must be programmed to match the applied ZCLK frequency. Both PCM and control data are transferred at the same ZCLK rate over the ZSI.

3.1.1 ZSI Timing

Figure 4 shows the protocol for multiplexing PCM and control signals onto the ZSI.

Note that chip select must be de-asserted at least one clock between bytes or a reset will be generated after 16 clocks.

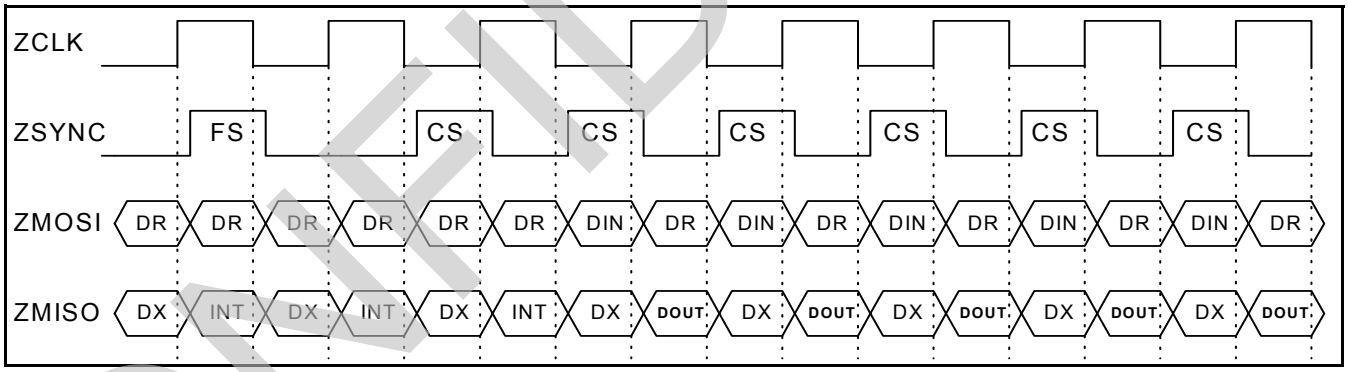


Figure 4 - ZSI Timing Protocol

3.2 ZSI Header

The ZSI port consists of the ZSYNC, ZMISO, ZMOSI, and ZCLK pins. Microsemi can provide a ZSI Snooper board that can demux and provide access to the ZSI interface. If access to this port is desired, a header footprint should be added to the system board.

Figure 5 shows the pinout for the ZSI header. For normal operation the 0 ohm resistors short the header. If the header is to be used, the 0 ohm resistors must be removed and replaced with the header.

Figure 6 depicts the ZSI header land pattern that needs to be added to the circuit board. The land pattern is designed for a Samtec FTSH-105-01-L-DV-K vertical 10-position, surface mount micro header. The 10-pin header mating pins are spaced 1.27 mm row to row and 1.27 mm column to column. Four 0 ohm resistors are shown

shorting the header. A 0402 inch / 1005 mm resistor will fit between the surface mount land pattern pads as illustrated in Figure 6.

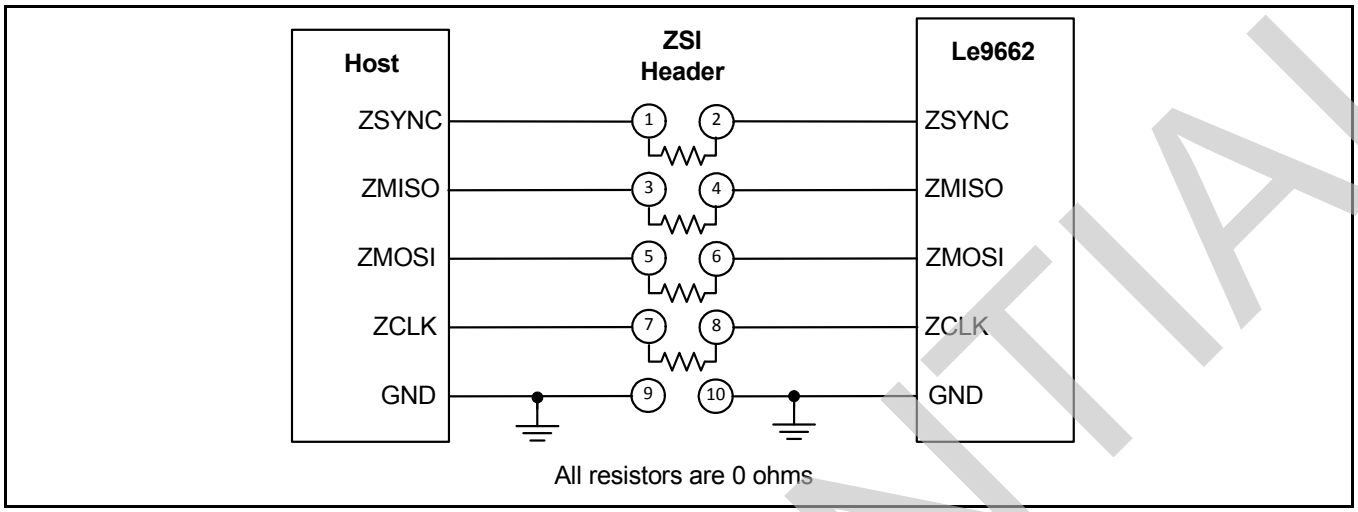


Figure 5 - ZSI Header

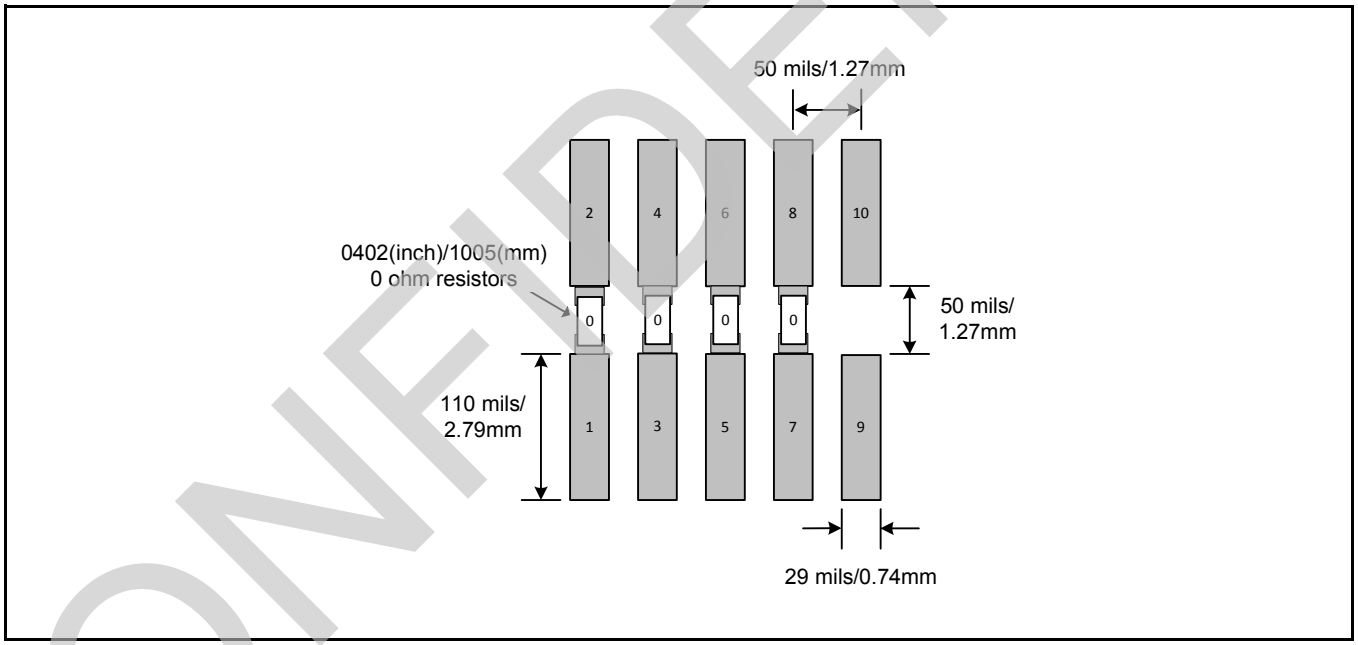


Figure 6 - ZSI Header Land Pattern with 0 Ohm Resistors

3.3 Input / Output Block

The Le9662 device features two dedicated and two optional general purpose input / output (I/O) pins. $I/O1_1$ and $I/O1_2$ can be configured by the user as inputs, outputs, or as high-current LED or relay drivers. $I/O2_1$ and $I/O2_2$ may be configured as general purpose digital inputs or outputs or as voltage sense pins (VS1 and VS2). When configured as inputs, $I/O2_1$ and $I/O2_2$ are capable of generating interrupts.

3.4 Voltage Sense

The voltage sense block allows the measurement of analog voltages at the pins VS1 and VS2, when they are configured as analog inputs. This makes it possible to monitor VSW and VBAT in real time and make switcher optimizations based on their levels and to measure power consumption. An external 1.0-MΩ, 1% resistor needs to be connected between each of these pins and the voltages to be measured.

3.5 Voice Signal Processor

This block, shown in Figure 7, performs digital signal processing for the transmission and reception of voice. It includes *G.711* compression/decompression, impedance matching, filtering, gain scaling, DTMF generation and general-purpose tone generators for each channel. Additionally Caller ID (FSK and DTMF) and metering generation are provided.

This block performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function
- Permits adjustment of the two-wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

Country-specific and standards-specific *Profiles* are available from Microsemi with pre-computed digital filter coefficients.

The Le9662 device is architected in such a way as to reduce the real time demands on the host processor. An integrated cadencer/sequencer controls ringing and call progress tone generation. This feature can also generate timed interrupts and substantially reduces the user's need to implement time critical functions.

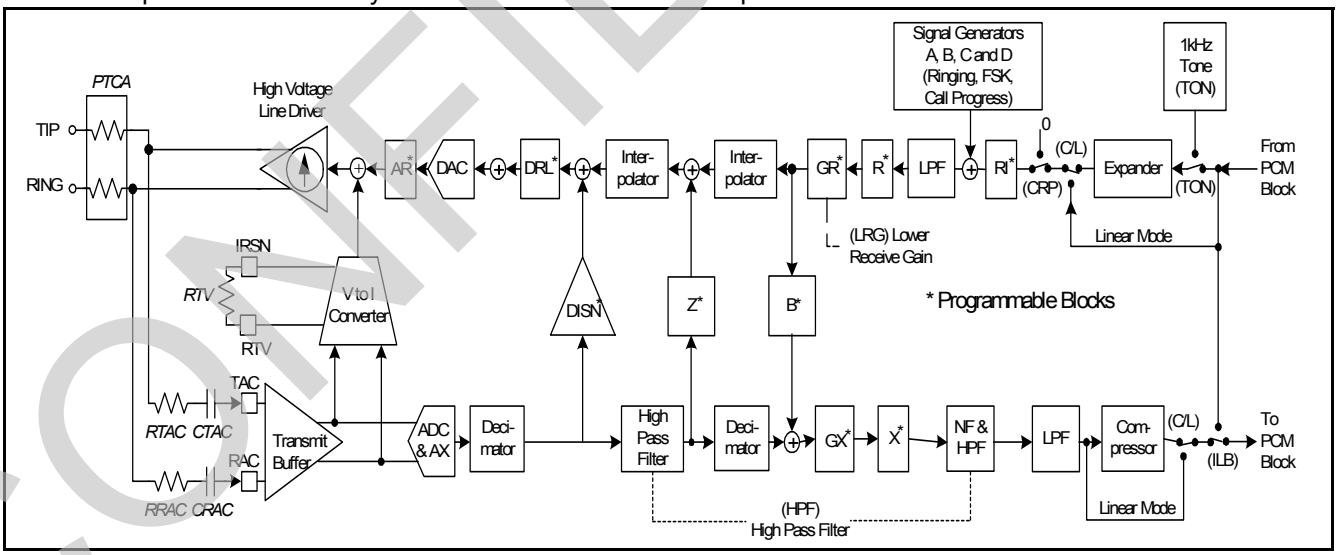


Figure 7 - Voice Signal Processing Block Diagram

3.5.1 Impedance Synthesis

The analog impedance synthesis loop is comprised of the SLIC block, the AC sense path components, the transmit amplifier, and a voltage to current converter. An external resistor, R_{TV}, synthesizes the nominal impedance in the analog domain. Additional refinement of the impedance is done in the DSP via the Digital Impedance Scaling Network (DISN) and Z-blocks.

The DISN path is comprised of the voice A/D and its first stage of decimation, a DISN, and the voice DAC. The 8-bit DISN synthesizes a portion of the AC impedance which appears in parallel with R_{TV} and is used to modify the impedance set by the external analog network.

The Z Filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. Together R_{TV}, DISN, and the Z Filter enable the user to synthesize virtually all required telephony device input impedances.

3.5.2 Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z Filter.

3.5.3 Transhybrid Balancing

The voice signal processor's programmable B Filter is used to adjust transhybrid balance. The filter has a single pole Infinite Impulse Response (IIR) section and an eight-tap Finite Impulse Response (FIR) section, both operating at 16 kHz.

3.5.4 Gain Adjustment

The transmit path of the FXS has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. The receive voice path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB. DRL is a digital loss block of 0 dB or 6.02 dB. AR is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. This provides an attenuation in the range of 0 dB to 18 dB.

The gain adjustment block can also be accessed by a *VP-API-II* function directly, without using an *AC FXS Profile*.

Function Name	Description
`VpSetRelGain()`	Adjusts transmit and/or receive gain up to +/-6 dB. Relative gain of 1 (0 dB) defined as initial value programmed by *AC FXS Profile*. Note that the supplied *AC FXS Profiles* have initial gains of -6 dBr receive and 0 dBr transmit
`VpSetOption()`	`VP_OPTION_ID_ABS_GAIN` -- Programs absolute gain

Table 1 - VP-API-II Functions for Gain Adjustment

3.5.5 Transmit Signal Processing

In the transmit path (A/D) of the FXS, the AC Tip - Ring analog input signal is sensed by the TAC and RAC pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for A-law or μ-law), and made available to the PCM blocks. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections. The first high-pass filter is for DC rejection, and the second high pass and notch filters reject low frequencies such as 50 Hz or 60 Hz.

3.5.6 Receive Signal Processing

In the receive path (D/A) of the FXS port, the digital signal is expanded (for A-law or µ-law), filtered, interpolated, converted to analog, and driven onto TIP and RING by the SLIC block. The AR, DRL, DISN, Z, R, and GR blocks are user-programmable filter sections.

3.5.7 Speech Coding

The A/D and D/A conversion follows either the A-law or the µ-law standard as defined in *ITU-T Recommendation G.711.* Alternate bit inversion is performed as part of the A-law coding. Linear code is an option on both the transmit and receive sides of the device. Two successive time slots are used for linear code operation. The linear code is a 16-bit two's-complement number with sign bit first.

3.5.8 Wideband Operation

Each channel on the Le9662 device can be set to operate in either Narrowband or Wideband mode under *VP-API-II* software control. In the Wideband mode, the nominal voice bandwidth is expanded to provide better voice quality. The 50/60 Hz notch filter can be disabled to support the full wideband range of 150 Hz to 6800 Hz. The *AC FXS Profiles* must be programmed with wideband coefficients. In the Wideband mode, the increased data rate is processed by accessing a second set of timeslots equally spaced in the frame.

Function Name	Description
`VpSetOption()`	`VP_OPTION_ID_TIMESLOT` -- Programs transmit and receive timeslot. `VP_OPTION_ID_CODEC` -- Programs speech coding mode.
`VpGetOption()`	`VP_OPTION_ID_TIMESLOT` -- Retrieves current values of transmit and receive timeslot. `VP_OPTION_ID_CODEC` -- Retrieves current speech coding mode.

Table 2 - VP-API-II Functions for Speech Coding

3.6 Signal Generation

Up to four programmable digital signal generators are available for the FXS channel. These signal generators can be programmed for multi-tone generation, amplitude and frequency modulation, and or the generation of complex sine, triangular or trapezoidal signals.

3.6.1 Multi-Tone Generation

In this configuration, up to four tone generators are summed into the output path, as shown in Figure 8. The Bias generator produces a DC bias that can be used to provide DC offset during ringing or DC test signals during diagnostics. This generator is automatically enabled when entering the `VP_LINE_RINGING` state.

Function Name	Description
`VpSetLineTone()`	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually to provide Special Indication Tone (SIT).
`VpSetLineState()`	`VP_LINE_RINGING` and `VP_LINE_RINGING_POLREV` -- Uses Signal Generator A (and B for trapezoidal type ringing) with user selected frequency, offset, amplitude, and type.
`VpSendSignal()`	`VP_SENDSIG_DTMF_DIGIT` -- Generates a DTMF digit on the line.
`VpInitCid()`	Sending Caller ID (FSK and DTMF message data supported) on an FXS line. Providing Type 2 CID Alerting tone.
`VpSendCid()`	
`VpContinueCid()`	

Table 3 - VP-API-II Functions Using Signal Generators

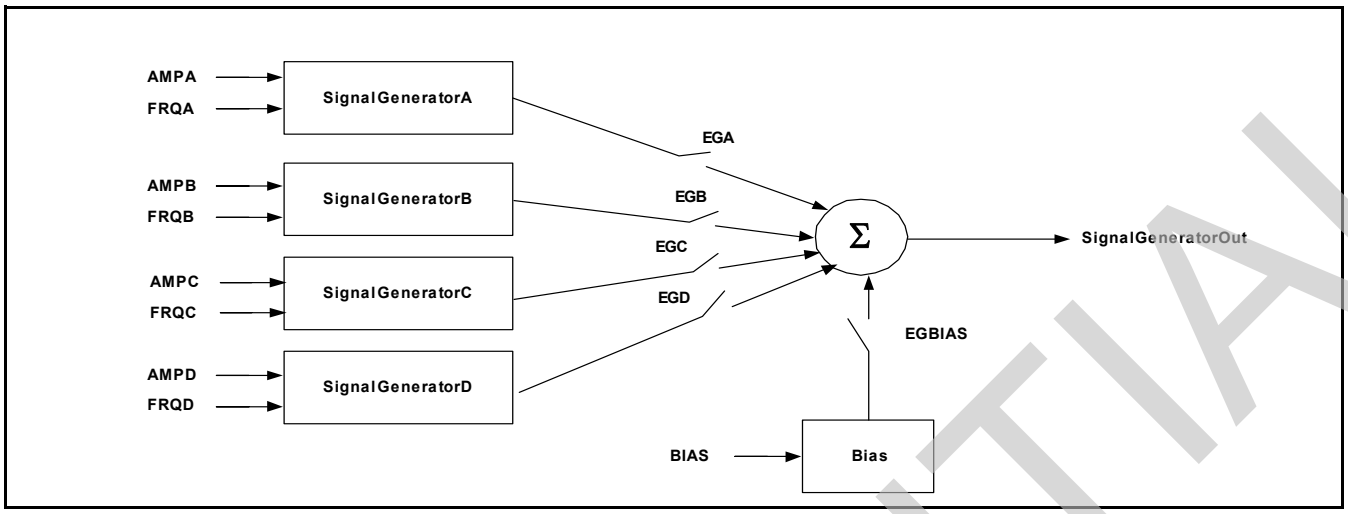


Figure 8 - Multi-Tone Generation

Signal Generator A is also used by the Microsemi *VeriVoice* test suites to produce slow ramps. This allows a complex sequence of diagnostic test voltages to be generated in a controlled manner without generating unwanted transients on the line.

Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system.

The EGA/B/C/D bits are controlled by the *VP-API-II* Cadencing engine.

3.6.2 Frequency and Amplitude Modulation

The signal generators can also be used to generate frequency-modulated and/or amplitude-modulated tones in conformance with worldwide Howler (receiver off-hook) and call progress tone requirements. Frequency modulation is performed in a dedicated hardware block, while amplitude modulation is performed in software by *VP-API-II*.

To generate frequency-modulated tones, Signal Generator A is configured as a modulator, while Signal Generator D is configured as a carrier. The output of Signal Generator A is the frequency input to Signal Generator D. Note that Signal Generator A needs a positive DC bias so that its output is always positive. Caller ID generation is not available while frequency modulation is taking place. Figure 9 shows the configuration for modulation. Note that Signal Generators B and C are available to be summed to the frequency-modulated signal, if necessary.

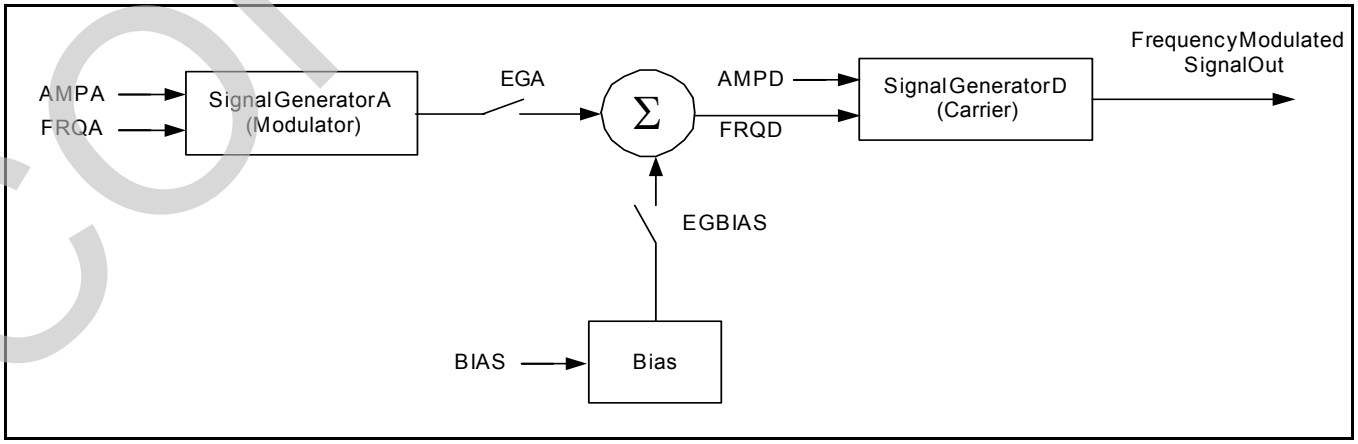


Figure 9 - Frequency Tone Modulation

Frequency and amplitude modulation allow the Le9662 device to meet exacting Howler tone requirements such as those specified in *BTNR 1080 Version 15* and *Draft 960-G*, *NTT Edition 5* and *Austel AUS002:2001*.

Table 4 lists the *VP-API-II* functions that are used for Howler tone generation.

Function Name	Description
`VpSetLineState()`	`VP_LINE_HOWLER` -- Places the device in a high gain state for Howler tone generation.
`VpSetLineTone()`	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually or modulated in order to generate Howler tones.

Table 4 - VP-API-II Functions for Howler Tone Generation

3.6.3 Triangular and Trapezoidal Signal Generation

The signal generators can also be used to generate trapezoidal waveforms for ringing. Figure 10 shows a configuration that is typically used to generate trapezoidal waveforms. Triangular waveforms can also be generated.

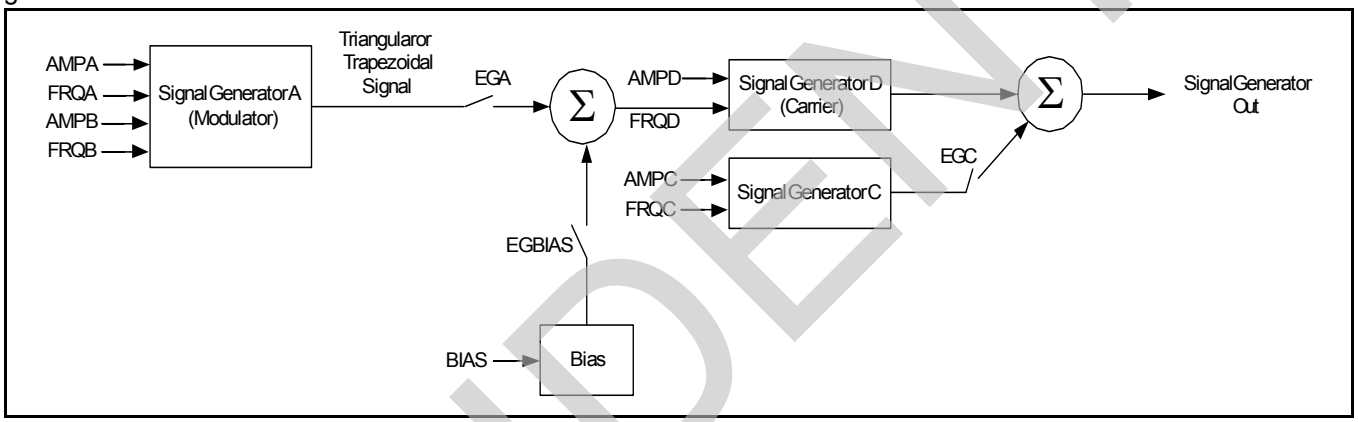


Figure 10 - Trapezoidal Signal Generation

3.7 Low Power DC Feed

The Le9662 device supports *Low Power Idle Mode (LPIM)*, which reduces the system power consumption during idle (On-Hook) state. *LPIM* provides a weak DC feed capable of at least 5 mA to the line and reacts to a change in the line voltage to create an off-hook indication when a telephone goes off-hook.

3.8 Normal DC Feed

DC feed is active in normal idle, talk and ringing states and the programmed characteristics appear between Tip and Ring. VAS is chosen to ensure that sufficient headroom is available for the amplifiers when on-hook to support on-hook transmission with the programmed open circuit (VOC) voltage. Values programmed in device for VAS, VOC, and ILA are determined during `VpCalLine()` to ensure circuit performance. Please refer to Figure 11, “Active State I / V Characteristic” on page 17 for the Active state I/V characteristic feed curve for Rfeed = 200 Ω.

The *DC Profile* produces a DC feed curve at Tip and Ring when the fuse resistors are inside the feedback loop formed by the RTDC and RRDC feedback network. Note that the value of the combined Tip and Ring feed resistors Rfeed is programmable to 0, 50, 100, or 200 Ω to correspond to the choice of PTCs or fuse resistors that are used. Refer to Figure 36, “Profile Wizard - DC Profile Configuration Example” on page 66 for more details.

3.9 Test Feed

The Tip Open test state presents the DC feed characteristic shown in Figure 11 between the Ring lead and ground.

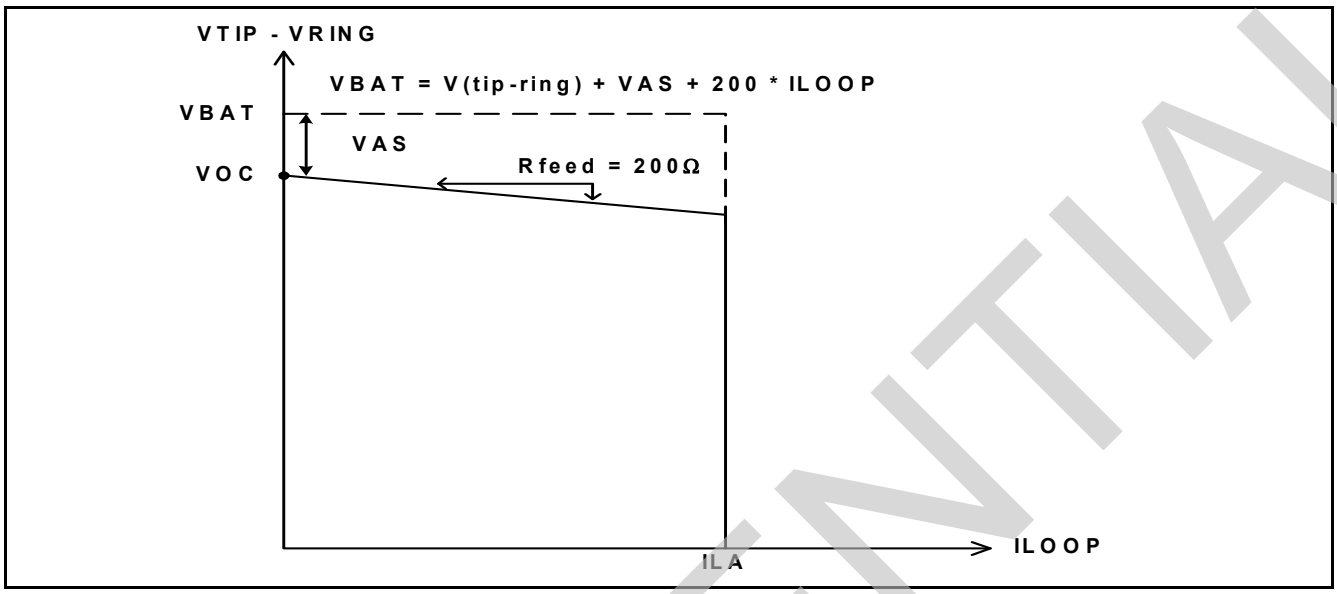


Figure 11 - Active State I / V Characteristic

3.10 Ringing

In this state, the voice DAC is used to apply the ringing signal and bias to the high voltage line driver. Internal feedback maintains a low system output impedance during ringing and the current limit is increased in the Ringing state. In order to minimize line transients, entry and exit from the Ringing states are intelligently managed by the Le9662 device. The Le9662 supports balanced ringing.

3.10.1 Balanced Ringing

Internal balanced ringing drives the subscriber line with balanced ringing voltage waveforms (see Figure 12).The Le9662 device can be programmed to output either sinusoidal or trapezoidal ringing waveforms. The ringing signal is driven differentially, thus maximizing the ringing signal swing. In this mode, the SLIC appears to the subscriber line as a voltage source with an output impedance of 200 Ω. The maximum ringing signal possible is 100-V_{PK} for FBABS operation or 85-V_{PK} for BBABS operation, corresponding to the maximum AC + DC voltages.

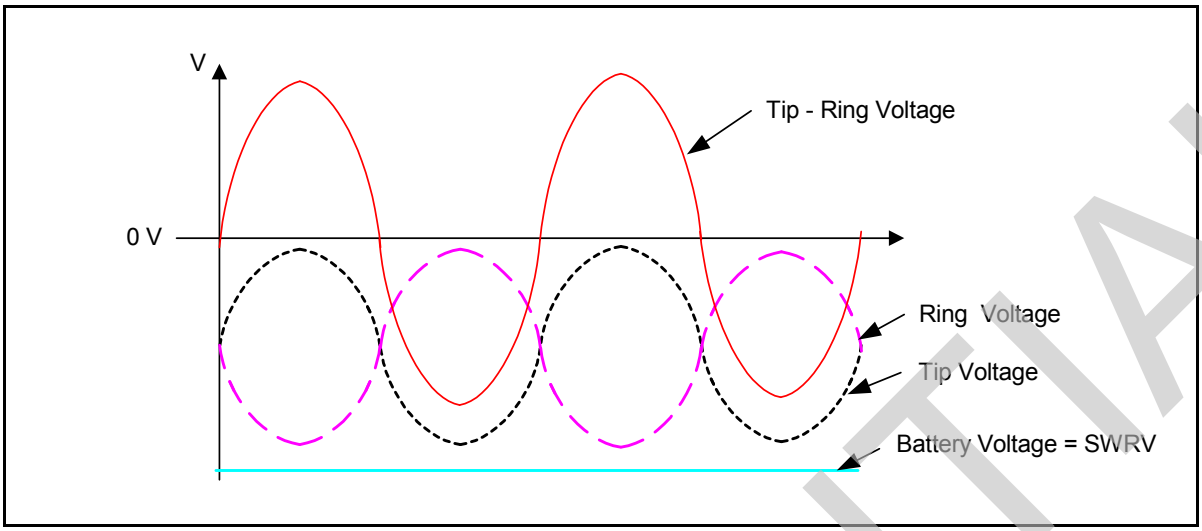


Figure 12 - Balanced Ringing with Fixed Supply

3.10.2 Adaptive Ringing Amplitude (BBABS Operation)

The Le9662 device supports adaptive ringing amplitude when configured for BBABS operation. Adaptive ringing amplitude limits the maximum power that is generated during ringing at or below a specified level.

3.10.3 Switch Hook Detection

The FXS supervision circuits of the Le9662 device provide debounced off-hook indications to an external processor via the host port interface. The supervision circuit compares a scaled version of the Tip-Ring current to a programmed off-hook threshold, TSH. The output of the comparator is debounced by a programmable debounce timer, DSH. A debounced off-hook indication generates an interrupt to the host processor.

3.10.4 Ring Trip Detection

Ring trip is the process of sensing a subscriber's off-hook event during ringing. This is accomplished by sensing the rise in loop current which occurs when a phone goes off-hook. The Le9662 device can detect ring trip when the ringing signal is purely AC and/or when the ringing signal has a DC bias on it. To do so, the ring trip algorithm is automatically altered internally by the Le9662 device based on the user-programmed parameters.

The ring trip detector uses the Tip-Ring current as an input. This current is rectified so that AC + DC ring trip can be detected. The output of the rectified signal is compared to a programmable ring trip threshold and the output is digitally debounced. The output is blanked upon ring entry to avoid false ring trips.

The ring trip detection circuit provides debounced ring trip indications to an external processor via the host port interface. The ring trip circuit compares a scaled version of the Tip-Ring current to a programmed Ring Trip Threshold (RTTH). The output of the comparator is processed by the ring trip algorithm on a cycle by cycle basis to provide immunity to false ring trips. In addition, spending more than 50% of the time in ringing current limit will generate a trip indication. A positive ring trip occurs if a trip indication is present for one (optional) or two (default) complete ring cycles, and an interrupt can be raised to the host processor. For AC-only ringing, the signal is half-wave rectified.

The Ring Trip Threshold (RTTH), integration method (positive half-wave for AC only or full-wave for AC+DC), the number of cycles (1 or 2), and Ringing Current Limit (ILR) are programmed in the *Ringing Profile*. Microsemi

provides a number of example *Ringing Profiles* for most common ringing requirements incorporating the ringing signal parameters and corresponding ring trip settings.

The following equations can be used to select new ring trip settings when using different ringing waveforms and different loads. They allow the ratio of the open circuit ringing voltage to the ringing threshold current to vary by +/-20%, which is conservative.

Name	Description
AMPA	Amplitude of signal generator A which is used for ringing
FREQA	Frequency of signal generator A which is used for ringing
BIAS	DC bias for ringing
RTDCAC	Ringing trip based on AC only or Battery Backed (DC) Ringing
RTTH	Ringing trip threshold in 0.5 mA steps from 0 to 63.5 mA
ILR	Ringing current limit programmed in 2 mA steps. ILR=0 represents 50 mA. ILR = 31 represents 112 mA
HOOK	Interrupt in signaling register indicating a ring trip occurred

Table 5 - Ring Trip Parameters

For AC only ringing, RTDCAC is 1 and the ringing current is half-wave rectified and averaged over a ringing cycle. If this result exceeds the RTTH threshold for two successive cycles, the HOOK bit will be set. This method limits the supported loop length x depending on the minimum must not trip ringing impedance (Rmnt in Ohms) and allowing for errors in the applied ringing voltage and trip level. The maximum loop resistance is given by:

$$RLOOP(max) = 0.67 x Rmnt - Rphone - 66\Omega$$

RLOOP (max) excludes the DC resistance of the phone (Rphone, typically 430 Ω in the U.S.), and the fuse resistance if DC line sensing is behind the fuse resistors.

For a sinusoidal ringing waveform of VRING (RMS) volts, and Rmnt impedance, the following ring trip settings should be used:

$$RTTH = \frac{0.54 x VRING}{Rmnt + 200\Omega}$$

$$ILR = \frac{1.4 x VRING}{Rmnt + 200\Omega}$$

In general for short loop applications, it is recommended to use AC ring trip even in the presence of a DC bias that could allow a DC based ring trip, and the above equations still apply. Note that the ringing source impedance is nominally 200 Ω.

3.11 Subscriber Line Testing

The Le9662 device provides the ability for the user to perform the *Telcordia GR-909-CORE / TIA-1063* diagnostic testing for the voice ports. In Test mode, a variety of input signals can be read from the voice ADC converter. These signals include the switching regulator voltage and the line DC and AC voltages.

3.11.1 VeriVoice Professional Test Suite Software

VeriVoice Professional Test Suite Software is an advanced test suite featuring the following tests:

- Line Voltage: Checks for hazardous and foreign AC and DC voltages.
- Receiver Off-Hook: Checks for longitudinal fault, off-hook resistive fault and receiver off-hook.
- Regular REN: Tests the impedance of the line and returns a fail if the Ringer Equivalence Number (REN) is too low or high.
- Electronic REN: Provides REN Tip to Ring, Tip to ground and Ring to ground based on capacitance
- Resistive Fault: Measures three-element resistance.
- GR-909-CORE / TIA-1063: Performs all of the *GR-909-CORE* outward tests in the correct sequence.
- Capacitance: Measures three element capacitance
- Master Socket: Detects master socket terminations
- Cross Connect: Detects cross connected FXS
- Loopback: Enables receive-to-transmit signal loopback using two different methods
- Read Loop Conditions: Measures voltages between Tip and Ring, Tip to ground, Ring to ground, and VBAT to ground. Also measures metallic and longitudinal line currents in supported states.
- Read Battery Conditions: Reads the battery voltages connected to the line circuit.
- DC Voltage Self-Test: Verifies that the line circuit has the ability to drive the voltage ranges required for the normal operation of the line circuit.
- DC Feed Self-Test Measures the voltage and current across a known internal test termination using the *DC Profile* that has been programmed.
- Ringing Self-Test Verifies ring signal generation, drive capability, and ring trip.
- On/Off-Hook Self-Test Creates on-hook and off-hook conditions on the line using the internal test termination and verifies that they are properly reported.

3.12 Manufacturing Testing

The Le9662 is supported by the *VeriVoice Manufacturing Test Package (VVMT),* a platform independent 'C' source code module which facilitates factory testing and calibration of assembled boards.

3.13 Metering

The Le9662 device is capable of 0.5 V_{RMS} metering into a 200 Ω metering load at either 12 kHz or 16 kHz. Smooth metering application and abrupt metering application are supported. A typical metering sequence is shown below in Figure 13.

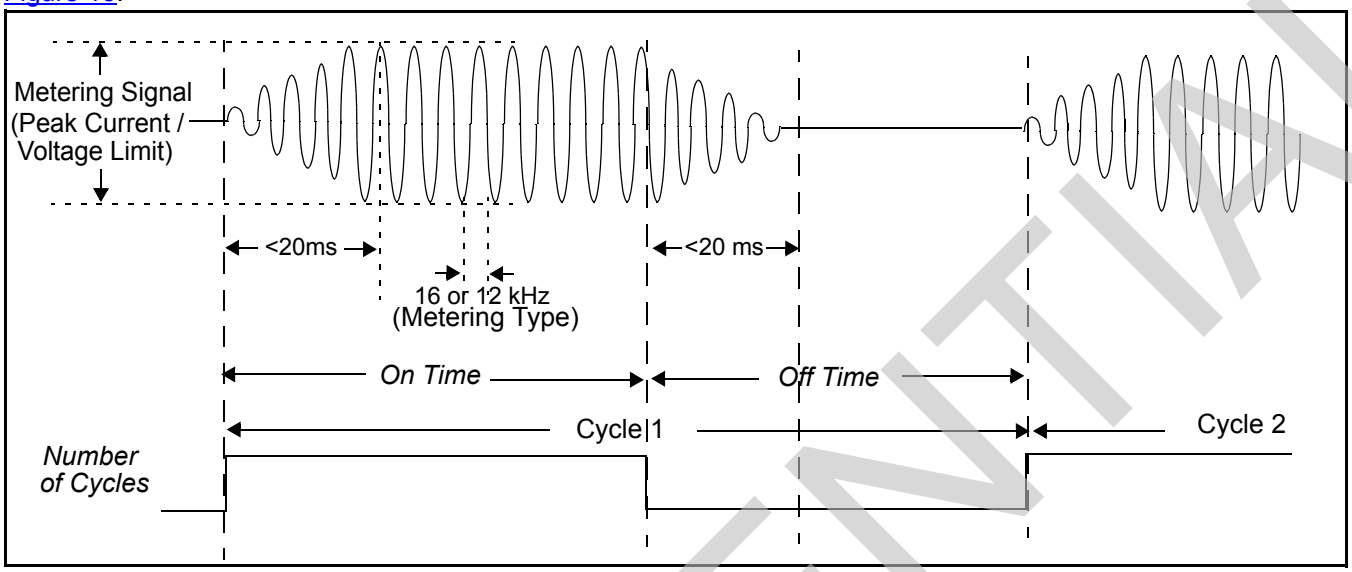


Figure 13 - Metering Pulse Definitions

The metering on time, off-time, and number of cycles are programmed in the *VP-API-II* function `VpStartMeter()`. This off-loads much of the timing from the host processor. Note that a ramp up / ramp down period of up to 20 ms is possible. The metering type (12 or 16 kHz), peak current and voltage limit are set in the *Metering Profile* and are used by the *VP-API-II* function `VpInitMeter()`. Note that in a normal configuration, some of the metering current flows into the CTD and CRD capacitors, so that the current sourced into an external load will be less than that programmed peak current parameter even when the metering voltage limit is not reached. The metering voltage at the load is also dependent on the total fuse resistance and the minimum load resistance (typically 200 Ω).

3.14 Switching Regulator Controllers

The switching regulator controller and the external power train circuitry provide a flexible switching regulator that automatically produces the negative supply voltages required to drive each line. The controller detects over current events and terminates the output pulse on a cycle by cycle basis.

The switching regulator has three modes of operation: Low, Medium, and High, which roughly correspond with On-Hook, Off-Hook, and Ringing states. These modes of operation provide for increased efficiency over a wide load range. In Low Power mode the switcher produces maximum efficiency in the idle condition while providing up to one watt of output power capability. In Medium Power mode the switcher provides greater power without significant sacrifice of efficiency. In High Power mode, which is usually of short duration, the switching regulator supports up to 10 watts of output power.

Switching regulator parameters are set in the *Device Profile.*

The Le9662 controller supports the following switching regulator types.

3.14.1 Shared Flyback Automatic Battery Switching (FBABS)

The recommended FBABS switching regulator circuit is shown in Figure 30 on page 51. The regulator shown is a typical flyback configuration with a multi-tap transformer configured for two outputs. The flyback configuration is capable of ringing both lines simultaneous and can ring a variety of loads without clipping. The control switching frequency for FBABS operation is 48 kHz for Low Power mode and 512 kHz for Medium and High Power modes.

Switcher Y has been configured to generate two fixed supplies, high battery voltage VBATH and low battery voltage VBATL, where the VBATL supply is regulated. By regulating VBATL at around -27 V and using a transformer with an output winding split into three equal sections, VBATH will be centered around -81 V. VBATH is applied to the VBH device pin and VBATL is applied to the VBL_1 and VBL_2 device pins.

The LFC pins support a soft start for the switching regulator controllers by filtering the internally generated switcher output reference using an external capacitor. LFC_1 is associated with Switcher Y, and LFC_2 is associated with Switcher Z. The pole is set with a nominal 4 kΩ internal resistance, allowing a 0.1 µF capacitor to provide a 10 ms ramp time. It is also possible to control the power-up of the switching regulators by appropriate use of the switcher power modes, eliminating the need for external capacitors. If the switcher controller is not being used, the corresponding LFC pin can be left open.

Even if the Le9662 device is not using the switching regulator controllers to generate the battery supplies, it must sense each of the applied batteries through the SWVSY and SWVSZ pins for correct longitudinal control and battery switching.

3.14.2 Shared Inverting Buck-Boost Automatic Battery Switching (BBABS)

The recommended patent-pending BBABS switching regulator circuit is shown in Figure 31 on page 53. The regulator shown is an inductor based inverting buck-boost configuration with output voltage doubler. The circuit adds the applied VSW voltage to the doubled battery voltage. The BBABS switching regulator circuit has been crafted for extremely low cost by using low cost, low voltage components while maintaining high performance and high efficiency. The switching regulator circuit is capable of simultaneous ringing of both lines without clipping. The control switching frequency for BBABS is 24 kHz for Low Power mode and 128 kHz for Medium and High Power modes.

Switcher Y has been configured to generate one fixed supply voltage, low battery voltage VBATL. The VBATL value is programmable. The VBATL supply is regulated but the switching circuit provides good VBATH regulation when VBATL is loaded. VBATH is obtained by the formula:

VBATH = -(VSW + (2 * |VBATL|) – 2 V).

VBATL can be programmed to a low value for supervision and active states and can be programmed to a high value to perform ringing. With a VSW of +12 V, a VBATL setting of -25 V produces a VBATH of -60 V, these voltages are adequate for line supervision and active off-hook operation. VBATL can be increased to -35 V to produce a VBATH of -80 V and open circuit ringing of 50 V_{RMS}; or VBATL can be increased to -40 V to produce a VBATH of -90 V and open circuit ringing of 60 V_{RMS}. For the short period of time that one channel is ringing, the adjacent channel will consume more power due to the elevated battery voltages, but overall performance in that channel will not be affected. VBATH is applied to the VBH device pin and VBATL is applied to the VBL_1 and VBL_2 device pins.

LFC pins and battery sense pins operate identically to that of FBABS operation, as described above.

3.15 Charge Pump Regulator and MOSFET Gate Driver

For FBABS operation, the Le9662 device features an internal charge pump regulator to generate a supply voltage suitable to drive external logic level rated (4.5 V, V_{GS}) MOSFET devices. The regulator converts DVDD (3.3 V) into VDDSW, which is programmable between 4.3 V and 5 V (with a 4.7 V default). This allows the use of a wide range of MOSFET devices.

The charge pump has an output under-voltage protection circuit with a threshold of about 0.2 V below the target voltage. Due to the limited capability of the charge pump, the maximum MOSFET total gate charge is limited to 16 nC for an operating frequency of 512 kHz. The charge pump regulator also includes an optional cycle skipping feature that allows the switcher controller to skip switching cycles in the event that the load on VDDSW is too high for the charge pump to maintain the programmed voltage. Even with cycle skipping, if the load is too heavy, the charge pump regulator can still shut down if the output voltage cannot be maintained.

For BBABS operation which uses PNP bipolar transistors, the charge pump should be disabled. Tie the VDDSW pin to DVDD (3.3 V).

Charge pump features, including charge pump use and output voltage, are configurable in the *Device Profile*. The default reference design profiles provided by Microsemi already have the charge pump settings appropriately configured.

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Ambient temperature, under Bias	-40°C < T_A < +85°C
Ambient relative humidity (non condensing)	5 to 95%
VBH, VBL voltage with respect to GND FBABS operation BBABS operation	 -125 V_{DC} to +0.5 V_{DC} -115 V_{DC} to +0.5 V_{DC}
VBH with respect to GND (both lines active VBL), VBL < |–50| V FBABS operation	 -160 V_{DC} to +0.5 V_{DC}
AVDD, DVDD, VDDHPI voltages with respect to GND	-0.4 V_{DC} to +4.0 V_{DC}
AVDD voltage with respect to DVDD	-0.4 V_{DC} to +0.4 V_{DC}
VDDSW voltage (1)	-0.4 V_{DC} to +4.0 V_{DC}
IDDSW current (1)	200 mA
$I/O1_1$, $I/O1_2$ current sink to GND (2)	70 mA
$TIPD_i$ or $RINGD_i$ voltage with respect to GND (continuous)	VBH – 1 V_{DC} to + 1 V_{DC}
$TIPD_i$ or $RINGD_i$ voltage with respect to GND (10 ms, F = 0.1Hz)	VBH – 5 V_{DC} to + 5 V_{DC}
$TIPD_i$ or $RINGD_i$ voltage with respect to GND (1 µs, F = 0.1Hz)	VBH – 10 V_{DC} to + 10 V_{DC}
$TIPD_i$ or $RINGD_i$ voltage with respect to GND (250 ns, F = 0.1Hz)	VBH – 15 V_{DC} to + 5 V_{DC}
$TIPD_i$ or $RINGD_i$ current (continuous)	±150 mA
$TIPD_i$ or $RINGD_i$ current (1 µs)	±400 mA
Latch up immunity (any pin)	±100 mA
Maximum device power dissipation, continuous (3) - T_A = 85°C, P_D	2.0 W
Junction to ambient thermal resistance (3), θ_{JA}	27°C/W
Junction to board thermal resistance (3), θ_{JB}	7.5°C/W
Junction to case bottom (exposed pad) thermal resistance, $\theta_{JC\ (BOTTOM)}$	3.85°C/W
Junction-to-top characterization parameter (3), ψ_{JT}	0.86°C/W
Reflow temperature, 10 sec., MSL3, per *JEDEC J-STD-020*	260°C
ESD immunity (Human Body Model)	*JESD22 Class 1C* compliant

Notes:

1. *When VDDSW is tied to DVDD*
2. *When configured as outputs (for LED or relay drive control)*
3. *See "Thermal Performance"*

4.2 Thermal Performance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane. Thermal performance depends on the number of PCB layers and the size of the copper area. Please refer to Microsemi's application note *QFN Package (Document ID#: 080791)* for general design and layout guidelines.

The thermal specifications in "Absolute Maximum Ratings" assume that the device is mounted on a highly effective thermal conductivity test board (4 layers, 2s2p) per *JEDEC JESD51-7* and *JESD51-5*, and featuring the recommended 8x8 array of thermal vias shown in Figure 44 on page 75.

4.3 Operating Ranges

Microsemi guarantees the performance of this device over industrial (-40ºC to 85ºC) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the *Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.*

4.3.1 Recommended Operating Conditions

Ambient temperature	-40°C < T_A < +85°C
Ambient relative humidity	15% to 85%
GND	0 V_{DC}
AVDD	+3.3 V_{DC} ± 5%
DVDD with respect to AVDD	±50 mV_{DC}
VDDHPI	+1.71 V_{DC} to DVDD
VDDSW VDDSW supplied from DVDD VDDSW internally generated	 +3.3 V_{DC} ± 5% +4.3 V_{DC} to +5.0 V_{DC}
FBABS operation VBH (both lines active VBL), VBL < |-50| V VBH (all other states) VBL (in active states) VBH with respect to VBL	 -150 V_{DC} to -(VOC + 7.0) V_{DC} -120 V_{DC} to -(VOC + 7.0) V_{DC} VBH to -20 V_{DC} 0 V_{DC} ≤ (VBL – VBH) < 90 V_{DC}
BBABS operation VBH VBL	 VBH = -(VSW + (2 * |VBL|) – 2V) -40 V_{DC} to -25 V_{DC}
Digital pins, except $I/O1_i$, $I/O2_i$	GND to VDDHPI
$I/O1_i$, $I/O2_i$	GND to DVDD
Analog pins	GND – 0.3 V_{DC} to AVDD + 0.3 V_{DC}

5.0 Electrical Characteristics

Unless otherwise noted, test conditions are:

- Typical values are for T_A = 25ºC and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in "Recommended Operating Conditions" on page 25, except where noted
- Default (unity) gain in X, R, DRL, AX and AR blocks; default coefficients in DISN, Z and B filters
- Battery voltage for FBABS operation: VBH = -81 V and $VBL_{1/2}$ = -27 V
- Battery voltage for BBABS operation:
  - Active and Idle states: VBH = -60 V and $VBL_{1/2}$ = -25 V
  - Ringing state: VBH = -80 V and $VBL_{1/2}$ = -35 V
- DC feed programmed and calibrated to:
  - ILA = 25 mA, VOC = 48.0 V, bsov = 2.92 V, and bshv = 5 V
- AC and DC load resistance R_L = 600 Ω
- Fuse resistors for device tests are R_F = 14 Ω
- 0 dBm0 = 0 dBm (600 Ω) = 0.775 V_{RMS}. Digital gains GX0 and GR0 to achieve 0 dBr relative levels are
  GX0 = +6.797 dB (7A20h) A-law or linear and GX0 = +6.737 dB (2A20h) µ-law to set A/D transmit gain to 0dB
  GR0 = -1.793 dB (6AA0h) A-law or linear and GR0 = -1.720 dB (3AA0h) µ-law to set D/A receive gain to 0dB
- Ringing tests use the following conditions:
  - C1 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 3 REN (2333 Ω + 24-µF) load
  - C2 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 5 REN (1386 Ω + 40-µF) load

5.1 Supply Currents and Power Dissipation

5.1.1 FBABS Operation

External Switcher circuit as shown in Figure 30 on page 51 with input voltage VSW = 12 V_{DC}.

Operational State	Condition	I_{DD} mA *(Note 2)*	I_{VSW} mA *(Note 3)*	I_{VBH} mA	$I_{VBL1/2}$ mA	Device Power mW	System Power mW	Power	Notes
		Typ	Typ	Typ	Typ	Typ	Typ		
Shutdown	Ch1/Ch2	1.5	0	0	0	5	5	Per Channel	
Disconnect	Ch1/Ch2	5.5	1.6	0.1	0	25	37		
Low Power Idle Mode (LPIM)	Ch1/Ch2	9.5	2.8	0.3	0	52	65		
Idle	On-Hook	14.5	14.2	0.8	0	116	218		
Active (normal or reverse polarity)	OHT	23	22.1	1.9	0	230	341		
	Off-Hook, 300 Ω	24	80.1	0.9	26	658	1048		
LPIM/Ringing	Ch1 LPIM, Ch2 Ringing C1	33.5	259	31.3	0	900	2191	Both Channels	*1.*
	Ch1 LPIM, Ch2 Ringing C2	33.5	174	21	0	1174	3211		
Active/Ringing	Ch1 Off-Hook, Ch2 Ringing C1	48	336	32	26	1506	3174		*1.*
	Ch1 Off-Hook, Ch2 Ringing C2	48	252	21.6	26	1880	4194		

1. *Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.*
2. *I_{DD} supply current is the sum of I_{AVDD} and I_{DVDD} for the device divided by 2.*
3. *I_{VSW} is not tested in production.*

5.1.2 BBABS Operation

External Switcher circuit as shown in Figure 31 on page 53 with input voltage VSW = 12 V_{DC}.

Operational State	Condition	I_{DD} mA *(Note 2)*	I_{VSW} mA *(Note 3)*	I_{VBH} mA	$I_{VBL1/2}$ mA	Device Power mW	System Power mW	Power	Notes
		Typ	Typ	Typ	Typ	Typ	Typ		
Shutdown	Ch1/Ch2	1.5	0	0	0	5	5	Per Channel	
Disconnect	Ch1/Ch2	5.5	0.7	0.1	0	25	26		
Low Power Idle Mode (LPIM)	Ch1/Ch2	9.5	1.6	0.3	0	47	51		
Idle	On-Hook	14.5	5.3	0.8	0	99	112		
Active (normal or reverse polarity)	OHT	23	11.9	1.9	0	190	219		
	Off-Hook, 300 Ω	24	73.3	0.9	26	520	959		
LPIM/Ringing	Ch1 LPIM, Ch2 Ringing C1	33.5	275	31.3	0	839	2319	Both Channels	*1.*
	Ch1 LPIM, Ch2 Ringing C2	33.5	184	21	0	1140	3406		
Active/Ringing	Ch1 Off-Hook, Ch2 Ringing C1	48	360	32	26	1523	3463		*1.*
	Ch1 Off-Hook, Ch2 Ringing C2	48	275	21.6	26	1793	4483		

1. *Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.*
2. *I_{DD} supply current is the sum of I_{AVDD} and I_{DVDD} for the device divided by 2.*
3. *I_{VSW} is not tested in production.*

5.2 DC Characteristics

Symbol	Parameter Descriptions	Min	Typ	Max	Unit	Note
V_{IL}	Digital input low voltage			0.8	V	
V_{IH}	Digital input high voltage	2.0				
I_{IL}	Digital input leakage current	-7		+7	µA	
I_{AIL}	Analog input leakage current	-1		+1		
V_{HYS}	Digital input hysteresis	0.16	0.25	0.34	V	*1.*
V_{OL}	Digital output low voltage $I/O1_1$, $I/O1_2$ (I_{OL} = 50 mA) $I/O2_1$, $I/O2_2$ (I_{OL} = 4 mA) $I/O2_1$, $I/O2_2$ (I_{OL} = 8 mA) Other digital outputs (I_{OL} = 2 mA)			0.8 0.4 0.8 0.4	V	*2.*
V_{OH}	Digital output high voltage $I/O2_1$, $I/O2_2$ (I_{OH} = 4 mA) $I/O2_1$, $I/O2_2$ (I_{OH} = 8 mA) Other digital outputs (I_{OH} = 400 µA)	V_{DVDD} – 0.4 V V_{DVDD} – 0.8 V 2.4				
I_{OL}	Digital output leakage current (Hi-Z state) 0 < V < DVDD	-7		+7	µA	
V_{REF}	VREF output open circuit voltage (I_{VREF} = +/-100 µA)	1.43	1.5	1.57	V	
C_{IREF}	IREF pin maximum load capacitance			20	pF	*1.*
C_I	Digital input capacitance			4		
C_O	Digital output capacitance			4		
$PSRR_1$	AVDD, DVDD power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	32	38		dB	
$PSRR_2$	VBH, VBL power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	40				*1.*

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *$I/O1_i$, and $I/O2_i$ outputs are resistive for less than a 0.8 V drop. Total DC current must not exceed absolute maximum ratings.*

5.3 DC Feed and Signaling – All States Except Low Power Idle Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
ILA programmable range, Active state FBABS operation BBABS operation		 18 18		 45 30	mA	*1.*
I_L, Loop current accuracy, Active state	I_L in constant-current region after ILA calibration	-10		+10	%	
I_{RINGD}, RINGD leakage, Ring Open state	VBH = -81 V R_L = 0 to GND or VBH			1000	µA	*1.*
I_{TIPD}, TIPD leakage, Tip Open state	VBH = -81 V R_L = 0 to GND or VBH			1000		
TIPD, RINGD leakage, Disconnect state	VBH = -81 V R_L = 0 to GND or VBH			10		
I_{RINGD}, RINGD current accuracy, Tip Open state	RINGD to ground	-10		+10	%	*1.*
V_{TIPD}, ground-start signaling	TIPD to -48 V = 7 kΩ, RINGD to ground = 100 Ω	-7.5	-5		V	
TDC, RDC input offset current		1.35	1.5	1.65	µA	*1., 2.*
Ground key accuracy	After calibration	-1 mA - 15%		+1 mA + 15%		
Switch hook accuracy	After calibration	-20		+20	%	
Open circuit voltage, $V_{TIPD} - V_{RINGD}$	VOC = 48 V, after VOC calibration	-7		+7		
V_{RINGD}, open circuit	VOC = 48 V, after VOC calibration	-56.5		-49.0	V	

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Analog input pad leakage can add to this value – see specification under "DC Characteristics" on page 28.*

5.4 DC Feed and Signaling – Low Power Idle Mode State

Description	Test Conditions	Min	Typ	Max	Unit	Note
$V_{TIPD} - V_{RINGD}$ voltage	VBH = -52 V, I_{LOAD} = 3 mA	44			V	*1.*
	R_{LOAD} = 3.5 KΩ	23	28	33		
	VBH = -52 V, R_{LOAD} = open	44	48	51		
I_{TIPD} current limit	TIPD sourcing current	9	31	70	mA	*1.*
I_{RINGD} current limit	RINGD sinking current, R_{LOAD} = 600 Ω	7.1	8.0	9.3		
Off-hook current settling time	R_{LOAD} = 200 Ω		150	800	µs	*1.*
DC feed resistance	I_{LOAD} < current limit		200		Ω	
	I_{LOAD} > current limit		230K			

Note:

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*

5.5 Metering

Description	Test Conditions	Min	Typ	Max	Unit	Note
Level accuracy	0.5 V_{RMS}, 12 or 16 kHz, 200 or 3000 Ω AC load	-5		+10	%	*1.*
Frequency accuracy	12 or 16 kHz	-0.1		+0.1	%	

Note:

1. This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.

5.6 Ringing

Description	Test Conditions	Min	Typ	Max	Unit	Note
Ringing Voltage Accuracy	52.5 V_{PK} into a 3 REN load	-7		+7	%	*1.*
Normal Polarity Ringing DC offset, $V_{TIPD} - V_{RINGD}$	R_L = open circuit, programmed rInging = 0 V_{PK}	-5	0	+2	V	*2.,3.*
Harmonic distortion	52.5 V_{PK} into a 3 REN load		3	5	%	
Ringing current limit accuracy	R_L = 600 Ω	-10		10		
Ringing source impedance			200		Ω	*2.*
DC ring trip accuracy	EGBIAS = 1	-15		+15	%	*2.,4.*
AC ring trip accuracy	EGBIAS = 0	-15		+15		
Ring trip delay	Periods of ringing	1		3	cycles	

Notes:

1. This production test is performed without calibration. After calibration, typical accuracy is within +/-4%.

2. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.

3. After calibration.

4. If the ringing current in the loop is near the current limit more than 50% of the time, a ring trip will occur regardless of the average current.

5.7 Switching Regulator Controller

The following specifications apply to switching regulator controllers Y and Z.

Description	Test Conditions	Min	Typ	Max	Unit	Note
SWISx shutdown threshold	Referenced to GND	85	100	115	mV	
SWISx hysteresis			25			*1.*
SWISx input bias current		-10		10	µA	
SWISx shutdown delay	V_{SWISx} > 115 mV	12		88	ns	*1., 2.*
SWCMPx output current		-200		200	µA	*1.*
SWCMPx operating range		0.4		2.6	V	
SWVSx to SWCMPx gain		0.4		40	V/nA	
SWVSx to SWCMPx bandwidth		100			kHz	
SWVSx input offset current	R_{VSx} = 1.0 MΩ	1.3	1.5	1.7	µA	
LFC output impedance			12		kΩ	
SWxV output voltage accuracy	FBABS operation: VBL regulation, calibrated -30 V voltage	-33		-27	V	*3.*

Notes:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.

2. Time from SWISx exceeding threshold to SWOUTx voltage passing through DVDD/2.

3. Accuracy following battery calibration depends on the battery voltage sense accuracy (+/-4%) plus the calibration resolution of +/- 0.625 V.

5.8 Charge Pump Controller and MOSFET Driver – FBABS Operation

The following specifications apply to the charge pump controller in FBABS operation when internally generating VDDSW and driving the switching regulator N-channel MOSFET devices.

Description	Test Conditions	Min	Typ	Max	Unit	Note
VDDSW output voltage range	I_{VDDSW} = 5 mA	4.3	4.7	5.0	V	*1.*
VDDSW step voltage	I_{VDDSW} = 5 mA		0.1			
VDDSW output voltage accuracy	VDDSW = 4.7 V, I_{VDDSW} = 5 mA	-3		+3	%	
VDDSW undervoltage lockout threshold	Below the target output voltage	110	200	290	mV	*1.*
SWOUTx peak source current	V_{SWOUTx} = 2.5 V, C_{LOAD} = 1.5 nF	100			mA	
SWOUTx peak sink current	V_{SWOUTx} = 2.5 V, C_{LOAD} = 1.5 nF	200				
Maximum total gate switching charge	VDDSW = 4.7 V, f = 512 kHz, VDDSW internally generated, switcher Y drive	16			nC	*1.*

Notes:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.

5.9 Voice ADC Signal Sense Accuracy

Description	Code	Full Scale	Useful Range	Min	Typ	Max	Unit	Note
Metallic AC coupled voltage (Tip/Ring voice)	00h	-3.44 to +3.44	-3.44 to +3.44	-4%		+4%	V	*1., 2.*
Voice DAC analog loopback	0Ah	-2.0 to +2.0	-1.0 to +1.0	-12%		+12%		

Notes:

1. All specifications assume calibration.

2. The % limits are defined as the % of programmed threshold value or the % of the actual voltage or current on Tip / Ring. The offset and percentage errors are independent and combine as RMS errors.

5.10 Supervision ADC Signal Sense Accuracy

Description	Code	Full Scale	Useful Range	Min	Typ	Max	Unit	Note
Sense at SWVSY	01h	-240 to +240	-180 to 0	-0.5 V – 4 %		+0.5 V + 4 %	V	*1., 2., 3., 6.*
Sense at SWVSZ	02h			-0.5 V – 4 %		+0.5 V + 4 %		
Sense at VS1, VS2	03h		-180 to +60	-0.5 V – 4 %		+0.5 V + 4 %		
Tip voltage to ground	04h		-225 to +225	-2.0 V – 4 %		+1.0 V + 4 %		
Ring voltage to ground	05h			-2.0 V – 4 %		+1.0 V + 4 %		
Metallic DC line voltage (Tip to Ring)	06h		-160 to +160	-0.5 V – 5 %		+0.5 V + 5 %		
Longitudinal DC line voltage (Tip to ground + Ring to ground)	0Ah			-1.0 V – 5 %		+1.0 V + 5 %		*1., 2., 6.*
MOSFET drive supply, VDDSW	10h	+2 to +10	+2.5 to +5.5	-0.08 V – 0.5 %		+0.08 V + 0.5 %		
Metallic loop current, IM (Tip to Ring) in Normal Mode	07h	-59.5 to +59.5[4]	-51 to +51[4]	-1.0 mA – 5 %		+1.0 mA + 5%	mA	
Longitudinal loop current, IL (total) in Normal Mode	08h	-59.5 to +59.5	-42 to +42	-1.0 mA – 5 %		+1.0 mA + 5%		
Ring current, IB (IM+IL)	0Eh			-2.0 mA – 5 %		+2.0 mA + 5%		
Tip current, IA (IM-IL)	0Fh			-2.0 mA – 5 %		+2.0 mA + 5%		
Metallic loop current (IM) in Low Gain Mode	08h	-297.5 to +297.5	-100 to +100	-5.0 µA – 5 %		+5.0 µA + 5%	µA	
Longitudinal loop current per wire (IL) in Low Gain Mode	07h		-250 to +250	-5.0 µA – 5 %		+5.0 µA + 5%		
Tip voltage to Longitudinal current ratio	N/A	N/A	N/A	-6.5		+6.5	%	*1., 5., 6., 7.*
Ring voltage to Longitudinal current ratio				-6.5		+6.5		
Metallic voltage to Metallic current ratio				-6.5		+6.5		
Temperature sense	0Dh	-50 to +150	-50 to +150	-15		+15	°C	*1., 6.*

Notes:

1. *All specifications assume calibration.*
2. *The % limits are defined as the % of programmed threshold value or the % of the actual voltage or current. The offset and percentage errors are independent and combine as RMS errors.*
3. *This is measured in production by calibrating offset voltage and applying -26 V for voltage to ground and 20 V Metallic. Accurately measuring smaller voltage requires care in offset calibration.*
4. *The Metallic loop current scale and range during ringing are -119 mA to +119 mA.*
5. *These are ratios of voltage to current measurements in Low Gain state performed during production testing.*
6. *Full scale is defined as a digital output code of ±32768.*
7. *Not tested in production.*

5.11 Transmission Characteristics – Narrowband Codec Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC – RAC overload level	Active state, GX = AX = 0 dB	3.4			V_{PK}	*1., 2.*
Transmit level, A/D	0 dBm, GX = GX0, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, GR = GR0, 1014 Hz		0		dBm	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, off-hook	-0.35		+0.35	dB	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, on-hook	-0.5		+0.5		
Idle channel noise $V_{TIPD} - V_{RINGD}$ Digital out	 Digital input = 0, A-law, 0 dBr Digital input = 0, µ-law, 0 dBr $V_{TIPD} - V_{RINGD}$ = 0 V_{AC}, A-law, 0 dBr $V_{TIPD} - V_{RINGD}$ = 0 V_{AC}, µ-law, 0 dBr			 -74 16 -65 19	 dBm0p dBrnC0 dBm0p dBrnC0	*5.*
Two-wire return loss	200 to 3400 Hz	26	30		dB	
Longitudinal to metallic balance	200 to 3400 Hz	50				*7.*
Longitudinal signal generation	300 to 3400 Hz	42				*7.*
Longitudinal current capability, per wire TIPD or RINGD	Active state	8.5			mA_{RMS}	*1.*
Longitudinal impedance at TIPD or RINGD	0 to 100 Hz, LI = 0		100		Ω/pin	
Crosstalk between channels TX or RX to TX RX or TX to RX	 0 dBm0, 1014Hz, Average 0 dBm0, 1014Hz, Average			 -76 -78	dBm0	
Attenuation distortion	300 to 3000 Hz	-0.125		+0.125	dB	*1., 3.*
Single frequency distortion	A-law or µ-law, off-hook			-46		*4.*
Second harmonic distortion, D/A	GR = 0 dB, linear mode, off-hook			-55		
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			678	µs	*1., 6.*
PESQ-LQ voice quality score	Linear, A-law, or µ-law		4.30			*1.*

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *See Figure 14 and Figure 15 on page 34.*
4. *0 dBm0 input signal, 300 to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.*
5. *No single frequency component in the range above 3800 Hz may exceed a level of -55 dBm0.*
6. *The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.*
7. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

5.12 Attenuation Distortion – Narrowband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 14 and Figure 15. The reference frequency is 1014 Hz and the signal level is -10 dBm0.

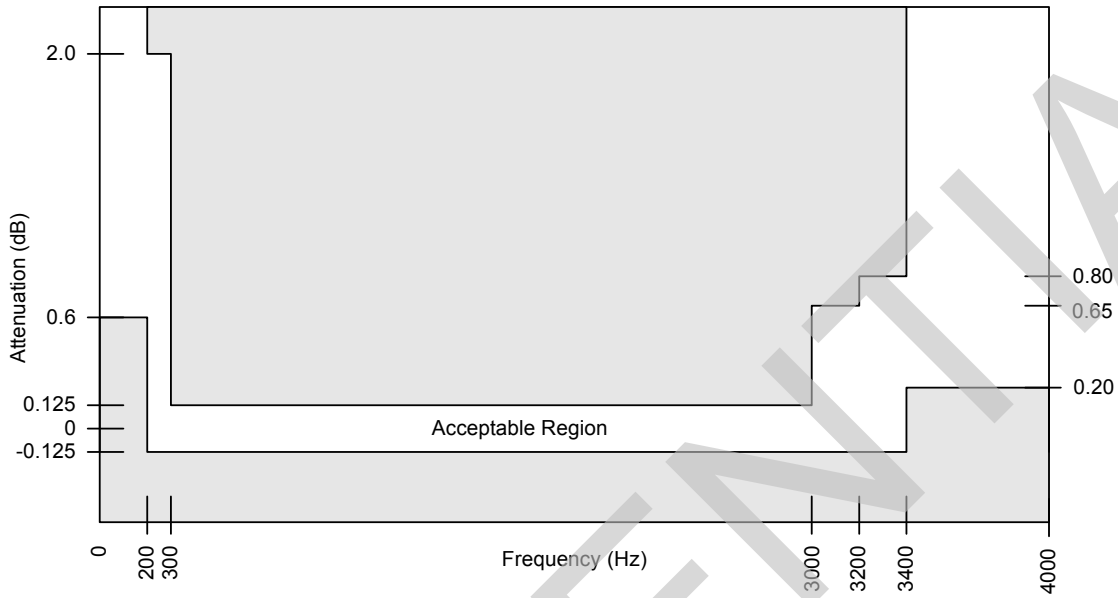


Figure 14 - Transmit (A to D) Path Attenuation vs. Frequency

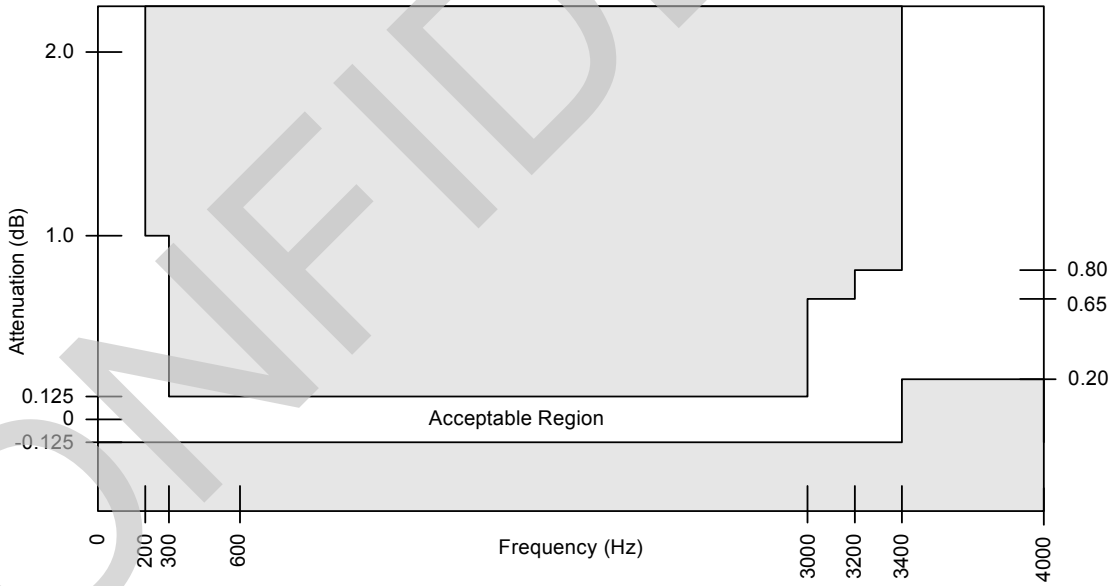


Figure 15 - Receive (D to A) Path Attenuation vs. Frequency

5.13 Discrimination Against Out-of-Band Input Signals – Narrowband Codec Mode

When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are

shown in Table 6. The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation} = \left[14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)\right] \text{dB}$$

.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	-25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	-25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	-25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	-25 dBm0 < A ≤ 0 dBm0	see Figure 16
4600 Hz < f < 100 kHz	-25 dBm0 < A ≤ 0 dBm0	32 dB

Table 6 - Out of Band Discrimination, Narrowband Codec Mode

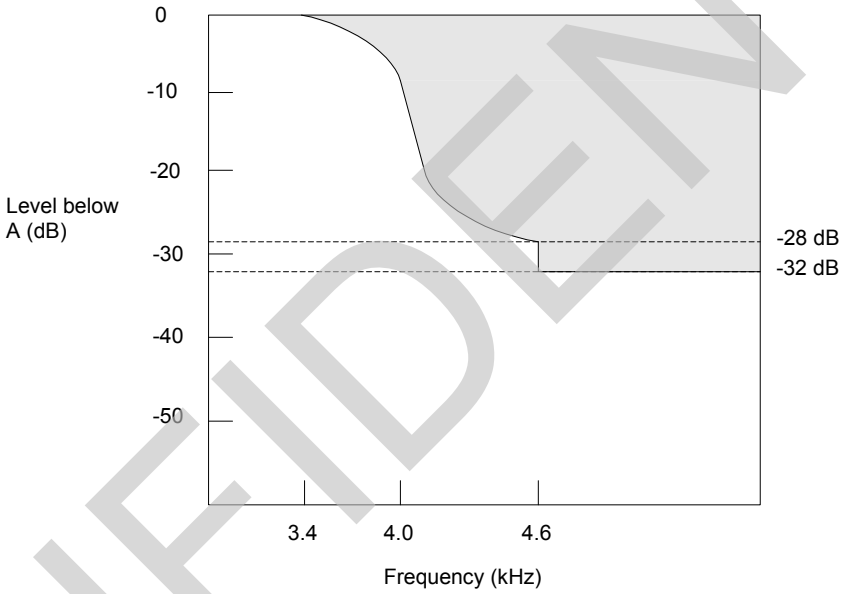


Figure 16 - Discrimination Against Out-of-Band Signals

5.14 Discrimination Against 12 kHz and 16 kHz Metering Signals – Narrowband Codec Mode

If the Le9662 device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones may also appear at the transmit input. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the TAC – RAC pin overload level.

5.15 Spurious Out-of-Band Signals at the Analog Output – Narrowband Codec Mode

With PCM idle code being applied from the host and either a quiet 600 Ω termination or an open being applied to Tip and Ring, any single frequency tone between 0 and 16 kHz measured at the analog output shall be less than -50 dBm0. With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of

0 dBm0 applied to the digital input, the level of the spurious Out-of-Band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	-32 dBm0
40 kHz to 240 kHz	-46 dBm0
240 kHz to 1 MHz	-36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 17. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[-14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] \text{dBm0}$$

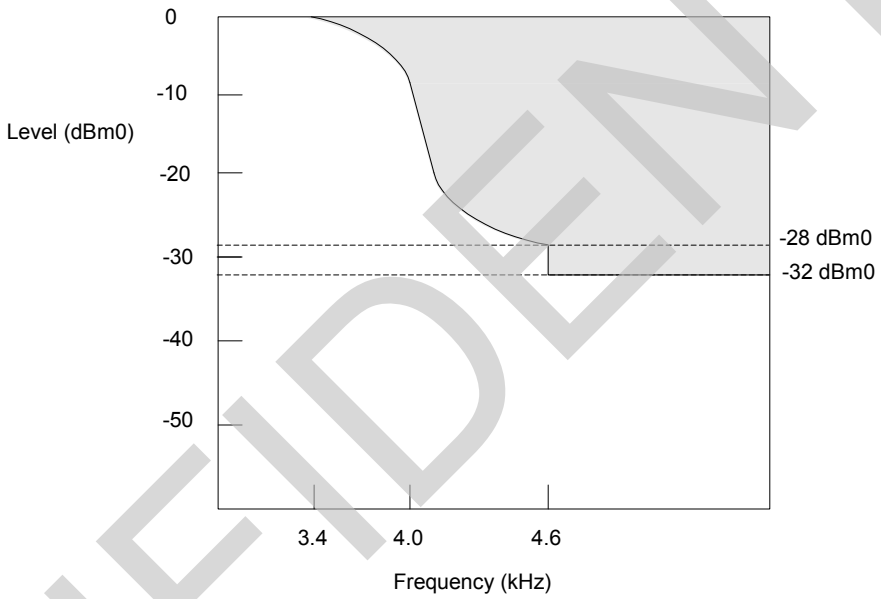


Figure 17 - Spurious Out-of-Band Signals

5.16 Overload Compression – Narrowband Codec Mode

Figure 18 on page 37 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. +1.2 dB < GX ≤ +12 dB
2. -12 dB ≤ GR < -1.2 dB
3. Digital voice output of one channel connected to digital voice input of a second channel.
4. Measurement analog-to-analog

.

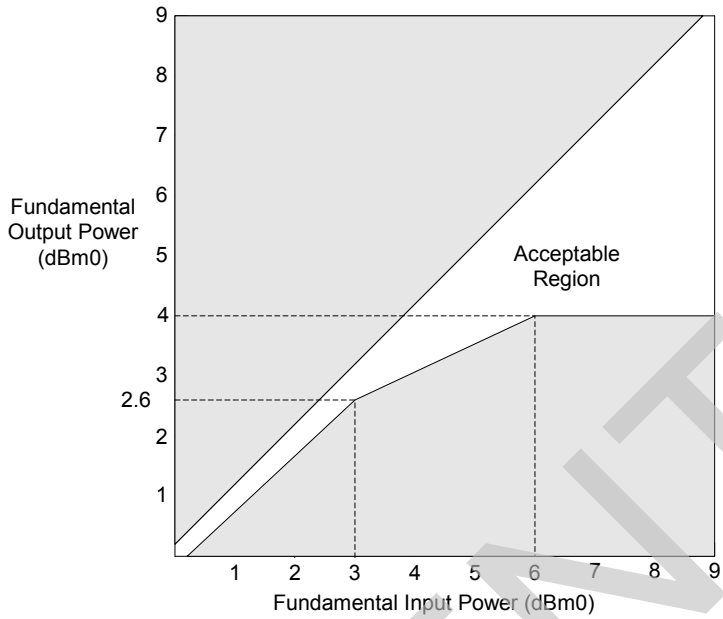


Figure 18 - Analog-to-Analog Overload Compression

5.17 Gain Linearity – Narrowband Codec Mode

The gain deviation relative to the gain at -10 dBm0 is within the limits shown in Figure 19 (A-law) and Figure 20 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

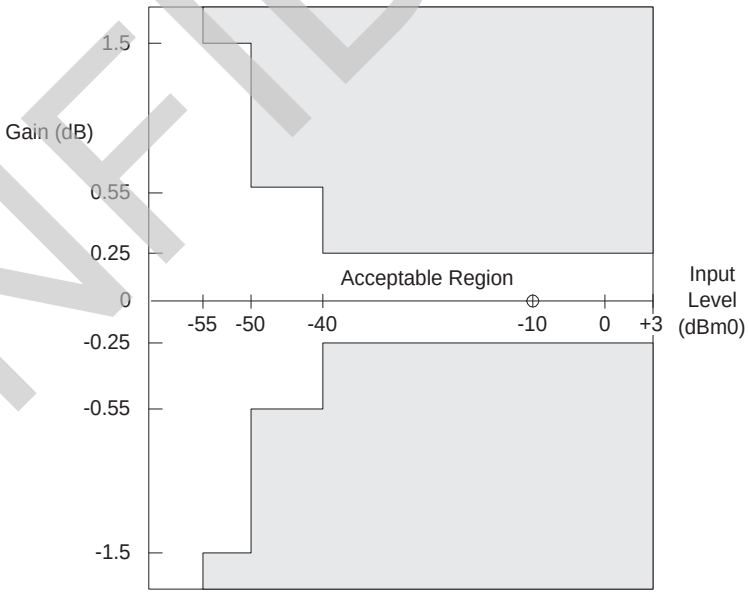


Figure 19 - A-law Gain Linearity with Tone Input (Both Paths)

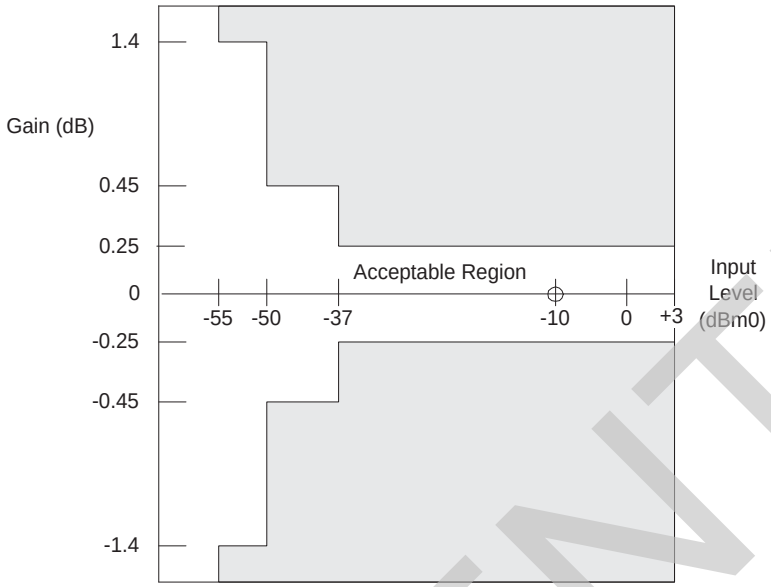


Figure 20 - µ-law Gain Linearity with Tone Input (Both Paths)

5.18 Total Distortion Including Quantizing Distortion – Narrowband Codec Mode

The signal to total distortion ratio will exceed the limits shown in Figure 21 for either path when the input signal is a sine wave with a frequency of 1014 Hz, using psophometric weighting for A-law and C-message weighting for µ-law

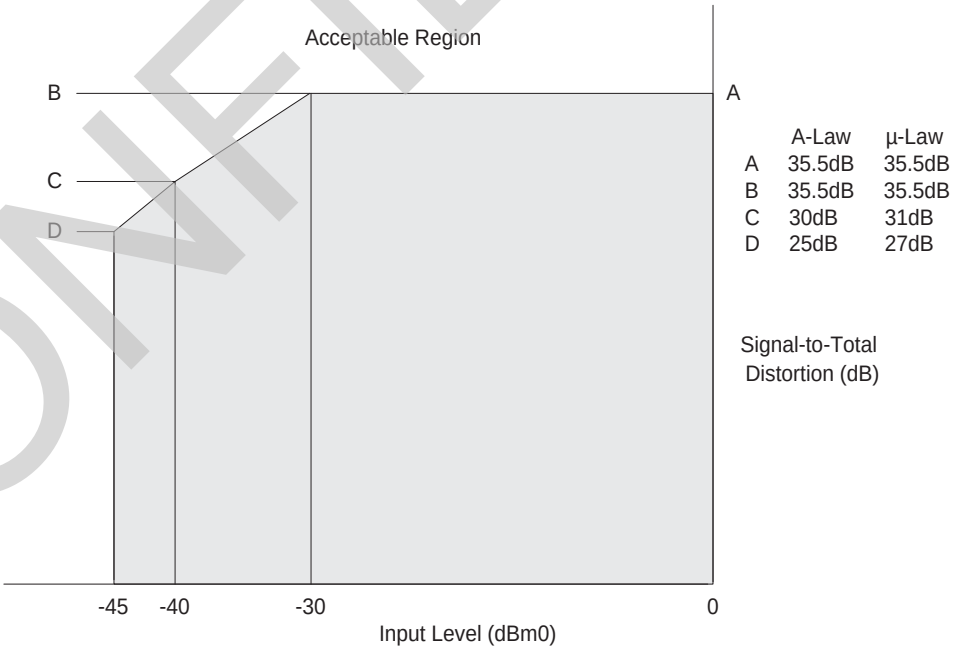


Figure 21 - Total Distortion with Tone Input (Both Paths)

5.19 Group Delay Distortion – Narrowband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in Figure 22. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0

.

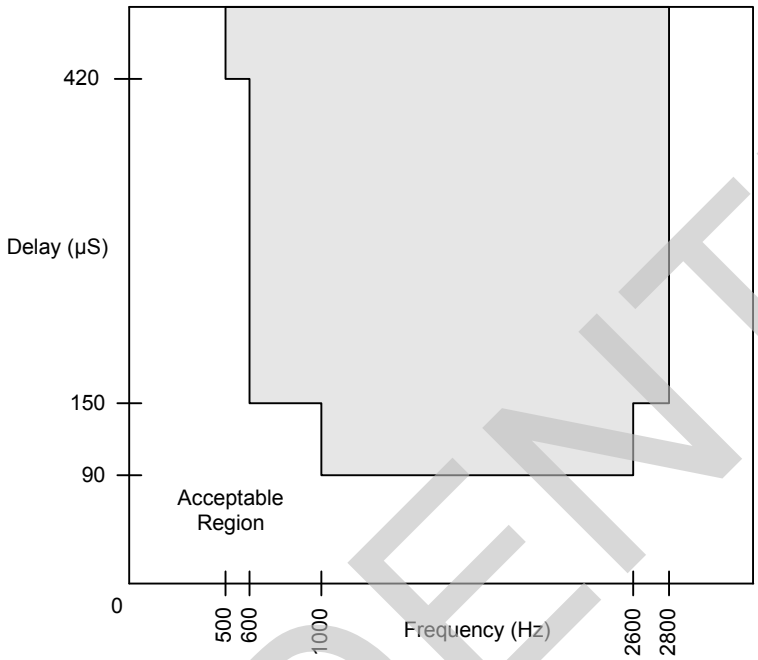


Figure 22 - Group Delay Distortion

5.20 Transmission Characteristics – Wideband Codec Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC – RAC overload level	Active state GX = AX = 0 dB	3.4			V_{PK}	*1., 2.*
Transmit level, A/D	0 dBm, GX = GX0, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, GR = GR0, 1014 Hz		0		dBm	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, off-hook	-0.5		+0.5	dB	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, on-hook	-0.5		+0.5		*1.*
Attenuation distortion	100 Hz to 6.0 kHz	-0.25		+0.25		*3.*
Single frequency distortion	0 dBm0, Linear Mode, 150 Hz to 6.8 kHz, off-hook			-50		*4.*
Signal to noise + distortion	0 dBm0, Linear Mode, 150 Hz to 6.8 kHz	50				*4.*
Second harmonic distortion, D/A	GR = 0 dB, off-hook			-55		
Idle channel noise, $V_{TIPD} - V_{RINGD}$ Digital out	Digital input = 0, linear, 0 dBr $V_{TIPD} - V_{RINGD}$ = 0 V_{AC}, linear, 0 dBr			-67 -67	dBm0p dBm0p	*1., 5.*
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			340	µs	*1., 6.*
Two-wire return loss	150 to 6800 Hz	20	26		dB	*1.*
Longitudinal to metallic balance	200 to 3400 Hz 6000 Hz	50 43			dB	*7.*
Longitudinal signal generation	300 to 3400 Hz	42				*1.*
Longitudinal current capability, per wire TIPD or RINGD	Active state	8.5			mA_{RMS}	*1.*
Longitudinal impedance at TIPD or RINGD	0 to 100 Hz, LI = 0		100		Ω/pin	*1.*
PESQ-LQ voice quality score	Linear			4.30		*1.*

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *See Figure 23 on page 41 and Figure 24 on page 41.*
4. *0 dBm0 input signal, 150 to 6800 Hz measurement at any other frequency, 150 to 6800 Hz.*
5. *No single frequency component in the range above 7600 Hz may exceed a level of -55 dBm0.*
6. *The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.*
7. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

5.21 Attenuation Distortion – Wideband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 23 and Figure 24. The reference frequency is 1014 Hz and the signal level is -10 dBm0.

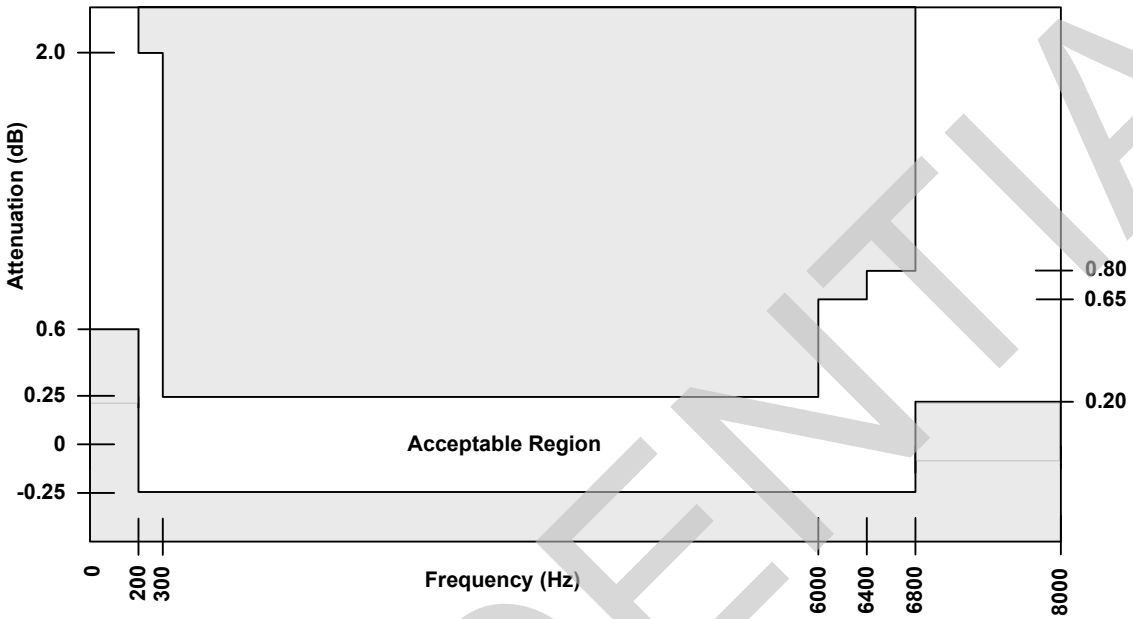


Figure 23 - Transmit (A to D) Path Attenuation vs. Frequency – (with High-Pass Filter Enabled)

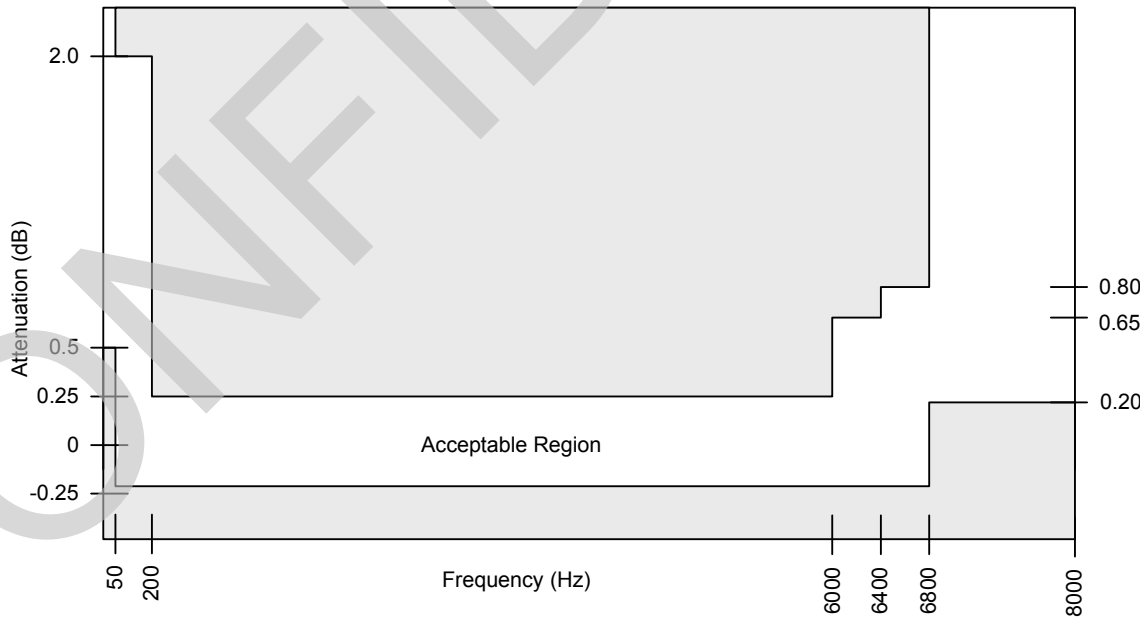


Figure 24 - Receive (D to A) Path Attenuation vs. Frequency

5.22 Group Delay Distortion – Wideband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in Figure 25. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

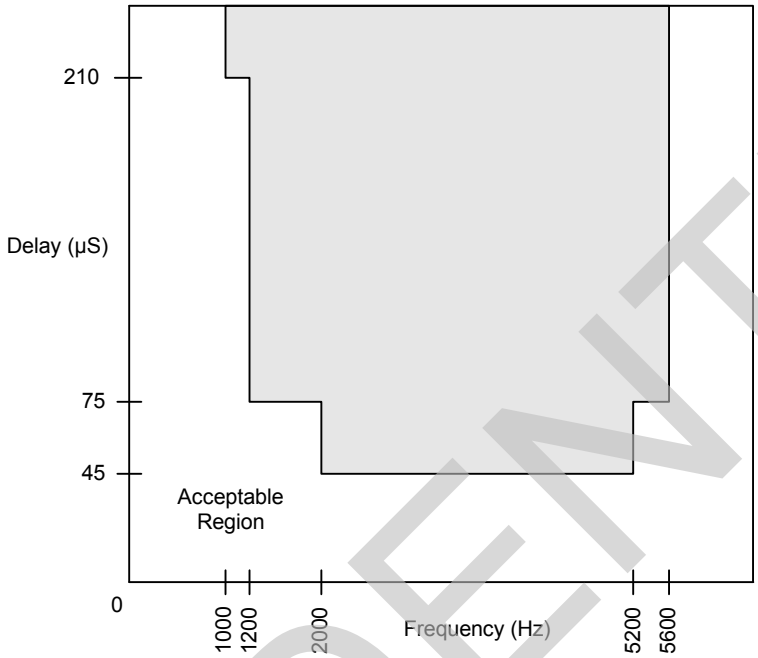


Figure 25 - Group Delay Distortion

6.0 Switching Characteristics and Waveforms

The following are the switching characteristics over operating range, unless otherwise noted. Minimum and maximum values are valid for all digital outputs with a 115 pF load.

6.1 ZSI Interface

ZCLK shall not exceed 8.192 MHz. All input setup and hold, and output delay and hold times are relative to either edge of ZCLK. Unless otherwise specified, the ZSI timing values are valid for VDDHPI = 1.8 V_{DC}, 2.5 V_{DC}, or 3.3 V_{DC}. See Figure 26 for the ZSI interface timing diagram.

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
1	t_{ZCY}	ZSI Clock (ZCLK) period	122		977	ns	*1.*
2	t_{ZCH}	ZCLK high pulse width	48				
3	t_{ZCL}	ZCLK low pulse width	48				
4	t_{ZCF}	ZCLK fall time			8		
5	t_{ZCR}	ZCLK rise time			8		
6	t_{ZSS}	ZSYNC setup time	5				*2.*
	t_{SIS}	ZMOSI slave input setup time	5				
7	t_{ZSH}	ZSYNC hold time	0				*2., 3.*
	t_{SIH}	ZMOSI slave input hold time	0				
8	t_{ZSOD}	ZMISO slave output delay	0		16		*2., 4.*
9	t_{ZST}	Allowed ZCLK or ZSYNCFS jitter time	-25		25		*2.*

Notes:

1. *The ZCLK frequency must be an integer multiple of the ZSYNC frequency. ZSYNC is expected to be an accurate 8 kHz pulse train. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If ZCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*
2. *ZSYNC, ZMOSI, and ZMISO contain dual data rate signals which are sampled or driven on both edges of the ZCLK clock.*
3. *Values shown for VDDHPI = 3.3 V. Minimum t_{ZSH} and t_{SIH} is 0.3 ns at 1.8 V and 0.2 ns at 2.5 V.*
4. *Value shown for VDDHPI = 3.3 V. Maximum t_{TZSOD} is 25 ns at 1.8 V and 18 ns at 2.5 V.*

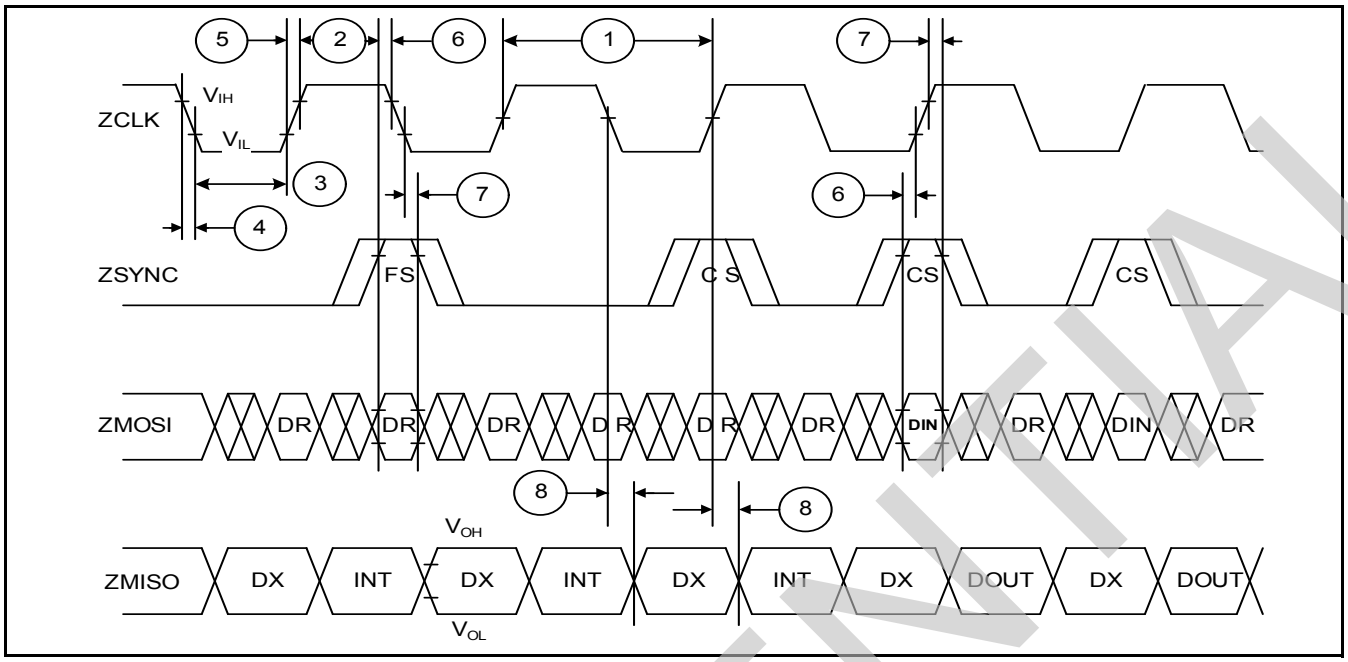


Figure 26 - ZSI Interface Timing Protocol

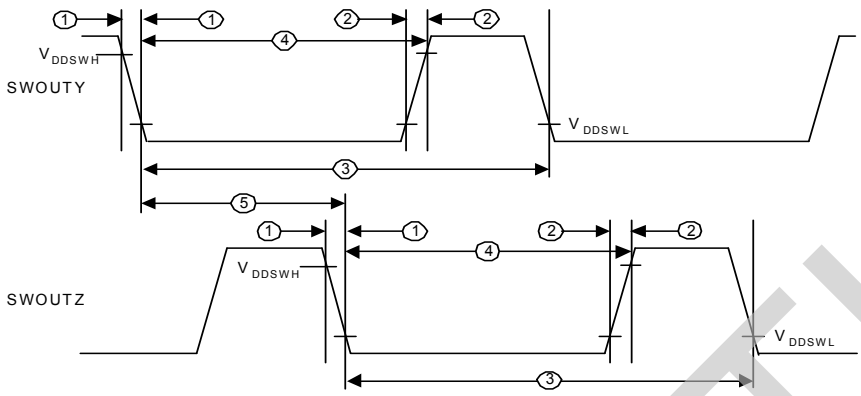
6.2 Switcher Output Timing

(See Figure 27 on page 45 for the SWOUTY, SWOUTZ timing diagram)

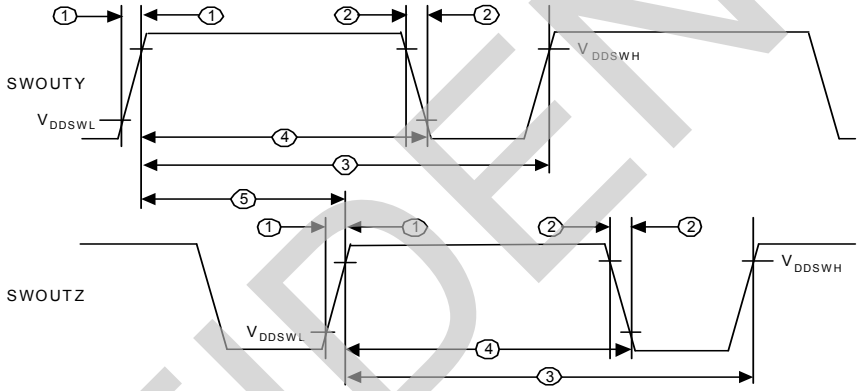
No.	Symbol	Parameter	Min	Typ	Max	Unit	Notes
1	Tfall	Output fall time		15		ns	*1.*
2	Trise	Output rise time		30			
3LP	TPeriod	Period for Low Power mode		41.667		µs	*2., 5.*
4LP	Tmax	Max on-time for Low Power mode		1.017			
3MP	TPeriod	Period for Medium Power mode		2.604			*3., 5.*
4MP	Tmax	Max on-time for Medium Power mode		1.017			
3HP	TPeriod	Period for High Power mode		1.953			*4., 5.*
4HP	Tmax	Max on-time for High Power mode		1.017			
–	Duty Cycle LP	Duty cycle Low Power mode	0	2.5		%	*2., 5.*
–	Duty Cycle MP	Duty cycle Medium Power mode	0	30.4			*3., 5.*
–	Duty Cycle HP	Duty cycle High Power mode	0	52.0			*4., 5.*
5	Y to Z offset	Delay from SWOUTZ to SWOUTY on		1.302		µs	
–		SWISY leading edge blanking period		120		ns	*6.*

Notes:

1. *Measured with a 1.5 nF load between SWOUTx and ground.*
2. *Register E6/E7h Write/Read Switching Regulator Control is loaded with Low Power mode 01h.*
3. *Register E6/E7h Write/Read Switching Regulator Control is loaded with Medium Power mode 02h.*
4. *Register E6/E7h Write/Read Switching Regulator Control is loaded with High Power mode 03h.*
5. *Timing values assume SWFS[1:0] = 00b in E4/E5h Write/Read Switching Regulator Parameters. Stated periods and on times scale inversely with frequency selected.*
6. *This is a programmable setting with the default value shown here. The value should be programmed to 0x01 (81 ns). This is automatically done by Profile Wizard.*



Flyback Mode (Representative of High Power Setting)



Inverting Buck-Boost Mode (Representative of High Power Setting)

Figure 27 - Switcher Output Waveform SWOUTY, SWOUTZ

7.0 Device Pinout

The pins of the Le9662 device are listed and described in this section. Note that there are no ground pins. All ground connections inside this device are made through the exposed pad.

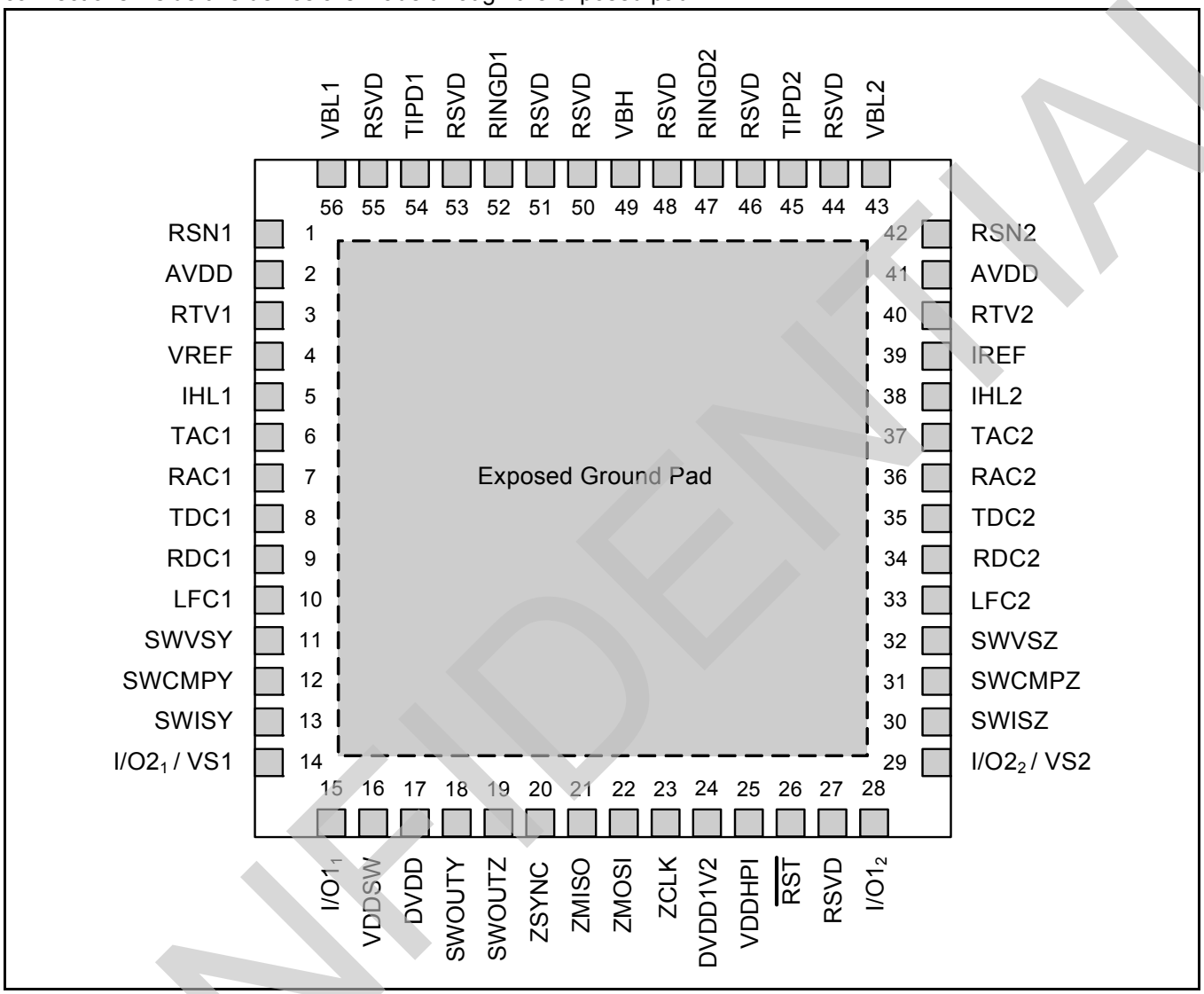


Figure 28 - Le9662 Device Pinout (56-Pin QFN) – Top View

Name	Type	Description
AVDD/DVDD	Power	3.3 V Analog and digital power supply inputs. AVDD and DVDD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VDD power supply pins should be connected together at the power supply or power connection to the printed circuit board.
DVDD1V2	Output	Internally generated 1.2 V supply. Connect a 0.1 µF ceramic decoupling capacitor between this pin and ground.
IHL_1,IHL_2	Output	High Level Current Drive Filter.
$I/O1_1$, $I/O1_2$	I/O	General Purpose Input/ Output 1 on Channels 1 and 2, respectively. Each of these two I/O's is capable of driving a 150 mW, 3 V relay (external catch diode required) or an LED, sinking up to 70 mA.
$I/O2_1$ / VS1	I/O or Input	General Purpose Input/ Output 2 on Channel 1 or Voltage Sense 1. When configured as a voltage sense input, connect a 1.0 MΩ 1% resistor between this pin and the voltage to be monitored. The maximum working voltage rating of the resistor must be higher than the monitored voltage.
$I/O2_2$ / VS2	I/O or Input	General Purpose Input/ Output 2 on Channel 2 or Voltage Sense 2. When configured as a voltage sense input, connect a 1.0 MΩ 1% resistor between this pin and the voltage to be monitored. The maximum working voltage rating of the resistor must be higher than the monitored voltage.
IREF	Input	Current Reference. An external resistor R_{REF} connected between this pin and analog ground generates an accurate current reference used by the analog circuits on the chip.
LFC_1,LFC_2	Output	Connection for longitudinal filter capacitor.
RAC_1,RAC_2	Input	Ring lead AC sense. A series R + C network is connected from this pin to the Ring lead.
RDC_1,RDC_2	Input	Ring lead DC Sense. A resistor is connected from this pin to the Ring lead. The connection can be to either side of the protection resistor.
$RINGD_1$, $RINGD_2$	Output	RING-lead (B) output to the two-wire line.
RSN_1, RSN_2	Input	High voltage line drive receive current summing node for each channel.
$\overline{RST}$	Input	Device Hardware Reset. A logic Low signal at this pin resets the device to its default state.
RSVD	Open	Reserved. Make no connection to these pins.
RTV_1, RTV_2	Output	Drive output for two-wire AC impedance scaling resistor.
SWCMPY, SWCMPZ	Output	Compensation connection for switching regulator controller.
SWISY, SWISZ	Input	Current sense input for switching regulator controller.
SWOUTY, SWOUTZ	Output	Pulse output for gate drive to switching regulator FET.
SWVSY, SWVSZ	Input	Voltage sense for switching regulator controller.
TAC_1,TAC_2	Input	Tip lead AC Sense. A series R + C network is connected from this pin to the Tip lead.
TDC_1,TDC_2	Input	Tip lead DC Sense. A resistor is connected from this pin to the Tip lead. The connection can be to either side of the protection resistor.
$TIPD_1$, $TIPD_2$	Output	TIP-lead (A) output to two-wire line.
VBH	Supply	High Negative Battery Supply. Used for on-hook, on-hook transmission (OHT), and ringing states.
VBL_1, VBL_2	Supply	Low Negative Battery Supply, channel 1 and channel 2. Used for off-hook states.
VDDHPI	Power	Digital power supply input for ZSI pins. Place a 0.1 µF ceramic decoupling capacitor between this pin and ground.

VDDSW	Power	This supply is used to drive the switching regulator. For FBABS operation, this supply is used to drive the MOSFETs on the external switcher circuit, enable the internal pump charge circuit to generate ~ 4.7 V_{DC}. For BBABS operation, connect this pin to DVDD. For both modes of operation, place a ceramic decoupling capacitor between this pin and ground. To avoid stressing this pin, ensure that VDDSW is never hard tied to ground at any time, including during power up and power down cycles.
VREF	Output	Analog Voltage Reference. The VREF output has an external 10 µF ceramic capacitor connected to ground, filtering noise present on the internal voltage reference.
ZCLK	Input	ZSI Data Clock 1.024 to 8.192 MHz. This is the clock for the ZSI interface.
ZMISO	Output	ZSI Data Output. Multiplexed PCM voice and control data is written serially out of the device through this pin, most significant bit first. ZCLK determines the data rate.
ZMOSI	Input	ZSI Data Input. Multiplexed PCM voice and control data is written serially into the device though this pin, most significant bit first. ZCLK determines the data rate.
ZSYNC	Input	Interface synchronization signal for multiplexed PCM voice and control channels.
Exposed Ground Pad (EPAD/GND)	Power	Thermal Pad and Circuit Ground. Connect to a ground plane on the printed circuit board for thermal conduction and electrical connection to ground return. This is the only ground connection on the device.

8.0 Application Information

8.1 FBABS and BBABS Line Interface Circuit

Figure 29 shows a typical line interface circuit for the Le9662 when the switching regulator circuit is configured for Automatic Battery Switching or Buck-Boost Automatic Battery Switching. Decoupling, filtering, reference generation components, and per channel protection are shown.

The parts list for this circuit is shown in "FBABS/BBABS Line Interface Circuit Bill of Materials" on page 50. The FBABS switching regulator circuit is detailed in Figure 30 and the BBABS switching regulator circuit is detailed in Figure 31. Consult Microsemi for the most recent reference design.

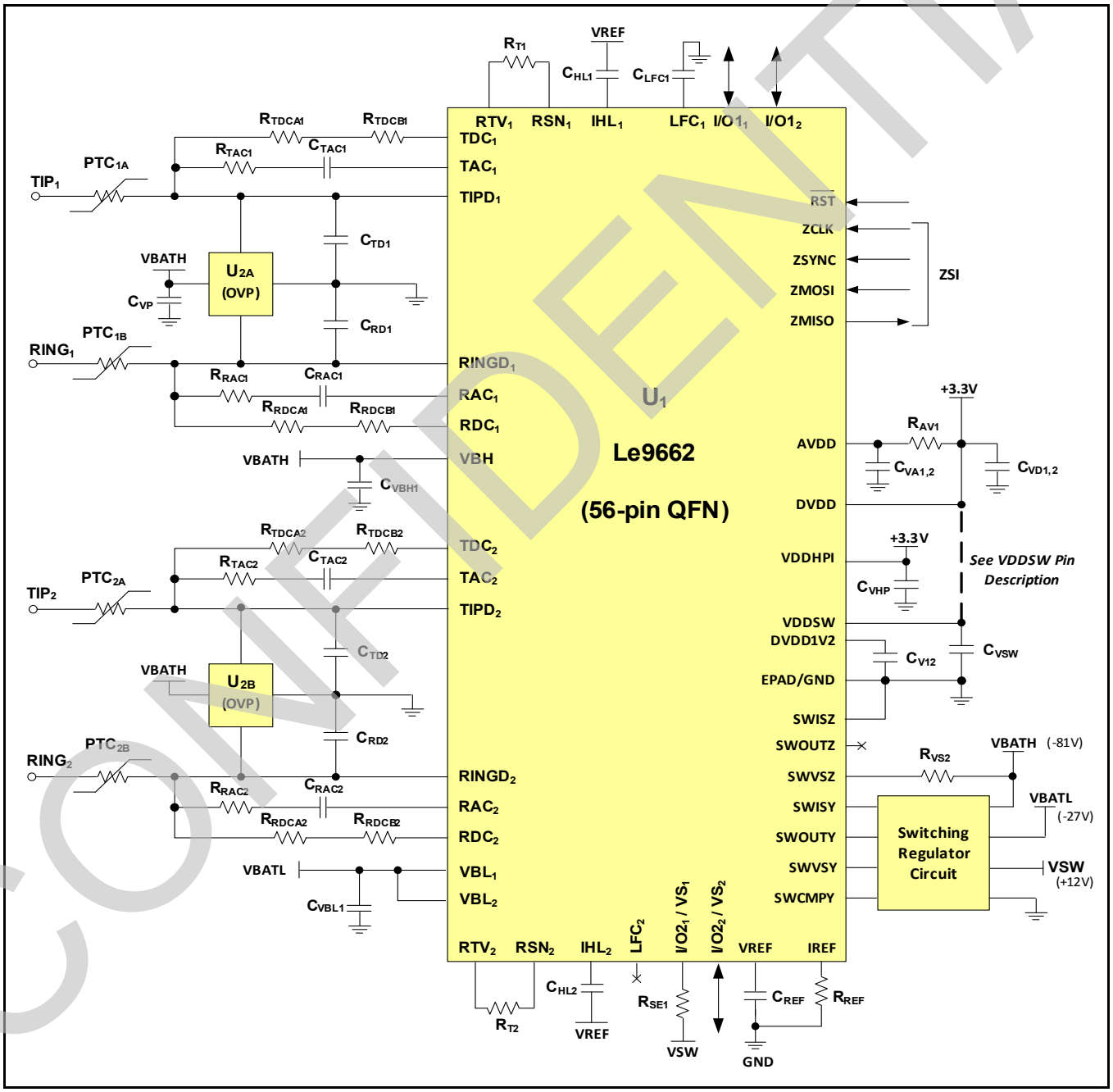


Figure 29 - Le9662 FBABS/BBABS Line Interface Circuit

8.2 FBABS/BBABS Line Interface Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Note
4	C_{HL1}, C_{HL2}, C_{VA1}, C_{VD1}	Ceramic Capacitor	4.7 µF, X5R	20%	6.3 V	0603	
3	C_{LFC1}, C_{V12}, C_{VA2}	Ceramic Capacitor	0.1 µF, X7R	10%	16 V	0402	
8	C_{RAC1}, C_{RAC2}, C_{RD1}, C_{RD2}, C_{TAC1}, C_{TAC2}, C_{TD1}, C_{TD2}	Ceramic Capacitor	0.022 µF, X7R	10%	100 V	0603 or 0805	*1.*
1	C_{REF}	Ceramic Capacitor	10 µF, X5R	10%	6.3 V	0805	
1	C_{VBH1}	Ceramic Capacitor	0.01 µF, X7R	20%	250 V	0805	
1	C_{VBL1}	Ceramic Capacitor	0.01 µF, X7R	10%	50 V	0603	
2	C_{VD2}, C_{VHP}	Ceramic Capacitor	0.01 µF, X7R	10%	16 V	0402	
1	C_{VP}	Ceramic Capacitor	0.1 µF, X7R	10%	100 V	0805	*1.*
1	C_{VSW}	Ceramic Capacitor	0.047 µF, X7R	10%	16 V	0402	
2	P_{TC1}, P_{TC2}	Dual Matched PTC Thermistors	7 Ω, 0.13 A Hold	20%	250 V_{RMS} / 3A		*2., 3.*
1	R_{AV1}	Resistor	1.0 Ω	5%	1/10 W	0603	
4	R_{RAC1},R_{RAC2}, R_{TAC1}, R_{TAC2}	Resistor	10 KΩ	1%	150 V	0805	
8	R_{RDCA1},R_{RDCA2}, R_{RDCB1},R_{RDCB2}, R_{TDCA1}, R_{TDCA2}, R_{TDCB1}, R_{TDCB2}	Resistor	499 KΩ	1%	200 V	1206	
1	R_{REF}	High-Precision Thin Film Resistor	75.0 KΩ	0.5%, 25ppm	1/16 W	0402	*4.*
1	R_{SE1}	Resistor	1.0 MΩ	1%	50 V	0402	*5.*
2	R_{T1}, R_{T2}	Resistor	47.5 KΩ	1%	1/16 W	0402	
1	R_{VS2}	Resistor	1.00 MΩ	1%	150 V	0805	
1	U_1	IC, miSLIC™	*Microsemi Le9662*		-100 V/-120 V	QFN-56	
1	U_2	IC, Programmable Quad Channel SLIC Protector	*Bourns TISP61089Q* or *TISP6NTP2C*, *STMicro LCDP1521S*		-150 V/30 A	SOIC-8	*2.*

Notes:

1. *For designs with ≥ 70 V_{PK} maximum ringing, the rating of these capacitors should be increased to 200 V or 250 V.*
2. *Protection components depend on the target application. The components on the BOM are believed to be suitable for ITU-T Recommendation K.21 (Basic Level) and Telcordia GR-1089-CORE Intra-Building compliance. Please check with Microsemi for component selection for other safety or EMC standards.*
3. *Recommended dual PTCs include Bourns CMF-SDP07 or MF-SD013/250.*
4. *The tolerance and stability of this resistor are critical as they affect calibration and measurement accuracy. Microsemi recommends using resistors with 0.5% tolerance and 25 ppm/°C temperature coefficient for most applications. Examples include Susumu RR0510P-753-D, Panasonic ERA-2AED753X, and Yageo RT0402DRD0775KL. For high-performance applications, 0.1% 25 ppm/°C resistors such as Panasonic ERA-2AEB753X or Yageo RT0402BRD0775KL are recommended.*
5. *Populate only to sense the voltages shown on the schematic. Always make sure that these resistors are selected so that their maximum working DC voltage rating is more than the desired sensed voltage.*

8.3 Shared FBABS Switching Regulator Circuit

The FBABS switching regulator circuit uses a flyback switcher architecture that regulates off of the low battery supply. Consult Microsemi for the most recent reference design.

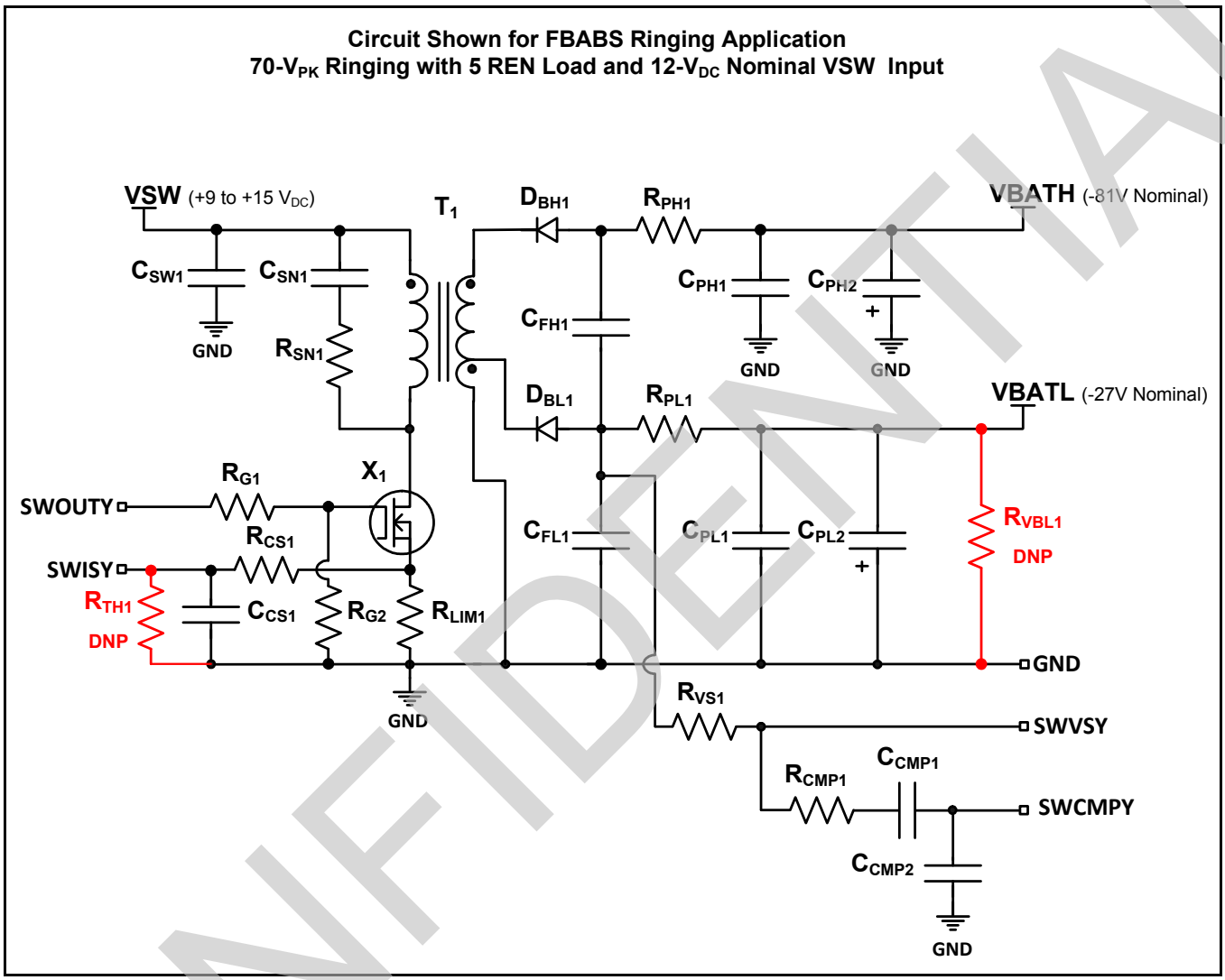


Figure 30 - FBABS Switching Regulator Circuit

8.4 Shared FBABS Switching Regulator Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Part Number / Note
1	C_{CMP1}	Ceramic Capacitor	0.01 µF, X7R	10%	25 V	0402	
2	C_{CMP2}, C_{CS1}	Ceramic Capacitor	220 pF, X7R	10%	50 V	0402	
1	C_{FH1}	Ceramic Capacitor	1.0 µF, X7R or X7S	20%	100 V	0805 or 1206	*1.*
1	C_{FL1}	Ceramic Capacitor	2.2 µF, X5R or X7R	10%	50 V	1206	
1	C_{PH1}	Ceramic Capacitor	0.1 µF, X7R or X7T	20%	100 V	0805 or 1206	*1.*
1	C_{PH2}	Electrolytic Capacitor	0.47 µF, 105°C	20%	160 V	6.3x11mm	
1	C_{PL1}	Ceramic Capacitor	1.0 µF, X7R	20%	50 V	0805	
1	C_{PL2}	Electrolytic Capacitor	1.0 µF, 105°C	20%	50 V	5x11 mm	Optional
1	C_{SN1}	Ceramic Capacitor	470 pF, X7R	20%	100 V	0603	
1	C_{SW1}	Ceramic Capacitor	10 µF, X5R or X7R	20%	25 V	1206	
2	D_{BH1}, D_{BL1}	Ultra-Fast Recovery Rectifier	t_{rr} ≤ 50 nS		1 A/ 400 V	SMA	*ES1G, US1G*, or equivalent
1	R_{CMP1}	Resistor	402 KΩ	1%	1/16 W	0402	
1	R_{CS1}	Resistor	1.00 KΩ	1%	1/16 W	0402	
1	R_{G1}	Resistor	4.7 Ω	5%	1/16 W	0402	
1	R_{G2}	Resistor	10 KΩ	5%	1/16 W	0402	
1	R_{LIM1}	Current Sense Resistor	0.02 Ω	1%	1/2 W	1206	*Yageo PF1206FRF070R02* or equivalent
2	R_{PH1}, R_{SN1}	Resistor	20 Ω	5%	1/4 W	1206	
1	R_{PL1}	Resistor	10 Ω	5%	1/4 W	1206	
1	R_{TH1}	Resistor	TBD	1%	1/16 W	0402	Do not populate
1	R_{VBL1}	Resistor	100 KΩ	5%	1/10 W	0603	Do not populate
1	R_{VS1}	Resistor	1.00 MΩ	1%	150 V	0805	
1	T_1	Flyback Transformer	2.0 µH, 1:10 Turns Ratio			EP7 or EE8.8	*UMEC TG-UTB02071s* or *TG-UTB02072s, Sumida C8800*, or *C8900* [2]
1	X_1	N-Channel MOSFET, Logic Level, Avalanche-Rated	$R_{DS\ (ON)}$ ≤ 100 mΩ, $Q_{G(tot\ max)}$ @ (V_{GS}=4.5V) ≤ 12 nC , I_{AR} > *10A*, E_{AR} > *1 mJ*		≥ 3.5 A/ 30 V	SOIC-8	*Alpha & Omega AO4466, Analog Power AM6612N, Diodes DMG4466SSS-13, Fairchild FDS6612A*, or equivalent

Notes:

1. *For designs with ≥ 70 V_{PK} maximum ringing, these capacitors should be rated at or 200 V or 250 V.*
2. *EP7 transformers are smaller, while EE8.8 transformers tend to be less expensive. Note that pin 1 location may vary between transformers.*

8.5 Shared BBABS Switching Regulator Circuit

The BBABS switching regulator circuit uses an inverting buck-boost inductor based architecture with voltage doubler that regulates off of the low battery supply. Consult Microsemi for the most recent reference design.

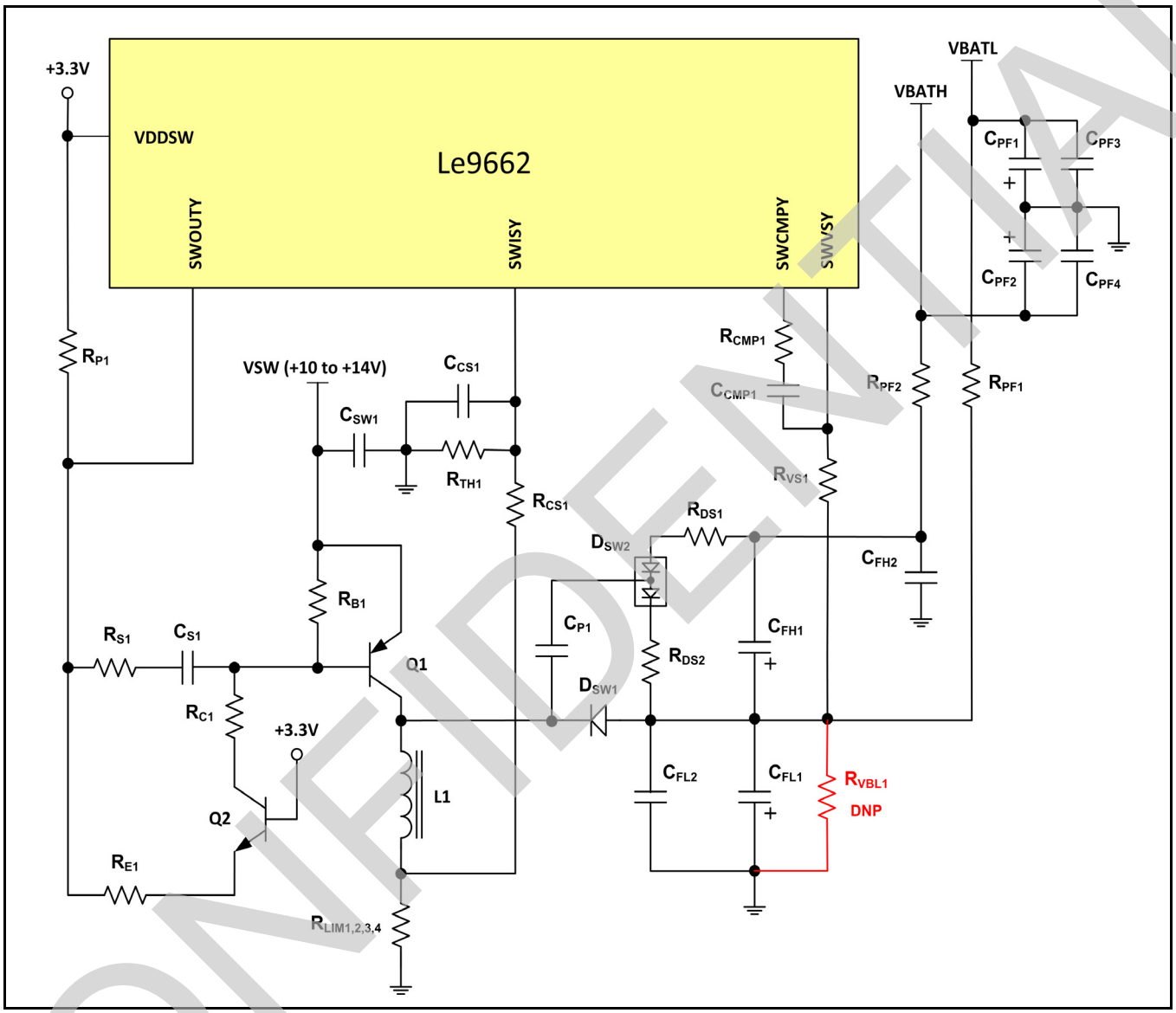


Figure 31 - BBABS Switching Regulator Circuit

8.6 Shared BBABS Switching Regulator Circuit Bill of Materials

Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
1	C_{CMP1}	Ceramic Capacitor	0.0022 µF, X7R	10%	16 V	0402	
1	C_{CS1}	Ceramic Capacitor	220 pF, X7R	10%	25 V	0402	
2	C_{FH1}, C_{FL1}	Electrolytic Capacitor	22 µF	20%	63 V		
2	C_{FH2}, C_{PF4}	Ceramic Capacitor	0.1 µF, X7R	10%	100 V	0805	
2	C_{FL2}, C_{PF3}	Ceramic Capacitor	0.1 µF, X7R	10%	50 V	0603	
1	C_{P1}	Ceramic Capacitor	0.22 µF, X7R	10%	100 V	0805	
1	C_{PF1}	Electrolytic Capacitor	2.2 µF	20%	50 V		
1	C_{PF2}	Electrolytic Capacitor	1.0 µF	20%	100 V		
1	C_{S1}	Ceramic Capacitor	0.1 µF, X7R	10%	25 V	0603	
1	C_{SW1}	Electrolytic Capacitor	220 µF, Low ESR	20%	25 V		
1	D_{SW1}	Ultrafast Diode	ES1B		100 V, 1.0 A		
1	D_{SW2}	Dual Diode	BAV23S		200 V, 0.2 A	SOT23	*1.*
1	L1	Power Inductor	47 µH	20%	1.5 A		
1	Q_1	Transistor	PNP, Low Vce, *ZXTP2013G Diodes Inc.® or equivalent*		100 V	SOT223	
1	Q_2	Transistor	NPN, *MMBT3904 Diodes Inc.® or equivalent*			SOT23	
1	R_{B1}	Resistor	1 KΩ	5%	1/16 W	0402	
2	R_{C1}, R_{E1}	Resistor	75 Ω	5%	1/10 W	0603	
1	R_{CMP1}	Resistor	1.0 MΩ	1%	1/16 W	0402	
1	R_{CS1}	Resistor	3.01 KΩ	1%	1/16 W	0402	
2	R_{DS1}, R_{PF2}	Resistor	10 Ω	5%	1/4 W	1206	
2	R_{DS2}, R_{PF1}	Resistor	5.1 Ω	5%	1/4 W	1206	
4	R_{LIM1}, R_{LIM2}, R_{LIM3}, R_{LIM4}	Resistor	1.0 Ω	5%	1/16 W	0402	
1	R_{P1}	Resistor	10 KΩ	5%	1/16 W	0402	
1	R_{S1}	Resistor	0 Ω	5%	1/16 W	0402	
1	R_{TH1}	Resistor	1 KΩ	1%	1/16 W	0402	
1	R_{VBL1}	Resistor	51 KΩ	5%	1/10 W	0603	Do not populate
1	R_{VS1}	Resistor	1.0 MΩ	1%	1/8 W	0805	

Notes:

1. Repetitive peak forward surge current rating of 600 mA.

9.0 Programming the Le9662

The Le9662 device is programmed through the *VoicePath Application Program Interface II (VP-API-II).* This API hides the complexity of the device and its internal registers and provides a much simpler interface to the software engineer. The *VP-API-II* allows for rapid development on proven software that is currently used to control over 100 million subscriber lines worldwide.

9.1 Programmable Features

- AC and DC coefficient programming
- Ringing parameter (amplitude, frequency, bias, type) and power management
- Tone generation (frequency, amplitude, and modulation)
- Programmable tone and ringing cadence
- Universal Caller ID generation (Types 1 and 2) with FSK and DTMF signaling
- Loop start signaling, including dial pulse detection
- Ground start signaling
- Seamless integration of the Microsemi *VeriVoice Professional Test Suite Software* for *Telcordia® GR-909-CORE* metallic loop testing
- Three modes of interrupt support (Level Triggered, Efficient Polling and Simple Polling)

9.2 VoicePath API-II Software Overview

The *VP-API-II* is an OS independent, C source library that abstracts the Microsemi ZL880, VE790, VE880, VE890 and miSLIC™ device registers into a common application interface used for configuration and control of the devices.

Two versions of the *VP-API-II* are available from the Microsemi Software Delivery System (SDS) web site – http://sds.microsemi.com/software.php. The first version of the software (*LE71SK0002*) contains the full software source and requires a Software License Agreement (SLA). The second version of the software (*LE71SDKAPIL*) called *VP-API-II Lite* is a subset of the full *VP-API-II* source and allows for basic configuration, control and event handling of the devices. The *Lite* version does not include Caller ID generation, tone or ringing cadence support. *VP-API-II Lite* does not require an SLA and is suitable for open-source applications. The miSLIC device is supported by *VP-API-II* versions 2.22.0 and later.

The following sections cover the more commonly used aspects of the *VP-API-II*. See the *VoicePath API-II Reference Guide (Doc ID #143271)* for complete coverage of this software.

9.2.1 Introduction

The Microsemi V*oicePath Application Programming Interface II* (*VP-API-II*) is a C source code module that provides a standard software interface for controlling, testing, and passing digitized voice through a set of subscriber lines using the Microsemi family of voice termination devices. This section describes a few of the device and line control capabilities using the *VP-API-II* interface. For a complete list, refer to *VP-API-II Reference Guide*. *VP-API-II* uses the layered architecture shown in Figure 32. The portion of the diagram in white is Microsemi-provided code, while the gray portions are customer-provided.

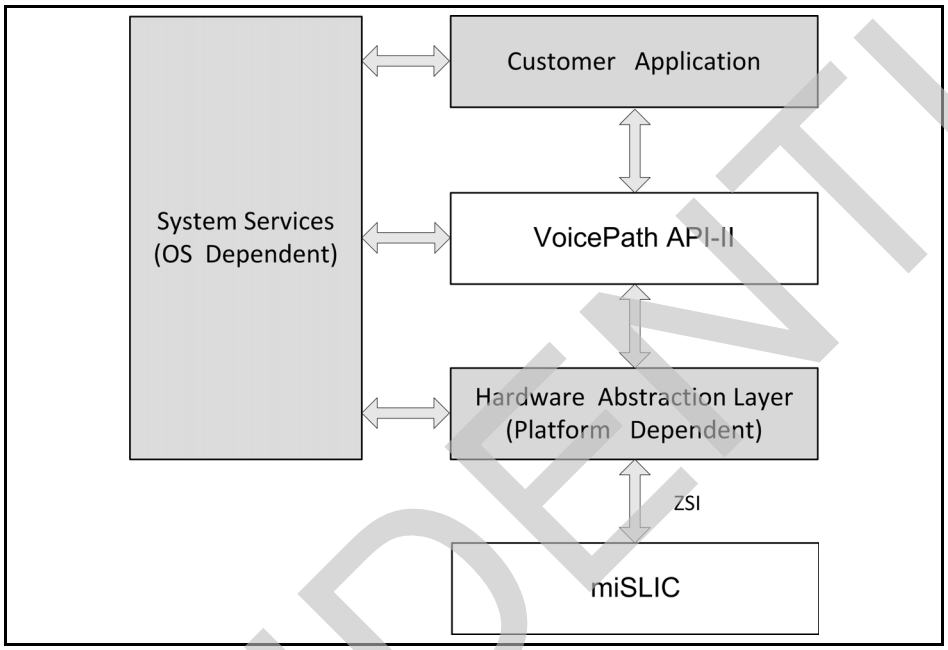


Figure 32 - VP-API-II Software Architecture

9.2.2 Customer Application

This block represents the user's line management module that performs tasks such as initializing the system, configuring lines, changing the line states in response to line events and other inputs, switching digitized voice traffic, etc. Microsemi provides example implementations of this layer as part of the *VoicePath SDK*.

9.2.3 VoicePath API-II

The *VoicePath API-II* is the core component of the Microsemi *VoicePath SDK*. This software module runs on the host microprocessor that controls one or more Microsemi voice telephony devices. This code is provided by Microsemi and should not require modification by the application developer.

9.2.4 Hardware Abstraction Layer

The Hardware Abstraction Layer (HAL) provides access to Microsemi voice telephony devices through the multiplexed ZSI interface. The HAL software is platform-dependent and must be implemented by the *VP-API-II* user. Microsemi provides example HAL source code with the *VoicePath SDK*.

9.2.5 System Services Layer

The System Services layer provides critical section, timing and interrupt control functions. These functions are system-dependent and must be implemented specifically for each platform on which the *VP-API-II* is used. Microsemi provides example System Services code for use with the Microsemi *ZTAP*. The following functions are included in the System Services layer.

Function Name	Description
`VpSysEnterCritical()`	A semaphore operation to provide protected access to device or shared memory. Required only in multi-threaded architectures.
`VpSysExitCritical()`	A semaphore operation to release protected access to device or shared memory. Required only in multi-threaded architectures.
`VpSysWait()`	Delay operator used to suspend program/thread execution. Delay parameter passed in 125 µs steps.
`VpSysDebugPrintf()`	Print mechanism used by *VP-API-II* debug features.
`VpSysTestInt()`	Interrupt function for Efficient Poll Mode. Required for backward compatibility with *VE880* code.

Table 7 - VP-API-II Functions for System Services

9.3 System Configuration Functions

Two main functions in *VP-API-II* are required in all applications are listed below:

Function Name	Description
`VpMakeDeviceObject()`	Configures a specific device (chip select) to a device context. Provides *VP-API-II* with device specific type (*`deviceType`*).
`VpMakeLineObject()`	Configures a specific line (channel) to a line and device context. Provides *VP-API-II* with line specific type (*`termType`*).

Table 8 - VP-API-II Functions for System Configuration

When using the Le9662 device, the following settings must be used:

- The value for *`deviceType`* in `VpMakeDeviceObject()` must be: `VP_DEV_960_SERIES`
- The value for *`termType`* in `VpMakeLineObject()` must be:
  - `VP_TERM_FXS_GENERIC` when *`channelId`* = 0 and Normal Standby operation is desired
  - `VP_TERM_FXS_LOW_PWR` when *`channelId`* = 0 and Low Power Standby operation is desired.

Please refer to *VP-API-II Reference Guide* for additional details.

9.4 Initialization

The *VP-API-II* functions that perform initialization are listed below.

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in the specified *Profiles*.
`VpInitLine()`	Resets and initializes line with parameters defined in the specified *Profiles*.
`VpInitRing()`	User function to provide Ringing Cadence. Also allows use selection of *Caller ID Profile* associated with ringing.

9.5 Line State Control

The Signaling Control blocks process the Line State information to perform related control functions such as DC feed, ringing generation, and line test for each channel.

Fifteen system states are possible for the operation of the FXS channel on the Le9662: VP_LINE_DISABLED, VP_LINE_DISCONNECT, VP_LINE_STANDBY, VP_LINE_TIP_OPEN, VP_LINE_OHT, VP_LINE_ACTIVE, VP_LINE_TALK, VP_LINE_RINGING, VP_LINE_HOWLER, and corresponding reverse polarity of each state.

Function Name	Description
VpSetLineState()	Sets line to state specified. After VpInitDevice() or VpInitLine(), the default line state is VP_LINE_DISCONNECT.

Table 9 - VP-API-II Functions for Line State Control

9.5.1 VP_LINE_DISABLED

VP_LINE_DISABLED is the power-up and hardware reset state of the device. The System State register is in *Shutdown*, the voice channel is deactivated and the switching regulator is off. No transmission or signaling is possible. This state can also be entered due to certain fault conditions such as battery overvoltage or clock fault.

9.5.2 VP_LINE_DISCONNECT

In the VP_LINE_DISCONNECT state, the SLIC block outputs are shut off providing a high impedance to the line. This state can be used for denial of service. The switching regulator is active and outputs the programmed SWFV floor voltage. The voice channel is normally deactivated, but can be activated and used with the converter configuration command to monitor the voltages on Tip or Ring for line diagnostics.

9.5.3 VP_LINE_STANDBY

The VP_LINE_STANDBY state is used when On-Hook. This state behaves differently based on the FXS line termination type selected according to "System Configuration Functions" on page 57.

If the termination type VP_TERM_FXS_GENERIC is selected, the DC feed is active, and hook supervision functions are enabled. The loop feed polarity is controlled by the *VP-API-II*. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed curve shown in Figure 11, "Active State I / V Characteristic" on page 17. The DC feed drives Tip and Ring to the programmed VOC. Voice transmission is disabled to save power.

If the termination type VP_TERM_FXS_LOW_PWR is selected, a special *Low Power Idle Mode (LPIM)* state is supported to reduce on-hook power consumption, while still being able to detect off-hook transitions. In this mode, the DC feed is not active and a voltage is presented to the Ring lead. The line voltage is monitored so that any transitions to off-hook state can be detected. Voice transmission is disabled in this state.

9.5.4 VP_LINE_OHT

In the VP_LINE_OHT states, the DC feed is activated and voice transmission is enabled. VP_LINE_OHT allows the transmission of Caller ID information. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

9.5.5 VP_LINE_ACTIVE, VP_LINE_TALK

In the VP_LINE_ACTIVE and VP_LINE_TALK states, the DC feed is activated. The PCM highway is enabled in VP_LINE_TALK and disabled in VP_LINE_ACTIVE. Both states allow the transmission of Caller ID information for Type 2 Caller ID. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

9.5.6 VP_LINE_TIP_OPEN

In the VP_LINE_TIP_OPEN state, the device provides a high impedance on the Tip lead and drives the Ring lead to the programmed VOC voltage. The loop supervision detector monitors the ground key current. When this current is larger than the programmed threshold, the *VP-API-II* reports a ground start event. This state can also be used to determine Ring to ground leakage and Ring to ground capacitance in combination with the appropriate converter configuration.

9.5.7 VP_LINE_RINGING

In the VP_LINE_RINGING state, the voice DAC is used to apply the ringing signal generated from Signal Generator A and the Bias generator to the SLIC block. Internal feedback maintains a low (200 Ω) system output impedance during ringing. The current limit is increased in the *Ringing* state and is programmable via the parameter, ILR. In order to minimize line transients, entry and exit from the VP_LINE_RINGING states are intelligently managed by the Le9662. When ringing is requested by the user, the corresponding signal generators are started but not applied to the subscriber line until the ringing voltage is equal to the on-hook Tip-Ring voltage. This algorithm, known as *Ring Entry*, assures that there is a smooth line transition when entering the VP_LINE_RINGING state. *Ring Entry* is guaranteed to occur within one period of the programmed ringing frequency. *Ring Exit i*s an analogous procedure whereby the ringing signal is not immediately removed from the line after a ring trip or new state request. The ringing signal will persist until its voltage is equal to the required line voltage. Ring Entry and Ring Exit are configured using the *VP-API-II* option VP_OPTION_ID_RING_CNTRL.

While in the VP_LINE_RINGING state, the integrated switching regulator may be programmed. See “Device Profile” on page 64 and “Ringing Profile” on page 67 for information on setting the switcher topology.

9.5.8 VP_LINE_HOWLER

In the VP_LINE_HOWLER state, the transmit (A to D) voice path and impedance generation are disabled. Gain is increased by 11.5 dB compared to a 0 dBr D/A setting.

9.6 Line Status Monitoring

Line status is monitored by the *VP-API-II* using the functions listed in Table 10.

Function Name	Description
VpGetEvent()	Typically used to implement event driven method to monitor line status. Provides event queue such that a single event reported for each instance function is called (when an event is active).
VpGetLineStatus()	Typically used to implement polling method to monitor line status.
	• VP_INPUT_HOOK -- Hook Status timing per Dial Pulse Detection.
	• VP_INPUT_RAW_HOOK -- Real time hook status. Changes during Dial Pulse
	• VP_INPUT_GKEY -- Real time ground key status.

Table 10 - VP-API-II Functions for Line Status Monitoring

9.7 Input / Output Control

The Le9662 device features four general purpose I/O pins that can be configured by the user as inputs, outputs, or relay drivers. All I/O pins are configured and accessed through the *VP-API-II* using the functions listed in Table 11

Function Name	Description
VpSetOption()	VP_DEVICE_OPTION_ID_DEVICE_IO - Used to configure pins individually as input, output, or as a voltage sense pin. Parameter directionPins_31_0 used to set pin as input (0) or output (1). Bit in directionPins_31_0 corresponding to I/O is ($I/O1_1$ = 0x1, $I/O1_2$ = 0x2, $I/O2_1$ = 0x4, and $IO2_2$ = 0x8). Other bits in directionPins_31_0 are ignored. Configuring output type done by setting corresponding bit location in outputTypePins_31_0 with VP_OUTPUT_DRIVEN_PIN (driven). Note that when writing a '1' to a driven pin results in voltage being present on the corresponding I/O pin.
VpGetOption()	VP_DEVICE_OPTION_ID_DEVICE_IO - Retrieves current I/O pin configuration. When calling VpGetOption(), an event (Response Category, Event ID VP_LINE_EVID_RD_OPTION) is generated and must be processed by the host application. Host application then calls VpGetResults() with pointer to structure of type VpOptionDeviceIoType that is filled in by *VP-API-II* with current I/O configuration data.
VpDeviceIoAccess()	Parameter *accessMask_31_0* provides bit field access to the I/O pins as ($I/O1_1$ = 0x1, $I/O1_2$ = 0x2, $I/O2_1$= 0x4, and $IO2_2$ = 0x8). Access is by 'OR' combination, so *accessMask_31_0* = 0x0F provides access to all lines simultaneously. The accessType parameter indicates read (VP_DEVICE_IO_READ) or write (VP_DEVICE_IO_WRITE) operation. For write operation, deviceIOData_31_0 is used to set lines to '0' or '1'. Bit mask is same as accessMask_31_0 ($I/O1_1$ is set to value in *deviceIOData_31_0* location 0x1, $I/O1_2$ in deviceIOData_31_0 location 0x2, and so on). All other parameters (accessMask_63_32 and deviceIOData_63_32) are ignored for the Le9662)

Table 11 - VP-API-II Functions for Configuring and Accessing I/O Lines

9.8 VoicePath API-II Software QuickStarts

Both versions of the *VP-API-II* software are distributed with minimalistic examples known as QuickStarts. These examples are intended to provide *VP-API-II* users with a starting point for their end application. The QuickStarts show how to properly setup, initialize, and configure the VP-API. Additionally, the examples show how to properly respond to VP-API events. The QuickStarts code also provide examples of the platform specific Hardware Abstraction Layer and System Service Layer functions discussed in 9.2.4, "Hardware Abstraction Layer" and 9.2.5, "System Services Layer".

10.0 VP-API-II Profiles

Profiles are structures that contain design data to meet specific system requirements. Many *VP-API-II* functions take *Profiles* as one or more arguments. There are several types of *Profiles*. Each defines a different set of parameters for a service aspect of the device. Table 12 provides a summary of all the *Profiles* that are used by the *VP-API-II* with the Le9662 device. *Profiles* are created using *VP Profile Wizard*.

Profile Name	Description
Device	The *Device Profile* provides default start-up values for device-specific configuration options that are normally set at initialization and never changed. These options include the bus clock frequency and configuration information, interrupt mode, voltage monitoring mode, dial pulse correction, device mode register, and switching regulator configuration.
AC FXS	Used for programming the transmission characteristics of the system, the *AC FXS Profile* holds the programmable gain and filter coefficient data. Over 70 country-specific *AC FXS Profiles* are provided and the user can select the one or ones that are required for his or her application.
DC	The *DC Profile* holds the DC feed and loop supervision parameters.
Ringing	The *Ringing Profile* contains the necessary commands and data to set up the ring generator of an FXS channel. Different *Profiles* can be used to vary the ringing characteristics of a line. Options available in the *Ringing Profile* include ringing waveform, frequency, amplitude, DC offset, ring trip method, maximum peak power, and ring cadence control.
Tone	The *Tone Profile* defines the various call progress tones that might be used in the FXS channel. The tones include dial tone, busy, ring-back, re-order, and howler.
Ringing Cadence	The *Ringing Cadence Profile* defines the cadence that is associated with ringing.
Tone Cadence	The *Tone Cadence Profile* defines the various call progress cadences that might be used in a system. The cadences include stutter dial, busy, ring-back, and reorder.
Caller ID	The *Caller ID Profile* defines the on- and off-hook signal generation for services such as Caller ID and message waiting indication. This *Profile* abstracts the physical and data link layers of the protocol. FSK and DTMF signaling are supported.
Metering	The *Metering Profile* sets the frequency (12- or 16-kHz), transition type, peak current, and echo voltage limits.

Table 12 - VP-API-II Profile Types

10.1 Profile Wizard Project Definition

The *Profile Wizard* application allows the user to define the requirements of the telephone line characteristics, switching and signaling with an intuitive user interface. After selecting the requirements, the user can generate the corresponding *Profiles* (.c and .h files) which the *VP-API-II* software uses to initialize and control the Le9662 device. Microsemi provides many example *Profiles* based on known country or standard requirements.

After launching *Profile Wizard*, it presents the user with the option of creating a new project based on a Microsemi telephony device family or evaluation board or to open an existing project. Figure 33 shows a typical screen shot for getting started and creating a new project

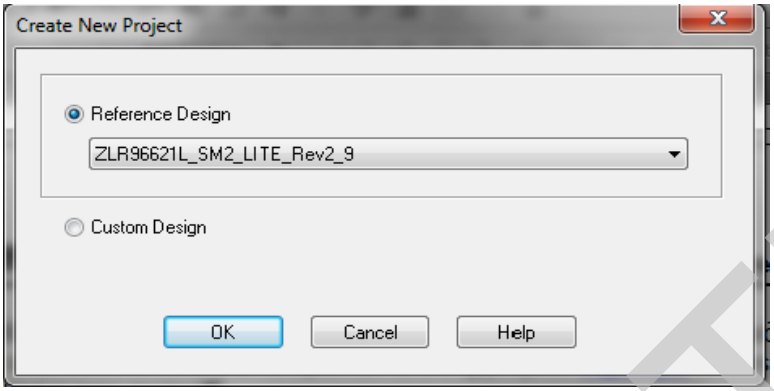


Figure 33 - Profile Wizard Screen – Creating a New Project

10.2 Profile Wizard Main Menu

Figure 34 shows a typical screen shot of the main menu of *Profile Wizard*. Note that the user can select from many standard country *Profiles*.

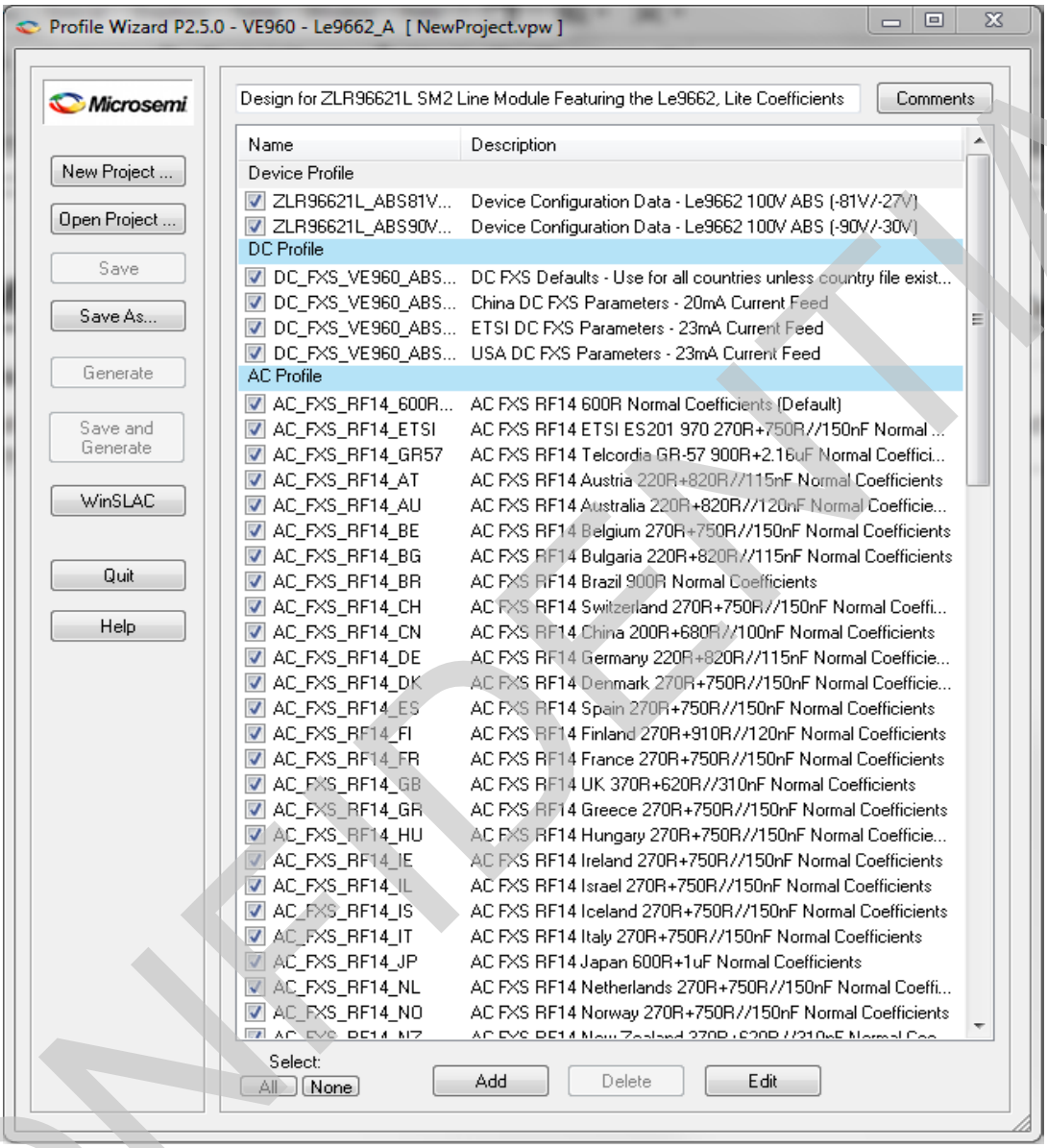


Figure 34 - Profile Wizard – Main Menu

10.3 Device Profile

10.3.1 Overview

The *Device Profile* configures device or circuit level parameters for the entire device. This *Profile* is required to enable reliable host communication with the device, to configure the switching regulator, and to define *VP-API-II* driver parameters. An example *Device Profile* is shown in Figure 35.

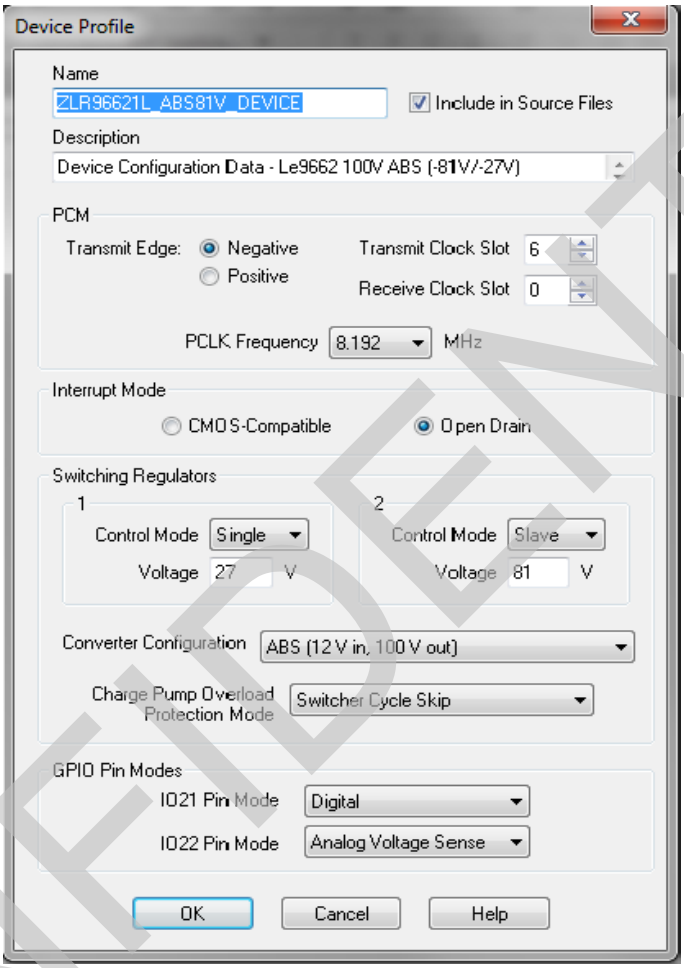


Figure 35 - Profile Wizard – Device Profile Configuration

Table 13 lists the *VP-API-II* functions which use values that are defined in the *Device Profile*.

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the above function. Refer to the *VP-API-II Reference Guide* for more details.

Table 13 - VP-API-II Functions For Device Configuration

10.4 AC FXS Profiles

AC FXS Profiles are used to define the input impedance, receive and transmit frequency response, hybrid balance, and initial gain values. Microsemi provides *AC FXS Profile* examples for over 70 countries including the following:

Input Impedance	Network Balance Impedance	Countries
150 Ω + (510 Ω // 47 nF)	150 Ω + (510 Ω // 47 nF)	Russia
200 Ω + (680 Ω // 100 nF)	200 Ω + (680 Ω // 100 nF)	China
220 Ω + (820 Ω // 115 nF)	220 Ω + (820 Ω // 115 nF)	Bulgaria, Germany, and South Africa
220 Ω + (820 Ω // 120 nF)	220 Ω + (820 Ω // 120 nF)	Australia
270 Ω + (750 Ω // 150 nF)	270 Ω + (750 Ω // 150 nF)	Belgium, Croatia, Denmark, Egypt, Estonia, France, Greece, Hungary, Iceland, Ireland, Israel, Italy, Ivory Coast, Netherlands, Nigeria, Norway, Portugal, Romania, Spain, Sweden, Switzerland, and Turkey
270 Ω + (910 Ω // 120 nF)	270 Ω + (1200 Ω // 120 nF)	Finland
370 Ω + (620 Ω // 310 nF)	370 Ω + (620 Ω // 310 nF)	New Zealand
300 Ω + (1000 Ω // 220 nF)	370 Ω + (620 Ω // 310 nF)	United Kingdom
600 Ω	600 Ω	USA, Argentina, Armenia, Belarus, Canada, Chile, Colombia, Czech Republic, Ecuador, El Salvador, Georgia, Hong Kong, India, Indonesia, Jordan, Korea, Kuwait, Malaysia, Mexico, Pakistan, Paraguay, Peru, Philippines, Poland, Qatar, Saudi Arabia, Singapore, South Korea, Taiwan, Thailand, Ukraine, UAE, Uruguay, and Venezuela.
600 Ω + 1.0 µF	600 Ω + 1.0 µF	Japan and PBX
900 Ω	900 Ω	Brazil
900 Ω + 2.16 µF	800 Ω // (0.05 µF + 100 Ω)	*Telcordia GR-57-CORE* Non-Loaded Loop

Table 14 - Supported AC Source Impedances

Notes:

1. *Table 14 provides suggested AC source impedances for the listed countries and are believed to be accurate as of the date of publication of this document. However, standards can and do change from time to time or new ones may be introduced. Some countries may support more than one standard AC source impedance. Customers are responsible for using the appropriate AC FXS Profiles for their applications.*
2. *VP Profile Wizard makes it easy to add additional countries as long as they are based on the supported impedances.*
3. *The standard files provided with VP Profile Wizard are for FXS interfaces with two 7-ohm PTC's in series with Tip and Ring. Please contact Microsemi CMPG Customer Applications if alternate series resistor or PTC resistance values are planned.*
4. *Narrowband and Wideband versions of these Profiles are available.*

Table 15 lists the *VP-API-II* functions which use values that are defined in the *AC FXS Profile*.

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and Ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details.

Table 15 - VP-API-II Functions Using AC FXS Profile

10.5 DC Profile

DC Profiles are used to define the feed and loop supervision conditions of the line. An example *DC Profile* is shown in Figure 36.

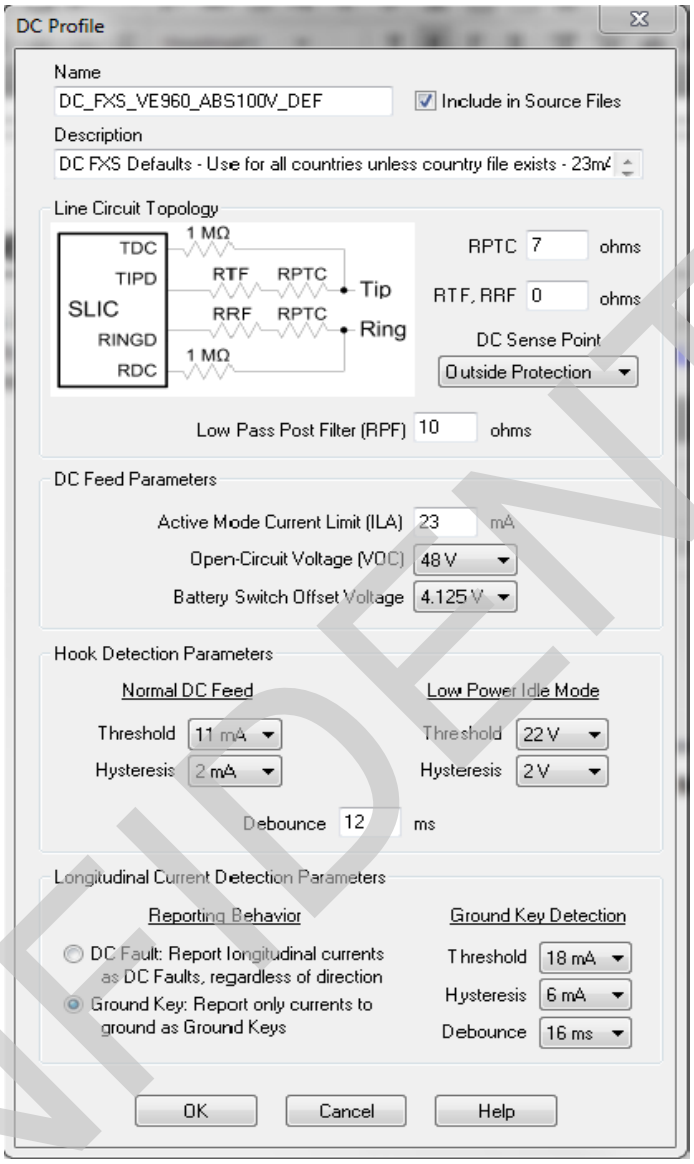


Figure 36 - Profile Wizard – DC Profile Configuration Example

Table 16 lists the *VP-API-II* functions which use values that are defined in the *DC Profile*.

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and Ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details.

Table 16 - VP-API-II Functions For DC Feed and Hook Detection Configuration

10.6 Ringing Profile

The *Ringing Profile* is used to define the type of ringing, ringing frequency, amplitude, offset, ring trip threshold, and ringing current limit. The *Ringing Profile* for the Le9662 using *VP Profile Wizard* is shown in Figure 37.

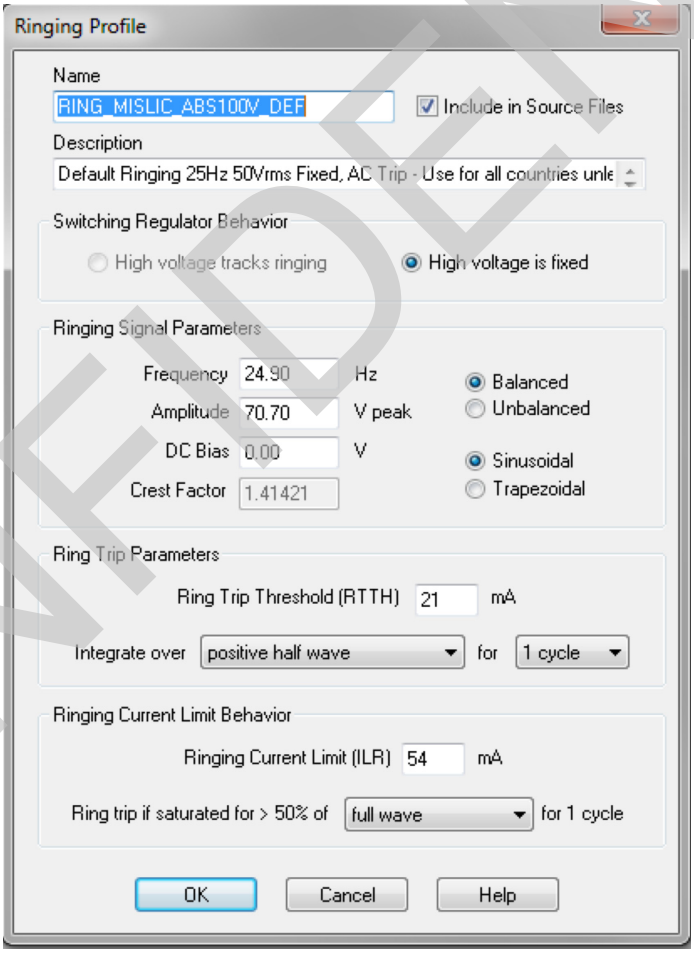


Figure 37 - Profile Wizard – Ringing Profile Configuration Example

Table 17 lists the *VP-API-II* functions which use values that are defined in the *Ringing Profile*.

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and Ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details.

Table 17 - VP-API-II Functions For Ringing and Ring Trip Definition

10.7 Tone Profile

Tone Profiles provide the capability to program up to four simultaneous tones on the line. The *Tone Profile* for the Le9662 using *VP Profile Wizard* is shown in Figure 38.

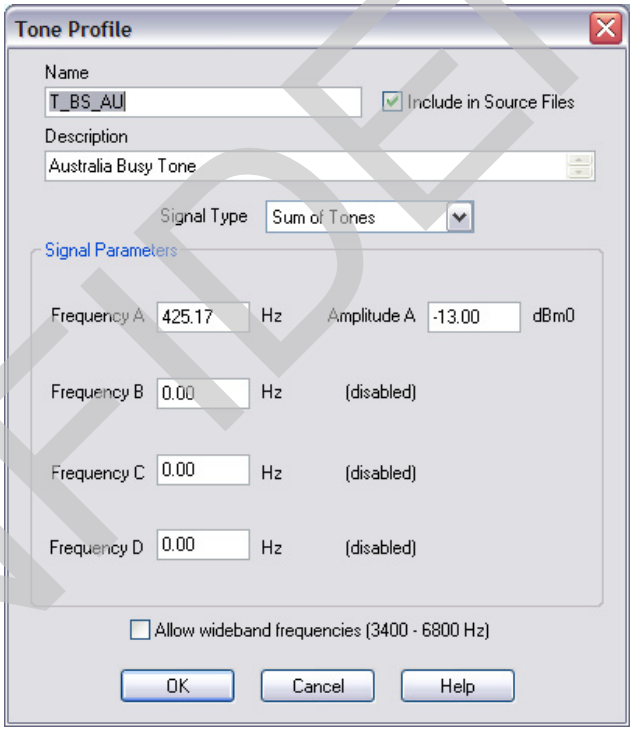


Figure 38 - Profile Wizard – Tone Profile Configuration

Table 18 lists the *VP-API-II* function which uses values that are defined in the *Tone Profile*.

Function Name	Description
`VpSetLineTone()`	Starts a tone on the line. The tone can be cadenced or “always on”.

Table 18 - VP-API-II Function Using Tone Profile

10.8 Tone Cadence Profile

VP-API-II Tone Cadencing is a highly flexible set of operators the user selects to implement any country-specific ringing or tone cadence requirements including Special Information Tones (SIT) and howler tones. Figure 39 shows how to define cadences for call progress tones with *VP Profile Wizard*.

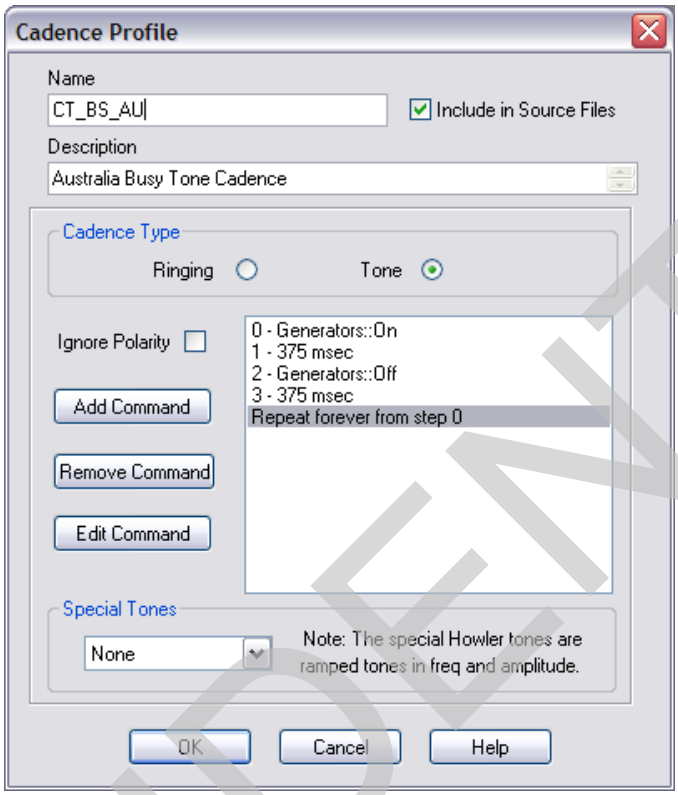


Figure 39 - Profile Wizard – Tone Cadence Profile Example

The *VP-API-II* Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific *VP-API-II* Line State.

Table 19 lists the *VP-API-II* function which uses values that are defined in the *Tone Cadence Profile*.

Function Name	Description
`VpSetLineTone()`	Provides tone cadencing for up to four tones. Also supports country-specific howler tone cadencing (AUS, UK, NTT) with ramp frequency and amplitude.

Table 19 - VP-API-II Function For Tone Cadencing

10.9 Ringing Cadence Profile

VP-API-II ringing cadencing is a flexible set of operators the user selects to implement any country-specific ringing cadence. Figure 40 shows how to define cadences for ringing generation with *VP Profile Wizard*. Note that events that are associated with Type 1 (on-hook) Caller ID ringing are included by this Profile.

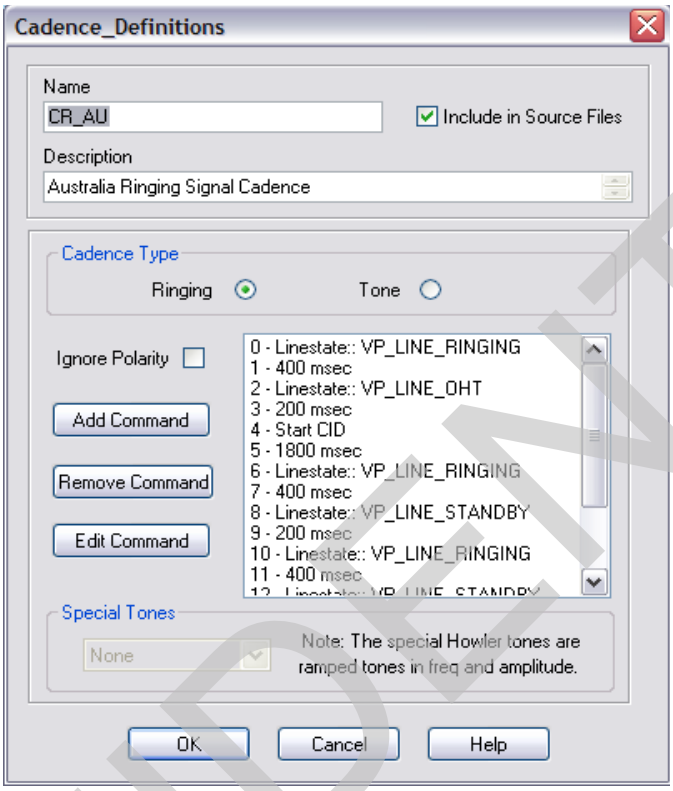


Figure 40 - Profile Wizard – Ringing Cadence Profile Example

The *VP-API-II* Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific *VP-API-II* line state.
5. Send CID -- Starts Caller ID (CID) on the line while continuing to run cadence. Used for Type 1 Caller ID when CID occurs after first regular ringing cycle in order to achieve a precise delay between the first and second rings.
6. Wait On Caller ID -- Starts Caller ID on the line and suspends currently running cadence. Used for Type 1 Caller ID when CID occurs prior to the first regular ringing cycle.

Table 20 lists the *VP-API-II* functions which use values that are defined in the *Ringing Cadence Profile*.

Function Name	Description
`VpSetLineState()`	`VP_LINE_RINGING` and `VP_LINE_RINGING_POLREV` for Ringing Cadence.
`VpInitRing()`	User function to provide Ringing Cadence. Also allows use selection of *Caller ID Profile* associated with ringing.

Table 20 - VP-API-II Functions For Ringing Cadencing

10.10 Caller ID Profile

The Caller ID block uses Generators C and D to generate phase-continuous 1200 baud FSK tones for on- or off-hook information such as Calling Line ID (or Caller ID) and Visual Message Waiting Indication (VMWI). The duration of each (bit) tone is fixed at 0.833 ms (1200 baud).

Bell 202 tone frequencies are used in the North American and some international markets, and the *ITU-T Recommendation V.23* tone frequencies are used in most of Europe and other international markets. The signal generator amplitude may need to be adjusted depending on the programmed loss plan. Data transmission levels are normally specified as -13.5 dBm +/-1.5 dB.

Exact preamble and mark sequences are generated by adjusting the framing mode and sending the appropriate number of characters. The *VP-API-II* abstracts this into a simple driver level interface. *VP Profile Wizard* enables the user to select the Caller ID parameters and build them into the *Caller ID Profile*, which generates the necessary coefficients and instructions for the *VP-API-II*. Note that the signal level in the example below is -7.5 dBm0, which corresponds to a transmitted signal of -13.5 dBm0 to the line due to the 6 dB D/A loss in the default *AC Profile*.

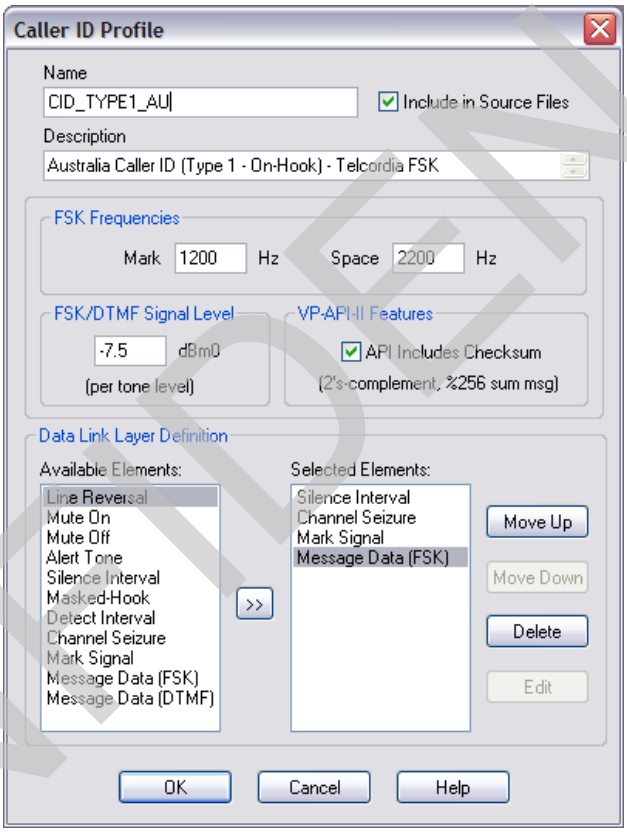


Figure 41 - Profile Wizard – Type 1 Caller ID Profile Example

Table 21 lists the *VP-API-II* functions which use values that are defined in the *Caller ID Profile*.

Function Name	Description
`VpInitRing()`	User function to provide *Caller ID Profile* associated with ringing.
`VpSendCid()`	Configures and starts Caller ID immediately. Used for Type 2 Caller ID.
`VpInitCid()`	Input for Caller ID Message Data up to 32 bytes.
`VpContinueCid()`	Input for Caller ID Message Data up to 16 bytes. Called after `VpInitCid()` or `VpSendCid()` when event `VP_LINE_EVID_CID_DATA` is generated.

Table 21 - VP-API-II Functions For Caller ID

10.11 Metering Profile

The *Metering Profile* allows the user to define the pulse metering frequency (12 or 16 kHz), peak current, and voltage limit. Figure 42 shows an example screen shot of the *Metering Profile* definition in *VP Profile Wizard*.

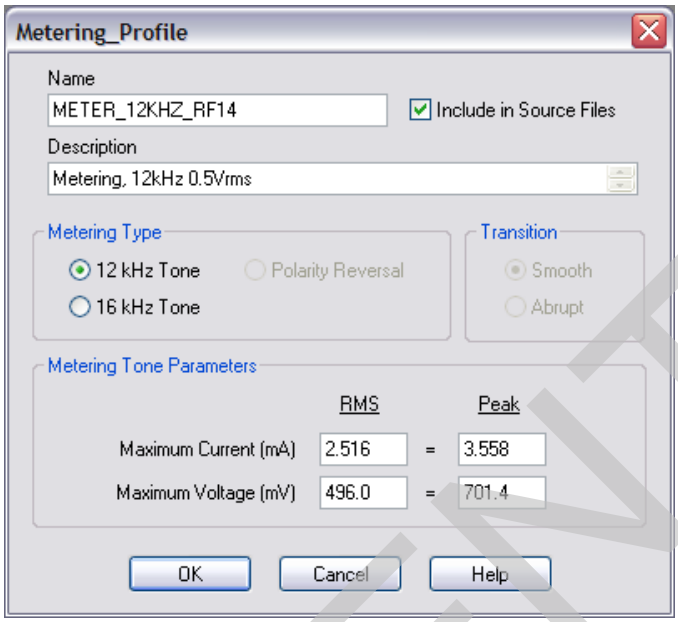


Figure 42 - Profile Wizard – Metering Profile Example

Table 22 lists the *VP-API-II* functions which use values that are defined in the *Metering Profile*.

Function Name	Description
`VpInitMeter()`	Configures the metering signal generator of an individual line.
`VpStartMeter()`	Starts metering pulses.

Table 22 - VP-API-II Functions for Metering

11.0 VoicePath API-II Software / Hardware Collateral

Microsemi develops and maintains several *VP-API-II* software / hardware collateral packages. These packages:

- Allow users to evaluate the *VP-API-II* device hardware without writing any code or designing any hardware.
- Extended the capability of the VP-API to include line testing capabilities.
- Provide a proven suite of factory hardware tests and device calibration.

11.1 Microsemi Telephony Applications Platform (ZTAP) and MiToolkit

ZTAP (Le71HP0400G) is a Linux based hardware platform designed to provide a demonstration and development vehicle for Microsemi's voice devices.

The platform can be run in two basic modes. In standalone mode, it operates as a basic call control environment that will automatically discover, setup and run Microsemi line modules. In interactive mode, along with the *Microsemi Toolkit Mini-PBX software application (Le71SDKTK)*, users can interact with the *VP-API-II* software to control the hardware connected to the ZTAP. This combination allows users to apply custom profiles, evaluate line testing capabilities, as well as perform voice quality measurements by connecting standard E1 or T1 test equipment to the ZTAP.

Microsemi provides *ZTAP Support Package software (Le71SDKZTAP)* for the ZTAP and is available from the Microsemi Software Delivery System (SDS) web site. The Le9662 device is supported by *ZTAP Support Package* version 1.16.0 and higher. The *MiToolkit* software is also available on the SDS and the Le9662 device is supported by version 1.10.0 and higher.

11.2 VeriVoice Professional Line Test software

The *VeriVoice Professional software package* provides customers with a set of cost-effective, reliable VoIP line tests. VeriVoice used in conjunction with the *VP-API-II* provides a set of comprehensive subscriber loop tests as well a set of inward facing self tests capable of diagnosing possible hardware issues. The VeriVoice Line Test software is distributed as OS independent, C source code and available from the Microsemi Software Delivery System web site.

11.3 VeriVoice Manufacturing Software

The *VeriVoice Manufacturing software package* is a stand-alone, self contained test package intended to facilitate factory testing of new hardware designs based on Microsemi ZL880 and miSLIC™ Series devices. The software is architected as a rapid set of tests which provide thorough test coverage of the Microsemi device and line circuit. The software eliminates the need for expensive external test equipment. The VeriVoice Manufacturing Software is distributed as OS independent, C source code and available from the Microsemi Software Delivery System web site.

12.0 Package Outline

The package outline drawings and the recommended land pattern for the Le9662 are presented in this section.

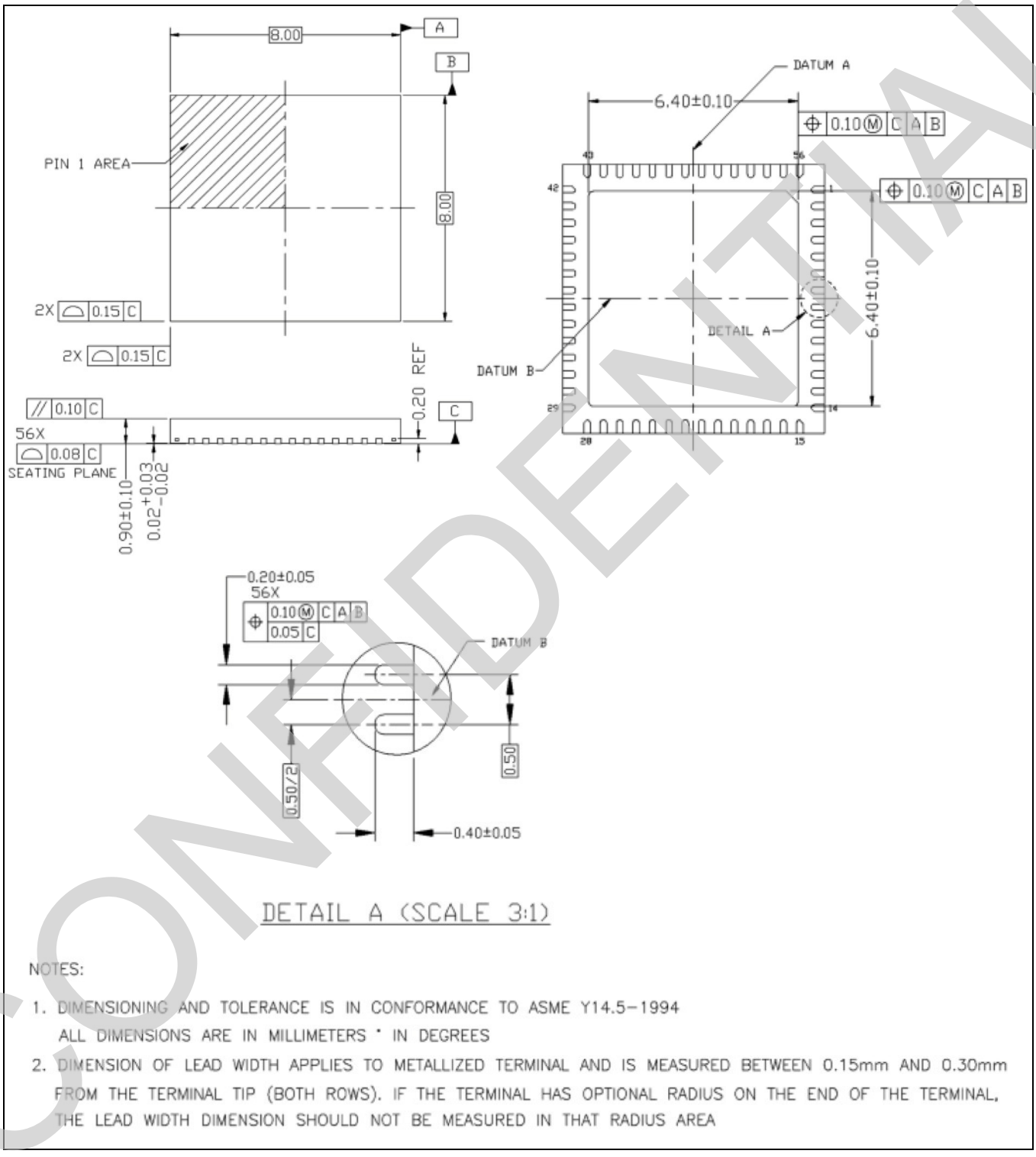
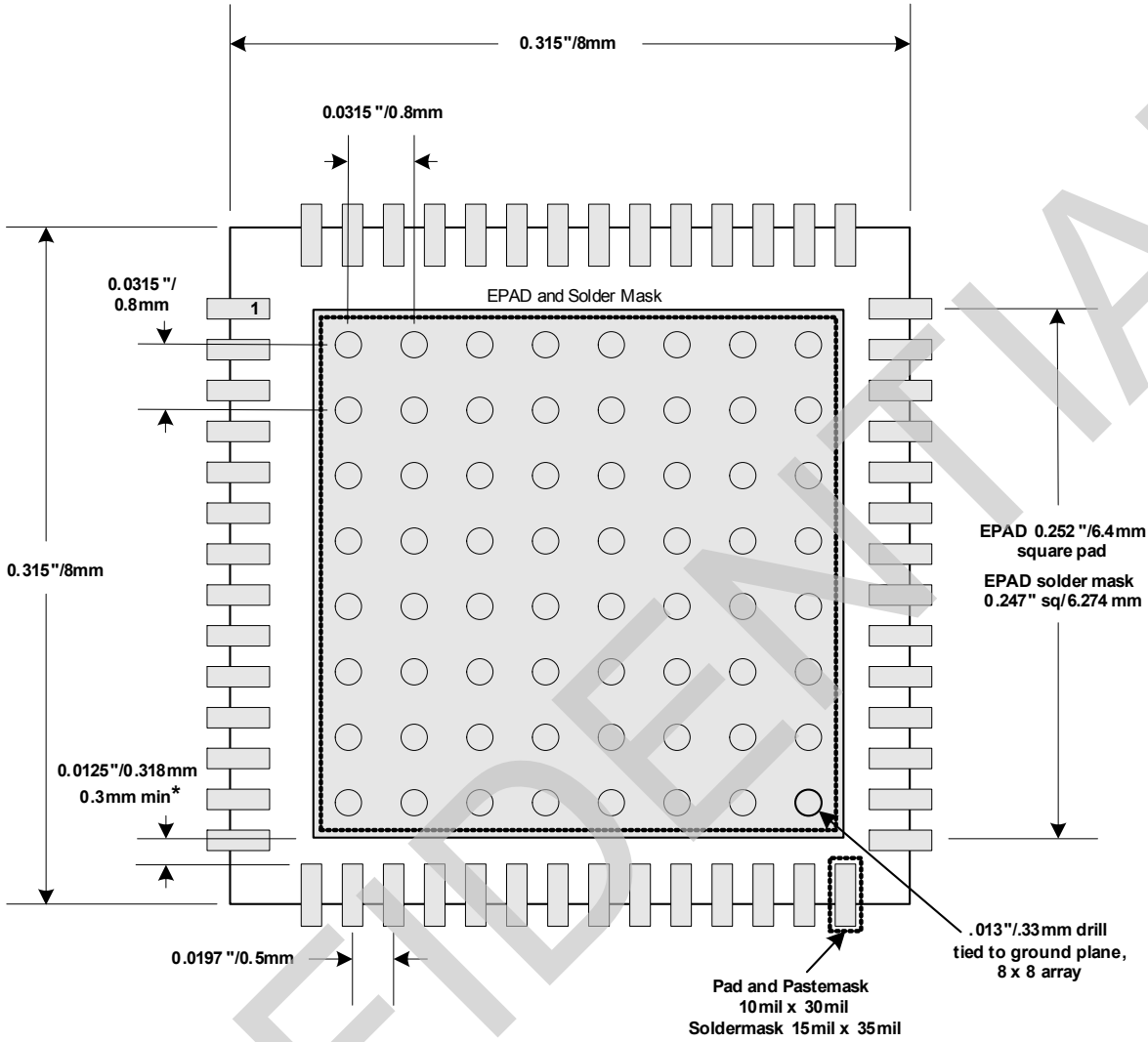


Figure 43 - Le9662 (56-Pin QFN) Package Drawing



Microsemi 56-pin QFN
8 mm x 8 mm, 0.5 mm pitch

* Minimum spacing between pins and EPAD must be 0.3 mm.

Recommended EPAD configuration uses a 0.252"/6.4 mm square pad tied to a ground plane with an 8x8 array of 0.33 mm vias. This is necessary for good thermal performance.

Figure 44 - Recommended Land Pattern (56-Pin QFN) – Top View

13.0 Related Collateral

The following documentation is available on the Microsemi website **www.microsemi.com/Le9662.**

13.1 Documentation

- **Le9662 Data Sheet**
- **Le9662 Product Brief**
- **VP-API-II Reference Guide** (*included with software download*)
- **VeriVoice Professional Test Suite Software** (*included with software download*)
- **ZLR96621 Reference Design User Guide**
- **ZLR96622 Reference Design User Guide**

13.1.1 Application Notes

- **EMI Radiated Immunity**
- **Two Layer PCB Design**

13.2 Development Hardware

Contact your sales representative for the latest Le9662 reference design hardware.

- **ZLR96621 SM2 Evaluation Module**
  - The *ZLR99621 Evaluation Module* features one *Le9662 Subscriber Line Interface Circuit miSLIC™ Series device* and a compact 2 FXS Flyback Automatic Battery Switching (FBABS) supply. The supply is provisioned for 70-V_{PK} ringing on each line with a 5 REN ringer load. This module plugs into the *SM2* receptacle on the *ZTAP* platform.
- **ZLR96622 SM2 Evaluation Module**
  - The *ZLR99622 Evaluation Module* features one *Le9662 Subscriber Line Interface Circuit miSLIC™ Series device* and a shared inverting Buck-Boost Automatic Battery Switching (BBABS) supply capable of generating up to 85-V_{PK} ringing on each line with a 5 REN ringer load. This module plugs into the *SM2* receptacle on the *ZTAP* platform.

13.3 Downloads, Firmware and Drivers

- **Le9662 IBIS Model,** available at **www.microsemi.com/Le9662.**

13.4 Development Software

URLs for the following software is available on the Microsemi website **www.microsemi.com/Le9662.**

- **Le71SK0002 VoicePath API-II Software**
  - The *VP-API-II* is a set of C source used by the host application to interface to the *VE880*, *VE890*, *ZL880, and miSLIC Series* and other Microsemi voice product families. A signed Software License Agreement (SLA) is required.
- **Le71SDKAPIL API-II Lite**
  - The *VP-API-II Lite* is identical to *VP-API-II*, with reduced functionality. *VP-API-II Lite* does not support tone or ringing cadencing, Caller ID, or Metering signal generation. This software is available without an SLA.

- **Le71SDKTK Microsemi CMPG Toolkit**
  - The Microsemi CMPG Toolkit application is a scripting environment that allows for the development and distribution of Tcl related collateral for Microsemi CMPG hardware and software products. The Toolkit includes several custom Microsemi CMPG Tcl extension packages, i.e. *VP-Script* and *Mini-PBX*.
  - The *VP-Script* application is intended to provide a robust interactive GUI and scripting environment for each of Microsemi CMPG's currently manufactured Microprocessor Interface (MPI) devices as well as for the next generation Host Bus Interface (HBI) devices.
  - *Mini-PBX* provides an interactive GUI for the *Voice Path API-2* and the *LT-API* libraries, i.e. *VeriVoice* and *LineCare*.
- **Le71SDKPRO Profile Wizard**
  - The *VP Profile Wizard* is a *Microsoft Windows* GUI application that aids in the organization and creation of country *Profiles* used in the *VP-API-II* into a single project file.
- **Le71SDKZTAP ZTAP Support Package**
  - The *ZTAP* is the latest in Microsemi CMPG's hardware platforms designed to provide a demonstration and development vehicle for Microsemi CMPG's voice devices. In standalone mode, it operates as a basic call control environment that will automatically run Microsemi CMPG line modules. When used with Microsemi CMPG Toolkit, devices/lines can be monitored and programmed with user specified parameters. Voice quality measurements can be made in either E1 or T1 mode by connecting standard test equipment to the *ZTAP*.
- **ZL880SLVVP VeriVoice Professional Test Suite**
  - The *VeriVoice™ Professional Test Suite* provides customers with the most cost-effective, reliable VoIP line-testing tools available on the market. The *VeriVoice Test Suite Software* is used in conjunction with *VoicePath™ API-II and API-II Lite* software to provide line test and self-test for select devices from the miSLIC™ Series and ZL880 VoicePort™ Series. The *VeriVoice™ Professional Test Suite* software is available in C code, allowing for easy integration and customization by a developer.
- **ZLS880VVMT VeriVoice Manufacturing Test Package**
  - The *VeriVoice™ Manufacturing Test Package* is a stand-alone, self contained test package intended to facilitate factory testing of new products based on Microsemi CMPG's *miSLIC™ Series, ZL880 Series, VE880 Series, and VE890 chipsets*. The software is distributed as a portable, platform-independent C source code module. The software is architected as a rapid set of tests which provide thorough test cover. The software eliminates the need for expensive test equipment.
- **LE71SDKWIN WinSLAC™ Software (available in Software Delivery System)**
  - The *WinSLAC™* utility is a software program that aids in the design and development of telephony interfaces and related voice band applications.

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