LX5575

5.15-5.85GHz 802.11ac Low Noise Amplifer

Description

The LX5575 is a 5GHz low noise amplifier (LNA) with bypass capability. The architecture and interface are optimized for next generation WLAN integration into high throughput 802.11ac devices and provides outstanding performance across temperature and voltage range.

The LX5575 is available in a 16-pin low profile 2.5x2.5x0.45mm QFN Package.

Features

- 3V to 5V Supply Voltage
- Integrated Bypassable LNA with Low NF
- Small Footprint: 2.5 x 2.5mm²
- Low Profile: 0.45mm max
- RoHS Compliant & Halogen Free

Applications

- Tablets
- Access Points
- Mobile Devices
- Notebooks
- Gaming

Block Diagram

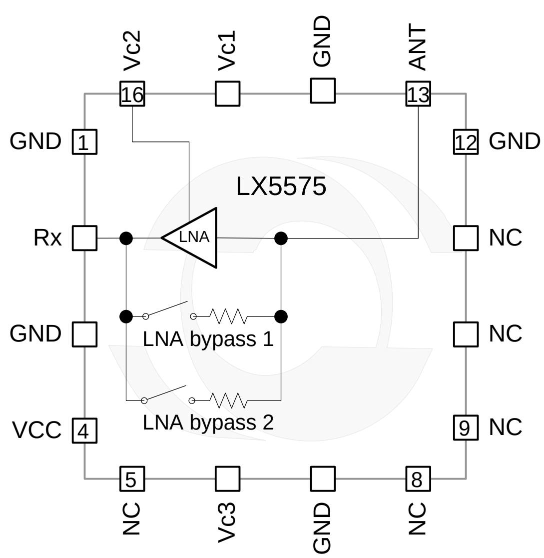
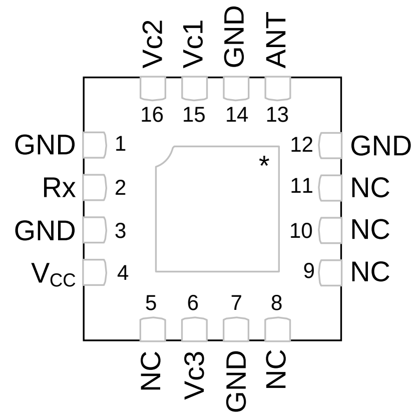


Figure 1 · Functional Block Diagram

Pin Configuration



* Pad is Ground

Figure 2 · Pinout (Top View)

Top mark •MSC
5575
YNNN = Trace code

Ordering Information

Ambient Temperature	Type	Package	Ordering Part Number	Packaging Type
-40°C to 85°C	RoHS2 Compliant, Pb-free 100% Matte Tin lead finish	QFN 2.5mm x 2.5mm x 0.45mm 16L	LX5575LL-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	GND	Ground
2	Rx	DC blocked 50ohm output of High Band bypassable LNA.
3	GND	Ground
4	V_{CC}	Supply voltage
5	NC	No connect
6	Vc3	Control line
7	GND	Ground
8	NC	No connect

Pin Number	Pin Designator	Description
9	NC	No connect
10	NC	No connect
11	NC	No connect
12	GND	Ground
13	ANT	DC blocked antenna port.
14	GND	Ground
15	Vc1	Control line
16	Vc2	Control line

Absolute Maximum Ratings

Parameter	Value	Units
DC Supply Voltage (V_{CC})	6	V
Control Inputs	3.6	V
Current on V_{CC} pin	20	mA
Total Power Dissipation	0.2	W
RF Input power at ANT Port	10	dBm
Maximum Junction Temperature (T_{JMAX})	+150	°C
Operational Ambient Temperature	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Peak Package Solder Reflow Temperature (40 seconds maximum exposure)	260	°C

Note: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times. The LX5575 typical ESD threshold level is >1000 VDC using Human Body Model (HBM) testing for all pins.

Exceeding any Absolute Maximum ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Absolute maximum DC supply and control voltage is specified as 6V applied for 10 seconds over the entire lifetime of the part. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JC} Junction to Case	20	°C/W
θ_{JA} Junction to Ambient	55	

Note: Note: The θJx numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Unless otherwise noted: Typical conditions are at 5.53GHz, T_A = 25°C, VCC = 5V. Min and max are across frequency, supply, and temperature, and QFN ground slug temperature. This includes unconditional stability of the LNA.						
General Characteristics						
F_{RFhi}	High Band Frequency Range	Fully functional, meeting all specifications	5.15		5.85	GHz
CHBW	Channel Bandwidth		20		80	MHz
VCC	Supply Voltage V_{CC}	Fully functional, meeting all specifications	3	5	5.25	V
V_{OH}	Control Logic Levels	High	3	3.3	3.6	V
V_{OL}		Low	0	0	0.4	V
Icl	Control Logic Current	Current consumption on any control pin		30	120	µA
Δt_{LNA}	LNA Switching Time	10% to 90%		15	20	ns
Δt_{rxlvl}	Rx Gain Switching Time	10% to 90%		50	100	ns
I_{LEAK}	Leakage Current	Device off with all supplies present and all control voltages floating		2	10	µA
Rx Parameters						
S_{11}	Input Return Loss	At Ant port for HG and Bypass2 Rx states	9	14		dB
		Bypass1 only	6	8.5		dB
S_{22}	Output Return Loss	At Rx port for all Rx gain states	10	20		dB
S_{21}	Rx Gain	LNA enabled	10	12	14	dB
		LNA bypass 1 state (bypass)	-12	-9	-6.5	
		LNA bypass state 2 (attenuation mode)		-20		
S_{21OOB}	Rx out of Band Gain	Gain at 2.45GHz with LNA enabled		-20	-15	dB
ΔS_{21}	Power Gain Variation	Over single 80MHz-chan			0.5	dB
		Over entire F_{RFlo}			2	
NF	Noise Figure	LNA enabled at 25°C, 3.3V		1.7	2.2	dB
		LNA enabled at 25°C, 5V		1.8	2.3	
		LNA Bypass State (bypass) @ 25°C		8		dB
IIP3	Input Third Order Intercept Point	At ANT port with LNA enabled; Pin (total) = -10 dBm	4	12		dBm
		At ANT port with LNA enabled and input tones at 2.412 and 2.437GHz and Pin (total) = 0 dBm.		16		dBm
		At ANT port with LNA bypassed and Pin (total)=5dBm	18	27		
I_{CC}	Operating Current	LNA enabled		9.2	14	mA
		LNA bypassed		1.4	10	µA

Functional State Table

Vc1	Vc2(LNA_EN)	Vc3	Default State
1	1	0	Rx High Gain
1	0	0	Rx Bypass State 1
0	0	1	Rx Bypass State 2 (high attenuation state)
0	0	0	Off/Sleep Mode
All other states undefined			

Characteristic Curves

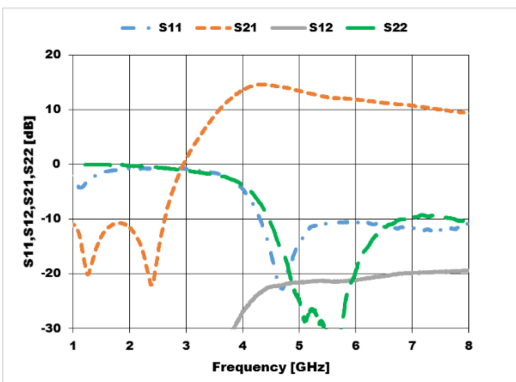


Figure 3 · S-Parameter (Vcc=5V, 25°C)

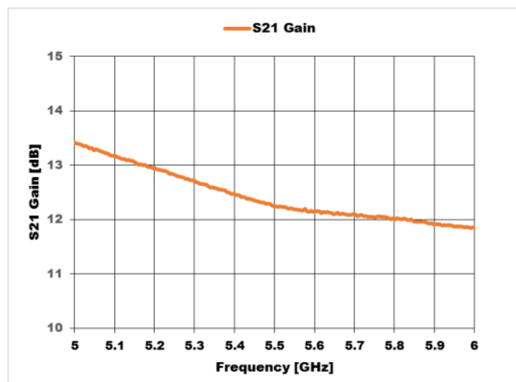


Figure 4 · S21 Gain (Vcc=5V, 25°C)

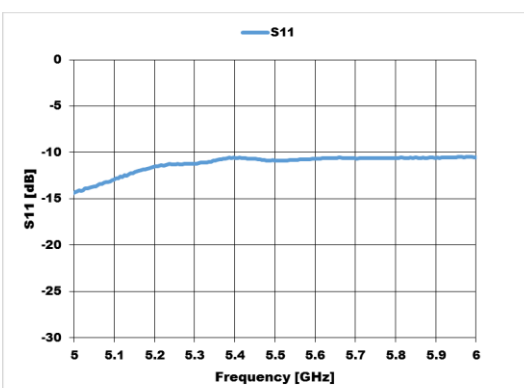


Figure 5 · RXHG Input Return Loss (Vcc=5V, 25°C)

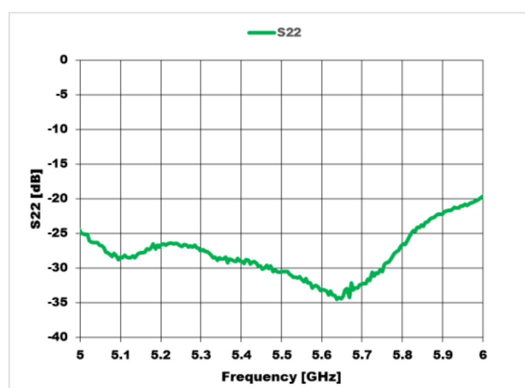


Figure 6 · RXHG Output Return Loss (Vcc=5V, 25°C)

Characteristic Curves

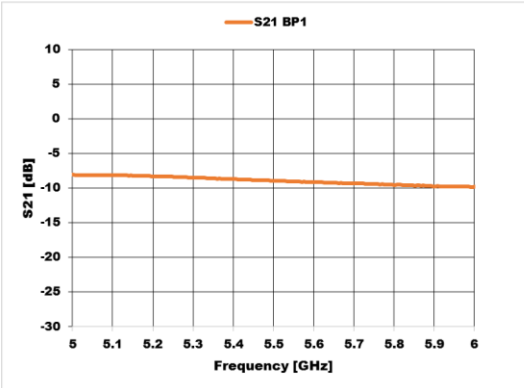


Figure 7 · BP1 Gain (Vcc=5V, 25°C)

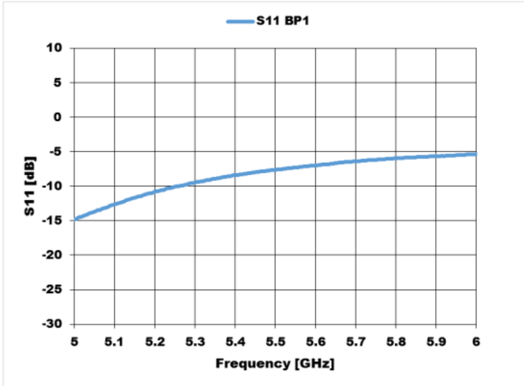


Figure 8 · BP1 Input Return Loss (Vcc=5V, 25°C)

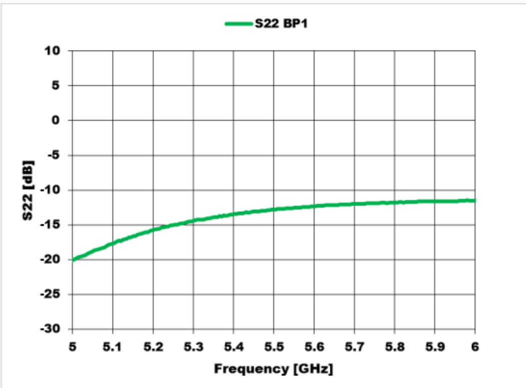


Figure 9 · BP1 Output Return Loss (Vcc=5V, 25°C)

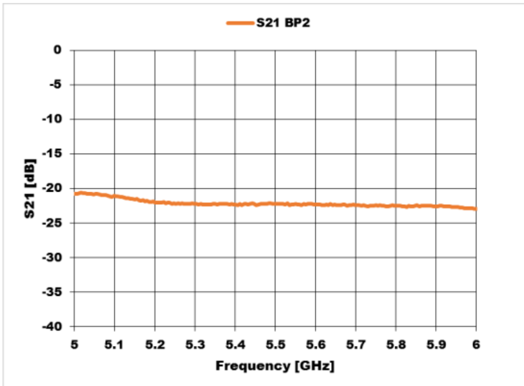


Figure 10 · BP2 Gain (Vcc=5V, 25°C)

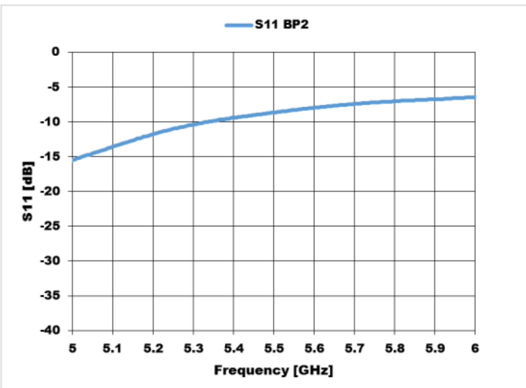


Figure 11 · BP2 Input Return Loss (Vcc=5V, 25°C)

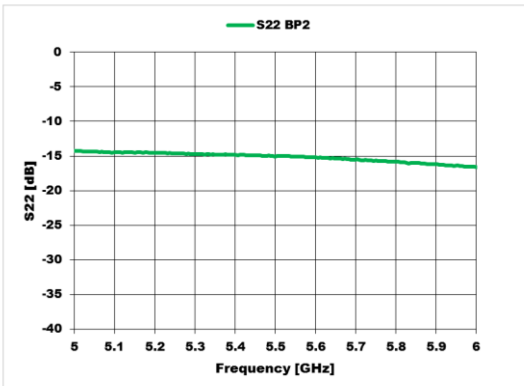


Figure 12 · BP2 Output Return Loss (Vcc=5V, 25°C)

Characteristic Curves

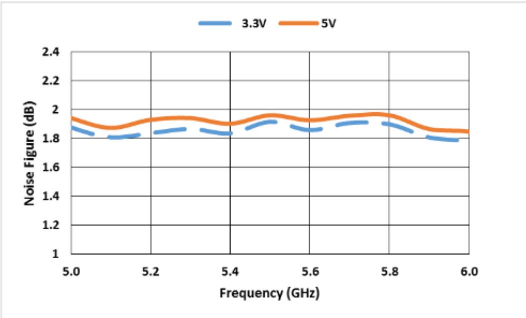


Figure 13 · HG mode Noise Figure (Vcc=5V, 25°C)

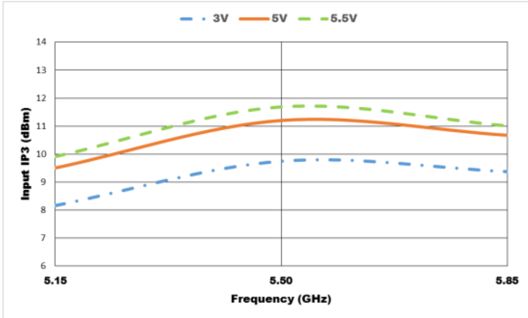


Figure 14 · Input IP3 25° C

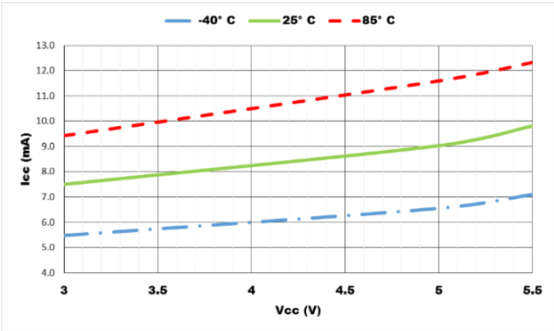
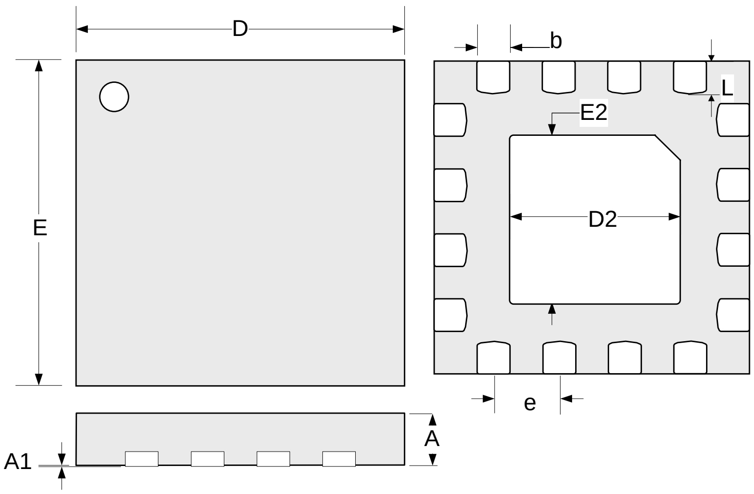


Figure 15 · Supply Current vs. Voltage over temperature

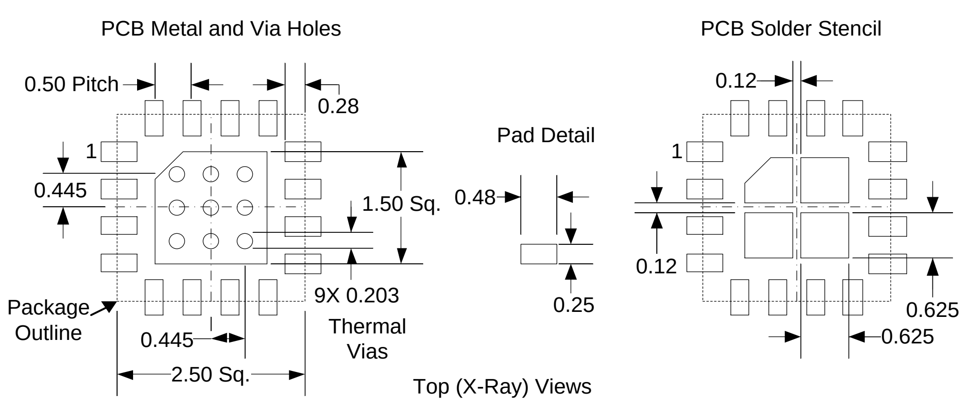
Package Outline Dimensions

The package is halogen free and meets RoHS2 and REACH standards.



DIMENSION	MILLIMETERS	
	MIN	MAX
A		0.45
A1	0	0.05
L	0.20	0.30
b	0.20	0.30
D	2.45	2.55
D2	1.30	1.40
E	2.45	2.55
E2	1.30	1.40
e	0.50 BSC	

Figure 16 · 16 Pin QFN Package Dimensions



Notes:
1. All dimensions are in millimeters.
2. Unless specified dimensions are symmetrical about center lines.
3. OSP or NiAu planar surface finish recommended.
4. Non-Solder Mask Defined (NSMD) pads recommended for terminal pads.
5. Recommended tented thermal vias as shown with vias filled with solder.
6. Stencil thickness < 0.15mm.
7. Aperture design for thermal pads using multiple openings with 60 to 80% solder paste coverage.

Figure 17 · PCB Layout Footprint (Top View)

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

a MICROCHIP company

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com