KSZ8993M

Integrated 3-Port 10/100 Managed Switch with PHYs

Features

- **Integrated 3-Port 10/100 Ethernet Switch**
  - 2nd Generation Switch with Three MACs and Two PHYs Fully Compliant to IEEE 802.3u Standard
  - Non-Blocking Switch Fabric Ensures Fast Packet Delivery by Utilizing a 1K MAC Address Lookup Table and a Store-and-Forward Architecture
  - Full-Duplex IEEE 802.3x Flow Control (PAUSE) with Force Mode Option
  - Half-Duplex Back Pressure Flow Control
  - Automatic MDI/MDI-X Crossover with Disable and Enable Option
  - 100BASE-FX Support on Port 1
  - MII Interface Supports Both MAC Mode and PHY Mode
  - 7-Wire Serial Network Interface (SNI) Support for Legacy MAC
  - Comprehensive LED Indicator Support for Link, Activity, Full-/Half-Duplex and 10/100 Speed
- **Comprehensive Configuration Register Access**
  - Serial Management Interface (SMI) to All Internal Registers
  - MII Management (MIIM) Interface to PHY Registers
  - SPI and I^2C Interface to all internal registers
  - I/O Pins Strapping and EEPROM to Program Selective Registers in Unmanaged Switch Mode
  - Control Registers Configurable on the Fly (Port-Priority, 802.1p/d/q, AN, etc.)
- **QoS/CoS Packet Prioritization Support**
  - Per Port, 802.1p, and DiffServ-Based
  - Re-Mapping of 802.1p Priority Field Per Port Basis
  - Four Priority Levels
- **Advanced Switch Features**
  - IEEE 802.1q VLAN Support for Up to 16 Groups (Full Range of VLAN IDs)
  - VLAN ID Tag/Untag Options, Per Port Basis
  - IEEE 802.1p/q Tag Insertion or Removal on a Per Port Basis (Egress)
  - Programmable Rate Limiting from 0 Mbps to 100 Mbps at the Ingress and Egress Port, Rate Options for High and Low Priority Per Port Basis
  - Broadcast Storm Protection with Percent Control (Global and Per Port Basis)
  - IEEE 802.1d Spanning Tree Protocol Support
  - Upstream Special Tagging Mode to Inform the Processor which Ingress Port Receives the Packet
  - IGMP V1/V2 Snooping Support for Multicast Packet Filtering
  - Double-Tagging Support
- **Switch Management Features**
  - Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port or MII
  - Management Information Base Counters for Fully Compliant Statistics Gathering, 34 MIB Counters Per Port
  - Loopback Modes for Remote Diagnostic of Failure
- **Low Power Dissipation**
  - <0.8 Watts (includes PHY transmit drivers)
  - Full-Chip Hardware Power-Down (Register Configuration Not Saved)
  - Per Port Based Software Power-Save on PHY (Idle Link Detection, Register Configuration Preserved)
  - Voltages: Core 1.8V, I/O and Transceiver 3.3V (Use KSZ8993ML for 3.3V-Only Operation)
- **Available in a 128-Pin PQFP Package**

Applications

- Universal Solutions
  - Broadband Gateway/Firewall/VPN
  - Integrated DSL or Cable Modem Multi-Port Router
  - Wireless LAN Access Point + Gateway
  - Residential and Enterprise VoIP Gateway/Phone
  - Set-Top/Game Box
  - Home Networking Expansion
  - Standalone 10/100 Switch
  - FTTx Customer Premises Equipment
  - Fiber Broadband Gateway
- Upgradeable Solutions (Note 1)
  - Unmanaged Switch with Future Option to Migrate to a Managed Solution
  - Single PHY Alternative with Future Expansion Option for Two Ports
- Industrial Solutions
  - Applications that Require Port Redundancy and Port Monitoring
  - Sensor Devices in Redundant Ring Topology

Note 1: The cost and time of PCB re-spin.

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1.0 INTRODUCTION

1.1 General Description

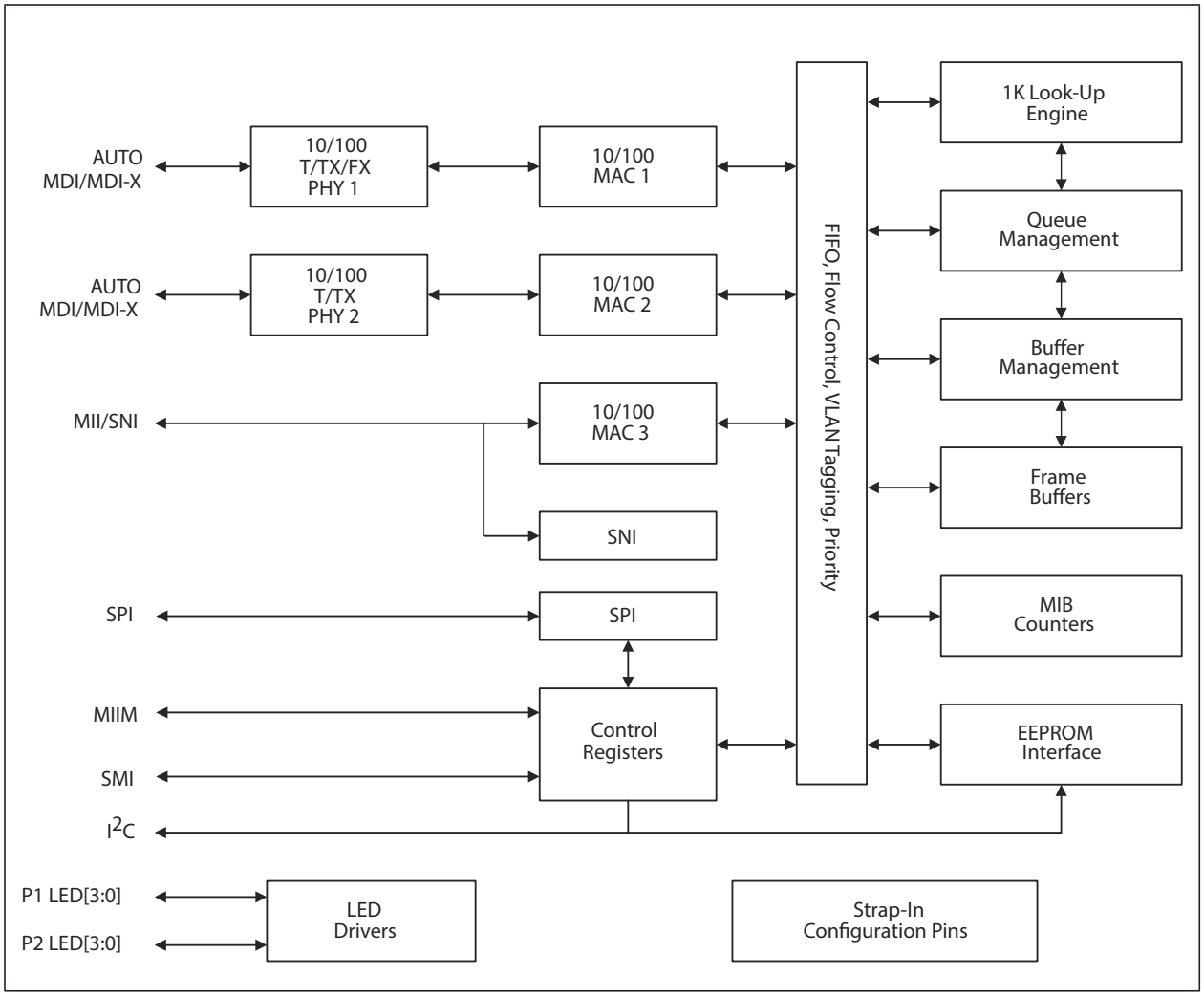
The KSZ8993M, a highly integrated Layer 2 managed switch, is designed for low port count, cost-sensitive 10/100 Mbps switch systems. It offers an extensive feature set that includes tag/port-based VLAN, quality of service (QoS) priority, management, management information base (MIB) counters, MII/SNI, and CPU control/data interfaces to effectively address a wide range of Fast Ethernet applications.

The KSZ8993M contains two 10/100 transceivers with patented mixed-signal low-power technology, three media access control (MAC) units, a high speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

Both PHY units support 10BASE-T and 100BASE-TX. In addition, one of the PHY unit supports 100BASE-FX.

The KSZ8993ML is the single supply version with the same features of the KSZ8993M.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 128-PIN PQFP ASSIGNMENT, (TOP VIEW)

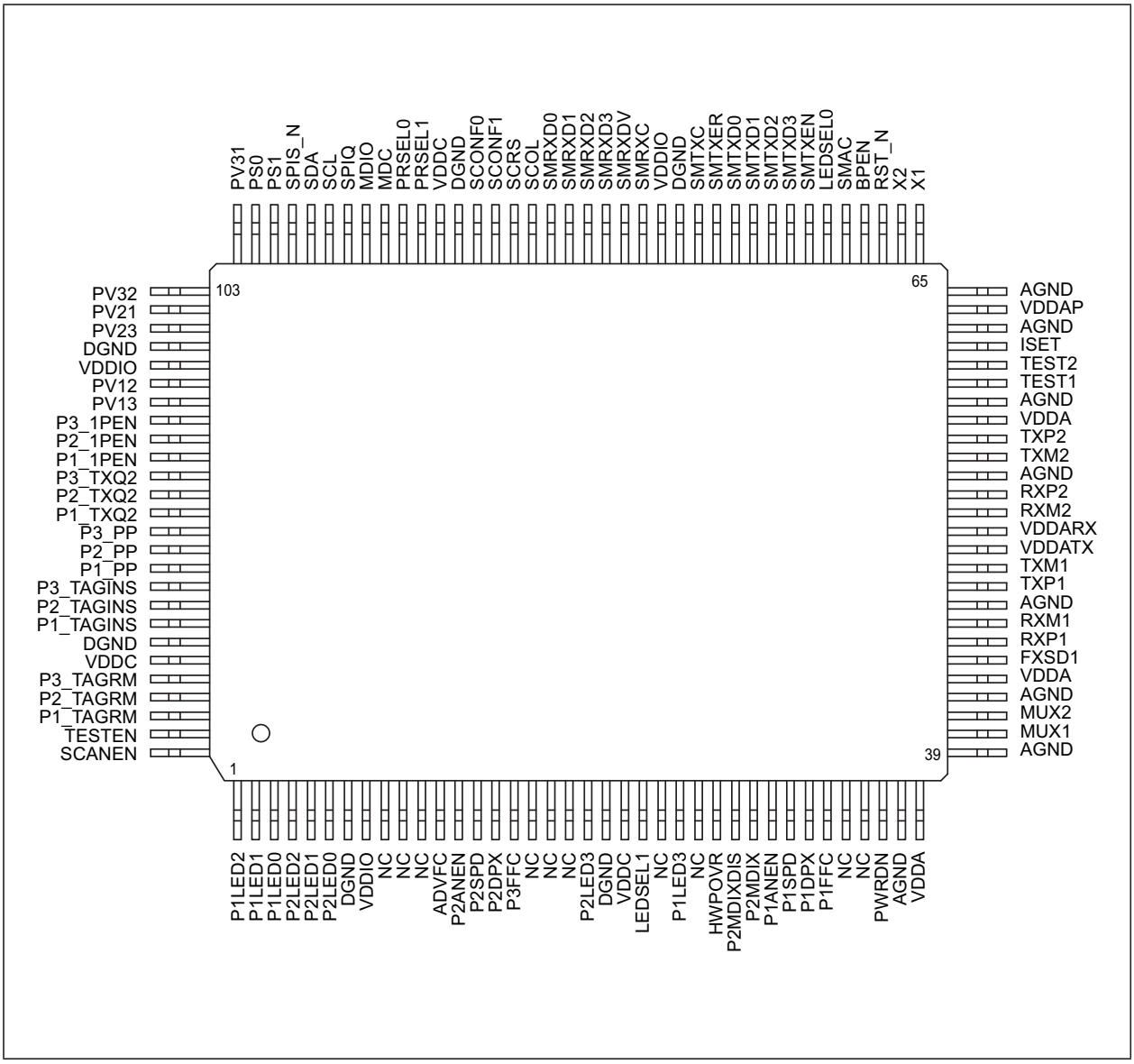


TABLE 2-1: SIGNALS

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="13">1
2
3</td><td rowspan="13">P1LED2
P1LED1
P1LED0</td><td rowspan="13">IPU/O</td><td>Port 1 LED Indicators</td></tr>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P1LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>P1LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td></td><td colspan="2"></td></tr>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P1LED3</td><td>Activity</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
<tr><td colspan="3">Note: LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td rowspan="13">4
5
6</td><td rowspan="13">P2LED2
P2LED1
P2LED0</td><td rowspan="13">IPU/O</td><td>Port 2 LED Indicators</td></tr>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>P2LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td></td><td colspan="2"></td></tr>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P2LED3</td><td>Activity</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P2LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>—</td></tr>
<tr><td colspan="3">Note: LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 20.
During reset, P2LED[2:0] are inputs for internal testing</td></tr>
<tr><td>7</td><td>DGND</td><td>GND</td><td colspan="2">Digital ground.</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td colspan="2">3.3V digital V_{DD}</td></tr>
<tr><td>9</td><td>NC</td><td>IPD</td><td colspan="2">No connect</td></tr>
<tr><td>10</td><td>NC</td><td>IPD</td><td colspan="2">No connect</td></tr>
<tr><td>11</td><td>NC</td><td>IPU</td><td colspan="2">No connect</td></tr>
<tr><td>12</td><td>ADVFC</td><td>IPU</td><td colspan="2">1 = Advertise the switch’s flow control capability via auto negotiation.
0 = Will not advertise the switch’s flow control capability via auto negotiation.</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
13	P2ANEN	IPU	1 = Enable auto negotiation on port 2 0 = Disable auto negotiation on port 2
14	P2SPD	IPD	1 = Force port 2 to 100BT if P2ANEN = 0 0 = Force port 2 to 10BT if P2ANEN =0
15	P2DPX	IPD	1 = Port 2 default to full-duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in full-duplex mode if P2ANEN = 0. 0 = Port 2 default to half-duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in half-duplex mode if P2ANEN = 0.
16	P2FFC	IPD	1 = Always enable (force) port 2 flow control feature 0 = Port 2 flow control feature enable is determined by auto negotiation result.
17	NC	OPU	No connect
18	NC	IPD	No connect
19	NC	IPD	No connect
20	P2LED3	OPD	Port 2 LED indicator **Note:** Internal pull-down is weak; it will not turn on the LED. See description for pin 4.
21	DGND	GND	Digital ground
22	VDDC/ VOUT_1V8	P	VDDC: For KSZ8993M, this is an input power pin for the 1.8V digital core V_{DD}. VOUT_1V8: For KSZ8993ML, this is a 1.8V output power pin to supply the KSZ8993ML's input power pins: VDDAP (pin 63), VDDC (pins 91 and 123), and VDDA (pins 38, 43, and 57).
23	LEDSEL1	IPD	LED display mode select See description for pins 1 and 4.
24	NC	O	No connect
25	P1LED3	OPD	Port 1 LED indicator **Note:** An external 1 kΩ pull-down is needed on this pin if it is connected to a LED. The 1 kΩ resistor will not turn on the LED. See description for pin 1.
26	NC	O	No connect
27	HWPOVR	IPD	Hardware pin overwrite 0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data. 1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for register 0x2C bits [7:5], (port 2: auto-negotiation enable, force speed, force duplex).
28	P2MDIXDIS	IPD	Port 2 Auto MDI/MDI-X PD (default) = Enable PU = Disable
29	P2MDIX	IPD	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2/TXM2 pins) PU = MDI, (transmit on RXP2/RXM2 pins)
30	P1ANEN	IPU	1 = Enable auto negotiation on port 1 0 = Disable auto negotiation on port 1
31	P1SPD	IPD	1 = Force port 1 to 100BT if P1ANEN = 0 0 = Force port 1 to 10BT if P1ANEN = 0

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
32	P1DPX	IPD	1 = Port 1 default to full duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = Port 1 default to half duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.
33	P1FFC	IPD	1 = Always enable (force) port 1 flow control feature 0 = Port 1 flow control feature enable is determined by auto negotiation result.
34	NC	IPD	No connect
35	NC	IPD	No connect
36	PWRDN	IPU	Chip power-down input (active-low)
37	AGND	GND	Analog ground
38	VDDA	P	1.8V analog V_{DD}
39	AGND	GND	Analog ground
40	MUX1	I	Factory test pin - float for normal operation
41	MUX2	I	Factory test pin - float for normal operation
42	AGND	GND	Analog ground
43	VDDA	P	1.8V analog V_{DD}
44	FXSD1	I	Fiber signal detect/factory test pin
45	RXP1	I/O	Physical receive or transmit signal (+ differential)
46	RXM1	I/O	Physical receive or transmit signal (– differential)
47	AGND	GND	Analog ground
48	TXP1	I/O	Physical transmit or receive signal (+ differential)
49	TXM1	I/O	Physical transmit or receive signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Physical receive or transmit signal (– differential)
53	RXP2	I/O	Physical receive or transmit signal (+ differential)
54	AGND	GND	Analog ground
55	TXM2	I/O	Physical transmit or receive signal (– differential)
56	TXP2	I/O	Physical transmit or receive signal (+ differential)
57	VDDA	P	1.8V analog V_{DD}
58	AGND	GND	Analog ground
59	TEST1	I	Factory test pin - float for normal operation
60	TEST2	IPU	Factory test pin - float or pull-up for normal operation
61	ISET	O	Set physical transmit output current. Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
62	AGND	GND	Analog ground
63	VDDAP	P	1.8V analog V_{DD} for PLL
64	AGND	GND	Analog ground
65	X1	I	25 MHz crystal/oscillator clock connections Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. **Note:** Clock is ±50 ppm for both crystal and oscillator.
66	X2	O	
67	RST_N	IPU	Hardware reset pin (active-low)

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
68	BPEN	IPD	Half-duplex back pressure 1 = Enable 0 = Disable
69	SMAC	IPD	Special MAC mode In this mode, the switch will do faster back-offs than normal. 1 = Enable 0 = Disable
70	LEDSEL0	IPD	LED display mode select See description for pins 1 and 4.
71	SMTXEN	IPD	Switch MII transmit enable
72	SMTXD3	IPD	Switch MII transmit data bit 3
73	SMTXD2	IPD	Switch MII transmit data bit 2
74	SMTXD1	IPD	Switch MII transmit data bit 1
75	SMTXD0	IPD	Switch MII transmit data bit 0
76	SMTXER	IPD	Switch MII transmit error
77	SMTXC	IPD/O	Switch MII transmit clock Output in PHY MII mode Input in MAC MII mode
78	DGND	GND	Digital ground
79	VDDIO	P	3.3V digital V_{DD}
80	SMRXC	IPD/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
81	SMRXDV	O	Switch MII receive data valid
82	SMRXD3	IPD/O	Switch MII receive data bit 3 Strap option: Switch MII full-duplex flow control PD (default) = Disable PU = Enable
83	SMRXD2	IPD/O	Switch MII receive bit 2 Strap option: Switch MII is in PD (default) = Full-duplex mode PU = Half-duplex mode
84	SMRXD1	IPD/O	Switch MII receive bit 1 Strap option: Switch MII is in PD (default) = 100 Mbps mode PU = 10 Mbps mode
85	SMRXD0	IPD/O	Switch MII receive bit 0 Strap option: Switch will accept packet size up to PD (default) = 1536 bytes (inclusive) PU = 1522 bytes (tagged), 1518 bytes (untagged)
86	SCOL	IPD/O	Switch MII collision detect
87	SCRS	IPD/O	Switch MII carrier sense

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description	
88 89	SCONF1 SCONF0	IPD	Priority select. Select queue servicing if using split queues. Use the table below to select the desired servicing. Note that this selection effects all split transmit queue ports in the same way.	
			[SCONF1, SCONF0]	**Description**
			[0,0]	Disable, outputs tri-stated
			[0,1]	PHY mode MII
			[1,0]	MAC mode MII
			[1,1]	PHY mode SNI
90	DGND	GND	Digital ground	
91	VDDC	P	1.8V digital V_{DD}	
92 93	PRSEL1 PRSEL0	IPD	Priority select. Select queue servicing if using split queues. Use the table below to select the desired servicing. Note that this selection effects all split transmit queue ports in the same way.	
			[PRSEL1, PRSEL0]	**Description**
			[0,0]	Transmit all high priority before low priority
			[0,1]	Transmit high priority and low priority at 10:1 ratio
			[1,0]	Transmit high priority and low priority at 5:1 ratio
			[1,1]	Transmit high priority and low priority at 2:1 ratio
94	MDC	IPU	MII management interface: Clock input	
95	MDIO	IPU/O	MII management interface: Data input/output Note: an external 4.7 kΩ pull-up is needed on this pin when it is in use.	
96	SPIQ	OPU	SPI slave mode: Serial data output See description for pins 100 and 101.	
97	SCL	IPU/O	SPI slave mode/I^2C slave mode: Clock input I^2C master mode: clock output See description for pins 100 and 101.	
98	SDA	IPU/O	SPI slave mode: Serial data input I^2C master/slave mode: Serial data input/output See description for pins 100 and 101.	
99	SPIS_N	IPU	SPI slave mode: Chip select (active-low) When SPIS_N is high, the KSZ8993M is deselected and SPIQ is held in high impedance state. A high-to-low transition is used to initiate SPI data transfer. See description for pins 100 and 101.	

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="20">100
101</td><td rowspan="20">PS1
PS0</td><td rowspan="20">IPD</td><td>Serial bus configuration pins to select mode of access to KSZ8993M internal registers.
[PS1, PS0] = [0, 0] — I²C master (EEPROM) mode
(If EEPROM is not detected, the power-up default values of the KSZ8993M internal registers will be used.)</td></tr>
<tr><td>
<table>
<tr><th>Interface Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
<tr><td>SCL</td><td>O</td><td>I²C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr>
<tr><td>SPIS_N</td><td>IPU</td><td>Not used</td></tr>
</table>
</td></tr>
<tr><td>[PS1, PS0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8993M device addresses are:
1011_1111 <read>
1011_1110 <write></td></tr>
<tr><td>
<table>
<tr><th>Interface Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
<tr><td>SCL</td><td>O</td><td>I²C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr>
<tr><td>SPIS_N</td><td>IPU</td><td>Not used</td></tr>
</table>
</td></tr>
<tr><td>[PS1, PS0] = [1, 0] — SPI slave mode</td></tr>
<tr><td>
<table>
<tr><th>Interface Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr>
<tr><td>SCL</td><td>I</td><td>SPI clock</td></tr>
<tr><td>SDA</td><td>I</td><td>SPI data in</td></tr>
<tr><td>SPIS_N</td><td>IPU</td><td>SPI chip select</td></tr>
</table>
</td></tr>
<tr><td>[PS1, PS0] = [1, 1] – SMI mode
In this mode, the KSZ8993M provides access to all its internal 8 bit registers through its MDC and MDIO pins.
Note: When (PS1, PS0) ≠ (1,1), the KSZ8993M provides access to its 16-bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr><td>102
103</td><td>PV31
PV32</td><td>IPU</td><td>Port 3 port-based VLAN mask bits – Use to select which ports may transmit packets received on port 3.
PV31 = 1, port 1 may transmit packets received on port 3
PV31 = 0, port 1 will not transmit any packets received on port 3
PV32 = 1, port 2 may transmit packets received on port 3
PV32 = 0, port 2 will not transmit any packets received on port 3</td></tr>
<tr><td>104
105</td><td>PV21
PV23</td><td>IPU</td><td>Port 2 port-based VLAN mask bits – Use to select which ports may transmit packets received on port 2.
PV21 = 1, port 1 may transmit packets received on port 2
PV21 = 0, port 1 will not transmit any packets received on port 2
PV23 = 1, port 3 may transmit packets received on port 2
PV23 = 0, port 3 will not transmit any packets received on port 2</td></tr>
<tr><td>106</td><td>DGND</td><td>GND</td><td>Digital ground</td></tr>
<tr><td>107</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DD}</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
108 109	PV12 PV13	IPU	Port 1 port-based VLAN mask bits – Use to select which ports may transmit packets received on port 1. PV12 = 1, port 2 may transmit packets received on port 1 PV12 = 0, port 2 will not transmit any packets received on port 1 PV13 = 1, port 3 may transmit packets received on port 1 PV13 = 0, port 3 will not transmit any packets received on port 1
110	P3_1PEN	IPD	Enable 802.1p priority classification on port 3 ingress 1 = Enable 0 = Disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P3_PP pin.
111	P2_1PEN	IPD	Enable 802.1p priority classification on port 2 ingress 1 = Enable 0 = Disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P2_PP pin.
112	P1_1PEN	IPD	Enable 802.1p priority classification on port 1 ingress 1 = Enable 0 = Disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P1_PP pin.
113	P3_TXQ2	IPD	Select transmit queue split on port 3 1 = Split 0 = No split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 3 is set by P3_TXQ2.
114	P2_TXQ2	IPD	Select transmit queue split on port 2 1 = Split 0 = No split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 2 is set by P2_TXQ2.
115	P1_TXQ2	IPD	Select transmit queue split on port 1 1 = Split 0 = No split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 1 is set by P1_TXQ2.
116	P3_PP	IPD	Select port-based priority on port 3 ingress 1 = High 0 = Low (default) 802.1p and DiffServ, if applicable, takes precedence.
117	P2_PP	IPD	Select port-based priority on port 2 ingress 1 = High 0 = Low (default) 802.1p and DiffServ, if applicable, takes precedence.
118	P1_PP	IPD	Select port-based priority on port 1 ingress 1 = High 0 = Low (default) 802.1p and DiffServ, if applicable, takes precedence.

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type	Description
119	P3_TAGINS	IPD	Enable tag insertion on port 3 egress 1 = Enable 0 = Disable All packets transmitted from port 3 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
120	P2_TAGINS	IPD	Enable tag insertion on port 2 egress 1 = Enable 0 = Disable All packets transmitted from port 2 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
121	P1_TAGINS	IPD	Enable tag insertion on port 1 egress 1 = Enable 0 = Disable All packets transmitted from port 1 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
122	DGND	GND	Digital ground
123	VDDC	P	1.8V digital V_{DD}
124	P3_TAGRM	IPD	Enable tag removal on port 3 egress 1 = Enable 0 = Disable All packets transmitted from port 3 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
125	P2_TAGRM	IPD	Enable tag removal on port 2 egress 1 = Enable 0 = Disable All packets transmitted from port 2 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
126	P1_TAGRM	IPD	Enable tag removal on port 1 egress 1 = Enable 0 = Disable All packets transmitted from port 1 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
127	TESTEN	IPD	Scan Test Enable For normal operation, pull-down this pin to ground.
128	SCANEN	IPD	Scan Test Scan Mux Enable For normal operation, pull-down this pin to ground.

Note 2-1 P = power supply; GND = ground; I = input; O = output
I/O = bi-directional
IPU/O = Input with internal pull-up during reset; output pin otherwise.
IPU = Input with internal pull-up.
IPD = Input with internal pull-down.
OPU = Output with internal pull-up.
OPD = Output with internal pull-down.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8993M contains two 10/100 physical layer transceivers and three MAC units with an integrated Layer 2 managed switch.

The KSZ8993M has the flexibility to be used as either a managed or unmanaged design. In a managed design, the host processor has complete control of the KSZ8993M via the SMI interface, MIIM interface, SPI bus, or I^2C bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

On the media side, the KSZ8993M supports IEEE 802.3 10BASE-T and 100BASE-TX on both PHY ports, and 100BASE-FX on PHY port 1. The KSZ8993M can be used as a media converter.

The KSZ8993ML is the single-supply version with all the same features of the KSZ8993M. In the KSZ8993ML version, pin 22 provides 1.8V output power to the KSZ8993ML's V_{DDC}, V_{DDA}, and V_{DDAP} power pins.
Refer to Table 2-1 for information about pin 22.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

3.1 Physical Layer Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01 kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.1.3 PLL CLOCK SYNTHESIZER

The KSZ8893M generates 125 MHz, 31.25 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

3.1.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.1.5 100BASE-FX OPERATION

100BASE-FX operation is similar to 100BASE-TX operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In 100BASE-FX mode, the auto negotiation feature is bypassed since there is no standard that supports fiber auto negotiation. The auto-MDI/MDI-X feature is also disabled.

3.1.6 100BASE-FX SIGNAL DETECTION

In 100BASE-FX operation, the FXSD1 (fiber signal detect) input pin is usually connected to the fiber transceiver's SD (signal detect) output pin. 100BASE-FX mode is activated when the FXSD1 input pin is greater than 1V. When FXSD1 is between 1V and 1.8V, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD1 is over 2.2V, the fiber signal is detected.

Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD1 input pin is tied high to force 100BASE-FX mode.

100BASE-FX signal detection is summarized in Table 3-1.

TABLE 3-1: FX AND TX MODE SELECTION

FXSD1 Input Voltage	Mode
Less than 0.2V	TX mode
Greater than 1V, but less than 1.8V	FX mode No signal detected Far-end fault generated
Greater than 2.2V	FX mode Signal detected

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver's SD output voltage swing to match the FXSD1 pin's input voltage threshold.

3.1.7 100BASE-FX FAR-END FAULT

An FEF occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8993M detects a FEF when its FXSD1 input is between 1.0V and 1.8V. When an FEF occurs, the transmission side signals the other end of the link by sending 84 1's followed by a zero in the idle period between frames.

Upon receiving an FEF, the LINK will go down (even when a fiber signal is detected) to indicate a fault condition. The transmitting side is not affected when an FEF is received and will continue to send out its normal transmit pattern from the MAC. By default, FEF is enabled. The FEF feature can be disabled through register setting.

3.1.8 10BASE-T TRANSMIT

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

3.1.9 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8993M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.10 POWER MANAGEMENT

The KSZ8993M features a per-port power down mode. To save power, the user can power down ports that are not in use by setting the port control registers or MII control registers. In addition, there is a full-chip power down mode. When activated, the entire chip will be shut down.

3.1.11 MDI/MDI-X AUTO CROSSOVER

The KSZ8993M supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the KSZ8993M device. This feature can be extremely useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in Table 3-2.

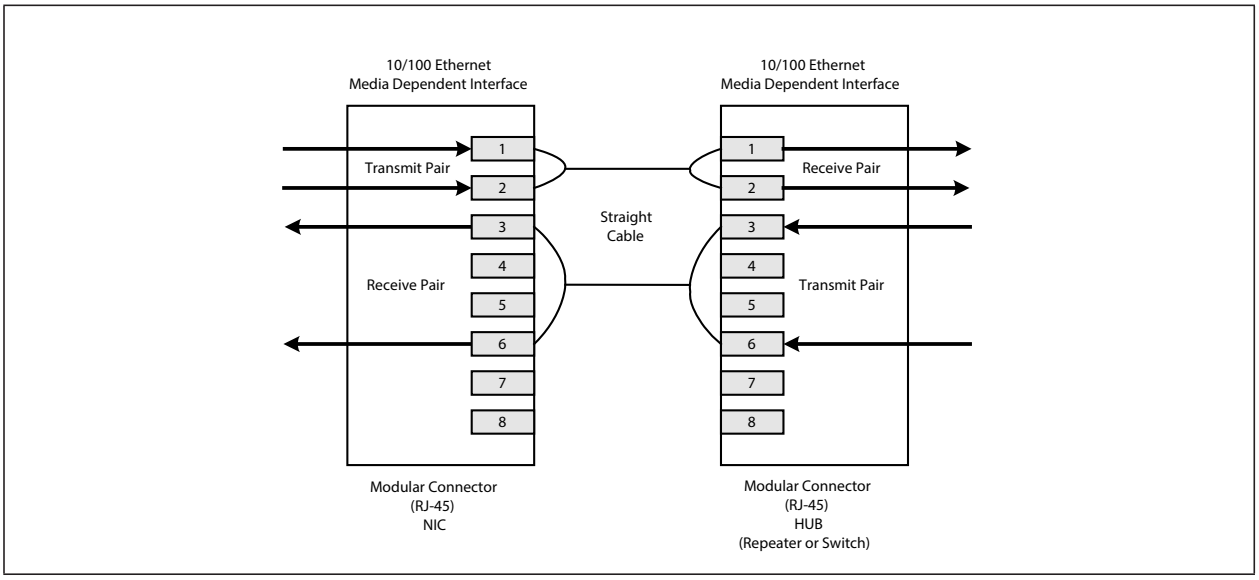
TABLE 3-2: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.1.11.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a NIC card (MDI) and a switch or hub (MDI-X).

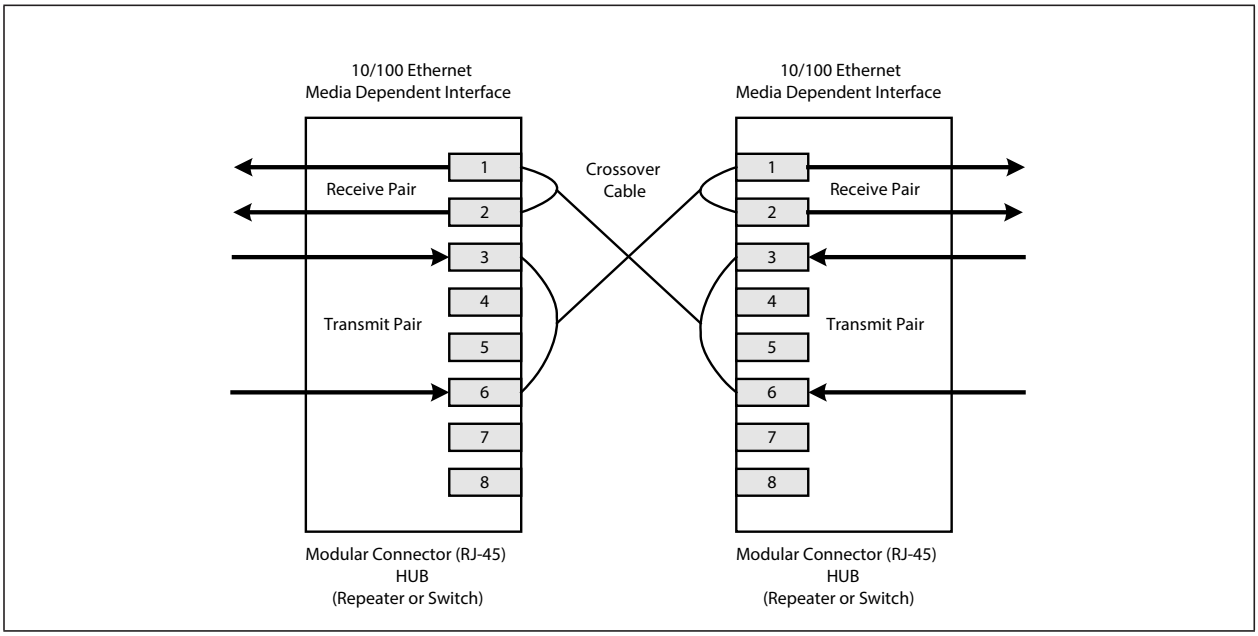
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.1.11.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION

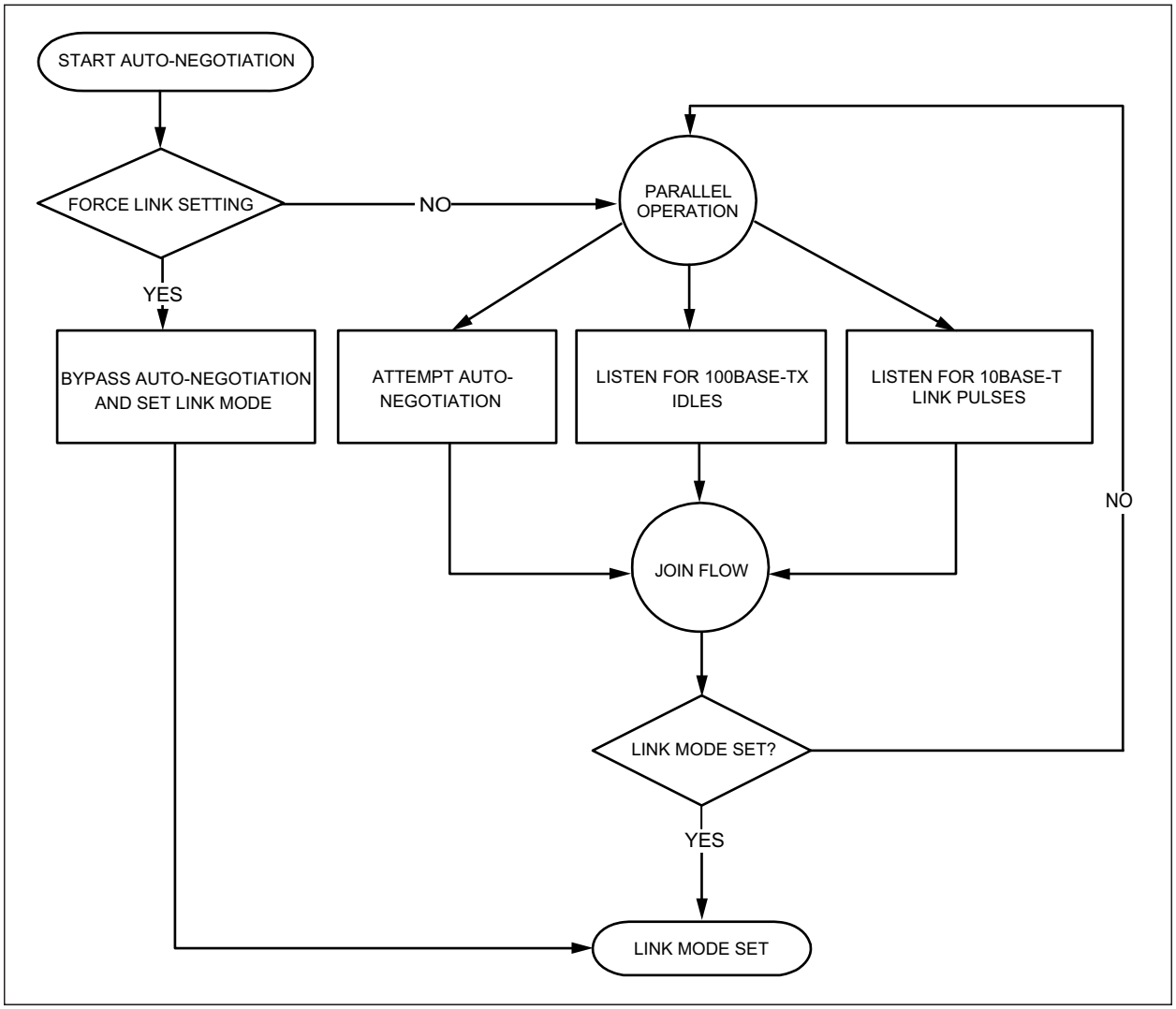


3.1.12 AUTO-NEGOTIATION

The KSZ8993M conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation, the link partners advertise capabilities across the link to each other. If auto-negotiation is not supported or the link partner to the KSZ8993M is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.2 MAC and Switch

3.2.1 ADDRESS LOOKUP

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KSZ8993M is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses that can be learned.

3.2.2 LEARNING

The internal lookup engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the lookup table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

3.2.3 MIGRATION

The internal lookup engine also monitors whether a station has moved. If a station has moved, it will update the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table, but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The lookup engine will update the existing record in the table with the new source port information.

3.2.4 AGING

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and will continuously remove aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through register 3 (0x03).

3.2.5 FORWARDING

The KSZ8993M forwards packets using the algorithm that is depicted in the following flowcharts. Figure 3-4 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with "port to forward 1" (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with "port to forward 2" (PTF2), as shown in Figure 3-5. The packet is sent to PTF2.

FIGURE 3-4: DESTINATION ADDRESS LOOKUP FLOW CHART, STAGE 1

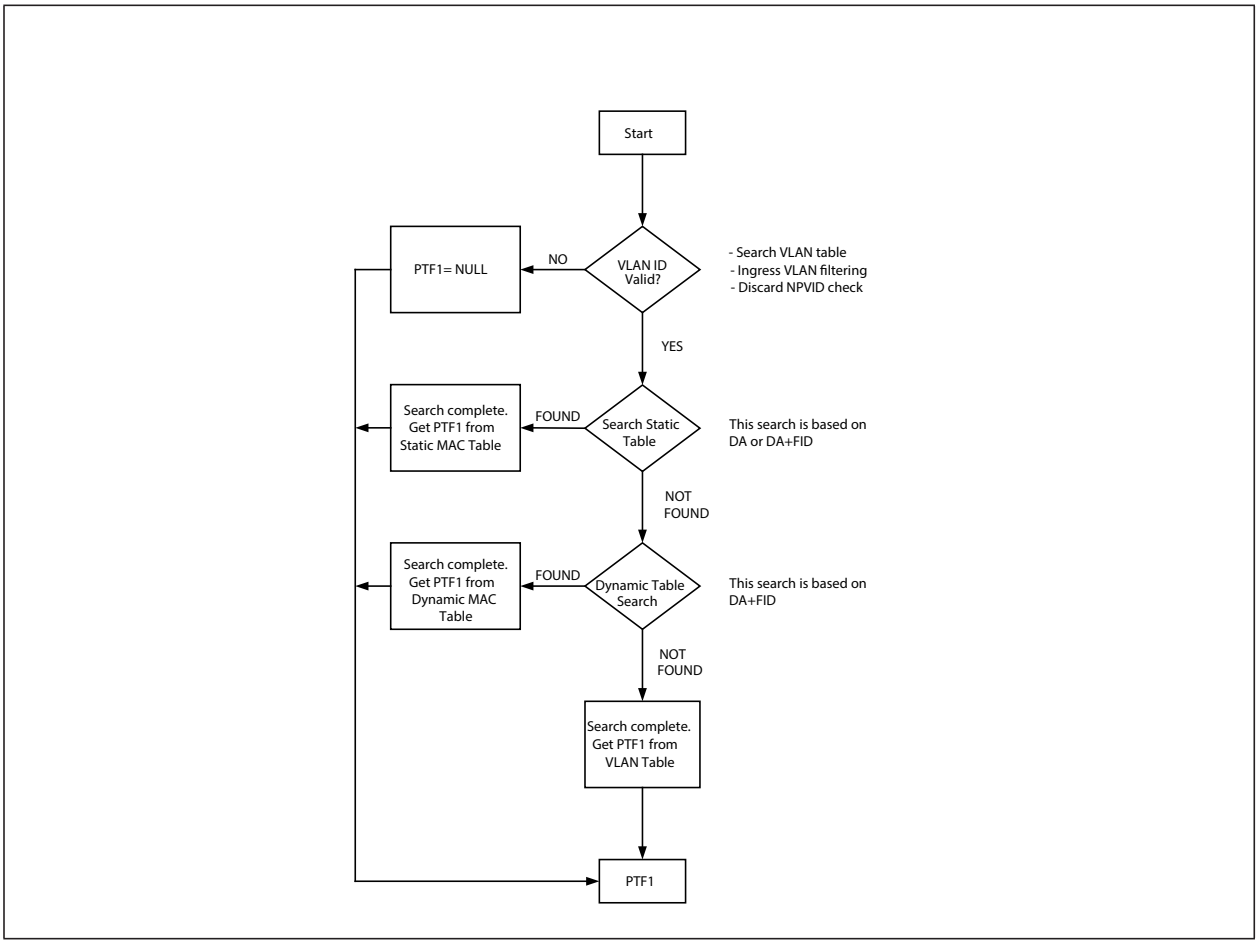
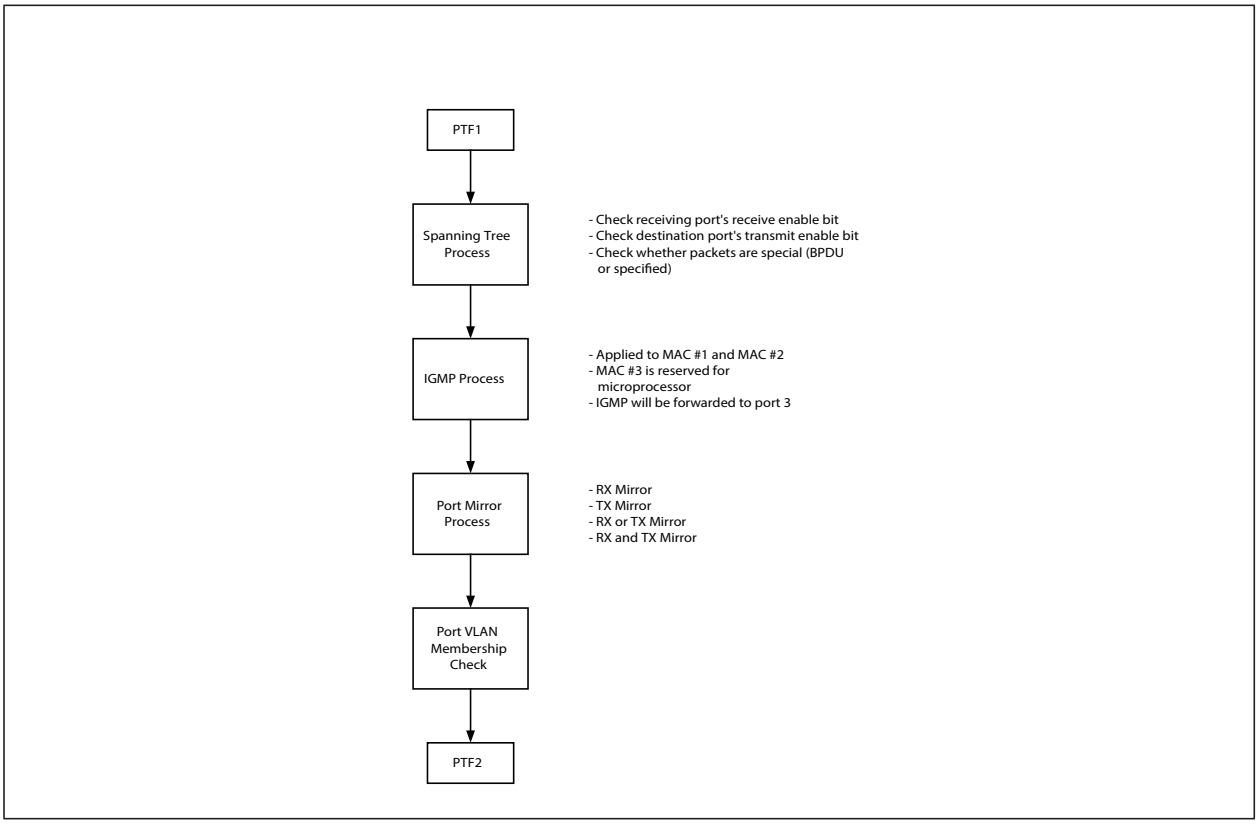


FIGURE 3-5: DESTINATION ADDRESS RESOLUTION FLOW CHART, STAGE 2



The KSZ8993M will not forward the following packets:

- Error packets: These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KSZ8993M will intercept these packets and perform the appropriate actions.
- "Local" packets: Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as local.

3.2.6 SWITCHING ENGINE

The KSZ8993M features a high-performance switching engine to move data to and from the MACs' packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KSZ8993M has a 32 kB internal frame buffer. This resource is shared between all three ports. The buffer sharing mode can be programmed through Global Register 2 (0x02). In one mode, ports are allowed to use any free buffers in the buffer pool. In the second mode, each port is only allowed to use one third of the total buffer pool. There are a total of 250 buffers available. Each buffer is sized at 128B.

3.2.7 MAC OPERATION

The KSZ8993M strictly abides by IEEE 802.3 standards to maximize compatibility.

3.2.7.1 Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bits time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bits time IPG is measured from MCRS and the next MTXEN.

3.2.7.2 Back-Off Algorithm

The KSZ8993M implements the IEEE 802.3 standard for the binary exponential back-off algorithm, and optional "aggressive mode" back-off. After 16 collisions, the packet is optionally dropped depending on the chip configuration in Global Register 3 (0x03).

3.2.7.3 Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

3.2.7.4 Illegal Frames

The KSZ8993M discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Global Register 4 (0x04). For special applications, the KSZ8993M can also be programmed to accept frames up to 1916 bytes in the same global register. Because the KSZ8993M supports VLAN tags, the maximum sizing is adjusted when these tags are present. See the EEPROM section for programming options.

3.2.7.5 Flow Control

The KSZ8993M supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8993M receives a pause control frame, the KSZ8993M will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KSZ8993M will be transmitted.

On the transmit side, the KSZ8993M has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8993M will flow control a port, which just received a packet, if the destination port resource is being used up. The KSZ8993M will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8993M will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being activated and deactivated too many times.

The KSZ8993M will flow control all ports if the receive queue becomes full.

3.2.7.6 Half-Duplex Backpressure

A half-duplex backpressure option (Note: not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full-duplex mode. If backpressure is required, the KSZ8993M will send preambles to defer the other stations' transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, carrier sense type backpressure will be active again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

To ensure no packet loss in 10 BASE-T or 100 BASE-TX half-duplex modes, the user must enable the following:

1. Aggressive back-off (Global Register 3 (0x03), bit 0 or external strap-in pin SMAC = high)
2. No excessive collision drop (Global Register 4 (0x04), bit 3 or external strap-in pin SMAC = high)

These bits are not set as defaults because this is not the IEEE standard.

3.2.7.7 Broadcast Storm Protection

The KSZ8993M has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8993M has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 67 ms interval for 100BT and a 500 ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in register 6 (0x06) and 7 (0x07). The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec × 67 ms/interval × 1% = 99 frames/interval (approx.) = 0x63

3.2.8 MII INTERFACE OPERATION

The MII is specified by the IEEE 802.3 standards committee and provides a common interface between physical layer and MAC layer devices. The MII Interface provided by the KSZ8993M is connected to the device's third MAC. The interface contains two distinct groups of signals: one for transmission and the other for reception. Table 3-3 describes the signals used by the MII bus.

TABLE 3-3: MII SIGNALS

KSZ8993 Port 3 MAC3 PHY Mode Connections		Pin Description	KSZ8993 Port 3 MAC3 MAC Mode Connections	
External MAC MII Signals	**KSZ8993M MII Signals**		**External PHY MII Signals**	**KSZ8993M MAC3 MII Signals**
MTXEN	SMTXEN	Transmit Enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit Error	MTXER	(NOT USED)
MTXD3	SMTXD[3]	Transmit Data Bit 3	MTXD3	SMRXD[3]
MTXD2	SMTXD[2]	Transmit Data Bit 2	MTXD2	SMRXD[2]
MTXD1	SMTXD[1]	Transmit Data Bit 1	MTXD1	SMRXD[1]
MTXD0	SMTXD[0]	Transmit Data Bit 0	MTXD0	SMRXD[0]
MTXC	SMTXC	Transmit Clock	MTXC	SMRXC
MCOL	SCOL	Collision Detection	MCOL	SCOL
MCRS	SCRS	Carrier Sense	MCRS	SCRS
MRXDV	SMRXDV	Receive Data Valid	MRXDV	SMTXEN
MRXER	(NOT USED)	Receive Error	MRXER	SMTXER
MRXD3	SMRXD[3]	Receive Data Bit 3	MRXD3	SMTXD[3]
MRXD2	SMRXD[2]	Receive Data Bit 2	MRXD2	SMTXD[2]
MRXD1	SMRXD[1]	Receive Data Bit 1	MRXD1	SMTXD[1]
MRXD0	SMRXD[0]	Receive Data Bit 0	MRXD0	SMTXD[0]
MRXC	SMRXC	Receive Clock	MRXC	SMTXC

The MII operates in either PHY mode or MAC mode. The data interface is a nibble wide and runs at one-quarter the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error has occurred during transmission. Similarly, the receive side has signals that convey when the data is valid and without physical layer errors. For half-duplex operation, there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the interface for PHY mode operation and the signal MTXER is not provided on the interface for MAC mode operation. Normally MRXER would indicate a receive error coming from the physical layer device. MTXER would indicate a transmit error from the MAC device. These signals are not appropriate for this configuration. For PHY mode operation, if the device interfacing with the KSZ8993M has an MRXER pin, it should be tied low. For MAC mode operation, if the device interfacing with the KSZ8993M has an MTXER pin, it should be tied low.

3.2.9 SNI (7-WIRE) OPERATION

The serial network interface (SNI), or 7-wire, is compatible with some controllers used for network layer protocol processing. In SNI mode, the KSZ8993M acts like a PHY and the external controller functions as the MAC. The KSZ8993M can interface directly with external controllers using the 7-wire interface. These signals are divided into two groups, one for transmission and the other for reception. The signals involved are described in the following table.

TABLE 3-4: SNI SIGNALS

Pin Description	External MAC Controller Signal	KSZ8993M PHY Signal
Transmit enable	TXEN	SMTXEN
Serial transmit data	TXD	SMTXD[0]
Transmit clock	TXC	SMTXC
Collision detection	COL	SCOL

TABLE 3-4: SNI SIGNALS (CONTINUED)

Pin Description	External MAC Controller Signal	KSZ8993M PHY Signal
Carrier sense	CRS	SMRXDV
Serial receive data	RXD	SMRXD[0]
Receive clock	RXC	SMRXC

The SNI interface is a bit wide data interface and, therefore, runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Similarly, the receive side has an indicator that conveys when the data is valid.

For half-duplex operation, the SCOL signal is used to indicate that a collision has occurred during transmission.

3.2.10 MII MANAGEMENT (MIIM) INTERFACE

The KSZ8993M supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8993M. An external device with MDC/MDIO capability is used to read the PHY status or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4.5 of the IEEE 802.3u Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8993M device.
- Access to a set of eight 16-bit registers, consisting of six standard MIIM registers [0:5].

The MIIM Interface can operate up to a maximum clock speed of 5 MHz.

Table 3-5 depicts the MII Management Interface frame format.

TABLE 3-5: MII MANAGEMENT INTERFACE FRAME FORMAT

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	xx0AA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	xx0AA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

For the KSZ8993M, MIIM register access is selected when bit 2 of the PHY address is set to '0'. PHY address bits [4:3] are not defined for MIIM register access, and can be set to either 0's or 1's in read/write operation.

3.2.11 SERIAL MANAGEMENT INTERFACE (SMI)

The SMI is the KSZ8993M non-standard MIIM interface that provides access to all KSZ8993M configuration registers. This interface allows an external device to completely monitor and control the states of the KSZ8993M.

The SMI interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8993M device.
- Access to all KSZ8993M configuration registers. Register access includes the Global, Port, and Advanced Control Registers 0-127 (0x00 – 0x7F), and indirect access to the standard MIIM registers [0:5].

Table 3-6 depicts the SMI frame format.

TABLE 3-6: SERIAL MANAGEMENT INTERFACE (SMI) FRAME FORMAT

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	RR1xx	RRRRR	Z0	0000_0000_DDDD_DDDD	Z
Write	32 1's	01	01	RR1xx	RRRRR	10	xxxx_xxxx_DDDD_DDDD	Z

For the KSZ8993M, SMI register access is selected when bit 2 of the PHY address is set to '1'. PHY address bits [1:0] are not defined for SMI register access, and can be set to either 0's or 1's in read/write operation.

To access the KSZ8993M registers 0-127 (0x00 – 0x7F), the following applies:

- PHYAD[4:3] and REGAD[4:0] are concatenated to form the 7-bits address; that is, {PHYAD[4:3], REGAD[4:0]} = bits [6:0] of the 7-bits address.
- Registers are 8 data bits wide.
  - For read operation, data bits [15:8] are read back as 0's.
  - For write operation, data bits [15:8] are not defined, and can be set to either '0's or '1's.

SMI register access is the same as the MIIM register access, except for the register access requirements presented in this section.

3.3 Advanced Switch Functions

3.3.1 SPANNING TREE SUPPORT

To support spanning tree, port 3 is designated as the processor port.

The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via "transmit enable", "receive enable", and "learning disable" register settings in registers 18 and 34 for ports 1 and 2, respectively. Table 3-7 shows the port setting and software actions taken for each of the five spanning tree states.

TABLE 3-7: SPANNING TREE STATES

Disable State	**Port Setting**	**Software Action**
The port should not forward or receive any packets. Learning is disabled.	"transmit enable = 0, receive enable = 0, learning disable =1"	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the "Static MAC table" with "overriding bit" set) and the processor should discard those packets. Address learning is disabled on the port in this state. Note: processor is connected to port 3 via MII interface.
Blocking State	**Port Setting**	**Software Action**
Only packets to the processor are forwarded. Learning is disabled.	"transmit enable = 0, receive enable = 0, learning disable =1"	The processor should not send any packets to the port(s) in this state. The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is disabled.	"transmit enable = 0, receive enable = 0, learning disable =1"	The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See Upstream Special Tagging Mode for details. Address learning is disabled on the port in this state.
Learning State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is enabled.	"transmit enable = 0, receive enable = 0, learning disable = 0"	The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See Upstream Special Tagging Mode for details. Address learning is enabled on the port in this state.
Forwarding State	**Port Setting**	**Software Action**
Packets are forwarded and received normally. Learning is enabled.	"transmit enable = 1, receive enable = 1, learning disable = 0"	The processor programs the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. See Upstream Special Tagging Mode for details. Address learning is enabled on the port in this state.

3.3.2 UPSTREAM SPECIAL TAGGING MODE

Upstream Special Tagging Mode is designed for spanning tree protocol IGMP snooping and is flexible for use in other applications. Upstream Special Tagging, similar to 802.1Q Tagging, requires software to change network drivers to insert/modify/strip/interpret the special tag. This mode is enabled by setting both register 11 bit [0] and register 48 bit [2] to '1'.

TABLE 3-8: UPSTREAMSPECIAL TAGGING MODE FORMAT

802.1Q Tag Format	Special Tag Format
TPID (tag protocol identifier, 0x8100) + TCI	STPID (special tag identifier, 0x810 + 4 bit for "port mask") + TCI

The STPID is only seen and used by the port 3 interface, which should be connected to a processor. The KSZ8993M uses a non-zero "port mask" to bypass the lookup result and override any port setting, regardless of port states (disable, blocking, listening, learning).

For packets from regular ports (port 1 & port 2) to port 3, the port mask is used to tell the processor which port the packets were received on, defined as follows:

- "0001", from port 1
- "0010", from port 2

No port mask values, other than the previous two defined ones, should be received in Upstream Special Tagging Mode. Table 3-9 below shows the processor to switch egress rules when dealing with STPID.

TABLE 3-9: STPID EGRESS RULES (PROCESSOR TO SWITCH PORT 3)

Ingress Tag Field	Egress Action to Tag Field
Tagged with 0x8100 + TCI	- Modify TPID to 0x810 + "port mask", which indicates source port. - Recalculate CRC. - No change to TCI if VID is not null. - Replace null VID with ingress port VID.
Not tagged	- Insert TPID to 0x810 + "port mask", which indicates source port. - Insert TCI with ingress port VID. - Recalculate CRC.

3.3.3 IGMP SUPPORT

For IGMP support in layer 2, the KSZ8993M provides two components:

3.3.3.1 IGMP Snooping

The KSZ8993M traps IGMP packets and forwards them only to the processor (port 3). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

3.3.3.2 Multicast Address Insertion in the Static MAC Table

Once the multicast address is programmed in the Static MAC Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

To enable IGMP support, set register 5 bit [6] to '1'. Also, Special Tagging Mode needs to be enabled, so that the processor knows which port the IGMP packet was received on. This is achieved by setting both register 11 bit [0] and register 48 bit [2] to '1'.

3.3.4 PORT MIRRORING SUPPORT

KSZ8993M supports port mirroring comprehensively as:

- **"Receive Only" mirror on a port:** All the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "receive sniff" and port 3 is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8993M forwards the packet to both port 2 and port 3. The KSZ8993M can optionally even forward "bad" received packets to the "sniffer port".
- **"Transmit Only" mirror on a port:** All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "transmit sniff" and port 3 is programmed to be the "sniffer port". A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8993M forwards the packet to both port 1

and port 3.

- **“Receive and Transmit” mirror on two ports:** All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the “AND” feature, set register 5 bit [0] to ‘1’. For example, port 1 is programmed to be “receive sniff”, port 2 is programmed to be “transmit sniff”, and port 3 is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8993M forwards the packet to both port 2 and port 3.

Multiple ports can be selected as “receive sniff” or “transmit sniff”. In addition, any port can be selected as the “sniffer port”. All these per port features can be selected through registers 17, 33, and 49 for ports 1, 2, and 3, respectively.

3.3.5 IEEE 802.1Q VLAN SUPPORT

The KSZ8993M supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8993M provides a 16-entry VLAN Table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for look-up. In VLAN mode, the look-up process starts with VLAN Table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning.

TABLE 3-10: FID+DA LOOKUP IN VLAN MODE

DA Found in Static MAC Table?	Use FID Flag?	FID Match?	FID+DA Found in Dynamic MAC Table?	Action
No	Don’t care	Don’t care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
No	Don’t care	Don’t care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	0	Don’t care	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	1	Yes	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]

TABLE 3-11: FID+SA LOOKUP IN VLAN MODE

FID+SA Found in Dynamic MAC Table?	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

Advanced VLAN features, such as “Ingress VLAN filtering” and “Discard Non PVID packets” are also supported by the KSZ8993M. These features can be set on a per port basis, and are defined in register 18, bit 6 and bit 5, respectively for port 1.

3.3.6 QOS PRIORITY SUPPORT

The KSZ8993M provides Quality of Service (QoS) for applications such as VoIP and video conferencing. The KSZ8993M per port transmit queue could be split into two priority queues: a high priority queue and a low priority queue. Bit 0 of registers 16, 32 and 48 is used to enable split transmit queues for ports 1, 2 and 3, respectively. Optionally, the Px_TXQ2 strap-in pins can be used to enable this feature. With split transmit queues, high priority packets will be placed in the high priority queue and low priority packets will be placed in the low priority queue.

For split transmit queues, the KSZ8993M provides four priority schemes:

- Transmit all high priority packets before low priority packets; i.e., a low priority packet can be transmitted only when the high priority queue is empty.
- Transmit high priority packets and low priority packets at 10:1 ratio; i.e., transmit a low priority packet after 10 high priority packets have been transmitted, if both queues are busy.
- Transmit high priority packets and low priority packets at 5:1 ratio.
- Transmit high priority packets and low priority packets at 2:1 ratio.

If a port's transmit queue is not split, both high priority packets and low priority packets have equal priority in the transmit queue. Register 5 bits [3:2] are used to select the desired priority scheme. Optionally, the PRSEL1 and PRSEL0 strap-in pins can be used.

3.3.7 PORT-BASED PRIORITY

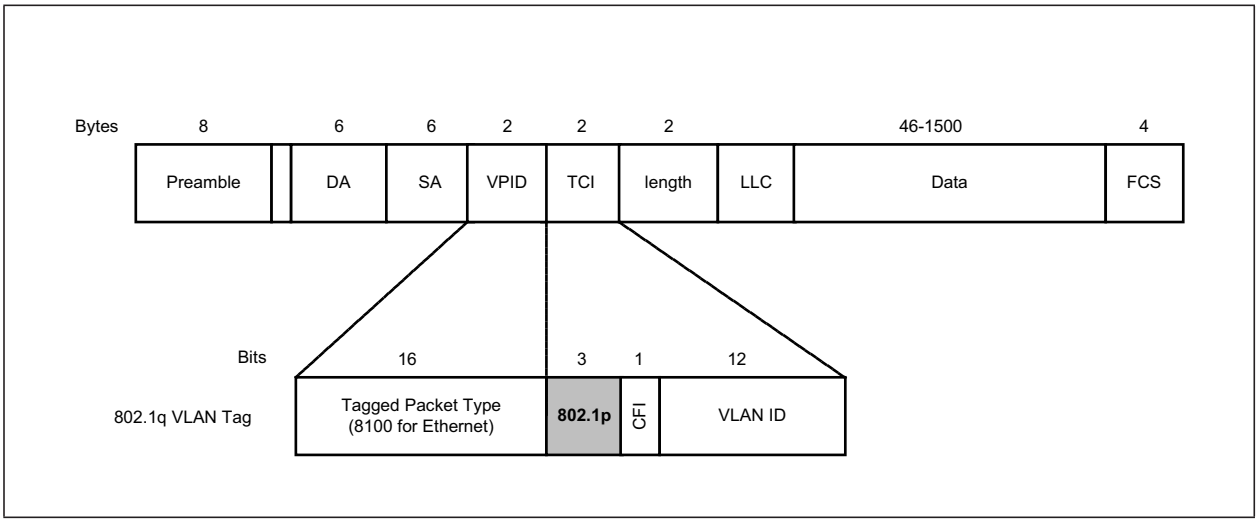
With port-based priority, each ingress port is individually classified as a high priority receiving port. All packets received at the high priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits [4:3] of registers 16, 32, and 48 are used to enable port-based priority for ports 1, 2, and 3, respectively. Optionally, the Px_PP strap-in pins can be used to enable this feature.

3.3.8 802.1P-BASED PRIORITY

For 802.1p-based priority, the KSZ8993M examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the “priority base” value, as specified by register 2 bits [6:4]. The “priority base” value is programmable; its default value is 0x4.

Figure 3-6 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 3-6: 802.1P PRIORITY FIELD FORMAT



If an ingress packet has an equal or higher priority value than the "priority base" value, the packet will be placed in the high priority transmit queue if the corresponding transmit queue is split. 802.1p based priority is enabled by bit 5 of registers 16, 32 and 48 for ports 1, 2 and 3, respectively. Optionally, the Px_1PEN strap-in pins can be used to enable this feature.

The KSZ8993M provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN Protocol ID (VPID) and the 2 bytes Tag Control Information field (TCI), is also referred to as the 802.1Q VLAN Tag.

Tag Insertion is enabled by bit 2 of registers 16, 32, and 48 for ports 1, 2, and 3, respectively. Optionally, the Px_TAGINS strap-in pins can be used to enable this feature. At the egress port, untagged packets are tagged with the ingress port’s default tag. The default tags are programmed in register sets {19,20}, {35,36}, and {51,52} for ports 1, 2, and 3, respectively. The KSZ8993M will not add tags to already tagged packets.

Tag Removal is enabled by bit 1 of registers 16, 32, and 48 for ports 1, 2, and 3, respectively. Optionally, the Px_TAGRM strap-in pins can be used to enable this feature. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8993M will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

802.1p Priority Field Re-mapping is a QoS feature that allows the KSZ8993M to set the "User Priority Ceiling" at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field. The "User Priority Ceiling" is enabled by bit 3 of registers 16, 32, and 48 for ports 1, 2, and 3, respectively.

3.3.9 DIFFSERV-BASED PRIORITY

DiffServ-based priority uses registers 96 to 103. More details are provided at the beginning of the Advanced Control Registers section.

3.3.10 RATE LIMITING SUPPORT

The KSZ8993M supports hardware rate limiting independently on the "receive side" and on the "transmit side" on a per port basis. Rate limiting is supported in both priority and non-priority environment. The rate limit starts from 0 kbps and goes up to the line rate in steps of 32 kbps. The KSZ8993M uses "one second" as the rate limiting interval. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval.

On the "receive side", if the number of bytes exceeds the programmed limit, the switch will stop receiving packets on the port until the "one second" interval expires. Flow control can be enabled to prevent packet loss. If the rate limit is programmed greater than or equal to 128 kbps and the byte counter is 8 Kbytes below the limit, flow control will be triggered. If the rate limit is programmed lower than 128 kbps and the byte counter is 2 Kbytes below the limit, flow control will also be triggered.

On the "transmit side", if the number of bytes exceeds the programmed limit, the switch will stop transmitting packets on the port until the "one second" interval expires.

If priority is enabled, the KSZ8993M can be programmed to support different rate limits for high priority packets and low priority packets.

3.4 Configuration Interface

The KSZ8993M can operate as both a managed switch and an unmanaged switch.

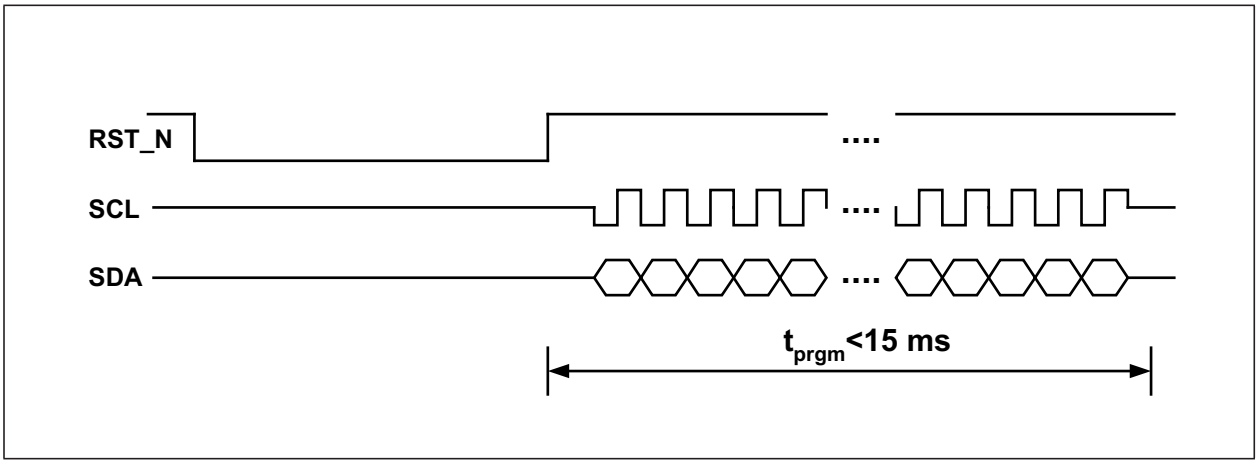
In unmanaged mode, the KSZ8993M is typically programmed using an EEPROM. If no EEPROM is present, the KSZ8993M is configured using its default register settings. Some default settings are configured via strap-in pin options. The strap-in pins are indicated in Table 2-1.

3.4.1 I^2C MASTER SERIAL BUS CONFIGURATION

With an additional I^2C ("2-wire") EEPROM, the KSZ8993M can perform more advanced switch features like "broadcast storm protection" and "rate control" without the need of an external processor.

For KSZ8993M I^2C Master configuration, the EEPROM stores the configuration data for register 0 to register 109 (as defined in the KSZ8993M register map) with the exception of the "Read Only" status registers. After the de-assertion of reset, the KSZ8993M sequentially reads in the configuration data for all 110 registers, starting from register 0. The configuration access time (t_{prgm}) is less than 15 ms, as depicted in Figure 3-7.

FIGURE 3-7: EEPROM CONFIGURATION TIMING DIAGRAM



The following is a sample procedure for programming the KSZ8993M with a pre-configured EEPROM:

1. Connect the KSZ8993M to the EEPROM by joining the SCL and SDA signals of the respective devices. For the KSZ8993M, SCL is pin 97 and SDA is pin 98.
2. Enable I^2C master mode by setting the KSZ8993M strap-in pins, PS[1:0] (pins 100 and 101, respectively) to “00”.
3. Check to ensure that the KSZ8993M reset signal input, RST_N (pin 67), is properly connected to the external reset source at the board level.
4. Program the desired configuration data into the EEPROM.
5. Place the EEPROM on the board and power up the board.
6. Assert an active-low reset to the RSTN pin of the KSZ8993M. After reset is de-asserted, the KSZ8993M begins reading the configuration data from the EEPROM. The KSZ8993M checks that the first byte read from the EEPROM is “93”. If this value is correct, EEPROM configuration continues. If not, EEPROM configuration access is denied and all other data sent from the EEPROM is ignored by the KSZ8993M. The configuration access time (t_{prgm}) is less than 15 ms.

For proper operation, ensure that the KSZ8993M PWRDN input signal (pin 36) is not asserted during the reset operation. The PWRDN input is active-low.

3.4.2 I^2C SLAVE SERIAL BUS CONFIGURATION

In managed mode, the KSZ8993M can be configured as an I^2C slave device. In this mode, an I^2C master device (external controller/CPU) has complete programming access to the KSZ8993M’s 128 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers, and indirect access to the “Static MAC Table”, “VLAN Table”, “Dynamic MAC Table,” and “MIB Counters.” The tables and counters are indirectly accessed via registers 110 to 120.

In I^2C slave mode, the KSZ8993M operates like other I^2C slave devices. Addressing the KSZ8993M’s 8-bit registers is similar to addressing the Microchip AT24C02 EEPROM’s memory locations. Details of I^2C read/write operations and related timing information can be found in the AT24C02 data sheet.

Two fixed 8-bit device addresses are used to address the KSZ8993M in I^2C slave mode. One is for read; the other is for write. The addresses are as follows:

- 1011_1111 <read>
- 1011_1110 <write>

The following is a sample procedure for programming the KSZ8993M using the I^2C slave serial bus:

1. Enable I^2C slave mode by setting the KSZ8993M strap-in pins PS[1:0] (pins 100 and 101, respectively) to “01”.
2. Power up the board and assert reset to the KSZ8993M. After reset, the “Start Switch” bit (register 1 bit [0]) is set to ‘0’.
3. Configure the desired register settings in the KSZ8993M using the I^2C write operation.
4. Read back and verify the register settings in the KSZ8993M using the I^2C read operation.
5. Write a ‘1’ to the “Start Switch” bit to start the KSZ8993M with the programmed settings.

The “Start Switch” bit cannot be set to ‘0’ to stop the switch after a ‘1’ is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the “Start Switch” bit is set to ‘1’.

Some of the configuration settings, such as “Aging Enable”, “Auto Negotiation Enable”, “Force Speed”, and “Power down” can be programmed after the switch has been started.

3.4.3 SPI SLAVE SERIAL BUS CONFIGURATION

In managed mode, the KSZ8993M can be configured as a SPI slave device. In this mode, a SPI master device (external controller/CPU) has complete programming access to the KSZ8993M’s 128 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the “Static MAC Table”, “VLAN Table”, “Dynamic MAC Table” and “MIB Counters”. The tables and counters are indirectly accessed via registers 110 to 120.

The KSZ8993M supports two standard SPI commands: ‘0000_0011’ for data read and ‘0000_0010’ for data write. SPI multiple read and multiple write are also supported by the KSZ8993M to expedite register read back and register configuration, respectively.

SPI multiple read is initiated when the master device continues to drive the KSZ8993M SPIS_N input pin (SPI Slave Select signal) low after a byte (a register) is read. After the read, the KSZ8993M internal address counter increments automatically to the next byte (next register) after the read. The next byte at the next register address is shifted out onto the KSZ8993M SPIQ output pin. SPI multiple read continues until the SPI master device terminates it by deasserting the SPIS_N signal to the KSZ8993M.

Similarly, SPI multiple write is initiated when the master device continues to drive the KSZ8993M SPIS_N input pin low after a byte (a register) is written. The KSZ8993M internal address counter increments automatically to the next byte (next register) after the write. The next byte that is sent from the master device to the KSZ8993M SDA input pin will be written to the next register address. SPI multiple write will continue until the SPI master device terminates it by de-asserting the SPIS_N signal to the KSZ8993M.

For both SPI multiple read and multiple write, the KSZ8993M internal address counter wraps back to register address zero once the highest register address is reached. This feature allows all 128 KSZ8993M registers to be read or written with a single SPI command from any initial register address.

The KSZ8993M is capable of supporting a 5 MHz SPI bus.

The following is a sample procedure for programming the KSZ8993M using the SPI bus:

1. At the board level, connect the KSZ8993M pins as follows:

TABLE 3-12: SPI CONNECTIONS

Pin Number	Signal Name	External Processor Signal Description
99	SPIS N	SPI Slave Select
97	SCL (SPIC)	SPI Clock
98	SDA (SPID)	SPI Data (Master output; Slave input)
96	SPIQ	SPI Data (Master input; Slave output)

2. Enable SPI slave mode by setting the KSZ8993M strap-in pins PS[1:0] (pins 100 and 101, respectively) to “10”.
3. Power up the board and assert reset to the KSZ8993M. After reset, the “Start Switch” bit (register 1 bit [0]) is set to ‘0’.
4. Configure the desired register settings in the KSZ8993M using the SPI write or multiple write command.
5. Read back and verify the register settings in the KSZ8993M using the SPI read or multiple read command.
6. Write a ‘1’ to the “Start Switch” bit to start the KSZ8993M with the programmed settings.

The “Start Switch” bit cannot be set to ‘0’ to stop the switch after a ‘1’ is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the “Start Switch” bit is set to ‘1’.

Some of the configuration settings, such as “Aging Enable,” “Auto Negotiation Enable,” “Force Speed,” and “Power Down” can be programmed after the switch has been started.

The following four figures illustrate the SPI data cycles for “Write,” “Read,” “Multiple Write,” and “Multiple Read.” The read data is registered out of SPIQ on the falling edge of SPIC, and the data input on SPID is registered on the rising edge of SPIC.

FIGURE 3-8: SPI WRITE DATA CYCLE

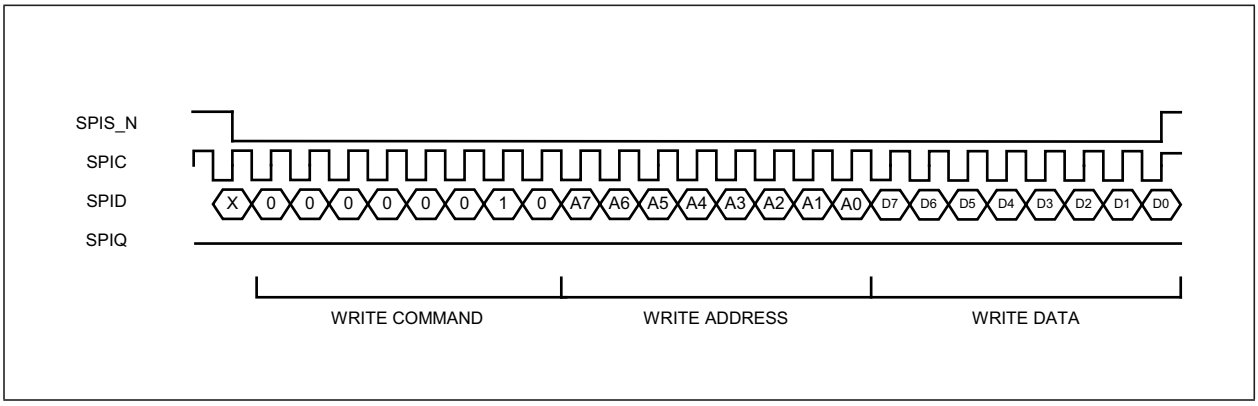


FIGURE 3-9: SPI READ DATA CYCLE

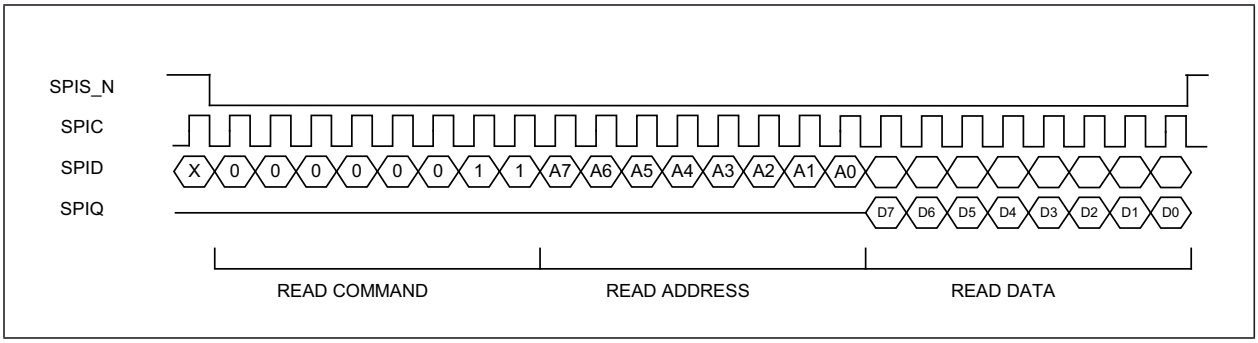


FIGURE 3-10: SPI MULTIPLE WRITE

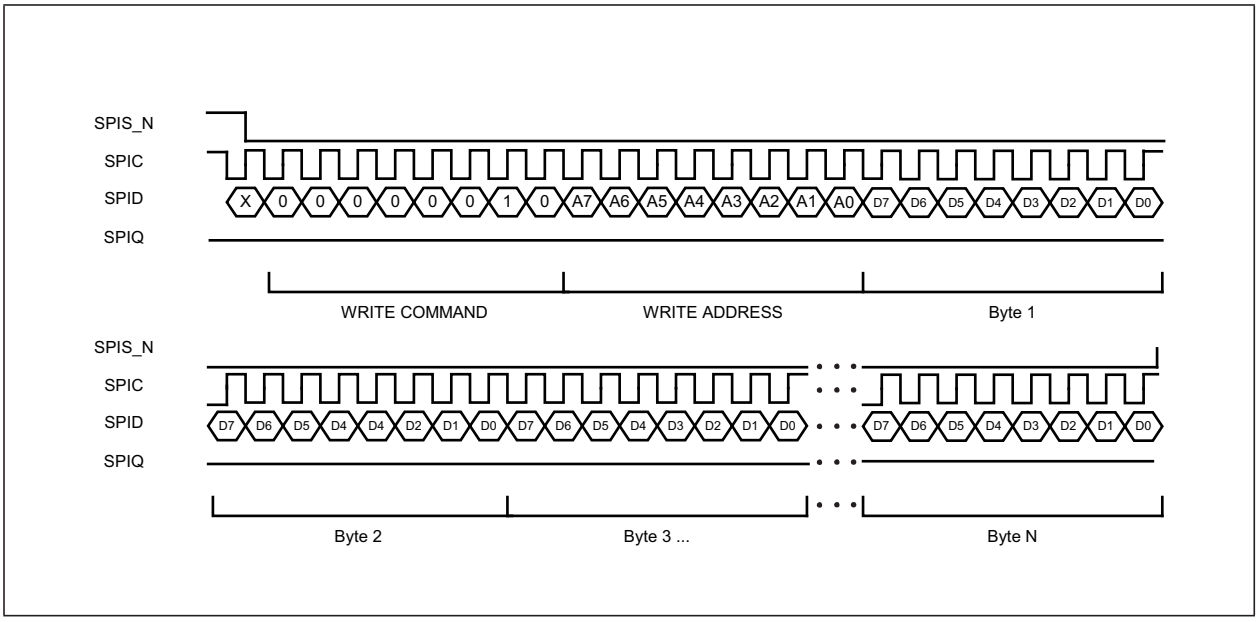
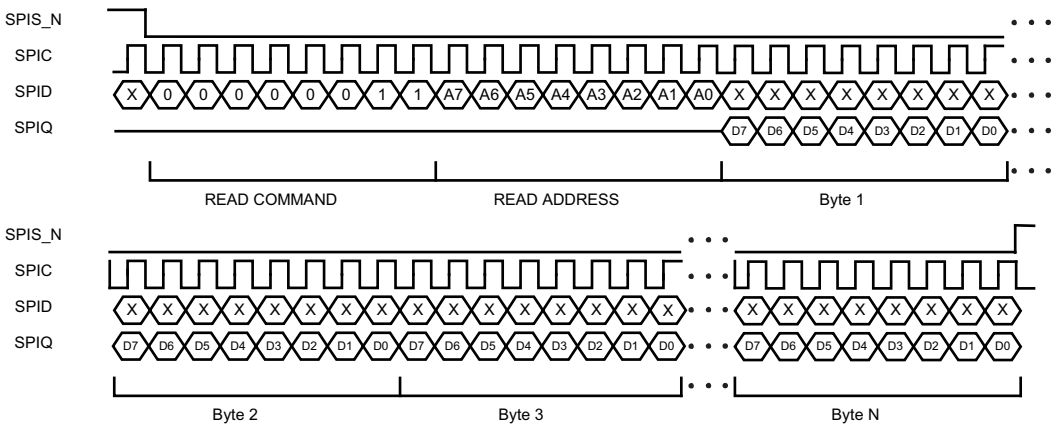


FIGURE 3-11: SPI MULTIPLE READ



3.5 Loopback Support

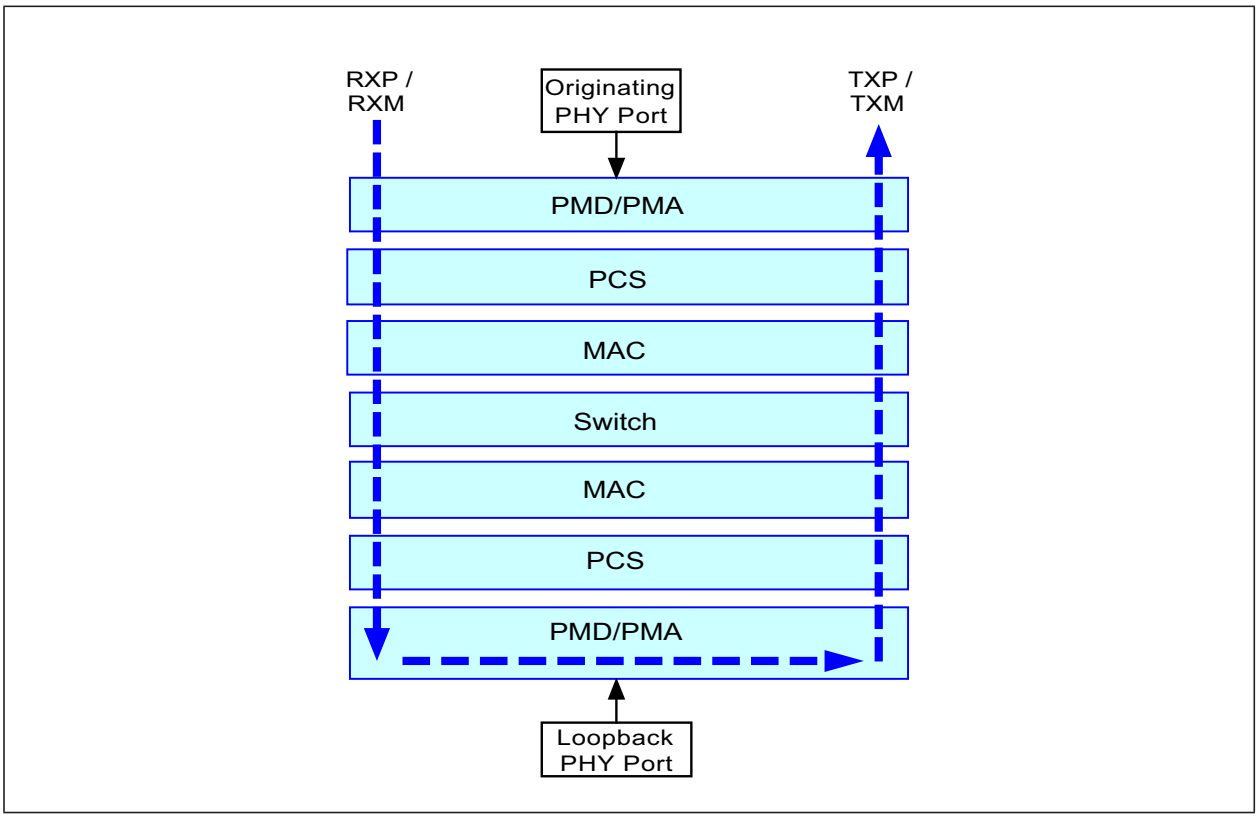
The KSZ8993M provides loopback support for remote diagnostic of failure. In loopback mode, the speed at both PHY ports needs to be set to 100BASE-TX, and the “Priority Buffer reserve” bit needs to be set to 48 preallocated buffers per output queue. The latter is required to prevent loopback packet drops and is achieved by setting register 4 bit 0 to ‘1’.

Bit 0 of registers 29 and 45 is used to enable loopback for ports 1 and 2, respectively.

Alternatively, the MII Management register 0, bit 14 can be used to enable loopback.

Loopback is conducted between the KSZ8993M’s two PHY ports. The loopback path starts at the “Originating.” PHY ports receive inputs (RXP/RXM), wraps around at the “loopback” PHY port’s PMD/PMA, and ends at the “Originating” PHY port’s transmit outputs (TXP/TXM). The KSZ8993M loopback path is illustrated in the following figure.

FIGURE 3-12: LOOPBACK PATH



4.0 REGISTER DESCRIPTIONS

4.1 MII Management (MIIM) Registers

The MIIM interface is used to access the MII PHY registers defined in this section. The SPI, I^2C, and SMI interfaces can also be used to access these registers. The latter three interfaces use a different mapping mechanism than the MIIM interface.

As defined in the IEEE 802.3 specification, the “PHYAD” are assigned as “0x1” for PHY port 1 and “0x2” for PHY port 2. The “REGAD” supported are 0,1,2,3,4, and 5.

TABLE 4-1: MIIM REGISTERS FOR KSZ8993M

Register Number	Description
0x0	Basic Control Register
0x1	Basic Status Register
0x2	Physical Identifier I
0x3	Physical Identifier II
0x4	Auto-Negotiation Advertisement Register
0x5	Auto-Negotiation Link Partner Ability Register
0x6 – 0x1F	Not supported

4.2 Register Descriptions

TABLE 4-2: REGISTER DESCRIPTIONS

Bit	Name	R/W	Description	Default	Reference
Register 0: MII Basic Control					
15	Soft Reset	RO	Not Supported	0	—
14	Loopback	R/W	1 = Loopback mode 0 = Normal operation	0	Reg. 29, bit 0 Reg. 45, bit 0
13	Force 100	R/W	1 = 100 Mbps 0 = 10 Mbps	0	Reg. 28, bit 6 Reg. 44, bit 6
12	AN Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	1	—
11	Power Down	R/W	1 = Power down 0 = Normal operation	0	Reg. 29, bit 3 Reg. 45, bit 3
10	Isolate	RO	Not Supported	0	—
9	Restart AN	R/W	1 = Restart auto-negotiation 0 = Normal operation	0	Reg. 29, bit 5 Reg. 45, bit 5
8	Force Full-Duplex	R/W	1 = Full-duplex 0 = Half-duplex	0	Reg. 28, bit 5 Reg. 44, bit 5
7	Collision Test	RO	Not Supported	0	—
6	Reserved	RO	—	0	—
5	Reserved	RO	—	0	—
4	Force MDI	R/W	1 = Force MDI (transmit on RXP/RXM pins) 0 = Normal operation (transmit on TXP/TXM pins)	0	Reg. 29, bit 1 Reg. 45, bit 1
3	Disable MDIX	R/W	1 = Disable auto MDI-X 0 = Normal operation	0	Reg. 29, bit 2 Reg. 45, bit 2
2	Disable Far-End Fault	R/W	1 = Disable far-end fault detection 0 = Normal operation	0	Reg. 29, bit 4
1	Disable Transmit	R/W	1 = Disable transmit 0 = Normal operation	0	Reg. 29, bit 6 Reg. 45, bit 6

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Bit	Name	R/W	Description	Default	Reference
0	Disable LED	R/W	1 = Disable LED 0 = Normal operation	0	Reg. 29, bit 7 Reg. 45, bit 7
Register 1: MII Basic Status					
15	T4 Capable	RO	0 = Not 100BASE-T4 capable	0	—
14	100 Full Capable	RO	1 = 100BASE-TX full-duplex capable 0 = Not capable of 100BASE-TX full-duplex	1	Always 1
13	100 Half Capable	RO	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	1	Always 1
12	10 Full Capable	RO	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1	Always 1
11	10 Half Capable	RO	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1	Always 1
10-7	Reserved	RO	—	0000	—
6	Preamble Suppressed	RO	Not Supported	0	—
5	AN Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation not completed	0	Reg. 30, bit 6 Reg. 46, bit 6
4	Far-End Fault	RO	1 = Far-end fault detected 0 = No far-end fault detected	0	Reg. 31, bit 0
3	AN Capable	RO	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1	Reg. 28, bit 7 Reg. 44, bit 7
2	Link Status	RO	1 = Link is up 0 = Link is down	0	Reg. 30, bit 5 Reg. 46, bit 5
1	Jabber Test	RO	Not Supported	0	—
0	Extended Capable	RO	0 = Not extended register capable	0	—
Register 2: PHYID High					
15-0	PHYID High	RO	High order PHYID bits	0x0022	—
Register 3: PHYID Low					
15-0	PHYID Low	RO	Low order PHYID bits	0x1430	—
Register 4: Auto-Negotiation Advertisement Ability					
15	Next Page	RO	Not Supported	0	—
14	Reserved	RO	—	0	—
13	Remote Fault	RO	Not Supported	0	—
12-11	Reserved	RO	—	00	—
10	Pause	R/W	1 = Advertise pause ability 0 = Do not advertise pause ability	1	Reg. 28, bit 4 Reg. 44, bit 4
9	Reserved	R/W	—	0	—
8	Adv 100 Full	R/W	1 = Advertise 100 full-duplex ability 0 = Do not advertise 100 full-duplex ability	1	Reg. 28, bit 3 Reg. 44, bit 3
7	Adv 100 Half	R/W	1 = Advertise 100 half-duplex ability 0 = Do not advertise 100 half-duplex ability	1	Reg. 28, bit 2 Reg. 44, bit 2
6	Adv 10 Full	R/W	1 = Advertise 10 full-duplex ability 0 = Do not advertise 10 full-duplex ability	1	Reg. 28, bit 1 Reg. 44, bit 1
5	Adv 10 Half	R/W	1 = Advertise 10 half-duplex ability 0 = Do not advertise 10 half-duplex ability	1	Reg. 28, bit 0 Reg. 44, bit 0
4-0	Selector Field	RO	802.3	00001	—

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Bit	Name	R/W	Description	Default	Reference
Register 5: Auto-Negotiation Link Partner Ability					
15	Next Page	RO	Not Supported	0	—
14	LP ACK	RO	Not Supported	0	—
13	Remote Fault	RO	Not Supported	0	—
12-11	Reserved	RO	—	00	—
10	Pause	RO	Link partner pause capability	0	Reg. 30, bit 4 Reg. 46, bit 4
9	Reserved	RO	—	0	—
8	Adv 100 Full	RO	Link partner 100 full-duplex capability	0	Reg. 30, bit 3 Reg. 46, bit 3
7	Adv 100 Half	RO	Link partner 100 half-duplex capability	0	Reg. 30, bit 2 Reg. 46, bit 2
6	Adv 10 Full	RO	Link partner 10 full-duplex capability	0	Reg. 30, bit 1 Reg. 46, bit 1
5	Adv 10 Half	RO	Link partner 10 half-duplex capability	0	Reg. 30, bit 0 Reg. 46, bit 0
4-0	Reserved	RO	—	00000	—

4.3 Register Map: Switch and PHY (8-bit registers)

TABLE 4-3: GLOBAL REGISTERS

Register (Decimal)	Register (Hex)	Description
0-1	0x00-0x01	Chip ID Register
2-11	0x02-0x0B	Global Control Register
12	0x0C	Reserved Register
13-15	0x0D-0x0F	User-Defined Registers

TABLE 4-4: PORT REGISTERS

Register (Decimal)	Register (Hex)	Description
16-29	0x10-0x1D	Port 1 Control Registers, including MII PHY Registers
30-31	0x1E-0x1F	Port 1 Status Registers, including MII PHY Registers
32-45	0x20-0x2D	Port 2 Control Registers, including MII PHY Registers
46-47	0x2E-0x2F	Port 2 Status Registers, including MII PHY Registers
48-61	0x30-0x3D	Port 3 Control Registers, including MII PHY Registers
62-63	0x3E-0x3F	Port 3 Status Registers, including MII PHY Registers
64-95	0x40-0x5F	Reserved

TABLE 4-5: ADVANCED CONTROL REGISTERS

Register (Decimal)	Register (Hex)	Description
96-103	0x60-0x67	TOS Priority Control Registers
104-109	0x68-0x6D	Switch Engine’s MAC Address Registers
110-111	0x6E-0x6F	Indirect Access Control Registers
112-120	0x70-0x78	Indirect Data Registers
121-122	0x79-0x7A	Digital Testing Status Registers
123-124	0x7B-0x7C	Digital Testing Control Registers
125-126	0x7D-0x7E	Analog Testing Control Registers

TABLE 4-5: ADVANCED CONTROL REGISTERS (CONTINUED)

Register (Decimal)	Register (Hex)	Description
127	0x7F	Analog Testing Status Register

4.4 Register Descriptions

TABLE 4-6: GLOBAL REGISTERS (0-15)

Bit	Name	R/W	Description	Default
Register 0 (0x00): Chip ID0				
7-0	Family ID	RO	Chip family	0x93
Register 1 (0x01): Chip ID1/Start Switch				
7-4	Chip ID	RO	0x0 is assigned to M series. (93M)	0x0
3-1	Revision ID	RO	Revision ID	—
0	Start Switch	R/W	1 = Start the chip when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1). **Note:** In (PS1, PS0) = (0, 0) mode, the chip will start automatically after trying to read the external EEPROM. If EEPROM does not exist, the chip will use pin strapping and default values for all internal registers. If EEPROM is present, the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x93, (2) Register 1 bits [7:4] = 0x0. If this check is OK, the contents in the EEPROM will override chip registers' default values. 0 = Chip will not start when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1).	1
Register 2 (0x02): Global Control 0				
7	New Back-Off Enable	R/W	New back-off algorithm designed for UNH 1 = Enable 0 = Disable	0
6-4	802.1p Base Priority	R/W	Used to classify priority for incoming 802.1Q packets. "User priority" is compared against this value. >= : Classified as high priority < : Classified as low priority	0x4
3	Pass Flow Control Packet	R/W	1 = Switch will not filter 802.1x flow control packets	0x0
2	Buffer Share Mode	R/W	1 = Buffer pool is shared by all ports. A port can use more buffers when other ports are not busy. 0 = A port is only allowed to use 1/3 of the buffer pool.	0x1
1	Reserved	R/W	Reserved	0
0	Link Change Age	R/W	1 = Link change from "link" to "no link" will cause fast aging (<800 µs) to age address table faster. After an age cycle is complete, the age logic will return to normal aging (about 200 sec). Note: If any port is unplugged, all addresses will be automatically aged out.	0
Register 3 (0x03): Global Control 1				
7	Pass All Frames	R/W	1 = Switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with sniffer mode only.	0

TABLE 4-6: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
6	Repeater Mode	R/W	1 = Repeater mode (half-duplex hub mode) 0 = Normal mode	0
5	IEEE 802.3x Transmit Direction Flow Control Enable	R/W	1 = Will enable transmit direction flow control feature. 0 = Will not enable transmit direction flow control feature.	1
4	IEEE 802.3x Receive Direction Flow Control Enable	R/W	1 = Will enable receive direction flow control feature. 0 = Will not enable receive direction flow control feature.	1
3	Frame Length Field Check	R/W	1 = Will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500). 0 = Will not check	0
2	Aging Enable	R/W	1 = Enable age function in the chip 0 = Disable age function in the chip	1
1	Fast Age Enable	R/W	1 = Turn on fast age (800 µs)	0
0	Aggressive Back-Off Enable	R/W	1 = Enable more aggressive back off algorithm in half-duplex mode to enhance performance. This is not an IEEE standard.	SMAC (Pin 69) value during reset.
Register 4 (0x04): Global Control 2				
7	Unicast Port-VLAN Mismatch Discard	R/W	This feature is used with port-VLAN (described in reg. 17, reg. 33, etc.) 1 = All packets cannot cross VLAN boundary 0 = Unicast packets (excluding unknown/multicast/broadcast) can cross VLAN boundary Note: Port mirroring is not supported if this bit is set to “0”.	1
6	Multicast Storm Protection Disable	R/W	1 = Broadcast Storm Protection does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets will be regulated. 0 = Broadcast Storm Protection includes DA = FF-FF-FF-FF-FF-FF and DA[40] = 1 packets.	1
5	Back Pressure Mode	R/W	1 = Carrier sense based back pressure is selected 0 = Collision based back pressure is selected	1
4	Flow Control and Back Pressure Fair Mode	R/W	1 = Fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. 0 = In this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be “fair” to the flow control port.	1
3	No Excessive Collision Drop	R/W	1 = The switch will not drop packets when 16 or more collisions occur. 0 = The switch will drop packets when 16 or more collisions occur.	SMAC (Pin 69) value during reset
2	Huge Packet Support	R/W	1 = Will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of this register. 0 = The max packet size will be determined by bit 1 of this register.	0

TABLE 4-6: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
1	Legal Maximum Packet Size Check Enable	R/W	0 = Will accept packet sizes up to 1536 bytes (inclusive). 1 = 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.	SMRXD0 (pin 85) value during reset
0	Priority Buffer Reserve	R/W	1 = Each port is pre-allocated 48 buffers used exclusively for high priority packets. It is recommended to enable this bit when the priority queue feature is turned on. 0 = No reserved buffers for high priority packets.	1
Register 5 (0x05): Global Control 3				
7	802.1Q VLAN Enable	R/W	1 = 802.1Q VLAN mode is turned on. VLAN table needs to set up before the operation. 0 = 802.1Q VLAN is disabled.	0
6	IGMP Snoop Enable on Switch MII Interface	R/W	1 = IGMP snoop is enabled. All IGMP packets will be forwarded to the Switch MII port. 0 = IGMP snoop is disabled.	0
5	Reserved	R/W	Reserved Do not change the default values.	0
4	Reserved	R/W	Reserved Do not change the default values.	0
3-2	Priority Scheme Select	R/W	00 = Always deliver high priority packets first 01 = Deliver high/low packets at ratio 10/1 10 = Deliver high/low packets at ratio 5/1 11 = Deliver high/low packets at ratio 2/1	00
1	Reserved	R/W	Reserved Do not change the default values.	0
0	Sniff Mode Select	R/W	1 = Will do RX AND TX sniff (both source port and destination port need to match) 0 = Will do RX OR TX sniff (either source port or destination port needs to match). This is the mode used to implement RX-only sniff.	0
Register 6 (0x06): Global Control 4				
7	Reserved	R/W	Reserved Do not change the default values.	0
6	Switch MII Half-Duplex Mode	R/W	1 = Enable MII interface half-duplex mode. 0 = Enable MII interface full-duplex mode.	Pin SMRXD2 strap option. Pull-down(0): Full-duplex mode Pull-up(1): Half-duplex mode Note: SMRXD2 has internal pull-down.

TABLE 4-6: GLOBAL REGISTERS (0-15) (CONTINUED)

Bit	Name	R/W	Description	Default
5	Switch MII Flow Control Enable	R/W	1 = Enable full-duplex flow control on Switch MII interface. 0 = Disable full-duplex flow control on Switch MII interface.	Pin SMRXD3 strap option. Pull-down(0): Disable flow control Pull-up(1): Enable flow control Note: SMRXD3 has internal pull-down.
4	Switch MII 10BT	R/W	1 = The switch interface is in 10 Mbps mode 0 = The switch interface is in 100 Mbps mode	Pin SMRXD1 strap option. Pull-down(0): Enable 100 Mbps Pull-up(1): Enable 10 Mbps Note: SMRXD1 has internal pull-down.
3	Null VID Replacement	R/W	1 = Will replace NULL VID with port VID (12 bits) 0 = No replacement for NULL VID	0
2-0	Broadcast Storm Protection Rate Bit [10:8]	R/W	This register along with the next register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 50 ms for 100BT or 500 ms for 10BT. The default is 1%.	000
Register 7 (0x07): Global Control 5				
7-0	Broadcast Storm Protection Rate Bit [7:0]	R/W	This register along with the previous register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 500 ms for 10BT. The default is 1%. Note: 100BT Rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx.) = 0x63	0x63
Register 8 (0x08): Global Control 6				
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x4E
Register 9 (0x09): Global Control 7				
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x24
Register 10 (0x0A): Global Control 8				
7-0	Factory Testing	R/W	Reserved Do not change the default values.	0x24
Register 11 (0x0B): Global Control 9				
7	Reserved	—	Reserved Do not change the default values.	0
6	PHY Power Save	R/W	1 = Enable PHY power save mode 0 = Disable PHY power save mode	0
5	Reserved	R/W	Reserved Do not change the default values.	0

TABLE 4-6: GLOBAL REGISTERS (0-15) (CONTINUED)

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td>4</td><td>Reserved</td><td>R/W</td><td>Testing mode.
Set to ‘0’ for normal operation.</td><td>0</td></tr>
<tr><td>3</td><td>Reserved</td><td>R/W</td><td>Reserved
Do not change the default values.</td><td>1</td></tr>
<tr><td>2</td><td>Reserved</td><td>R/W</td><td>Reserved
Do not change the default values.</td><td>0</td></tr>
<tr><td>1</td><td>LED Mode</td><td>R/W</td><td>This register bit sets the LEDSEL0 selection only.
LEDSEL1 is set via strap-in pin.
Port x LED indicators, defined below:
<table>
<tr><th></th><th>[LEDSEL1, LEDSEL0]</th><th></th></tr>
<tr><th></th><th>[0, 0]</th><th>[0, 1]</th></tr>
<tr><td>PxLED3</td><td>—</td><td>—</td></tr>
<tr><td>PxLED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>PxLED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>PxLED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><th></th><th>[LEDSEL1, LEDSEL0]</th><th></th></tr>
<tr><th></th><th>[1, 0]</th><th>[1, 1]</th></tr>
<tr><td>PxLED3</td><td>Activity</td><td>—</td></tr>
<tr><td>PxLED2</td><td>Link</td><td>—</td></tr>
<tr><td>PxLED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>PxLED0</td><td>Speed</td><td>—</td></tr>
</table>
Note: LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.</td><td>LEDSEL0 pin value during reset</td></tr>
<tr><td>0</td><td>Special TPID Mode</td><td>R/W</td><td>Used for direct mode forwarding from port 3. See description in spanning tree functional description.
0 = Disable
1 = Enable</td><td>0</td></tr>
<tr><td colspan="5">Register 12 (0x0C): Reserved Register</td></tr>
<tr><td>7-0</td><td>Reserved</td><td>—</td><td>Reserved
Do not change the default values.</td><td>0x00</td></tr>
<tr><td colspan="5">Register 13 (0x0D): User-Defined Register 1</td></tr>
<tr><td>7-0</td><td>UDR1</td><td>R/W</td><td>—</td><td>0x00</td></tr>
<tr><td colspan="5">Register 14 (0x0E): User-Defined Register 2</td></tr>
<tr><td>7-0</td><td>UDR2</td><td>R/W</td><td>—</td><td>0x00</td></tr>
<tr><td colspan="5">Register 15 (0x0F): User-Defined Register 3</td></tr>
<tr><td>7-0</td><td>UDR3</td><td>R/W</td><td>—</td><td>0x00</td></tr>
</table>

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

TABLE 4-7: PORT REGISTERS (REGISTERS 16 - 95)

Bit	Name	R/W	Description	Default
Register 16 (0x10): Port 1 Control 0 Register 32 (0x20): Port 2 Control 0 Register 48 (0x30): Port 3 Control 0				
7	Broadcast Storm Protection Enable	R/W	1 = Enable broadcast storm protection for ingress packets on the port 0 = Disable broadcast storm protection	0
6	DiffServ Priority Classification Enable	R/W	1 = Enable DiffServ priority classification for ingress packets on the port 0 = Disable DiffServ function	0
5	802.1p Priority Classification Enable	R/W	1 = Enable 802.1p priority classification for ingress packets on the port 0 = Disable 802.1p	Pin value during reset: P1_1PEN (port 1) P2_1PEN (port 2) P3_1PEN (port 3)
4	Port-based Priority Classification Enable	R/W	1 = Ingress packets on the port will be classified as high priority if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 0 = Ingress packets on port will be classified as low priority if “DiffServ” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.	Pin value during reset: P1_PP (port 1) P2_PP (port 2) P3_PP (port 3)
3	User Priority Ceiling	R/W	1 = If the packet’s “user priority field” is greater than the “user priority field” in the port default tag register, replace the packet’s “user priority field” with the “user priority field” in the port default tag register. 0 = Do not compare and replace the packet’s ‘user priority field”	0
2	Tag Insertion	R/W	1 = When packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion	Pin value during reset: P1_TAGINS (port 1) P2_TAGINS (port 2) P3_TAGINS (port 3)
1	Tag Removal	R/W	1 = When packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal	Pin value during reset: P1_TAGRM (port 1) P2_TAGRM (port 2) P3_TAGRM (port 3)
0	Priority Enable	R/W	1 = The port output queue is split into high and low priority queues. 0 = Single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.	Pin value during reset: P1_TXQ2 (port 1) P2_TXQ2 (port 2) P3_TXQ2 (port 3)

TABLE 4-7: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 17 (0x11): Port 1 Control 1 Register 33 (0x21): Port 2 Control 1 Register 49 (0x31): Port 3 Control 1				
7	Sniffer Port	R/W	1 = Port is designated as sniffer port and will transmit packets that are monitored. 0 = Port is a normal port	0
6	Receive Sniff	R/W	1 = All packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = No receive monitoring	0
5	Transmit Sniff	R/W	1 = All packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = No transmit monitoring	0
4	Double Tag	R/W	1 = All packets will be tagged with port default tag of ingress port regardless of the original packets are tagged or not 0 = Do not double tagged on all packets	0x0
3	Reserved	R/W	Reserved Do not change the default values.	0x0
2-0	Port VLAN Membership	R/W	Define the port’s egress port VLAN membership. Bit 2 stands for port 3, bit 1 for port 2 bit 0 for port 1. The Port can only communicate within the membership. A ‘1’ includes a port in the membership. A ‘0’ excludes a port from membership.	Pin value during reset: For port 1, (PV13, PV12, 1) For port 2, (PV23, 1, PV21) For port 3, (1, PV32, PV31)
Register 18 (0x12): Port 1 Control 2 Register 34 (0x22): Port 2 Control 2 Register 50 (0x32): Port 3 Control 2				
7	Reserved	—	Reserved Do not change the default values.	0
6	Ingress VLAN Filtering	R/W	1 = The switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port. 0 = No ingress VLAN filtering.	0
5	Discard non-PVID Packets	R/W	1 = The switch will discard packets whose VID does not match ingress port default VID. 0 = No packets will be discarded	0
4	Force Flow Control	R/W	1 = Will always enable flow control on the port, regardless of AN result. 0 = Flow control is enabled based on AN result.	Pin value during reset: For port 1, P1FFC pin For port 2, P2FFC pin For port 3, this bit has no meaning. Flow control is set by Reg. 6, bit 5.
3	Back Pressure Enable	R/W	1 = Enable port’s half-duplex back pressure 0 = Disable port’s half-duplex back pressure	Pin value during reset: BPEN pin

TABLE 4-7: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
2	Transmit Enable	R/W	1 = Enable packet transmission on the port 0 = Disable packet transmission on the port Note: This bit is used for spanning tree support.	1
1	Receive Enable	R/W	1 = Enable packet reception on the port 0 = Disable packet reception on the port Note: This bit is used for spanning tree support.	1
0	Learning Disable	R/W	1 = Disable switch address learning capability 0 = Enable switch address learning Note: This bit is used for spanning tree support.	0
Register 19 (0x13): Port 1 Control 3 **Register 35 (0x23): Port 2 Control 3** **Register 51 (0x33): Port 3 Control 3**				
7-0	Default Tag [15:8]	R/W	Port's default tag, containing 7-5 = User priority bits 4 = CFI bit 3-0 = VID[11:8]	0x00
Register 20 (0x14): Port 1 Control 4 **Register 36 (0x24): Port 2 Control 4** **Register 52 (0x34): Port 3 Control 4**				
7-0	Default Tag [7:0]	R/W	Port's default tag, containing 7-0: VID[7:0]	0x01
Note: Registers 19 and 20 (and those corresponding to other ports) serve two purposes: Associated with the ingress untagged packets, and used for egress tagging. Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.				
Register 21 (0x15): Port 1 Control 5 **Register 37 (0x25): Port 2 Control 5** **Register 53 (0x35): Port 3 Control 5**				
7-0	Transmit High Priority Rate Control [7:0]	R/W	This register along with port control 7, bits [3:0] form a 12-bits field to determine how many "32 Kbps" high priority blocks can be transmitted in a unit of 4 Kbytes in a one second period).	0x00
Register 22 (0x16): Port 1 Control 6 **Register 38 (0x26): Port 2 Control 6** **Register 54 (0x36): Port 3 Control 6**				
7-0	Transmit Low Priority Rate Control [7:0]	R/W	This register along with port control 7, bits [7:4] form a 12-bits field to determine how many "32 Kbps" low priority blocks can be transmitted in a unit of 4 Kbytes in a one second period).	0x00
Register 23 [6:0] (0x17): Port 1 Control 7 **Register 39 [6:0] (0x27): Port 2 Control 7** **Register 55 [6:0] (0x37): Port 3 Control 7**				
7-4	Transmit Low Priority Rate Control [11:8]	R/W	These bits along with port control 6, bits [7:0] form a 12-bits field to determine how many "32 Kbps" low priority blocks can be transmitted in a unit of 4 Kbytes in a one second period).	0x0
3-0	Transmit High Priority Rate Control [11:8]	R/W	These bits along with port control 5, bits [7:0] form a 12-bits field to determine how many "32 Kbps" high priority blocks can be transmitted (in a unit of 4 Kbytes in a one second period).	0x0

TABLE 4-7: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
Register 24 [6:0] (0x18): Port 1 Control 8 Register 40 [6:0] (0x28): Port 2 Control 8 Register 56 [6:0] (0x38): Port 3 Control 8				
7-0	Receive High Priority Rate Control [7:0]	R/W	This register along with port control 10, bits [3:0] form a 12-bits field to determine how many “32 Kbps” high priority blocks can be received in a unit of 4 Kbytes in a one second period).	0x00
Register 25 [6:0] (0x19): Port 1 Control 9 Register 41 [6:0] (0x29): Port 2 Control 9 Register 57 [6:0] (0x39): Port 3 Control 9				
7-0	Receive Low Priority Rate Control [7:0]	R/W	This register along with port control 10, bits [7:4] form a 12-bits field to determine how many “32 Kbps” low priority blocks can be received (in a unit of 4 Kbytes in a one second period).	0x00
Register 26 (0x1A): Port 1 Control 10 Register 42 (0x2A): Port 2 Control 10 Register 58 (0x3A): Port 3 Control 10				
7-4	Receive Low Priority Rate Control [11:8]	R/W	These bits along with port control 9, bits [7:0] form a 12-bits field to determine how many “32 Kbps” low priority blocks can be received (in a unit of 4 Kbytes in a one second period).	0x0
3-0	Receive High Priority Rate Control [11:8]	R/W	These bits along with port control 8, bits [7:0] form a 12-bits field to determine how many “32 Kbps” high priority blocks can be received (in a unit of 4 Kbytes in a one second period).	0x0
Register 27 (0x1B): Port 1 Control 11 Register 43 (0x2B): Port 2 Control 11 Register 59 (0x3B): Port 3 Control 11				
7	Receive Differential Priority Rate Control	R/W	1 = If bit 6 is also ‘1’ this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also ‘1’, this will enable receive rate control on high priority packets at the high priority rate. 0 = Receive rate control will be based on the low priority rate for all packets on this port.	0
6	Low Priority Receive Rate Control Enable	R/W	1 = Enable port’s low priority receive rate control feature 0 = Disable port’s low priority receive rate control	0
5	High Priority Receive Rate Control Enable	R/W	1 = If bit 7 is also ‘1’ this will enable the port’s high priority receive rate control feature. If bit 7 is a ‘0’ and bit 6 is a ‘1’, all receive packets on this port will be rate controlled at the low priority rate. 0 = Disable port’s high priority receive rate control feature	0
4	Low Priority Receive Rate Flow Control Enable	R/W	1 = Flow control may be asserted if the port’s low priority receive rate is exceeded. 0 = Flow control is not asserted if the port’s low priority receive rate is exceeded.	0
3	High Priority Receive Rate Flow Control Enable	R/W	1 = Flow control may be asserted if the port’s high priority receive rate is exceeded. (To use this, differential receive rate control must be on.) 0 = Flow control is not asserted if the port’s high priority receive rate is exceeded.	0

TABLE 4-7: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
2	Transmit Differential Priority Rate Control	R/W	1 = Will do transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets respectively. 0 = Will do transmit rate control on any packets. The rate counters defined in low priority will be used.	0
1	Low Priority Transmit Rate Control Enable	R/W	1 = Enable the port's low priority transmit rate control feature 0 = Disable the port's low priority transmit rate control feature	0
0	High Priority Transmit Rate Control Enable	R/W	1 = Enable the port's high priority transmit rate control feature 0 = Disable the port's high priority transmit rate control feature	0
Note:	Port Control 12 and 13, and Port Status 0 contents can also be accessed with the MIIM (MDC/MDIO) interface via the Standard MIIM registers.			
Register 28 (0x1C): Port 1 Control 12 **Register 44 (0x2C): Port 2 Control 12** **Register 60 (0x3C): Reserved, Not Applicable to Port 3**				
7	Auto Negotiation Enable	R/W	1 = Auto negotiation is on 0 = Disable auto negotiation; speed and duplex are determined by bits 6 and 5 of this register.	For port 1, P1ANEN pin value during reset. For port 2, P2ANEN pin value during reset
6	Force Speed	R/W	1 = Forced 100BT if AN is disabled (bit 7) 0 = Forced 10BT if AN is disabled (bit 7)	For port 1, P1SPD pin value during reset. For port 2, P2SPD pin value during reset.
5	Force Duplex	R/W	1 = Forced full-duplex if (1) AN is disabled or (2) AN is enabled but failed. 0 = Forced half-duplex if (1) AN is disabled or (2) AN is enabled but failed.	For port 1, P1DPX pin value during reset. For port 2, P2DPX pin value during reset.
4	Advertise Flow Control Capability	R/W	1 = Advertise flow control (pause) capability 0 = Suppress flow control (pause) capability from transmission to link partner	ADVFC pin value during reset.
3	Advertise 100BT Full-Duplex Capability	R/W	1 = Advertise 100BT full-duplex capability 0 = Suppress 100BT full-duplex capability from transmission to link partner	1
2	Advertise 100BT Half-Duplex Capability	R/W	1 = Advertise 100BT half-duplex capability 0 = Suppress 100BT half-duplex capability from transmission to link partner	1

TABLE 4-7: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
1	Advertise 10BT Full-Duplex Capability	R/W	1 = Advertise 10BT full-duplex capability 0 = Suppress 10BT full-duplex capability from transmission to link partner	1
0	Advertise 10BT Half-Duplex Capability	R/W	1 = Advertise 10BT half-duplex capability 0 = Suppress 10BT half-duplex capability from transmission to link partner	1
Register 29 (0x1D): Port 1 Control 13 Register 45 (0x2D): Port 2 Control 13 Register 61 (0x3D): Reserved, Not Applicable to Port 3				
7	LED Off	R/W	1 = Turn off all port's LEDs (LEDx_3, LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one. 0 = Normal operation	0
6	Txdis	R/W	1 = Disable the port's transmitter 0 = Normal operation	0
5	Restart AN	R/W	1 = Restart auto-negotiation 0 = Normal operation	0
4	Disable Far-End Fault	R/W	1 = Disable far-end fault detection and pattern transmission. 0 = Enable far-end fault detection and pattern transmission	0 Note: Only port 1 supports fiber. This bit is applicable to port 1 only.
3	Power Down	R/W	1 = Power down 0 = Normal operation	0
2	Disable Auto MDI/MDI-X	R/W	1 = Disable auto MDI/MDI-X function 0 = Enable auto MDI/MDI-X function	0 For port 2, P2MDIX disable pin value during reset.
1	Force MDI-X	R/W	If auto MDI/MDI-X is disabled, 1 = Force PHY into MDI mode (transmit on RXP/RXM pins) 0 = Force PHY into MDI-X mode (transmit on TXP/TXM pins)	0 For port 2, P2MDIX pin value during reset.
0	Loopback	R/W	1 = Perform loopback, as indicated: Port 1 Loopback (reg. 29, bit 0 = '1') Start: RXP2/RXM2 (port 2) Loopback: PMD/PMA of port 1's PHY End: TXP2/TXM2 (port 2) Port 2 Loopback (reg. 45, bit 0 = '1') Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 2's PHY End: TXP1/TXM1 (port 1) 0 = Normal operation	0
Register 30 (0x1E): Port 1 Status 0 Register 46 (0x2E): Port 2 Status 0 Register 62 (0x3E): Reserved, Not Applicable to Port 3				
7	MDI-X Status	RO	1 = MDI-X 0 = MDI	0
6	AN Done	RO	1 = Auto-negotiation completed 0 = Auto-negotiation not completed	0

TABLE 4-7: PORT REGISTERS (REGISTERS 16 - 95) (CONTINUED)

Bit	Name	R/W	Description	Default
5	Link Good	RO	1 = Link good 0 = Link not good	—
4	Partner Flow Control Capability	RO	1 = Link partner flow control (pause) capable 0 = Link partner not flow control (pause) capable	—
3	Partner 100BT Full-Duplex Capability	RO	1 = Link partner 100BT full-duplex capable 0 = Link partner not 100BT full-duplex capable	0
2	Partner 100BT Half-Duplex Capability	RO	1 = Link partner 100BT half-duplex capable 0 = Link partner not 100BT half-duplex capable	0
1	Partner 10BT Full-Duplex Capability	RO	1 = Link partner 10BT full-duplex capable 0 = Link partner not 10BT full-duplex capable	0
0	Partner 10BT Half-Duplex Capability	RO	1 = Link partner 10BT half-duplex capable 0 = Link partner not 10BT half-duplex capable	0
Register 31 (0x1F): Port 1 Status 1 Register 47 (0x2F): Port 2 Status 1 Register 63 (0x3F): Port 3 Status 1				
7	Reserved	RO	Reserved Do not change the default value.	0
6-5	Reserved	RO	Reserved Do not change the default value.	0
4	Receive Flow Control Enable	RO	1 = Receive flow control feature is active 0 = Receive flow control feature is inactive	0
3	Transmit Flow Control Enable	RO	1 = Transmit flow control feature is active 0 = Transmit flow control feature is inactive	0
2	Operation Speed	RO	1 = Link speed is 100 Mbps 0 = Link speed is 10 Mbps	0
1	Operation Duplex	RO	1 = Link duplex is full 0 = Link duplex is half	0
0	Far-End Fault	RO	1 = Far-end fault status detected 0 = No far-end fault status detected	0 Note: Only port 1 supports fiber. This bit is applicable to port 1 only.

4.5 Advanced Control Registers (Registers 96-127)

The IPv4 Type of Service (TOS) Priority Control Registers implement a fully decoded, 64-bit Differentiated Services Code Point (DSCP) register set that is used to determine priority from the 6-bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bits in the DSCP register to determine the priority. If the register bit is a 1, the priority is high; if it is a 0, the priority is low.

TABLE 4-8: ADVANCED CONTROL REGISTERS (REGISTERS 96-127)

Bit	Name	R/W	Description	Default
Register 96 (0x60): TOS Priority Control Register 0				
7-0	DSCP[63:56]	R/W	—	0000_0000
Register 97 (0x61): TOS Priority Control Register 1				
7-0	DSCP[55:48]	R/W	—	0000_0000
Register 98 (0x62): TOS Priority Control Register 2				
7-0	DSCP[47:40]	R/W	—	0000_0000
Register 99 (0x63): TOS Priority Control Register 3				
7-0	DSCP[39:32]	R/W	—	0000_0000
Register 100 (0x64): TOS Priority Control Register 4				
7-0	DSCP[31:24]	R/W	—	0000_0000
Register 101 (0x65): TOS Priority Control Register 5				
7-0	DSCP[23:16]	R/W	—	0000_0000
Register 102 (0x66): TOS Priority Control Register 6				
7-0	DSCP[15:8]	R/W	—	0000_0000
Register 103 (0x67): TOS Priority Control Register 7				
7-0	DSCP[7:0]	R/W	—	0000_0000
Registers 104 to 109 define the switching engine's MAC address. This 48-bit address is used as the SA for MAC pause control frames.				
Register 104 (0x68): MAC Address Register 0				
7-0	MACA[47:40]	R/W	—	0x00
Register 105 (0x69): MAC Address Register 1				
7-0	MACA[39:32]	R/W	—	0x00
Register 106 (0x6A): MAC Address Register 2				
7-0	MACA[31:24]	R/W	—	0x00
Register 107 (0x6B): MAC Address Register 3				
7-0	MACA[23:16]	R/W	—	0x00
Register 108 (0x6C): MAC Address Register 4				
7-0	MACA[15:8]	R/W	—	0x00
Register 109 (0x6D): MAC Address Register 5				
7-0	MACA[7:0]	R/W	—	0x00
Use registers 110 and 111 to read or write data to the static MAC address table, VLAN table, dynamic address table, or the MIB counters.				
Register 110 (0x6E): Indirect Access Control 0				
7-5	Reserved	R/W	Reserved	000
4	Read High Write Low	R/W	1 = Read cycle 0 = Write cycle	0
3-2	Table Select	R/W	00 = Static MAC address table selected 01 = VLAN table selected 10 = Dynamic address table selected 11 = MIB counter selected	00

TABLE 4-8: ADVANCED CONTROL REGISTERS (REGISTERS 96-127) (CONTINUED)

Bit	Name	R/W	Description	Default
1-0	Indirect High Address	R/W	Bit 9-8 of indirect address	00
Register 111 (0x6F): Indirect Access Control 1				
7-0	Indirect Address Low	R/W	Bit 7-0 of indirect address Note: Write to register 111 will actually trigger a command. Read or write access is determined by Register 110 bit 4.	0000_0000
Register 112 (0x70): Indirect Data Register 8				
68-64	Indirect Data	R/W	Bit 68-64 of indirect data	0_0000
Register 113 (0x71): Indirect Data Register 7				
63-56	Indirect Data	R/W	Bit 63-56 of indirect data	0000_0000
Register 114 (0x72): Indirect Data Register 6				
55-48	Indirect Data	R/W	Bit 55-48 of indirect data	0000_0000
Register 115 (0x73): Indirect Data Register 5				
47-40	Indirect Data	R/W	Bit 47-40 of indirect data	0000_0000
Register 116 (0x74): Indirect Data Register 4				
39-32	Indirect Data	R/W	Bit 39-32 of indirect data	0000_0000
Register 117 (0x75): Indirect Data Register 3				
31-24	Indirect Data	R/W	Bit 31-24 of indirect data	0000_0000
Register 118 (0x76): Indirect Data Register 2				
23-16	Indirect Data	R/W	Bit 23-16 of indirect data	0000_0000
Register 119 (0x77): Indirect Data Register 1				
15-8	Indirect Data	R/W	Bit 15-8 of indirect data	0000_0000
Register 120 (0x78): Indirect Data Register 0				
7-0	Indirect Data	R/W	Bit 7-0 of indirect data	0000_0000
Registers 121 to 127 are Reserved.				

4.6 Static MAC Address Table

The KSZ8993M has both a static and a dynamic MAC address table. When a destination address (DA) lookup is requested, both tables are searched to make a packet forwarding decision. When a SA lookup is requested, only the dynamic table is searched for aging, migration and learning purposes. The static DA lookup result will have precedence over the dynamic DA lookup result. If there is a DA match in both tables, the result from the static table will be used. The static table can be accessed and controlled by an external processor via the SMI, SPI, and I^2C interfaces. The external processor performs all addition, modification and deletion of static table entries. These entries in the static table will not be aged out by the KSZ8993M.

TABLE 4-9: FORMAT OF STATIC MAC TABLE (8 ENTRIES)

Bit	Name	R/W	Description	Default
57-54	FID	R/W	Filter VLAN ID – identifies one of the 16 active VLANs	0000
53	Use FID	R/W	1 = Use (FID+MAC) for static table look ups 0 = Use MAC only for static table look ups	0
52	Override	R/W	1 = Override port setting “transmit enable=0” or “receive enable=0” setting 0 = No override	0
51	Valid	R/W	1 = This entry is valid, the lookup result will be used 0 = This entry is not valid	0

TABLE 4-9: FORMAT OF STATIC MAC TABLE (8 ENTRIES) (CONTINUED)

Bit	Name	R/W	Description	Default
50-48	Forwarding Ports	R/W	These 3 bits control the forwarding port(s): 001 = Forward to port 1 010 = Forward to port 2 100 = Forward to port 3 011 = Forward to port 1 and port 2 110 = Forward to port 2 and port 3 101 = Forward to port 1 and port 3 111 = Broadcasting (excluding the ingress port)	000
47-0	MAC Address	R/W	48-bit MAC Address	0x0000_0000_0000

Examples:

1. Static Address Table Read (Read the 2nd Entry)

Write to reg. 110 with 0x10 // Read static table selected

Write to reg. 111 with 0x01 // Trigger the read operation

Then,

Read reg. 113, static table bits [57:56]

Read reg. 114, static table bits [55:48]

Read reg. 115, static table bits [47:40]

Read reg. 116, static table bits [39:32]

Read reg. 117, static table bits [31:24]

Read reg. 118, static table bits [23:16]

Read reg. 119, static table bits [15:8]

Read reg. 120, static table bits [7:0]

2. Static Address Table Write (Write the 8th Entry)

Write to reg. 113, static table bits [57:56]

Write to reg. 114, static table bits [55:48]

Write to reg. 115, static table bits [47:40]

Write to reg. 116, static table bits [39:32]

Write to reg. 117, static table bits [31:24]

Write to reg. 118, static table bits [23:16]

Write to reg. 119, static table bits [15:8]

Write to reg. 120, static table bits [7:0]

Write to reg. 110 with 0x00 // Write static table selected

Write to reg. 111 with 0x07 // Trigger the write operation

4.7 VLAN Table

If 802.1Q VLAN mode is enabled (Register 5, Bit 7 = ‘1’), the VLAN table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (filter ID), VID (VLAN ID), and VLAN membership as described in the following table.

TABLE 4-10: FORMAT OF STATIC VLAN TABLE (16 ENTRIES)

Bit	Name	R/W	Description	Default
19	Valid	R/W	1 = Entry is valid 0 = Entry is invalid	1

TABLE 4-10: FORMAT OF STATIC VLAN TABLE (16 ENTRIES) (CONTINUED)

Bit	Name	R/W	Description	Default
18-16	Membership	R/W	Specify which ports are members of the VLAN. If a DA lookup fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example, 101 means port 3 and 1 are in this VLAN.	111
15-12	FID	R/W	Filter ID. KSZ8993M supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.	0x0
11-0	VID	R/W	IEEE 802.1Q 12 bits VLAN ID	0x001

If 802.1Q VLAN mode is enabled, KSZ8993M will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non null VID, the VID in the tag will be used. The lookup process will start from the VLAN table lookup. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA lookup determines the forwarding ports. If FID+DA fails, the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

Examples:

1. VLAN Table Read (read the 3rd entry)

Write to reg. 110 with 0x14 // Read VLAN table selected

Write to reg. 111 with 0x02 // Trigger the read operation

Then,

Read reg. 118, VLAN table bits [19:16]

Read reg. 119, VLAN table bits [15:8]

Read reg. 120, VLAN table bits [7:0]

2. VLAN Table Write (write the 7th entry)

Write to reg. 118, VLAN table bits [19:16]

Write to reg. 119, VLAN table bits [15:8]

Write to reg. 120, VLAN table bits [7:0]

Write to reg. 110 with 0x04 // Write VLAN table selected

Write to reg. 111 with 0x06 // Trigger the write operation

4.8 Dynamic MAC Address Table

The KSZ8993M maintains the dynamic MAC address table. Only read access is allowed.

TABLE 4-11: FORMAT OF DYNAMIC MAC ADDRESS TABLE (1K ENTRIES)

Bit	Name	R/W	Description	Default
71	Data Not Ready	RO	1 = Entry is not ready, continue retrying until this bit is set to 0 0 = Entry is ready	—
70-67	Reserved	RO	Reserved	—
66	MAC Empty	RO	1 = There is no valid entry in the table 0 = There are valid entries in the table	1
65-56	Number of Valid Entries	RO	Indicates how many valid entries in the table 0x3FF means 1k entries 0x001 means 2 entries 0x000 and bit 66 = 0 means 1 entry 0x000 and bit 66 = 1 means 0 entry	00_0000_0000

TABLE 4-11: FORMAT OF DYNAMIC MAC ADDRESS TABLE (1K ENTRIES) (CONTINUED)

Bit	Name	R/W	Description	Default
55-54	Time Stamp	RO	2 bits counter for internal aging	—
53-52	Source Port	RO	The source port where FID+MAC is learned 00 = Port 1 01 = Port 2 10 = Port 3	00
51-48	FID	RO	Filter ID	0x0
47-0	MAC Address	RO	48-bit MAC Address	0x0000_0000_0000

Example:

Dynamic MAC Address Table Read (read the 1st entry and retrieve the MAC table size)

Write to reg. 110 with 0x18 // Read dynamic table selected

Write to reg. 111 with 0x00 // Trigger the read operation

Then,

Read reg. 112, dynamic table bits [71:64] // if bit 71 = 1, restart (reread) from this register

Read reg. 113, dynamic table bits [63:56]

Read reg. 114, dynamic table bits [55:48]

Read reg. 115, dynamic table bits [47:40]

Read reg. 116, dynamic table bits [39:32]

Read reg. 117, dynamic table bits [31:24]

Read reg. 118, dynamic table bits [23:16]

Read reg. 119, dynamic table bits [15:8]

Read reg. 120, dynamic table bits [7:0]

4.9 Management Information Base (MIB) Counters

The KSZ8993M provides 34 MIB counters per port. These counters are used to monitor the port activity for network management. The MIB counters have two format groups: “Per Port” and “All Port Dropped Packet.”

TABLE 4-12: FORMAT OF “PER PORT” MIB COUNTERS

Bit	Name	R/W	Description	Default
31	Reserved	RO	Reserved	0
30	Count Valid	RO	1 = Counter value is valid 0 = Counter value is not valid	0
29-0	Counter Values	RO	Counter value	0

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for all three ports are:

- Port 1, base is 0x00 and range is (0x00-0x1F)
- Port 2, base is 0x20 and range is (0x20-0x3F)
- Port 3, base is 0x40 and range is (0x40-0x5F)

Port 1 MIB counters are read using the indirect memory offsets in Table 4-13.

TABLE 4-13: PORT 1’S “PER PORT” MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC

TABLE 4-13: PORT 1'S "PER PORT" MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 or 1522 bytes)
0x5	RxJabbers	Rx packets longer than 1522 bytes w/ either CRC errors, alignment errors, or symbol errors (depends on max packet size setting)
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on max packet size setting)
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting)
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in Ether-Type field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting)
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multi-cast packets)
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

TABLE 4-14: FORMAT OF "ALL PORT DROPPED PACKET" MIB COUNTERS

Bit	Name	R/W	Description	Default
30-16	Reserved	N/A	Reserved	N/A
15-0	Counter Value	RO	Counter Value	0

"All Port Dropped Packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 4-15.

TABLE 4-15: "ALL PORT DROPPED PACKET" MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x100	Port 1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port 2 TX Drop Packets	TX packets dropped due to lack of resources
0x102	Port 3 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port 1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port 2 RX Drop Packets	RX packets dropped due to lack of resources
0x105	Port 3 RX Drop Packets	RX packets dropped due to lack of resources

Examples:

1. MIB Counter Read (Read port 1 "Rx64Octets" Counter)

Write to reg. 110 with 0x1c // Read MIB counters selected

Write to reg. 111 with 0x0e // Trigger the read operation

Then

Read reg. 117, counter bits [30:24] // If bit 30 = 0, restart (reread) from this register

Read reg. 118, counter bits [23:16]

Read reg. 119, counter bits [15:8]

Read reg. 120, counter bits [7:0]

2. MIB Counter Read (Read port 2 "Rx64Octets" Counter)

Write to reg. 110 with 0x1c // Read MIB counter selected

Write to reg. 111 with 0x2e // Trigger the read operation

Then,

Read reg. 117, counter bits [30:24] // If bit 30 = 0, restart (reread) from this register

Read reg. 118, counter bits [23:16]

Read reg. 119, counter bits [15:8]

Read reg. 120, counter bits [7:0]

3. MIB Counter Read (Read "Port 1 TX Drop Packets" Counter)

Write to reg. 110 with 0x1D // Read MIB counter selected

Write to reg. 111 with 0x00 // Trigger the read operation

Then

Read reg. 119, counter bits [15:8]

Read reg. 120, counter bits [7:0]

4.9.1 ADDITIONAL MIB COUNTER INFORMATION

"Per Port" MIB counters are designed as "read clear." These counters will be cleared after they are read.

"All Port Dropped Packet" MIB counters are not cleared after they are accessed and do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

To read out all the counters, the best performance over the SPI bus is (160+3) x 8 x 200 = 260 ms, where there are 160 registers, 3 overheads, 8 clocks per access, at 5 MHz. In the heaviest condition, the counters will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds.

A high performance SPI master is also recommended to prevent counters overflow.

Per Port MIB counters are designed as “read clear.” That is, these counters will be cleared after they are read.

“All Port Dropped Packet” MIB counters are not cleared after they are read.

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage
(V_{DDA}, V_{DDAP}, V_{DDC}) ..... –0.5V to +2.4V

(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... –0.5V to +4.0V

Input Voltage (all inputs) ..... –0.5V to +4.0V

Output Voltage (all outputs) ..... –0.5V to +4.0V

Lead Temperature (soldering, 10s) ..... +260°C

Storage Temperature (T_S) ..... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

5.2 Operating Ratings**

Supply Voltage
(V_{DDA}, V_{DDAP}, V_{DDC}) ..... +1.710V to +1.890V

(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... +3.135V to +3.465V

Ambient Operating Temperature for M, ML Options (T_A) ..... 0°C to +70°C

Ambient Operating Temperature for MI, MLI Options (T_A) ..... –40°C to +85°C

Maximum Junction Temperature (T_J) ..... +125°C

Thermal Resistance (Note 5-1) (Θ_{JA}) ..... +32°C/W

**The device is not guaranteed to function outside its operating ratings.

Note 5-1 No heat spreader (HS) in this package.

Note:	Do not drive input signals without power supplied to the device.

6.0 ELECTRICAL CHARACTERISTICS

T_A = 25°C. Specification is for packaged product only. Current consumption is for the single 3.3V supply KSZ8893FQL device only, and includes the 1.2V supply voltages (V_{DDA}, V_{DDAP}, V_{DDC}) that are provided by the KSZ8893FQL via power output pin 22. Each PHY port's transformer consumes an additional 45 mA @ 3.3V for 100BASE-TX and 70 mA @ 3.3V for 10BASE-T.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
100BASE-TX Operation (All Ports @ 100% Utilization)						
100BASE-TX (analog core + PLL + digital core)	I_{DDC}	—	92	—	mA	V_{DDA}, V_{DDAP}, V_{DDC} = 1.8V
100BASE-TX (Transceiver + Digital I/O)	I_{DDXIO}	—	33	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
10BASE-T Operation (All Ports @ 100% Utilization)						
10BASE-T (analog core + PLL + digital core)	I_{DDC}	—	66	—	mA	V_{DDA}, V_{DDAP}, V_{DDC} = 1.8V
10BASE-T (Transceiver + Digital I/O)	I_{DDXIO}	—	35	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
CMOS Inputs						
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input Current	I_{IN}	–10	—	10	µA	V_{IN} = GND ~ V_{DDIO}
CMOS Outputs						
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –8 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output Tri-State Leakage	$\|I_{OZ}\|$	—	—	10	µA	—
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	0.95	—	1.05	V	100Ω termination across differential output.
Output Voltage Imbalance	V_{IMB}	—	—	2	%	100Ω termination across differential output.
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty Cycle Distortion	—	—	—	±0.5	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of I_{SET}	V_{SET}	—	0.5	—	V	—
Output Jitter	—	—	0.7	1.4	ns	Peak-to-peak
10BASE-T Receive						
Squelch Threshold	V_{SQ}	—	400	—	mV	5 MHz square wave
10BASE-T Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_P	—	2.3	—	V	100Ω termination across differential output.
Jitter Added	—	—	—	±3.5	ns	Peak-to-peak
Rise/Fall Time	t_r/t_f	—	25	—	ns	—

7.0 TIMING SPECIFICATIONS

7.1 EEPROM Timing

FIGURE 7-1: EEPROM INTERFACE INPUT TIMING DIAGRAM

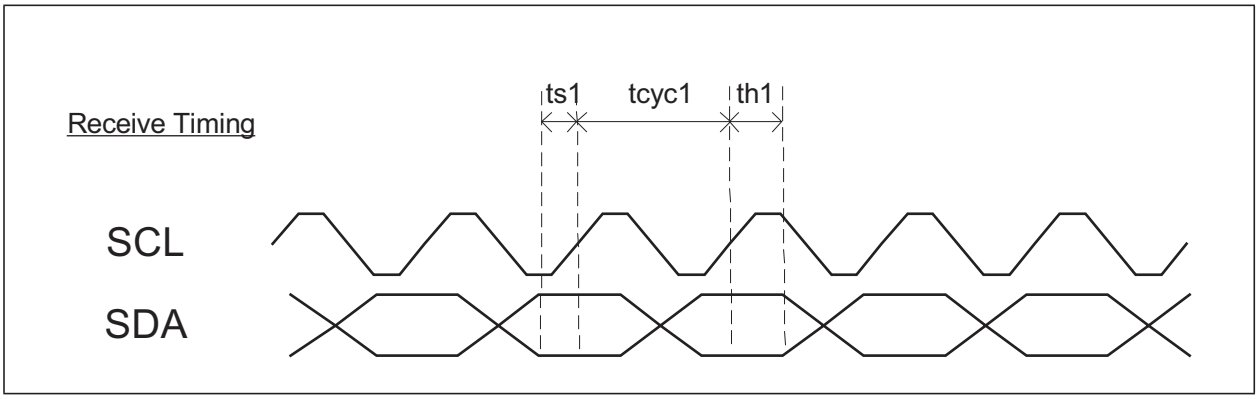


FIGURE 7-2: EEPROM INTERFACE OUTPUT TIMING DIAGRAM

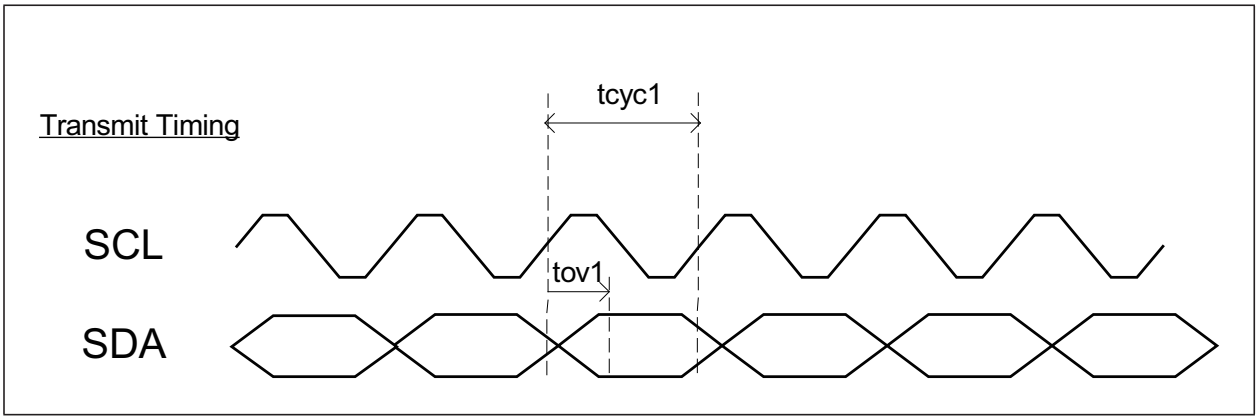


TABLE 7-1: EEPROM TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{cyc1}	Clock cycle	—	16384	—	ns
t_{s1}	Setup time	20	—	—	ns
t_{h1}	Hold time	20	—	—	ns
t_{ov1}	Output valid	4096	4112	4128	ns

7.2 SNI Timing

FIGURE 7-3: SNI INPUT TIMING

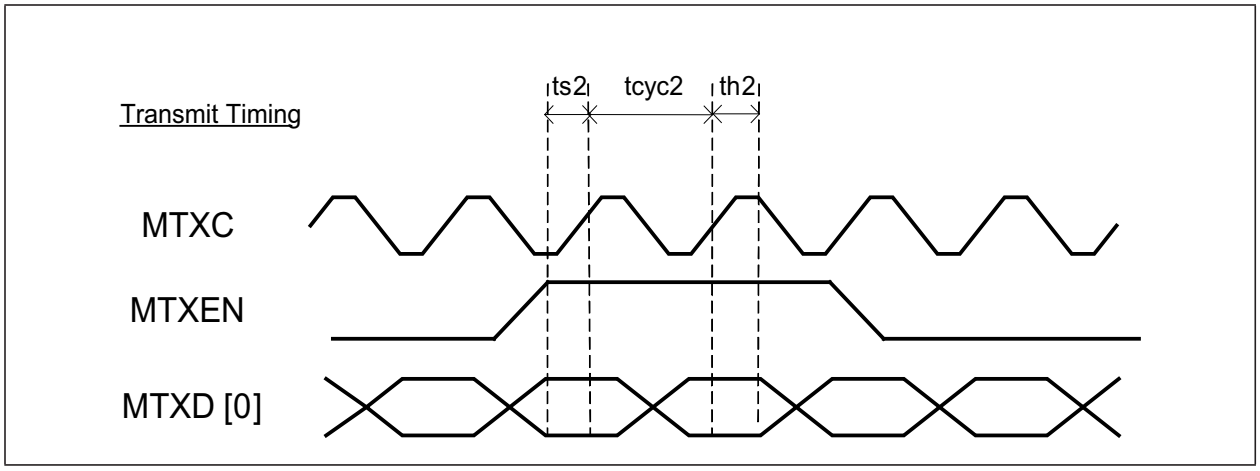


FIGURE 7-4: SNI OUTPUT TIMING

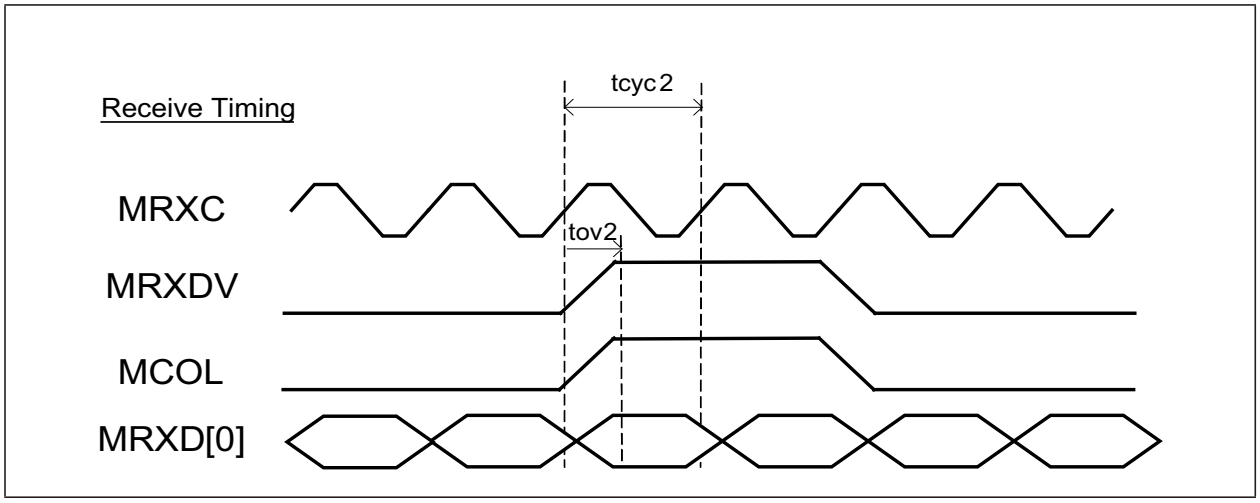


TABLE 7-2: SNI TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{cyc2}	Clock cycle	—	100	—	ns
t_{s2}	Setup time	10	—	—	ns
t_{h2}	Hold time	0	—	—	ns
t_{ov2}	Output valid	0	3	6	ns

7.3 MAC Mode MII Timing

FIGURE 7-5: MAC MODE MII TIMING - DATA RECEIVED FROM MII

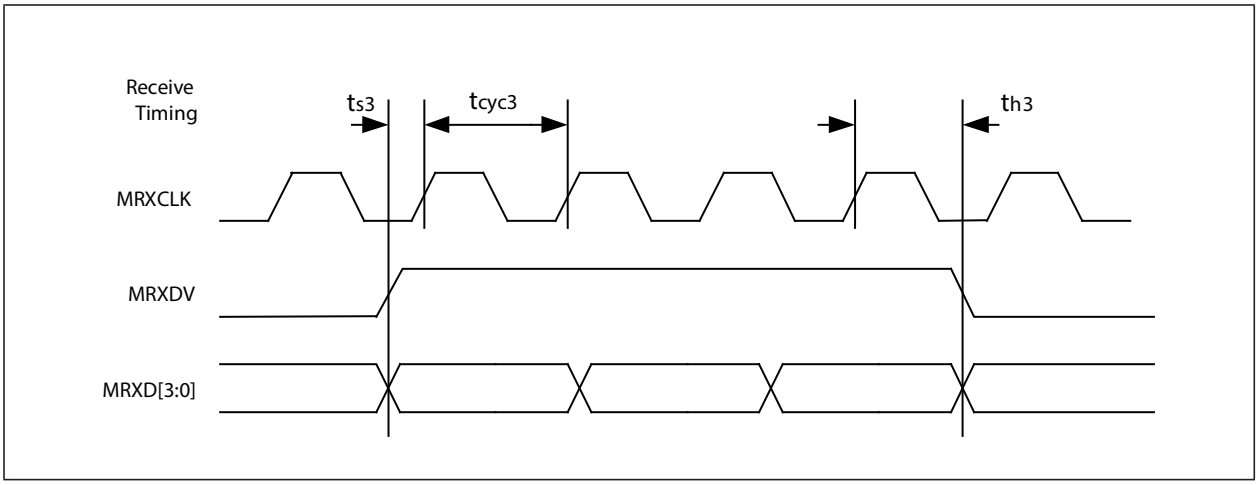


FIGURE 7-6: MAC MODE MII TIMING - DATA INPUT TO MII

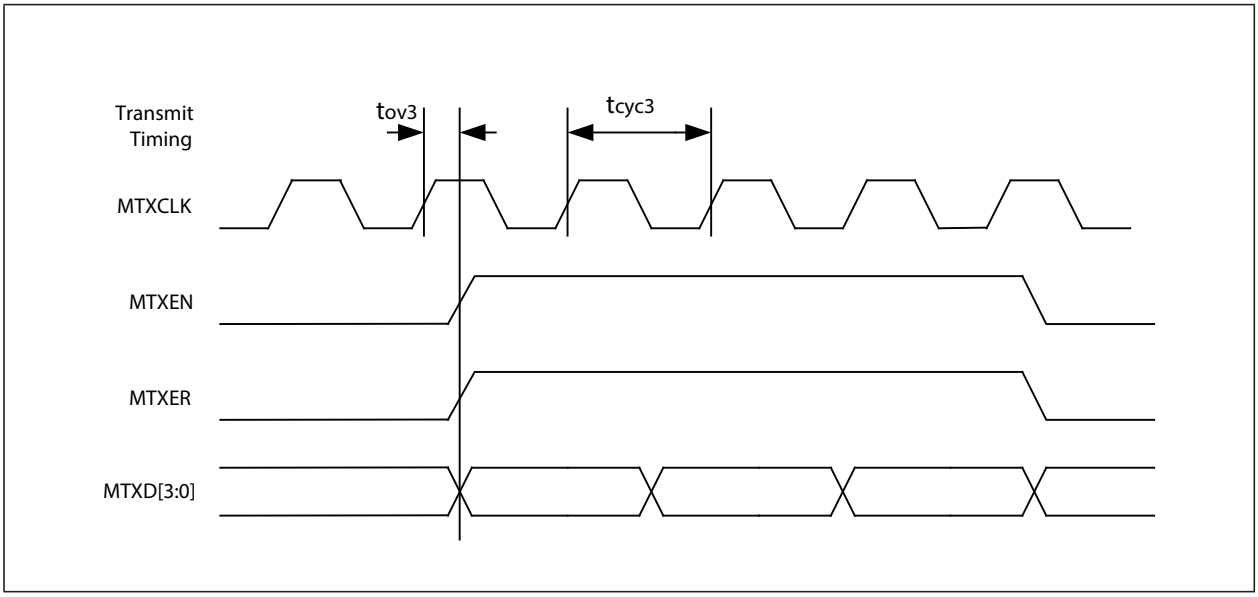


TABLE 7-3: MAC MODE MII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{cyc3}	Clock cycle (100BASE-TX)	—	40	—	ns
t_{cyc3}	Clock cycle (10BASE-T)	—	400	—	ns
t_{s3}	Setup time	10	—	—	ns
t_{h3}	Hold time	10	—	—	ns
t_{ov3}	Output valid	0	—	25	ns

7.4 PHY Mode MII Timing

FIGURE 7-7: PHY MODE MII TIMING – DATA RECEIVED FROM MII

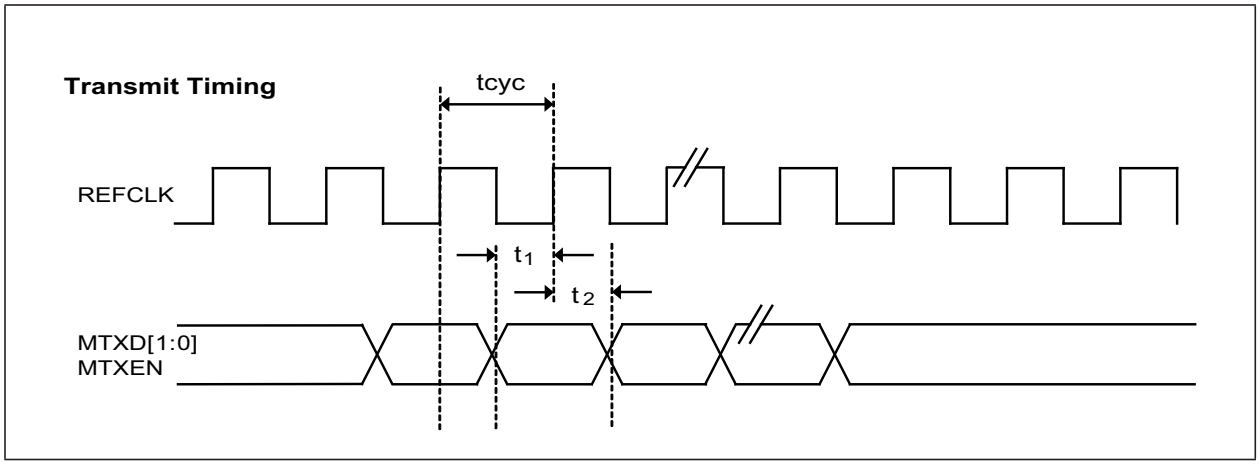


FIGURE 7-8: PHY MODE MII TIMING – DATA INPUT TO MII

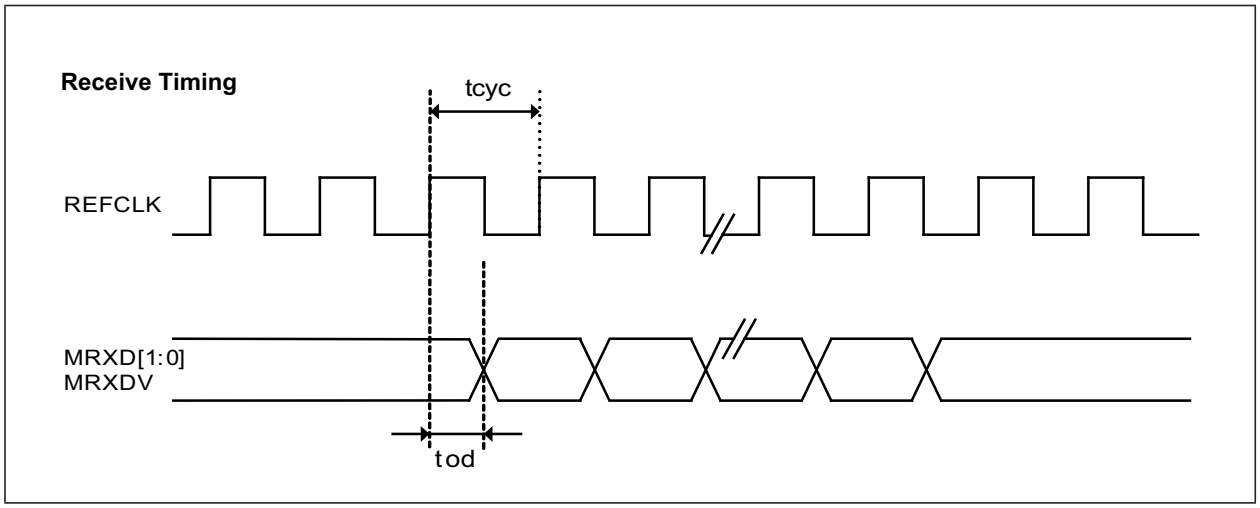


TABLE 7-4: RMII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{cyc4}	Clock cycle (100BASE-T)	—	40	—	ns
t_{cyc4}	Clock cycle (10BASE-T)	—	400	—	ns
t_{s4}	Setup time	10	—	—	ns
t_{h4}	Hold time	10	—	—	ns
t_{ov4}	Output valid	0	—	25	ns

7.5 SPI Timing

FIGURE 7-9: SPI INPUT TIMING

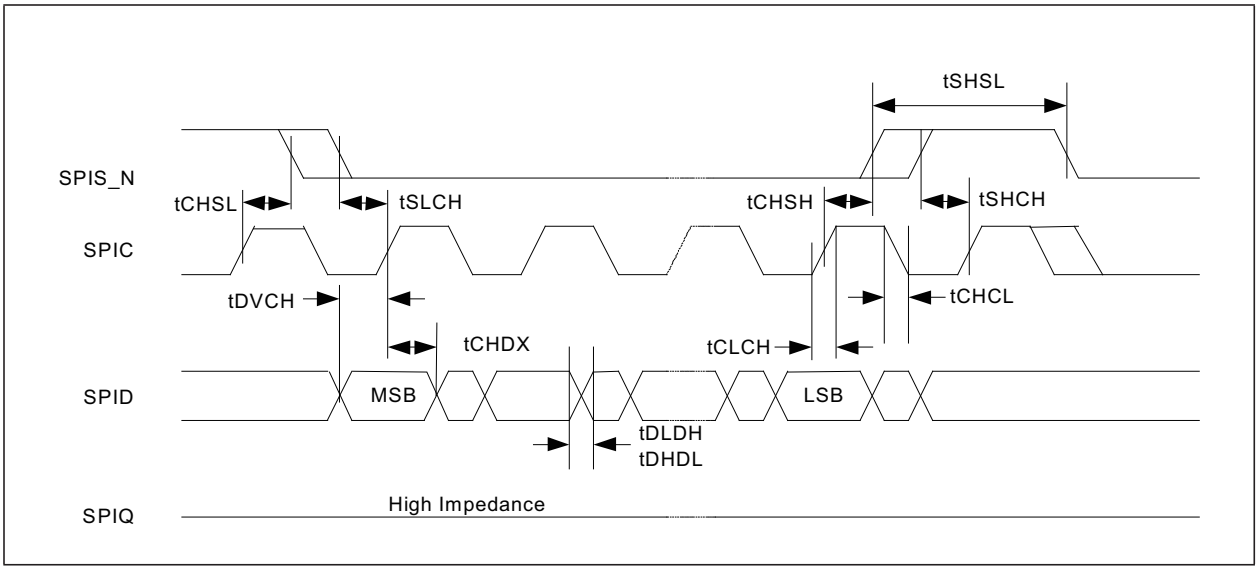


TABLE 7-5: SPI INPUT TIMING PARAMETERS[1]

Parameter	Description	Min.	Max.	Units
f_C	Clock frequency	—	5	MHz
t_{CHSL}	SPIS_N inactive hold time	90	—	ns
t_{SLCH}	SPIS_N active setup time	90	—	ns
t_{CHSH}	SPIS_N active old time	90	—	ns
t_{SHCH}	SPIS_N inactive setup time	90	—	ns
t_{SHSL}	SPIS_N deselect time	100	—	ns
t_{DVCH}	Data input setup time	20	—	ns
t_{CHDX}	Data input hold time	30	—	ns
t_{CLCH}	Clock rise time	—	1	µs
t_{CHCL}	Clock fall time	—	1	µs
t_{DLDH}	Data input rise time	—	1	µs
t_{DHDL}	Data input fall time	—	1	µs

FIGURE 7-10: SPI OUTPUT TIMING

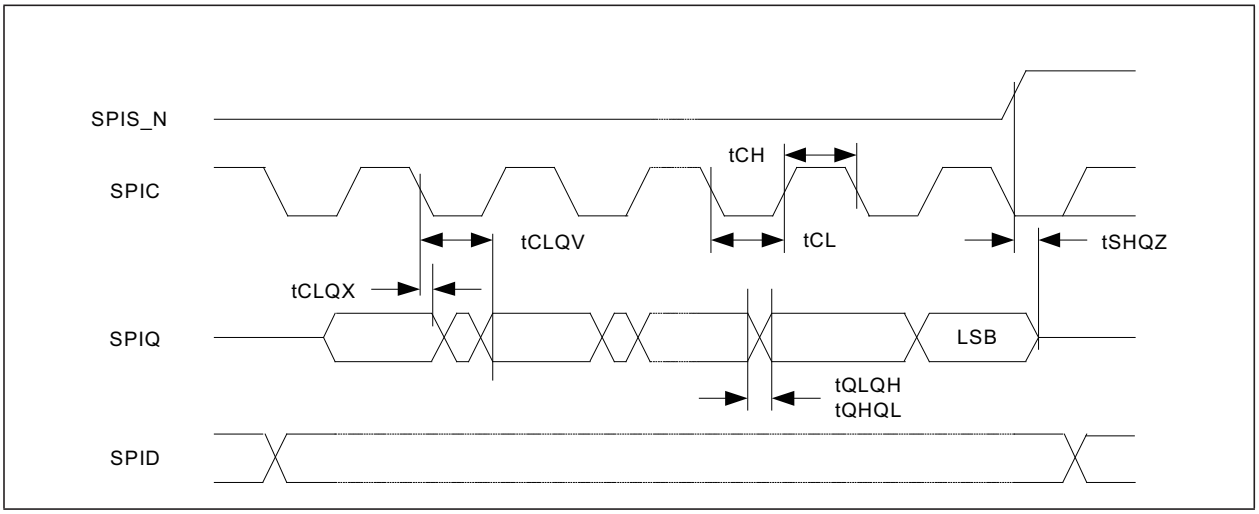


TABLE 7-6: SPI OUTPUT TIMING PARAMETERS

Parameter	Description	Min.	Max.	Units
f_C	Clock frequency	—	5	MHz
t_{CLQX}	SPIQ hold time	0	0	ns
t_{CLQV}	Clock low to SPIQ valid	—	60	ns
t_{CH}	Clock high time	90	—	ns
t_{CL}	Clock low time	90	—	ns
t_{QLQH}	SPIQ rise time	—	50	ns
t_{QHQL}	SPIQ fall time	—	50	ns
t_{SHQZ}	SPIQ disable time	—	100	ns

7.6 Reset Timing

As long as the stable supply voltages to reset high timing (minimum of 10 ms) are met, there is no power sequencing requirement for the KSZ8993M supply voltages (1.8V, 3.3).

It is recommended to wait 100 µs after the de-assertion of reset before starting programming on the managed interface.

The reset timing requirement is summarized in Figure 7-11 and Table 7-7.

FIGURE 7-11: RESET TIMING

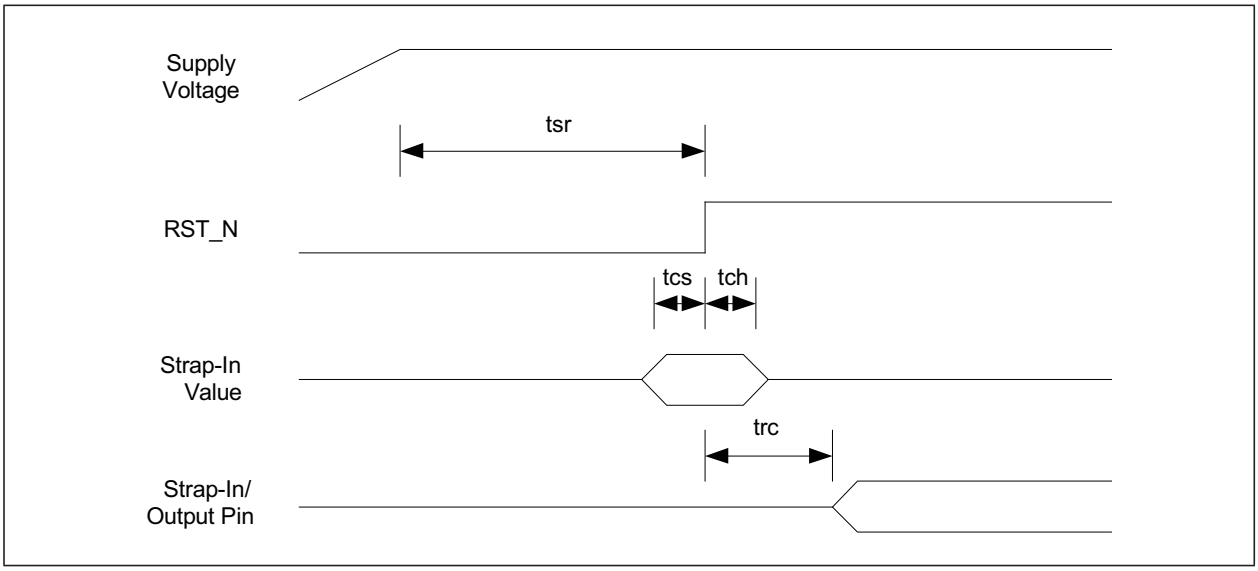


TABLE 7-7: RESET TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{SR}	Stable supply voltages to reset high	10	—	—	ms
t_{CS}	Configuration setup time	50	—	—	ns
t_{CH}	Configuration hold time	50	—	—	ns
t_{RC}	Reset to strap-in pin output	50	—	—	µs

8.0 RESET CIRCUIT

Microchip recommends the following discrete reset circuit as shown in Figure 8-1 when powering up the KSZ8893M/ML/MI device. For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), we recommend the reset circuit as shown in Figure 8-2.

FIGURE 8-1: RECOMMENDED RESET CIRCUIT

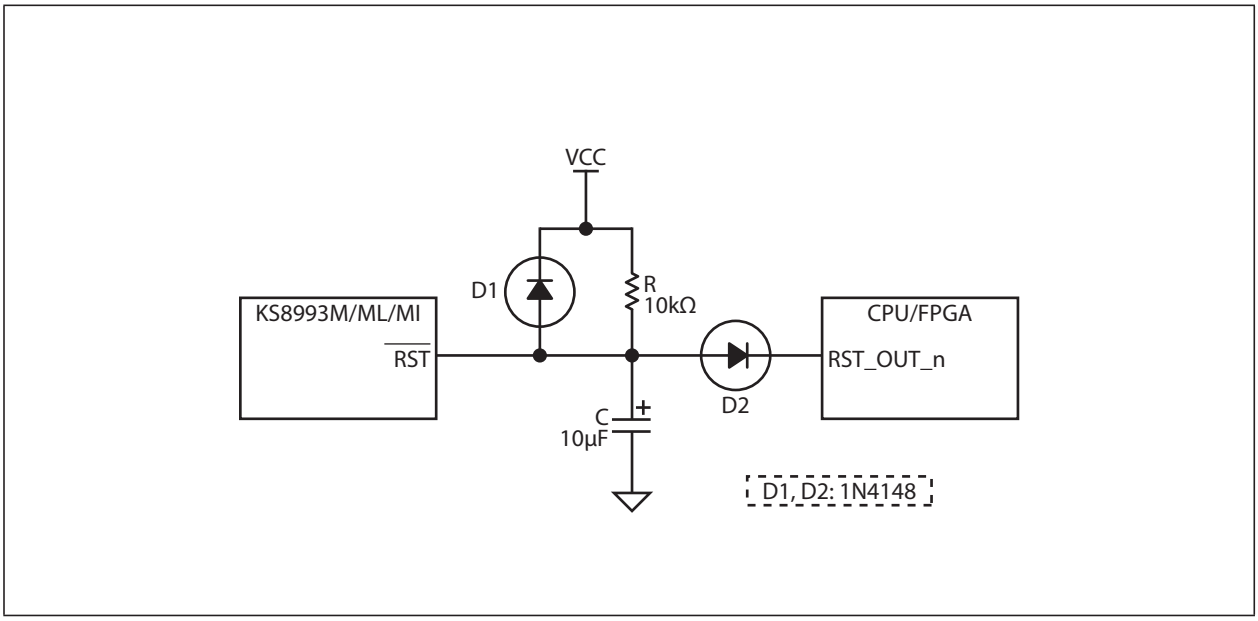
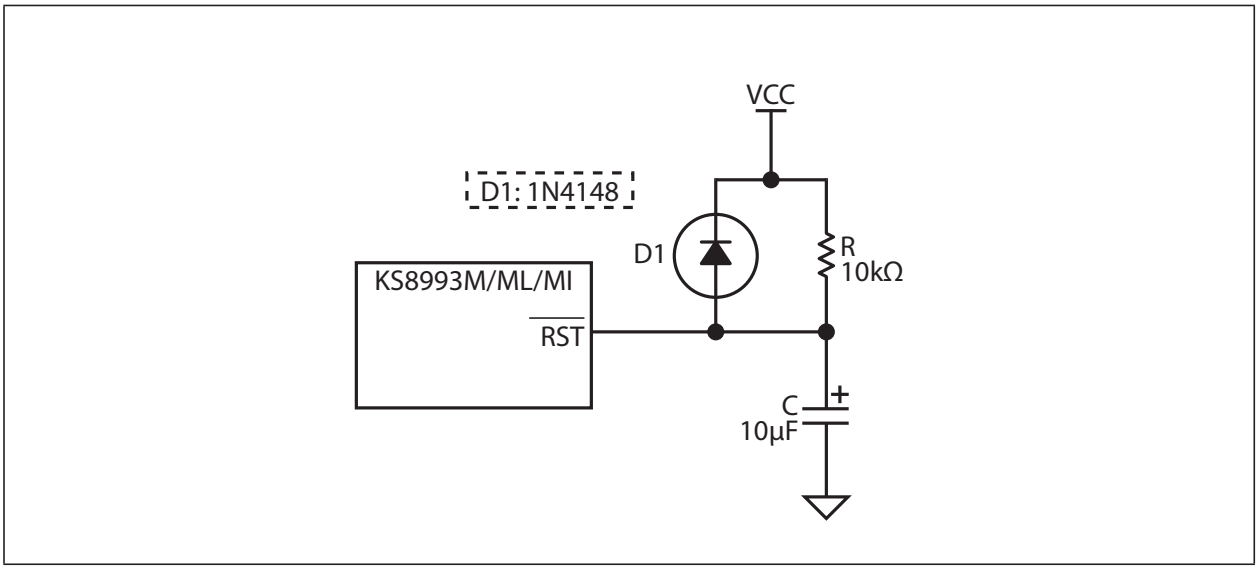


FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET



At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommended to power up the VDD core voltage earlier than VDDIO voltage. At worst case, the both VDD core and VDDIO voltages should come up at the same time.

9.0 SELECTION OF ISOLATION TRANSFORMERS

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements.

Table 9-1 lists recommended transformer characteristics.

TABLE 9-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT : 1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
D.C. Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	1.0 dB	0 MHz to 65 MHz
HIPOT (min.)	1500 V_{RMS}	—

TABLE 9-2: QUALIFIED SINGLE-PORT MAGNETICS

Manufacturer	Part Number	Auto MDI-X
Bel Fuse	S558-5999-U7	Yes
Bel Fuse (MagJack)	SI-46001	Yes
Bel Fuse (MagJack)	SI-50170	Yes
Delta	LF8505	Yes
LanKom	LF-H41S	Yes
Pulse	H1102	Yes
Pulse (Low Cost)	H1260	Yes
Transpower	HB726	Yes
YCL	LF-H41S	Yes

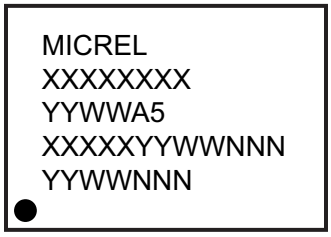
TABLE 9-3: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

Characteristic	Value
Frequency	25 MHz
Frequency Tolerance (max.)	±50 ppm
Load Capacitance (max.)	20 pF
Series Resistance	25Ω

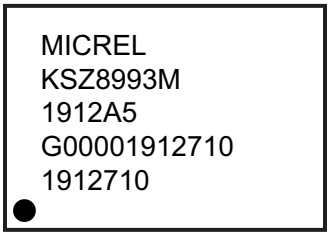
10.0 PACKAGE OUTLINE

10.1 Package Marking Information

128-Lead PQFP*



Example

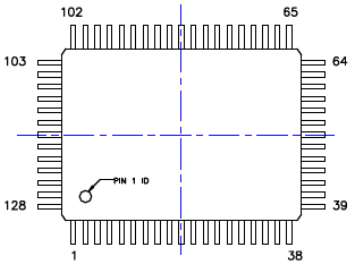


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

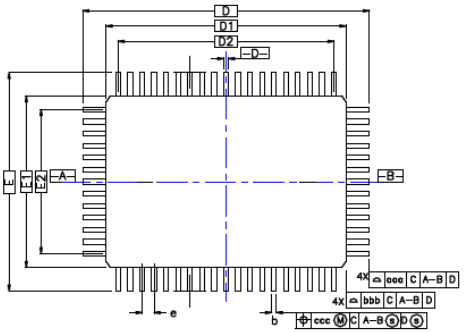
FIGURE 10-1: 128-LEAD PQFP 20 MM X 14 MM PACKAGE

TITLE
128 LEAD PQFP 14x20mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

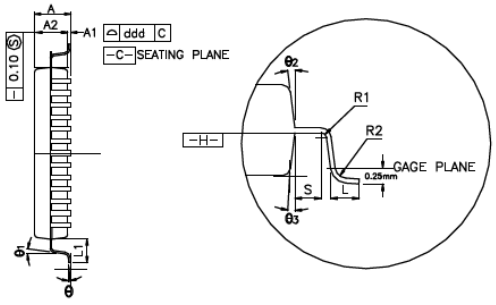
DRAWING #	PQFP14x20-128LD-PL-1	UNIT	MM [INCHES]



TOP VIEW
Note 1,2,3



BOTTOM VIEW
Note 1,2,3



SIDE VIEW
Note 1,2,3

DETAILED VIEW

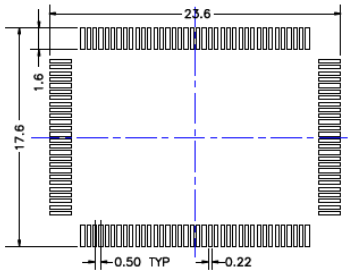
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2 , θ3	15° REF			15° REF		

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.
4. ALL UNITS IN mm. TOLERANCE +/– 0.05 IF NOT NOTED.



RECOMMENDED LAND PATTERN
Note 4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003066A (10-04-19)	—	Converted Micrel data sheet KSZ8993M to Microchip DS00003066A. Minor text changes throughout.

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- Technical Support

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Technical support is available through the web site at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	X	—	XX
Device	Interface	Supply Voltage	Temperature		Media Type

Device:	KSZ8993 (in 128-lead 20 mm x 14 mm PQFP)
Interface:	M = MII Interface
Supply Voltage:	L = Single 3.3V Power Supply Supported with Internal 1.8V LDO
Temperature:	<blank> = 0°C to +70°C (Commercial) I = –40°C to +85°C (Industrial)
Media Type:	<blank> = 66/Tray TR = 350/Reel

Examples:

a) KSZ8993M
MII Interface
128-lead 20 mm x 14 mm PQFP
Commercial Temperature Range
66/Tray

b) KSZ8993M-TR
MII Interface
128-lead 20 mm x 14 mm PQFP
Commercial Temperature Range
350/Reel

c) KSZ8993MI
MII Interface
128-lead 20 mm x 14 mm PQFP
Industrial Temperature Range
66/Tray

d) KSZ8993ML
MII Interface
128-lead 20 mm x 14 mm PQFP
Single 3.3V Power Supply Supported with Internal 1.8V LDO
Commercial Temperature Range
66/Tray

e) KSZ8993MLI
MII Interface
128-lead 20 mm x 14 mm PQFP
Single 3.3V Power Supply Supported with Internal 1.8V LDO
Industrial Temperature Range
66/Tray

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip devices:

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