

300V, Low-Charge Injection, 16-Channel, High-Voltage Analog Switch

Features

- 300V, 16-Channel High-Voltage Analog Switch
- 3.3V or 5.0V CMOS Input Logic Level
- 33 MHz Data Shift Clock Frequency
- Very Low Quiescent Current (10 μ A)
- Low Parasitic Capacitance
- DC to 50 MHz Analog Small-Signal Frequency
- -60 dB Typical Off Isolation at 5.0 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Flexible Operating Supply Voltage
- Integrated Bleed Resistors on the Outputs (both sides for HV2721, one side only for HV2722)

Applications

- Medical Ultrasound Imaging
- Nondestructive Testing (NDT) Metal Flaw Detection
- Multi-Layer Printed Circuit Board (PCB) Tester
- Piezoelectric Transducer Drivers
- Inkjet Printer Head
- Optical MEMS Module

General Description

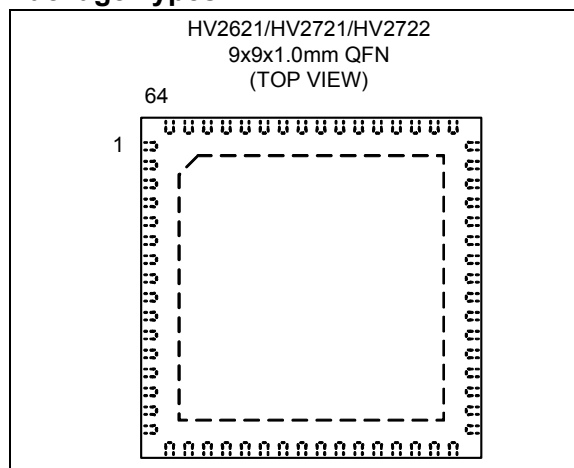
The HV2621/HV2721/HV2722 devices are 300V, low-charge injection, 16-channel, high-voltage analog switches. These devices are designed for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers. HV2621/HV2721 are almost identical to HV2601/2701 but have larger signal range. If the $V_{PP}/V_{NN} = \pm 150V$, HV2621/HV2721/HV2722 can pass the analog signal up to $\pm 135V$.

The HV2721 has integrated bleed resistors on both sides of the switches. HV2722 has integrated bleed resistors on one side, SWxA only. HV2621 has no bleed resistors. The bleed resistor eliminates voltage build-up on capacitive loads such as piezoelectric transducers.

Input data are shifted into a 16-bit shift register that can then be retained in a 16-bit latch. To change all the switch state at the same time, the latch enable bar should be left high until all bits are clocked in. The input data are clocked in at the rising edge of the clock. After all bits are clocked in to the shift register, a negative pulse of the latch enable bar changes all the switch ON/OFF states defined by input data at the same time. Using the HVC MOS technology, these devices combine 300V high-voltage bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

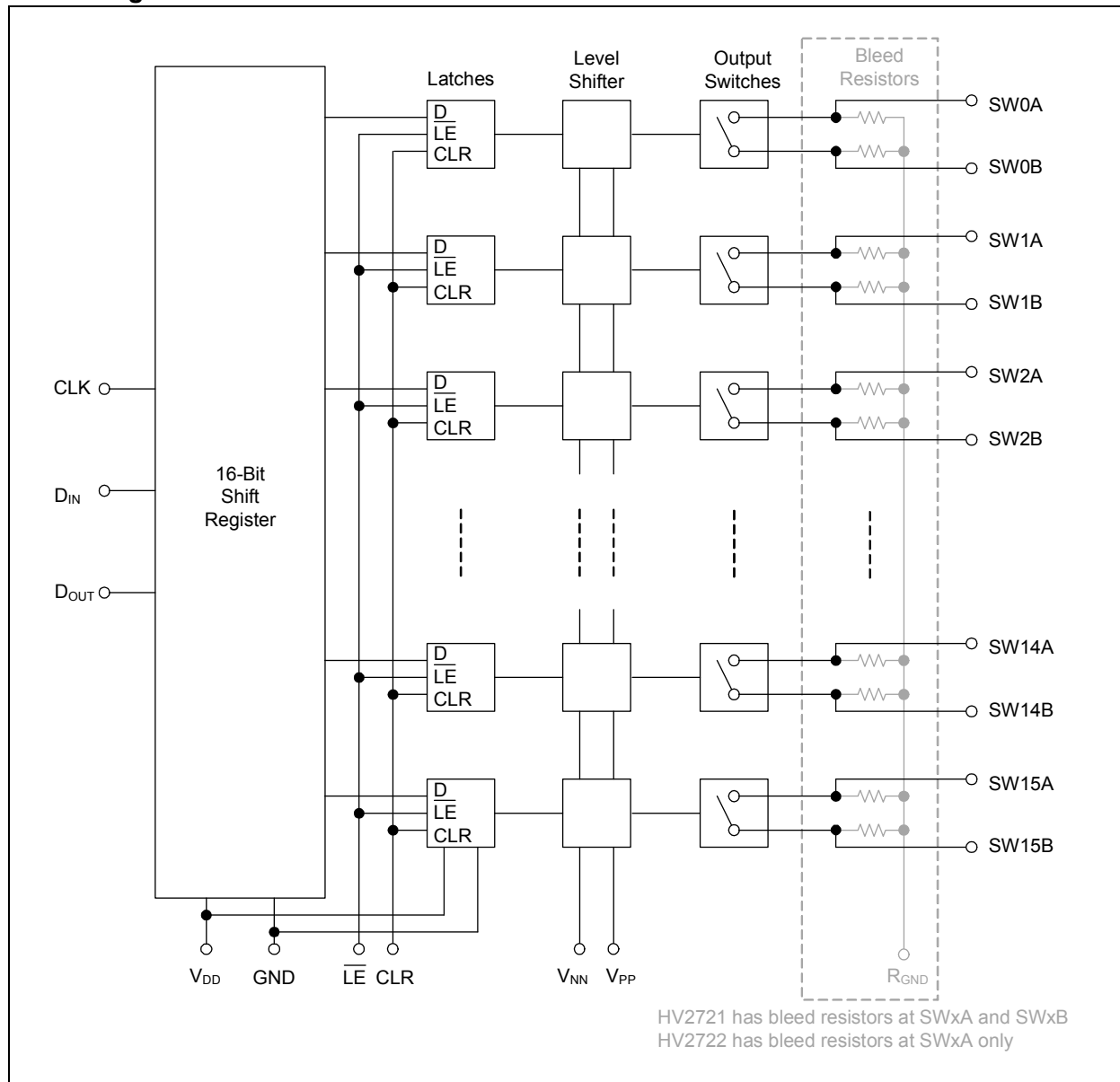
These devices are suitable for various combinations of high-voltage supplies, e.g., V_{PP}/V_{NN} : +60V/-240V, +150V/-150V, and +260V/-40V.

Package Types



HV2621/HV2721/HV2722

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Logic Supply Voltage (V_{DD}).....	-0.5V to 6.5V
Differential Supply Voltage ($V_{PP}-V_{NN}$).....	330V
Positive Supply Voltage (V_{PP}).....	-0.5V to $V_{NN}+300V$
Negative Supply Voltage (V_{NN}).....	-300V to +0.5V
Logic Input Voltage (V_{IN}).....	-0.5V to $V_{DD}+0.3V$
Analog Signal Range (V_{SIG}).....	V_{NN} to V_{PP}
Peak Analog Signal Current/Channel (I_{PK}).....	3A

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES 1, 2, 3)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{DD}	3	—	5.5	V	
Differential Supply Voltage	$V_{PP}-V_{NN}$	60	—	300	V	
Positive Supply Voltage	V_{PP}	60	—	260	V	
Negative Supply Voltage	V_{NN}	-240	—	0	V	
High-Level Input Voltage	V_{IH}	$0.9V_{DD}$	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	$0.1V_{DD}$	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	$V_{NN}+15$	—	$V_{PP}-15$	V	

- Note 1:** Recommended power up sequence is V_{DD} , V_{PP} and V_{NN} . Power down is in reverse order.
Note 2: V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
Note 3: Rise and fall times of power supplies, V_{DD} , V_{PP} and V_{NN} should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{PP} = +150V$, $V_{NN} = -150V$, $V_{DD} = 5.0V$, $T_A = 25^\circ C$. **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Small Signal Switch On-Resistance	R_{ONS}	—	26	48	Ω	$I_{SIG} = 5 \text{ mA}$ $V_{PP} = +60V$, $V_{NN} = -240V$
		—	22	32	Ω	$I_{SIG} = 150 \text{ mA}$
		—	22	30	Ω	$I_{SIG} = 5 \text{ mA}$ $V_{PP} = +150V$, $V_{NN} = -150V$
		—	18	27	Ω	$I_{SIG} = 150 \text{ mA}$
		—	20	30	Ω	$I_{SIG} = 5 \text{ mA}$ $V_{PP} = +260V$, $V_{NN} = -40V$
		—	16	27	Ω	$I_{SIG} = 150 \text{ mA}$
Small Signal Switch On-Resistance Matching	ΔR_{ONS}	—	5	20	%	$I_{SIG} = 5 \text{ mA}$, $V_{PP} = +150V$, $V_{NN} = -150V$
Large Signal Switch On-Resistance	R_{ONL}	—	17	—	Ω	$V_{SIG} = V_{PP}-15V$, $I_{SIG} = 1A$
Value of Output Bleed Resistor (HV2721/HV2722 Only)	R_{INT}	30	50	70	k Ω	Output switch to RGND, $I_{RINT} = 0.5 \text{ mA}$
Switch Off Leakage per Switch	I_{SOL}	—	1	15	μA	$V_{SIG} = V_{PP}-15V$, $V_{NN} = +15V$. See Figure 3-1
DC Offset Switch Off	V_{OS}	—	1	10	mV	$R_{LOAD} = 35 \text{ k}\Omega$ (HV2621), 70 k Ω (HV2722), No load (HV2721), see Figure 3-2
DC Offset Switch On		—	1	10		

HV2621/HV2721/HV2722

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, $V_{PP} = +150V$, $V_{NN} = -150V$, $V_{DD} = 5.0V$, $T_A = 25^\circ C$. **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments	
Quiescent V _{PP} Supply Current	I _{PPQ}	—	10	50	μA	All switches off	
Quiescent V _{NN} Supply Current	I _{NNQ}	—	10	50	μA		
Quiescent V _{PP} Supply Current	I _{PPQ}	—	10	50	μA	All switches on, I _{SW} = 5.0 mA	
Quiescent V _{NN} Supply Current	I _{NNQ}	—	10	50	μA		
Switch Output Peak Current	I _{SW}	2.0	3.0	—	A	V _{SIG} duty cycle <0.1% (Note 1)	
Output Switching Frequency	f _{SW}	—	—	50	kHz	Duty cycle = 50% (Note 1)	
Average V _{PP} Supply Current	I _{PP}	—	—	3	mA	V _{PP} = +60V, V _{NN} = -240V	All output switches are turning on and off at 10 kHz with no load
		—	—	4	mA	V _{PP} = +150V, V _{NN} = -150V	
		— —	—	6	mA	V _{PP} = +260V, V _{NN} = -40V	
Average V _{NN} Supply Current	I _{NN}	—	—	3	mA	V _{PP} = +60V, V _{NN} = -240V	All output switches are turning on and off at 10 kHz with no load
		—	—	4	mA	V _{PP} = +150V, V _{NN} = -150V	
		— —	—	6	mA	V _{PP} = +260V, V _{NN} = -40V	
Average V _{DD} Supply Current	I _{DD}	—	—	4	mA	f _{CLK} = 5 MHz, f _{DIN} = 2.5 MHz	
Quiescent V _{DD} Supply Current	I _{DDQ}	—	—	10	μA	All logic inputs are static	
Data Out Source Current	I _{SOR}	8	—	—	mA	V _{OUT} = V _{DD} -0.7V	
Data Out Sink Current	I _{SINK}	12	—	—	mA	V _{OUT} = 0.7V	
Logic Input Capacitance	C _{IN}	—	—	10	pF	Note 2	

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{PP} = +150V$, $V_{NN} = -150V$, $V_{DD} = 5.0V$, $t_R = t_F \leq 5.0\text{ ns}$, 50% duty cycle, $C_{LOAD} = 20\text{ pF}$, $T_A = 25^\circ C$, **Boldface** specifications apply over the full operating temperature range.

Sym.	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Setup Time before \overline{LE} rises	t_{SD}	25	—	—	ns	Note 1
Time Width of \overline{LE}	t_{WLE}	56	—	—	ns	$V_{DD} = 3.3V$ (Note 1)
		12	—	—	ns	$V_{DD} = 5.0V$ (Note 1)
Clock Delay Time to Data Out	t_{DO}	-	—	45	ns	$V_{DD} = 3.3V$
		-	—	25	ns	$V_{DD} = 5.0V$
Time Width of CLR	t_{WCLR}	55	—	—	ns	Note 1
Setup Time Data to Clock	t_{SU}	7	—	—	ns	$V_{DD} = 3.3V$ (Note 1)
		7	—	—	ns	$V_{DD} = 5.0V$ (Note 1)
Hold Time Data from Clock	t_H	4	—	—	ns	$V_{DD} = 3.3V$ (Note 1)
		3.5	—	—	ns	$V_{DD} = 5.0V$ (Note 1)

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, $V_{PP} = +150V$, $V_{NN} = -150V$, $V_{DD} = 5.0V$, $t_R = t_F \leq 5.0$ ns, 50% duty cycle, $C_{LOAD} = 20$ pF, $T_A = 25^\circ C$, **Boldface** specifications apply over the full operating temperature range.

Sym.	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Clock Frequency	f_{CLK}	—	—	16	MHz	$V_{DD} = 3.3V$ (Note 1)
		—	—	33	MHz	$V_{DD} = 5.0V$ (Note 1)
Clock Rise and Fall Time	t_R, t_F	—	—	50	ns	Note 1
Turn-On Time	t_{ON}	—	—	6	μs	$V_{SIG} = V_{PP}-15V$, $R_{LOAD} = 20$ k Ω See Figure 3-3
Turn-Off Time	t_{OFF}	—	—	6		
Maximum V_{SIG} Slew Rate	dV/dt	—	—	20	V/ns	$V_{PP} = +60V$, $V_{NN} = -240V$ (Note 1)
		—	—	20		$V_{PP} = +150V$, $V_{NN} = -150V$ (Note 1)
		—	—	20		$V_{PP} = +260V$, $V_{NN} = -40V$ (Note 1)
Off Isolation	K_O	—	-55	-50	dB	$f = 5.0$ MHz, 1.0 k Ω /15 pF load See Figure 3-4 (Note 1)
		—	-60	-58		$f = 5.0$ MHz, 50 Ω load See Figure 3-4 (Note 1)
Switch Crosstalk	K_{CR}	—	-70	-60	dB	$f = 5.0$ MHz, 50 Ω load See Figure 3-5 (Note 1)
Output Switch Isolation Diode Current	I_{ID}	—	—	200	mA	300 ns pulse width, 2.0% duty cycle, See Figure 3-6 (Note 1)
Off Capacitance SW to GND	$C_{SG(OFF)}$	—	10	—	pF	$V_{SIG} = 50$ mV@1MHz, no load (Note 1)
On Capacitance SW to GND	$C_{SG(ON)}$	—	18	—		
Output Voltage Spike at SWA, SWB	$+V_{SPK}$	—	—	250	mV	$V_{PP} = +60V$, $V_{NN} = -240V$, $R_{LOAD} = 50\Omega$, see Figure 3-7 (Note 1)
	$-V_{SPK}$	-250	—	—		
	$+V_{SPK}$	—	—	250		$V_{PP} = +150V$, $V_{NN} = -150V$, $R_{LOAD} = 50\Omega$, see Figure 3-7 (Note 1)
	$-V_{SPK}$	-250	—	—		
	$+V_{SPK}$	—	—	250		$V_{PP} = +260V$, $V_{NN} = -40V$, $R_{LOAD} = 50\Omega$, see Figure 3-7 (Note 1)
	$-V_{SPK}$	-250	—	—		
Charge Injection	QC	—	1000	—	pC	$V_{PP} = +60V$, $V_{NN} = -240V$, $V_{SIG} = 0V$, see Figure 3-8 (Note 1)
		—	770	—		$V_{PP} = +150V$, $V_{NN} = -150V$, $V_{SIG} = 0V$, see Figure 3-8 (Note 1)
		—	360	—		$V_{PP} = +260V$, $V_{NN} = -40V$, $V_{SIG} = 0V$, see Figure 3-8 (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATION

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Range						
Operating Temperature Range	T_A	0	—	+70	$^\circ C$	
Storage Temperature Range	T_S	-65	—	+150	$^\circ C$	
Maximum Junction Temperature	T_J	—	—	+125	$^\circ C$	
Package Thermal Resistance						
Thermal Resistance, 64L QFN	Θ_{JA}	—	21	—	$^\circ C/W$	

HV2621/HV2721/HV2722

TABLE 1-1: TRUTH TABLE (NOTES 1, 2, 3, 4, 5, 6)

D0	D1	...	D7	D8	...	D15	$\overline{\text{LE}}$	CLR	SW0	SW1	...	SW7	SW8	...	SW15	
L	—	...	—	—	...	—	L	L	OFF	—	...	—	—	...	—	
H	—		—	—		—	L	L	ON	—		—	—			
—	L		—	—		—	L	L	—	OFF		—	—			
—	H		—	—		—	L	L	—	ON		—	—			
—	—		—	—		—	L	L	—	—		—	—			
—	—		—	—		—	L	L	—	—		—	—			
—	—		L	—		—	L	L	—	—		OFF	—		—	
—	—		H	—		—	L	L	—	—		ON	—		—	
—	—		—	L		—	L	L	—	—		—	OFF		—	—
—	—		—	H		—	L	L	—	—		—	ON		—	—
—	—		—	—		—	—	L	L	—		—	—		—	—
—	—		—	—		—	—	L	L	—		—	—		—	—
—	—		—	—		—	L	L	L	—		—	—		—	—
—	—		—	—		—	H	L	L	—		—	—		—	—
X	X		X	X		X	X	X	H	L		HOLD PREVIOUS STATE				
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF							

- Note 1:** The 16 switches operate independently.
- 2:** Serial data is clocked in on the L to H transition of the CLK.
- 3:** All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{\text{LE}}$. When $\overline{\text{LE}}$ is low, the shift registers data flow through the latch.
- 4:** DOUT is high when data in the register 15 is high.
- 5:** Shift register clocking has no effect on the switch states if $\overline{\text{LE}}$ is high.
- 6:** The CLR clear input overrides all the inputs.

1.1 Typical Timing Diagrams

Figure 1-1 shows the timing of the AC characteristic parameters graphically.

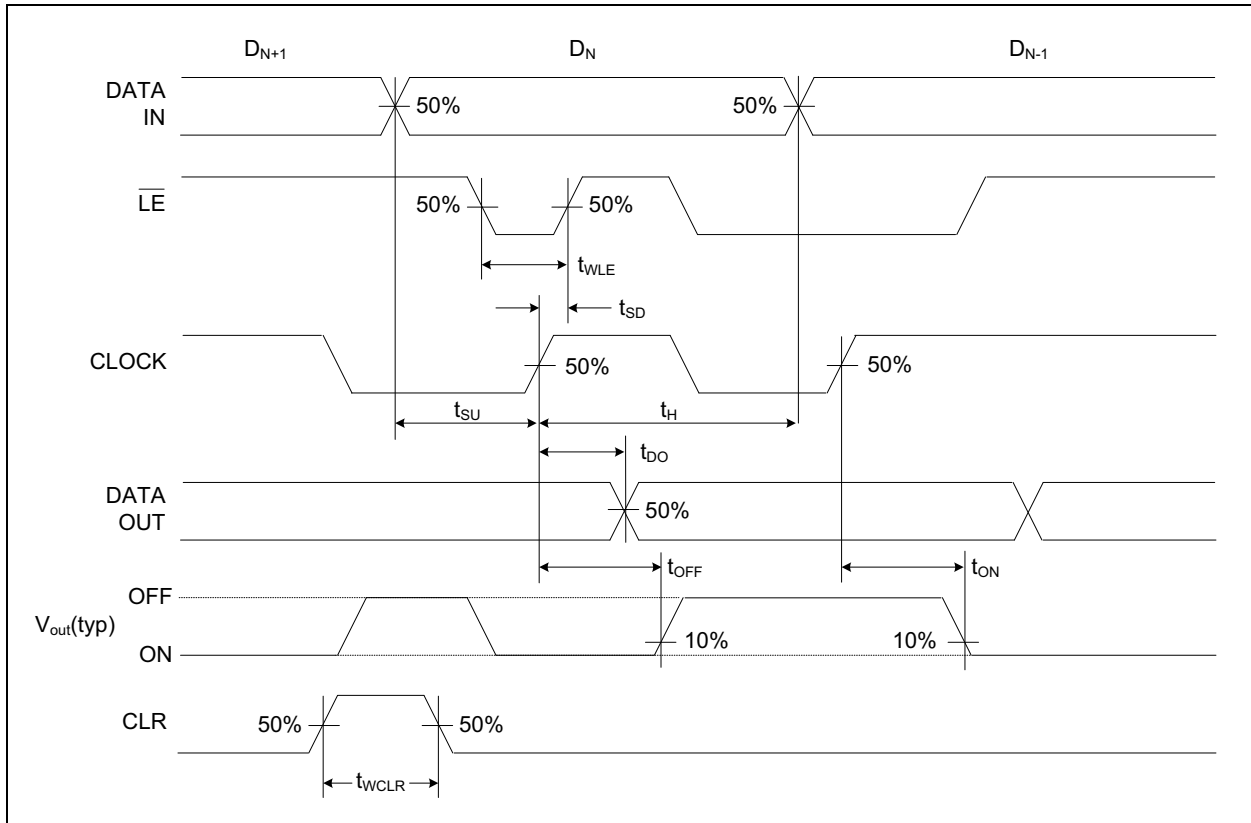


FIGURE 1-1: Logic Input Timing Diagram.

HV2621/HV2721/HV2722

2.0 PIN DESCRIPTION

This section details the pin description for 64-lead QFN package (Figure 2-1).The descriptions of the pins are listed in Table 2-1.

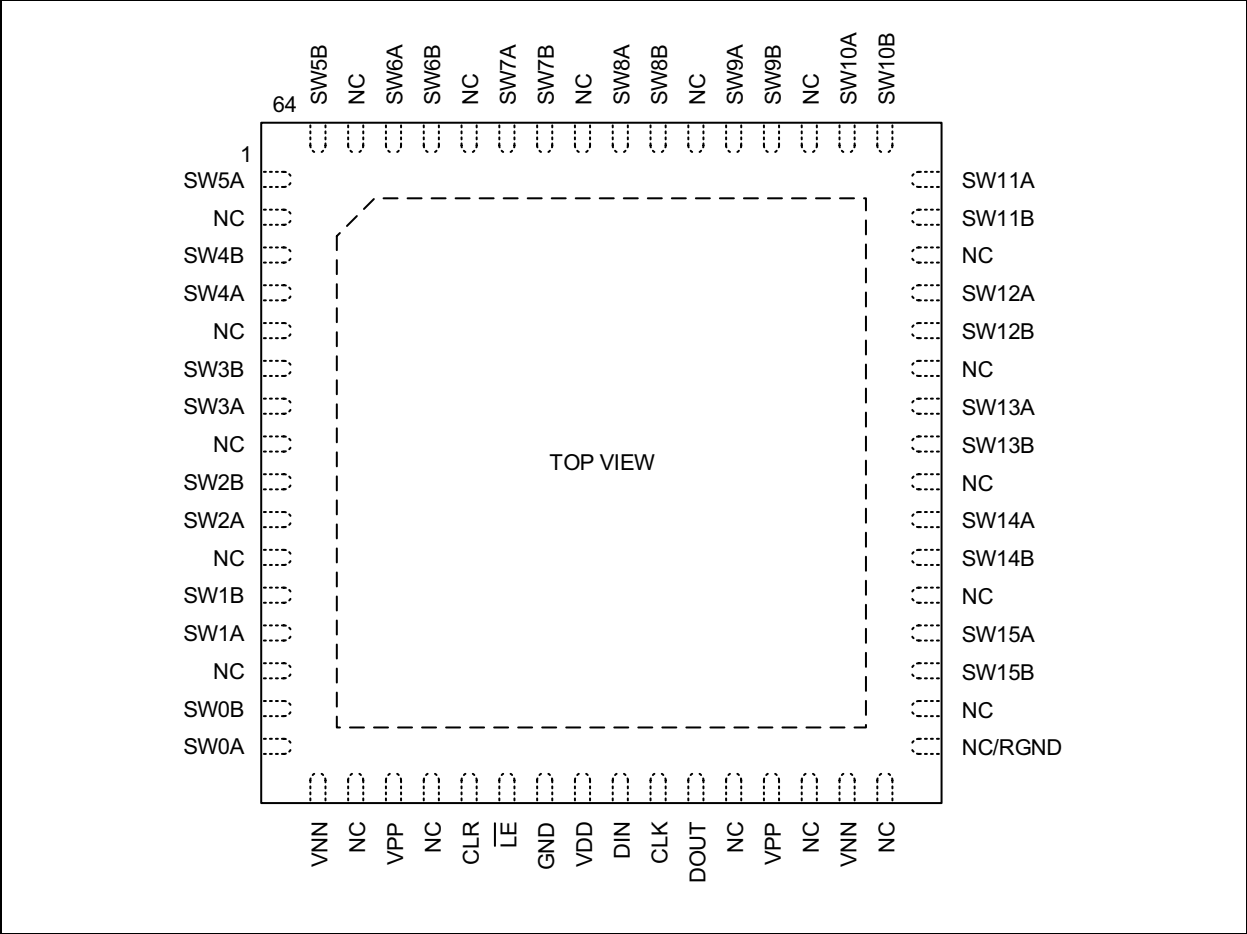


FIGURE 2-1: 64-Lead QFN Package - Top View.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol		Description
	HV2621	HV2721/ HV2722	
1	SW5A	SW5A	Analog Switch 5 Terminal A
2	NC	NC	No Connection
3	SW4B	SW4B	Analog Switch 4 Terminal B
4	SW4A	SW4A	Analog Switch 4 Terminal A
5	NC	NC	No Connection
6	SW3B	SW3B	Analog Switch 3 Terminal B
7	SW3A	SW3A	Analog Switch 3 Terminal A
8	NC	NC	No Connection
9	SW2B	SW2B	Analog Switch 2 Terminal B
10	SW2A	SW2A	Analog Switch 2 Terminal A
11	NC	NC	No Connection

HV2621/HV2721/HV2722

Pin Number	Symbol		Description
	HV2621	HV2721/ HV2722	
12	SW1B	SW1B	Analog Switch 1 Terminal B
13	SW1A	SW1A	Analog Switch 1 Terminal A
14	NC	NC	No Connection
15	SW0B	SW0B	Analog Switch 0 Terminal B
16	SW0A	SW0A	Analog Switch 0 Terminal A
17	V _{NN}	V _{NN}	Negative Supply Voltage
18	NC	NC	No Connection
19	V _{PP}	V _{PP}	Positive Supply Voltage
20	NC	NC	No Connection
21	CLR	CLR	Latch Clear Logic Input
22	$\overline{\text{LE}}$	$\overline{\text{LE}}$	Latch Enable Logic Input
23	GND	GND	Ground
24	V _{DD}	V _{DD}	Logic Supply Voltage
25	D _{IN}	D _{IN}	Data In Logic Input
26	CLK	CLK	Clock Logic Input for Shift Register
27	D _{OUT}	D _{OUT}	Data Out Logic Output
28	NC	NC	No Connection
29	V _{PP}	V _{PP}	Positive Supply Voltage
30	NC	NC	No Connection
31	V _{NN}	V _{NN}	Negative Supply Voltage
32	NC	NC	No Connection
33	NC	RGND	No Connection/Ground for Bleed Resistor
34	NC	NC	No Connection
35	SW15B	SW15B	Analog Switch 15 Terminal B
36	SW15A	SW15A	Analog switch 15 Terminal A
37	NC	NC	No Connection
38	SW14B	SW14B	Analog Switch 14 Terminal B
39	SW14A	SW14A	Analog Switch 14 Terminal A
40	NC	NC	No Connection
41	SW13B	SW13B	Analog Switch 13 Terminal B
42	SW13A	SW13A	Analog switch 13 Terminal A
43	NC	NC	No Connection
44	SW12B	SW12B	Analog Switch 12 Terminal B
45	SW12A	SW12A	Analog Switch 12 Terminal A
46	NC	NC	No Connection
47	SW11B	SW11B	Analog Switch 11 Terminal B
48	SW11A	SW11A	Analog Switch 11 Terminal A
49	SW10B	SW10B	Analog Switch 10 Terminal B
50	SW10A	SW10A	Analog Switch 10 Terminal A
51	NC	NC	No Connection
52	SW9B	SW9B	Analog Switch 9 Terminal B
53	SW9A	SW9A	Analog Switch 9 Terminal A
54	NC	NC	No Connection

HV2621/HV2721/HV2722

Pin Number	Symbol		Description
	HV2621	HV2721/ HV2722	
55	SW8B	SW8B	Analog Switch 8 Terminal B
56	SW8A	SW8A	Analog Switch 8 Terminal A
57	NC	NC	No Connection
58	SW7B	SW7B	Analog Switch 7 Terminal B
59	SW7A	SW7A	Analog Switch 7 terminal A
60	NC	NC	No Connection
61	SW6B	SW6B	Analog Switch 6 Terminal B
62	SW6A	SW6A	Analog Switch 6 Terminal A
63	NC	NC	No Connection
64	SW5B	SW5B	Analog Switch 5 Terminal B
VSUB (Thermal Pad)			The central thermal pad on the bottom of package must be connected to VNN externally

3.0 TEST CIRCUIT EXAMPLES

This section details a few example of test circuits.

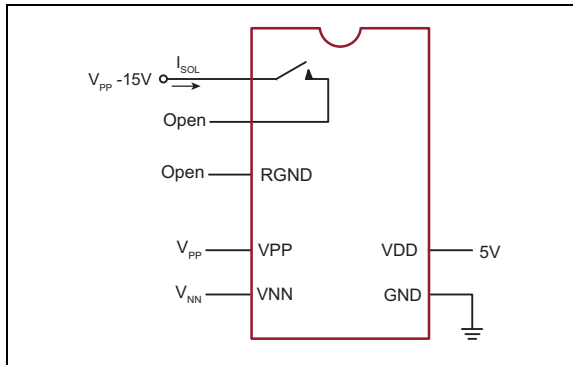


FIGURE 3-1: Switch Off Leakage per Switch.

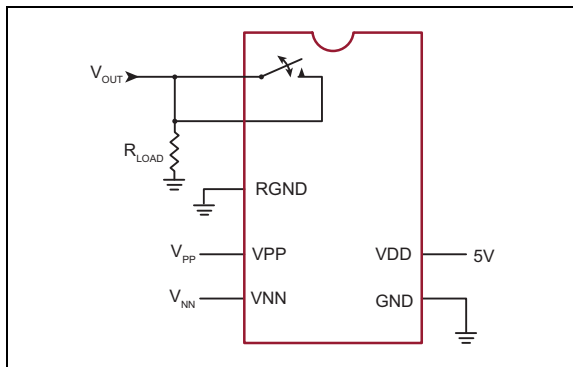


FIGURE 3-2: DC Offset Switch On/Off.

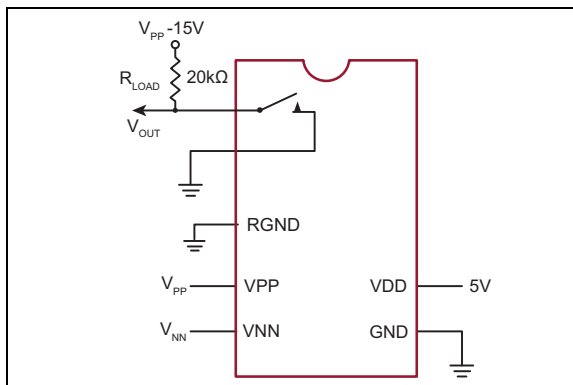


FIGURE 3-3: T_{ON}/T_{OFF} Test Circuit.

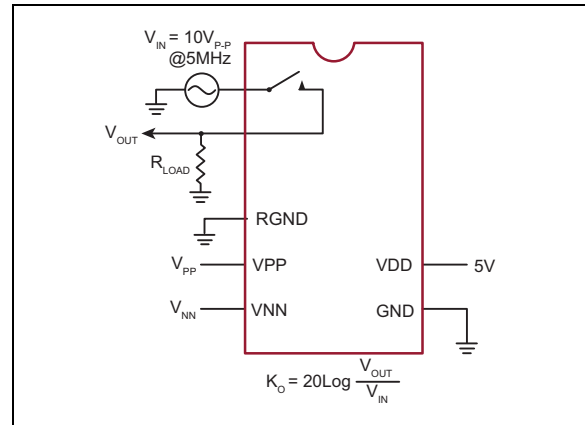


FIGURE 3-4: Off Isolation.

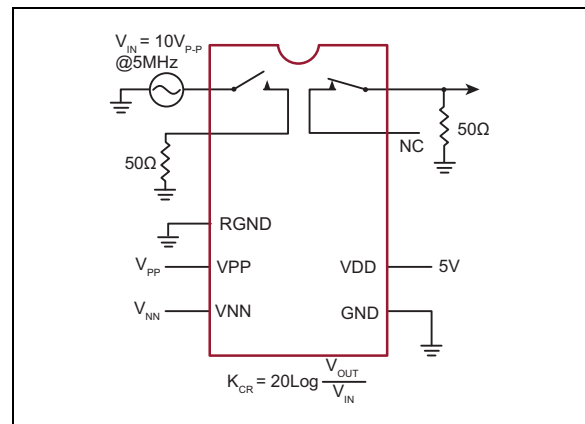


FIGURE 3-5: Switch Crosstalk.

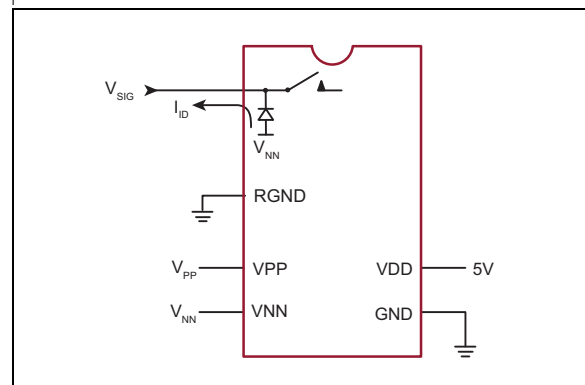


FIGURE 3-6: Isolation Diode Current.

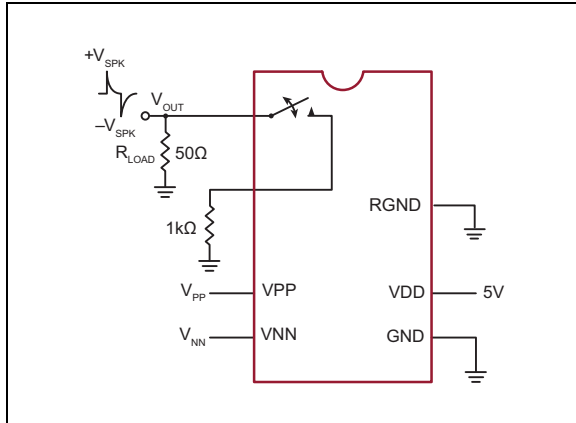


FIGURE 3-7: Output Voltage Spike.

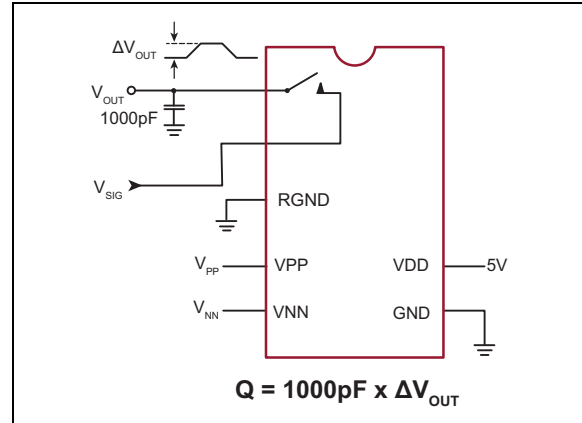


FIGURE 3-8: Charge Injection.

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{PP} = +150V$, $V_{NN} = -150V$, $V_{DD} = 5.0V$, $T_A = 25^\circ C$.

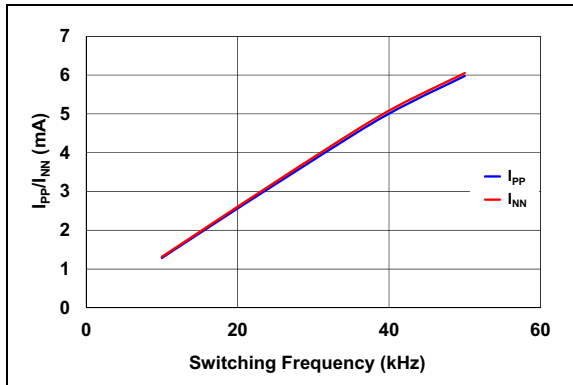


FIGURE 4-1: I_{PP}/I_{NN} vs. Switching Frequency.

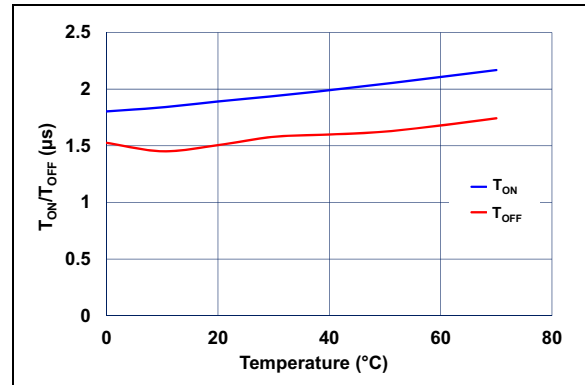


FIGURE 4-4: T_{ON}/T_{OFF} vs. Temperature.

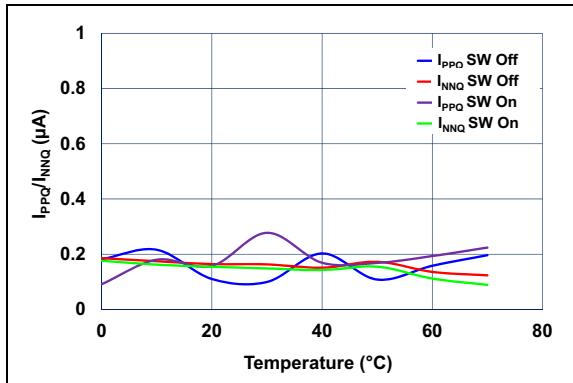


FIGURE 4-2: I_{PPQ}/I_{NNQ} vs. Temperature.

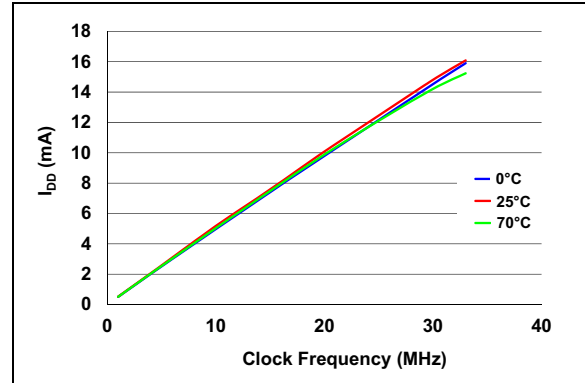


FIGURE 4-5: I_{DD} vs. CLK Frequency.

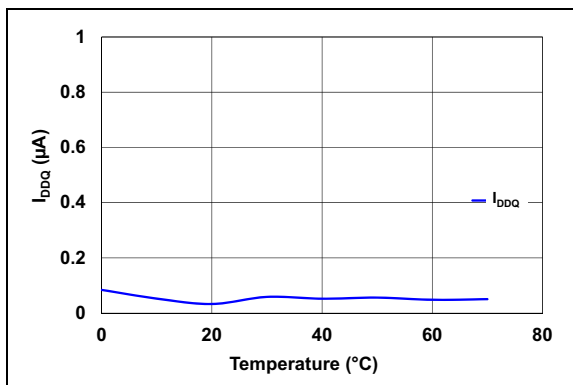


FIGURE 4-3: I_{DDQ} vs. Temperature.

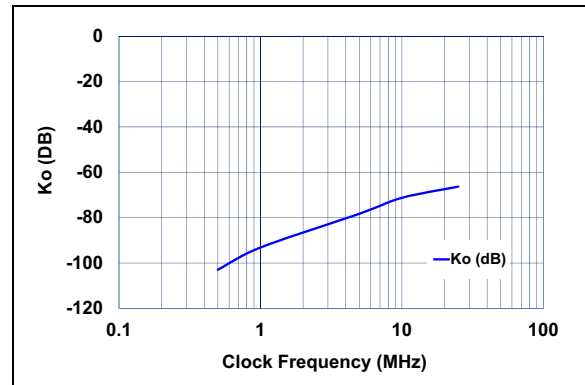


FIGURE 4-6: K_O vs. Frequency with 50Ω Load.

5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

The HV2621/HV2721/HV2722 are 300V, low-charge injection, 16-channel, high-voltage analog switches. The high-voltage analog switches are used for multiplexing a piezoelectric transducer array in a probe to multiple channel transmitters (Tx) arrays in a medical ultrasound system.

The HV2621/HV2721/HV2722 are distinguished by bleed resistors that eliminate voltage build-up in capacitance load such as piezoelectric transducers. These devices can pass $\pm 135\text{V}$ high-voltage large signal with $V_{PP}/V_{NN} = \pm 150\text{V}$. These devices have typical 18Ω on-resistance and 50 MHz bandwidth for small-signals.

Figure 5-1 shows a typical medical ultrasound image system consisting 64-channels of transmit pulsers, 64-channels of receivers (LNA and ADC) and 64-channels of T/R switches connecting to 192 elements of an ultrasound probe via a HV2XXX high-voltage analog switch array.

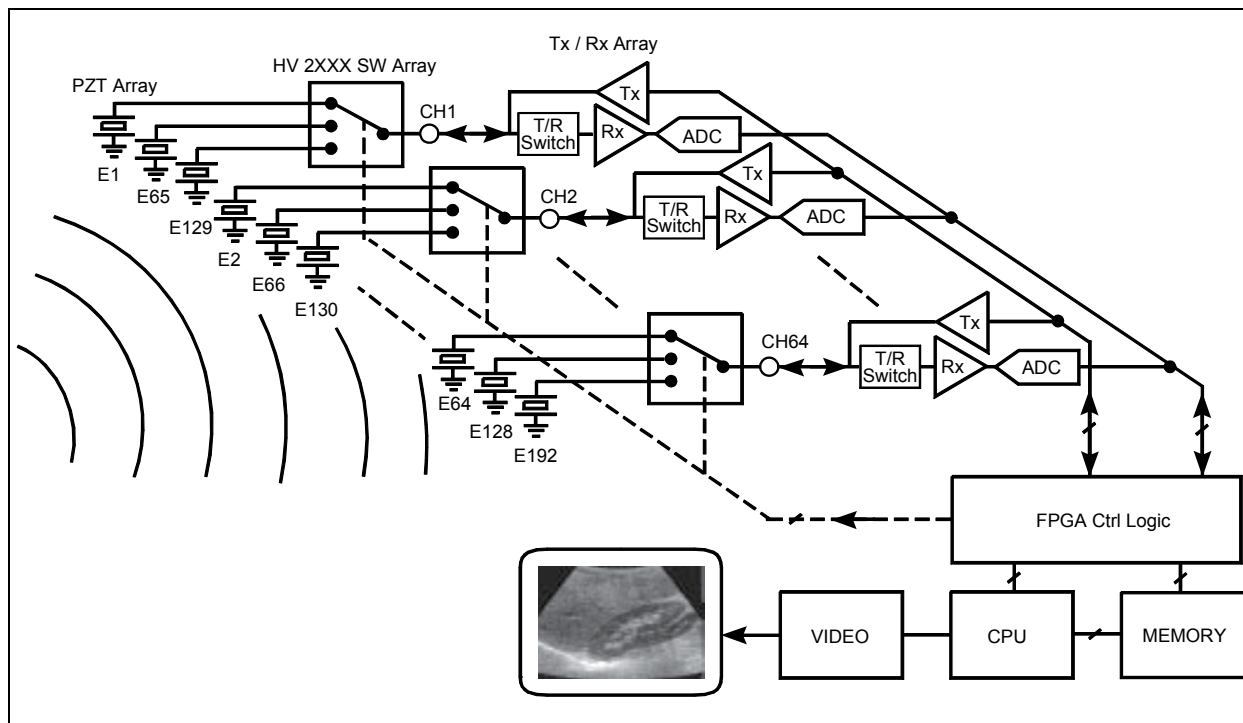


FIGURE 5-1: Typical Medical Ultrasound Imaging System.

5.2 Logic Input Timing

The HV2621/HV2721/HV2722 have digital serial interface consisting of Data In (D_{IN}), Clock (CLK), Data Out (D_{OUT}), Latch Enable (\overline{LE}), and Clear (CLR) to control 16 switches individually. The digital circuits are supplied by V_{DD} . The serial clock frequency is up to 33 MHz.

The switch state configuration data is shifted into the shift registers at the rising edge (low-to-high transition) of the clock. The switch configuration bit of SW15 is shifted in first and the configuration bit of SW0 is shifted in last. To change all the switch states at the same time, the Latch Enable Input (\overline{LE}) should remain high while the 16-bit Data In signal is shifted into the 16-bit register. After the valid 16-bit data completes shifting into the shift registers, the high-to-low transition of the \overline{LE} signal transfers the contents of the shift

registers into the latches. Finally, setting the \overline{LE} high again, allows all the latches to keep the current state while new data can now be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 16 latches to low. Consequently, all the high-voltage switches are set to OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate regardless of the CLR signal. Therefore, when the CLR input is low, the shift register still retains the previous data.

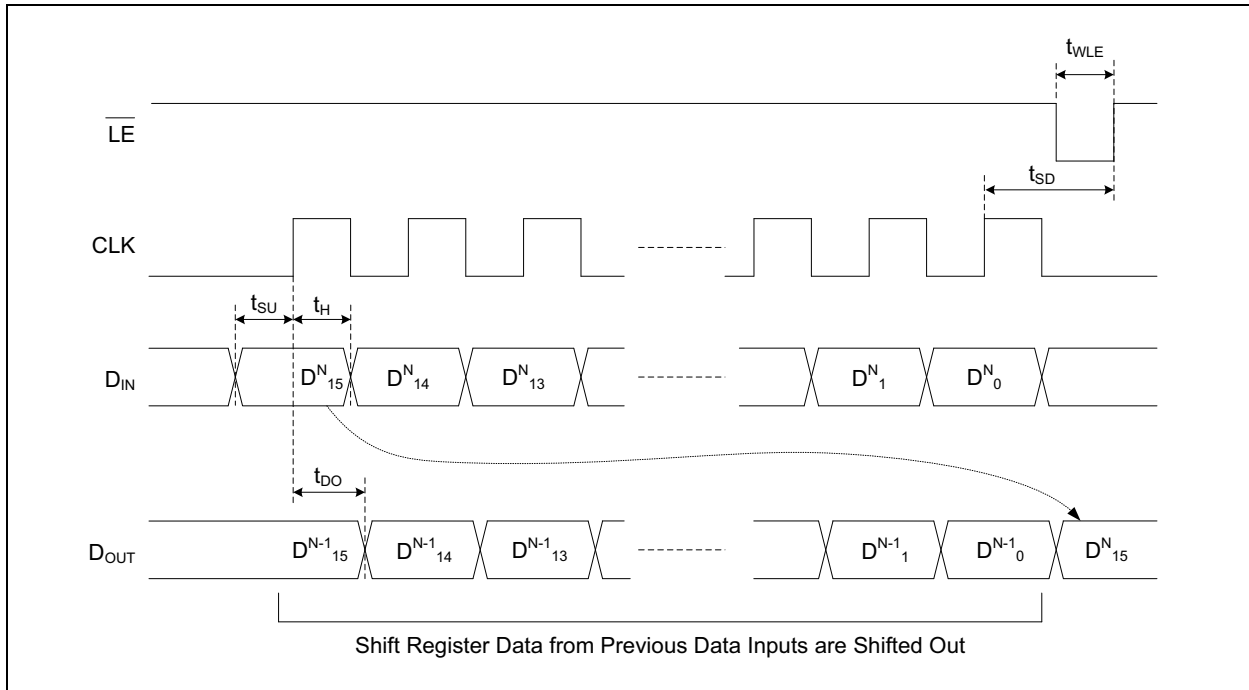


FIGURE 5-2: Latch Enable Timing Diagram.

5.3 Multiple Devices Connection

The digital serial interface of the HV2621/HV2721/HV2722 allows multiple devices to make a daisy-chain together. In this configuration, D_{OUT} of a device is connected to the D_{IN} of the subsequent device, and so forth. The last D_{OUT} of the daisy-chained HV2621/HV2721/HV2722 can be either floating or fed back to an FPGA to check the previously stored data in the shift registers.

To control all the high-voltage analog switch states in daisy-chained N devices, N -times 16 clocks and N -times 16 bits of data are shifted into shift registers, while \overline{LE} remains high and CLR remains low. After all the data finishes shifting in, one single negative pulse of \overline{LE} transfers the data from all the shift registers to all the latches simultaneously. Consequently, all N -times 16 high-voltage analog switches change states simultaneously.

5.4 Power Up/Down Sequence and Decoupling Capacitor

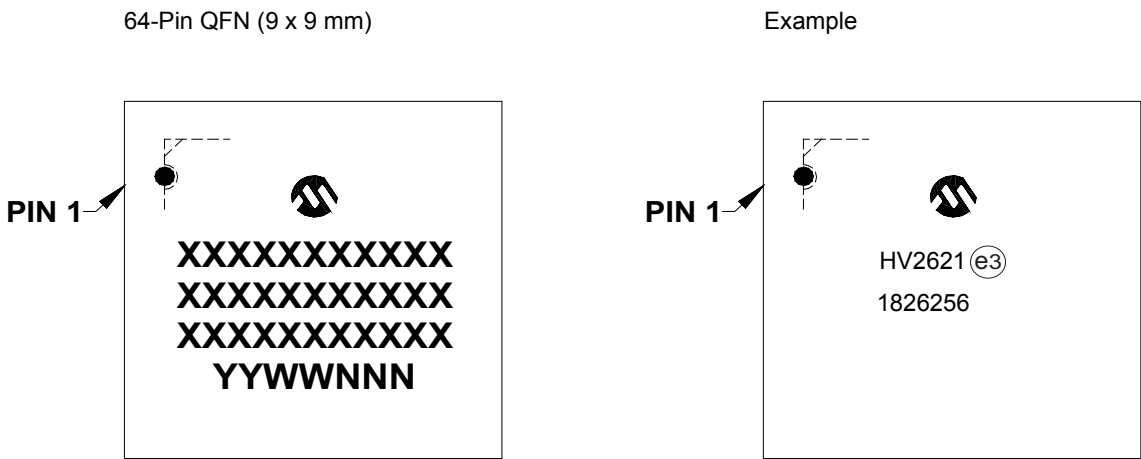
The recommended power up sequence is V_{DD} , V_{PP} and V_{NN} . The power down sequence is in reverse order. We also recommend the rise time and fall time of power supplies are greater than 1 msec. During the power up/down period, all the analog switch inputs should be within between V_{PP} and V_{NN} or floating.

It is recommended that 0.1 μF or larger ceramic decoupling capacitors, with the appropriate voltage ratings, be connected between GND and other supplies (V_{PP} , V_{NN} and V_{DD}). These decoupling capacitors should be placed as close as possible to the device.

HV2621/HV2721/HV2722

6.0 PACKAGING INFORMATION

6.1 Package Marking Information



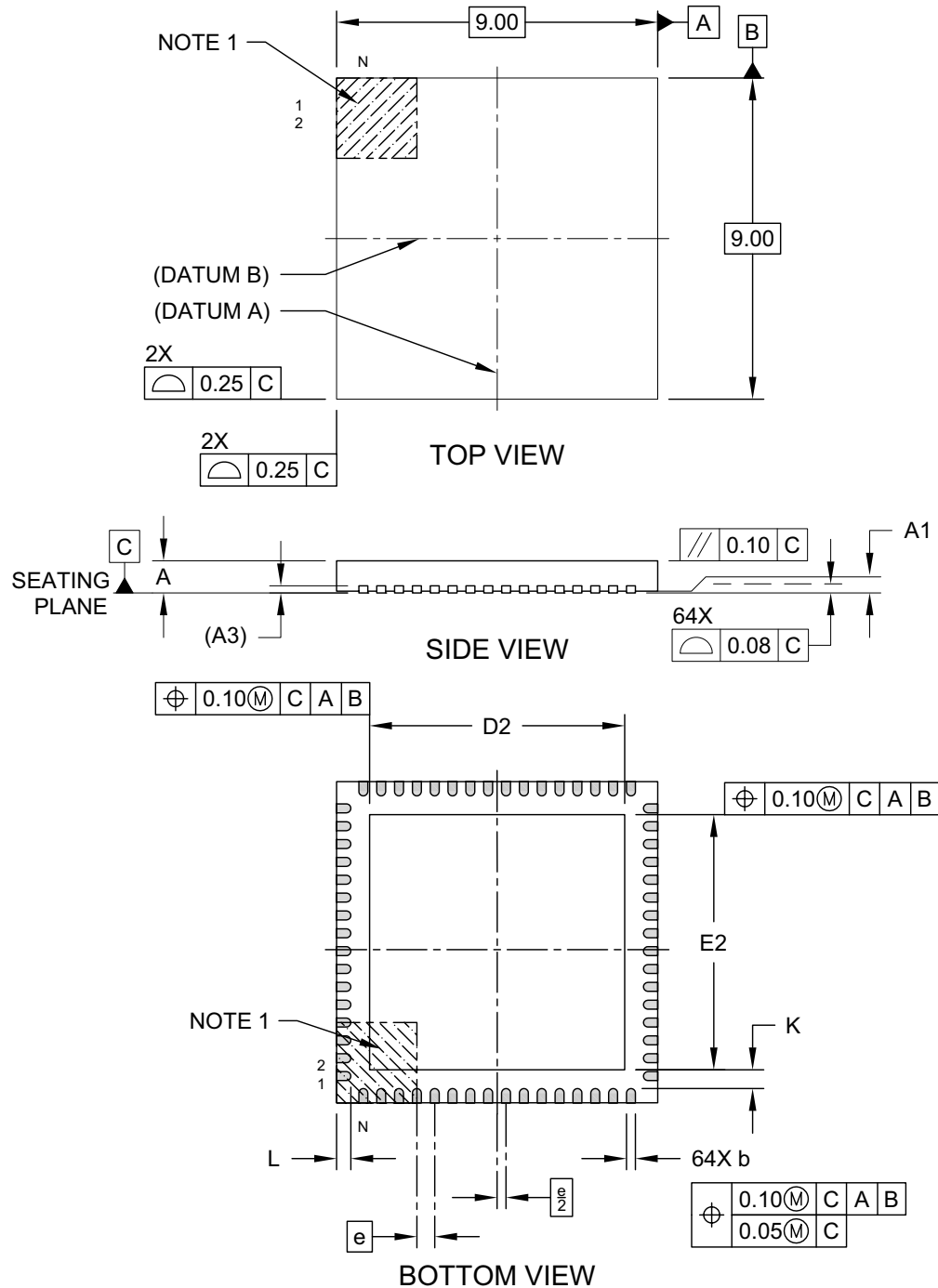
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

HV2621/HV2721/HV2722

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN] With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

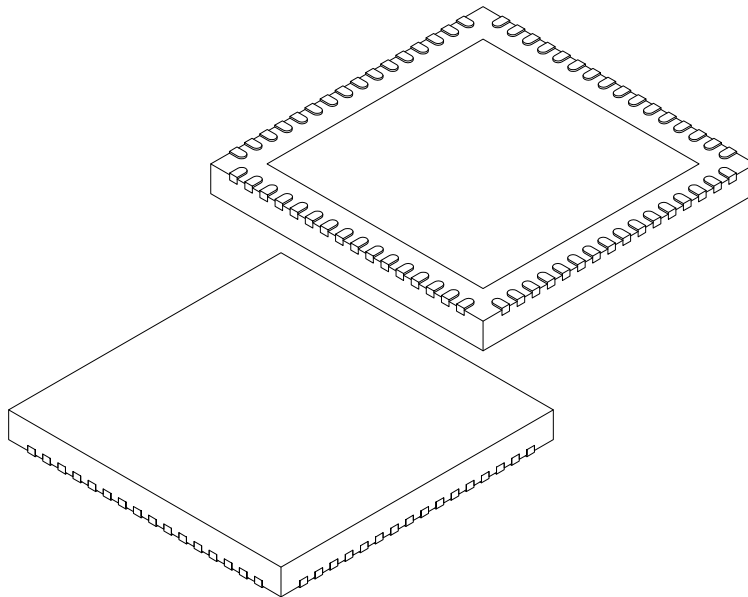


Microchip Technology Drawing C04-149D [R4X] Sheet 1 of 2

HV2621/HV2721/HV2722

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN] With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	7.05	7.15	7.25
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	7.05	7.15	7.25
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

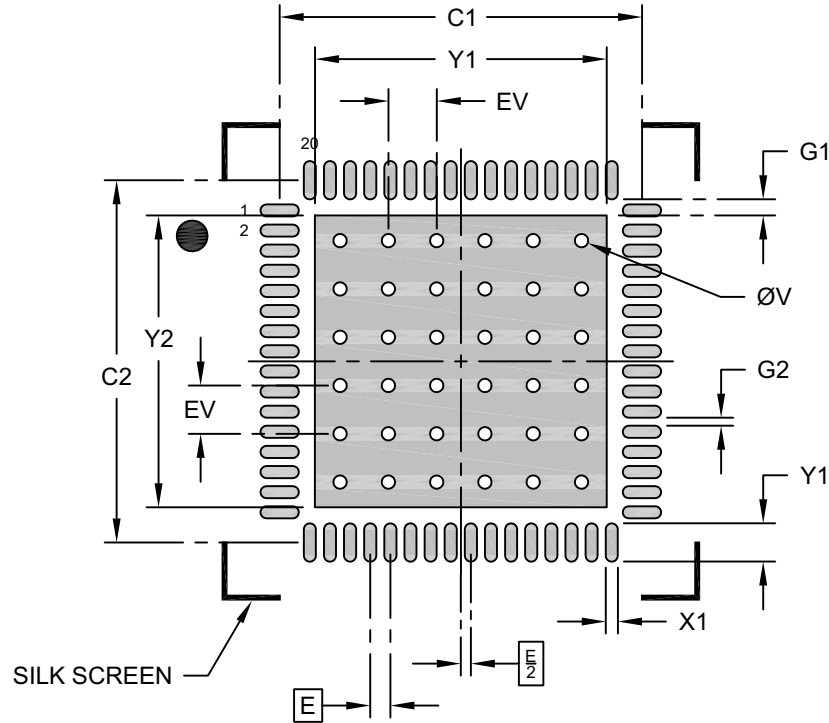
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149D [R4X] Sheet 2 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN] With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			7.25
Optional Center Pad Length	Y2			7.25
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.95
Contact Pad to Center Pad (X64)	G1	0.40		
Spacing Between Contact Pads (X60)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-149C [R4X]

HV2621/HV2721/HV2722

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2019)

- Original release of this document

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>/XX</u>	Examples: a) HV2621/R4X: 16-Channel High-Voltage Analog Switch, 64-lead QFN
Device	Package	
Device: HV2621: 300V, Low-Charge Injection 16-Channel High-Voltage Analog Switch HV2721: 300V, Low-Charge Injection 16-Channel High-Voltage Analog Switch with Bleed Resistor at Both Sides of Switch HV2722: 300V, Low-Charge Injection 16-Channel High-Voltage Analog Switch with Bleed Resistor at One Side of Switch		
Package:	R4X= Very Thin Plastic Quad Flat Pack, No Lead Package – 9x9x0.9 mm Body, 64-Lead (QFN)	

HV2621/HV2721/HV2722

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTrackr, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-5019-1

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Microchip:](#)

[HV2721/R4X](#) [HV2621/R4X](#)