MCP33131D/21D/11D-XX

1 Msps/500 kSPS 16/14/12-Bit Differential Input SAR ADC

Features

- Sample Rate (Throughput):
  - MCP33131D/21D/11D-10: 1 Msps
  - MCP33131D/21D/11D-05: 500 kSPS
- 16/14/12-Bit Resolution with No Missing Codes
- No Latency Output
- Wide Operating Voltage Range:
  - Analog Supply Voltage (AV_{DD}): 1.8V
  - Digital Input/Output Interface Voltage (DV_{IO}): 1.7V - 5.5V
  - External Reference (V_{REF}): 2.5V - 5.1V
- Differential Input Operation
  - Input Full-Scale Range: $-V_{REF}$ to $+V_{REF}$
- Ultra Low Current Consumption (typical):
  - During Input Acquisition (Standby): ~ 0.8 µA
  - During Conversion:

    MCP33131D/21D/11D-10: ~1.6 mA

    MCP33131D/21D/11D-05: ~1.4 mA
- SPI-Compatible Serial Communication:
  - SCLK Clock Rate: up to 100 MHz
- ADC Self-Calibration for Offset, Gain, and Linearity Errors:
  - During Power-Up (automatic)
  - On-Demand via user's command during normal operation
- AEC-Q100 Qualified:
  - Temperature Grade 1: -40°C to +125°C
- Package Options: MSOP-10 and TDFN-10

Typical Applications

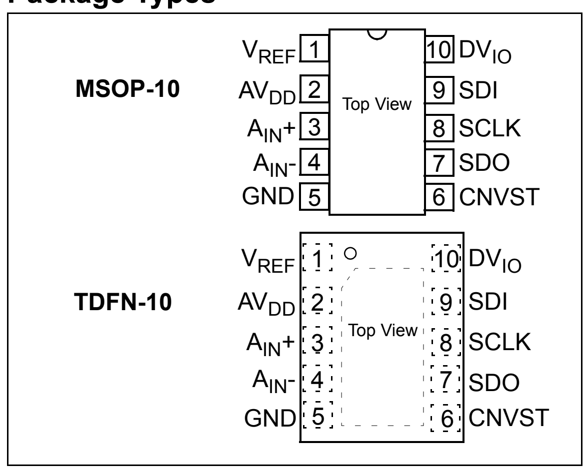
- High-Precision Data Acquisition
- Medical Instruments
- Test Equipment
- Electric Vehicle Battery Management Systems
- Motor Control Applications
- Switch-Mode Power Supply Applications
- Battery-Powered Equipment

System Design Supports

The MCP331x1D-XX Evaluation Kit demonstrates the performance of the MCP331x1D-XX SAR ADC family devices. The evaluation kit includes: (a) MCP331x1D Evaluation Board, (b) PIC32MZ EF Curiosity Board for data collection, and (c) SAR ADC Utility PC GUI.

Contact Microchip Technology Inc. for the evaluation tools and the PIC32 MCU firmware example codes.

Package Types

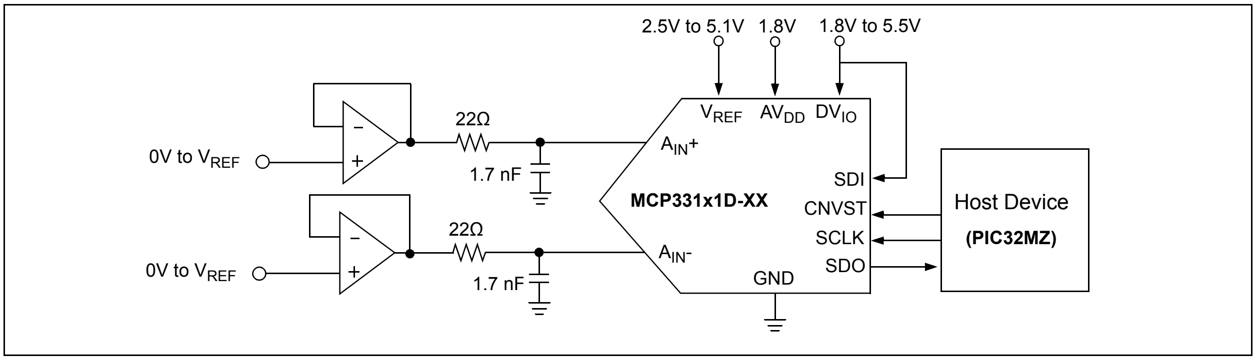


MCP331x1D-XX Device Offering (Note 1):

Part Number	Resolution	Sample Rate	Input Type	Input Range (Differential)	Performance (Typical)				
					SNR (dBFS)	SFDR (dB)	THD (dB)	INL (LSB)	DNL (LSB)
MCP33131D-10	16-bit	1 Msps	Differential	±5.1V	91.3	103.5	-99.3	±2	±0.8
MCP33121D-10	14-bit	1 Msps	Differential	±5.1V	85.1	103.5	-99.2	±0.5	±0.25
MCP33111D-10	12-bit	1 Msps	Differential	±5.1V	73.9	99.3	-96.7	±0.12	±0.06
MCP33131D-05	16-bit	500 kSPS	Differential	±5.1V	91.3	103.5	-99.3	±2	±0.8
MCP33121D-05	14-bit	500 kSPS	Differential	±5.1V	85.1	103.5	-99.2	±0.5	±0.25
MCP33111D-05	12-bit	500 kSPS	Differential	±5.1V	73.9	99.3	-96.7	±0.12	±0.06

Note 1: SNR, SFDR, and THD are measured with f_{IN} = 10 kHz, V_{IN} = -1 dBFS, V_{REF} = 5.1V.

Application Diagram



Description

The MCP33131D/MCP33121D/MCP33111D-10 and MCP33131D/MCP33121D/MCP33111D-05 are fully-differential 16, 14, and 12-bit, single-channel 1 Msps and 500 kSPS ADC family devices, respectively, featuring low power consumption and high performance, using a successive approximation register (SAR) architecture.

The device operates with a 2.5V to 5.1V external reference (V_{REF}), which supports a wide range of input full-scale range from $-V_{REF}$ to $+V_{REF}$. The reference voltage setting is independent of the analog supply voltage (AV_{DD}) and is higher than AV_{DD}. The conversion output is available through an easy-to-use simple SPI- compatible 3-wire interface.

The device requires a 1.8V analog supply voltage (AV_{DD}) and a 1.7V to 5.5V digital I/O interface supply voltage (DV_{IO}). The wide digital I/O interface supply (DV_{IO}) range (1.7V – 5.5V) allows the device to interface with most host devices (Master) available in the current industry such as the PIC32 microcontrollers, without using external voltage level shifters.

When the device is first powered-up, it performs a self-calibration to minimize offset, gain and linearity errors. The device performance stays stable across the specified temperature range. However, when extreme changes in the operating environment, such as in the reference voltage, are made with respect to the initial conditions (e.g. the reference voltage was not fully settled during the initial power-up sequence), the user may send a recalibrate command anytime to initiate another self-calibration to restore optimum performance.

When the initial power-up sequence is completed, the device enters a low-current input acquisition mode, where sampling capacitors are connected to the input pins. This mode is called Standby.

During Standby, most of the internal analog circuitry is shutdown in order to reduce current consumption. Typically, the device consumes less than 1 µA during Standby. A new conversion is started on the rising edge of CNVST. When the conversion is complete and the host lowers CNVST, the output data is presented on SDO, and the device enters Standby to begin acquiring the next input sample. The user can clock out the ADC output data using the SPI-compatible serial clock during Standby.

The ADC system clock is generated by the internal on-chip clock, therefore the conversion is performed independent of the SPI serial clock (SCLK).

This device can be used for various high-speed and high-accuracy analog-to-digital data conversion applications, where design simplicity, low power, and no output latency are needed.

The device is AEC-Q100 qualified for automotive applications and operates over the extended temperature range of -40°C to +125°C. The available package options are Pb-free small 3 mm x 3 mm TDFN-10 and MSOP-10.

1.0 KEY ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

External Analog Supply Voltage (AV_{DD})............ -0.3V to 2.0V
External Digital Supply Voltage (DV_{IO}).............. -0.3V to 5.8V
External Reference Voltage (V_{REF})................... -0.3V to 5.8V
Analog Inputs w.r.t GND .... -0.3V to V_{REF}+0.3V
Current at Input Pins ....±2 mA
Current at Output and Supply Pins ....±250 mA
Storage Temperature ....-65°C to +150°C
Maximum Junction Temperature (T_J).........................+150°C
ESD protection on all pins .... ≤2kV HBM, ≤200V MM, ≤2kV CDM

†Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Electrical Specifications

TABLE 1-1: KEY ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF
- MCP331x1D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
- MCP331x1D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Requirements						
Analog Supply Voltage Range	AV_{DD}	1.7	1.8	1.9	V	**(Note 3)**
Digital Input/Output Interface Voltage Range	DV_{IO}	1.7	—	5.5	V	**(Note 3)**
Analog Supply Current at AV_{DD} pin: During Conversion During Standby	I_{DDAN} I_{DDAN_STBY}	— — —	1.6 1.4 0.8	2.4 2.0 —	mA mA µA	f_s = 1 Msps **(MCP331x1D-10)** f_s = 500 kSPS **(MCP331x1D-05)** During input acquisition (t_{ACQ})
Digital Supply Current At DV_{DD} pin: During Output Data Reading During Standby	I_{IO_DATA} I_{IO_STBY}	— — —	290 200 30	— — —	µA µA nA	f_s = 1 Msps **(MCP331x1D-10)** f_s = 500 kSPS **(MCP331x1D-05)** During input acquisition (t_{ACQ})
External Reference Voltage Input						
Reference Voltage **(Note 2)**, **(Note 3)**	V_{REF}	2.5 2.7		5.1 5.1	V	-40°C ≤ T_A ≤ 85°C 85°C < T_A ≤ 125°C
Reference Load Current at V_{REF} pin: During Conversion During Standby	I_{REF} I_{REF_STBY}	— —	450 220 240	600 360 —	µA µA nA	f_s = 1 Msps **(MCP331x1D-10)** f_s = 500 kSPS **(MCP331x1D-05)** During input acquisition (t_{ACQ})
Total Power Consumption (Including AV_{DD}, DV_{IO}, V_{REF} pins)						
MCP331x1D-10						
at 1 Msps at 500 kSPS at 100 kSPS During Standby	P_{DISS_TOTAL} P_{DISS_STBY}	— — — —	6.2 3.1 0.6 2.6	— — — —	mW mW mW µW	Averaged power for t_{ACQ} + t_{CNV} During input acquisition (t_{ACQ})
MCP331x1D-05						
at 500 kSPS at 100 kSPS During Standby	P_{DISS_TOTAL} P_{DISS_STBY}	— — —	4.2 0.8 2.6	— — —	mW mW µW	Averaged power for t_{ACQ} + t_{CNV} During input acquisition (t_{ACQ})

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: Differential Input Full-Scale Range (FSR) = 2 x V_{REF}
5: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
6: ENOB = (SINAD - 1.76)/6.02

TABLE 1-1: KEY ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF

- MCP331x1D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
- MCP331x1D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Analog Inputs						
Input Voltage Range **(Note 2)**	V_{IN+}	-0.1	—	V_{REF}+0.1	V	Differential Input: $V_{IN} = (V_{IN+} - V_{IN-})$
	V_{IN-}	-0.1	—	V_{REF}+0.1	V	
Input Full-Scale Voltage Range	FSR	$-V_{REF}$	—	$+V_{REF}$	V_{PP}	Differential Input **(Note 2)**, **(Note 4)**
Input Common-Mode Voltage Range	V_{CM}	0	$V_{REF}/2$	V_{REF}		**(Note 2)**
Input Sampling Capacitance	C_S	—	31	—	pF	**(Note 1)**
-3dB Input Bandwidth	BW_{-3dB}	—	25	—	MHz	**(Note 1)**
Aperture Delay **(Note 1)**		—	2.5	—	ns	Time delay between CNVST rising edge and when input is sampled
Leakage Current at Analog Input Pin	$I_{LEAK\_AN\_INPUT}$	—	±2	±200	nA	During input acquisition (t_{ACQ})
System Performance						
Sample Rate (Throughput rate)	f_s	—	—	1	Msps	MCP331x1D-10
		—	—	500	kSPS	MCP331x1D-05
Resolution (No Missing Codes)		16	—	—	Bits	MCP33131D-10 and MCP33131D-05
		14	—	—	Bits	MCP33121D-10 and MCP33121D-05
		12	—	—	Bits	MCP33111D-10 and MCP33111D-05
Integral Nonlinearity	INL	-6	±2	+6	LSB	MCP33131D-10 and MCP33131D-05
		-1.5	±0.5	+1.5	LSB	MCP33121D-10 and MCP33121D-05
			±0.12		LSB	MCP33111D-10 and MCP33111D-05
Differential Nonlinearity	DNL	-0.98	±0.8	+1.8	LSB	MCP33131D-10 and MCP33131D-05
		-0.8	±0.25	+0.8	LSB	MCP33121D-10 and MCP33121D-05
		-0.3	±0.06	+0.3	LSB	MCP33111D-10 and MCP33111D-05
Offset Error			±0.1	±2.3	mV	MCP33131D-10 and MCP33131D-05
		—	±0.125	±3	mV	MCP33121D-10 and MCP33121D-05
		—	±0.8	±3.66	mV	MCP33111D-10 and MCP33111D-05
Offset Error Drift with Temperature		—	±0.8	—	µV/°C	
Gain Error	G_{ER}	—	±2	—	LSB	MCP33131D-10 and MCP33131D-05
		—	±0.5	—	LSB	MCP33121D-10 and MCP33121D-05
		—	±0.1	—	LSB	MCP33111D-10 and MCP33111D-05
Gain Error Drift with temperature		—	±0.35	—	µV/°C	
Input common-mode rejection ratio	CMRR	—	84	—	dB	
Power Supply Rejection Ratio	PSRR	—	70	—	dB	**(Note 5)**

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: Differential Input Full-Scale Range (FSR) = 2 x V_{REF}
5: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
6: ENOB = (SINAD - 1.76)/6.02

TABLE 1-1: KEY ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF

- MCP331x1D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
- MCP331x1D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dynamic Performance						
Signal-to-Noise Ratio	SNR	**MCP33131D-10 and MCP33131D-05: 16-bit ADC**				
		—	91.6	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	86.6	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		88.7	91.3	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	86.6	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33121D-10 and MCP33121D-05: 14-bit ADC				
		—	85.2	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	83.5	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		81.7	85.1	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	83.5	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33111D-10 and MCP33111D-05: 12-bit ADC				
		—	73.9	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	73.8	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		71.1	73.9	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	73.8	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
Signal-to-Noise and Distortion Ratio **(Note 6)**	SINAD	**MCP33131D-10 and MCP33131D-05: 16-bit ADC**				
		—	91.5	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	86.6	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	91	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	86.2	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33121D-10 and MCP33121D-05: 14-bit ADC				
		—	85.2	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	83.5	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	85	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	83.3	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33111D-10 and MCP33111D-05: 12-bit ADC				
		—	73.9	—	dBFS	V_{REF} = 5V, f_{IN} = 1 kHz
		—	73.8	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	73.9	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	73.8	—		V_{REF} = 2.5V, f_{IN} = 10 kHz

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: Differential Input Full-Scale Range (FSR) = 2 x V_{REF}
5: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
6: ENOB = (SINAD - 1.76)/6.02

TABLE 1-1: KEY ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF
- MCP331x1D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
- MCP331x1D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Spurious Free Dynamic Range	SFDR	**MCP33131D-10 and MCP33131D-05: 16-bit ADC**				
		—	103.7	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	98	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	103.5	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	97.5	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33121D-10 and MCP33121D-05: 14-bit ADC				
		—	103.6	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	98	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	103.5	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	97.4	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33111D-10 and MCP33111D-05: 12-bit ADC				
		—	99.3	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	97.7	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	99.3	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	97.2	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
Total Harmonic Distortion (first five harmonics)	THD	**MCP33131D-10 and MCP33131D-05: 16-bit ADC**				
		—	-100.4	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	-95.4	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	-99.3	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	-95.4	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33121D-10 and MCP33121D-05: 14-bit ADC				
		—	-100.1	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	-95.3	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	-99.2	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	-95.3	—		V_{REF} = 2.5V, f_{IN} = 10 kHz
		MCP33111D-10 and MCP33111D-05: 12-bit ADC				
		—	-97.5	—	dBc	V_{REF} = 5V, f_{IN} = 1 kHz
		—	-94.4	—		V_{REF} = 2.5V, f_{IN} = 1 kHz
		—	-96.7	—		V_{REF} = 5V, f_{IN} = 10 kHz
		—	-94.4	—		V_{REF} = 2.5V, f_{IN} = 10 kHz

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: Differential Input Full-Scale Range (FSR) = 2 x V_{REF}
5: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
6: ENOB = (SINAD - 1.76)/6.02

TABLE 1-1: KEY ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF
- MCP331x1D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
- MCP331x1D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
System Self-Calibration						
Self-Calibration Time	t_{CAL}	—	500	650	ms	(Note 2)
Number of SCLK Clocks for Recalibrate Command	$ReCal_{NSCLK}$	—	1024	—	clocks	Includes clocks for data bits
Serial Interface Timing Information: See Table 1-2						
Digital Inputs/Outputs						
High-level Input voltage	V_{IH}	0.7 * DV_{IO}	—	DV_{IO} + 0.3	V	DV_{IO} ≥ 2.3V
		0.9 * DV_{IO}	—	DV_{IO} + 0.3	V	DV_{IO} < 2.3V
Low-level input voltage	V_{IL}	-0.3	—	0.3 * DV_{IO}	V	DV_{IO} ≥ 2.3V
		-0.3	—	0.2 * DV_{IO}	V	DV_{IO} < 2.3V
Hysteresis of Schmitt Trigger Inputs	V_{HYST}	—	0.2 * DV_{IO}	—	V	All digital inputs
Low-level output voltage	V_{OL}	—	—	0.2 * DV_{IO}	V	I_{OL} = 500 µA (sink)
High-level output voltage	V_{OH}	0.8 * DV_{IO}	—	—	V	I_{OL} = - 500 µA (source)
Input leakage current	I_{LI}	—	—	±1	µA	CNVST/SDI/SCLK = GND or DV_{IO}
Output leakage current	I_{LO}	—	—	±1	µA	Output is high-Z, SDO = GND or DV_{IO}
Internal capacitance (all digital inputs and outputs)	C_{INT}	—	7	—	pF	T_A = 25°C (Note 1)

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: Decoupling capacitor is recommended on the following pins:
(a) AV_{DD} pin: 1 µF ceramic capacitor, (b) DV_{IO} pin: 0.1 µF ceramic capacitor, (c) V_{REF} pin: 10 µF tantalum capacitor.
4: Differential Input Full-Scale Range (FSR) = 2 x V_{REF}
5: PSRR (dB) = -20 log (D_{VOUT}/AV_{DD}), where D_{VOUT} = change in conversion result.
6: ENOB = (SINAD - 1.76)/6.02

TABLE 1-2: SERIAL INTERFACE TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS sine wave, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF. +25°C is applied for typical value. All timings are measured at 50%. See Figure 1-1 for timing diagram.

- MCP331x1D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
- MCP331x1D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

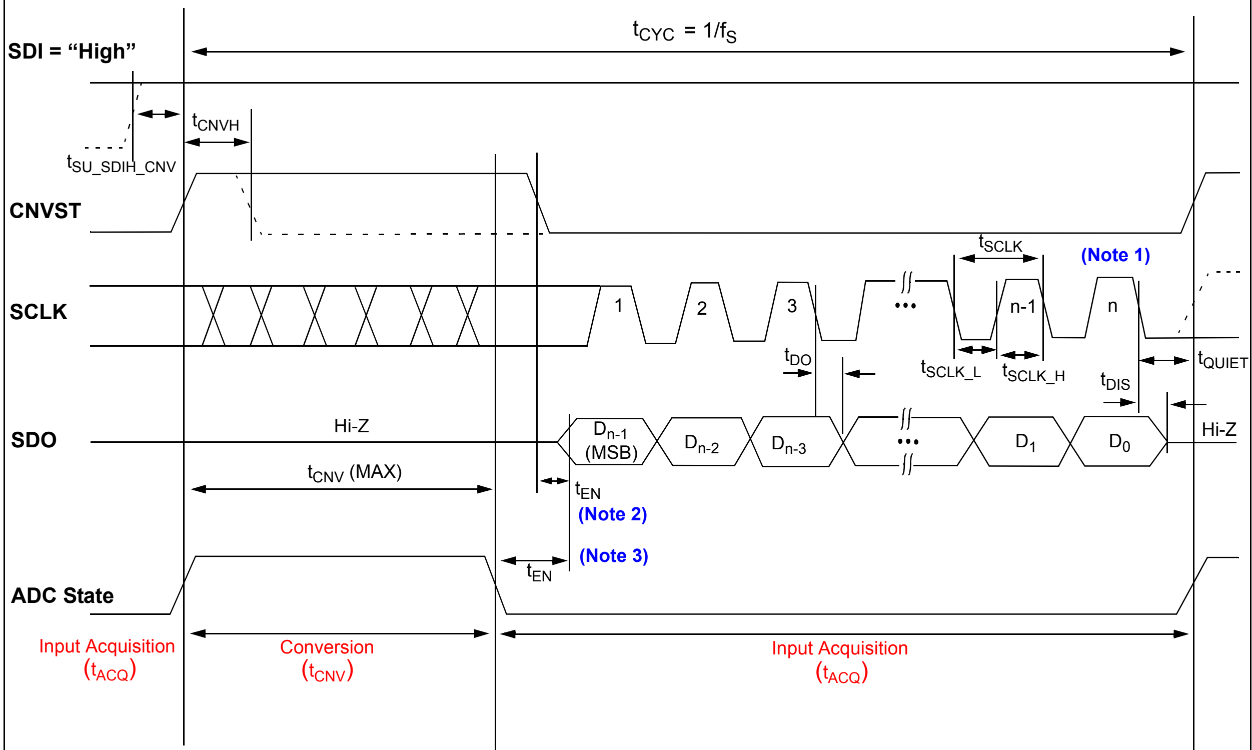
Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Serial Clock frequency	f_{SCLK}	—	—	100	MHz	See t_{SCLK} specification
SCLK Period	t_{SCLK}	10	—	—	ns	DV_{IO} ≥ 3.3V, f_{SCLK} = 100 MHz (Max)
		12	—	—	ns	DV_{IO} ≥ 2.3V, f_{SCLK} = 83.3 MHz (Max)
		16	—	—	ns	DV_{IO} ≥ 1.7V, f_{SCLK} = 62.5 MHz (Max)
SCLK Low Time	t_{SCLK_L}	3	—	—	ns	DV_{IO} ≥ 2.3V
		4.5	—	—	ns	DV_{IO} ≥ 1.7V
SCLK High Time	t_{SCLK_H}	3	—	—	ns	DV_{IO} ≥ 2.3V
		4.5	—	—	ns	DV_{IO} ≥ 1.7V
Output Valid from SCLK Low	t_{DO}	—	—	9.5	ns	DV_{IO} ≥ 3.3V
		—	—	12	ns	DV_{IO} ≥ 2.3V
		—	—	16	ns	DV_{IO} ≥ 1.7V
Quiet time	t_{QUIET}	10	—	—	ns	(Note 2)
3-Wire Operation:						
SDI Valid Setup time	$t_{SU\_SDIH\_CNV}$	5	—	—	ns	SDI High to CNVST Rising Edge
CNVST Pulse Width High Time	t_{CNVH}	10	—	—	ns	
Output Enable Time	t_{EN}	—	—	10	ns	DV_{IO} ≥ 2.3V
		—	—	15	ns	DV_{IO} ≥ 1.7V
Output Disable Time	t_{DIS}	—	—	15	ns	(Note 2)
MCP331x1D-10						
Sample Rate	f_s	—	—	1	Msps	Throughput rate
Input Acquisition Time (Note 2)	t_{ACQ}	290 250	300	— —	ns	-40°C ≤ T_A ≤ 85°C 85°C < T_A ≤ 125°C
Data Conversion Time	t_{CNV}	— —	700	710 750	ns	-40°C ≤ T_A ≤ 85°C 85°C < T_A ≤ 125°C
Time between Conversions	t_{CYC}	1	—	—	µs	t_{CYC} = t_{ACQ} + t_{CNV}, f_S = 1 Msps
MCP331x1D-05						
Sample Rate	f_s	—	—	500	kSPS	Throughput rate
Input Acquisition Time (Note 2)	t_{ACQ}	700	800	—	ns	-40°C ≤ T_A ≤ 125°C
Data Conversion Time	t_{CNV}	—	1200	1300	ns	-40°C ≤ T_A ≤ 125°C
Time between Conversions	t_{CYC}	2	—	—	µs	t_{CYC} = t_{ACQ} + t_{CNV}, f_S = 500 kSPS

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.

TABLE 1-3: TEMPERATURE CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	(Note 1)
Storage Temperature Range	T_A	-65	—	+150	°C	(Note 1)
Thermal Package Resistance						
Thermal Resistance, MSOP-10	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, TDFN-10	θ_{JA}	—	68	—	°C/W	

Note 1: The internal junction temperature (T_j) must not exceed the absolute maximum specification of +150°C.



Note 1: n = 16 for 16-bit, 14 for 14-bit device, and 12 for 12-bit device.
2: t_{EN} when CNVST is lowered after t_{CNV} (MAX).
3: t_{EN} when CNVST is lowered before t_{CNV} (MAX).

FIGURE 1-1: *Interface Timing Diagram. CNVST is used as chip select. See Figure 7-2 for more details.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES FOR 16-BIT DEVICES (MCP33131D-XX)

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33131D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33131D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

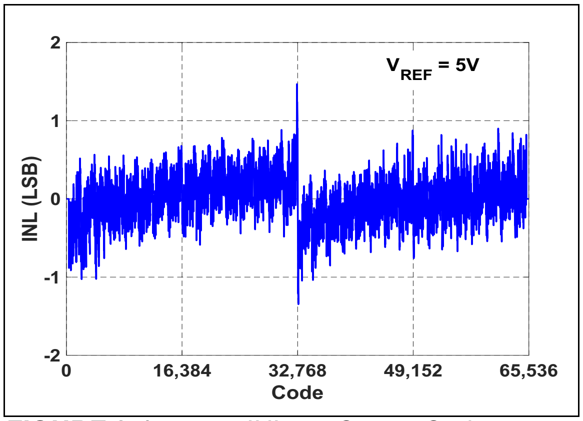


FIGURE 2-1: INL vs. Output Code.

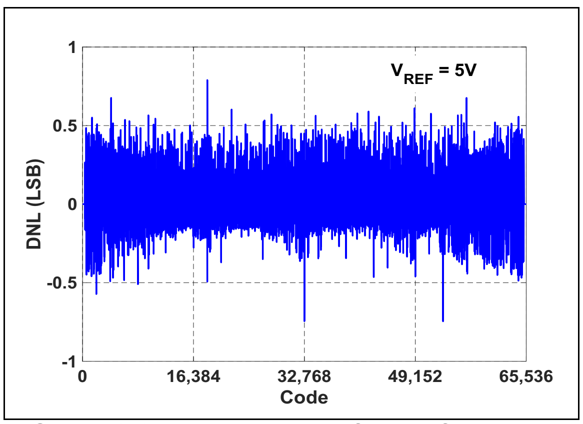


FIGURE 2-2: DNL vs. Output Code.

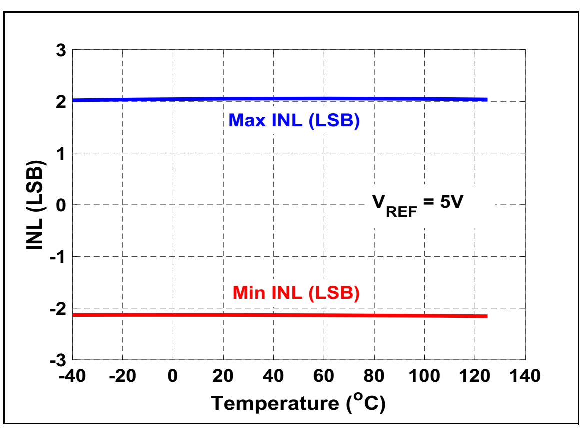


FIGURE 2-3: INL vs. Temperature.

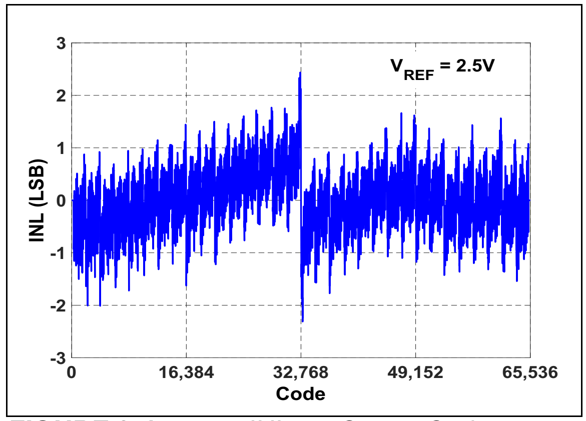


FIGURE 2-4: INL vs. Output Code.

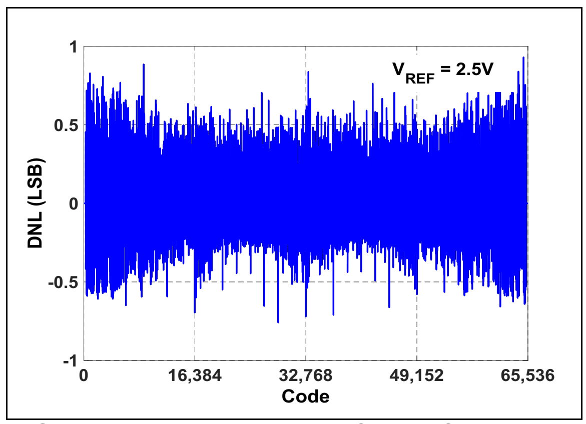


FIGURE 2-5: DNL vs. Output Code.

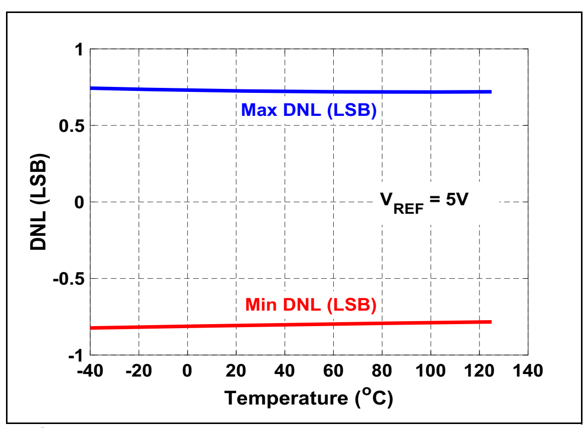


FIGURE 2-6: DNL vs. Temperature.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33131D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33131D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

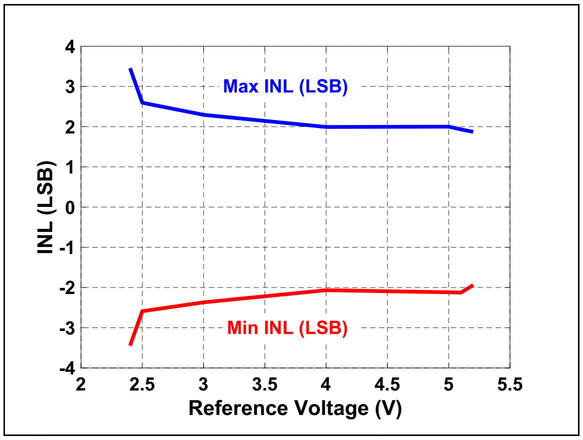


FIGURE 2-7: *INL vs. Reference Voltage.*

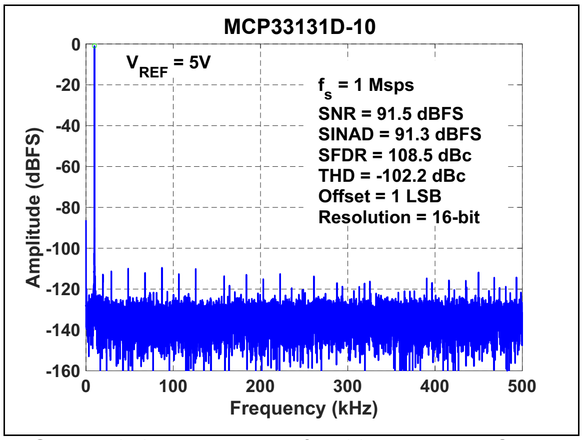


FIGURE 2-8: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 5V.*

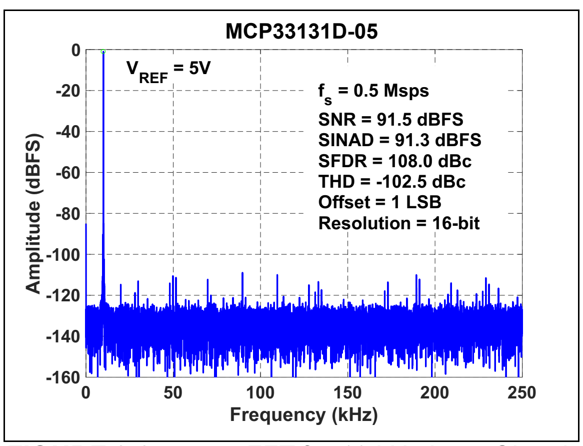


FIGURE 2-9: *FFT for 10 kHz Input Signal: f_S = 500 kSPS, V_{IN} = -1 dBFS, V_{REF} = 5V.*

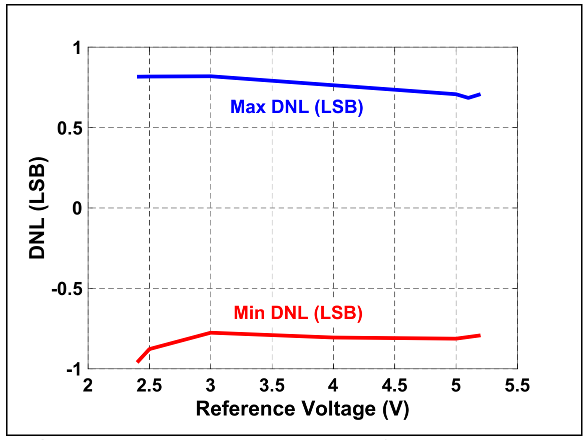


FIGURE 2-10: *DNL vs. Reference Voltage.*

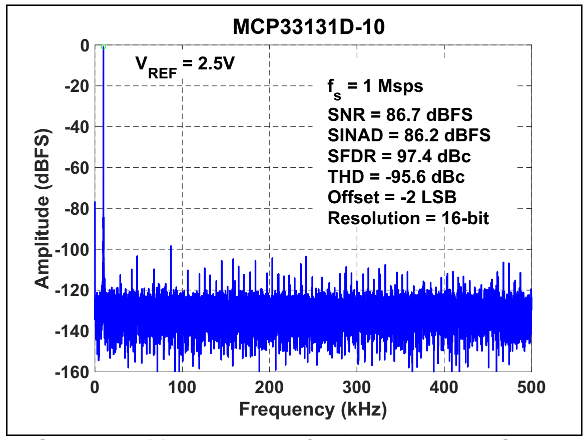


FIGURE 2-11: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 2.5V.*

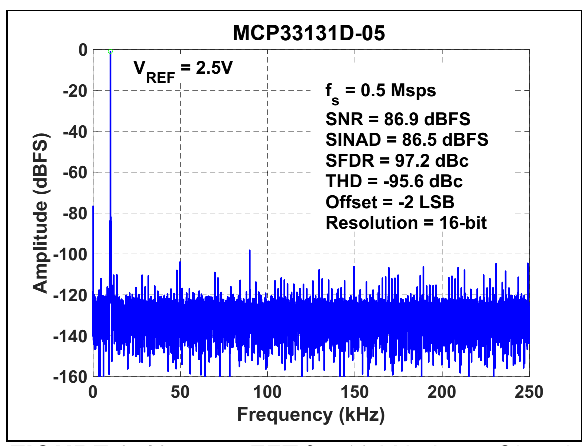


FIGURE 2-12: *FFT for 10 kHz Input Signal: f_S = 500 kSPS, V_{IN} = -1 dBFS, V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33131D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33131D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

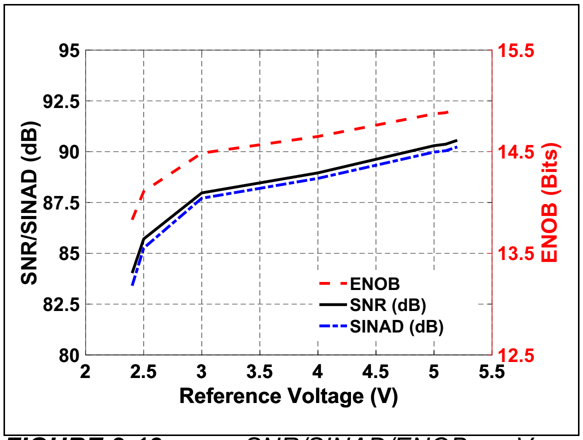


FIGURE 2-13: SNR/SINAD/ENOB vs. V_{REF}

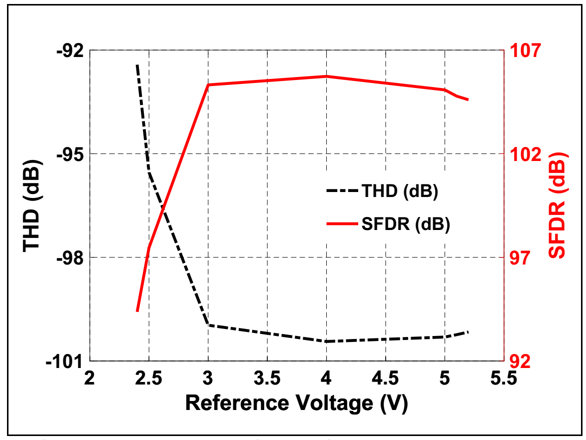


FIGURE 2-16: SFDR/THD vs. V_{REF}

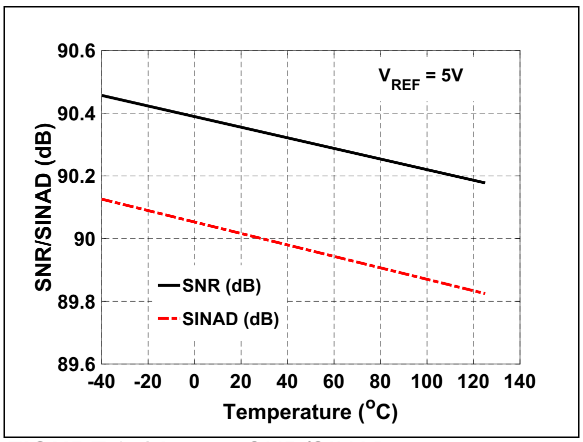


FIGURE 2-14: SNR/SINAD vs. Temperature: V_{REF} = 5V.

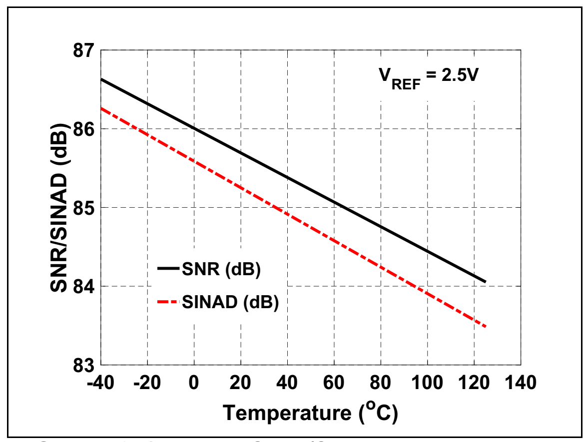


FIGURE 2-17: SNR/SINAD vs. Temperature: V_{REF} = 2.5V.

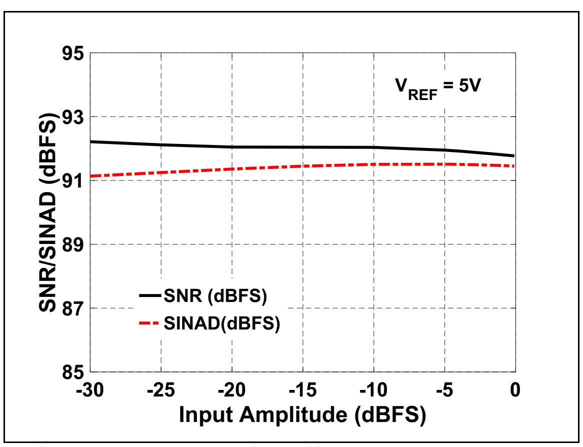


FIGURE 2-15: SNR/SINAD vs. Input Amplitude: F_{IN} = 10 kHz.

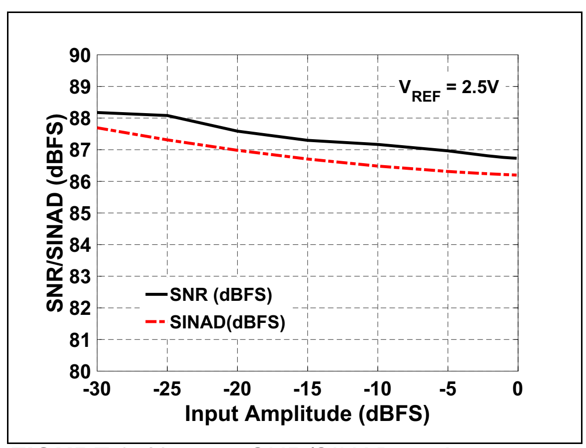


FIGURE 2-18: SNR/SINAD vs. Input Amplitude: F_{IN} = 10 kHz.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33131D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33131D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

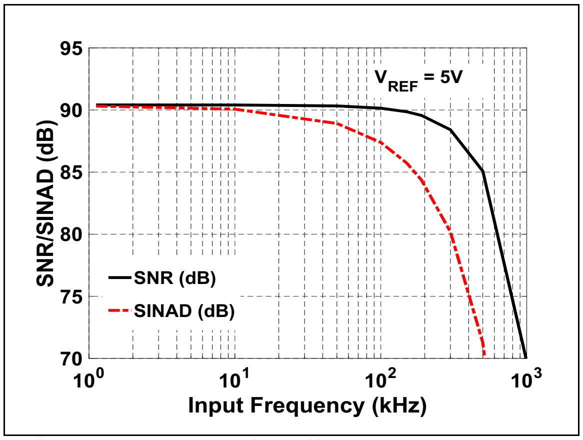


FIGURE 2-19: *SNR/SINAD vs.Input Frequency: V_{IN} = -1 dBFS.*

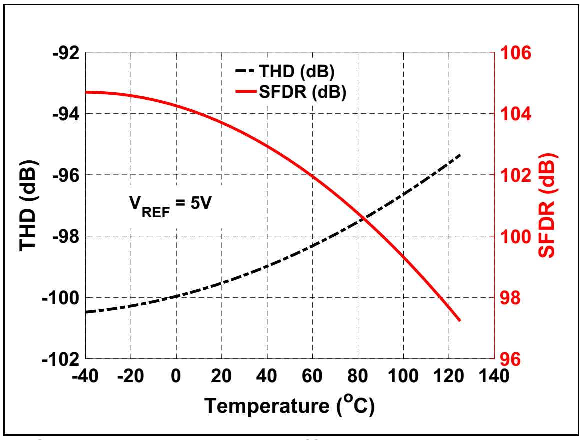


FIGURE 2-20: *THD/SFDR vs. Temperature: V_{REF} = 5V.*

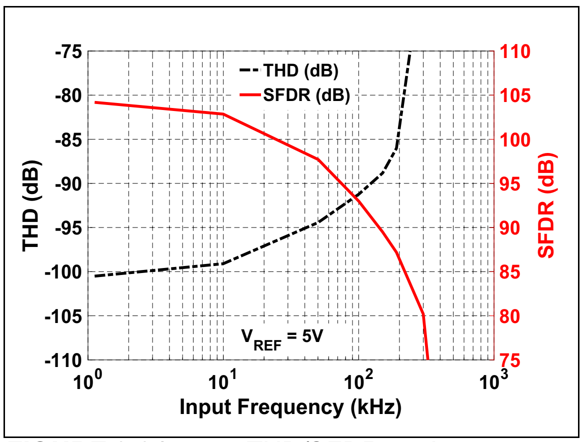


FIGURE 2-21: *THD/SFDR vs. Input Frequency: V_{REF} = 5V.*

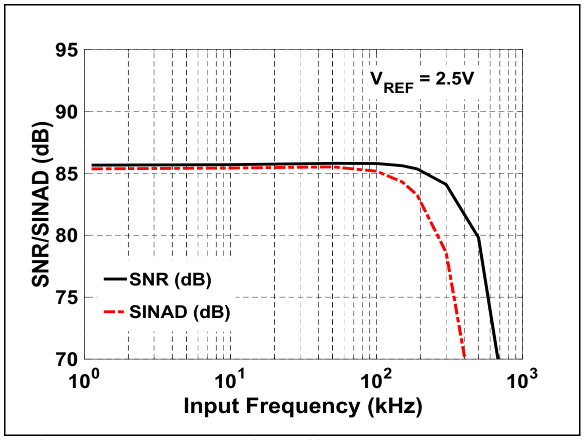


FIGURE 2-22: *SNR/SINAD vs.Input Frequency: V_{IN} = -1 dBFS.*

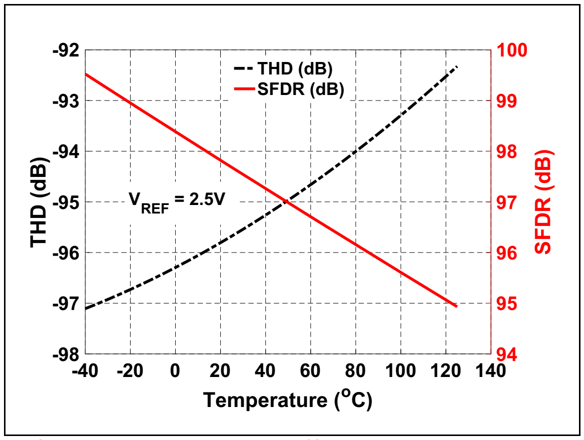


FIGURE 2-23: *THD/SFDR vs. Temperature: V_{REF} = 2.5V.*

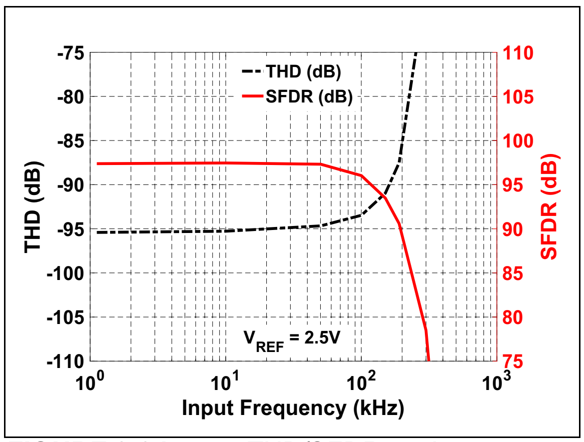


FIGURE 2-24: *THD/SFDR vs. Input Frequency: V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (V_{IN}) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33131D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33131D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

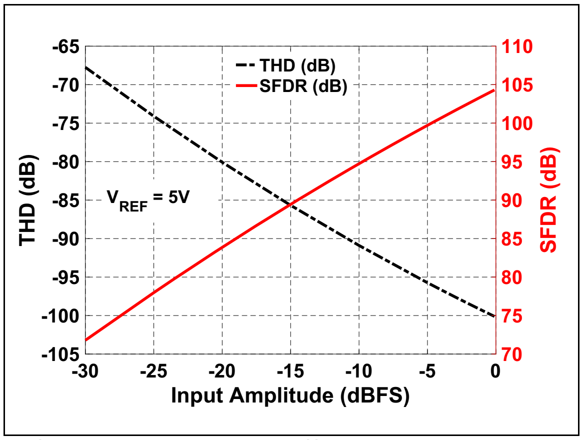


FIGURE 2-25: *THD/SFDR vs. Input Amplitude: V_{REF} = 5V.*

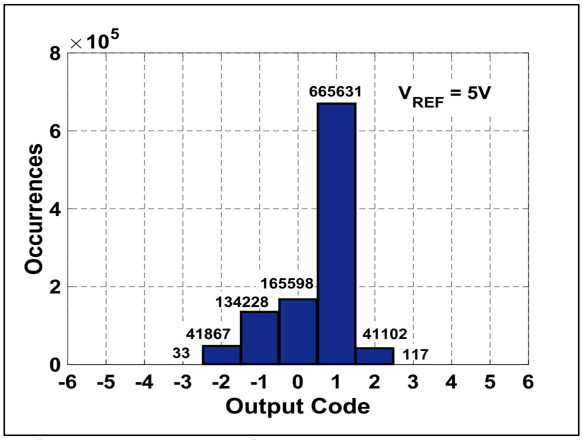


FIGURE 2-26: *Shorted Input Histogram: V_{REF} = 5V.*

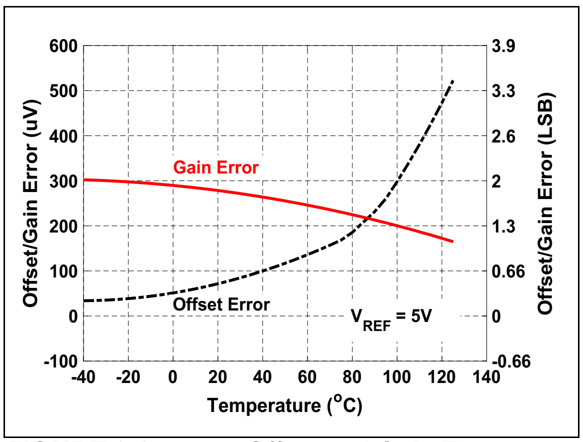


FIGURE 2-27: *Offset and Gain Error vs. Temperature: V_{REF} = 5V.*

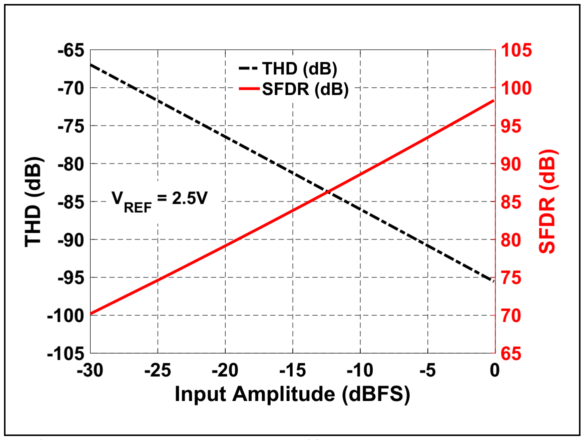


FIGURE 2-28: *THD/SFDR vs. Input Amplitude: V_{REF} = 2.5V.*

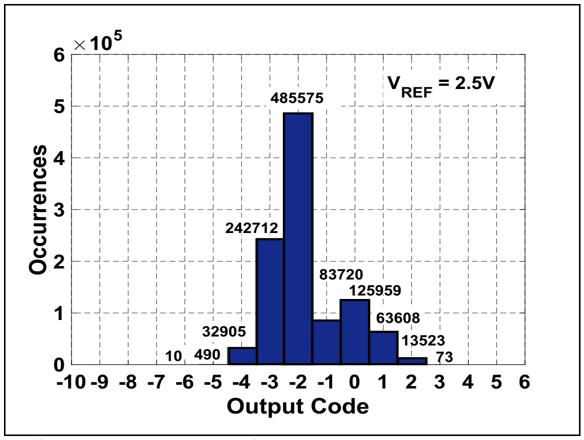


FIGURE 2-29: *Shorted Input Histogram: V_{REF} = 2.5V.*

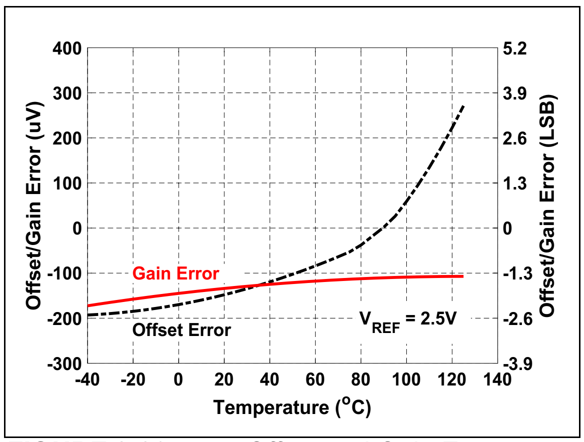


FIGURE 2-30: *Offset and Gain Error vs. Temperature: V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33131D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33131D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

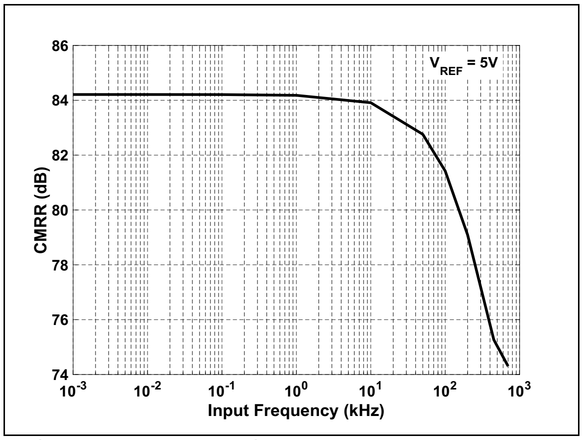


FIGURE 2-31: *CMRR vs. Input Frequency: V_{REF} = 5V.*

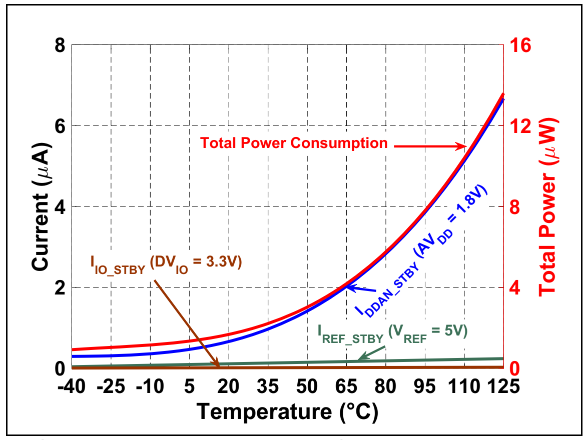


FIGURE 2-34: *Power Consumption vs. Temperature during Shutdown.*

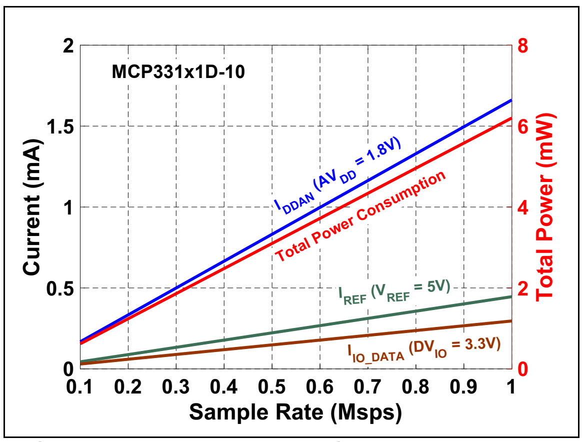


FIGURE 2-32: *Power Consumption vs. Sample Rate: C_{LOAD_SDO} = 20 pF.*

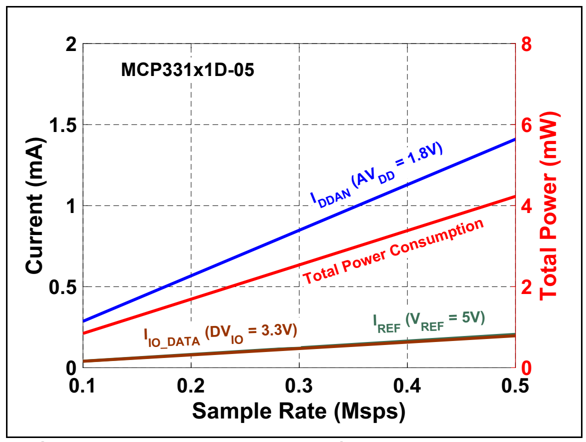


FIGURE 2-35: *Power Consumption vs. Sample Rate: C_{LOAD_SDO} = 20 pF.*

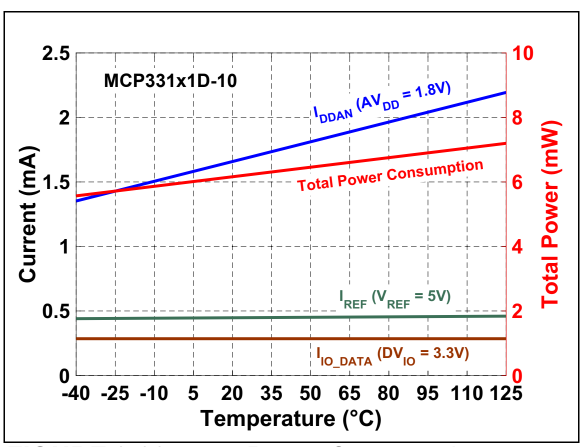


FIGURE 2-33: *Power Consumption vs. Temperature: C_{LOAD_SDO} = 20 pF.*

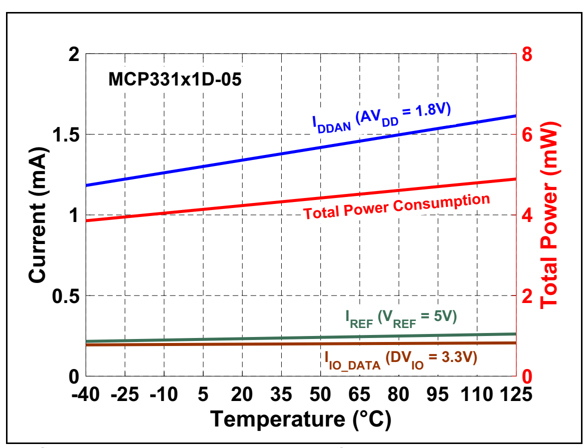


FIGURE 2-36: *Power Consumption vs. Temperature: C_{LOAD_SDO} = 20 pF.*

3.0 TYPICAL PERFORMANCE CURVES FOR 14-BIT DEVICES (MCP33121D-XX)

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33121D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33121D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

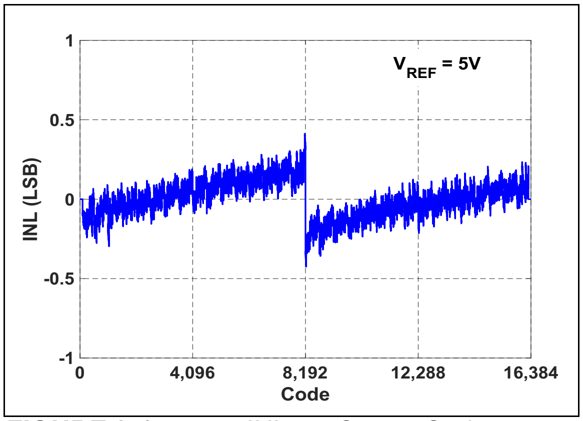


FIGURE 3-1: INL vs. Output Code.

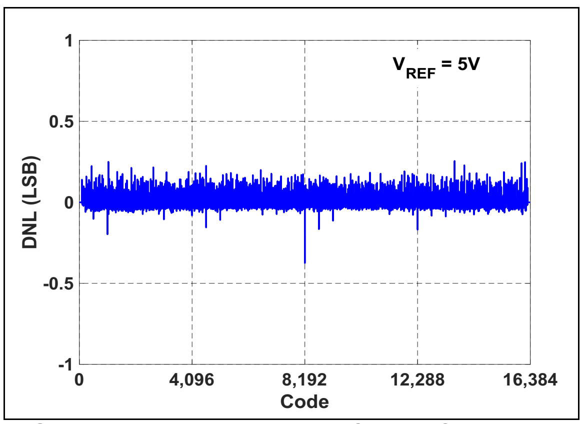


FIGURE 3-2: DNL vs. Output Code.

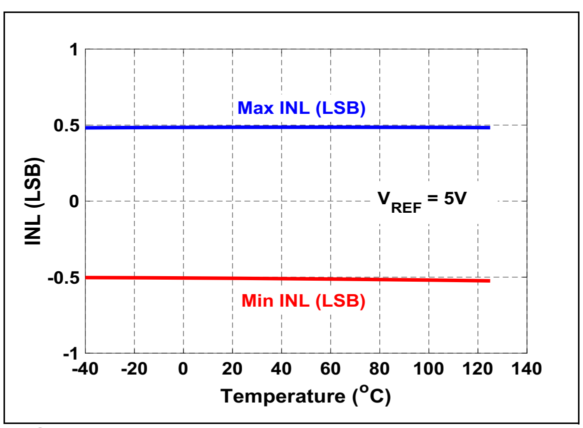


FIGURE 3-3: INL vs. Temperature.

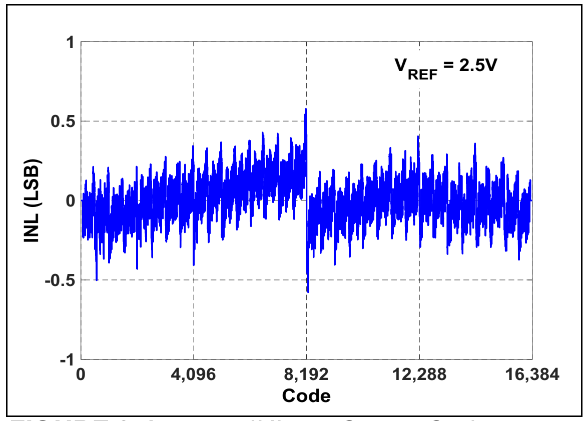


FIGURE 3-4: INL vs. Output Code.

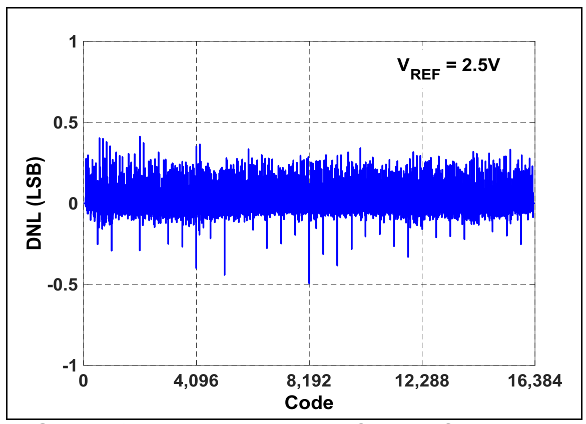


FIGURE 3-5: DNL vs. Output Code.

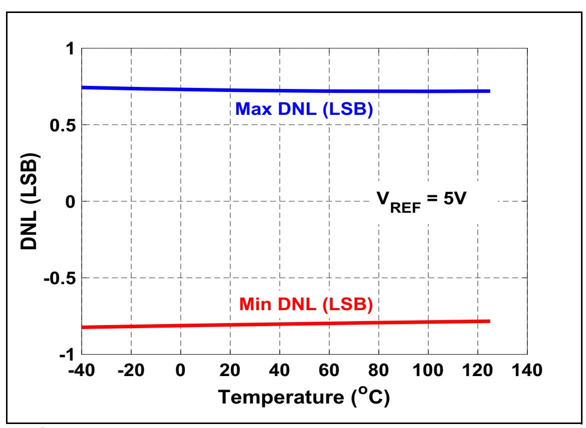


FIGURE 3-6: DNL vs. Temperature.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33121D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33121D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

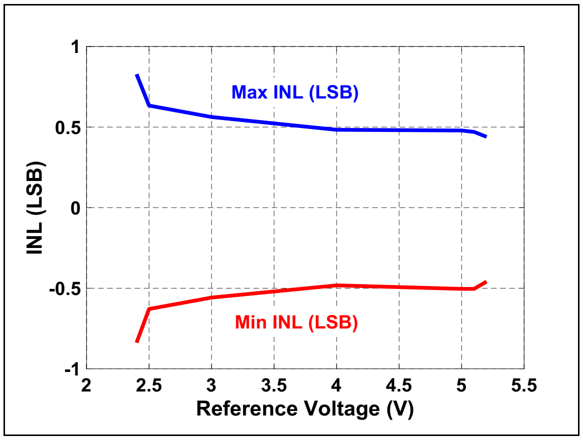


FIGURE 3-7: *INL vs. Reference Voltage.*

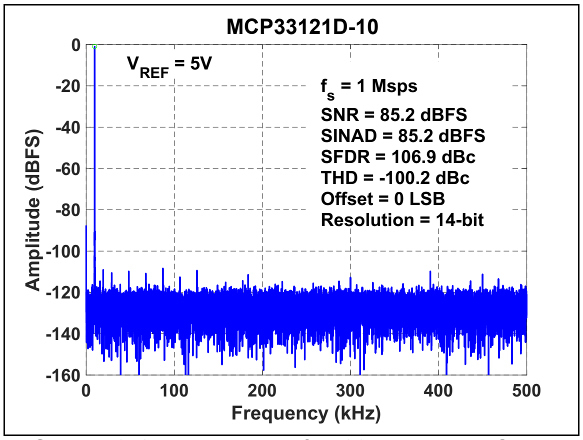


FIGURE 3-8: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 5V.*

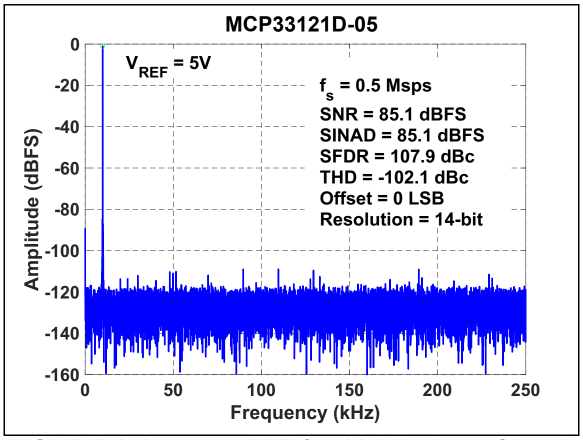


FIGURE 3-9: *FFT for 10 kHz Input Signal: f_S = 500 kSPS, V_{IN} = -1 dBFS, V_{REF} = 5V.*

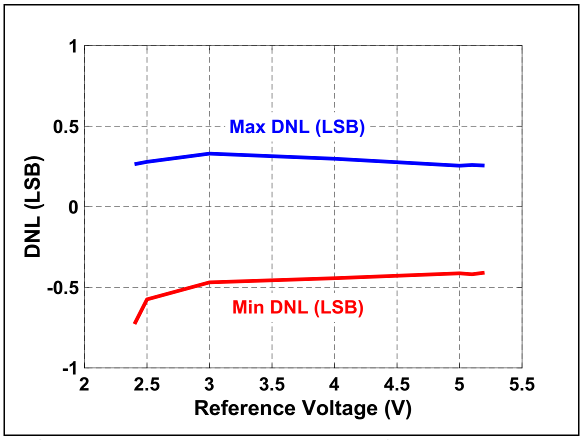


FIGURE 3-10: *DNL vs. Reference Voltage.*

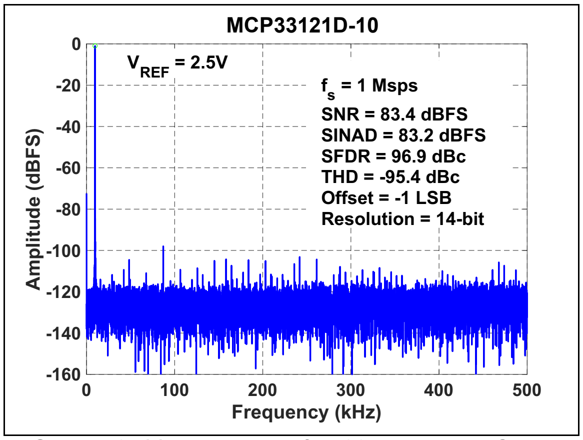


FIGURE 3-11: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 2.5V.*

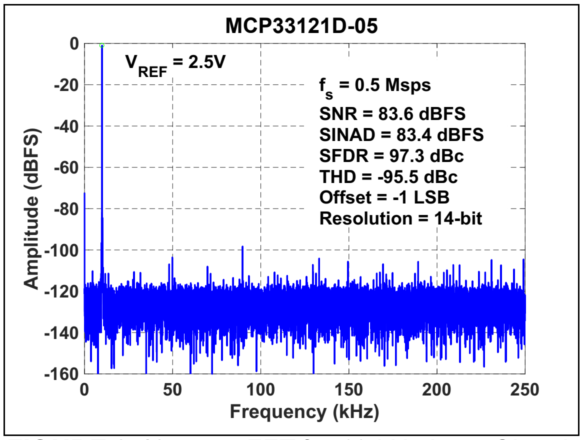


FIGURE 3-12: *FFT for 10 kHz Input Signal: f_S = 500 kSPS, V_{IN} = -1 dBFS, V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33121D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33121D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

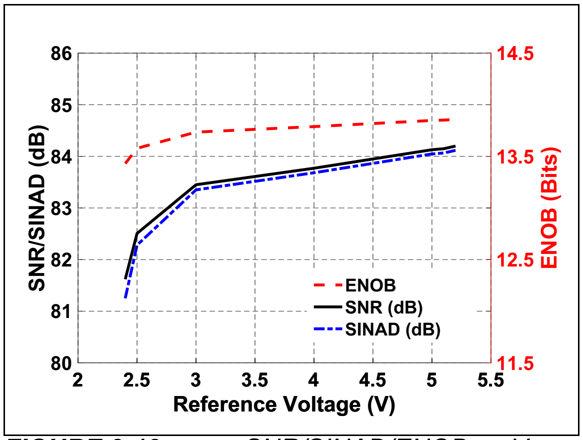


FIGURE 3-13: *SNR/SINAD/ENOB vs. V_{REF}*

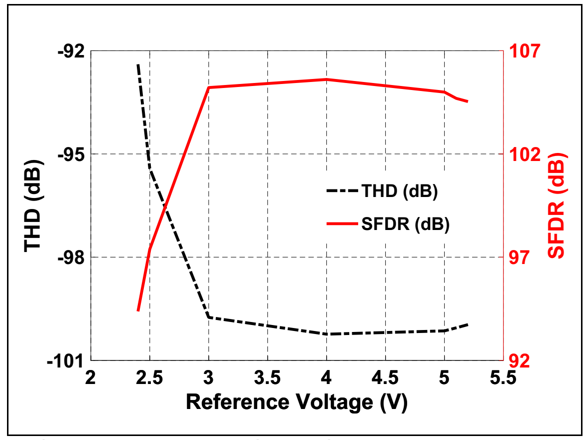


FIGURE 3-16: *SFDR/THD vs. V_{REF}*

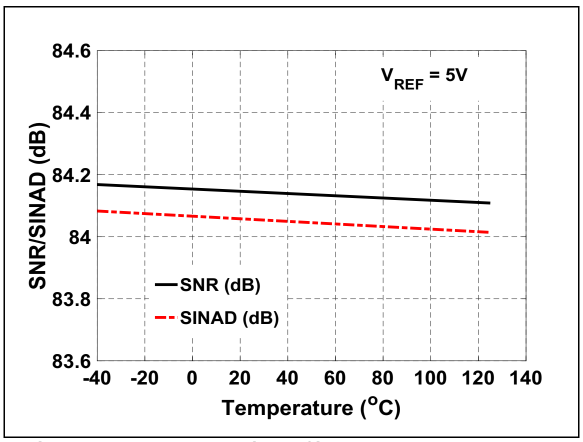


FIGURE 3-14: *SNR/SINAD vs. Temperature: V_{REF} = 5V.*

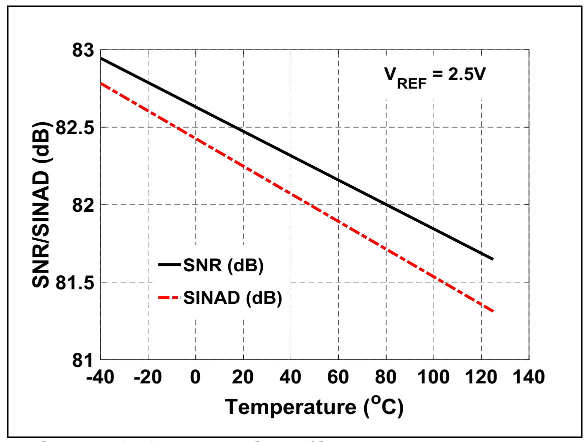


FIGURE 3-17: *SNR/SINAD vs. Temperature: V_{REF} = 2.5V.*

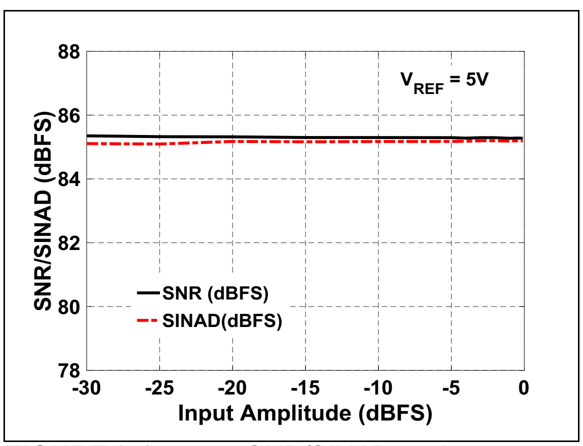


FIGURE 3-15: *SNR/SINAD vs. Input Amplitude: F_{IN} = 10 kHz.*

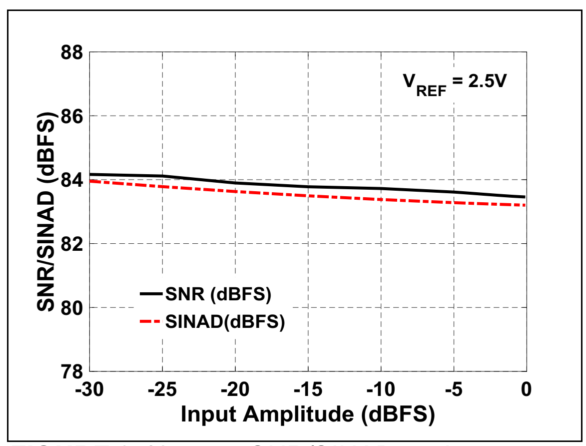


FIGURE 3-18: *SNR/SINAD vs. Input Amplitude: F_{IN} = 10 kHz.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33121D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33121D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

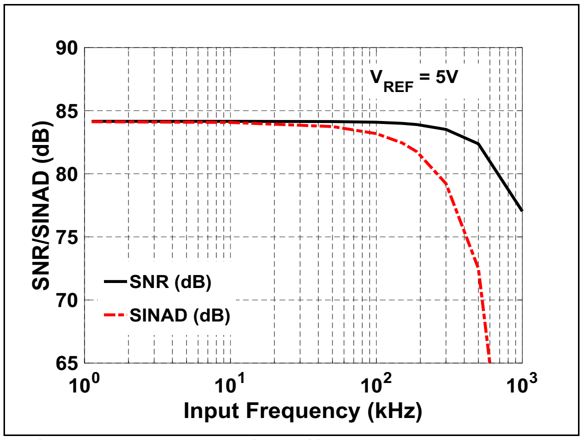


FIGURE 3-19: SNR/SINAD vs.Input Frequency: V_{IN} = -1 dBFS.

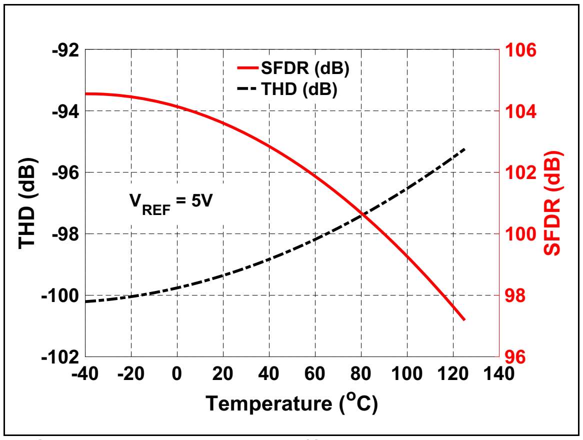


FIGURE 3-20: THD/SFDR vs. Temperature: V_{REF} = 5V.

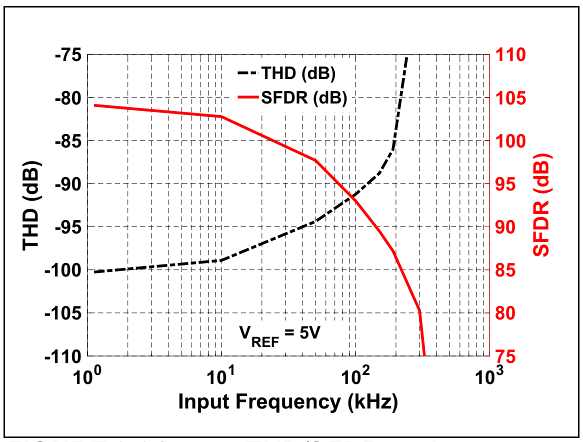


FIGURE 3-21: THD/SFDR vs. Input Frequency: V_{REF} = 5V.

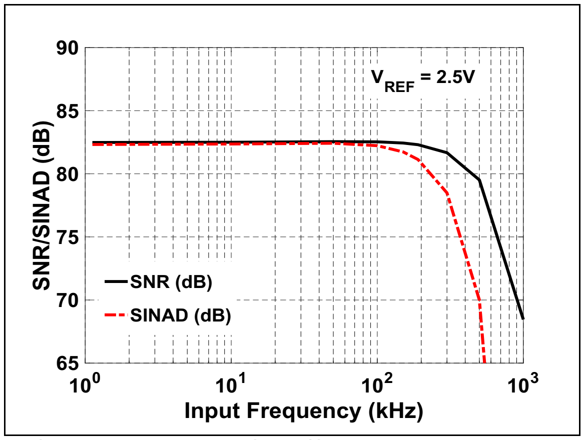


FIGURE 3-22: SNR/SINAD vs.Input Frequency: V_{IN} = -1 dBFS.

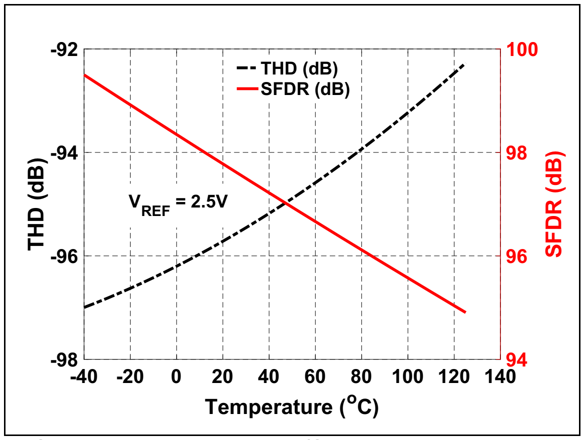


FIGURE 3-23: THD/SFDR vs. Temperature: V_{REF} = 2.5V.

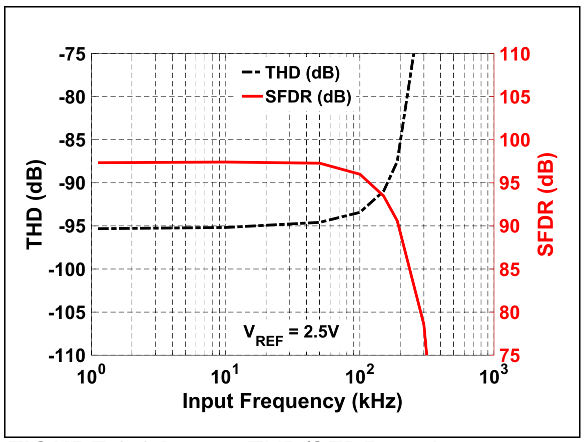


FIGURE 3-24: THD/SFDR vs. Input Frequency: V_{REF} = 2.5V.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33121D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33121D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

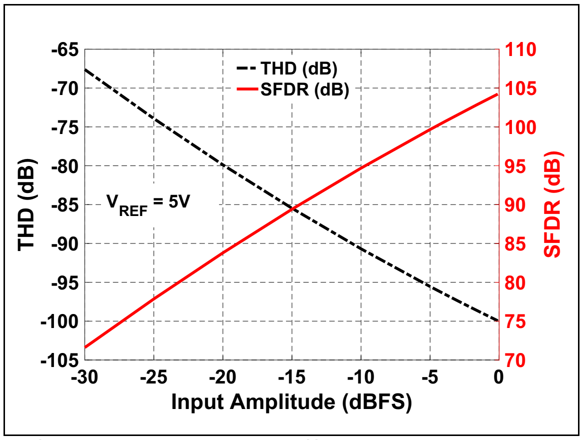


FIGURE 3-25: *THD/SFDR vs. Input Amplitude: V_{REF} = 5V.*

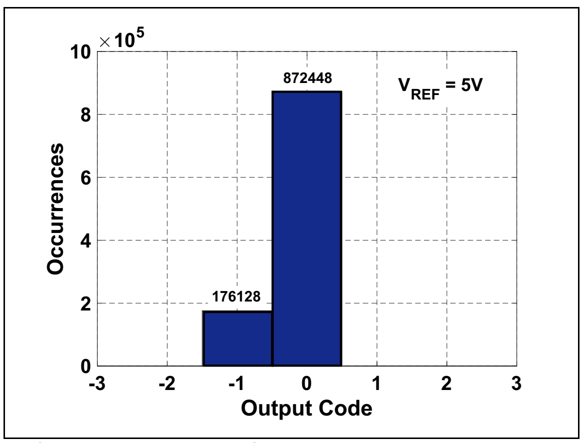


FIGURE 3-26: *Shorted Input Histogram: V_{REF} = 5V.*

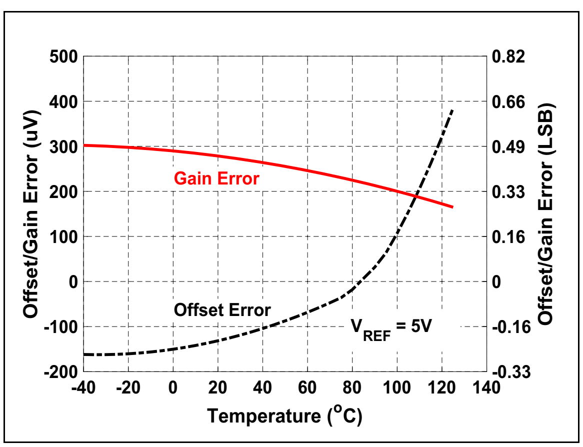


FIGURE 3-27: *Offset and Gain Error vs. Temperature: V_{REF} = 5V.*

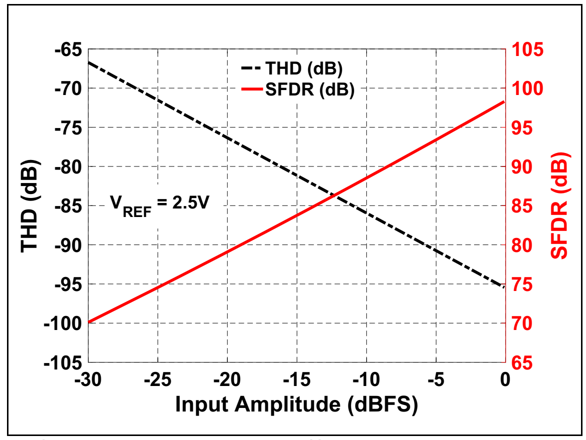


FIGURE 3-28: *THD/SFDR vs. Input Amplitude: V_{REF} = 2.5V.*

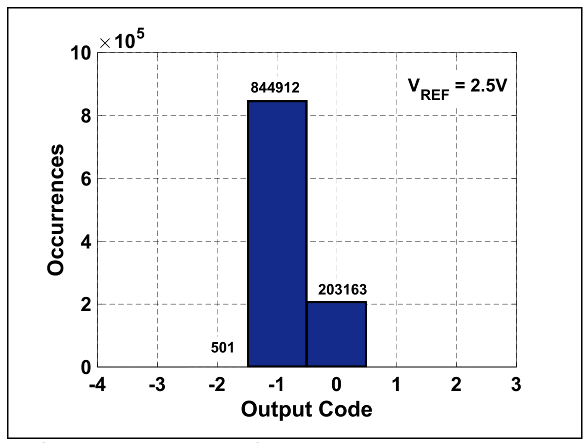


FIGURE 3-29: *Shorted Input Histogram: V_{REF} = 2.5V.*

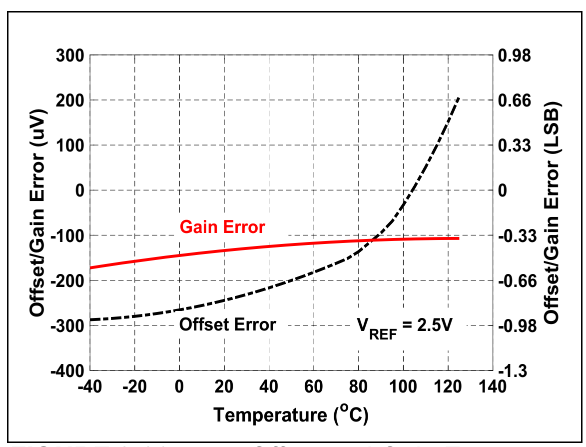


FIGURE 3-30: *Offset and Gain Error vs. Temperature: V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33121D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33121D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

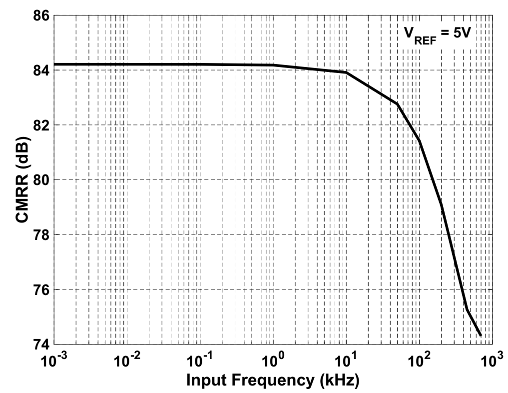


FIGURE 3-31: *CMRR vs. Input Frequency: V_{REF} = 5V.*

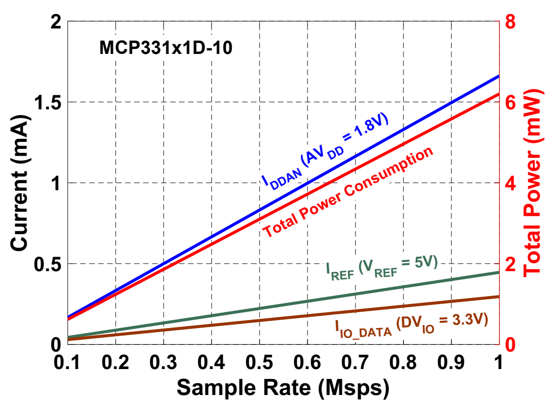


FIGURE 3-32: *Power Consumption vs. Sample Rate: C_{LOAD_SDO} = 20 pF.*

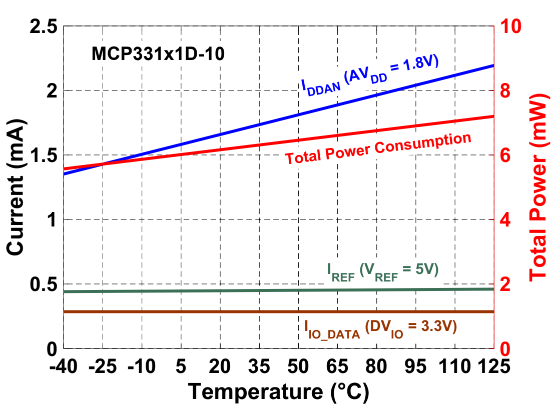


FIGURE 3-33: *Power Consumption vs. Temperature: C_{LOAD_SDO} = 20 pF.*

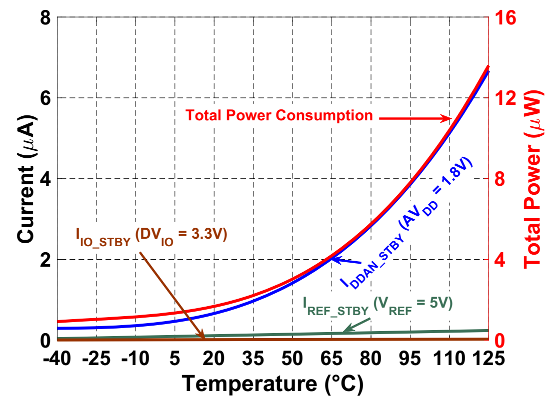


FIGURE 3-34: *Power Consumption vs. Temperature during Shutdown.*

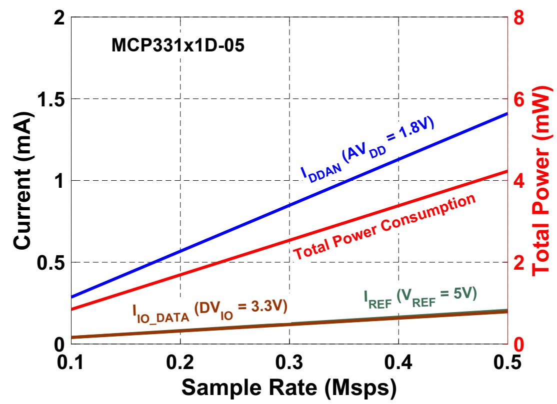


FIGURE 3-35: *Power Consumption vs. Sample Rate: C_{LOAD_SDO} = 20 pF.*

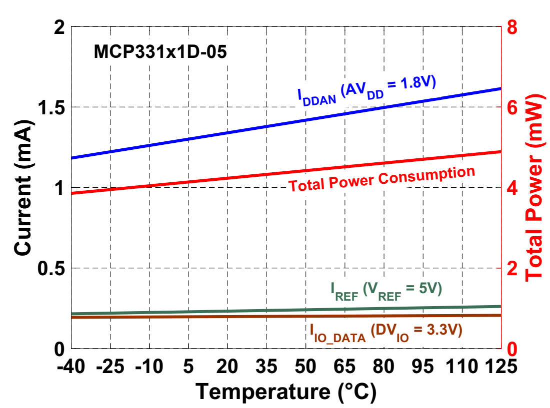


FIGURE 3-36: *Power Consumption vs.*

4.0 TYPICAL PERFORMANCE CURVES FOR 12-BIT DEVICES (MCP33111D-XX)

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33111D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33111D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

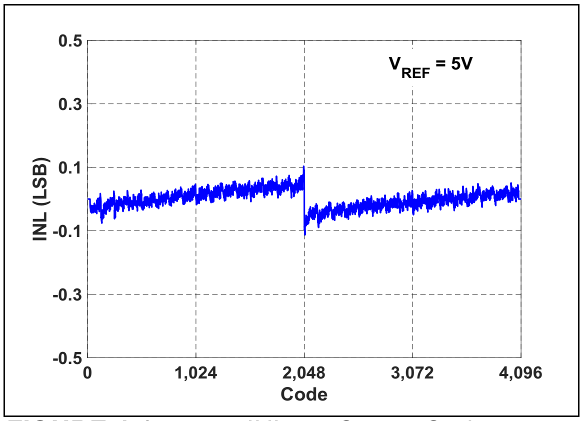


FIGURE 4-1: INL vs. Output Code.

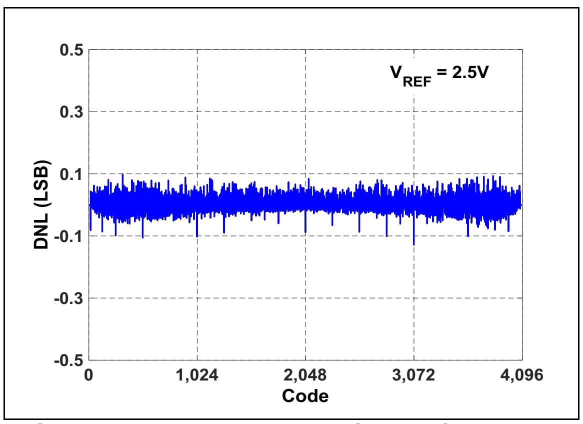


FIGURE 4-2: DNL vs. Output Code.

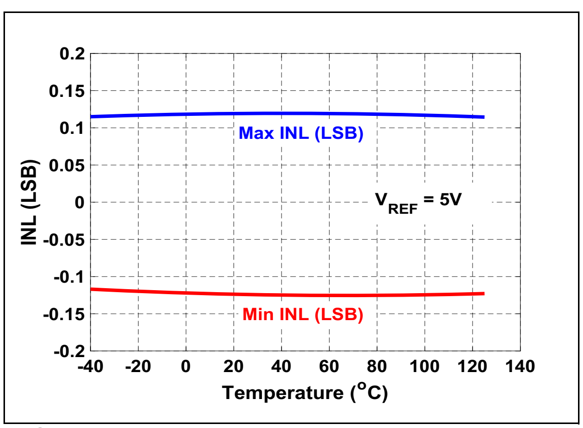


FIGURE 4-3: INL vs. Temperature.

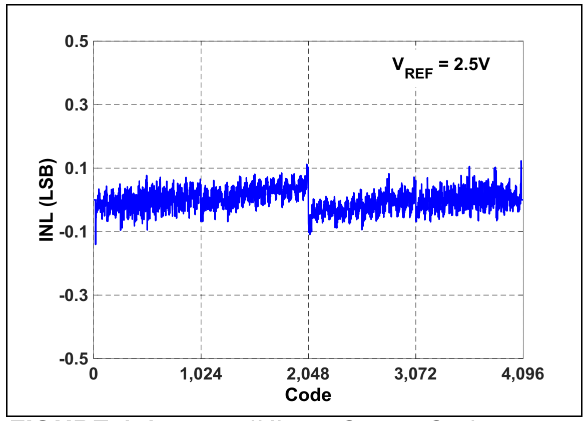


FIGURE 4-4: INL vs. Output Code.

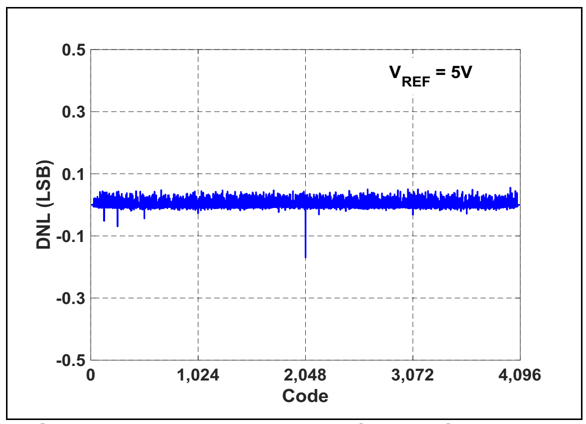


FIGURE 4-5: DNL vs. Output Code.

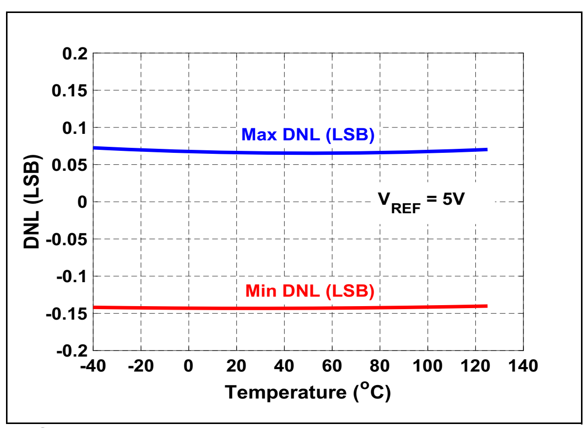


FIGURE 4-6: DNL vs. Temperature.

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33111D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33111D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

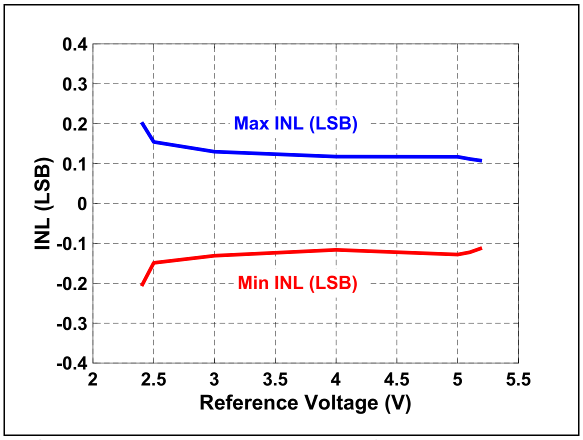


FIGURE 4-7: *INL vs. Reference Voltage.*

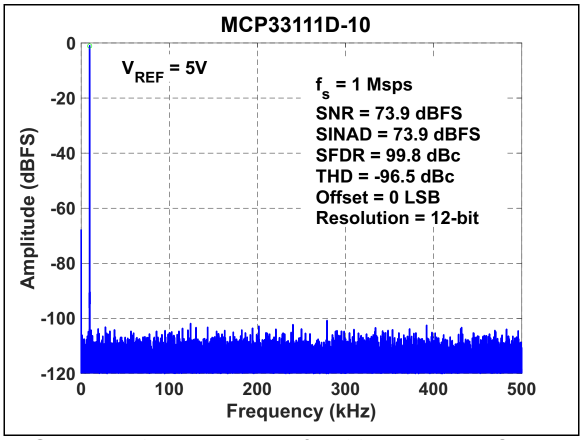


FIGURE 4-8: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 5V.*

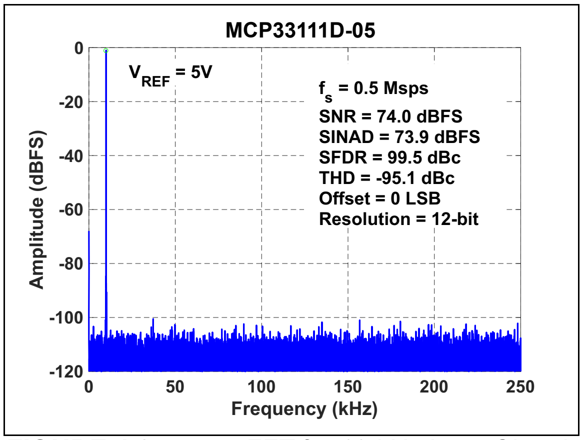


FIGURE 4-9: *FFT for 10 kHz Input Signal: f_S = 500 kSPS, V_{IN} = -1 dBFS, V_{REF} = 5V.*

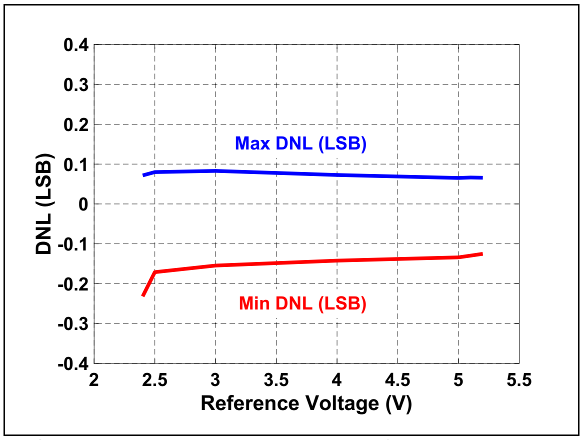


FIGURE 4-10: *DNL vs. Reference Voltage.*

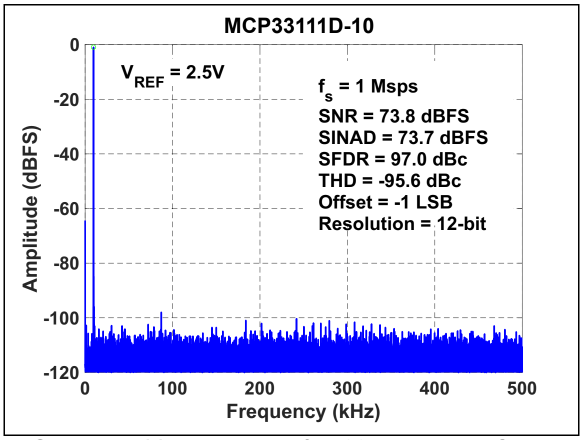


FIGURE 4-11: *FFT for 10 kHz Input Signal: f_S = 1 Msps, V_{IN} = -1 dBFS, V_{REF} = 2.5V.*

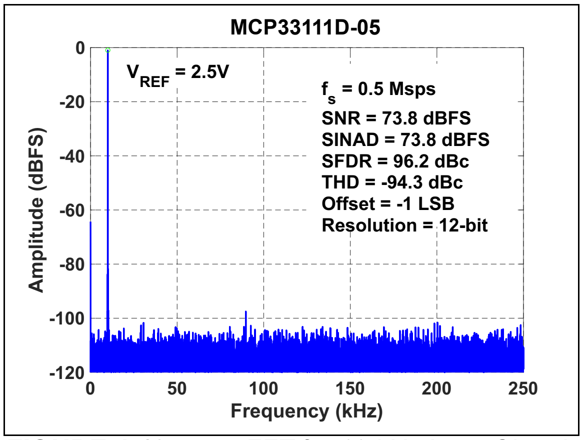


FIGURE 4-12: *FFT for 10 kHz Input Signal: f_S = 500 kSPS, V_{IN} = -1 dBFS, V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33111D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33111D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

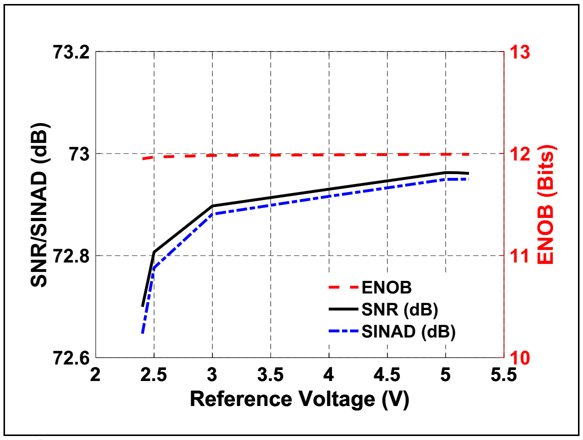


FIGURE 4-13: *SNR/SINAD/ENOB vs. V_{REF}*

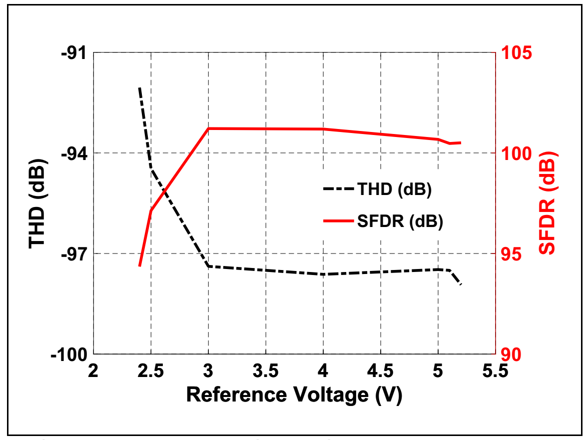


FIGURE 4-16: *SFDR/THD vs. V_{REF}*

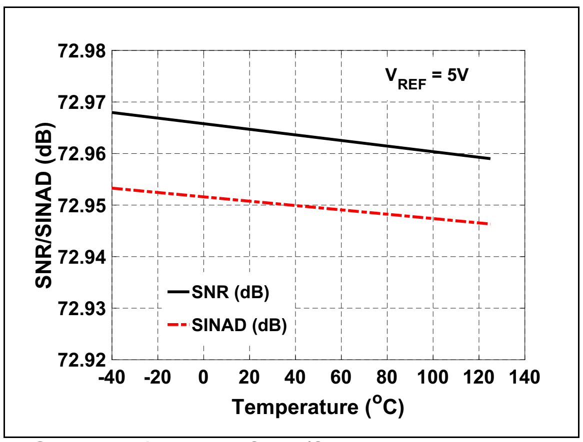


FIGURE 4-14: *SNR/SINAD vs. Temperature: V_{REF} = 5V.*

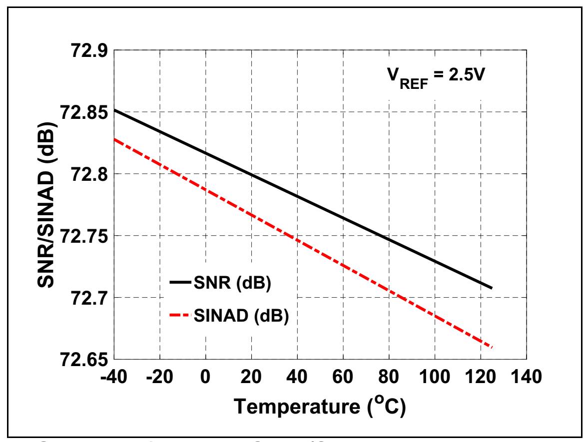


FIGURE 4-17: *SNR/SINAD vs. Temperature: V_{REF} = 2.5V.*

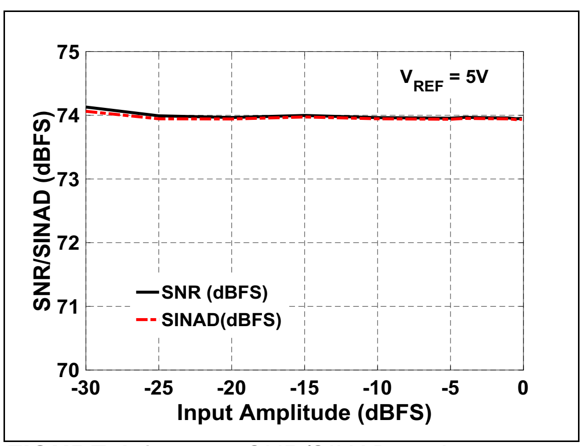


FIGURE 4-15: *SNR/SINAD vs. Input Amplitude: F_{IN} = 10 kHz.*

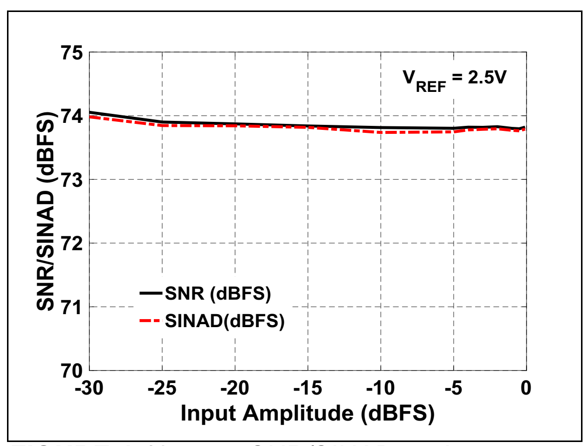


FIGURE 4-18: *SNR/SINAD vs. Input Amplitude: F_{IN} = 10 kHz.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33111D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33111D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

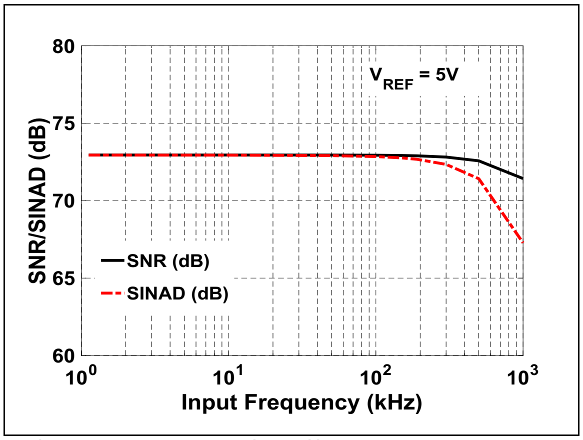


FIGURE 4-19: *SNR/SINAD vs. Input Frequency: V_{IN} = -1 dBFS*

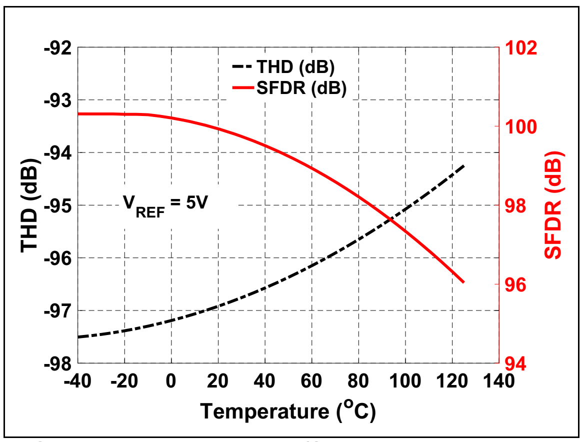


FIGURE 4-20: *THD/SFDR vs. Temperature: V_{REF} = 5V.*

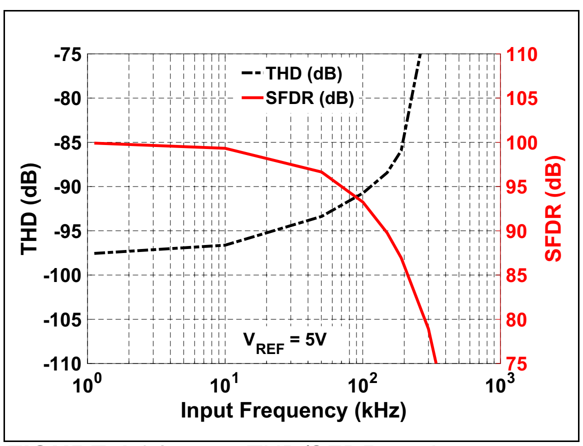


FIGURE 4-21: *THD/SFDR vs. Input Frequency: V_{REF} = 5V.*

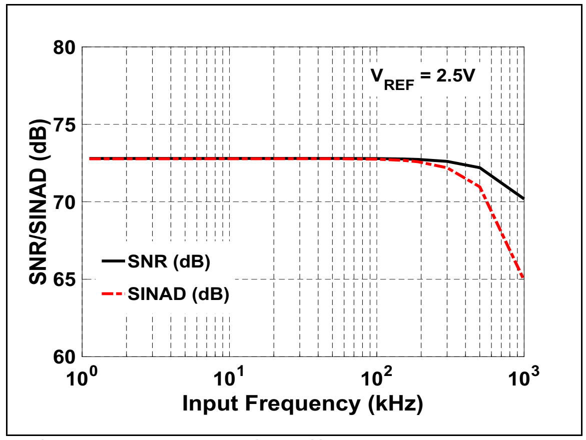


FIGURE 4-22: *SNR/SINAD vs. Input Frequency: V_{IN} = -1 dBFS.*

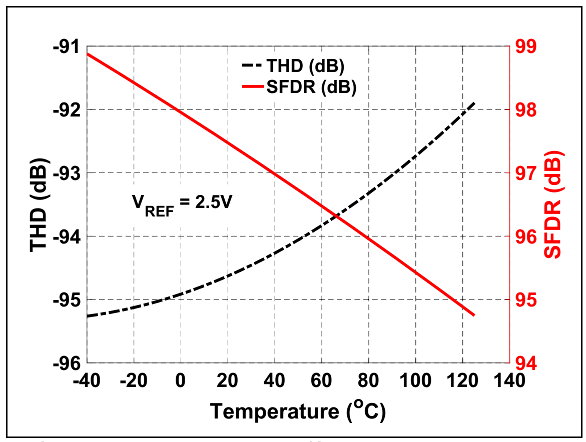


FIGURE 4-23: *THD/SFDR vs. Temperature: V_{REF} = 2.5V.*

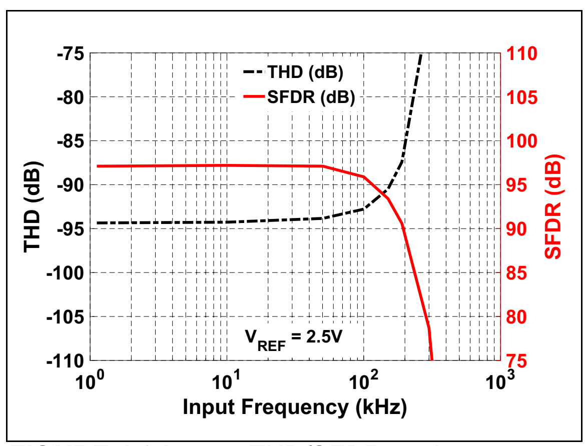


FIGURE 4-24: *THD/SFDR vs. Input Frequency: V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33111D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33111D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

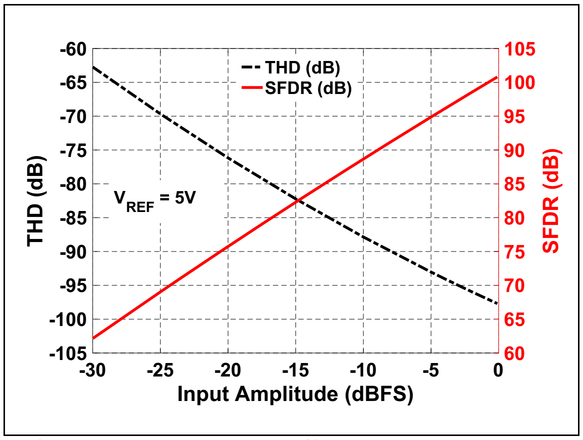


FIGURE 4-25: *THD/SFDR vs. Input Amplitude: V_{REF} = 5V.*

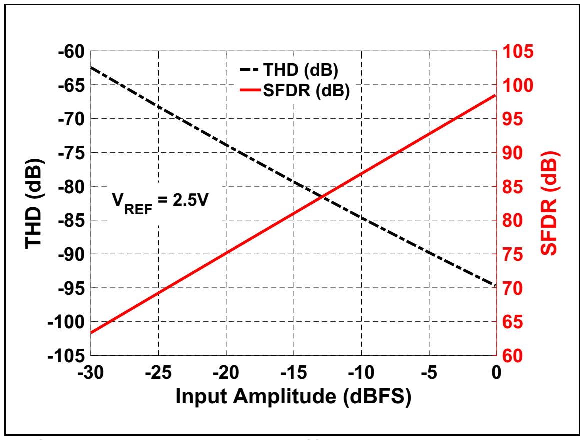


FIGURE 4-28: *THD/SFDR vs. Input Amplitude: V_{REF} = 2.5V.*

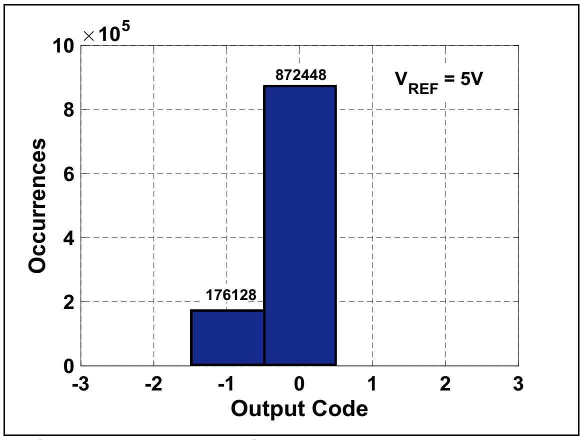


FIGURE 4-26: *Shorted Input Histogram: V_{REF} = 5V.*

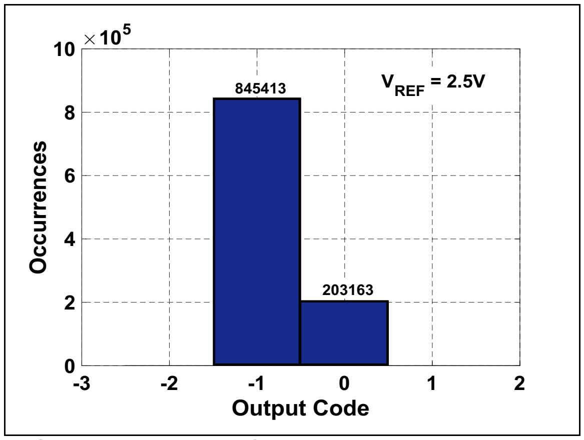


FIGURE 4-29: *Shorted Input Histogram: V_{REF} = 2.5V.*

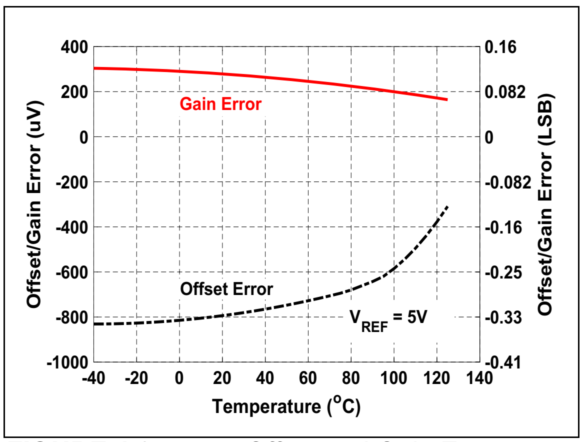


FIGURE 4-27: *Offset and Gain Error vs. Temperature: V_{REF} = 5V.*

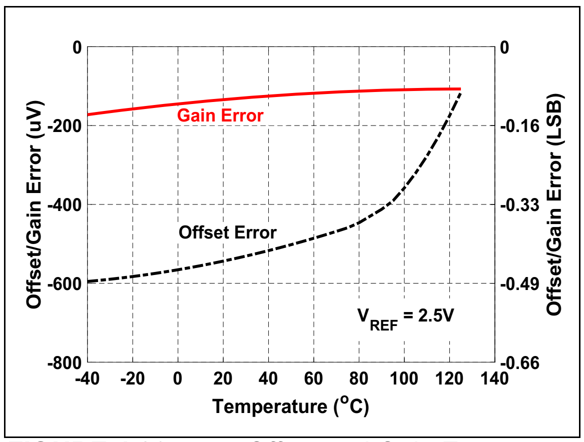


FIGURE 4-30: *Offset and Gain Error vs. Temperature: V_{REF} = 2.5V.*

Note: Unless otherwise specified, all parameters apply for T_A = +25°C, AV_{DD} = 1.8V, DV_{IO} = 3.3V, V_{REF} = 5V, GND = 0V, Differential Analog Input (VIN) = -1 dBFS, f_{IN} = 10 kHz, C_{LOAD_SDO} = 20 pF.
MCP33111D-10: Sample Rate (f_S) = 1 Msps, SPI Clock Input (SCLK) = 60 MHz.
MCP33111D-05: Sample Rate (f_S) = 500 kSPS, SPI Clock Input (SCLK) = 30 MHz.

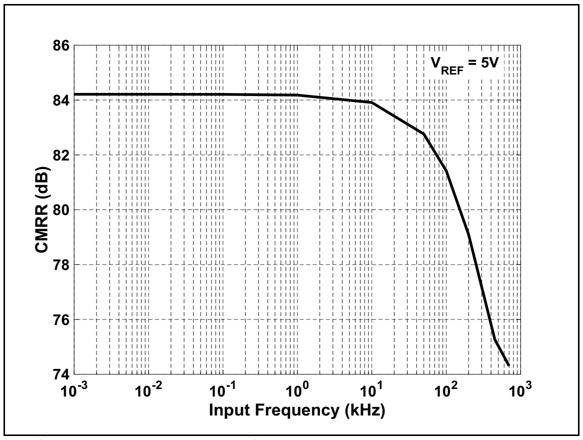


FIGURE 4-31: *CMRR vs. Input Frequency: V_{REF} = 5V.*

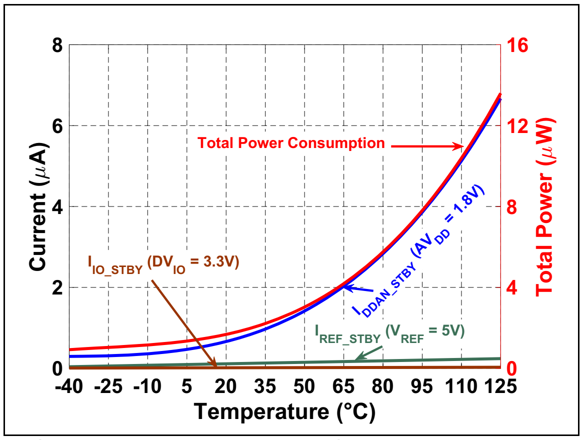


FIGURE 4-34: *Power Consumption vs. Temperature during Shutdown.*

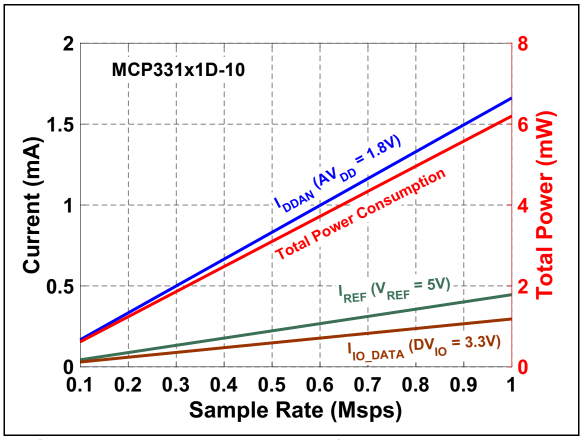


FIGURE 4-32: *Power Consumption vs. Sample Rate: C_{LOAD_SDO} = 20 pF.*

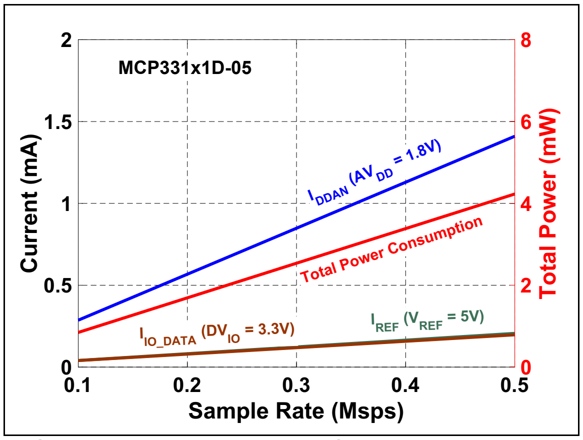


FIGURE 4-35: *Power Consumption vs. Sample Rate: C_{LOAD_SDO} = 20 pF.*

MCP331x1D-10

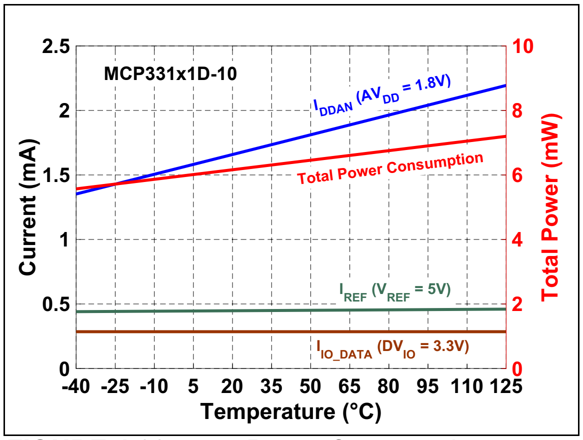


FIGURE 4-33: *Power Consumption vs. Temperature: C_{LOAD_SDO} = 20 pF.*

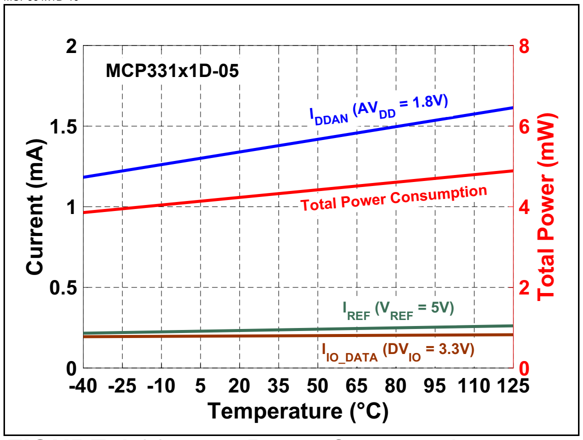


FIGURE 4-36: *Power Consumption vs. Temperature: C_{LOAD_SDO} = 20 pF.*

5.0 PIN FUNCTION DESCRIPTIONS

TABLE 5-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Function
1	V_{REF}	Reference voltage input (2.5V - 5.1V). This pin should be decoupled with a 10 µF tantalum capacitor.
2	AV_{DD}	DC supply voltage input for analog section (1.8V). This pin should be decoupled with a 1 µF ceramic capacitor.
3	$A_{IN}+$	Differential positive analog input.
4	$A_{IN}-$	Differential negative analog input.
5	GND	Power supply ground reference. This pin is a common ground for both the analog power supply (AV_{DD}) and digital I/O supply (DV_{IO}).
6	CNVST	Conversion-start control and active-low SPI chip-select digital input. A new conversion is started on the rising edge of CNVST. When the conversion is complete, output data is available at SDO by lowering CNVST.
7	SDO	SPI-compatible serial digital data output: ADC conversion data is shifted out by SCLK clock, with MSB first.
8	SCLK	SPI-compatible serial data clock digital input. The ADC output is synchronously shifted out by this clock.
9	SDI	SPI-compatible serial data digital input. Tie to DV_{IO} for normal operation.
10	DV_{IO}	DC supply voltage for digital input/output interface (1.7V - 5.5V). This pin should be decoupled with a 0.1 µF ceramic capacitor.

5.1 Supply Voltages and Reference Voltage

The device has two power supply pins:

a) Analog power supply (AV_{DD}): 1.8V

b) Digital input/output interface power supply (DV_{IO}): 1.7V to 5.5V.

The large supply voltage range of DVIO allows the device to interface with various host devices that are operating with different supply voltages. See Table 1-2 for timing specifications for I/O interface signal parameters depending on DVIO voltage.

Note: Proper decoupling capacitors (1 µF to AV_{DD}, 0.1 µF to DV_{IO}) should be mounted as close as possible to the respective pins.

5.2 Reference Voltage (V_{REF})

The device requires a single-ended external reference voltage (V_{REF}). The external input reference range is from 2.5V to 5.1V. This reference voltage sets the input full-scale range from 0V to V_{REF}. See Figure 6-2 to Figure 6-8 for example application circuits and reference voltage settings.

Note: The reference pin needs a tantalum decoupling capacitor (10 µF, 10V rating). Additional multiple ceramic capacitors can be added in parallel to decouple high-frequency noises.

Note: During the initial power-up sequence, the reference voltage (V_{REF}) must be provided prior to supplying AV_{DD} or within about 64 ms after supplying AV_{DD}. Otherwise, it is strongly recommended to send a recalibrate command. See **Section 7.1 "Recalibrate Command"** for more details.

5.2.1 VOLTAGE REFERENCE SELECTION

The performance of the voltage reference has a large impact on the accuracy of high-precision data acquisition systems. The voltage reference should have high-accuracy, low-noise, and low-temperature drift. A ±0.1% output accuracy of the reference directly corresponds to ±0.1% absolute accuracy of the ADC output. The RMS output noise voltage of the reference should be less than 1/2 LSB of the ADC.

6.0 DEVICE OVERVIEW

When the MCP33131D/MCP33121D/MCP33111D-XX is first powered-up, it performs a self-calibration and enters a low current input acquisition mode (Standby) by itself.

The external reference voltage (V_{REF}) ranging from 2.5V to 5.1V sets the differential input full-scale range (FSR) from $-V_{REF}$ to $+V_{REF}$.

The differential input signal needs an appropriate input common-mode voltage from 0V to V_{REF}, depending on the input signal condition. $V_{REF}/2$ is typically used for a symmetric differential input.

During input acquisition (Standby), the internal input sampling capacitors are connected to the input signal, while most of the internal analog circuits are shutdown to save power. During this input acquisition time (t_{ACQ}), the device consumes less than 1 µA.

The user can operate the device with an easy-to-use SPI-compatible 3-wire interface.

The device initiates data conversion on the rising edge of the conversion-start control (CNVST). The data conversion time (t_{CNV}) is set by the internal clock. Once the conversion is complete and the host lowers CNVST, the output data is available on SDO and the device starts the next input acquisition by itself. During this input acquisition time (t_{ACQ}), the user can clock out the output data by providing the SPI-compatible serial clock (SCLK).

The device provides conversion data with no missing codes. This ADC device family has a large input full-scale range, high precision, high throughput with no output latency, and is an ideal choice for various ADC applications.

6.1 Analog Inputs

Figure 6-1 shows a simplified equivalent circuit of the differential input architecture with a switched capacitor input stage. The input sampling capacitors (C_S^+ and C_S^-) are about 31 pF each. The back-to-back diodes (D_1 - D_2) at each input are ESD protection diodes. Note that these ESD diodes are tied to V_{REF}, so that each input signal can swing from 0V to $+V_{REF}$ and from $-V_{REF}$ to $+V_{REF}$ differentially.

During input acquisition (Standby), the sampling switches are closed and each input sees the sampling capacitor (≈ 31 pF) in series with the on-resistance of the sampling switch, R_{SON} (≈ 200Ω).

For high-precision data conversion applications, the input voltage needs to be fully settled within 1/2 LSB during the input acquisition period (t_{ACQ}). The settling time is directly related to the source impedance: A lower impedance source results in faster input settling time. Although the device can be driven directly with a low impedance source, using a low noise input driver is highly recommended.

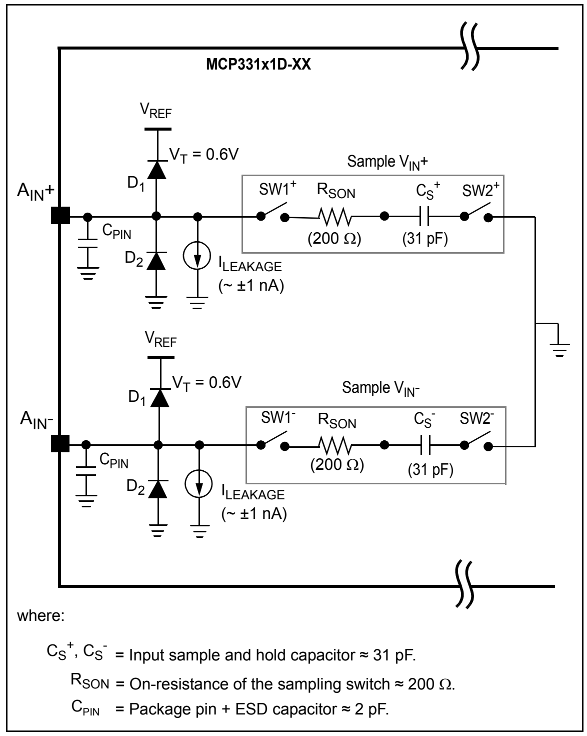


FIGURE 6-1: *Simplified Equivalent Analog Input Circuit.*

6.1.1 ABSOLUTE MAXIMUM INPUT VOLTAGE RANGE

The input voltage at each input pin ($A_{IN}+$ and $A_{IN}-$) must meet the following absolute maximum input voltage limits:

- ($V_{IN}+$, $V_{IN}-$) < V_{REF} + 0.1V
- ($V_{IN}+$, $V_{IN}-$) > GND - 0.1V

Note:	The ESD diodes at the analog input pins are biased from V_{REF}. Any input voltage outside the absolute maximum range can turn on the input ESD protection diodes and results in input leakage current which may cause conversion errors and permanent damage to the device. Care must be taken in setting the input voltage ranges so that the input voltage does not exceed the absolute maximum input voltage range.

6.1.2 INPUT VOLTAGE RANGE

The differential input (V_{IN}) and common-mode voltage (V_{CM}) at the input pins are defined by:

EQUATION 6-1: DIFFERENTIAL INPUT

$$V_{IN} = V_{IN^+} - V_{IN^-}$$

$$V_{CM} = \frac{V_{IN^+} + V_{IN^-}}{2}$$

where $V_{IN}+$ is the input at the $A_{IN}+$ pin and $V_{IN}-$ is the input at $A_{IN}-$ pin. The input signal swings around an input common-mode voltage (V_{CM}), typically centered at $V_{REF}/2$ for the best performance.

The absolute value of the differential input (V_{IN}) needs to be less than the reference voltage. The device will output saturated output codes (all 0s or all 1s except sign bit) if the absolute value of the input (V_{IN}) is greater than the reference voltage.

The differential input full-scale voltage range (FSR) is given by the external reference voltage (V_{REF}) setting:

EQUATION 6-2: FSR AND INPUT RANGE

$$\text{Input Full-Scale Range (FSR)} = 2V_{REF}$$

$$\text{Input Range:} \quad -V_{REF} \le V_{IN} \le (V_{REF} - 1LSB)$$

6.2 Analog Input Conditioning Circuits

The MCP33131D/MCP33121D/MCP33111D-XX supports various input types, such as: (a) fully-differential inputs, (b) arbitrary waveform inputs and (c) single-ended inputs.

6.2.1 FULLY-DIFFERENTIAL INPUT SIGNALS

The MCP33131D/MCP33121D/MCP33111D-XX provides the best linearity performance with fully-differential inputs. Figure 6-2 shows an example of a fully-differential input conditioning circuit with a differential input driver followed by an RC anti-aliasing filter. Figure 6-3 shows its transfer function.

The differential input (V_{IN}) between the two differential ADC analog input pins ($A_{IN}+$, $A_{IN}-$) swings from $-V_{REF}$ to $+V_{REF}$ centered at the input common-mode voltage (V_{OCM}).

The front-end differential driver provides a low output impedance, which provides fast settling of the analog inputs during the acquisition phase and provides isolation between the signal source and the ADC. The RC low-pass anti-aliasing filter band-limits the output noise of the input driver and attenuates the kick-back noise spikes from the ADC during conversion.

Figure 6-2 is the reference circuit that is used to collect most of the linearity performance data shown in Table 1-1.

The differential input driver shown in Figure 6-2 can be replaced with a low noise dual-channel op-amp. See **Section 6.3 “ADC Input Driver Selection”** for the driver selection.

6.2.2 ARBITRARY WAVEFORM INPUT SIGNALS

The MCP33131D/MCP33121D/MCP33111D-XX can convert input signals with arbitrary waveforms at the inputs $A_{IN}+$ and $A_{IN}-$. These inputs can be symmetric, non-symmetric or independent with respect to each other.

In the arbitrary input configuration, each ADC analog input is connected to a single ended source ranging from 0V to V_{REF}. In this case, the ADC converts the voltage difference between the two input signals. Figure 6-4 shows the configuration example for the arbitrary input signals.

6.2.3 SINGLE-ENDED INPUT SIGNALS

Although the MCP33131D/MCP33121D/MCP33111D-XX is a fully-differential input device, it can also convert single-ended input signals. The most commonly recommended single-ended configurations are:

(a) pseudo-differential bipolar configuration and
(b) pseudo-differential unipolar configuration.

6.2.3.1 Pseudo-Differential Bipolar Configuration

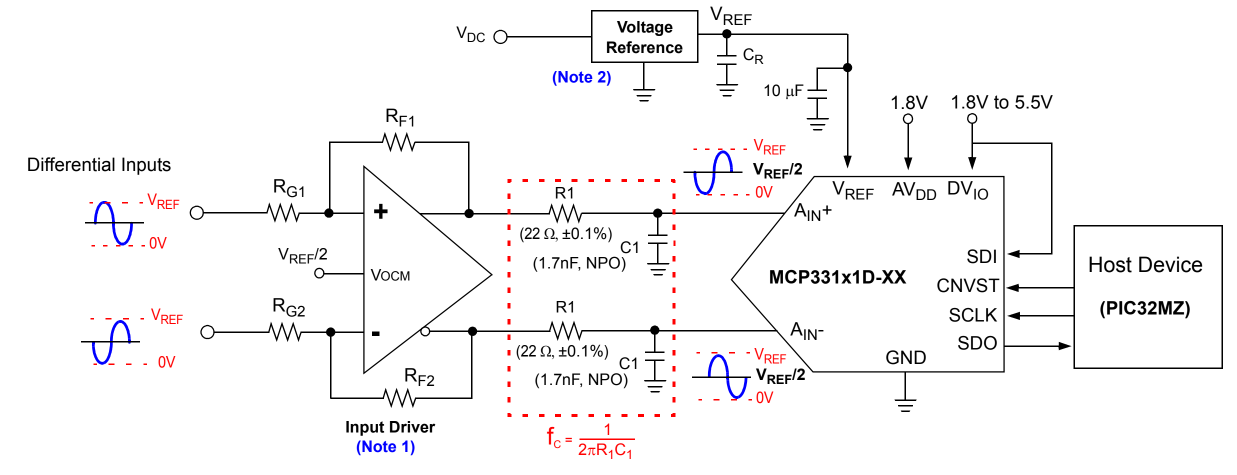
In the pseudo-differential bipolar configuration, one of the ADC analog inputs (typically $A_{IN}-$) is driven with a fixed DC voltage (typically $V_{REF}/2$), while the other ($A_{IN}+$) is connected to a single-ended signal in the range 0V to V_{REF}.

In this case, the ADC converts the voltage difference between the single-ended signal and the DC voltage. Figure 6-5 shows the configuration example and Figure 6-6 shows its transfer function.

6.2.3.2 Pseudo-Differential Unipolar Configuration

In the pseudo-differential unipolar input configuration, one of the ADC analog inputs (typically $A_{IN}-$) is connected to ground, while the other ($A_{IN}+$) is connected to a single ended signal in the range 0V to V_{REF}.

In this case, the ADC converts the voltage difference between the single ended signal and ground. Figure 6-7 shows the configuration example and Figure 6-8 shows its transfer function.



Note 1: Contact Microchip Technology Inc. for availability of the differential input driver amplifiers.

2: Contact Microchip Technology Inc. for the MCP1501 voltage reference application circuit.

FIGURE 6-2: *Input Conditional Circuit for Fully-Differential Input.*

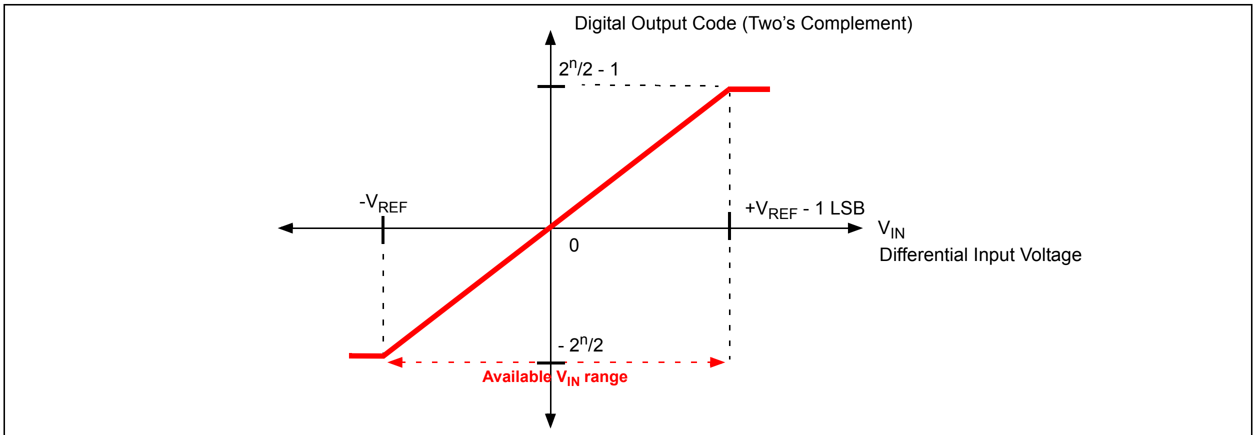
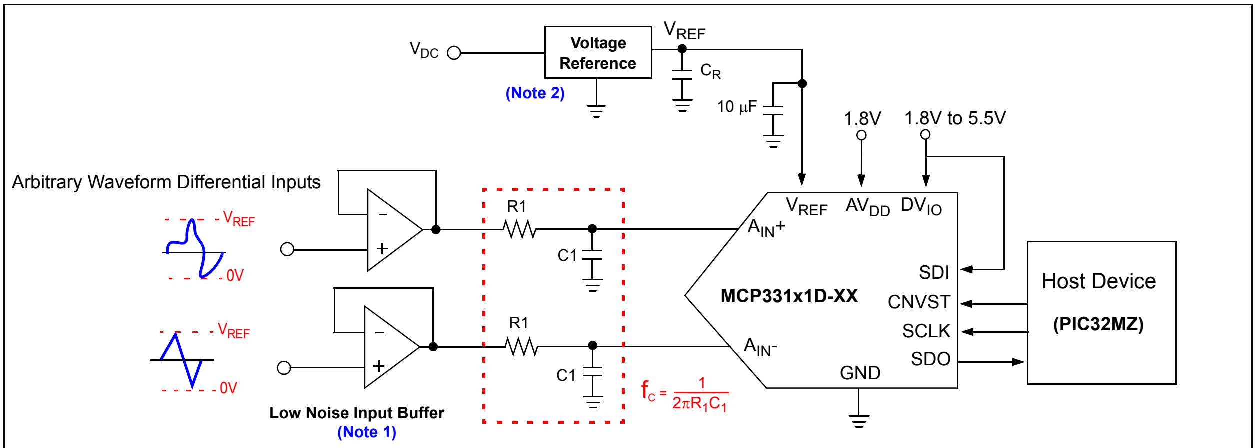
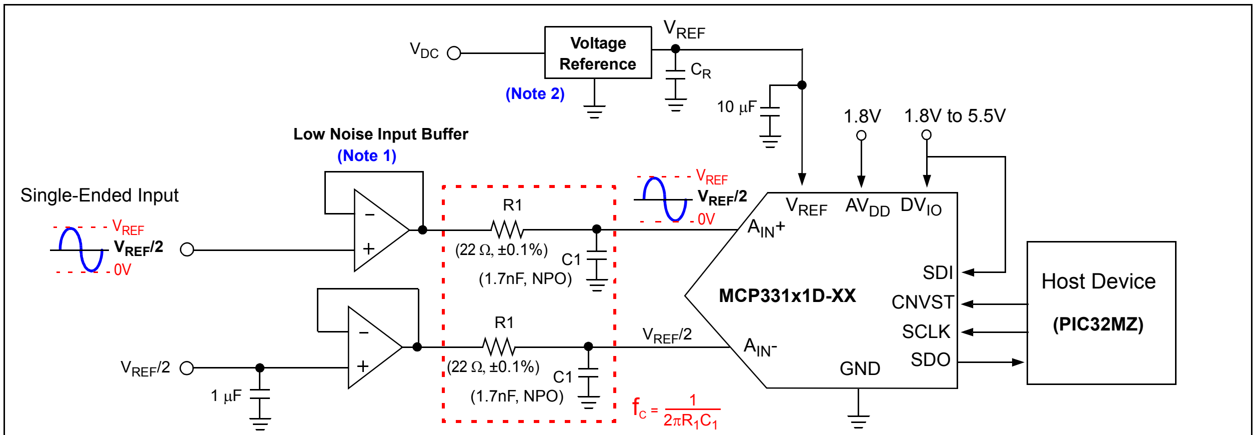


FIGURE 6-3: *Transfer Function for Figure 6-2.*



Note 1: Contact Microchip Technology Inc. for availability of the low-noise input driver amplifiers.
2: Contact Microchip Technology Inc. for the MCP1501 voltage reference application circuit.

FIGURE 6-4: *Input Configuration for Arbitrary Waveform Input Signals.*



Note 1: Contact Microchip Technology Inc. for availability of the low-noise input driver amplifiers.
2: Contact Microchip Technology Inc. for the MCP1501 voltage reference application circuit.

FIGURE 6-5: *Pseudo-Differential Bipolar-Input Configuration for Single-Ended Input Signal.*

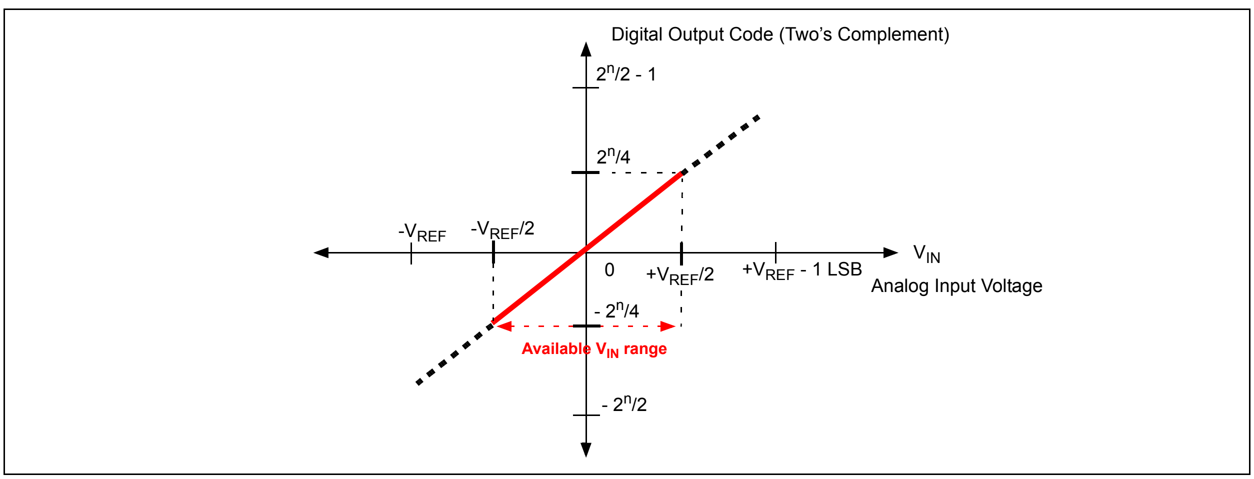
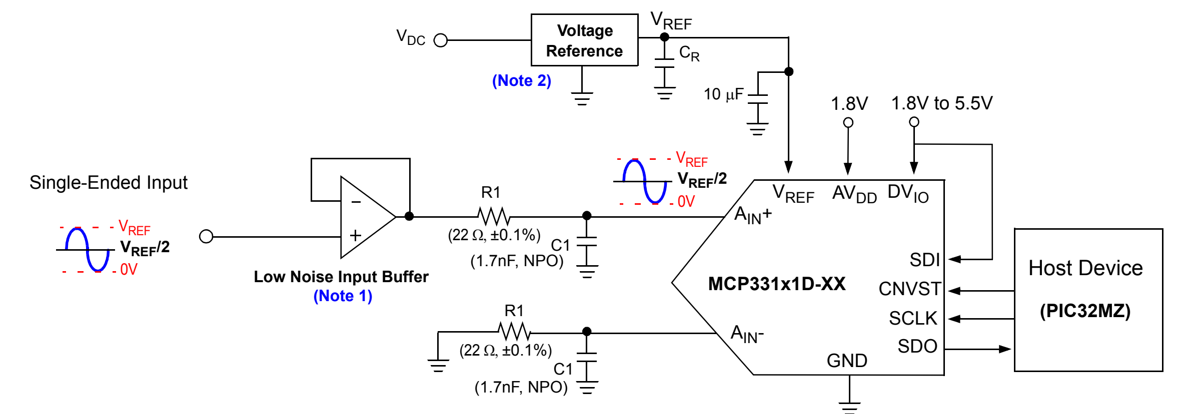


FIGURE 6-6: *Transfer Function for Figure 6-5.*



Note 1: Contact Microchip Technology Inc. for availability of the low-noise input driver amplifiers.
2: Contact Microchip Technology Inc. for the MCP1501 voltage reference application circuit.

FIGURE 6-7: *Pseudo-Differential Unipolar-Input Configuration for Single-Ended Input Signal.*

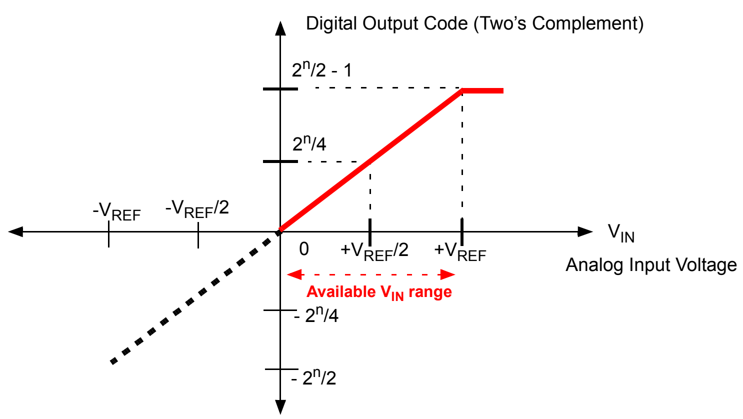


FIGURE 6-8: *Transfer Function for Figure 6-7.*

6.3 ADC Input Driver Selection

The noise and distortion of the ADC input driver can degrade the dynamic performance (SNR, SFDR, and THD) of the overall ADC application system. Therefore, the ADC input driver needs better performance specifications than the ADC itself. The data sheet of the driver typically shows the output noise voltage and harmonic distortion parameters.

Figure 6-9 shows a simplified system noise presentation block diagram for the front-end driver and ADC.

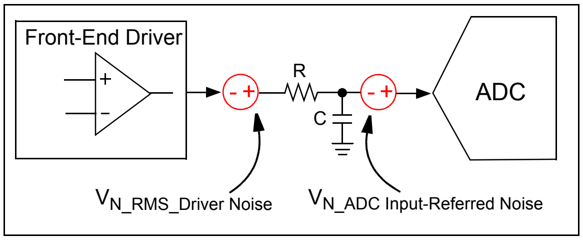


***FIGURE 6-9:** Simplified System Noise Representation.*

- **Unity-Gain Bandwidth:**

An input driver with higher bandwidth usually results in better overall linearity performance. Typically, the driver should have the unity-gain bandwidth greater than 5 times the -3 dB cutoff frequency of the anti-aliasing filter:

EQUATION 6-3: BANDWIDTH REQUIREMENT FOR ADC INPUT DRIVER

$$BW_{Input\ Driver} \geq 5 \times f_B \quad \text{(Hz)}$$
$$\geq \frac{5}{2\pi RC} \quad \text{for a single-pole RC filter}$$

where, f_B = -3 dB bandwidth of RC anti-aliasing filter as shown in Figure 6-9.

- **Distortion:**

The nonlinearity characteristics of the input driver cause distortions in the ADC output. Therefore, the input driver should have less distortion than the ADC itself. The recommended total harmonic distortion (THD) of the driver is at least 10 dB less than that of the ADC:

EQUATION 6-4: RECOMMENDED THD FOR ADC INPUT DRIVER

$$THD_{Input\ Driver} \leq THD_{ADC} - 10 \quad \text{(dB)}$$

- **ADC Input-Referred Noise:**

When the ADC is operating with a full-scale input range, the ADC input-referred RMS noise is approximated as shown in Equation 6-5.

EQUATION 6-5: ADC INPUT-REFERRED NOISE

$$V_{N\_ADC\ Input\text{-}Referred\ Noise}$$
$$= \frac{FSR}{2\sqrt{2}} 10^{-\frac{SNR}{20}} \quad \text{(V)}$$
$$= \frac{V_{REF}}{\sqrt{2}} 10^{-\frac{SNR}{20}} \quad \text{for differential input}$$
$$= \frac{V_{REF}}{2\sqrt{2}} 10^{-\frac{SNR}{20}} \quad \text{for single-ended input}$$

where FSR is the input full-scale range of ADC.

- **Noise Contribution from the Front-End Driver:**

The noise from the input driver can degrade the ADC's SNR performance. Therefore, the selected input driver should have the lowest possible broadband noise density and 1/f noise. When an anti-aliasing filter is used after the input driver, the output noise density of the input driver is integrated over the -3 dB bandwidth of the filter.

Equation 6-6 shows the RMS output noise voltage calculation using the RC filter's bandwidth and noise density (e_N) of the input driver. G_N in Equation 6-6 is the noise gain of the driver amplifier and becomes 1 for a unity gain buffer driver.

EQUATION 6-6: NOISE FROM FRONT-END DRIVER AMPLIFIER

$$V_{N\_RMS\_Driver\ Noise} \approx G_N \frac{e_N}{\sqrt{2}} \sqrt{\pi f_B} \quad \text{(V)}$$

where e_N is the broadband noise density (V/√Hz) of the front-end driver amplifier and is typically given in its data sheet. In Equation 6-6, 1/f noise ($e_{NFlicker}$) is ignored assuming it is very small compared to the broadband noise (e_N).

For high precision ADC applications, the noise contribution from the front-end input driver amplifier is typically constrained to be less than about 20% (or 1/5 times) of the ADC input-referred noise as shown in Equation 6-7:

EQUATION 6-7: RECOMMENDED ADC INPUT DRIVER NOISE

$$V_{N\_RMS\_Driver\ Noise} \leq \frac{1}{5} V_{N\_ADC\ Input\text{-}Referred\ Noise}$$

Using Equation 6-5 to Equation 6-7, the recommended noise voltage density (e_N) limit of the ADC input driver is expressed in Equation 6-8:

EQUATION 6-8: NOISE DENSITY FOR ADC INPUT DRIVER

$$G_N \frac{e_N}{\sqrt{2}}\sqrt{\pi\ f_B} \leq \frac{1}{5}\ V_{N\_ADC\ Input\text{-}Referred\ Noise}$$

(a) e_N for differential input ADC:

$$e_N \leq \frac{1}{5\ G_N}\ \frac{1}{\sqrt{\pi\ f_B}}\ V_{REF}\ 10^{-\frac{SNR}{20}}\ \left(\frac{V}{\sqrt{Hz}}\right)$$

(b) e_N for single-ended input ADC:

$$e_N \leq \frac{1}{10\ G_N}\ \frac{1}{\sqrt{\pi\ f_B}}\ V_{REF}\ 10^{-\frac{SNR}{20}}\ \left(\frac{V}{\sqrt{Hz}}\right)$$

Using Equation 6-8, the recommended maximum noise voltage density limit for unity gain input driver for differential input ADC can be estimated. Table 6-1 to Table 6-3 show a few example results with G_N = 1. The user may use these tables as a reference when selecting the ADC input driver amplifier.

TABLE 6-1: Noise Voltage Density (e_N) of Input Driver for MCP33131D-XX

ADC (Note 1)			RC Filter	ADC Input Driver Amplifier (G_N = 1)
V_{REF}	SNR (dBFS)	ADC Input-Referred Noise	f_B (Table 2)	Noise Voltage Density (e_N)
2.5V	87	79.1 µV	3 MHz	7.3 nV/√Hz
			4 MHz	6.3 nV/√Hz
			5 MHz	5.6 nV/√Hz
3.3V	89	82.8 µV	3 MHz	7.6 nV/√Hz
			4 MHz	6.6 nV/√Hz
			5 MHz	5.9 nV/√Hz
5V	92	88.8 µV	3 MHz	8.2 nV/√Hz
			4 MHz	7.1 nV/√Hz
			5 MHz	6.3 nV/√Hz

Note 1: See Equation 6-5 for the ADC input-referred noise calculation for differential input.
2: f_B is -3dB bandwidth of the RC anti-aliasing filter.

TABLE 6-2: Noise Voltage Density (e_N) of Input Driver for MCP33121D-XX

ADC (Note 1)			RC Filter	ADC Input Driver Amplifier (G_N = 1)
V_{REF}	SNR (dBFS)	ADC Input-Referred Noise	f_B (Note 2)	Noise Voltage Density (e_N)
2.5V	84	111.5 µV	3 MHz	10.3 nV/√Hz
			4 MHz	8.9 nV/√Hz
			5 MHz	8 nV/√Hz
3.3V	84.5	139 µV	3 MHz	12.8 nV/√Hz
			4 MHz	11.1 nV/√Hz
			5 MHz	9.9 nV/√Hz
5V	85	198.8 µV	3 MHz	18.3 nV/√Hz
			4 MHz	15.9 nV/√Hz
			5 MHz	14.2 nV/√Hz

Note 1: See Equation 6-5 for the ADC input-referred noise calculation for differential input.
2: f_B is -3dB bandwidth of the RC anti-aliasing filter.

TABLE 6-3: Noise Voltage Density (e_N) of Input Driver for MCP33111D-XX

ADC (Note 1)			RC Filter	ADC Input Driver Amplifier (G_N = 1)
V_{REF}	SNR (dBFS)	ADC Input-Referred Noise	f_B (Note 2)	Noise Voltage Density (e_N)
2.5V	73.8	360.9 µV	3 MHz	33.3 nV/√Hz
			4 MHz	28.8 nV/√Hz
			5 MHz	25.8 nV/√Hz
3.3V	73.9	471 µV	3 MHz	43.4 nV/√Hz
			4 MHz	37.6 nV/√Hz
			5 MHz	33.6 nV/√Hz
5V	74	705.4 µV	3 MHz	65 nV/√Hz
			4 MHz	56.3 nV/√Hz
			5 MHz	50.3 nV/√Hz

Note 1: See Equation 6-5 for the ADC input-referred noise calculation for differential input.
2: f_B is -3dB bandwidth of the RC anti-aliasing filter.

6.4 Device Operation

When the MCP33131D/MCP33121D/MCP33111D-XX is first powered-up, it self-calibrates internal systems and enters input acquisition mode by itself. The device operates in two phases: **(a)** Input Acquisition (Standby) and **(b)** Data Conversion. Figure 6-10 shows the ADC operating sequence.

6.4.1 INPUT ACQUISITION PHASE (STANDBY)

During the input acquisition phase (t_{ACQ}), also called Standby, the two input sampling capacitors, C_S^+ and C_S^-, are connected to the $A_{IN}+$ and $A_{IN}-$ pins, respectively. The input voltage is sampled until a rising edge on CNVST is detected. The input voltage should be fully settled within 1/2 LSB during t_{ACQ}.

During this input acquisition time (t_{ACQ}), the ADC consumes less than 1 µA. The acquisition time (t_{ACQ}) is user-controllable. The system designer can increase the acquisition time (t_{ACQ}) as long as needed for additional power savings.

6.4.2 DATA CONVERSION PHASE

The start of the conversion is controlled by CNVST. On the rising edge of CNVST, the sampled charge is locked (sample switches are opened) and the ADC performs the conversion. Once a conversion is started, it will not stop until the current conversion is complete. The data conversion time (t_{CNV}) is not user controllable. After the conversion is complete and the host lowers CNVST, the output data is presented on SDO.

Any noise injection during the conversion phase may affect the accuracy of the conversion. To reduce external environment noise, minimize I/O events and running clocks during the conversion time.

The output data is clocked out MSB first. While the output data is being transferred, the device enters the next input acquisition phase.

Note:	Transferring output data during the acquisition phase can disturb the next input sample. It is highly recommended to allow at least t_{QUIET} (10 ns, typical) between the last edge on the SPI interface and the rising edge on CNVST. See Figure 1-1 for t_{QUIET}.

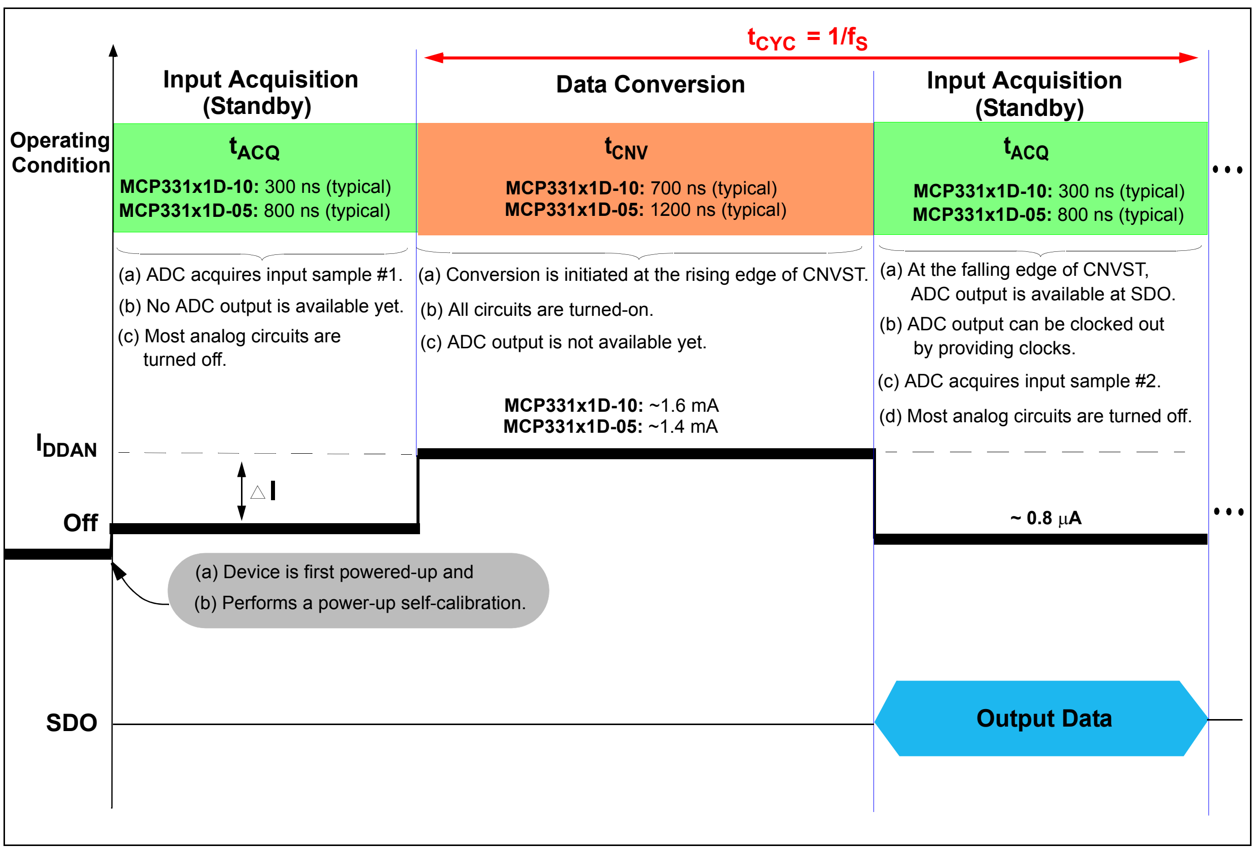


FIGURE 6-10: *Device Operating Sequence.*

6.4.3 SAMPLE (THROUGHPUT) RATE

The device completes data conversion within the maximum specification of the data conversion time (t_{CNV}). The continuous input sample rate is the inverse of the sum of input acquisition time (t_{ACQ}) and data conversion time (t_{CNV}). Equation 6-9 shows the continuous sample rate calculation using the minimum and maximum specifications of the input acquisition time (t_{ACQ}) and data conversion time (t_{CNV}).

EQUATION 6-9: SAMPLE RATE

$$\text{Sample Rate} = \frac{1}{(t_{ACQ} + t_{CNV})}$$

(a) MCP331x1D-10:

$$\text{Sample Rate} = \frac{1}{(290ns + 710ns)} = 1 \ Msps$$

(b) MCP331x1D-05:

$$\text{Sample Rate} = \frac{1}{(700ns + 1300ns)} = 500 \ kSPS$$

6.4.4 SERIAL SPI CLOCK FREQUENCY REQUIREMENT

The ADC output is collected during the input acquisition time (t_{ACQ}). For continuous input sampling and data conversion sequence, the SPI clock frequency should be fast enough to clock out all output data bits during the input acquisition time (t_{ACQ}). For the continuous sampling rate (f_S), the minimum SPI clock frequency requirement is determined by the following equation:

EQUATION 6-10: SPI CLOCK FREQUENCY REQUIREMENT

$$t_{ACQ} = N \times T_{SCLK} + t_{QUIET} + t_{EN}$$

$$f_{SCLK} = \frac{1}{T_{SCLK}} = \frac{N}{t_{ACQ} - (t_{QUIET} + t_{EN})}$$

where N is the number of output data bits, given by

N = 16-bit for MCP33131D-XX
= 14-bit for MCP33121D-XX
= 12-bit for MCP33111D-XX

T_{SCLK} = Period of SPI clock
$N \times T_{SCLK}$ = Output data window
t_{QUIET} = Quiet time between the last output bit and beginning of the next conversion start.
= 10 ns (min)
t_{EN} = Output enable time = 10 ns (max), with $DV_{IO} \geq 2.3V$

Note: See Figure 1-1 for interface timing diagram.

where f_{SCLK} is the minimum SPI serial clock frequency required to transfer all N-bits of the output data during input acquisition time (t_{ACQ}).

Table 6-4 and Table 6-5 show the examples of calculated minimum SPI clock (f_{SCLK}) requirements for various input acquisition times for 1 Msps and 500 kSPS family devices, respectively.

TABLE 6-4: SPI CLOCK SPEED VS. INPUT ACQUISITION TIME (T_{ACQ}) FOR MCP331X1D-10

Input Acquisition Time: t_{ACQ} (nS)	Data Conversion Time (nS)	SPI Clock (f_{SCLK}) Speed Requirement (Note 1), (Note 2)			Sample Rate: f_S (Msps)	Conditions
		MCP33131D-10 (16-bit)	MCP33121D-10 (14-bit)	MCP33111D-10 (12-bit)		
250	750	69.57 MHz	60.87 MHz	52.17 MHz	1	85°C < T_A ≤ 125°C (Note 3)
270		64 MHz	56 MHz	48 MHz	0.98	
280		61.54 MHz	53.85 MHz	46.15 MHz	0.97	
290	710	59.26 MHz	51.85 MHz	44.44 MHz	1	-40°C ≤ T_A ≤ 85°C
300		57.15 MHz	50 MHz	42.86 MHz	0.99	
320		53.33 MHz	46.67 MHz	40 MHz	0.97	
400		42.11 MHz	36.84 MHz	30 MHz	0.9	
540		30.77 MHz	26.92 MHz	23.08 MHz	0.8	
720		22.86 MHz	20 MHz	17.14 MHz	0.7	
720		17.2 MHz	15.05MHz	12.9 MHz	0.6	
1290		12.6 MHz	11.02 MHz	9.45 MHz	0.5	
1750		9.04 MHz	7.91 MHz	6.78 MHz	0.4	
2620		6.15 MHz	5.39 MHz	4.62 MHz	0.3	
4290		3.75 MHz	3.28 MHz	2.81 MHz	0.2	
9290		1.73 MHz	1.51 MHz	1.3 MHz	0.1	

Note 1: This is the minimum SPI clock speed requirement to collect all N-bits of the ADC output during the input acquisition time (t_{ACQ}), when the ADC is operating in continuous input sampling mode.
2: See Equation 6-10 for the calculation of the SPI clock speed requirement.
3: In extended temperature range, the device takes longer data conversion time (t_{CNV}: 750 nS, max). Using a shorter input acquisition time is recommended (t_{ACQ}: 250 nS) for 1 Msps throughput rate.

TABLE 6-5: SPI CLOCK SPEED VS. INPUT ACQUISITION TIME (T_{ACQ}) FOR MCP331X1D-05

Input Acquisition Time: t_{ACQ} (nS)	Data Conversion Time (nS)	SPI Clock (f_{SCLK}) Speed Requirement (Note 1), (Note 2)			Sample Rate: f_S (kSPS)	Conditions
		MCP33131D-05 (16-bit)	MCP33121D-05 (14-bit)	MCP33111D-05 (12-bit)		
700	1300	23.53MHz	20.59 MHz	17.65 MHz	500	$-40°C \le T_A \le 125°C$
740		22.22 MHz	19.44 MHz	16.67 MHz	490	
790		20.78 MHz	18.18 MHz	15.58 MHz	480	
930		17.58 MHz	15.39 MHz	13.19 MHz	450	
1200		13.56 MHz	11.86 MHz	10.17 MHz	400	
1560		10.39 MHz	9.09 MHz	7.79 MHz	350	
2030		7.96 MHz	6.97 MHz	5.97 MHz	300	
2700		5.97 MHz	5.22MHz	4.48 MHz	250	
3700		4.35 MHz	3.8 MHz	3.26 MHz	200	
5370		2.99 MHz	2.62 MHz	2.25 MHz	150	
8700		1.84 MHz	1.61 MHz	1.38 MHz	100	

Note 1: This is the minimum SPI clock speed requirement to collect all N-bits of the ADC output during the input acquisition time (t_{ACQ}), when the ADC is operating in continuous input sampling mode.

2: See Equation 6-10 for the calculation of the SPI clock speed requirement.

6.5 Transfer Function

The differential analog input is

$V_{IN} = (V_{IN}+) - (V_{IN}-)$.

The LSB size is given by Equation 6-11. and an example of LSB size vs. reference voltage is summarized in Table 6-6.

EQUATION 6-11: LSB SIZE - EXAMPLE

$$LSB = \frac{2V_{REF}}{2^N}$$

where N is the resolution of the ADC in bits.

TABLE 6-6: LSB SIZE VS. REFERENCE

Reference Voltage (V_{REF})	LSB Size		
	MCP33131D-XX (16-bit)	MCP33121D-XX (14-bit)	MCP33111D-XX (12-bit)
2.5V	76.3 µV	305.2 µV	1.2207 mV
2.7V	82.4 µV	329.6 µV	1.3184 mV
3V	91.6 µV	366.2 µV	1.4648 mV
3.3V	100.7 µV	402.8 µV	1.6113 mV
3.5V	106.8 µV	427.3 µV	1.7090 mV
4V	122.1 µV	488.3 µV	1.9531 mV
4.5V	137.3 µV	549.3 µV	2.1973 mV
5V	152.6 µV	610.4 µV	2.4414 mV
5.1V	155.6 µV	622.6 µV	2.4902 mV

Figure 6-11 shows the ideal transfer function and Table 6-7 shows the digital output codes for the MCP33131D/MCP33121D/MCP33111D-XX.

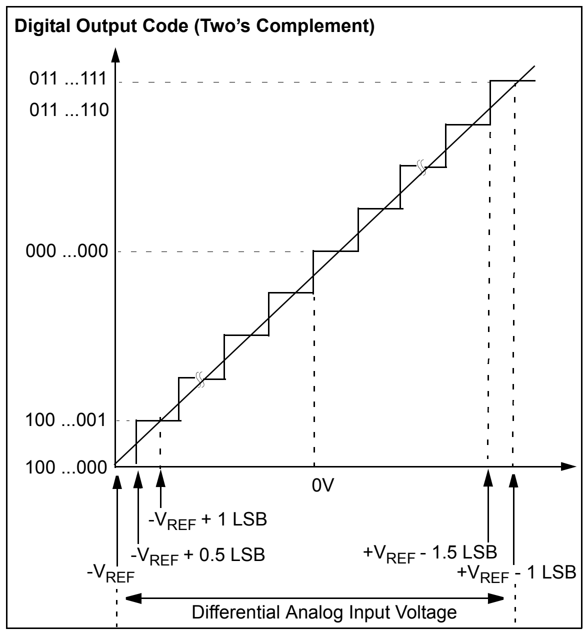


FIGURE 6-11: Ideal Transfer Function for Fully-Differential Input Signal.

6.6 Digital Output Code

The digital output code is proportional to the input voltage. The output data is in binary two's complement format. With this coding scheme the MSB can be considered a sign indicator. When the MSB is a logic '0', the input is positive. When the MSB is a logic '1', the input is negative. The following is an example of the output code:

(a) for a negative full-scale input:

Analog Input: $(V_{IN}+) - (V_{IN}-) = -V_{REF}$
Output Code: `1000...0000`

(b) for a zero differential input:

Analog Input: $(V_{IN}+) - (V_{IN}-) = 0V$
Output Code: `0000...0000`

(c) for a positive full-scale input:

Analog Input: $(V_{IN}+) - (V_{IN}-) = +V_{REF}$
Output Code: `0111...1111`

The MSB (sign bit) is always transmitted first through the SDO pin.

The code will be locked at `0111...11` for all voltages greater than (V_{REF} - 1 LSB) and `1000...00` for voltages less than $-V_{REF}$. Table 6-7 shows an example of output codes of various input levels.

TABLE 6-7: DIGITAL OUTPUT CODE

Input Voltage (V)	Digital Output Codes		
	MCP33131D-XX (16-bit)	MCP33121D-XX (14-bit)	MCP33111D-XX (12-bit)
V_{REF}	0111-1111-1111-1111	01-1111-1111-1111	0111-1111-1111
V_{REF} - 1 LSB	0111-1111-1111-1111	01-1111-1111-1111	0111-1111-1111
. .	. .	. .	. .
2 LSB	0000-0000-0000-0010	00-0000-0000-0010	0000-0000-0010
1 LSB	0000-0000-0000-0001	00-0000-0000-0001	0000-0000-0001
0V	0000-0000-0000-0000	00-0000-0000-0000	0000-0000-0000
-1 LSB	1111-1111-1111-1111	11-1111-1111-1111	1111-1111-1111
-2 LSB	1111-1111-1111-1110	11-1111-1111-1110	1111-1111-1110
. .	. .	. .	. .
$-V_{REF}$	1000-0000-0000-0000	10-0000-0000-0000	1000-0000-0000
$< -V_{REF}$	1000-0000-0000-0000	10-0000-0000-0000	1000-0000-0000

7.0 DIGITAL SERIAL INTERFACE

The device has a SPI-compatible serial digital interface using four digital pins: CNVST, SDI, SDO and SCLK.

Figure 7-1 shows the connection diagram with the host device and Figure 7-2 shows the SPI-compatible serial interface timing diagram.

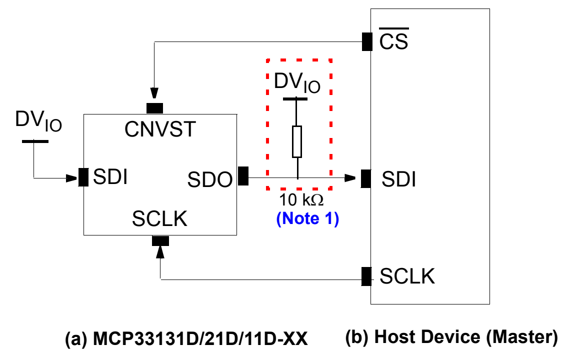
The SDI pin can be tied to the digital I/O interface supply voltage (DV_{IO}) or just maintain logic "High" level by the host. The CNVST pin is used for both chip select ($\overline{CS}$) and conversion-start control.

A rising edge on CNVST initiates the conversion process. Once the conversion is initiated, the device will complete the conversion regardless of the state of CNVST. This means the CNVST pin can be used for other purposes during t_{CNV}.

When the conversion is complete, the output is available at SDO by lowering CNVST. Data is sent MSB-first and changes on the falling edge of SCLK.

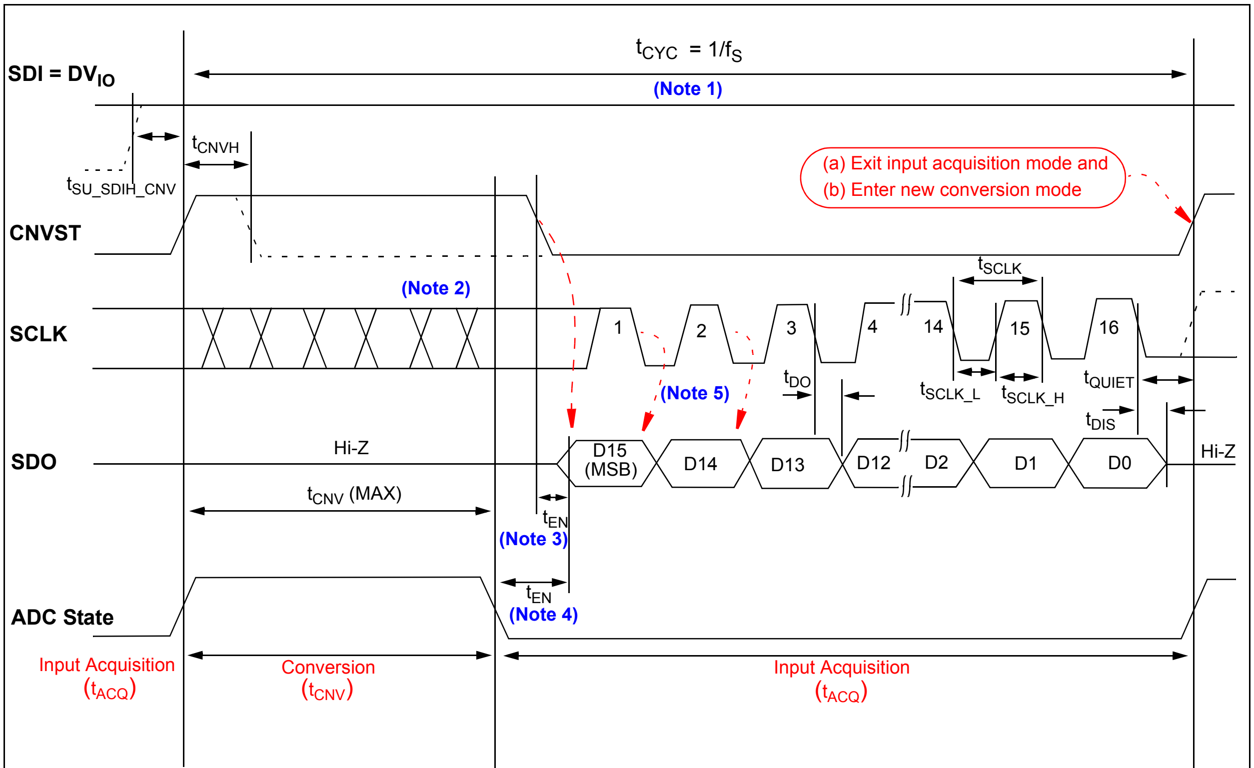
Output data can be sampled on either edge of SCLK. However, a digital host capturing data on the falling edge of SCLK can achieve a faster read out rate.

SDO returns to high-Z state after the last data bit is clocked out or when CNVST goes high, whichever occurs first.



Note 1: Adding this pull-up is needed when monitoring status of Recalibrate.

FIGURE 7-1: *Digital Interface Connection Diagram.*



Note 1: SDI must maintain "High" during the entire t_{CYC}.

2: Any SCLK toggling events (dummy clocks) before CNVST is changed to "Low" are ignored.

3: t_{EN} when CNVST is lowered after t_{CNV} (Max).

4: t_{EN} when CNVST is lowered before t_{CNV} (Max).

5: Recommended data detection: Detect SDO on the falling edge of SCLK.

FIGURE 7-2: *SPI™ Compatible Serial Interface Timing Diagram (16-bit device).*

7.1 Recalibrate Command

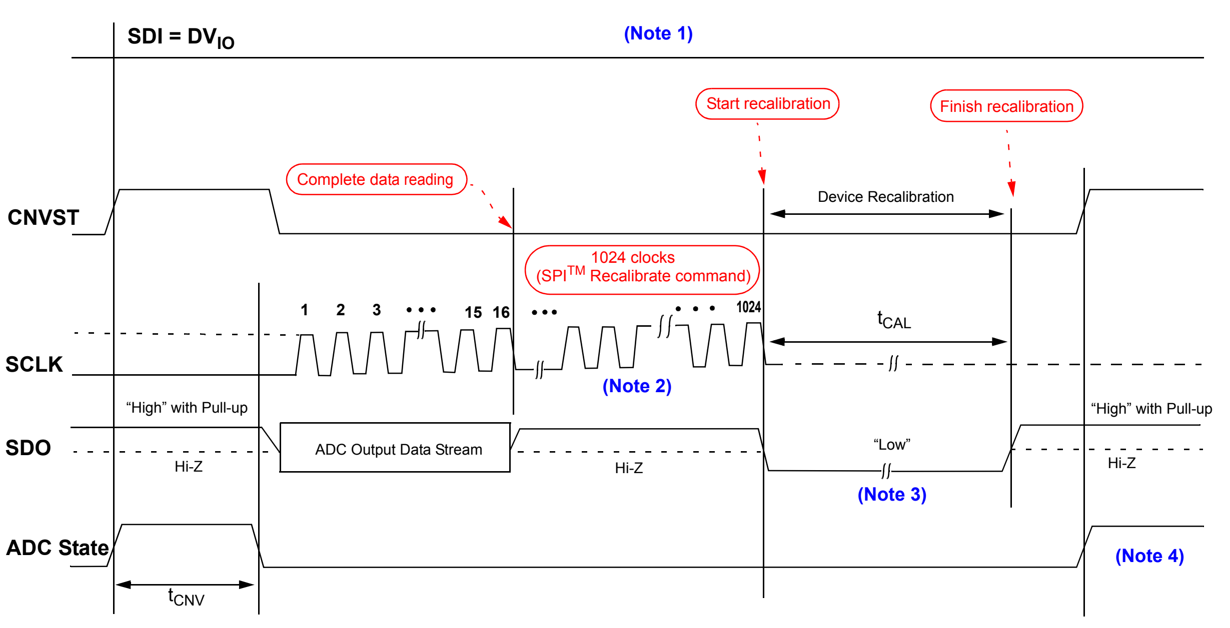
The user may use the recalibrate command in the following cases:

- When the reference voltage was not fully settled during the first-power sequence.
- During operation, to ensure optimum performance across varying environment conditions, such as reference voltage and temperature.

A self-calibration is initiated by sending the recalibrate command. The host device sends a recalibrate command by transmitting 1024 SCLK pulses (including the clocks for data bits) while the device is in the acquisition phase (Standby).

The device drives SDO low during the recalibration procedure, and returns to high-Z once completed. The status of the recalibration procedure can be monitored by placing a pull-up on SDO, so that SDO goes high when the recalibration is complete.

Figure 7-3 shows the recalibrate command timing diagram. The calibration takes approximately 500 ms (t_{CAL}).



Note 1: SDI must remain "High" during the entire recalibration cycle.
2: The 1024 clocks include the clocks for data bits.
3: SDO outputs "Low" during calibration, and Hi-Z when exiting the calibration.
4: After finishing the recalibration procedure, the device is ready for a new input sampling immediately.

FIGURE 7-3: *Recalibrate Command Timing Diagram.*

Note: When the device performs a self-calibration, it is important to note that both AV_{DD} and the reference voltage (V_{REF}) must be stabilized for a correct calibration. This is also true when the device is first powered-up, the reference voltage (V_{REF}) must be stabilized before self-calibration begins. This means the V_{REF} must be provided prior to supplying AV_{DD} or within about 64 ms after supplying AV_{DD}.

8.0 DEVELOPMENT SUPPORT

8.1 Device Evaluation Board

Microchip offers a high speed/high precision SAR ADC evaluation platform which can be used to evaluate Microchip's latest high speed/high resolution SAR ADC products. The platform consists of an MCP331x1D-XX evaluation board, a data capture board (PIC32MZ EF Curiosity Board), and a PC-based Graphical User Interface (GUI) software.

Figure 8-1 and Figure 8-2 show this evaluation tool. This evaluation platform allows users to quickly evaluate the ADC's performance for their specific application requirements.

Note:	Contact Microchip Technology Inc. for the PIC32 MCU firmware and the MCP331x1D-XX Evaluation Kit.

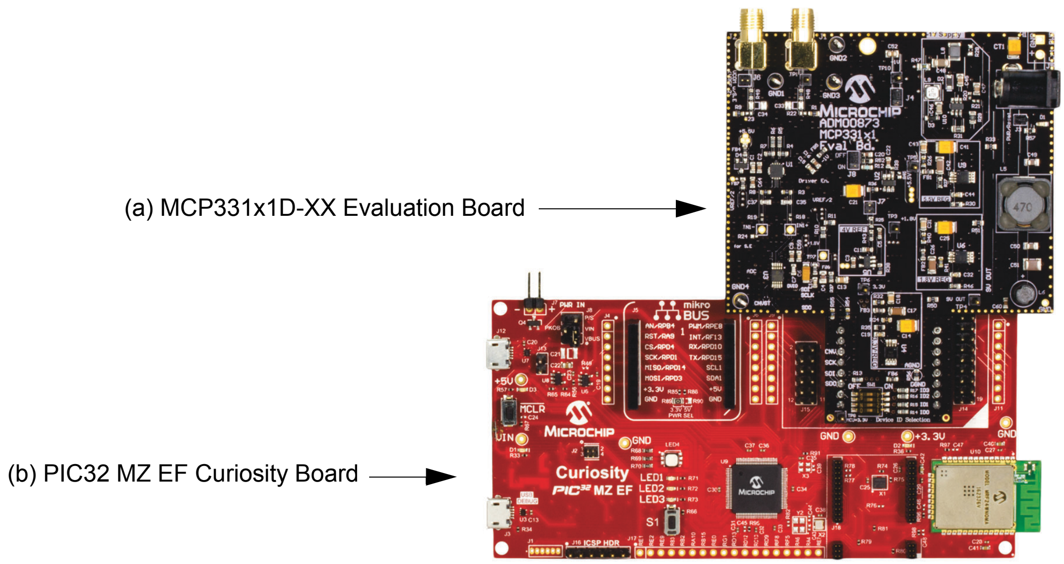


FIGURE 8-1: *MCP331x1D-XX Evaluation Kit.*

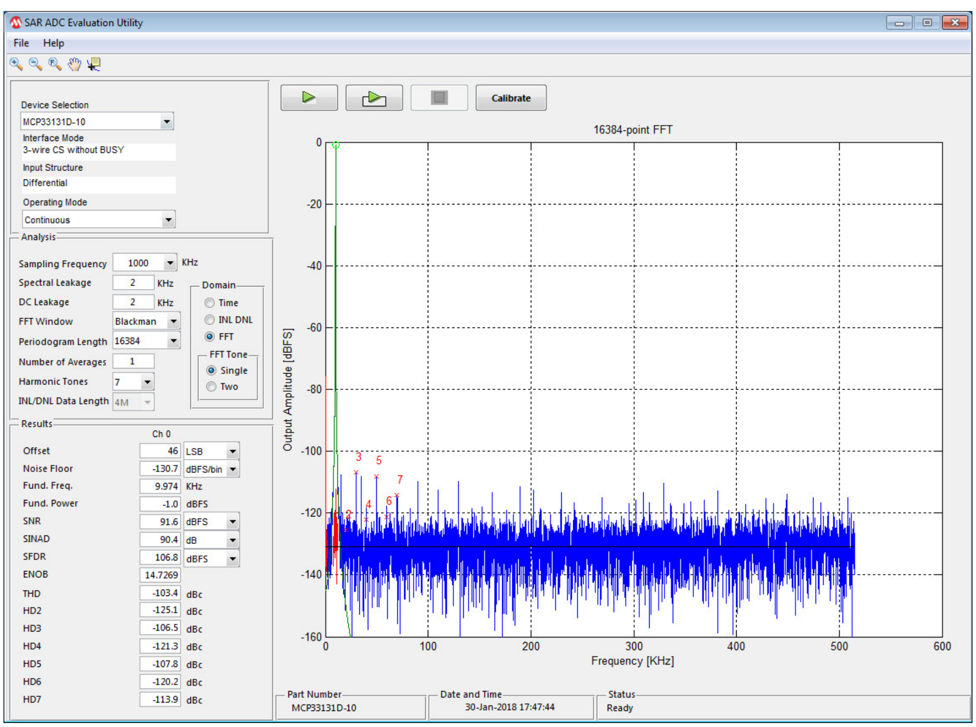


FIGURE 8-2: *PC-Based Graphical User Interface Software.*

8.2 PCB Layout Guidelines:

Microchip provides the schematics and PCB layout of the MCP331x1D-XX Evaluation Board. It is strongly recommended that the user references the example circuits and PCB layouts.

A good schematic with low noise PCB layout is critical for high performing ADC application system designs. A few guidelines are listed below:

- Use low noise supplies (AV_{DD}, DV_{IO}, and V_{REF}).
- All supply voltage pins, including reference voltage, need decoupling capacitors. Decoupling capacitor requirements for each supply pin are shown in **Table 5-1**.
- Use NPO or COG type capacitor for the RC anti-aliasing filters in the analog input network.
- Keep the analog circuit section (analog input driver amplifiers, filters, voltage reference, ADC, etc.) with an analog ground plane, and the digital circuit section (MCU, digital I/O interface) with a digital ground plane. Keep these sections as much apart as possible. This will minimize any digital switching noise coupling into the analog section.
- Connect the analog and digital ground planes at a single point (away from the sensitive analog sections) with a 0 Ω resistor or with a ferrite bead. See Figure 8-3 as an example of separated ground planes.
- Keep the clock and digital output data lines short and away from the sensitive analog sections as much as possible.
- **PCB material and Layers:** Low loss FR-4 material is most commonly used. The following 4 layers are recommended:

  (a) Top Layer: Most of the noise-sensitive analog components are populated on the top layer. Use all unused surface area as ground planes: analog ground plane in analog circuit section and digital ground in digital circuit section. These ground planes need to be tied to the corresponding ground planes in the second and bottom layers using multiple vias.

  (b) 2nd Layer: Use this layer as the ground plane: Analog ground plane under the analog circuit section of the top layer and digital ground plane under the digital circuit section on the top layer. Each ground plane is tied to its corresponding ground plane of top and bottom layers using multiple vias.

  (c) 3rd Layer: This layer is used to distribute various power supplies of the circuits. Use separate trace paths for the power supplies of analog and digital sections. Do not use the same power supply source for both analog and digital circuits.

  (d) Bottom Layer: This layer is mostly used as a solid ground plane: Analog ground plane under the analog circuit section of the top layer and digital ground plane under the digital circuit section on the top layer. Each ground plane is tied to its corresponding ground plane of all layers using multiple vias.

  Figure 8-3 and Figure 8-4 show brief examples of the PCB layout. See more details of the schematics and PCB layout in the MCP331x1D-XX Evaluation Board User's Guide.

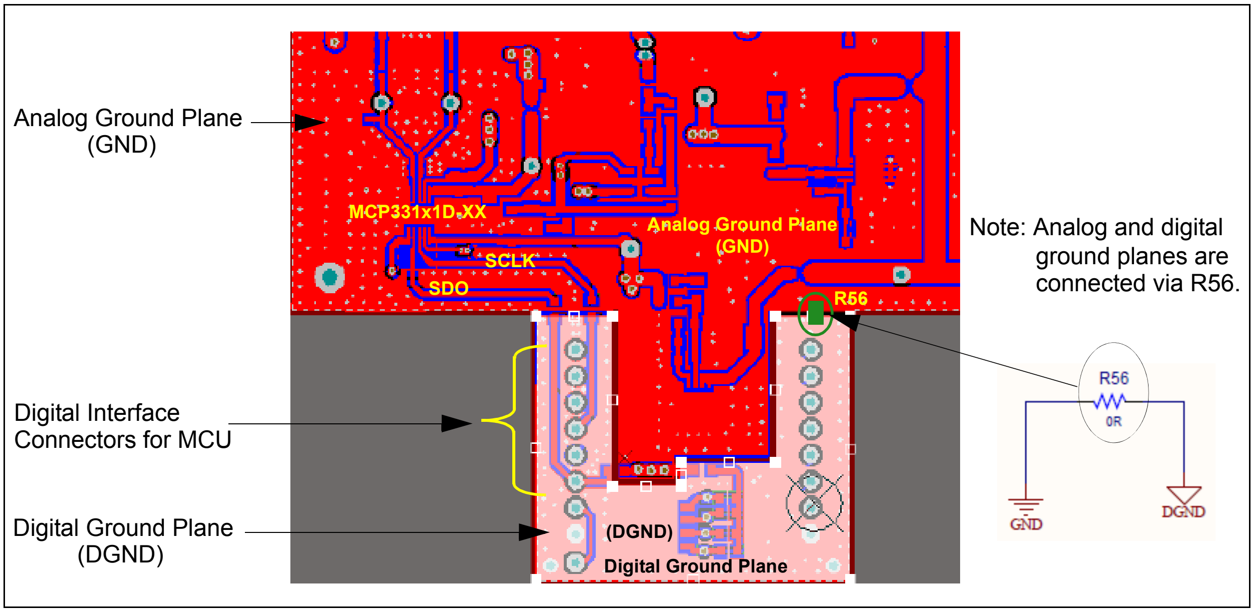
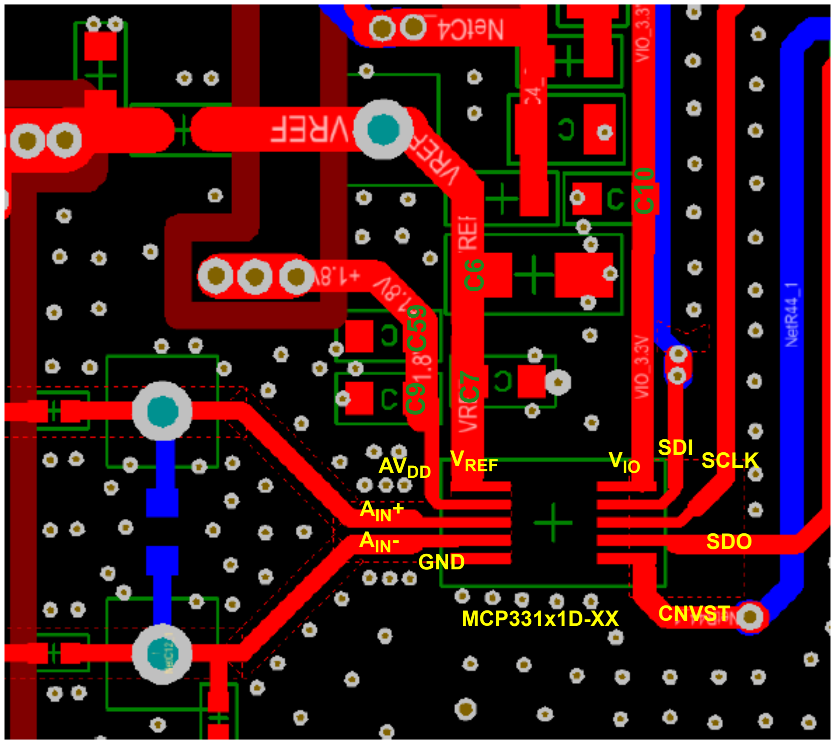
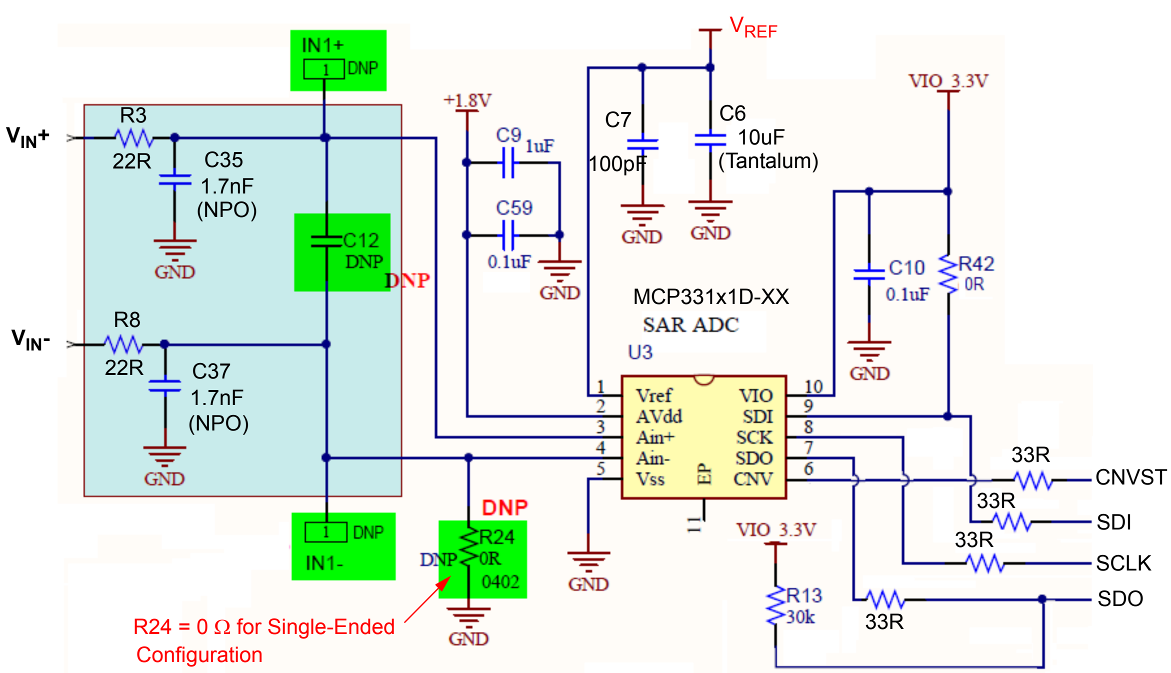


FIGURE 8-3: PCB Layout Example: Analog and Digital Ground Planes



(a) PCB layout example



(b) Schematic example from the MCP331x1D-XX Evaluation Board

FIGURE 8-4: *PCB Layout Example: See more details in the MCP331x1D-XX EV Kit User's Guide.*

NOTES:

9.0 TERMINOLOGY

Analog Input Bandwidth (Full-Power Bandwidth)

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay or Sampling Delay

This is the time delay between the rising edge of the CNVST input and when the input signal is held for a conversion.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. No missing codes to 16-bit resolution indicates that all 65,536 codes (16,384 codes for 14-bit, 4096 codes for 12-bit) must be present over all the operating conditions.

Integral Nonlinearity (INL)

INL is the maximum deviation of each individual code from an ideal straight line drawn from negative full scale through positive full scale.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), below the Nyquist frequency and excluding the power at DC and the first nine harmonics.

EQUATION 9-1:

$$SNR = 10log\left(\frac{P_S}{P_N}\right)$$

SNR is either given in units of dBc (dB to carrier), when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale), when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D) below the Nyquist frequency, but excluding DC:

EQUATION 9-2:

$$SINAD = 10log\left(\frac{P_S}{P_D + P_N}\right) = -10log\left[10^{-\frac{SNR}{10}} - 10^{-\frac{THD}{10}}\right]$$

SINAD is either given in units of dBc (dB to carrier), when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale), when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

EQUATION 9-3:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Gain Error

Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error is usually expressed in LSB or as a percentage of full-scale range (%FSR).

Offset Error

The major carry transition should occur for an analog value of ½ LSB below $A_{IN}+ = A_{IN}-$. Offset error is defined as the deviation of the actual transition from that point.

Temperature Drift

The temperature drift for offset error and gain error specifies the maximum change from the initial (+25°C) value to the value at across the T_{MIN} to T_{MAX} range. The value is normalized by the reference voltage and expressed in µV/°C or ppm/°C.

Maximum Conversion Rate

The maximum clock rate at which parametric testing is performed.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier) or dBFS.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the summed power of the first 13 harmonics (P_D).

EQUATION 9-4:

$$THD = 10log\left(\frac{P_S}{P_D}\right)$$

THD is typically given in units of dBc (dB to carrier). THD is also shown by:

EQUATION 9-5:

$$THD = -20log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_1^2}$$

Where:

V_1 = RMS amplitude of the fundamental frequency

V_1 through V_n = Amplitudes of the second through n^{th} harmonics

Common-Mode Rejection Ratio (CMRR)

Common-mode rejection is the ability of a device to reject a signal that is common to both sides of a differential input pair. The common-mode signal can be an AC or DC signal or a combination of the two. CMRR is measured using the ratio of the differential signal gain to the common-mode signal gain and expressed in dB with the following equation:

EQUATION 9-6:

$$CMRR = 20log\left(\frac{A_{DIFF}}{A_{CM}}\right)$$

Where:

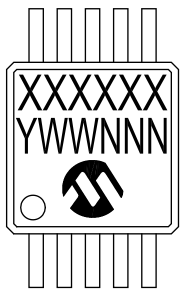
A_{DIFF} = ΔOutput Code/ΔDifferential Voltage

A_{DIFF} = ΔOutput Code/ΔCommon-Mode Voltage

10.0 PACKAGING INFORMATION

10.1 Package Marking Information

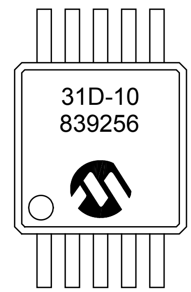
10-Lead MSOP (3x3 mm)



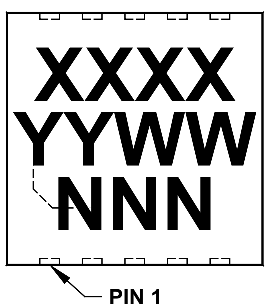
Corresponding Part Number:

31D-10	=	MCP33131D-10
31D-05	=	MCP33131D-05
21D-10	=	MCP33121D-10
21D-05	=	MCP33121D-05
11D-10	=	MCP33111D-10
11D-05	=	MCP33111D-05

Example



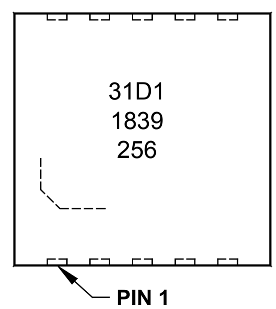
10-Lead TDFN (3x3x0.9 mm)



Corresponding Part Number:

31D1	=	MCP33131D-10
31D0	=	MCP33131D-05
21D1	=	MCP33121D-10
21D0	=	MCP33121D-05
11D1	=	MCP33111D-10
11D0	=	MCP33111D-05

Example

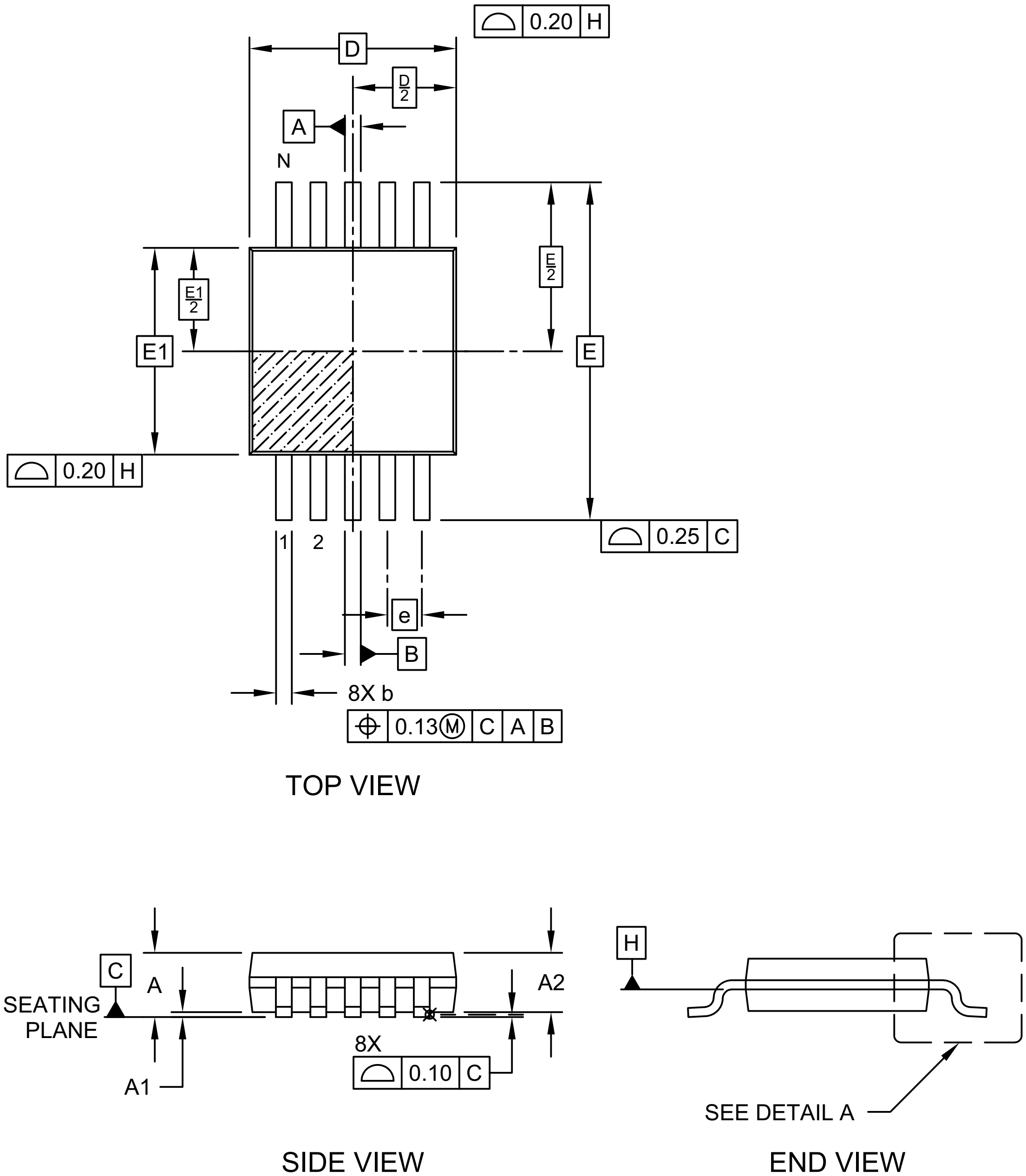


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

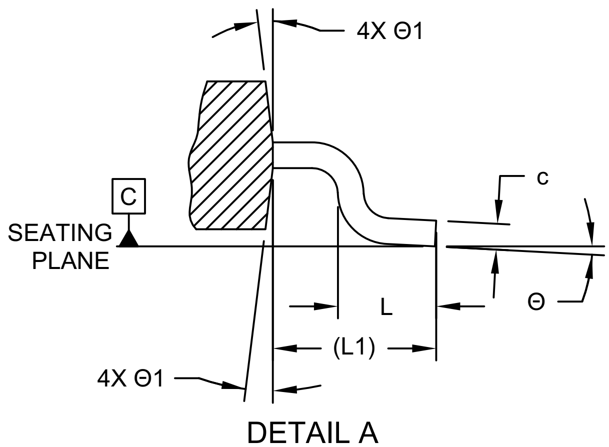
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

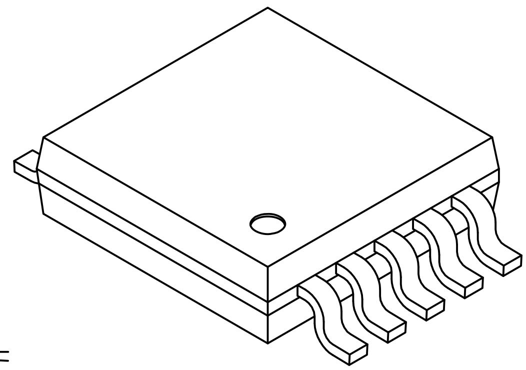


Microchip Technology Drawing C04-021D Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





		Units	MILLIMETERS	
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Mold Draft Angle	Θ	0°	-	8°
Foot Angle	Θ1	5°	-	15°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

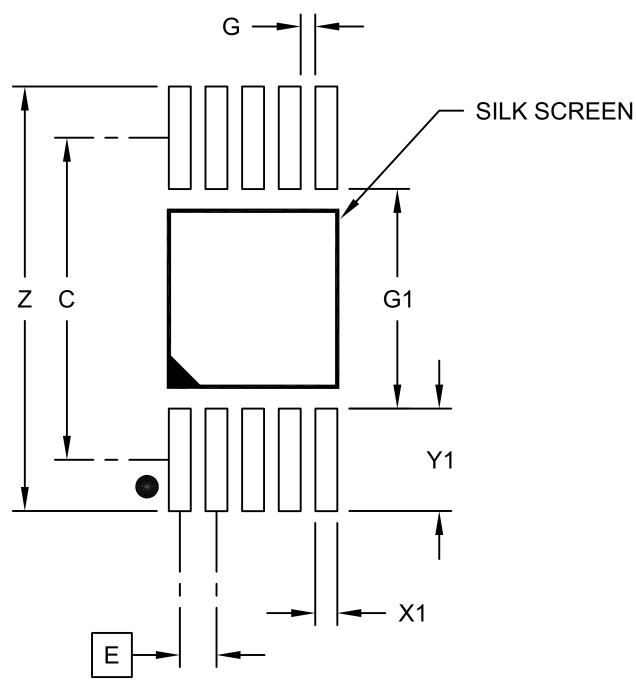
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021D Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

Notes:

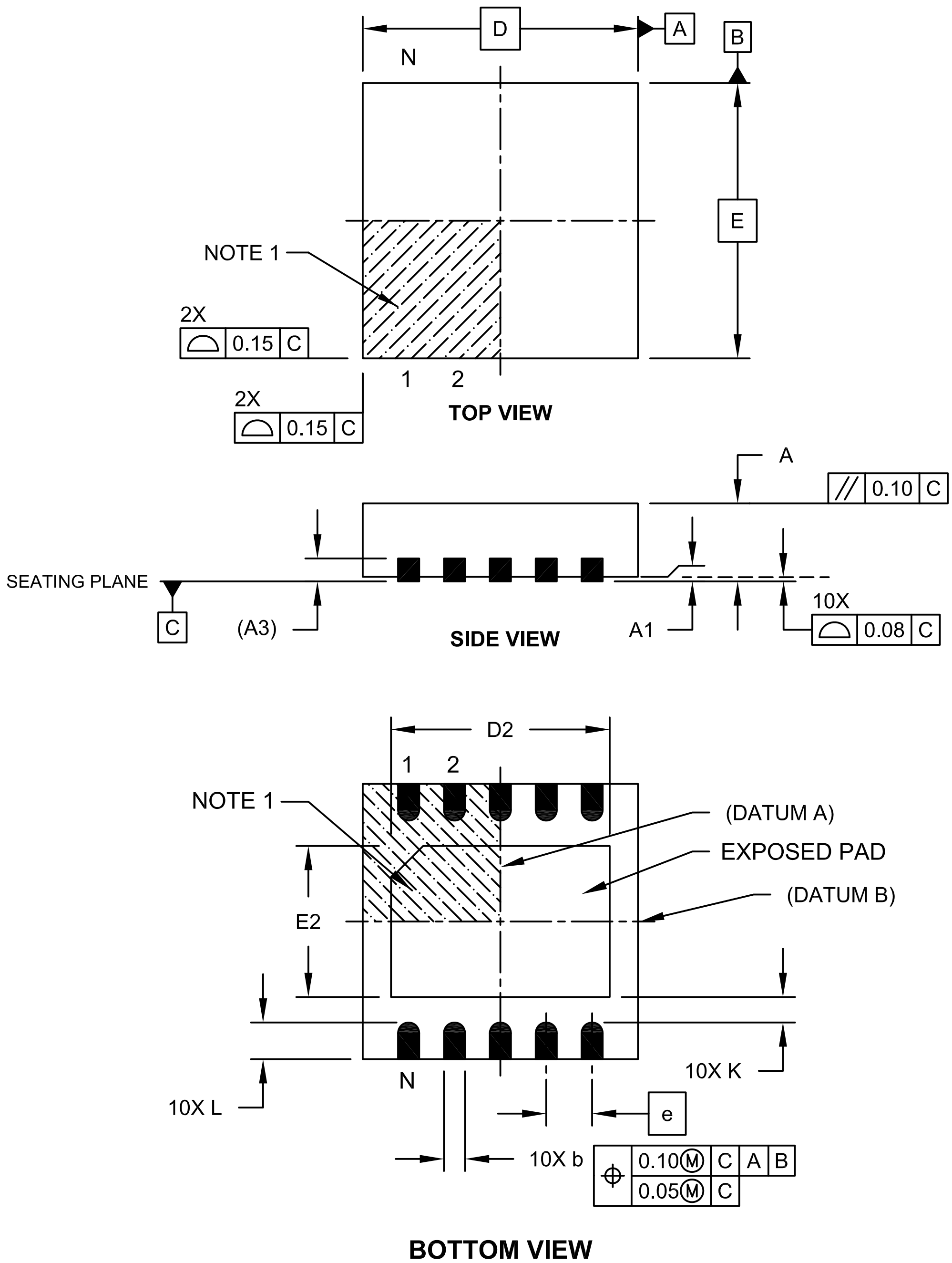
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021B

10-Lead Thin Plastic Dual Flat, No Lead Package (MN) - 3x3x0.8mm Body [TDFN]

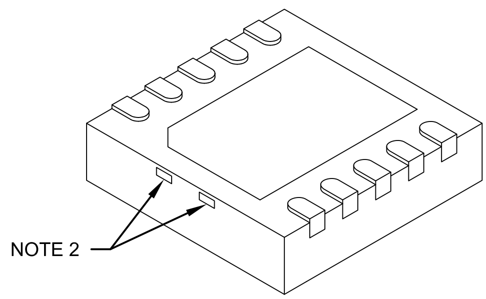
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-185A Sheet 1 of 2

10-Lead Thin Plastic Dual Flat, No Lead Package (MN) - 3x3x0.8mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.30	2.35
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.55	1.65	1.70
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-0185A Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision B (November 2018)

- Added TDFN-10 package release
- Added AEC-Q100 qualification
- Added 500 kSPS family devices (MCP33131D/MCP33121D/MCP33111D-05)
- Minor typographical corrections

Revision A (March 2018)

- Original release of this document

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–XX	X	–X	/XX
Device	Input Type	Sample Rate	Tape and Reel	Temperature Range	Package

Device:	MCP33131D-10:	1 Msps 16-Bit Differential Input SAR ADC
	MCP33121D-10:	1 Msps 14-Bit Differential Input SAR ADC
	MCP33111D-10:	1 Msps 12-Bit Differential Input SAR ADC
	MCP33131D-05:	500 kSPS 16-Bit Differential Input SAR ADC
	MCP33121D-05:	500 kSPS 14-Bit Differential Input SAR ADC
	MCP33111D-05:	500 kSPS 12-Bit Differential Input SAR ADC
Input Type	D: Differential Input	
Sample Rate:	10	= 1 Msps
	05	= 500 kSPS
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel
Temperature Range:	E	= -40°C to +125°C (Extended)
	I	= -40°C to +85°C (Industrial)
Package:	MS	= Plastic Micro Small Outline Package (MSOP), 10-Lead
	MN	= Thin Plastic Dual Flat No Lead Package (TDFN), 10-Lead

Note: Tape and Reel identifier appears only in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) MCP33131D-10-I/MS: 1 Msps, 10LD MSOP, 16-bit device
b) MCP33131D-10T-I/MS: 1 Msps, 10LD MSOP, Tape and Reel, 16-bit device
c) MCP33131D-10-I/MN: 1 Msps, 10LD TDFN, 16-bit device
d) MCP33131D-10T-I/MN: 1 Msps, 10LD TDFN, Tape and Reel, 16-bit device
e) MCP33121D-10-I/MS: 1 Msps, 10LD MSOP, 14-bit device
f) MCP33121D-10T-I/MS: 1 Msps, 10LD MSOP, Tape and Reel, 14-bit device
g) MCP33121D-10-I/MN: 1 Msps, 10LD TDFN, 14-bit device
h) MCP33121D-10T-I/MN: 1 Msps, 10LD TDFN, Tape and Reel, 14-bit device
i) MCP33111D-10-I/MS: 1 Msps, 10LD MSOP, 12-bit device
j) MCP33111D-10T-I/MS: 1 Msps, 10LD MSOP, Tape and Reel, 12-bit device
k) MCP33111D-10-I/MN: 1 Msps, 10LD TDFN, 12-bit device
l) MCP33111D-10T-I/MN: 1 Msps, 10LD TDFN, Tape and Reel, 12-bit device
m) MCP33131D-05-I/MS: 500 kSPS, 10LD MSOP, 16-bit device
n) MCP33131D-05T-I/MS: 500 kSPS, 10LD MSOP, Tape and Reel, 16-bit device
o) MCP33131D-05-I/MN: 500 kSPS, 10LD TDFN, 16-bit device
p) MCP33131D-05T-I/MN: 500 kSPS, 10LD TDFN, Tape and Reel, 16-bit device
q) MCP33121D-05-I/MS: 500 kSPS, 10LD MSOP, 14-bit device
r) MCP33121D-05T-I/MS: 500 kSPS, 10LD MSOP, Tape and Reel, 14-bit device
s) MCP33121D-05-I/MN: 500 kSPS, 10LD TDFN, 14-bit device
t) MCP33121D-05T-I/MN: 500 kSPS, 10LD TDFN, Tape and Reel, 14-bit device
u) MCP33111D-10-I/MS: 500 kSPS, 10LD MSOP, 12-bit device
v) MCP33111D-10T-I/MS: 500 kSPS, 10LD MSOP, Tape and Reel, 12-bit device
w) MCP33111D-10-I/MN: 500 kSPS, 10LD TDFN, 12-bit device
x) MCP33111D-10T-I/MN: 500 kSPS, 10LD TDFN, Tape and Reel, 12-bit device

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