Atmel mXT336T
Revision 1.0

maXTouch 336-node Touchscreen Controller

DATASHEET

Features

- Atmel® maXTouch® Adaptive Sensing Touchscreen Technology
  - Up to 24 X (transmit) lines and 14 Y (receive) lines
  - A maximum of 336 nodes can be allocated to the touchscreen
  - Screen sizes of 5.3 inches diagonal are supported while meeting Microsoft® Phone touch performance requirements
  - Multi-touch support with up to 16 concurrent touches tracked in real time
- Dual-boot OS support for Windows and Android
- Advanced Touch Handling
  - Moisture/Water Compensation
    - No false touch with condensation or water drop up to 22 mm diameter
    - One-finger tracking with condensation or water drop up to 22 mm diameter
  - Stylus Support
    - Supports passive stylus with 1 mm contact diameter, subject to configuration, stack up, and sensor design
  - Glove Support
    - Supports multiple-finger glove touch up to 1.5 mm thickness
    - Supports single-touch gloved operation with various materials up to 5 mm thickness
- Touch Performance
  - Mutual capacitance and self capacitance measurements supported for touch detection
  - Response Times
    - Initial latency <15 ms for first touch from idle, subject to configuration
  - Atmel maXCharger® technology to combat ambient, charger noise, and power-line noise:
    - Up to 240 Vpp between 1 Hz and 1 kHz sinusoidal waveform
    - Up to 20 Vpp between 1 kHz and 1 MHz sinusoidal waveform
  - Scan Speed
    - Typical report rate for 5 touches ≥100 Hz
- Enhanced Algorithms
  - Lens bending algorithms to remove signal distortions
  - Touch suppression algorithms to remove unintentional touches
  - Palm Recovery Algorithm for quick restoration to normal state
- Panel / Cover Glass Support
  - Supports fully-laminated sensors, touch-on-lens stack-ups and on-cell designs
  - Works with PET or glass, including curved profiles
    - Glass from 0.55 mm to 2.5 mm, dependent on screen size and touch size
    - Plastic from 0.2 mm to 1.2 mm, dependent on screen size and touch size
  - Works with all proprietary sensor patterns recommended by Atmel
  - Compatible with True Single Layer designs

- Keys
  - Up to 8 nodes can be allocated as mutual capacitance sensor keys (subject to other configurations)
  - Adjacent Key Suppression® (AKS®) technology is supported for false touch prevention
- Power Saving
  - Programmable timeout for automatic transition from active to idle states
  - Pipelined analog sensing detection and digital processing to optimize system power efficiency
- Application Interfaces
  - I^2C-compatible slave mode: Standard/Fast mode 400 kHz, Fast-plus mode 1 MHz, High-speed mode up to 3.4 MHz
  - Interrupt to indicate when a message is available
- Power Supply
  - Digital (Vdd) 3.3 V nominal
  - Analog (AVdd) 3.3 V nominal
  - Host interface I/O voltage (VddIO) 1.8 V to 3.3 V nominal
  - High voltage internal X line drive (XVdd) = 2 × Vdd (6.6 V), with internal voltage doubler
- Packages
  - 56-pin UFQFN 6 × 6 × 0.6 mm, 0.35 mm pitch
  - 64-ball UFBGA 5 × 5 × 0.6 mm, 0.5 mm pitch
  - 72-ball UFBGA 6 × 6 × 0.6 mm, 0.5 mm pitch
- Environmental Conditions
  - Operating temperature –40°C to +85°C

Table of Contents

1. Overview of mXT336T

1.1 Introduction

The Atmel maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer applications. The mXT336T features the latest generation of Atmel Adaptive Sensing technology that utilizes a hybrid mutual- and self-capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Patented capacitive sensing method** – The mXT336T uses a unique charge-transfer acquisition engine to implement the Atmel-patented QMatrix® capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track number of individual finger touches with a high degree of accuracy in the shortest response time.
- **Capacitive Touch Engine (CTE)** – The mXT336T features an acquisition engine, which uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Atmel proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.
- **Touch detection** – The mXT336T allows for both mutual- and self-capacitance measurements, with the self-capacitance measurements being used to augment the mutual-capacitance measurements to produce reliable touch information.

  When self-capacitance measurements are enabled, touch classification is achieved using both mutual- and self-capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

  During idle mode, the device performs self-capacitance touch scans. When a touch is detected, the device starts performing mutual-capacitance touch scans as well as self capacitance scans.

  Mutual-capacitance touch data is used wherever possible to classify touches as this has greater granularity than self-capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual-capacitance touch data. If the self-capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual-capacitance touch data is available.

  Self-capacitance measurements, on the other hand, allow for the detection of single touches in extreme case, such as single thick-glove touches, when touches can only be detected by self-capacitance data and may be missed by mutual-capacitance touch detection.
- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware that combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of charger and LCD noise.
- **Processing power** – The main CPU has two powerful microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing, postprocessing and housekeeping to be partitioned in an efficient and flexible way.
- **Interpreting user intention** – The Atmel hybrid mutual- and self-capacitance method provides unambiguous multitouch performance. Algorithms in the mXT336T provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touch triggered by ambient noise or conductive material on the sensor surface, such as water. The suppression of unintentional touches from the user's gripping fingers, resting palm or touching cheek or ear also help ensure that the user's intentions are correctly interpreted.

2. Connection and Configuration Information

2.1 Pin Configuration – UFQFN 56 Pins

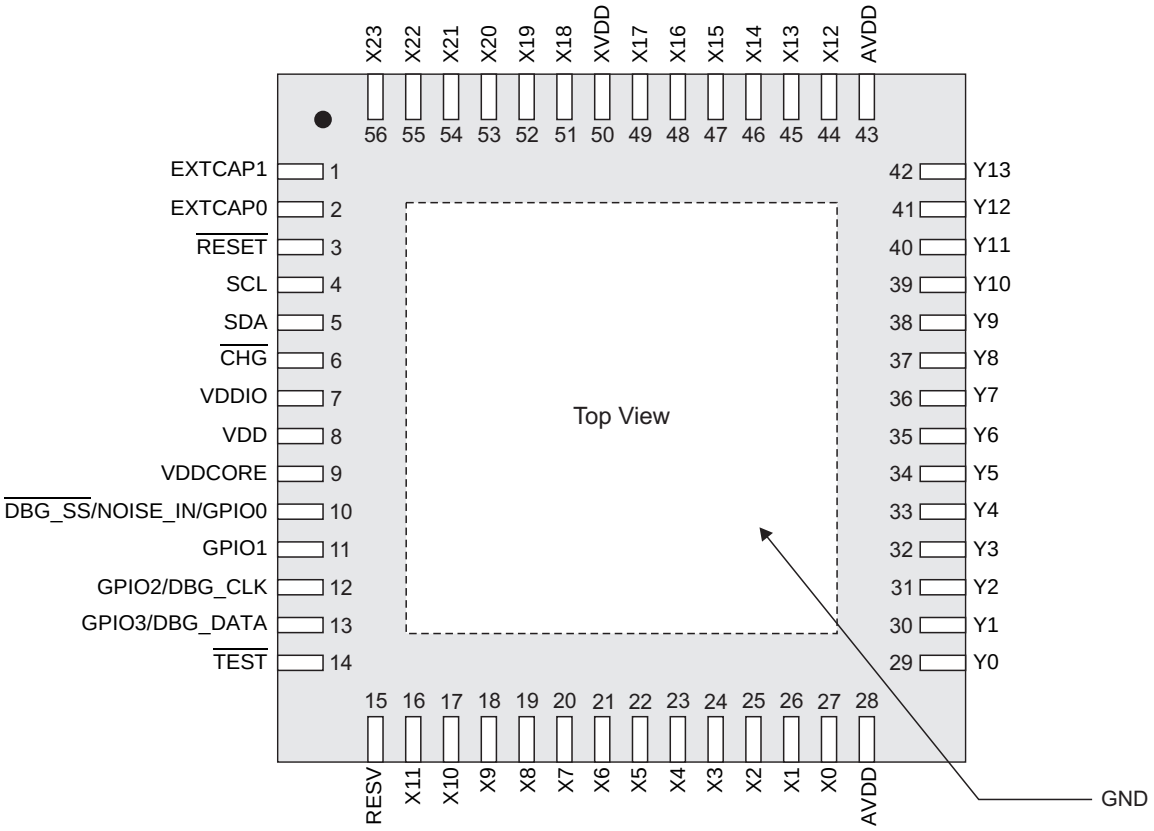


Table 2-1. Pin Listing – UFQFN 56 Pins

Pin	Name	Type	Description	If Unused...
1	EXTCAP1	P	Normal mode – leave open Voltage doubler mode – connect to EXTCAP0 via capacitor	Leave open
2	EXTCAP0	P	Normal mode – leave open Voltage doubler mode – connect to EXTCAP1 via capacitor	Leave open
3	$\overline{\text{RESET}}$	I	Reset low. Connection to host system is recommended	Pull up to VddIO
4	SCL	OD	Serial Interface clock	–
5	SDA	OD	Serial Interface Data	–
6	$\overline{\text{CHG}}$	OD	State change interrupt Note: Briefly set (~100 ms) as an input after power-up/reset for diagnostic purposes	Pull up to VddIO
7	VDDIO	P	Digital IO interface power	–
8	VDD	P	Digital power	–
9	VDDCORE	P	Digital core power	–
10	$\overline{\text{DBG\_SS}}$ NOISE_IN GPIO0	I/O	Debug SS line Noise present input General purpose I/O	Input: GND Output: leave open
11	GPIO1	I/O	General purpose I/O	Input: GND Output: leave open
12	GPIO2 DBG_CLK	I/O	General purpose I/O Debug Clock	Input: GND Output: leave open
13	GPIO3 DBG_DATA	I/O	General purpose I/O Debug Data	Input: GND Output: leave open
14	$\overline{\text{TEST}}$	–	Reserved for factory use; always pull up to VddIO	Pull up to VddIO
15	RESV	–	Reserved for future use	Connect to GND
16	X11	S	X line connection	Leave open
17	X10	S	X line connection	Leave open
18	X9	S	X line connection	Leave open
19	X8	S	X line connection	Leave open
20	X7	S	X line connection	Leave open
21	X6	S	X line connection	Leave open
22	X5	S	X line connection	Leave open
23	X4	S	X line connection	Leave open
24	X3	S	X line connection	Leave open
25	X2	S	X line connection	Leave open

Table 2-1. Pin Listing – UFQFN 56 Pins

Pin	Name	Type	Description	If Unused...
26	X1	S	X line connection	Leave open
27	X0	S	X line connection	Leave open
28	AVDD	P	Analog power	–
29	Y0	S	Y line connection	Leave open
30	Y1	S	Y line connection	Leave open
31	Y2	S	Y line connection	Leave open
32	Y3	S	Y line connection	Leave open
33	Y4	S	Y line connection	Leave open
34	Y5	S	Y line connection	Leave open
35	Y6	S	Y line connection	Leave open
36	Y7	S	Y line connection	Leave open
37	Y8	S	Y line connection	Leave open
38	Y9	S	Y line connection	Leave open
39	Y10	S	Y line connection	Leave open
40	Y11	S	Y line connection	Leave open
41	Y12	S	Y line connection	Leave open
42	Y13	S	Y line connection	Leave open
43	AVDD	P	Analog power	–
44	X12	S	X line connection	Leave open
45	X13	S	X line connection	Leave open
46	X14	S	X line connection	Leave open
47	X15	S	X line connection	Leave open
48	X16	S	X line connection	Leave open
49	X17	S	X line connection	Leave open
50	XVDD	P	X line drive power	Leave open
51	X18	S	X line connection	Leave open
52	X19	S	X line connection	Leave open
53	X20	S	X line connection	Leave open
54	X21	S	X line connection	Leave open

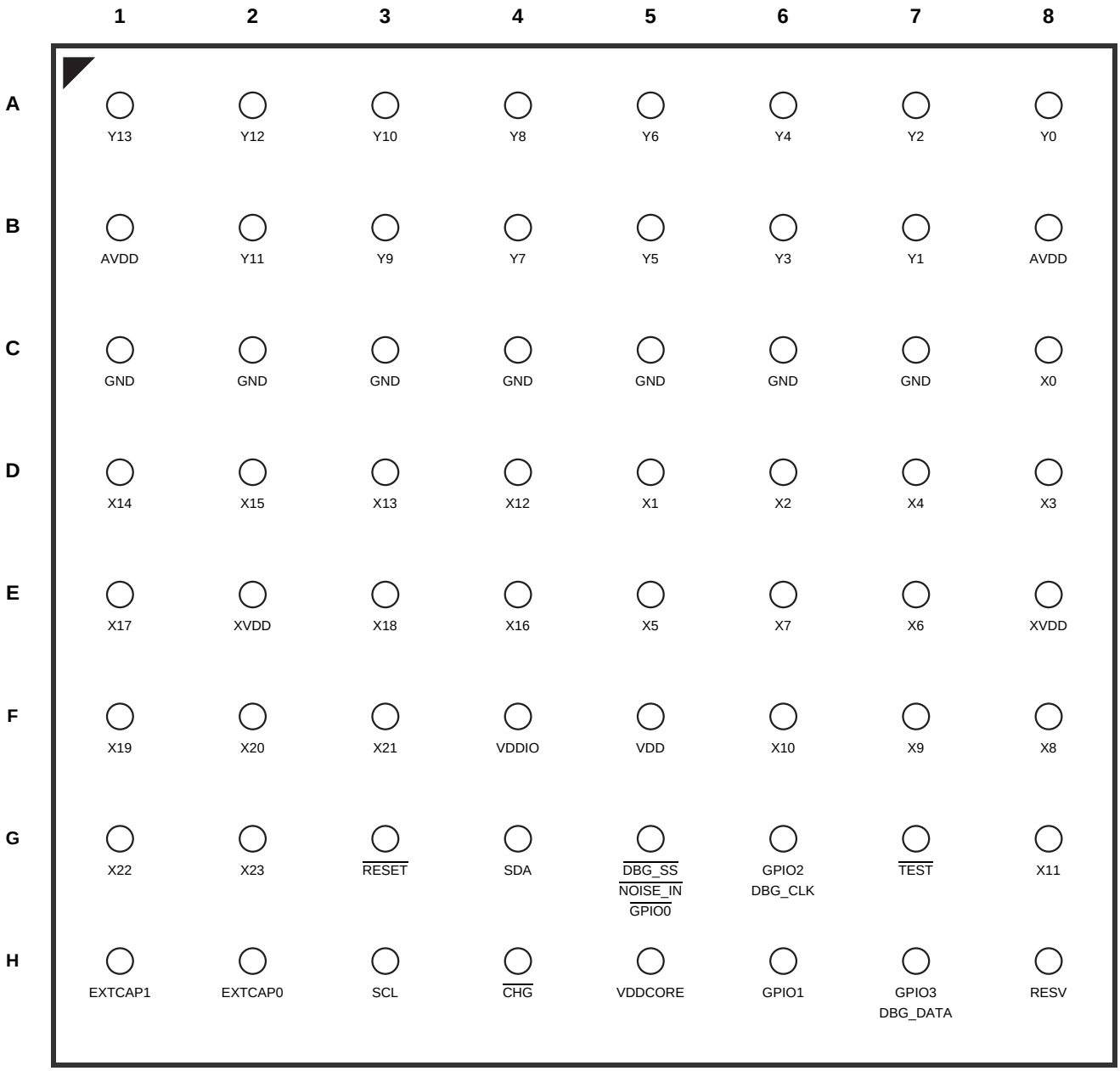
Table 2-1. Pin Listing – UFQFN 56 Pins

Pin	Name	Type	Description	If Unused...
55	X22	S	X line connection	Leave open
56	X23	S	X line connection	Leave open
Pad	GND	P	Exposed pad must be connected to GND	–

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

2.2 Pin Configuration – UFBGA 64 Balls



Top View

Table 2-2. Pin Listing – UFBGA 64 Balls

Pin	Name	Type	Description	If Unused...
A1	Y13	S	Y line connection	Leave open
A2	Y12	S	Y line connection	Leave open
A3	Y10	S	Y line connection	Leave open
A4	Y8	S	Y line connection	Leave open
A5	Y6	S	Y line connection	Leave open
A6	Y4	S	Y line connection	Leave open
A7	Y2	S	Y line connection	Leave open
A8	Y0	S	Y line connection	Leave open
B1	AVDD	P	Analog power	–
B2	Y11	S	Y line connection	Leave open
B3	Y9	S	Y line connection	Leave open
B4	Y7	S	Y line connection	Leave open
B5	Y5	S	Y line connection	Leave open
B6	Y3	S	Y line connection	Leave open
B7	Y1	S	Y line connection	Leave open
B8	AVDD	P	Analog power	–
C1	GND	P	Ground	–
C2	GND	P	Ground	–
C3	GND	P	Ground	–
C4	GND	P	Ground	–
C5	GND	P	Ground	–
C6	GND	P	Ground	–
C7	GND	P	Ground	–
C8	X0	S	X line connection	Leave open
D1	X14	S	X line connection	Leave open
D2	X15	S	X line connection	Leave open
D3	X13	S	X line connection	Leave open
D4	X12	S	X line connection	Leave open
D5	X1	S	X line connection	Leave open
D6	X2	S	X line connection	Leave open
D7	X4	S	X line connection	Leave open
D8	X3	S	X line connection	Leave open

Table 2-2. Pin Listing – UFBGA 64 Balls

Pin	Name	Type	Description	If Unused...
E1	X17	S	X line connection	Leave open
E2	XVDD	P	X line drive power	Leave open
E3	X18	S	X line connection	Leave open
E4	X16	S	X line connection	Leave open
E5	X5	S	X line connection	Leave open
E6	X7	S	X line connection	Leave open
E7	X6	S	X line connection	Leave open
E8	XVDD	P	X line drive power	Leave open
F1	X19	S	X line connection	Leave open
F2	X20	S	X line connection	Leave open
F3	X21	S	X line connection	Leave open
F4	VDDIO	P	Digital IO interface power	–
F5	VDD	P	Digital power	–
F6	X10	S	X line connection	Leave open
F7	X9	S	X line connection	Leave open
F8	X8	S	X line connection	Leave open
G1	X22	S	X line connection	Leave open
G2	X23	S	X line connection	Leave open
G3	$\overline{\text{RESET}}$	I	Reset low. Connection to host system is recommended	Pull up to VddIO
G4	SDA	OD	Serial Interface Data	–
G5	$\overline{\text{DBG\_SS}}$ NOISE_IN GPIO0	I/O	Debug SS line Noise present input General purpose I/O	Input: GND Output: leave open
G6	GPIO2 DBG_CLK	I/O	General purpose I/O Debug Clock	Input: GND Output: leave open
G7	$\overline{\text{TEST}}$	–	Reserved for factory use; always pull up to VddIO	Pull up to VddIO
G8	X11	S	X line connection	Leave open
H1	EXTCAP1	P	Connect to EXTCAP0 via capacitor; see schematic notes	Leave open
H2	EXTCAP0	P	Connect to EXTCAP1 via capacitor; see schematic notes	Leave open
H3	SCL	OD	Serial Interface Clock	–
H4	$\overline{\text{CHG}}$	OD	State change interrupt Note: Briefly set (~100 ms) as an input after power-up/reset for diagnostic purposes	Pull up to VddIO
H5	VDDCORE	P	Digital core power	–

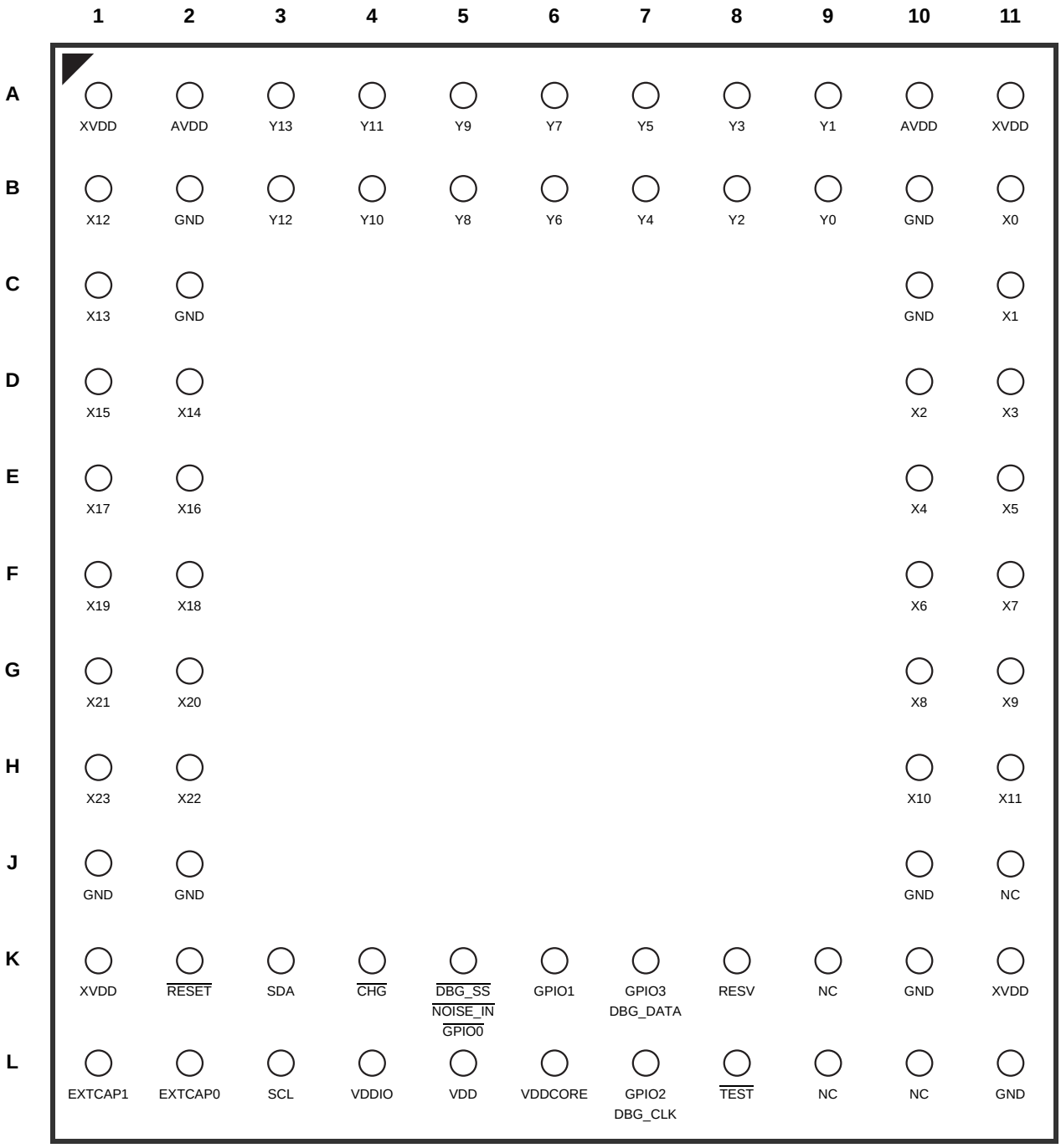
Table 2-2. Pin Listing – UFBGA 64 Balls

Pin	Name	Type	Description	If Unused...
H6	GPIO1	I/O	General purpose I/O	Input: GND Output: leave open
H7	GPIO3 DBG_DATA	I/O	General purpose I/O Debug Data	Input: GND Output: leave open
H8	RESV	–	Reserved for future use	Connect to GND

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

2.3 Pin Configuration – UFBGA 72 Balls



Top View

Table 2-3. Pin Listing – UFBGA 72 Balls

Pin	Name	Type	Description	If Unused...
A1	XVDD	P	X line drive power	Leave open
A2	AVDD	P	Analog power	–
A3	Y13	S	Y line connection	Leave open
A4	Y11	S	Y line connection	Leave open
A5	Y9	S	Y line connection	Leave open
A6	Y7	S	Y line connection	Leave open
A7	Y5	S	Y line connection	Leave open
A8	Y3	S	Y line connection	Leave open
A9	Y1	S	Y line connection	Leave open
A10	AVDD	P	Analog power	–
A11	XVDD	P	X line drive power	Leave open
B1	X12	S	X line connection	Leave open
B2	GND	P	Ground	–
B3	Y12	S	Y line connection	Leave open
B4	Y10	S	Y line connection	Leave open
B5	Y8	S	Y line connection	Leave open
B6	Y6	S	Y line connection	Leave open
B7	Y4	S	Y line connection	Leave open
B8	Y2	S	Y line connection	Leave open
B9	Y0	S	Y line connection	Leave open
B10	GND	P	Ground	–
B11	X0	S	X line connection	Leave open
C1	X13	S	X line connection	Leave open
C2	GND	P	Ground	–
…				
C10	GND	P	Ground	–
C11	X1	S	X line connection	Leave open
D1	X15	S	X line connection	Leave open
D2	X14	S	X line connection	Leave open
…				
D10	X2	S	X line connection	Leave open
D11	X3	S	X line connection	Leave open

Table 2-3. Pin Listing – UFBGA 72 Balls (Continued)

Pin	Name	Type	Description	If Unused...
E1	X17	S	X line connection	Leave open
E2	X16	S	X line connection	Leave open
…				
E10	X4	S	X line connection	Leave open
E11	X5	S	X line connection	Leave open
F1	X19	S	X line connection	Leave open
F2	X18	S	X line connection	Leave open
…				
F10	X6	S	X line connection	Leave open
F11	X7	S	X line connection	Leave open
G1	X21	S	X line connection	Leave open
G2	X20	S	X line connection	Leave open
…				
G10	X8	S	X line connection	Leave open
G11	X9	S	X line connection	Leave open
H1	X23	S	X line connection	Leave open
H2	X22	S	X line connection	Leave open
…				
H10	X10	S	X line connection	Leave open
H11	X11	S	X line connection	Leave open
J1	GND	P	Ground	–
J2	GND	P	Ground	–
…				
J10	GND	P	Ground	–
J11	NC	–	No connection	–
K1	XVDD	P	X line drive power	Leave open
K2	$\overline{\text{RESET}}$	I	Reset low. Connection to host system is recommended	Pull up to VddIO
K3	SDA	OD	Serial Interface Data	–
K4	$\overline{\text{CHG}}$	OD	State change interrupt Note: Briefly set (~100 ms) as an input after power-up/reset for diagnostic purposes	Pull up to VddIO
K5	$\overline{\text{DBG\_SS}}$ NOISE_IN GPIO0	I/O	Debug SS line Noise present input General purpose I/O	Input: GND Output: leave open

Table 2-3. Pin Listing – UFBGA 72 Balls (Continued)

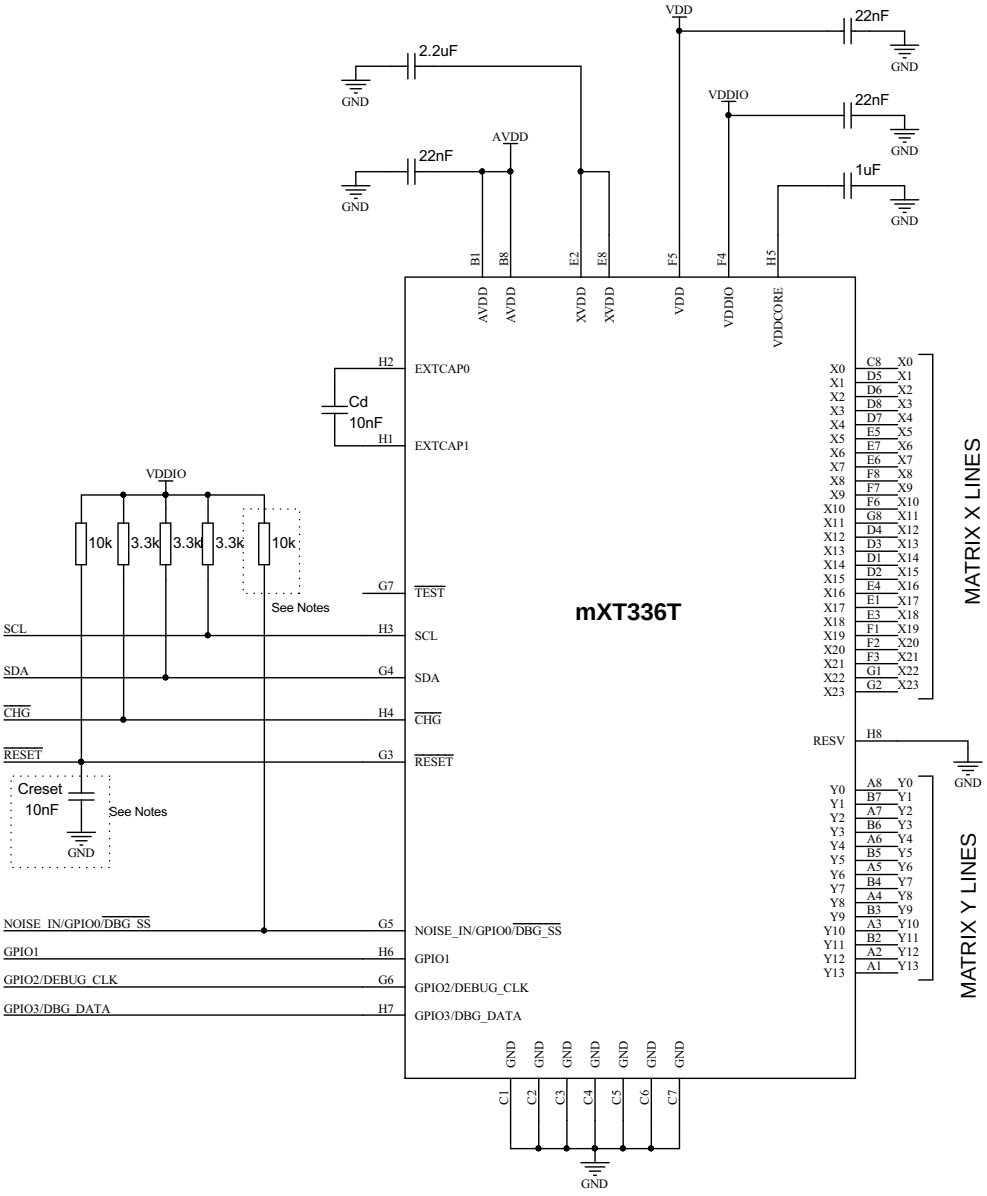
Pin	Name	Type	Description	If Unused...
K6	GPIO1	I/O	General purpose I/O	Input: GND Output: leave open
K7	GPIO3 DBG_DATA	I/O	General purpose I/O Debug Data	Input: GND Output: leave open
K8	RESV	–	Reserved for future use	Connect to GND
K9	NC	–	No connection	–
K10	GND	P	Ground	–
K11	XVDD	P	X line drive power	Leave open
L1	EXTCAP1	P	Normal mode – leave open Voltage doubler mode – connect to EXTCAP0 via capacitor	Leave open
L2	EXTCAP0	P	Normal mode – leave open Voltage doubler mode – connect to EXTCAP1 via capacitor	Leave open
L3	SCL	OD	Serial Interface clock	–
L4	VDDIO	P	Digital IO interface power	–
L5	VDD	P	Digital power	–
L6	VDDCORE	P	Digital core power	–
L7	GPIO2 DBG_CLK	I/O	General purpose I/O Debug Clock	Input: GND Output: leave open
L8	$\overline{\text{TEST}}$	–	Reserved for factory use; always pull up to VddIO	Pull up to VddIO
L9	NC	–	No connection	–
L10	NC	–	No connection	–
L11	GND	P	Ground	–

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

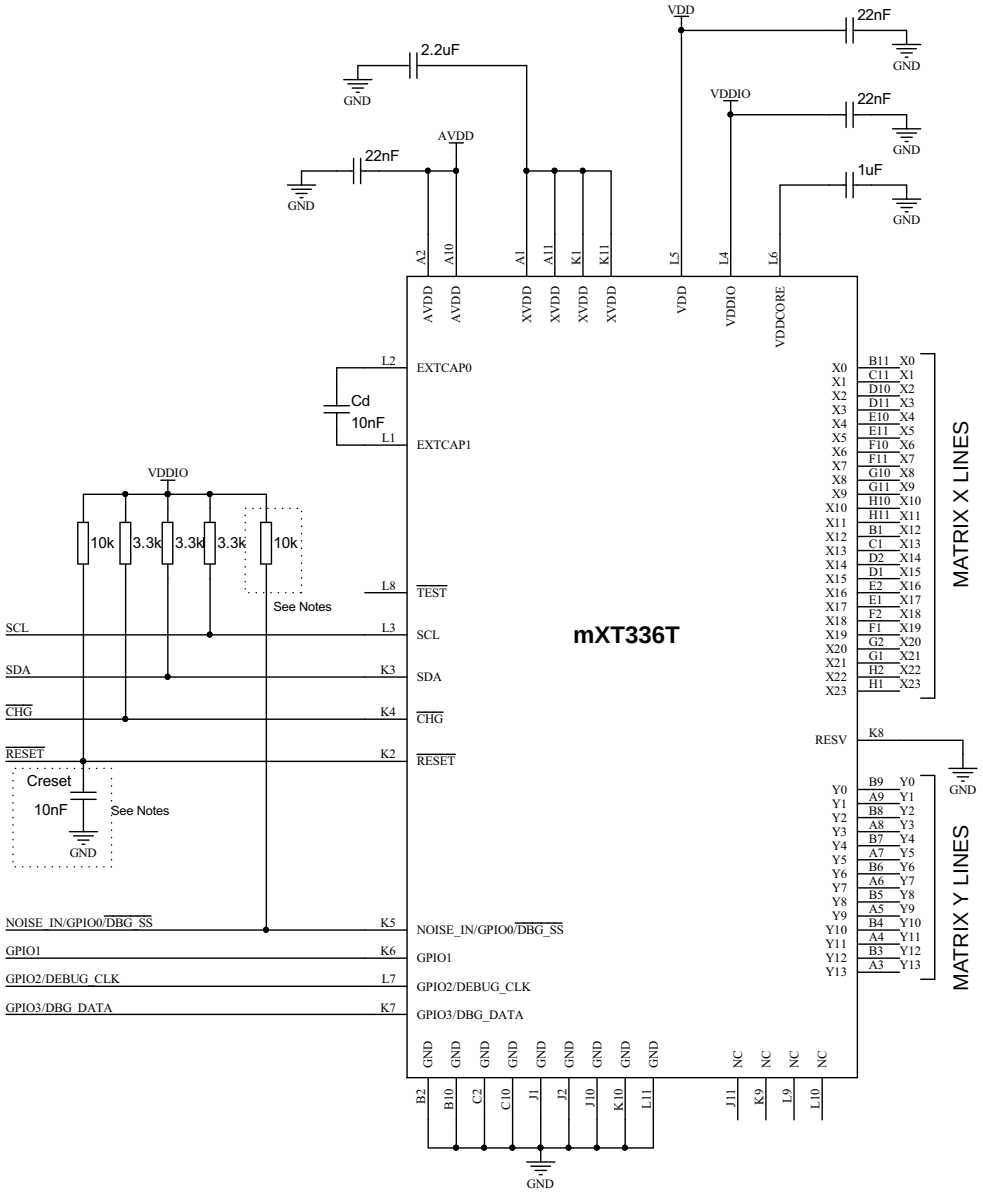
3. Schematics

3.1 64-ball UFBGA

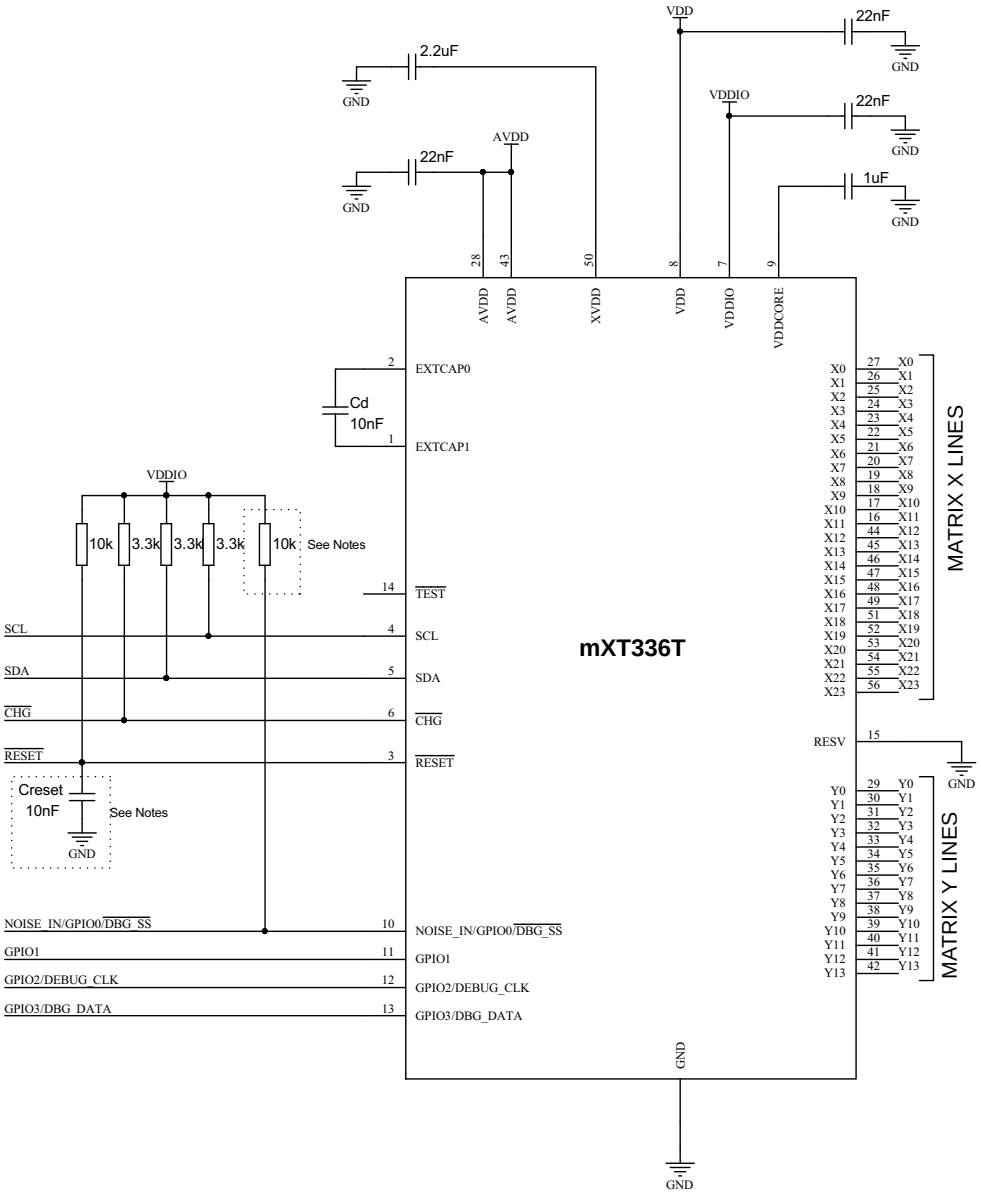


See Section 3.4 “Schematic Notes” on page 22

3.2 72-ball UFBGA



3.3 56-pin UFQFN



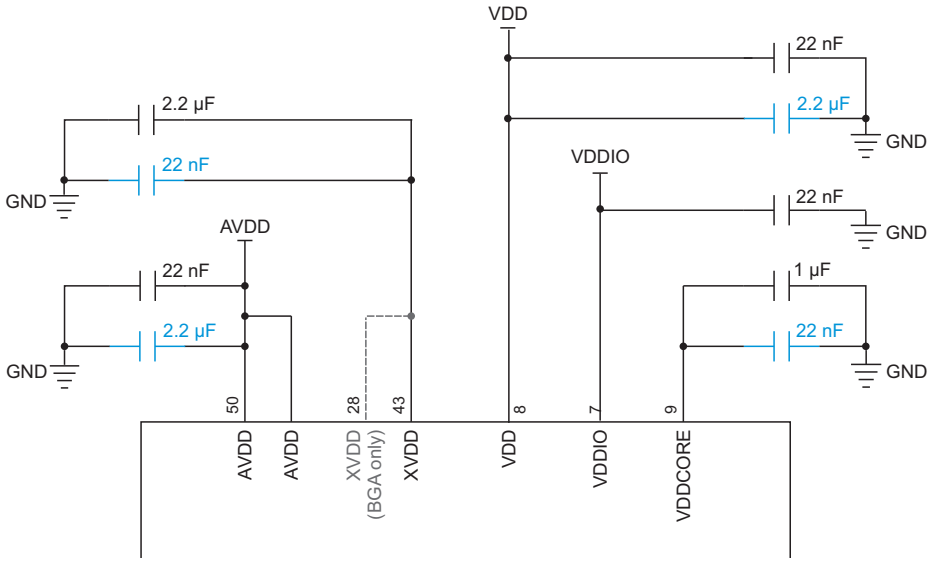
See Section 3.4 “Schematic Notes” on page 22

3.4 Schematic Notes

3.4.1 Decoupling capacitors:

1. All decoupling capacitors must be X7R or X5R and placed <5 mm away from the pins for which they act as decoupling capacitors.
2. The schematics show the minimum capacitors required. If the ball configuration means that sharing a decoupling capacitor is not possible, then the number of capacitors should be increased.
3. If the device is placed on the system board, the minimum number of capacitors required is as shown in the schematics on page 19 and page 21. Note that this requires that the voltage regulator supplies for Avdd/Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is < 50 mm.
4. If an active tail design is used, the voltage regulators are likely to be some distance from the device and it may be necessary to implement additional decoupling. In this case, a parallel combination of capacitors is recommended to give high and low frequency filtering, as shown in Figure 3-1.

Figure 3-1. Additional Recommended Decoupling Capacitors



NOTE: Recommended additional decoupling capacitors are shown in blue

3.4.2 VDDCORE

VDDCore is internally generated from the Vdd 3.3 V power supply. To guarantee stability of the internal voltage regulator, a minimum value of 1 µF must be used for decoupling on VDDCORE.

3.4.3 $\overline{\text{DBG\_SS}}$ Line

The $\overline{\text{DBG\_SS}}$ line shares the same pin as GPIO0. Only one of these two functions can be chosen and the circuit should be designed accordingly.

The pull-up resistor R1 in the schematics is optional and should be present only if the ball/pin is used as $\overline{\text{DBG\_SS}}$. For more information refer to Application Note: *QTAN0050 Using the maXTouch Debug Port*.

3.4.4 $\overline{\text{RESET}}$ Line

The $\overline{\text{RESET}}$ line is shown on the schematics with a 10 nF capacitor to ground. This capacitor is optional but may help if ESD issues are encountered.

3.4.5 Voltage Doubler

To use XVdd voltage doubler:

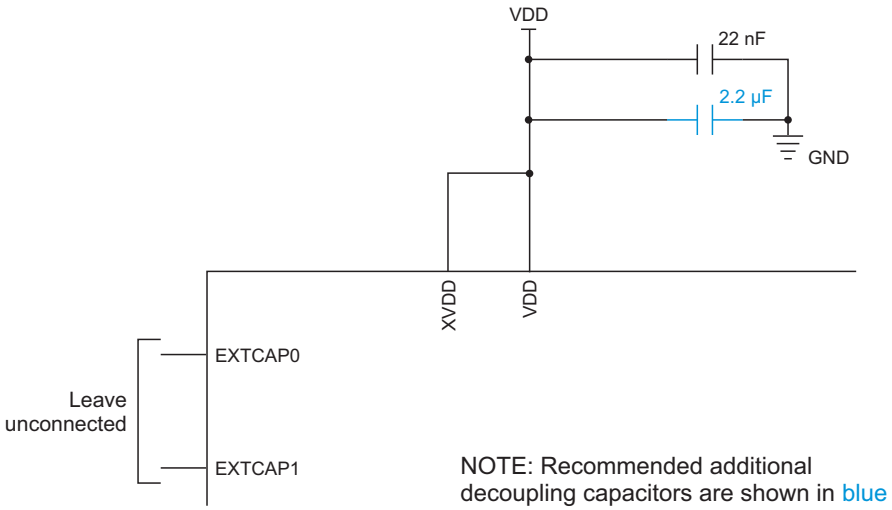
1. EXTCAP0 must be connected to EXTCAP1 via a capacitor (Cd) to provide XVdd voltage doubler mode.
2. The recommended value of the capacitor is 10 nF. Other values can be used if necessary after consultation with Atmel.

If XVdd voltage doubler is not required:

1. The capacitor can be omitted and EXTCAP0 and EXTCAP1 left unconnected.
2. XVDD line(s) should be connected to VDD.

   These modifications are shown in Figure 3-2.

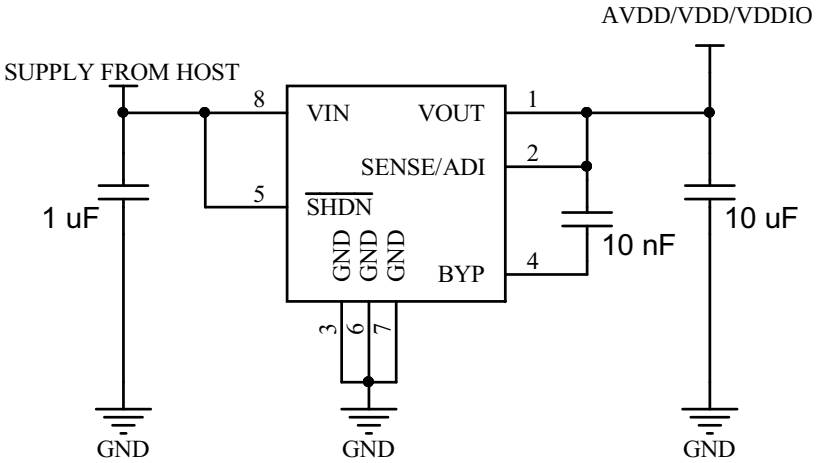
Figure 3-2. No voltage Doubler



3.4.6 Low Drop-Out Voltage Regulators (LDOs)

In applications where the VddIO supply is at the same voltage level as Vdd and AVdd (that is, 3.3 V) it is permissible to use a single LDO for all supply rails (AVDD/VDD/VDDIO). A suitable circuit is shown in Figure 3-3.

Figure 3-3. Low Drop-Out Regulators



Where poor or inadequate tracking or decoupling leads to high noise levels on the supply rails, Atmel recommends that a separate low drop-out voltage regulator supply is used for the AVdd supply.

See Section 4.4 on page 25 for further details. A list of approved regulators is given in Table 4-1 on page 26.

4. Circuit Components

4.1 Decoupling Capacitors

Each power supply pin requires decoupling as described in Section 3.4 on page 22. The capacitors should be ceramic X7R or X5R.

The PCB traces connecting the decoupling capacitors to the pins of the device must not exceed 10 mm in length. This limits any stray inductance that would reduce filtering effectiveness.

4.2 I^2C Line Pull-up Resistors

The values for pull-up resistors on SDA and SCL need to be chosen to ensure rise times are within I^2C specification – if the rise time is too long the overall clock rate will be reduced.

If using a VddIO at the low end of the allowable range it is likely that the pull-up resistor values will need to be reduced from those shown on the schematic.

4.3 Supply Quality

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Always operate the device with a well-regulated and clean AVdd supply. It supplies the sensitive analog stages in the device.

4.4 Suggested Voltage Regulators

An LDO regulator should be chosen that provides adequate output capability, low noise, good load regulation and step response.

Suitable fixed output LDO devices are shown in Table 4-1 on page 26.

With a single regulator, PCB layout is more critical than with multiple LDO regulators, and special care with the PCB layout should be taken. See Section 10.5 on page 44 for information concerning PCB design with a single LDO.

4.4.1 Multiple Voltage Regulator Supply

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Atmel recommends that the supply for the analog section of the board be supplied by a regulator that is separate from the logic supply. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

4.4.2 Suggested Voltage Regulators

The voltage regulators listed in Table 4-1 have been tested and found to work well with the mXT336T.

Table 4-1. Suitable LDO Regulators

Manufacturer	Device	Current Rating (mA)
Analog Devices	ADP122/ADP123	300
Diodes Inc.	AP2125	300
Diodes Inc.	AP7335	300
Linear Technology	LT1763CS8-3.3	500
NXP	LD6836	300
Texas Instruments	LP2981	100
Texas Instruments	LP3981	300
Texas Instruments	LP5996	150 / 300

1. Some manufacturers claim that minimal or no capacitance is required for correct regulator operation. However, in all cases, a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices should be used. The manufacturer's datasheets should always be referred to when selecting capacitors for these devices and the typical recommended values, types and dielectrics adhered to.

4.4.3 LDO Selection Criteria

The LDO devices in Table 4-1 have been proved to provide satisfactory performance in Atmel maxTouch controllers, however, if it is desired to use an alternative LDO, certain performance criteria should be verified before using the device. These are:

- Stable with low value multi-layer ceramic capacitors on input and output – actual values will be device dependent, but it is good design practice to use values greater than the minimum specified in the LDO regulator data sheet
- Low output noise – less than 100 µV RMS over the range 10 Hz to 1 MHz
- Good load transient response – this should be less than 35 mV peak when a load step change of 100 mA is applied at the device output terminal
- Input supply requirement of between 4.5 V and 5.5 V
- Low quiescent current to improve battery life
- Thermal and current limit overload protection
- Ideally, select an LDO with common footprint, to allow interchanging between regulators

5. Touchscreen Basics

5.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are constructed from Indium Tin Oxide (ITO) or metal mesh. Thicker electrodes yield lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner electrodes lead to higher levels of resistance (perhaps hundreds to thousands of Ω/square) with some of the best optical characteristics.

Interconnecting tracks can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, the tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen viewing area.

5.2 Electrode Configuration

The specific electrode designs used in Atmel touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized in Section 6. on page 29.

5.3 Scanning Sequence

All nodes are scanned in sequence by the device. There is a full parallelism in the scanning sequence to improve overall response time. The nodes are scanned by measuring capacitive changes at the intersections formed between the first X line and all the Y lines. Then the intersections between the next X line and all the Y lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some nodes so that they are not scanned at all. This can be used to improve overall scanning time.

5.4 Touchscreen Sensitivity

5.4.1 Adjustment

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitic capacitance of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the far edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a node is considered to have enough signal change to qualify as being in detect.

5.4.2 Mechanical Stackup

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. QMatrix technology has an excellent ability to operate in the presence of ground planes close to the sensor. QMatrix sensitivity is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 1.2 mm, and glass up to about 2.5 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

Note: Care should be taken using ultra-thin glass panels as retransmission effects can occur, which can significantly degrade performance.

6. Sensor Layout

6.1 Mutual Capacitance Matrix

The specific electrode designs used in Atmel touchscreens are the subject of various patents and patent applications. Further information is available on request.

The physical matrix can be configured to have one or more touch objects. These are configured using the appropriate touch objects (Multiple Touch Touchscreen T100 and Key Array T15). It is not mandatory to have all the allowable touch objects present. The objects are disabled by default so only those that you wish to use need to be enabled. Refer to the *mXT336T 1.0 Protocol Guide* for more information on configuring the touch objects.

The device supports various configurations of electrodes as summarized below:

- Touchscreen: 24 X × 14 Y maximum (subject to other configurations)
- Keys: Up to 8 keys in an X/Y grid

When designing the physical layout of the touch panel, obey the following rules:

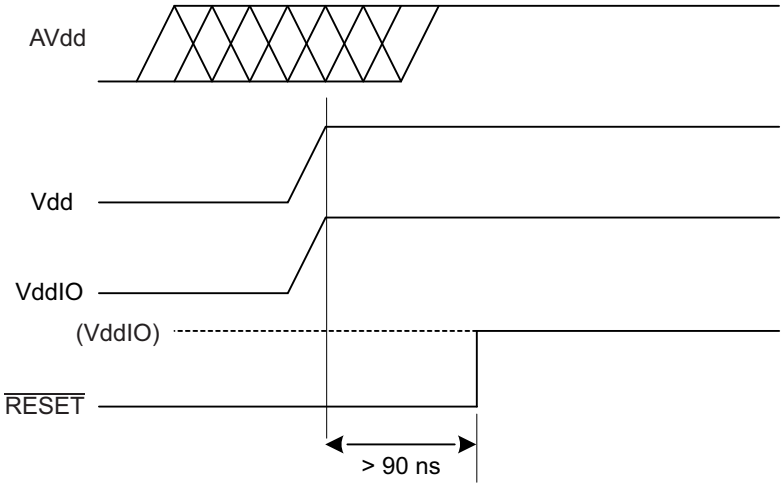
- Each touch object should be a regular rectangular shape in terms of the lines it uses
- The touch objects cannot share X and Y lines if self-capacitance measurement is enabled.
- It is recommended that the touchscreen should start at X0, Y0; if self-capacitance measurement is enabled, the touchscreen **must** start at X0, Y0
- It is recommended that the keys should occupy the highest X and Y lines

7. Power-up / Reset Requirements

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in RESET (active low) while the digital (Vdd) analog (AVdd) and I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the RESET signal is deasserted (that is, goes high). This is shown in Figure 7-1. See Section 13.2 on page 50 for nominal values for Vdd, VddIO, and AVdd.

Figure 7-1. Power Sequencing on the mXT336T



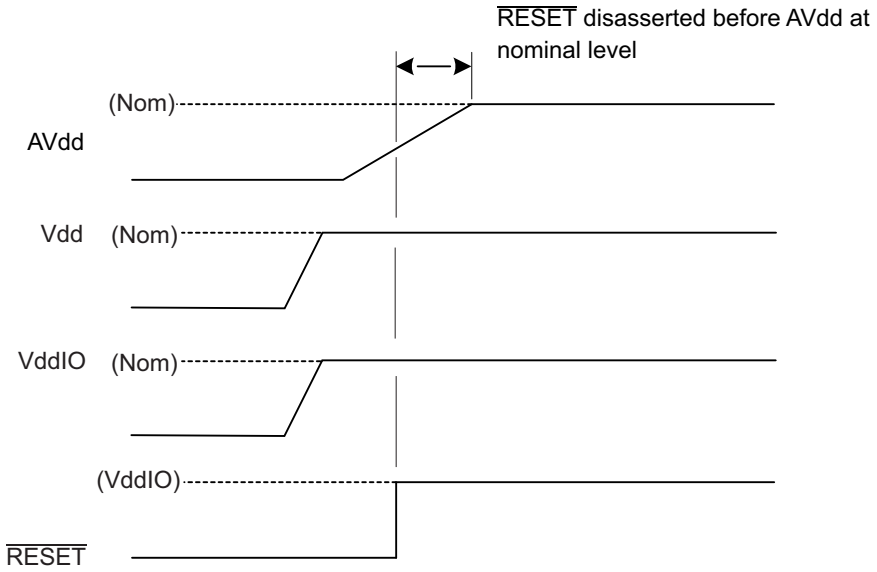
Note: When using external RESET at power-up, VddIO must not be enabled after Vdd

After power-up, the device takes 91.5 ms before it is ready to start communications.

If the RESET line is released before the AVdd supply has reached its nominal voltage (see Figure 7-2 on page 31), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in deep sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a reset command.

Figure 7-2. Power Sequencing on the mXT336T – Late rise on AVdd or XVdd



The RESET pin can be used to reset the device whenever necessary. The RESET pin must be asserted low for at least 90 ns to cause a reset. After releasing the RESET pin the device takes 91.3 ms before it is ready to start communications. It is recommended to connect the RESET pin to a host controller to allow it to initiate a full hardware reset without requiring a power-down.

Make sure that any lines connected to the device are below or equal to Vdd during power-up. For example, if RESET is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the RESET signal could parasitically couple power via the RESET pin into the Vdd supply.

Note that the voltage level on the RESET pin of the device must never exceed VddIO (digital supply voltage).

A software reset command can be used to reset the chip (refer to the Command Processor T6 object in the *mXT336T 1.0 Protocol Guide*. A software reset takes a maximum of 108.2 ms. After the chip has finished it asserts the CHG line to signal to the host that a message is available. The reset flag is set in the Message Processor object to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

A checksum check is performed on the configuration settings held in the nonvolatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. This is signaled to the host by setting the configuration error bit in the message data for the Command Processor T6 object (refer to the *mXT336T 1.0 Protocol Guide* for more information).

Note that the CHG line is briefly set as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the CHG line pull-up resistor during this period. It should not be driven by the host (see Table 13.7.3 on page 56).

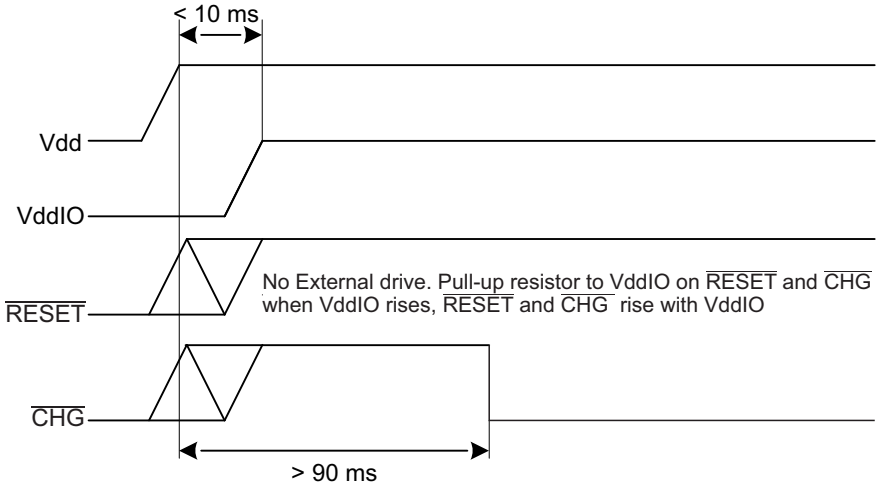
At power-on, the device performs a self-test routine to check for shorts that might cause damage to the device. Refer to the Self Test T25 object in the *mXT336T 1.0 Protocol Guide* for more details about this process.

7.1 Power-up and Reset Sequence – VddIO Enabled after Vdd

The Power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 7-3.

In this case the communication interface to mXT is not driven by the host system. The $\overline{\text{RESET}}$ and $\overline{\text{CHG}}$ pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors, $\overline{\text{RESET}}$ and $\overline{\text{CHG}}$ will rise with VddIO. The internal POR system ensures reliable boot up of the device and the $\overline{\text{CHG}}$ line will go low approximately 90 ms after Vdd to notify the host that the device is ready to start communication.

Figure 7-3. Power-up Sequence



7.1.1 Summary

The Power-up and RESET requirements for the maXTouch devices are summarised in the table below.

Condition	External $\overline{\text{RESET}}$	VddIO Delay (After Vdd)	AVdd Power-Up	Comments
1	Low at Power-up	0 ms	Before $\overline{\text{RESET}}$ is released	If AVdd bring-up is delayed then additional actions will be required by the host. See notes in Figure 7-1 on page 30
2	Not driven	<10 ms	Before VddIO	

8. Detailed Operation

8.1 Touch Detection

The mXT336T allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches. Refer to the *mXT336T 1.0 Protocol Guide* for more information on measurements.

Self capacitance measurements, on the other hand, allow for the detection of single touches in extreme case, such as single thick glove touches, when touches can only be detected by self capacitance data and may be missed by mutual capacitance touch detection.

8.2 Operational Modes

The device operates in two modes: Active (touch detected) and Idle (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an *Active to Idle Timeout* setting is provided.

Refer to the *mXT336T 1.0 Protocol Guide* for full information on how these modes operate, and how to use the settings provided.

8.3 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T100, Key Array T15). Refer to the *mXT336T 1.0 Protocol Guide* for more information.

8.4 Sensor Acquisition

The maximum acquisition time for one X line on the mXT336T is 5 µs. Care should be taken to ensure that the total time for one X line configured by the Acquisition Configuration T8 and CTE Configuration T46 objects do not exceed this (refer to the *mXT336T 1.0 Protocol Guide* for details on these objects).

8.5 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Nodes are only calibrated on reset and when:

- The node is enabled (that is, activated).

or

- The node is already enabled and one of the following applies:
  - The node is held in detect for longer than the Touch Automatic Calibration setting (refer to the *mXT336T 1.0 Protocol Guide* for more information on TCHAUTOCAL setting in the Acquisition Configuration object).

- The signal delta on a node is at least the touch threshold (TCHTHR) in the anti-touch direction, while it meets the criteria in the Touch Recovery Processes that results in a recalibration. (Refer to the *mXT336T 1.0 Protocol Guide* for objects Acquisition Configuration T8 and Self Capacitance Configuration T111).
- The host issues a recalibrate command.
- Certain configuration settings are changed.

A status message is generated on the start and completion of a calibration.

Note that the device performs a global calibration; that is, all the nodes are calibrated together.

8.6 Digital Filtering and Noise Suppression

The mXT336T supports on-chip filtering of the acquisition data received from the sensor. Specifically, the maXCharger T72 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the analog-to-digital conversions (ADCs) received from the sensor.

Additional noise suppression is provided by the Self Capacitance maXCharger T108 object. Similar in both design and configuration to the maXCharger T72 object, the Self Capacitance maXCharger T108 object is the noise suppression interface for self capacitance touch measurements.

Noise suppression is triggered when a noise source is detected.

- A hardware trigger can be implemented using the NOISE_IN pin.
- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements.The maXCharger T72 and Self Capacitance maXCharger T108 object selects the appropriate controls to suppress the noise present in the system.

Refer to the *mXT336T 1.0 Protocol Guide* for more information on the maXCharger T72 and Self Capacitance maXCharger T108 objects.

8.7 Shieldless Support and Display Noise Suppression

The mXT336T can support shieldless sensor design even with a noisy LCD by using the following features.

- **Optimal Integration:** This feature is not filtering as such, but enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source. This feature is configured using the Shieldless T56 object. Refer to the *mXT336T 1.0 Protocol Guide* for more information
- **Display noise suppression:** This feature is based on filtering provided by the Lens Bending T65 object (See Section 8.9 on page 35). This feature allows the device to overcome display noise simultaneously with external noise. Refer to the *mXT336T 1.0 Protocol Guide* for more information

8.8 Retransmission Compensation

The device can limit the undesirable effects on the mutual capacitance touch signals caused by poor device coupling to ground, such as poor sensitivity and touch break-up. This is achieved using the Retransmission Compensation T80 object. This object can be configured to allow the touchscreen to compensate for signal degradation due to these undesirable effects. If self capacitance measurements are also scheduled, the Retransmission Compensation T80 object will use the resultant data to enhance the compensation process.

The Retransmission Compensation T80 object is also capable of compensating for water presence on the sensor if self capacitance measurements are scheduled. In this case, both mutual capacitance and self capacitance measurements are used to detect moisture and then, once moisture is detected, self capacitance measurements are used to detect single touches in the presence of moisture.

Refer to the *mXT336T 1.0 Protocol Guide* for more information on the Retransmission Compensation T80 object.

8.9 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal and also to measure the bend component.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor

The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend. As the bend component is primarily influenced by the user touch force, it can be used as a secondary source to identify the presence of a touch. The additional benefit of the Lens Bending T65 object is that it will eliminate LCD noise as well.

Refer to the *mXT336T 1.0 Protocol Guide* for more information on the Lens Bending T65 object.

8.10 Glove Detection

The device has glove detection algorithms that process the measurement data received from the touchscreen classifying touches as potential gloved touches.

The Glove Detection T78 object is used to detect glove touches. In Normal Mode the Glove Detection T78 object applies vigorous glove classification to small signal touches to minimize the effect of unintentional hovering finger reporting. Once a gloved touch is found, the Glove Detection T78 object enters Glove Confidence Mode. In this mode the device expects the user to be wearing gloves so the classification process is much less stringent.

Refer to the *mXT336T 1.0 Protocol Guide* for more information on the Glove Detection T78 object.

8.11 Stylus Support

The mXT336T allows for the particular characteristics of passive stylus touches, whilst still allowing conventional finger touches to be detected. The touch sensitivity and threshold controls for stylus touches are configured separately from those for conventional finger touches so that both types of touches can be accommodated.

Stylus support ensures that the small touch area of a stylus registers as a touch, as this would otherwise be considered too small for the touchscreen. Additionally, there are controls to distinguish a stylus touch from an unwanted approaching finger (such as on the hand holding the stylus).

Passive stylus touches are configured by the Stylus T47 object. There is one instance of the Stylus T47 object for each Multiple Touch Touchscreen T100 object present on the device.

Refer to the *mXT336T 1.0 Protocol Guide* for more information on configuring a stylus.

8.12 Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected. There is one instance of the Touch Suppression T42 object for each Multiple Touch Touchscreen T100 object present on the device.

Refer to the *mXT336T 1.0 Protocol Guide* for more information on the Touch Suppression T42 object.

8.13 Adjacent Key Suppression Technology

Adjacent Key Suppression (AKS) technology is a patented method used to detect which touch object is touched when objects are located close together. A touch in a group of AKS objects is only indicated on the object in that group that is touched first. This is assumed to be the intended object. Once an object in an AKS group is in detect, there can be no further detections within that group until the object is released. Objects can be in more than one AKS group.

Note that AKS technology works best when it operates in conjunction with a detect integration setting of several acquisition cycles.

The device has two levels of AKS. The first level works between the touch objects (Multiple Touch Touchscreen T100 and Key Array T15). The touch objects are assigned to AKS groups. If a touch occurs within one of the touch objects in a group, then touches within other objects inside that group are suppressed. For example, if a touchscreen and a Key Array are placed in the same AKS group, then a touch in the touchscreen will suppress touches in the Key Array, and vice versa.

The second level of AKS is internal AKS within an individual Key Array object (note that internal AKS is not present on other types of touch objects, only a Key Array T15). If internal AKS is enabled, then when one key is touched, touches on all the other keys within the Key Array are suppressed.

AKS is configured using the touch objects (Multiple Touch Touchscreen T100 or Key Array T15).

Refer to the *mXT336T 1.0 Protocol Guide* for more information.

Note: If a touch is in detect and then AKS is enabled, that touch will not be forced out of detect. It will not go out of detect until the touch is released. AKS will then operate normally. This applies to both levels of AKS.

8.14 GPIO Pins

The mXT336T has 4 GPIO pins. The pins can be set to be either an input or an output, as required. Note that unused GPIO pins can be left externally unconnected as long as they are given a defined state by using the GPIO/PWM Configuration T19 object. With the GPIO/PWM Configuration T19 object, an unused GPIO pin can be either set to Input mode, with internal pull-up, or Output mode.

By default GPIO pins are set to be inputs. If not used they should be connected to GND. Alternatively, they can be set as outputs using the GPIO/PWM Configuration T19 object and left open.

9. I²C Communications

The device can use an I²C interface for communication. See Appendix B. on page 67 for details of the I²C protocol.

The I²C interface is used in conjunction with the $\overline{CHG}$ line. The $\overline{CHG}$ line going active signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred.

9.1 I²C Address

The device supports one I²C device address – 0x4A. This is shifted left to form the SLA+W or SLA+R address when transmitted over the I²C interface, as shown in Figure 9-1.

Table 9-1. Format of an I²C Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4A							Read/write

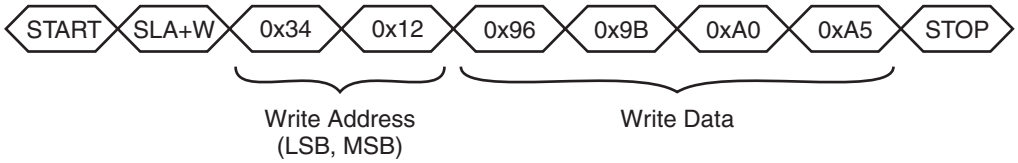
9.2 Writing To the Device

A WRITE cycle to the device consists of a START condition followed by the I²C address of the device (SLA+W). The next two bytes are the address of the location into which the writing starts. The first byte is the Least Significant Byte (LSByte) of the address, and the second byte is the Most Significant Byte (MSByte). This address is then stored as the address pointer.

Subsequent bytes in a multi-byte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer + 1, location of the address pointer + 2, and so on. The address pointer returns to its starting value when the WRITE cycle STOP condition is detected.

Figure 9-1 shows an example of writing four bytes of data to contiguous addresses starting at 0x1234.

Figure 9-1. Example of a Four-byte Write Starting at Address 0x1234

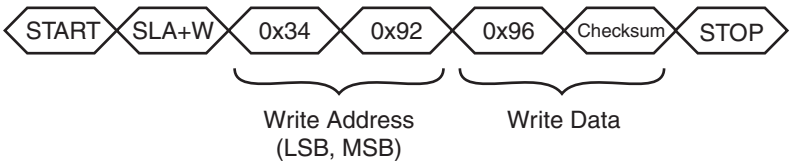


9.3 I²C Writes in Checksum Mode

In I²C checksum mode an 8-bit CRC is added to all I²C writes. The CRC is sent at the end of the data write as the last byte before the STOP condition. All the bytes sent are included in the CRC, including the two address bytes. Any command or data sent to the device is processed even if the CRC fails.

To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the address is set to 1. For example, the I²C command shown in Figure 9-2 writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x9234 to indicate checksum mode.

Figure 9-2. Example of a Write To Address 0x1234 With a Checksum



9.4 Reading From the Device

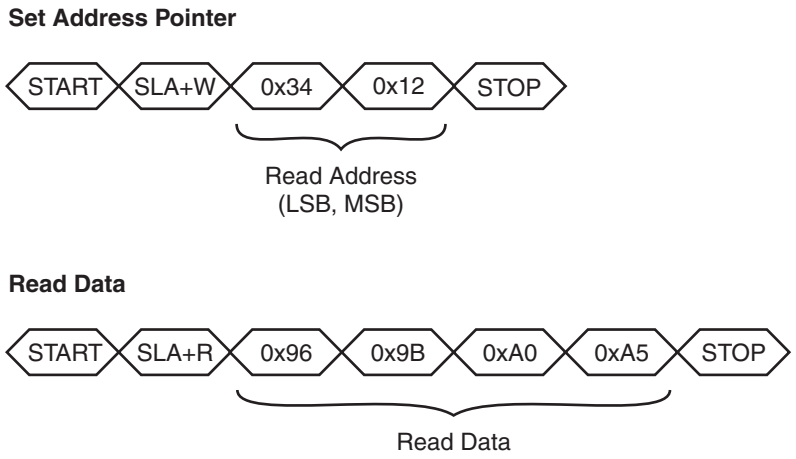
Two I²C bus activities must take place to read from the device. The first activity is an I²C write to set the address pointer (LSByte then MSByte). The second activity is the actual I²C read to receive the data. The address pointer returns to its starting value when the read cycle NACK is detected.

It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to allow continuous reads (see Section 9.5).

The WRITE and READ cycles consist of a START condition followed by the I²C address of the device (SLA+W or SLA+R respectively).

Figure 9-3 shows the I²C commands to read four bytes starting at address 0x1234.

Figure 9-3. Example of a Four-byte Read Starting at Address 0x1234



9.5 Reading Status Messages with DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a direct memory access (DMA) controller for the fast reading of messages, as follows:

1. The host uses a write operation to set the address pointer to the start of the Message Count T44 object, if necessary (1). If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.
2. The host starts the read operation of the message by sending a START condition.
3. The host reads the Message Count T44 object (one byte) to retrieve a count of the pending messages (refer to the *mXT336T 1.0 Protocol Guide* for details).
4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor T5 object (2).
5. Note that the size of the Message Processor T5 object as recorded in the Object Table includes a checksum byte. If a checksum has not been requested, one byte should be deducted from the size of the object. That is: number of bytes = count × (size – 1).
6. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.

1. The STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T44 object following a previous message read.
2. The host should have already read the size of the Message Processor T5 object in its initialization code.

7. The host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of Message Count T44 object.

Figure 9-4 shows an example of using a continuous read operation to read three messages from the device without a checksum. Figure 9-5 on page 40 shows the same example with a checksum.

Figure 9-4. Continuous Message Read Example – No Checksum

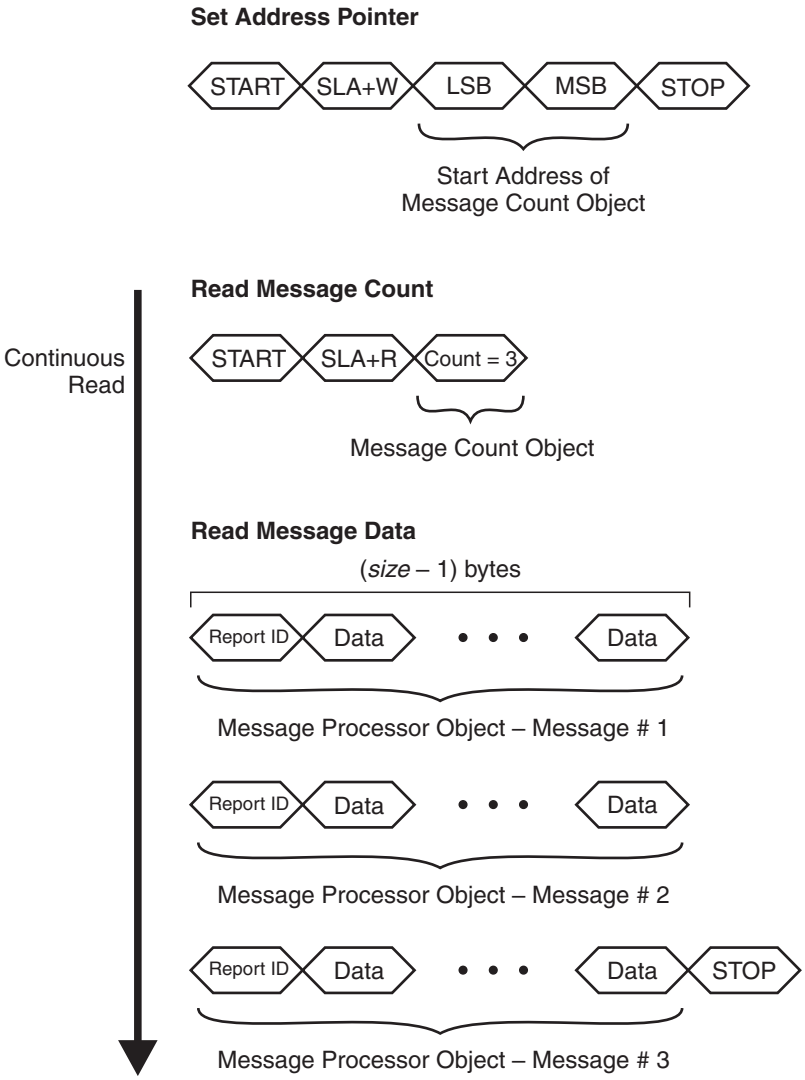
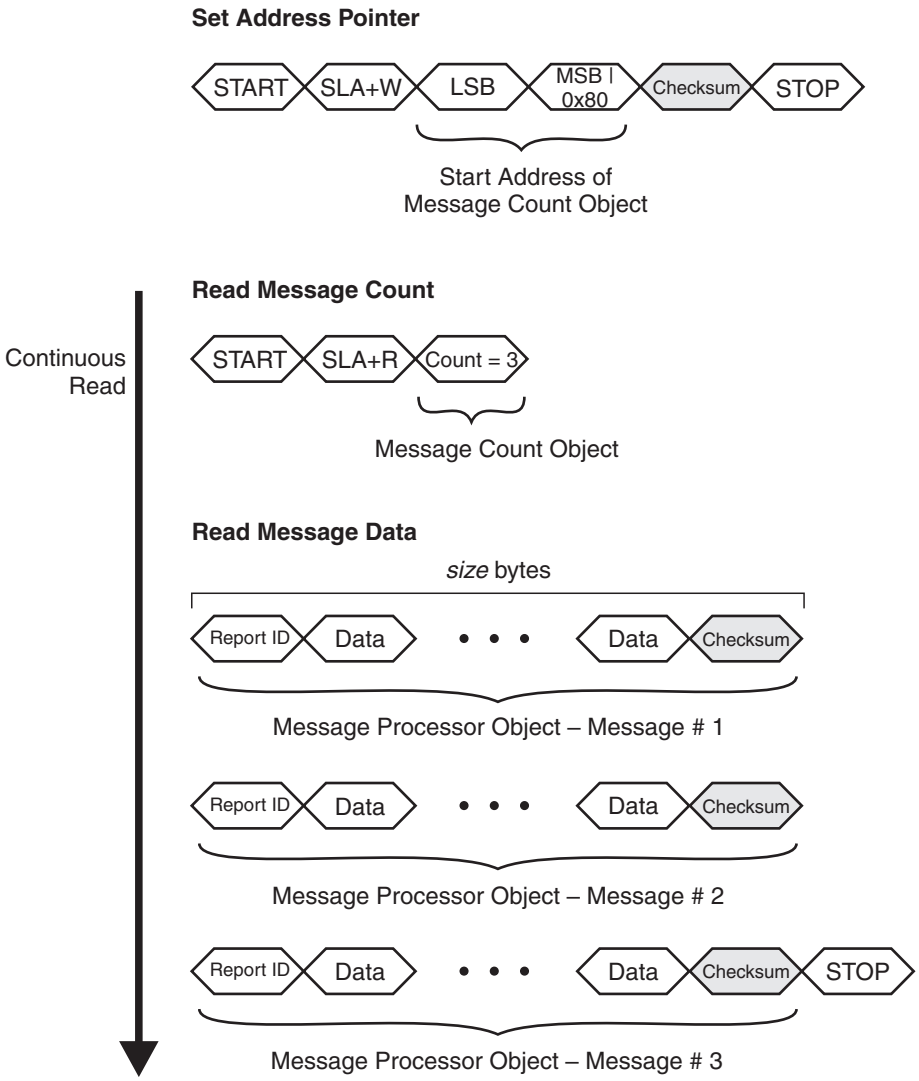


Figure 9-5. Continuous Message Read Example – I²C Checksum Mode



There are no checksums added on any other I²C reads. An 8-bit CRC can be added, however, to all I²C writes, as described in Section 9.3 on page 37.

An alternative method of reading messages using the $\overline{\text{CHG}}$ line is given in Section 9.6.

9.6 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor T5 object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I²C communications.

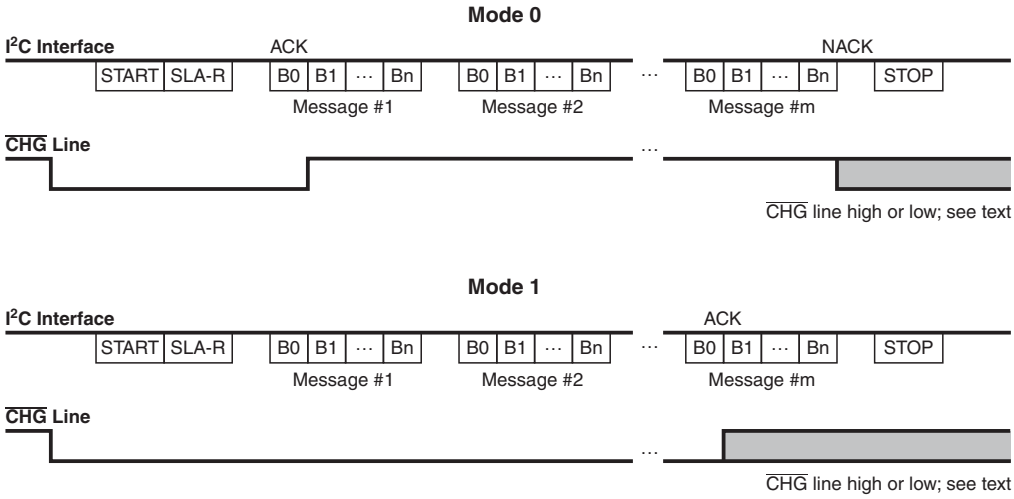
The $\overline{\text{CHG}}$ line remains low as long as there are messages to be read. The host should be configured so that the $\overline{\text{CHG}}$ line is connected to an interrupt line that is level-triggered. The host should not use an edge-triggered interrupt as this means adding extra software precautions.

The $\overline{\text{CHG}}$ line should be allowed to float during normal usage. This is particularly important after power-up or reset (see Section 7. on page 30).

A pull-up resistor is required, typically 3.3 kΩ to VddIO.

The $\overline{\text{CHG}}$ line operates in two modes, as defined by the Communications Configuration T18 object (refer to the *mXT336T 1.0 Protocol Guide*).

Figure 9-6. $\overline{\text{CHG}}$ Line Modes for I²C-compatible Transfers



In Mode 0:

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I²C transfer causes the $\overline{\text{CHG}}$ line to stay high if there are no more messages. Otherwise the $\overline{\text{CHG}}$ line goes low to indicate a further message.

Mode 0 allows the host to continually read messages. Messaging reading ends when a report ID of 255 (“invalid message”) is received. Alternatively the host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If and when there is another message present, the $\overline{\text{CHG}}$ line goes low, as in step 1. In this mode the state of the $\overline{\text{CHG}}$ line does not need to be checked during the I²C read.

In Mode 1:

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line remains low while there are further messages to be sent after the current message.
3. The $\overline{\text{CHG}}$ line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the $\overline{\text{CHG}}$ line goes high, and the state of the $\overline{\text{CHG}}$ line determines whether or not the host should continue receiving messages from the device.

Note: The state of the $\overline{\text{CHG}}$ line should be checked only between messages and not between the bytes of a message. The precise point at which the $\overline{\text{CHG}}$ line changes state cannot be predicted and so the state of the $\overline{\text{CHG}}$ line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the $\overline{\text{CHG}}$ line. In addition to the $\overline{\text{CHG}}$ line operation modes described above, this object allows the use of edge-based interrupts, as well as direct control over the state of the $\overline{\text{CHG}}$ line. Refer to the *mXT336T 1.0 Protocol Guide* for more information.

9.7 SDA, SCL

The I²C bus transmits data and clock with SDA and SCL, respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to Vdd if no I²C device is pulling it down.

The termination resistors should be chosen so that the rise times on SDA and SCL meet the I²C specifications for the interface speed being used, bearing in mind other loads on the bus (see Section 13.9 on page 57).

9.8 Clock Stretching

The device supports clock stretching in accordance with the I^2C specification. It may also instigate a clock stretch if a communications event happens during a period when the device is busy internally. The maximum clock stretch is approximately 10 – 15 ms.

The device has an internal bus monitor that can reset the internal I^2C hardware if SDA or SCL is stuck low for more than 200 ms. This means that if a prolonged clock stretch of more than 200 ms is seen by the device, then any ongoing transfers with the device may be corrupted. The bus monitor is enabled or disabled using the Communications Configuration T18 object. Refer to the *mXT336T 1.0 Protocol Guide* for more information.

10. PCB Design Considerations

10.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT336T. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

10.2 Printed Circuit Board

Atmel recommends the use of a four-layer printed circuit board for mXT336T applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

10.2.1 PCB Cleanliness

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

CAUTION: If a PCB is reworked to correct soldering faults relating to any of the device devices, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

10.3 Supply Rails and Ground Tracking

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the 0 V plane. The flood filling should be done on the outside layers of the board.

10.4 Power Supply Decoupling

As a rule, a suitable decoupling capacitor should be placed on each and every supply pin on all digital devices. It is important that these capacitors are placed as close to the chip supply pins as possible (less than 10 mm away). The ground connection of these capacitors should be tracked to 0 V by the shortest, heaviest traces possible.

Capacitors with a Type II dielectric, such as X5R or X7R and with a value of at least 100 nF, should be used for this purpose.

In addition, at least one ‘bulk’ decoupling capacitor, with a minimum value of 4.7 µF should be placed on each power rail, close to where the supply enters the board.

Surface mounting capacitors are preferred to wire leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

Refer to the application note *Selecting Decoupling Capacitors for Atmel PLDs* (doc0484.pdf; available on the Atmel website) for further general information on decoupling capacitors.

10.5 Single Supply Operation

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

10.6 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

10.7 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible. This simple point is often overlooked when initially planning a PCB layout and can save hours of work at a later stage.

10.7.1 Digital Signals

In general, when tracking digital signals, it is advisable to avoid sharp directional changes, sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

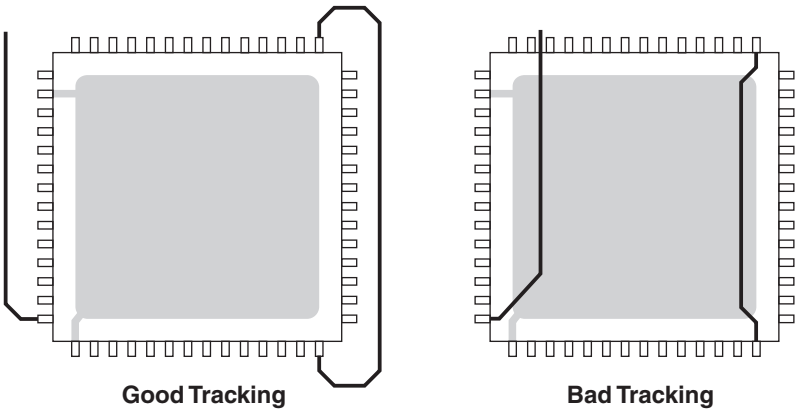
A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities in the ground return path.

10.7.2 UQFN Package Restrictions

The central pad on the underside of the UQFN device should be connected to ground. Do not run any tracks underneath the body of the device, only ground. Figure 10-1 shows an example of good/bad tracking.

Figure 10-1. Examples of Good and Bad Tracking

Note: The number of pins and their functions is shown for example purposes only and may not reflect the actual number or function on the device.



10.8 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer's datasheet for more information.

11. Getting Started with mXT336T

11.1 Establishing Contact

11.1.1 Communication with the Host

The host can use the following interface to communicate with the device:

- I^2C interface (see Section 9. on page 37)

11.1.2 Power-up Sequence

On power-up, the $\overline{CHG}$ line goes low to indicate that there is new data to be read from the Message Processor T5 object. If the $\overline{CHG}$ line does not go low, there is a problem with the device.

The host should attempt to read any available messages to establish that the device is present and running following power-up or a reset. Examples of messages include reset or calibration messages. The host should also check that there are no configuration errors reported.

11.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device. Refer to the *mXT336T 1.0 Protocol Guide* for more information.

The host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.

11.3 Writing to the Device

There are a number of mechanisms for writing to the device:

- Using an I^2C write operation (see Section 9.2 on page 37).

To communicate with the device, you write to the appropriate object:

- To send a command to the device, you write the appropriate command to the Command Processor T6 object (refer to the *mXT336T 1.0 Protocol Guide*).
- To configure the device, you write to an object. For example, to configure the device power consumption you write to the global Power Configuration T7 object, and to set up a touchscreen you write to a Multiple Touch Touchscreen T100 object. Some objects are optional and need to be enabled before use. Refer to the *mXT336T 1.0 Protocol Guide* for more information on the objects.

11.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device. The following mechanisms provide an interrupt-style interface for reading messages in the Message Processor T5 object:

- The $\overline{CHG}$ line is asserted whenever a new message is available in the Message Processor T5 object (see Section 9.6 on page 40). See Section 9.4 on page 38 for information on the format of the I^2C read operation.

Note that the host should always wait to be notified of messages. The host should not poll the device for messages.

11.5 Configuring the Device

The objects are designed such that a default value of zero in their fields is a “safe” value that typically disables functionality. The objects must be configured before use and the settings written to the nonvolatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

Refer to the *mXT336T 1.0 Protocol Guide* for more information on configuring the objects.

The following objects require no configuration:

- Debug Objects
  - Diagnostic Debug T37
- General objects:
  - Message Processor T5
  - Command Processor T6
- Support objects:
  - Message Count T44

The following objects must be configured before use:

- General objects
  - Power Configuration T7
  - Acquisition Configuration T8

The following objects should be checked and configured as necessary:

- Touch objects:
  - Key Array T15
  - Multiple Touch Touchscreen T100
- Signal processing objects:
  - Stylus T47
- Support objects:
  - Communications Configuration T18
  - GPIO/PWM Configuration T19
  - User Data T38
  - CTE Configuration T46
  - Self Capacitance Global Configuration T109
  - Self Capacitance Tuning Parameters T110
  - Self Capacitance Configuration T111
  - Self Capacitance Measurement Configuration T113

The following objects are optional and can be configured, as required:

- Signal processing objects:
  - Touch Suppression T42
  - Shieldless T56
  - Lens Bending T65
  - maXCharger T72
  - Glove Detection T78
  - Retransmission Compensation T80
  - Symbol Gesture Processor T92
  - Self Capacitance maXCharger T108

- Support objects:
  - Self Test T25
  - Timer T61
  - Dynamic Configuration Controller T70
  - Dynamic Configuration Container T71
  - Auxiliary Touch Configuration T104

12. Debugging

The device provides a mechanism for obtaining raw data for development and testing purposes by reading data from the Diagnostic Debug T37 object. Refer to the *mXT336T 1.0 Protocol Guide* for more information on this object.

A second mechanism is provided that allows the host to read the real-time raw data using the low-level debug port. This can be accessed via the SPI interface. Refer to QTAN0050, *Using the maXTouch Debug Port*, for more information on the debug port.

There is also a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. This object also performs an initial pin fault test on power-up to ensure that there is no X-to-Y short before the high-voltage supply is enabled inside the chip. A high-voltage short into the analog circuitry would break the device.

Refer to the *mXT336T 1.0 Protocol Guide* and QTAN0059, *Using the maXTouch Self Test Feature*, for more information on the Self Test T25 object.

13. Specifications

13.1 Absolute Maximum Specifications

Vdd	3.6 V
VddIO	3.6 V
AVdd	3.6 V
XVdd	9.0 V
Voltage forced onto any pin	–0.3 V to (Vdd, VddIO or AVdd) + 0.3 V
Configuration parameters maximum writes (flash memory write cycles)	10,000

CAUTION: Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

13.2 Recommended Operating Conditions

Operating temp	–40°C to +85°C
Storage temp	–60°C to +150°C
Vdd	3.3 V
VddIO	1.8 V to 3.3 V
AVdd	3.3 V
XVdd with internal voltage doubler	Vdd to 2 × Vdd
Cx transverse load capacitance per channel	0.6 pF to 3 pF
Temperature slew rate	10°C/min

13.3 DC Characteristics

13.3.1 Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
Operating limits	2.7	3.3	3.47	V	
Supply Rise Rates	–	–	0.25	V/µs	

13.3.2 Digital Voltage Supply

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits	1.71	–	3.47	V	I^2C-compatible. For compatibility with future devices in the same chip family, VddIO should be at the same level as Vdd.
Supply Rise Rates	–	–	0.25	V/µs	
Vdd					
Operating limits	3.0	3.3	3.47	V	
Supply Rise Rates	–	–	0.25	V/µs	

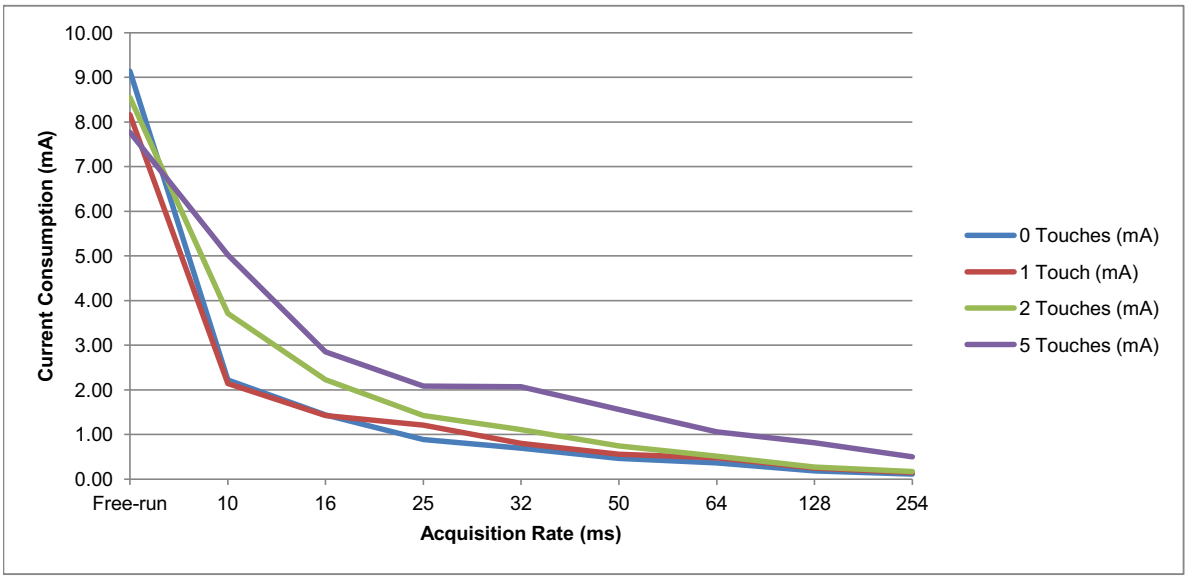
13.4 Current Consumption

Note: Measurements taken with firmware version 1.0.AB.

13.4.1 Analog Supply

I2C Interface, AVdd = 3.3V

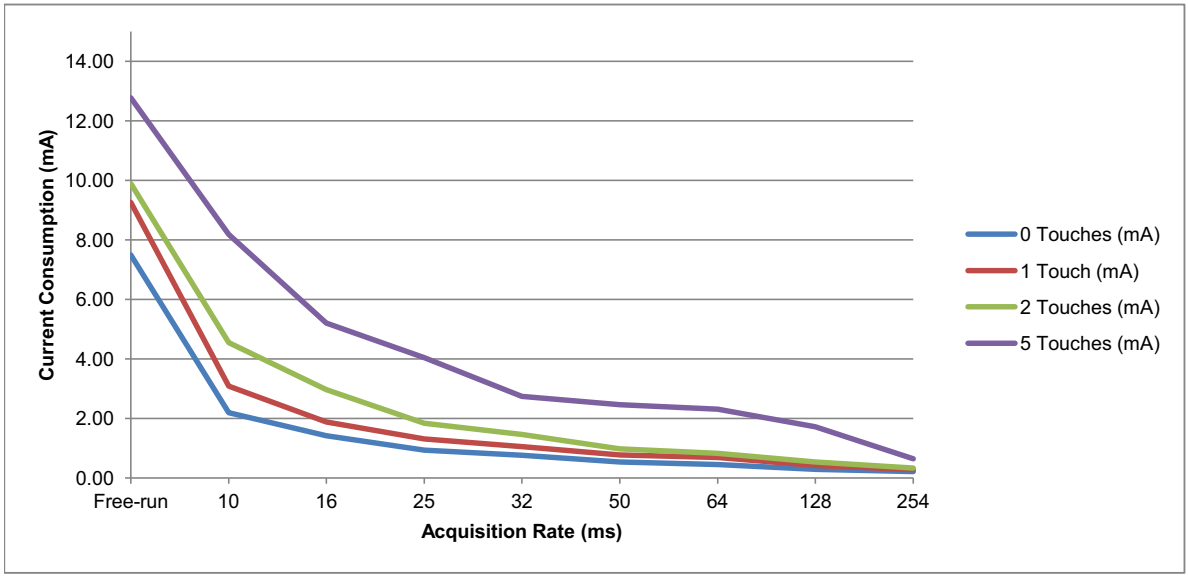
Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)
Free-run	9.14	8.17	8.55	7.77
10	2.22	2.14	3.71	5.02
16	1.44	1.43	2.23	2.85
25	0.88	1.21	1.42	2.08
32	0.70	0.80	1.11	2.07
50	0.46	0.56	0.75	1.56
64	0.36	0.48	0.51	1.06
128	0.19	0.25	0.27	0.81
254	0.11	0.15	0.17	0.50



13.4.2 Digital Supply

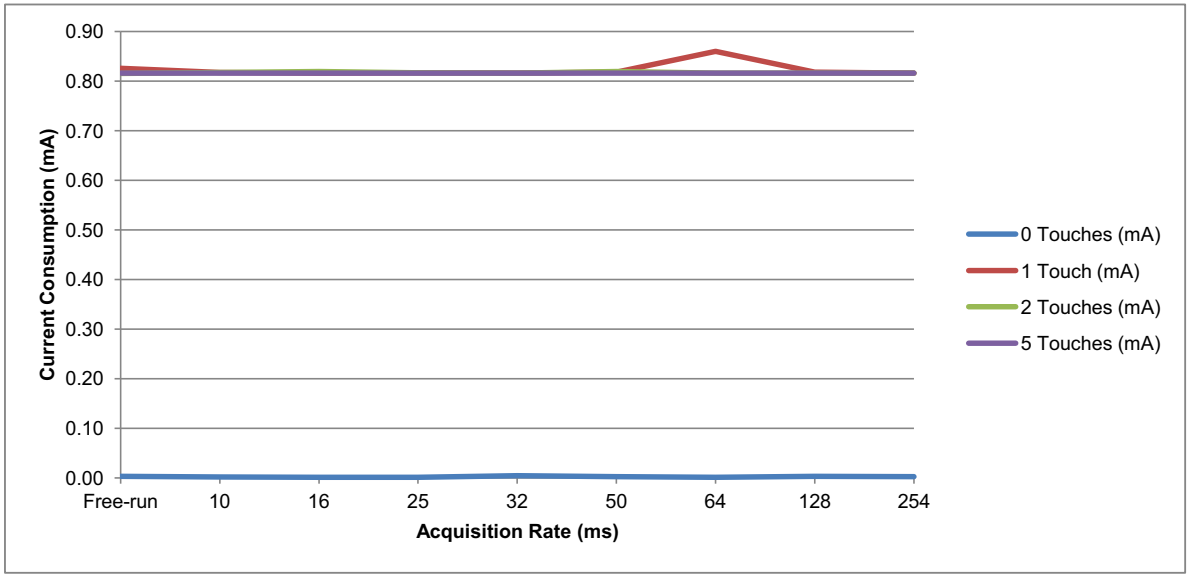
I2C Interface, Vdd = 3.3V

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)
Free-run	7.50	9.26	9.89	12.77
10	2.20	3.09	4.54	8.18
16	1.41	1.88	2.96	5.20
25	0.94	1.31	1.84	4.04
32	0.76	1.05	1.46	2.74
50	0.53	0.77	0.98	2.46
64	0.44	0.68	0.83	2.31
128	0.28	0.42	0.53	1.72
254	0.22	0.28	0.33	0.64



I2C Interface, VddIO = 1.8V

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	2 Touches (mA)	5 Touches (mA)
Free-run	0.00	0.83	0.82	0.82
10	0.00	0.82	0.82	0.82
16	0.00	0.82	0.82	0.82
25	0.00	0.82	0.82	0.82
32	0.00	0.82	0.82	0.82
50	0.00	0.82	0.82	0.82
64	0.00	0.86	0.82	0.82
128	0.00	0.82	0.82	0.82
254	0.00	0.82	0.82	0.82



13.5 Deep Sleep Current

T_A = 25°C

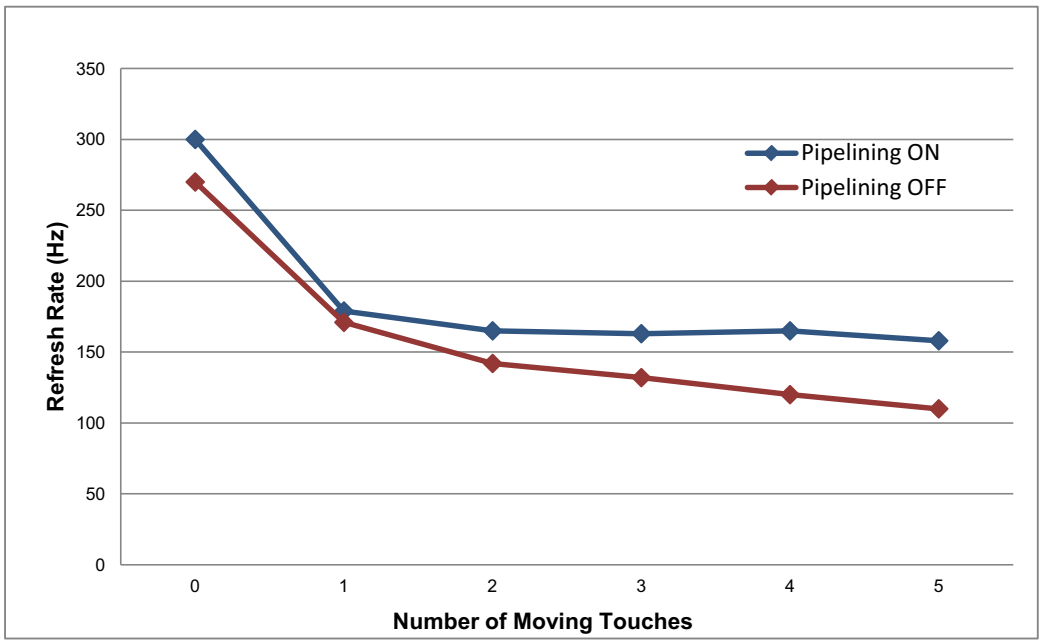
Parameter	Min	Typ	Max	Units	Notes
Deep Sleep Current	–	45	–	µA	Vdd = 3.3 V, AVdd = 3.3 V
Deep Sleep Power	–	148	–	µW	Vdd = 3.3 V, AVdd = 3.3 V

13.6 Power Supply Ripple and Noise

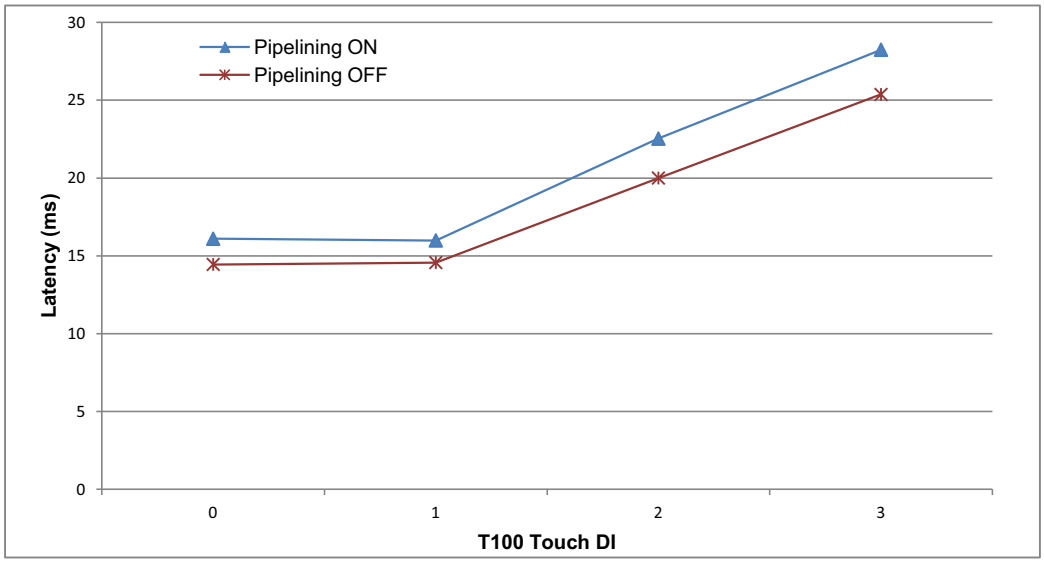
Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd (with noise suppression enabled)	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled

13.7 Timing Specifications

13.7.1 Refresh Rate



13.7.2 Touch Latency



13.7.3 Reset Timing

Parameter	Min	Typ	Max	Units	Notes
Power on to $\overline{\text{CHG}}$ line low	–	91.5	–	ms	Vdd supply for POR VddIO supply for external reset
Hardware reset to $\overline{\text{CHG}}$ line low	–	91.3	–	ms	
Software reset to $\overline{\text{CHG}}$ line low	–	108.2	–	ms	

The mXT336T meets Microsoft Windows 8 requirements.

Note: Any $\overline{\text{CHG}}$ line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired (see Table 13.7.3 on page 56).

13.8 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input ($\overline{\text{RESET}}$, GPIO, SDA, SCL)						
Vil	Low input logic level	–0.3	–	0.3 × VddIO	V	VddIO = 1.8 V to Vdd
Vih	High input logic level	0.7 × VddIO	–	VddIO	V	VddIO = 1.8 V to Vdd
Iil	Input leakage current	–	–	1	µA	Pull-up resistors disabled
$\overline{\text{RESET}}$ pin	Internal pull-up resistor	20	40	60	kΩ	
Output ($\overline{\text{CHG}}$, GPIO)						
Vol	Low output voltage	0	–	0.2 × VddIO	V	VDDIO = 1.8 V to VDD. Iol = -2mA
Voh	High output voltage	0.8 × VddIO	–	VddIO	V	VDDIO = 1.8 V to VDD. Ioh = 2mA

13.9 I²C Specifications

Parameter	Value
Addresses	0x4A
Maximum bus speed (SCL)	3.4 MHz
I²C specification	Version 6.0
Required pull-up resistance for standard mode (100 kHz)	1 kΩ to 10 kΩ (1)
Required pull-up resistance for fast mode (400 kHz)	1 kΩ to 3 kΩ (1)
Required pull-up resistance for fast+ mode (1 MHz)	0.7 kΩ (max) (1)
Required pull-up resistance for high-speed mode (3.4 MHz)	0.5 kΩ to 0.75 kΩ (1)

Notes: 1. The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I²C specification. The value required will depend on the amount of stray capacitance on the line.

13.10 Touch Accuracy and Repeatability

Parameter	Min	Typ	Max	Units	Notes
Linearity (touch only; 5.4 mm electrode pitch)	–	±1	–	mm	8 mm or greater finger
Linearity (touch only; 4.2 mm electrode pitch)	–	±0.5	–	mm	4 mm or greater finger
Accuracy	–	±1	–	mm	
Accuracy at edge	–	±2	–	mm	
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

13.11 Thermal Packaging

13.11.1 Thermal Data

Parameter	Typ	Unit	Condition	Package
Junction to ambient thermal resistance	46.5	°C/W	Still air	UFBGA 64, 5 × 5 mm
Junction to case thermal resistance	7.3	°C/W		UFBGA 64, 5 × 5 mm
Junction to ambient thermal resistance	48.4	°C/W	Still air	UFBGA 72, 6 × 6 mm
Junction to case thermal resistance	5.3	°C/W		UFBGA 72, 6 × 6 mm
Junction to ambient thermal resistance	22.4	°C/W	Still air	UFQFN 56, 6 × 6 mm
Junction to case thermal resistance	5.2	°C/W	–	UFQFN 56, 6 × 6 mm

13.11.2 Junction Temperature

The average chip junction temperature, T_J in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA}= package thermal resistance, Junction to ambient (°C/W).
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W).
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet.
- P_D = device power consumption (W).
- T_A is the ambient temperature (°C).

13.12 ESD Information

Parameter	Value	Reference standard
Human Body Model (HBM)	±2000 V	JEDEC JS–001
Charge Device Model (CDM)	±250 V	

13.13 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

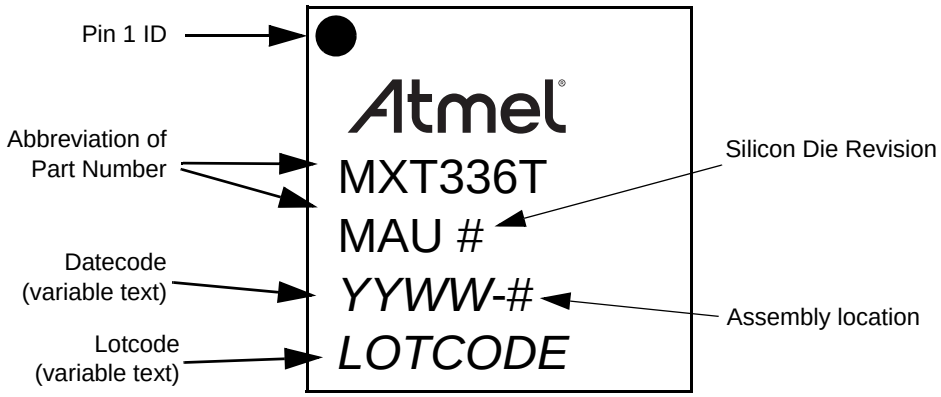
13.14 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL1	QFN	260°C	IPC/JEDEC J-STD-020
MSL3	BGA	260°C	IPC/JEDEC J-STD-020

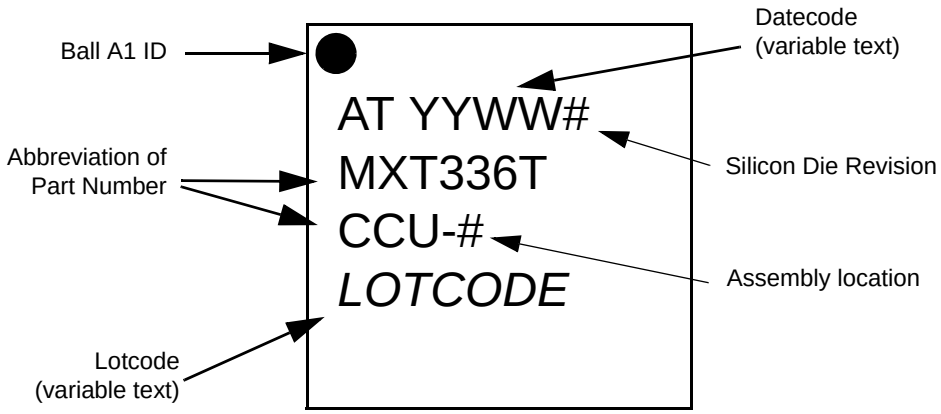
14. Package Information

14.1 Part Marking

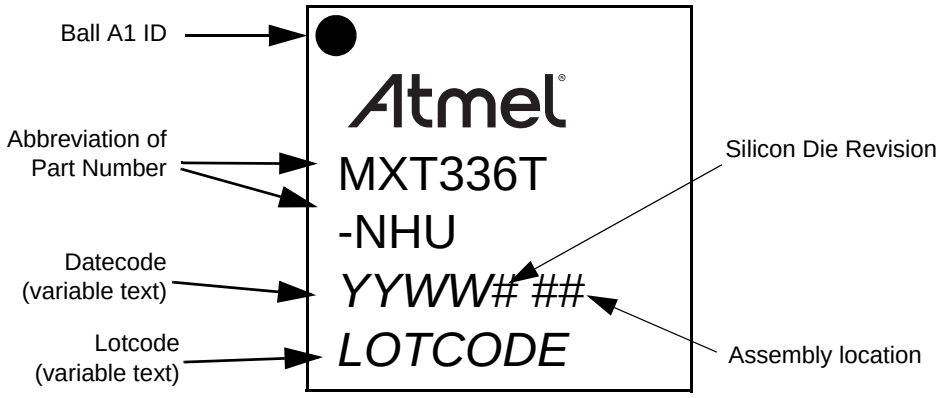
14.1.1 56-Pin UFQFN Package



14.1.2 64-Ball UFBGA Package



14.1.3 72-Ball UFBGA Package

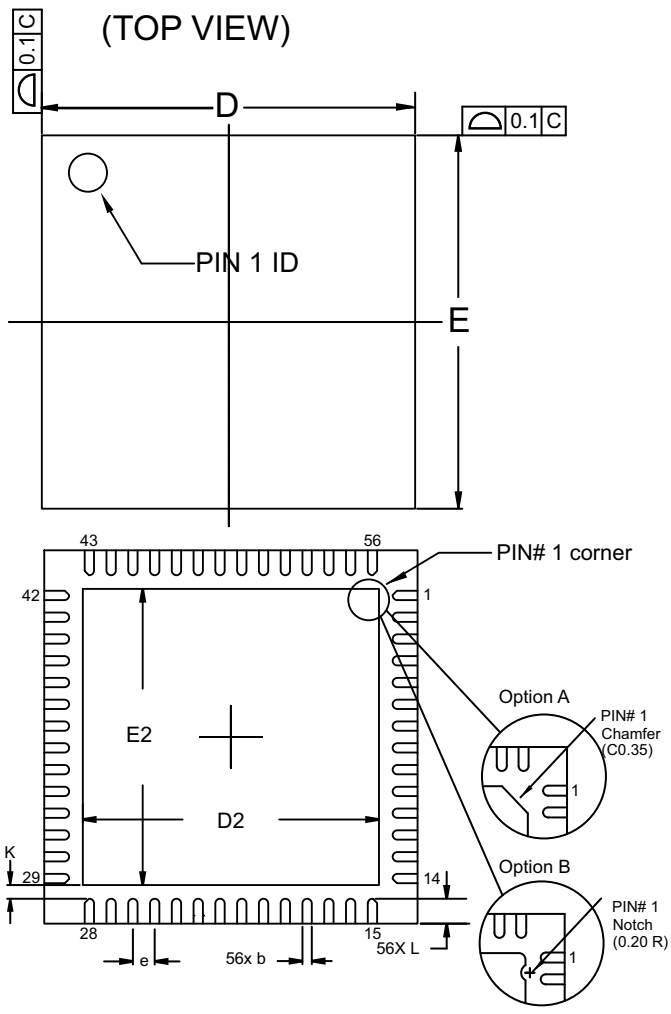


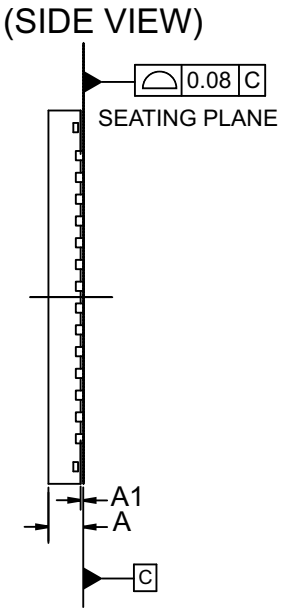
14.2 Orderable Part Numbers

Orderable Part Number	QS Number	Firmware Revision	Description
ATMXT336T-MAU (trays)	823	1.0.AA	56-pin UQFN 6 × 6 × 0.6 mm, 0.35 mm pin pitch, RoHS compliant
ATMXT336T-MAUR (tape and reels)	823	1.0.AA	56-pin UQFN 6 × 6 × 0.6 mm, 0.35 mm pin pitch, RoHS compliant
ATMXT336T-CCU (trays)	823	1.0.AA	64-ball UFBGA 5 × 5 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant
ATMXT336T-CCUR (tape and reels)	823	1.0.AA	64-ball UFBGA 5 × 5 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant
ATMXT336T-NHU (trays)	823	1.0.AA	72-ball UFBGA 6 × 6 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant
ATMXT336T-NHUR (tape and reels)	823	1.0.AA	72-ball UFBGA 6 × 6 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant
ATMXT336T-MAU (trays)	956	1.0.AB	56-pin UQFN 6 × 6 × 0.6 mm, 0.35 mm pin pitch, RoHS compliant
ATMXT336T-MAUR (tape and reels)	956	1.0.AB	56-pin UQFN 6 × 6 × 0.6 mm, 0.35 mm pin pitch, RoHS compliant
ATMXT336T-CCU (trays)	956	1.0.AB	64-ball UFBGA 5 × 5 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant
ATMXT336T-CCUR (tape and reels)	956	1.0.AB	64-ball UFBGA 5 × 5 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant
ATMXT336T-NHU (trays)	956	1.0.AB	72-ball UFBGA 6 × 6 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant
ATMXT336T-NHUR (tape and reels)	956	1.0.AB	72-ball UFBGA 6 × 6 × 0.6 mm, 0.5 mm ball pitch, RoHS compliant

14.3 Mechanical Drawings

14.3.1 UFQFN 56 Pins





NOTE :

1. Dimension "b" applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

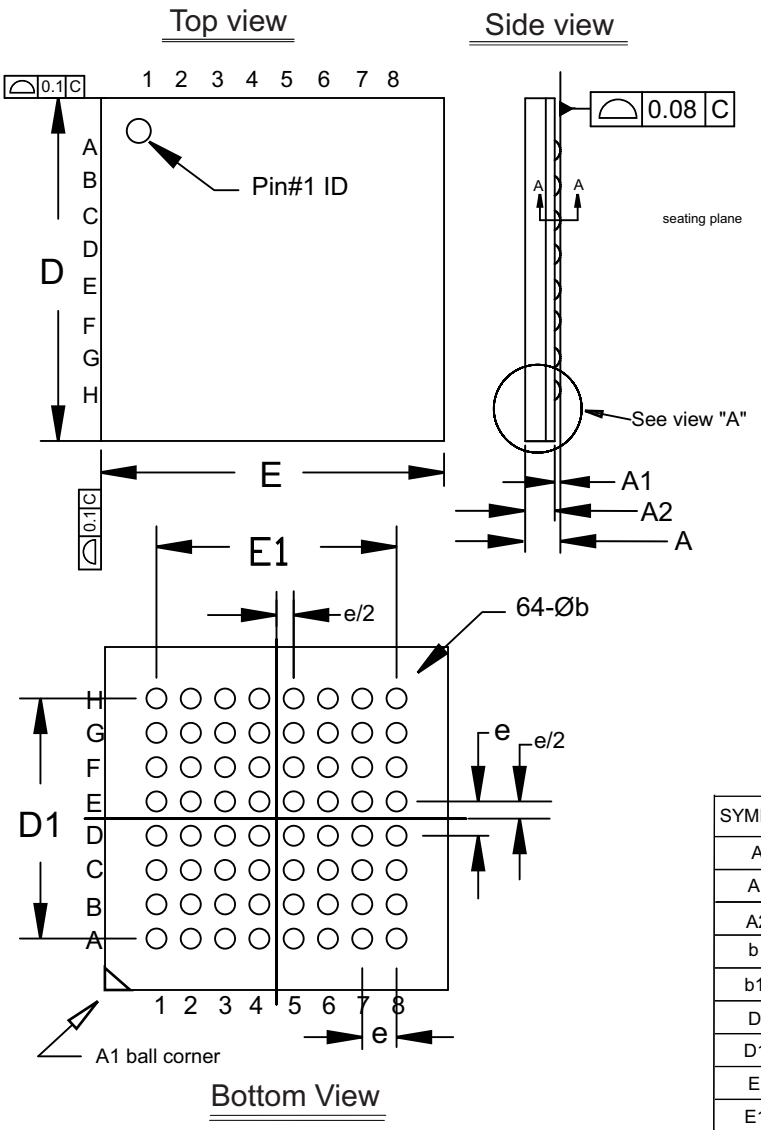
COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	0.55	0.60	
A1	0.00	-	0.05	
b	0.13	0.18	0.23	1
D		6.00 BSC		
D2	4.40	4.50	4.60	
E		6.00 BSC		
E2	4.40	4.50	4.60	
e	-	0.35	-	
L	0.35	0.40	0.45	
K	0.30	-	-	

03/26/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 56MA2, 56-pad, 6x6x0.6mm body,0.35mm pitch, (4.5mmSq Thermal ePAD) Ultra-Thin, Fine-Pitch Quad Flat No Lead Package (Sawn)(UFQFN)	GPC ZEK	DRAWING NO. 56MA2	REV. B

14.3.2 UFBGA 64 Balls



COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	0.53	0.60	
A1	0.12	-	-	
A2		0.38 REF		
b	0.25	0.30	0.35	1
b1	0.25	-	-	2
D	4.90	5.00	5.10	
D1		3.50 BSC		
E	4.90	5.00	5.10	
E1		3.50 BSC		
e		0.50BSC		

Note 1: Dimension "b" is measured at the maximum ball dia. in a plane parallel to seating plane.

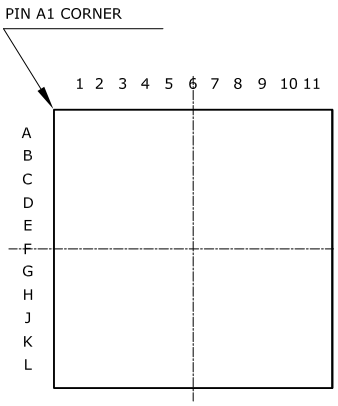
Note 2: Dimension "b1" is the solderable surface defined by the opening of the solder resist layer.

9/15/2011

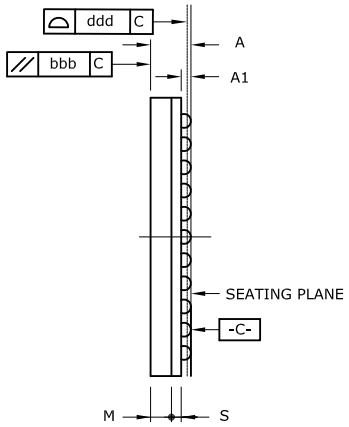
Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 64CC1, 64-ball, 5x5x0.6mm body,0.50mm ball pitch, (8 x 8 Array) Ultra-Thin, Fine-Pitch Ball Grid Array (UFBGA)	**GPC** CAJ	**DRAWING NO.** 64CC1	**REV.** A

14.3.3 UFBGA 72 Balls

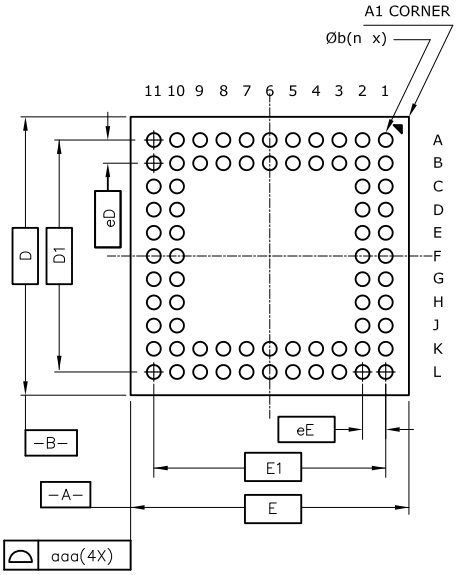
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	0.600	
A1	0.105	-----	0.205	
E/D	6.00 / 6.00			
E1/D1	5.00 / 5.00			
b	0.225	-----	0.325	
eD/eE	Ball pitch : 0.500			
M	Mold thickness : 0.250 ref			
S	Subst thickness : 0.136 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Copla : 0.080			
ball diam	0.250			
n	72			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, for proper dimensions, tolerances, datums, etc.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

05/02/2013

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	7C, 72-ball (11x11 array, 2 Out. rings), 0.5mm pitch, 6x6x0.6mm Ultra Thin Fine-Pitch Ball Grid Array Package (UFBGA)	CAD	7C	B

Appendix A. QMatrix Primer

A.1 Acquisition Technique

QMatrix capacitive acquisition uses a series of pulses to deposit charge into a sampling capacitor, Cs. The pulses are driven on X lines from the controller. The rising edge of the pulse causes current to flow in the mutual capacitance, Cx, formed between the X line and a neighboring receiver electrode or Y line. While one X line is being pulsed, all others are grounded. This leads to excellent isolation of the particular mutual capacitances being measured [1], a feature that makes for good inherent touchscreen performance.

After a fixed number of pulses (known as the burst length) the sampling capacitor's voltage is measured to determine how much charge has accumulated. This charge is directly proportional to Cx and therefore changes if Cx [2] changes. The transmit-receive charge transfer process between the X lines and Y lines causes an electric field to form that loops from X to Y. The field itself emanates from X and terminates on Y. If the X and Y electrodes are fixed directly [3] to a dielectric material like plastic or glass, then this field tends to channel through the dielectric with very little leakage of the field out into free-space (that is, above the panel). Some proportion of the field does escape the surface of the dielectric, however, and so can be influenced during a touch.

When a finger is placed in close proximity (a few millimeters) or directly onto the dielectric's surface, some of this stray field and some of the field that would otherwise have propagated via the dielectric and terminated onto the Y electrode, is diverted into the finger and is conducted back to the controller chip via the human body rather than via the Y line.

This means that less charge is accumulated in Cs, and hence the terminal voltage present on Cs, after all the charge transfer pulses are complete, becomes less. In this way, the controller can measure changes in Cx during touch. This means that the measured capacitance Cx goes down during touch, because the coupled field is partly diverted by the touching object.

The spatial separation between the X and Y electrodes is significant to make the electric field to propagate well in relation to the thickness of the dielectric panel.

A.2 Moisture Resistance

A useful side effect of the QMatrix acquisition method is that placing a floating conductive element between the X and Y lines tends to increase the field coupling and so increases the capacitance Cx. This is the opposite change direction to normal touch, and so can be quite easily ignored or compensated for by the controller. An example of such floating conductive elements is the water droplets caused by condensation.

As a result, QMatrix-based touchscreens tend not to go into false detect when they are covered in small non-coalesced water droplets. Once the droplets start to merge, however, they can become large enough to bridge the field across to nearby ground return paths (for example, other X lines not currently driven, or ground paths in mechanical chassis components). When this happens, the screen's behavior can become erratic.

There are some measures used in these controllers to help with this situation, but in general there comes a point where the screen is so contaminated by moisture that false detections become inevitable. It should also be noted that uniform condensation soon becomes non-uniform once a finger has spread it around. Finger grease renders the water highly conductive, making the situation worse overall.

In general, QMatrix has industry-leading moisture tolerance but there comes a point when even the best capacitive touchscreen suffers due to moisture on the dielectric surface.

1. A common problem with other types of capacitive acquisition technique when used for touchscreens, is that this isolation is not so pronounced. This means that when touching one region of the screen, the capacitive signals also tend to change slightly in nearby nodes too, causing small but often significant errors in the reported touch position.
2. To a first approximation.
3. Air gaps in front of QMatrix sensors massively reduce this field propagation and kill sensitivity. Normal optically clear adhesives work well to attach QMatrix touchscreens to their dielectric front panel.

A.3 Interference Sources

A.3.1 Power Supply

The device can tolerate short-term power supply fluctuations. If the power supply fluctuates slowly with temperature, the device tracks and compensate for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism is not able to keep up, causing sensitivity anomalies or false detections.

If power supply noise is present (usually caused by LEDs, relays, or other high current devices) and affects the measurement results then a separate Low Dropout (LDO) type regulator should be used for the AVdd power supply.

It is recommended that all ceramic decoupling capacitors on supply lines are placed very close (<5 mm) to the chip. A bulk capacitor of at least 2.2 µF and a higher frequency capacitor of around 10 nF to 100 nF in parallel are recommended; both must be X7R or X5R dielectric capacitors.

A.3.2 Other Noise Sources

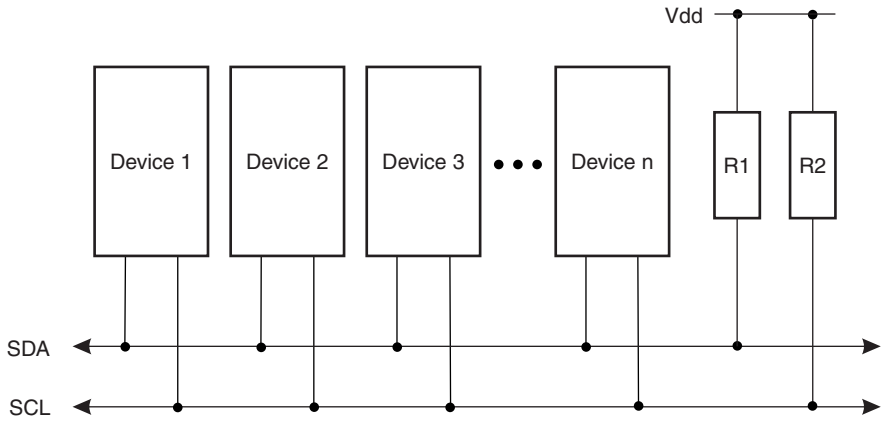
Refer to QTAN0079, *Buttons, Sliders and Wheels Sensor Design Guide*, for information (downloadable from the Touch Technology area of the Atmel website).

Appendix B. I²C Basics (I²C Operation)

B.1 Interface Bus

The device communicates with the host over an I²C bus. The following sections give an overview of the bus; more detailed information is available from www.nxp.com/documents/user_manual/UM10204.pdf. Devices are connected to the I²C bus as shown in Figure B-1. Both bus lines are connected to Vdd via pull-up resistors. The bus drivers of all I²C devices must be open-drain type. This implements a wired AND function that allows any and all devices to drive the bus, one at a time. A low level on the bus is generated when a device outputs a zero.

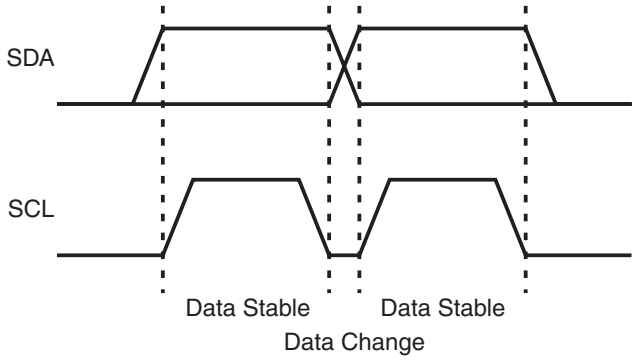
Figure B-1. I²C Interface Bus



B.2 Transferring Data Bits

Each data bit transferred on the bus is accompanied by a pulse on the clock line. The level of the data line must be stable when the clock line is high; the only exception to this rule is for generating START and STOP conditions.

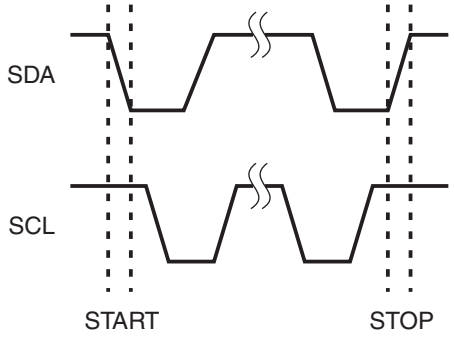
Figure B-2. Data Transfer



B.3 START and STOP Conditions

The host initiates and terminates a data transmission. The transmission is initiated when the host issues a START condition on the bus, and is terminated when the host issues a STOP condition. Between the START and STOP conditions, the bus is considered busy. As shown in Figure B-3, START and STOP conditions are signaled by changing the level of the SDA line when the SCL line is high.

Figure B-3. START and STOP Conditions

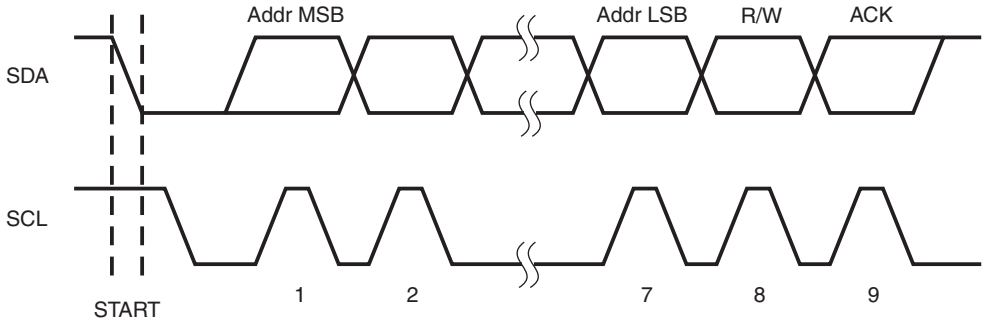


B.4 Address Byte Format

All address bytes are 9 bits long, consisting of 7 address bits, one READ/WRITE control bit and an acknowledge bit. If the READ/WRITE bit is set, a read operation is performed, otherwise a write operation is performed. When the device recognizes that it is being addressed, it will acknowledge by pulling SDA low in the ninth SCL (ACK) cycle. An address byte consisting of a slave address and a READ or a WRITE bit is called SLA+R or SLA+W, respectively.

The most significant bit of the address byte is transmitted first. The address sent by the host must be consistent with that selected with the option jumpers.

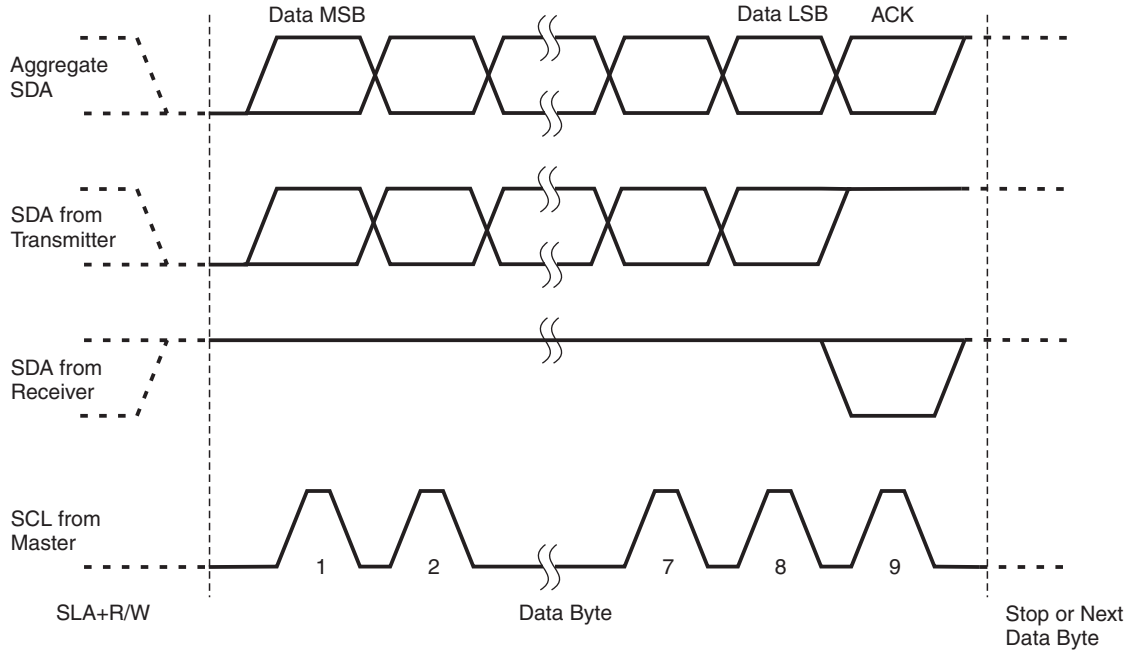
Figure B-4. Address Byte Format



B.5 Data Byte Format

All data bytes are 9 bits long, consisting of 8 data bits and an acknowledge bit. During a data transfer, the host generates the clock and the START and STOP conditions, while the receiver is responsible for acknowledging the reception. An acknowledge (ACK) is signaled by the receiver pulling the SDA line low during the ninth SCL cycle. If the receiver leaves the SDA line high, a NACK is signaled.

Figure B-5. Data Byte Format



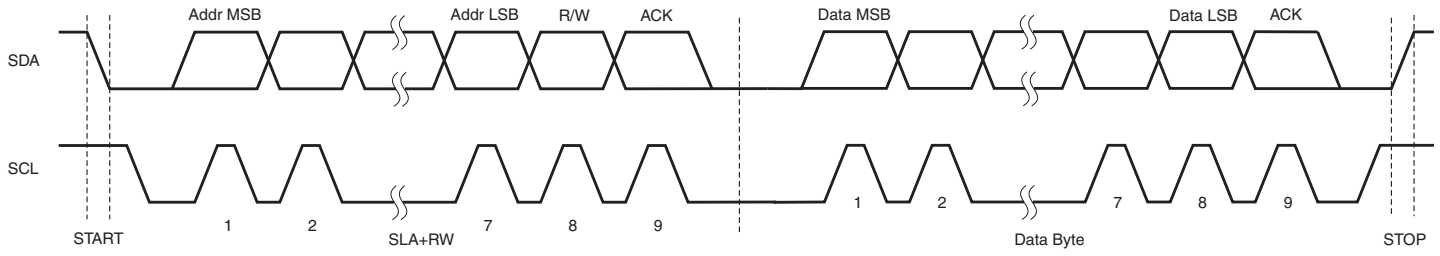
B.6 Combining Address and Data Bytes into a Transmission

A transmission consists of a START condition, an SLA+R/W, one or more data bytes and a STOP condition. The wired “ANDing” of the SCL line is used to implement handshaking between the host and the device. The device extends the SCL low period by pulling the SCL line low whenever it needs extra time for processing between the data transmissions.

Note: Each write or read cycle must end with a stop condition. The device may not respond correctly if a cycle is terminated by a new start condition.

Figure B-6 shows a typical data transmission. Note that several data bytes can be transmitted between the SLA+R/W and the STOP.

Figure B-6. Byte Transmission



Appendix C. Glossary of Terms

Channel

See **Node**.

Jitter

The peak-to-peak variance in the reported location for an axis when a fixed touch is applied. Typically jitter is random in nature and has a Gaussian [1] distribution, therefore measurement of peak-to-peak jitter must be conducted over some period of time, typically a few seconds. Jitter is typically measured as a percentage of the axis in question.

For example a 100 × 100 mm Touchscreen that shows ±0.5% jitter in X and ±1% jitter in Y would show a peak deviation from the average reported coordinate of ±0.5 mm in X and ±1 mm in Y. Note that by defining the jitter relative to the average reported coordinate, the effects of linearity are ignored.

Linearity

The measurement of the peak-to-peak deviation of the reported touch coordinate in one axis relative to the absolute position of touch on that axis. This is often referred to as the nonlinearity. Non-linearity in either X or Y axes manifest themselves as regions where the perceived touch motion along that axis (alone) is not reflected correctly in the reported coordinate giving the sense of moving too fast or too slow. Linearity is measured as a percentage of the axis in question.

For each axis, a plot of the true coordinate versus the reported coordinate should be a perfect straight line at 45°. A non-linearity makes this plot deviate from this ideal line. It is possible to correct modest non-linearity using on-chip linearization tables, but this correction trades linearity for resolution in regions where stronger corrections are needed (because there is a stretching or compressing effect to correct the nonlinearity, so altering the resolution in these regions). Linearity is typically measured using data that has been sufficiently filtered to remove the effects of jitter. For example, a 100 mm slider with a nonlinearity of ±1% reports a position that is, at most, 1 mm away in either direction from the true position.

Multitouch

The ability of a touchscreen to report multiple concurrent touches. The touches are reported as separate sets of XY co-ordinates.

Node

One of the capacitive measurement points at which the sensor controller can detect capacitive change.

Resolution

The measure of the smallest movement on a slider or touchscreen in an axis that causes a change in the reported coordinate for that axis. Resolution is normally expressed in bits and tends to refer to resolution across the whole axis in question. For example, a resolution of 10 bits can resolve a movement of 0.0977 mm on a slider 100 mm long. Jitter in the reported position degrades usable resolution.

Touchscreen

A two-dimensional arrangement of electrodes whose capacitance changes when touched, allowing the location of touch to be computed in both X and Y axes. The output from the XY computation is a pair of numbers, typically 12-bits each, ranging from 0 to 4095, representing the extents of the touchscreen active region.

1. Sometimes called Bell-shaped or Normal distribution.

Associated Documents

Note: The documents listed below are available under NDA only. In addition, some documents may have further restrictions placed upon them.

For information on using and configuring the device, see the following:

- *mXT336T 1.0 Protocol Guide* (distributed with Atmel approval only)

The following documents may also be useful (available by contacting Atmel Touch Technology Division):

- **Touchscreen design and PCB/FPCB layout guidelines:**
  - Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
  - Application Note: MXTAN0208 – *Design Guide for PCB Layouts for Atmel Touch Controllers*
  - Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*
- **Configuring the device:**
  - Application Note: QTAN0078 – *maXTouch Stylus Tuning*
  - Application Note: QTAN0059 – *Using the maXTouch Self Test Feature*
  - Application Note: QTAN0070 – *Recovering from Palm Touches During Calibration with maXTouch Touchscreen Controllers*
- **Miscellaneous:**
  - Application Note: QTAN0050 – *Using the maXTouch Debug Port*
  - Application Note: QTAN0058 – *Rejecting Unintentional Touches with the maXTouch Touchscreen Controllers*
  - Application Note: QTAN0061 – *maXTouch Sensitivity Effects for Mobile Devices*
  - Application Note: QTAN0083 – *Power and Speed Considerations*
  - Application Note: QTAN0051 – *Bootloading Procedure for Atmel Touch Sensors Based on the Object Protocol*
- **Tools:**
  - QTAN0101 – Object Server User Guide

Revision History

Revision Number	History
Revision ASX– October 2013	Initial edition for firmware revision 1.0 – Summary
Revision BSX– November 2013	• Pinout information updated with GPIO pins • EXTCAP pins renumbered from 0 • Schematics updated with additional GPIO pins and additional notes
Revision CSX – December 2013	• VDDIN renamed to VDD
Revision DX – June 2014	Updated for general distribution – Released
Revision EX – June 2014	• Schematic for 64-ball BGA updated to show correct X line pins • Section on Single Supply Operation updated • Specification for power ripple and noise added • Other minor edits
Revision FX – June 2014	• Changed RESV pin (15 on UFQFN56, H8 on UFBGA-64, K8 on UFBGA-72) *if unused* description for future compatibility
Revision GX – July 2014	Updated for general distribution for firmware revision 1.0.AB – Released • Updated power figures • Added QS numbers for firmware revision 1.0.AB
Revision HX – January 2015	Updated for general distribution for firmware revision 1.0.AB – Released • Revised voltage regulator recommendations
Revision IX – February 2015	• Updated Power-up /Reset Requirements section

Notes

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