CENTELLAX

0.04 - 30GHz Broadband MMIC Low-Power Amplifier

Application

The UATS30S1C Broadband MMIC Low-Power Amplifier is designed for high efficiency broadband applications in RF and microwave communications, test equipment and military systems. By using specific external components, the bandwidth of operation can be extended below 40MHz.

Description

The UATS30S1C is an eight stage traveling wave amplifier. The amplifier has been designed for low power dissipation, high drain efficiency, and low mid-band noise figure. The amplifier typically requires 383mW (4.5V, 85mA) to deliver 10.5dB gain and 16.5dBm output power.

Features

The UATS30S1C has >30dB dynamic gain control.

Device Highlights

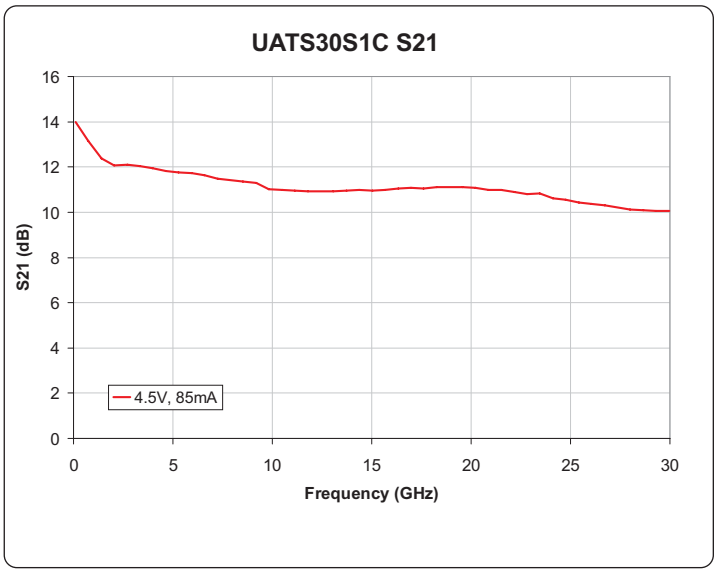
- Very low power dissipation:
  - 4.5V, 85mA (383mW)
  - High drain efficiency (43dBm/W)
- Good 1.5-20GHz performance:
  - Flat gain (11 ± 0.75dB)
  - 16.5dBm P_{sat}, 14dBm P_{-1dB}
- Good input / output return loss
- High isolation (20dBm)
- >30dB dynamic gain control
- 100% DC, RF, and visually tested
- Size: 1640x835um (64.6x32.9mil)

Key Specifications

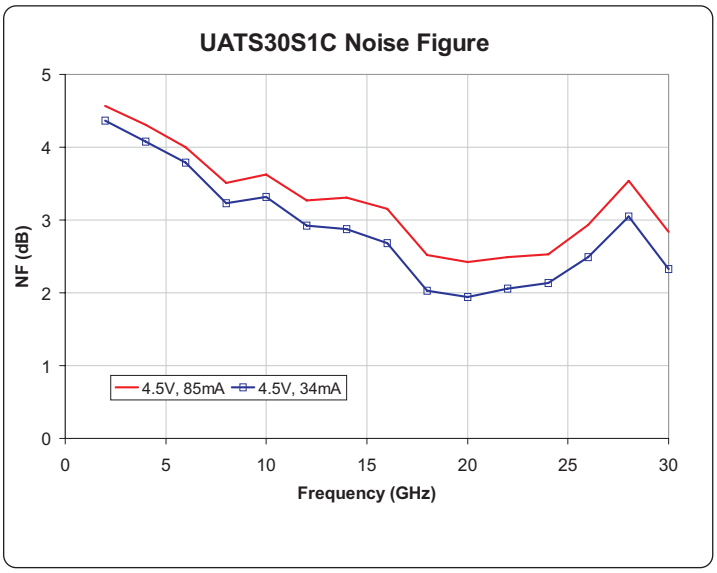
Vdd=4.5V, Idd=85mA, Zo=50Ω

Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

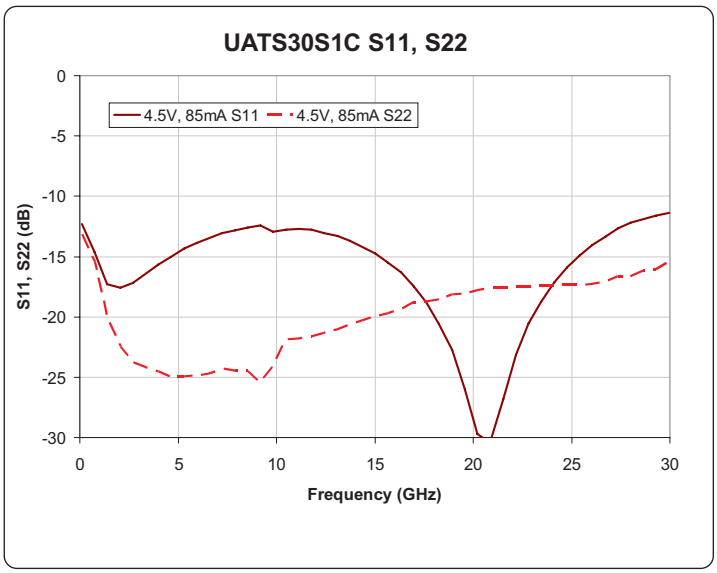
		1.5 - 20GHz			0.04 - 30GHz		
Parameter	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
S21 (dB)	Small Signal Gain	9.5	11		9	10.5	
Flatness (±dB)	Gain Flatness		0.75	1.0		1.5	1.75
S11 (dB)	Input Match		-14	-10		-13	-10
S22 (dB)	Output Match		-20	-15		-20	-15
S12 (dB)	Reverse Isolation		-26	-20		-24	-20
P_{-1dB} (dBm)	1dB Compressed Output Power	12.5	14		12.5	14	
P_{sat} (dBm)	Saturated Output Power	15	16.5		15	16.5	
P_{out} @8dB (dBm)	Output Power at 8dB Gain	14.5	16		14.5	16	
NF (dB)	Noise Figure		4.5			4.5	



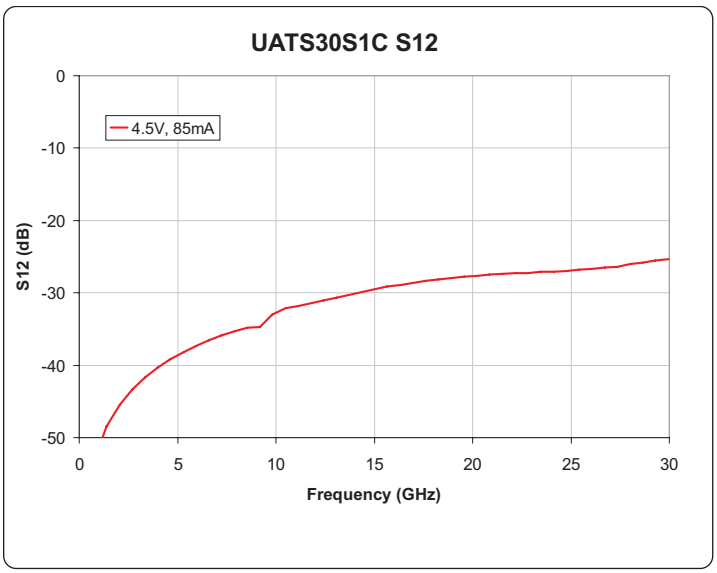
Typical IC performance measured on-wafer



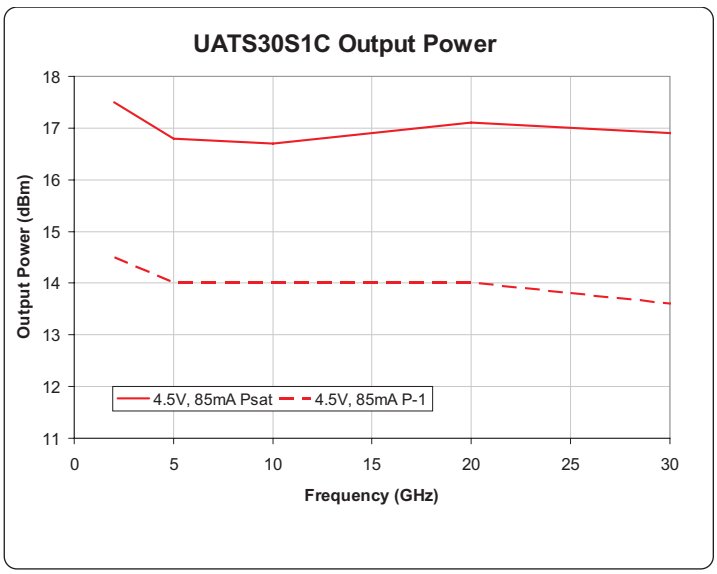
Typical IC performance with package de-embedded



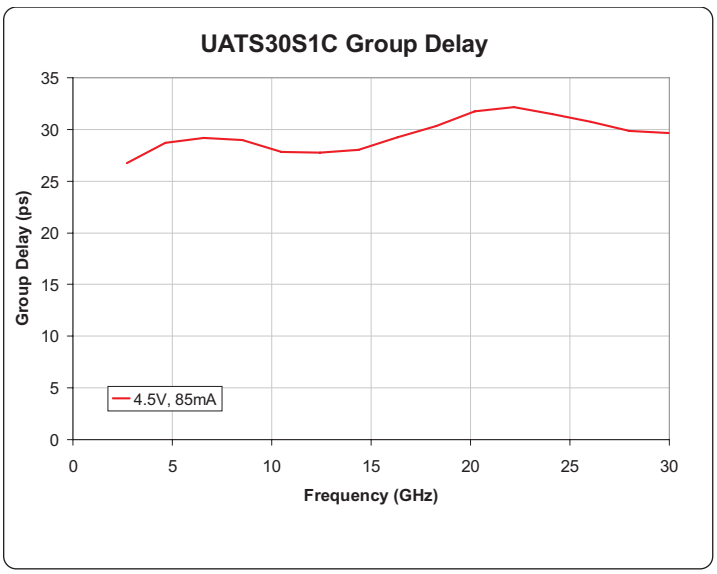
Typical IC performance measured on-wafer



Typical IC performance measured on-wafer



Typical IC performance measured on-wafer



Typical IC performance measured on-wafer

Typical measurement data is available upon request. Email support@centellax.com for more information.

Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vdd	Drain Bias Voltage	3V	4.5V	7.5V
Idd	Drain Bias Current	—	85mA	120mA
Vg1	1st Gate Bias Voltage	-4V	—	+0.5V
Vg2	2nd Gate Bias Voltage	Vdd-Vg2<7V	N/C	+4V
P_{in}	Input Power (CW)			20dBm
P_{dc}	Power Dissipation		0.383W	
T_{ch}	Channel Temperature			150°C
Θ_{ch}	Thermal Resistance (T_{case}=85°C)		22°C/W	

DC Bias

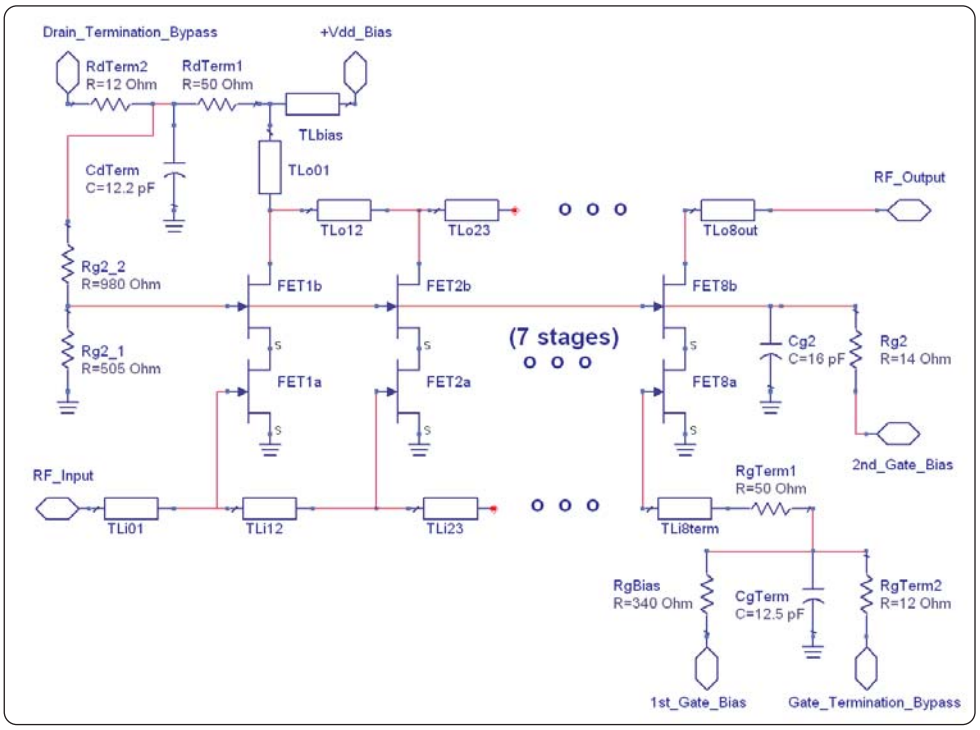
The UATS30S1C is biased by applying a positive voltage to the drain (Vdd), then setting the drain current (Idd) using a negative voltage on the gate (Vg1).

When zero volts is applied to the gate, the drain to source channel is open; this results in high Idd. When Vg1 is biased negatively, the channel is pinched off and Idd decreases.

The nominal bias is Vdd=4.5V, Idd=85mA. Improved noise or power performance can be achieved with application-specific biasing.

Gain Control

Dynamic gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to the second gate (Vg2) reduces amplifier gain.



Low-Frequency Use

The UATS30S1C has been designed so that the bandwidth can be extended to low frequencies. The low end corner frequency of the device is primarily determined by the external biasing and AC coupling circuitry.

Matching

The amplifier incorporates on-chip termination resistors on the RF input and output. These resistors are RF grounded through on-chip capacitors, which are small and become open circuits at frequencies below 1GHz.

A pair of gate and drain termination bypass pads are provided for connecting external capacitors required for the low frequency extension network. These capacitors should be 10x the value of the DC blocking capacitors.

DC Blocks

The amplifier is DC coupled to the RF input and output pads; DC voltage on these pads must be isolated from external circuitry.

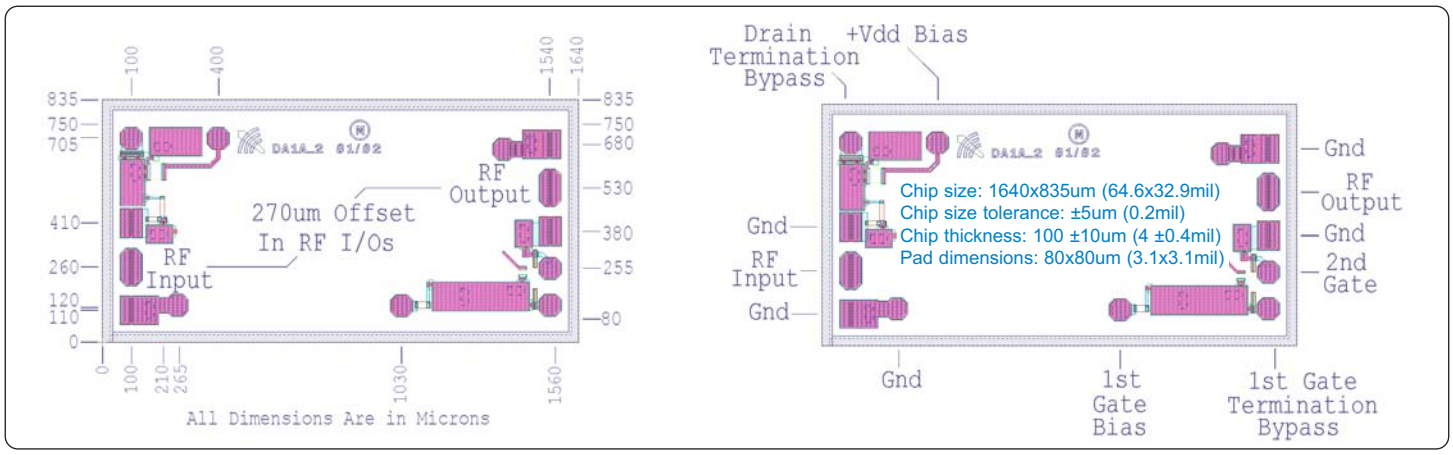
For operation above 2GHz, a series DC-blocking capacitor with minimum value of 20pF is recommended; operation above 40MHz requires a minimum of 120pF.

Inductor Bias

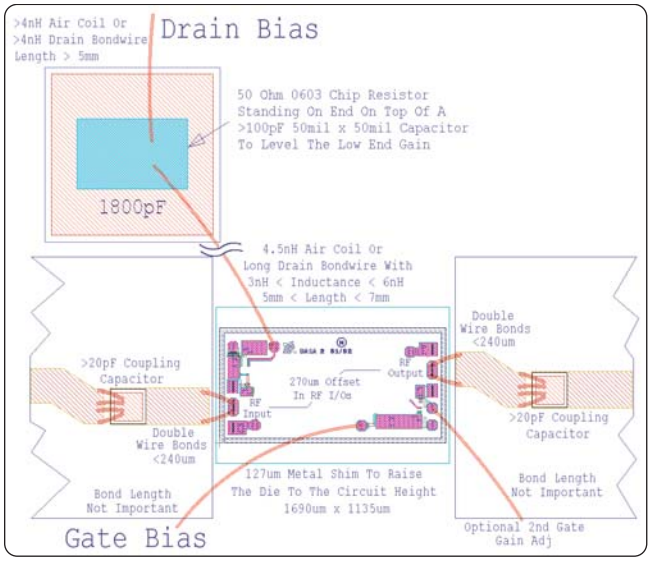
DC bias applied to the drain (Vdd) must be decoupled with an off-chip RF choke inductor. The amount of bias inductance will determine the low frequency operating point. Inductive biasing can also be applied to the chip through the RF output.

For many applications above 2GHz, a bondwire from the Vdd pad will suffice as the biasing inductor. Ensure the correct bond length as shown in the assembly diagrams.

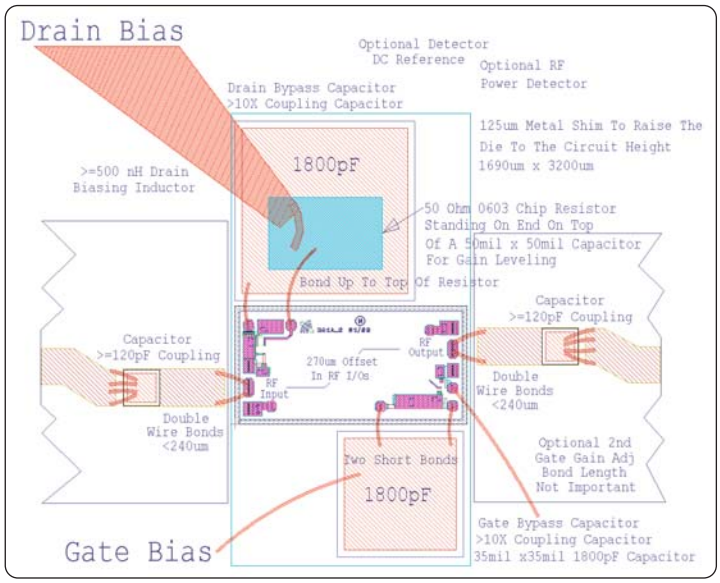
UATS30S1C Datasheet



Die size, pad locations, and pad descriptions



2 - 30GHz bonding diagram



40MHz - 30GHz bonding diagram

Applications Support

Alternate assembly diagrams and other additional application support are available upon request. Visit the Centellax website for large printable assembly diagrams and application notes: http://www.centellax.com/products/microwave/mmics/UATS30S1C.shtml.

Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center**; handle from edges or with a collet.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please visit our website for more handling, die attach and bonding information: http://www.centellax.com/.

Recommended Components

>20pF 10x10mil DC Block:
Presidio SL1010X7R101M16VH

1800pF 50x50mil Drain Bypass:
Presidio SL5050X7R182M16VH

>120pF 10x10mil DC Block:
Presidio SL1010X7R181M16VH

Drain Bias Inductor:
Piconics CC21T36K240G5

1800pF 35x35mil Gate Bypass:
Presidio SL3535X7R182M16VH

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