# UAPL65SC Datasheet

CENTELLAX

# 0.04 - 65GHz Broadband MMIC Medium-Power Amplifier with PLFX

## Application

The UAPL65SC Broadband MMIC Medium-Power Amplifier with PLFX is designed for broadband power applications in RF and microwave communications, test equipment and military systems. By using specific external components, the bandwidth of operation can be extended below 40MHz.

## Description

The UAPL65SC is an eight stage traveling wave amplifier. The amplifier features Centellax PLFX (Passive Low Frequency eXtension) circuitry designed to reduce the integration cost of the amplifier. PLFX isolates the amplifier from bias inductor resonances, allowing use of a less-expensive coil.

## Features

The UAPL65SC has >30dB dynamic gain control, includes a temperature-referenced power detector output, and features patented PLFX technology.

## Device Highlights

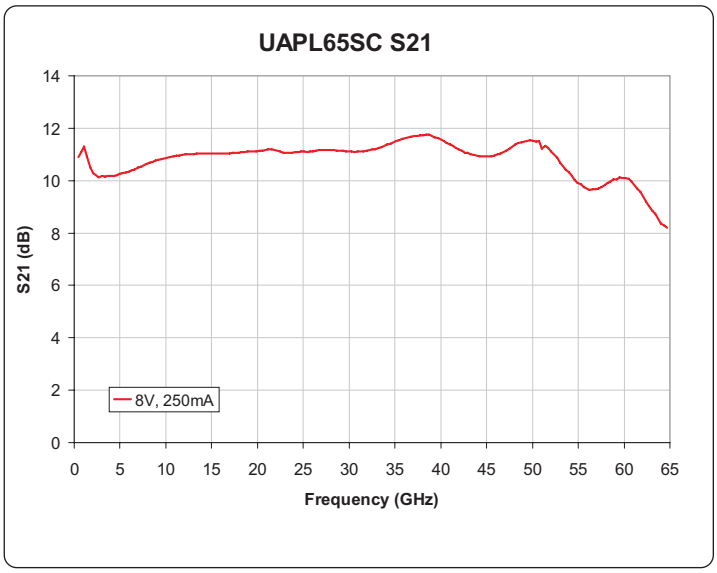
- Integrated PLFX technology:
  - Allows use of less-expensive coil
- Excellent 0.04-50GHz performance:
  - 9.5 ± 0.75dB gain
  - 19.5dBm $P_{sat}$, 16.5dBm $P_{-1dB}$
  - 11dB return loss
- Broadband 65GHz performance:
  - 7.5dB gain, 9dB return loss
- >30dB dynamic gain control
- Integrated power detector
- 100% DC, RF, and visually tested
- Size: 1640x920um (64.6x36.2mil)

## Key Specifications

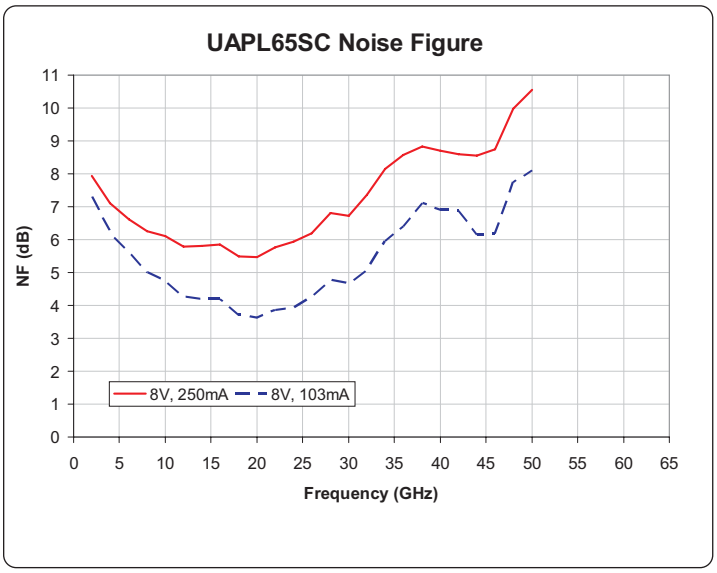
Vdd=8V, Idd=250mA, Zo=50Ω

Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

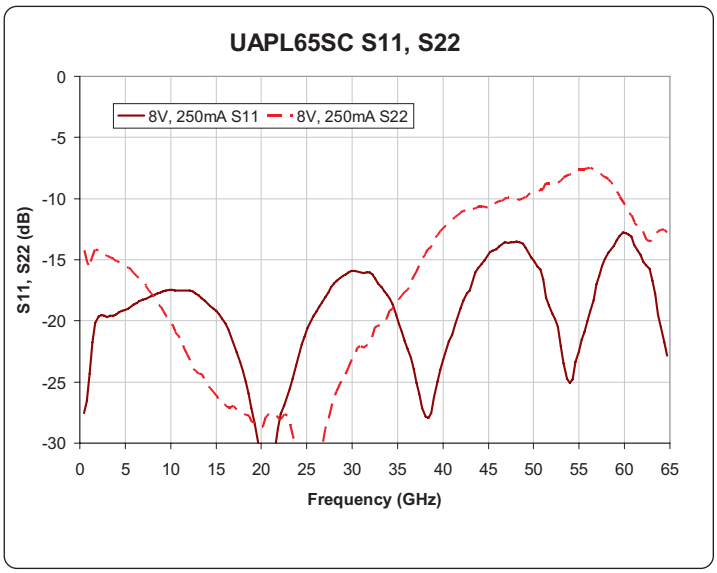
| | | 1.5 - 40GHz | | | 0.04 - 50GHz | | | 0.04 - 65GHz | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| S21 (dB) | Small Signal Gain | 8.5 | 10 | | 8.5 | 9.5 | | 6 | 7.5 | |
| Flatness (±dB) | Gain Flatness | | 0.75 | 1.25 | | 0.75 | 1.25 | | | |
| S11 (dB) | Input Match | | -16 | -12 | | -16 | -12 | | -14 | -10 |
| S22 (dB) | Output Match | | -13 | -10 | | -11 | -8 | | -9 | -7 |
| S12 (dB) | Reverse Isolation | | -25 | -22 | | -20 | -17 | | -18 | -15 |
| $P_{-1dB}$ (dBm) | 1dB Compressed Output Power | 16.5 | 18 | | 15 | 16.5 | | | | |
| $P_{sat}$ (dBm) | Saturated Output Power | 21 | 22.5 | | | 19.5 | | | | |
| NF (dB) | Noise Figure | | 9 | | | 10.5 | | | | |
| $RF_{det}$ (mV/mW) | RF Detector Sensitivity | | 0.8 | | | 0.8 | | | | |



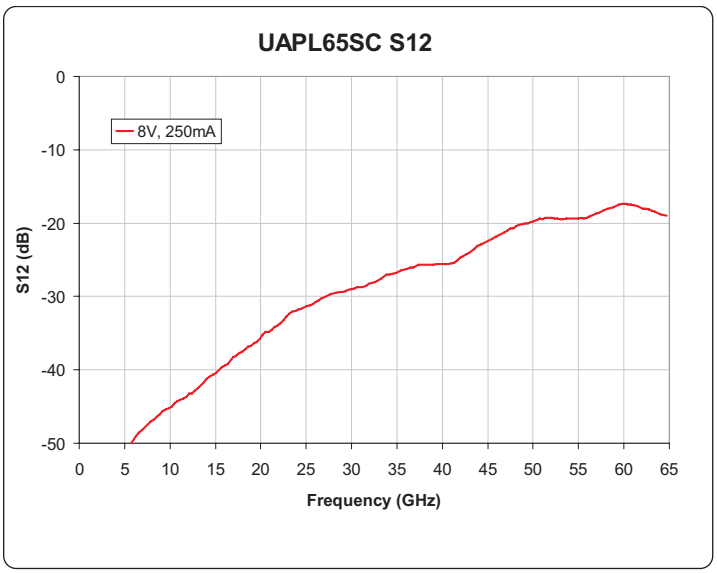

*Typical IC performance measured on-wafer*



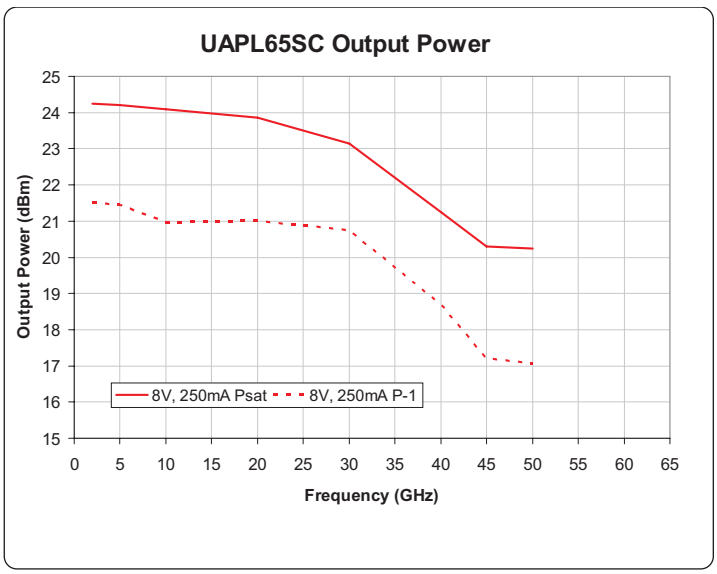

*Typical IC performance with package de-embedded*



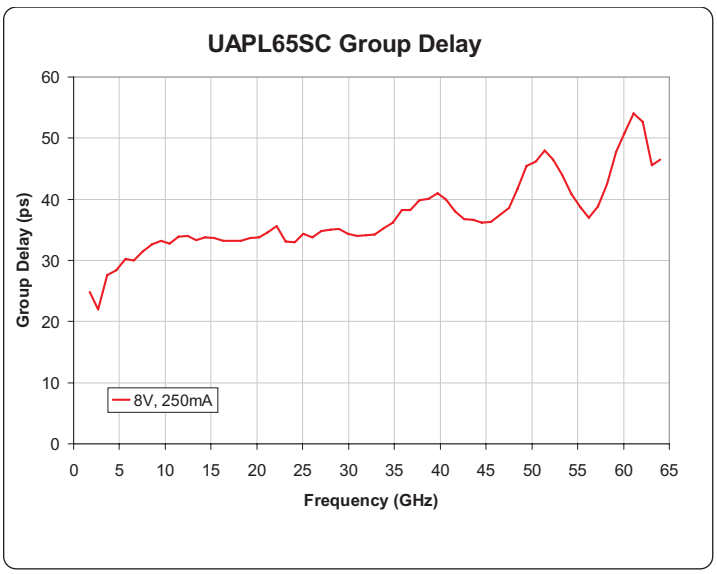

*Typical IC performance measured on-wafer*




*Typical IC performance measured on-wafer*




*Typical IC performance measured on-wafer*




*Typical IC performance measured on-wafer*

Typical measurement data is available upon request. Email support@centellax.com for more information.

## Supplemental Specifications

| Parameter | Description | Min | Typ | Max |
|---|---|---|---|---|
| Vdd | Drain Bias Voltage | — | 8V | 8.2V |
| Idd | Drain Bias Current | — | 250mA | 300mA |
| Vg1 | 1st Gate Bias Voltage | -4V | — | +0.5V |
| Vg2 | 2nd Gate Bias Voltage | Vdd-Vg2<7V | N/C | +4V |
| $P_{in}$ | Input Power (CW) | | | 23dBm |
| $P_{dc}$ | Power Dissipation | | 2W | |
| $T_{ch}$ | Channel Temperature | | | 150°C |
| $\Theta_{ch}$ | Thermal Resistance ($T_{case}$=85°C) | | 21°C/W | |

## DC Bias

The UAPL65SC features a patented on-chip passive bias circuit called 'PLFX'. This circuit isolates the amplifier from bias coil resonances above 14GHz, allowing the use of less expensive coils; traditional biasing requires bias coils with self-resonances outside the operating range of the amplifier.

The device is biased by applying a positive voltage to the drain (Vdd), then setting the drain current (Idd) using a negative voltage on the gate (Vg1). The nominal bias is Vdd=8V, Idd=250mA.

Improved performance can be achieved with gate bias adjustment; use the drain termination bypass to alter the output voltage (detected from the drain sense).

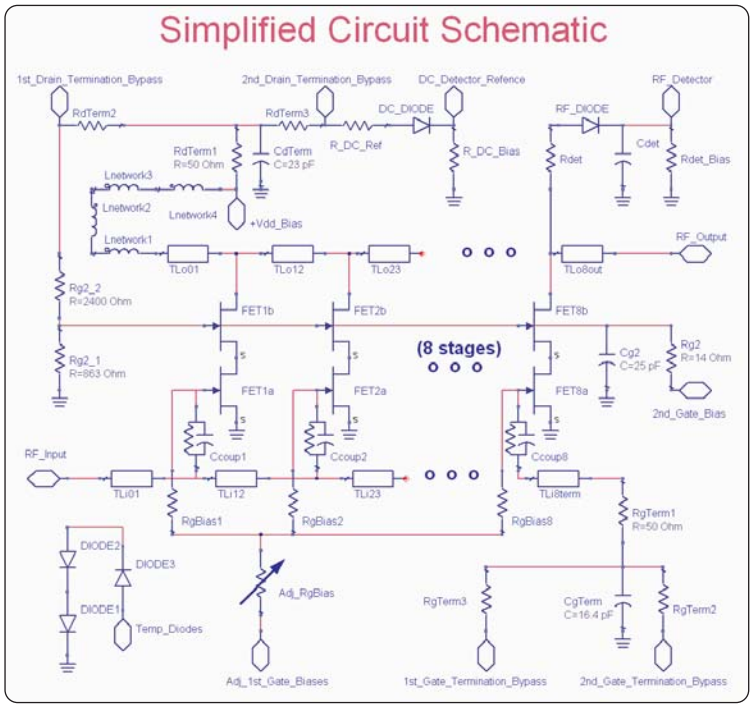
## Gain Control

Dynamic gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to the second gate (Vg2) reduces amplifier gain.

## RF Power Detection

RF output power can be calculated from the difference between the RF detector voltage and the DC detector voltage, minus a DC offset. Please consult the application note available on the Centellax website.

### Simplified Circuit Schematic




## Low-Frequency Use

The UAPL65SC has been designed so that the bandwidth can be extended to low frequencies. The low end corner frequency of the device is primarily determined by the external biasing and AC coupling circuitry.

## Matching

The amplifier incorporates on-chip termination resistors on the RF input and output. These resistors are RF grounded through on-chip capacitors, which are small and become open circuits at frequencies below 1GHz.

A pair of gate and drain termination bypass pads are provided for connecting external capacitors required for the low frequency extension network. These capacitors should be 10x the value of the DC blocking capacitors.

## DC Blocks

The amplifier is DC coupled to the RF input and output pads; DC voltage on these pads must be isolated from external circuitry.

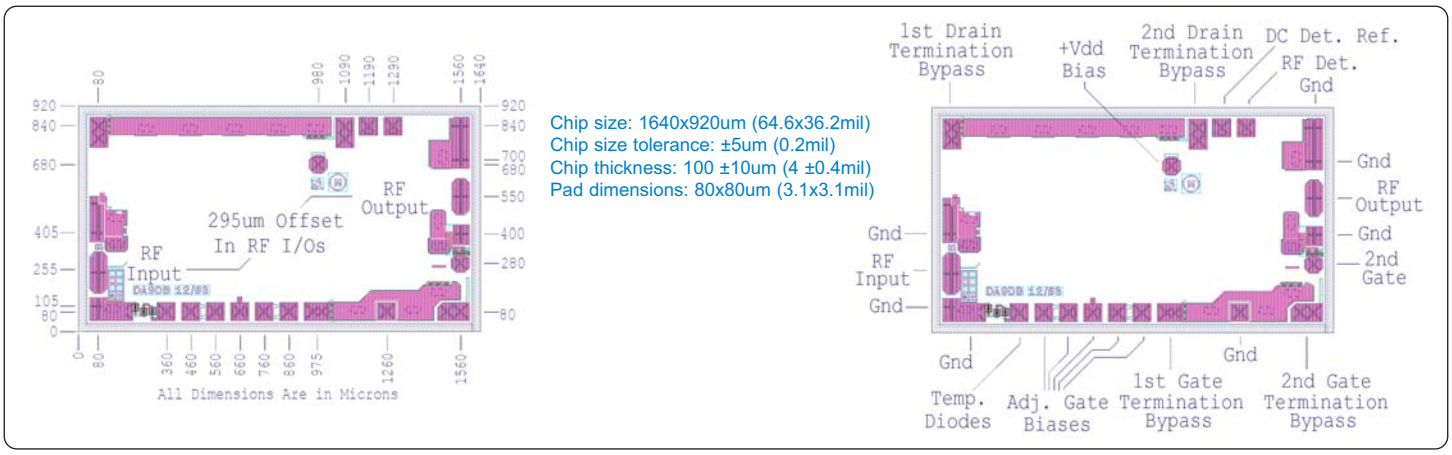
For operation above 2GHz, a series DC-blocking capacitor with minimum value of 20pF is recommended; operation above 40MHz requires a minimum of 120pF.

## Inductor Bias

DC bias applied to the drain (Vdd) must be decoupled with an off-chip RF choke inductor. The amount of bias inductance will determine the low frequency operating point. Inductive biasing can also be applied to the chip through the RF output.

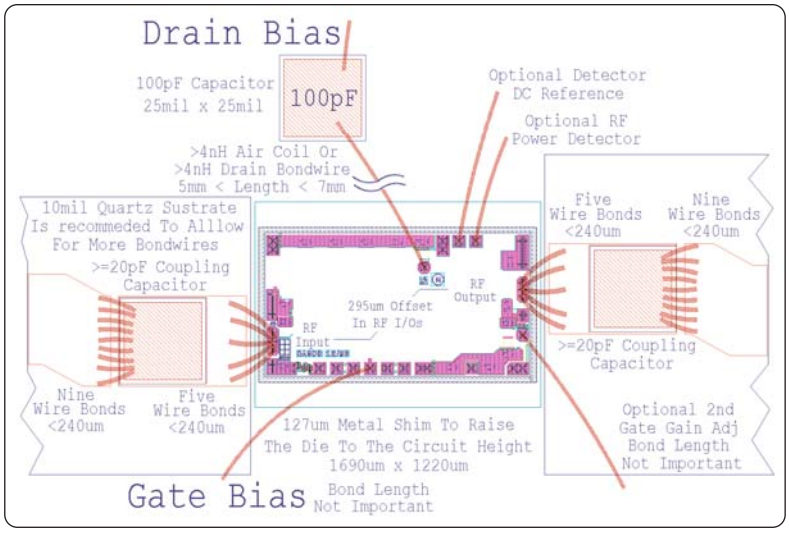
For many applications above 2GHz, a bondwire from the Vdd pad will suffice as the biasing inductor. Ensure the correct bond length as shown in the assembly diagrams.

# UAPL65SC Datasheet

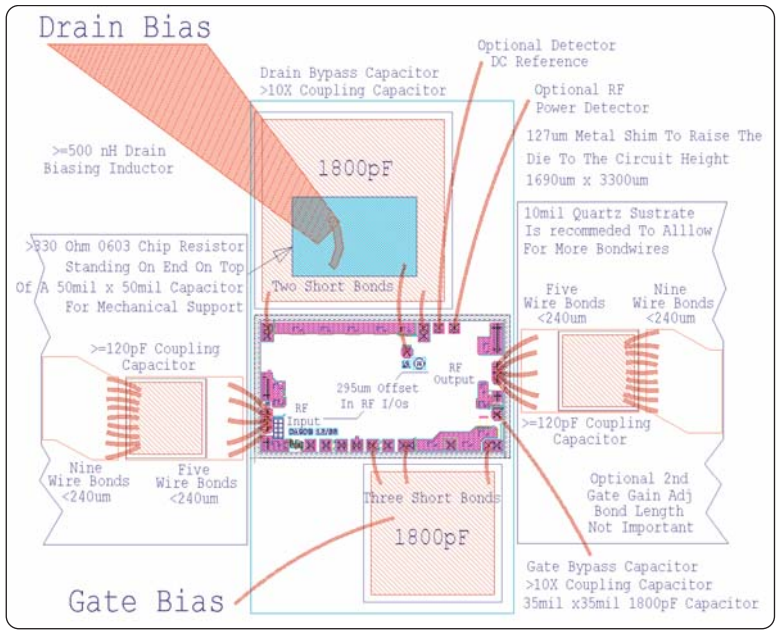



Chip size: 1640x920um (64.6x36.2mil)
Chip size tolerance: ±5um (0.2mil)
Chip thickness: 100 ±10um (4 ±0.4mil)
Pad dimensions: 80x80um (3.1x3.1mil)

*Die size, pad locations, and pad descriptions*




*2 - 65GHz bonding diagram*




*40MHz - 65GHz bonding diagram*

## Applications Support

Alternate assembly diagrams and other additional application support are available upon request. Visit the Centellax website for large printable assembly diagrams and application notes: http://www.centellax.com/products/microwave/mmics/UAPL65SC.shtml.

## Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center**; handle from edges or use a collet.

## Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

## ESD Handling and Bonding:

**This MMIC is ESD sensitive;** preventive measures should be taken during handling, die attach, and bonding.

**Epoxy die attach is recommended**. Please visit our website for more handling, die attach and bonding information: http://www.centellax.com/.

## Recommended Components

>20pF 20x20mil DC Block:
Presidio SL2020X7R101M16VH

100pF 25x25mil Drain Bypass:
Presidio SL2525X7R101M16VH

Drain Bias Inductor:
Piconics CC21T36K240G5

>120pF 20x20mil DC Block:
Presidio SL2020X7R181M16VH

1800pF Drain/Gate Bypass:
35x35mil Presidio SL3535X7R182M16VH
50x50mil Presidio SL5050X7R182M16VH

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