Atmel ATPL220A

PRIME compliant Power Line Communications SoC

DATASHEET

Features

- Modem
  - Power Line Carrier Modem for 50 and 60 Hz mains
  - 97-carrier OFDM PRIME compliant
  - Baud rate Selectable: 21400 to 128600 bps
  - Differential BPSK, QPSK, 8-PSK modulations
- Memory
  - 32Kbytes on-chip SRAM
- Automatic Gain Control and signal amplitude tracking
- Embedded on-chip DMAs
- Media Access Control
  - Viterbi decoding and CRC PRIME compliant
  - 128-bit AES encryption
  - Channel sensing and collision pre-detection
- Package
  - 120-lead LQFP, 14 x 14 mm, pitch 0.4 mm
  - Pb-free and RoHS compliant
- Typical Applications
  - Automated Meter Reading (AMR) & Advanced Meter Management (AMM)
  - Street lighting
  - Home Automation

Description

ATPL220A is a PRIME (PoweRline Intelligent Metering Evolution) compliant ASIC specifically designed for PLC Base Nodes implementation. Systems using this ASIC support both mono-phase and multi-phase PLC injection. Mono-phase injection is achieved by means of a single ATPL220A device, whereas several ATPL220A can be combined to achieve multi-phase injection based on Atmel MIMO technology.

The combination of multi-phase injection and Atmel MIMO technology increases PRIME Base Nodes performance, resulting in outstanding robustness and network coverage.

ATPL220A has been conceived to be easily managed by an external microcontroller by means of an SPI interface. The external microcontroller implements Base Node upper layers (as specified in PRIME standard) while ATPL220A carries out PHY layer functionalities.

Line coupling front end design is extremely simplified, resulting in a very low cost bill of materials.

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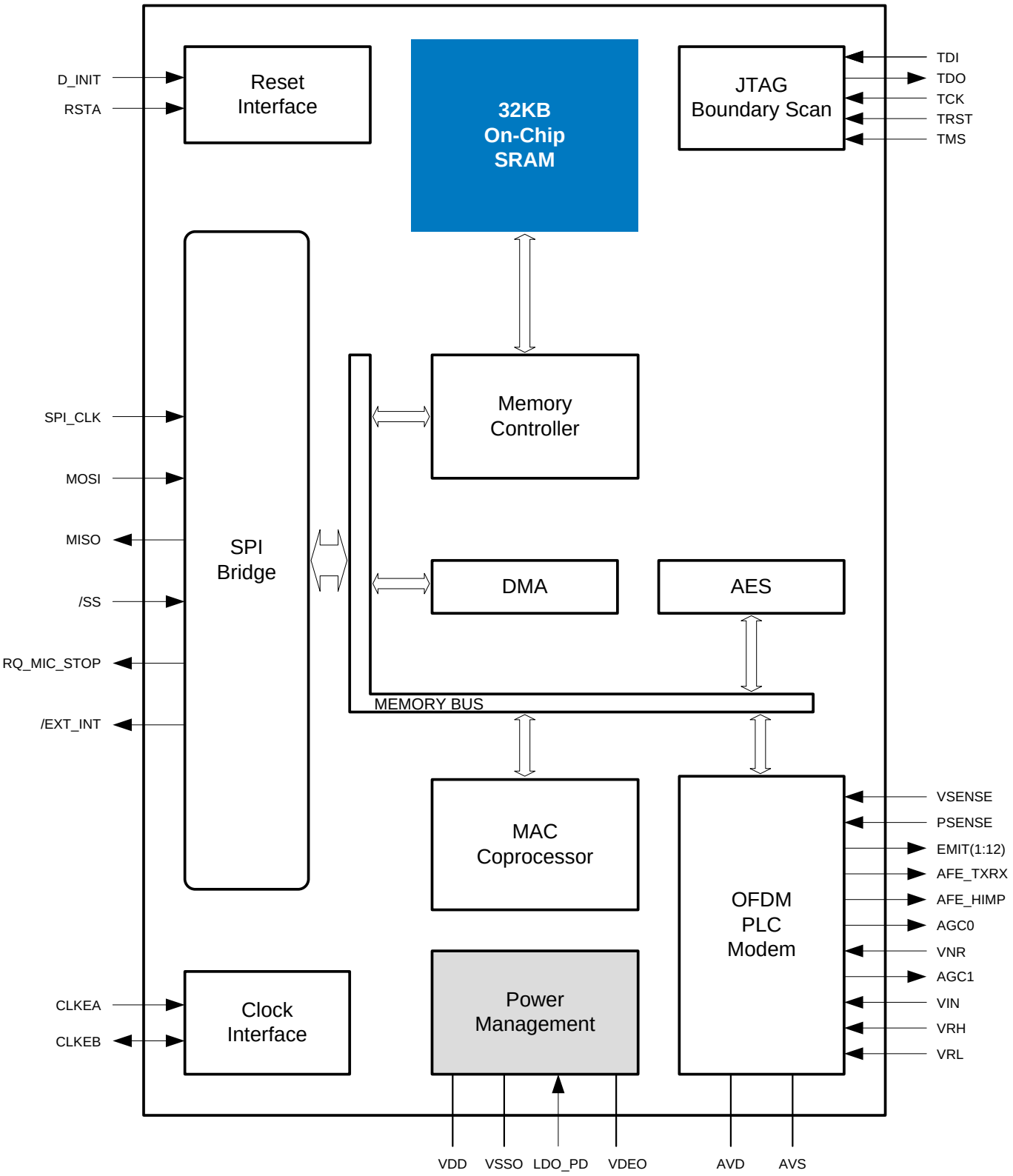
1. Block Diagram

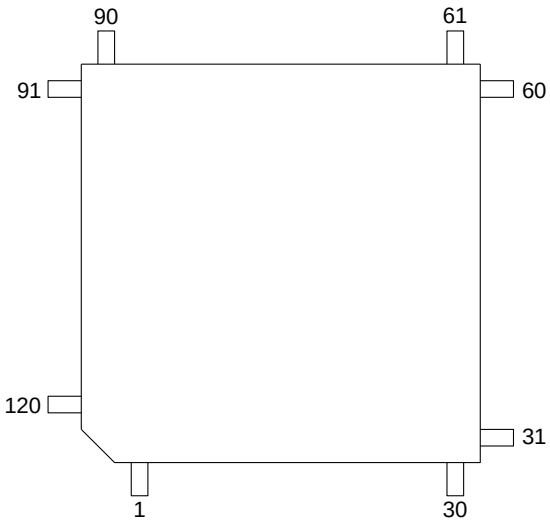
Figure 1-1. ATPL220A 120-pin Block Diagram



2. Package and Pinout

2.1 120-Lead LQFP Package Outline

Figure 2-1. Orientation of the 120-Lead Package



2.2 120-Lead LQFP Pinout

Table 2-1. ATPL220A 120-Lead LQFP pinout

PinNo	Pin Name	I/O	I(mA)	Res	HY
1	NC	-	-	-	-
2	NC	-	-	-	-
3	GND	P	-	-	-
4	VCC	P	-	-	-
5	NC	-	-	-	-
6	NC	-	-	-	-
7	NC	-	-	-	-
8	NC	-	-	-	-
9	NC	-	-	-	-
10	NC	-	-	-	-
11	NC	-	-	-	-
12	NC	-	-	-	-
13	NC	-	-	-	-
14	VCC	P	-	-	-
15	GND	P	-	-	-
16	VDD	P	-	-	-
17	NC	-	-	-	-
18	NC	-	-	-	-
19	NC	-	-	-	-
20	NC	-	-	-	-
21	NC	-	-	-	-
22	NC	-	-	-	-
23	NC	-	-	-	-
24	NC	-	-	-	-
25	NC	-	-	-	-
26	GND	P	-	-	-
27	VCC	P	-	-	-
28	NC	-	-	-	-
29	NC	-	-	-	-
30	MISO	O	±5	PU	-
31	MOSI	I	±5	PU	-
32	SPICLK	I	±5	PU	-
33	/SS	I	±5	PU	-
34	RQ_MIC_STOP	O	±5	PU	-
35	/EXT_INT	O	±5	PU	-
36	VCC	P	-	-	-
37	GND	P	-	-	-
38	EMIT.1	O	±X	-	-

PinNo	Pin Name	I/O	I(mA)	Res	HY
39	EMIT.2	O	±X	-	-
40	EMIT.3	O	±X	-	-
41	EMIT.4	O	±X	-	-
42	VCC	P	-	-	-
43	GND	P	-	-	-
44	EMIT.5	O	±X	-	-
45	EMIT.6	O	±X	-	-
46	EMIT.7	O	±X	-	-
47	EMIT.8	O	±X	-	-
48	VCC	P	-	-	-
49	GND	P	-	-	-
50	EMIT.9	O	±X	-	-
51	EMIT.10	O	±X	-	-
52	EMIT.11	O	±X	-	-
53	EMIT.12	O	±X	-	-
54	VCC	P	-	-	-
55	GND	P	-	-	-
56	AFE_HIMP	O	±10	-	-
57	AFE_TXRX	O	±10	-	-
58	VSENSE	I	-	-	Y
59	PSENSE	I	-	-	Y
60	VNR	I	-	-	Y
61	TDI	I	-	PU	-
62	TMS	I	-	PU	-
63	TDO	O	±5	-	-
64	GND[1]	P	-	-	-
65	GND	P	-	-	-
66	VCC	P	-	-	-
67	TRST	I	-	PU	-
68	TCK	I	-	-	-
69	RSTA	I	-	PD	Y
70	D_INIT	I	-	PD	Y
71	GND	P	-	-	-
72	VCC	P	-	-	-
73	GND	P	-	-	-
74	VDD	P	-	-	-
75	LDO_PD	I	-	-	-
76	VSS0	P	-	-	-

PinNo	Pin Name	I/O	I(mA)	Res	HY
77	VDE0	P	-	-	-
78	VDE0	P	-	-	-
79	GND	P	-	-	-
80	GND	P	-	-	-
81	VCC	P	-	-	-
82	CLKEA	I	-	-	-
83	GND	P	-	-	-
84	CLKEB	I/O	-	-	-
85	VCC	P	-	-	-
86	NC	-	-	-	-
87	NC	-	-	-	-
88	GND	P	-	-	-
89	NC	-	-	-	-
90	NC	-	-	-	-
91	NC	-	-	-	-
92	NC	-	-	-	-
93	GND	P	-	-	-
94	AGC1	O	±10	-	-
95	AGC0	O	±10	-	-
96	GND	P	-	-	-
97	VCC	P	-	-	-
98	AVS2	P	-	-	-

PinNo	Pin Name	I/O	I(mA)	Res	HY
99	AVD2	P	-	-	-
100	AVS1	P	-	-	-
101	AVD1	P	-	-	-
102	VRH	I	-	-	-
103	VIN	I	-	-	-
104	VRL	I	-	-	-
105	GND	P	-	-	-
106	VCC	P	-	-	-
107	NC	-	-	-	-
108	NC	-	-	-	-
109	NC	-	-	-	-
110	NC	-	-	-	-
111	NC	-	-	-	-
112	NC	-	-	-	-
113	NC	-	-	-	-
114	GND	P	-	-	-
115	VCC	P	-	-	-
116	NC	-	-	-	-
117	NC	-	-	-	-
118	NC	-	-	-	-
119	NC	-	-	-	-
120	NC	-	-	-	-

Notes: 1. Mandatory to be tied down

I/O=pin direction: **I**=input, **O**=Output, **P**=Power

I(mA)=nominal current: **+**=source, **-**=sink, **X**=fixed by external resistor

RES=pin pullup/pulldown resistor: **PU**=pullup, **PD**=pulldown,

HY=Input Hysteresis

3. Pin Description

Table 3-1. Pin Description List

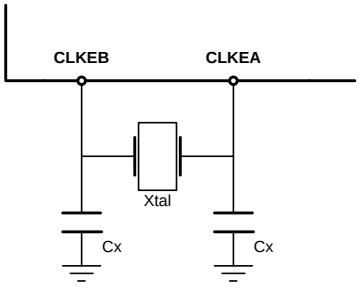
Pin Number	Pin Name	Type	Comments
1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13, 17, 18, 19, 20, 21, 22, 23, 24, 25, 28, 29, 86, 87, 89, 90, 91, 92, 107, 108, 109, 110, 111, 112, 113, 116, 117, 118, 119, 120	NC	--	No connect
3, 15, 26, 37, 43, 49, 55, 64, 65, 71, 73, 79,80, 83, 88, 93, 96, 105, 114	GND	Power	Digital Ground
4, 14, 27, 36, 42, 48, 54, 66, 72, 81, 85, 97,106, 115	VCC	Power	3.3v digital supply. Digital power supply must be decoupled by external capacitors
16, 74.	VDD	Power	LDO Power Output. A capacitor in the range 0.1µF-10µF must be connected to each pin
30	MISO	Output	SPI MISO. • SPI bridge Master In Slave Out • Internal configuration: 33kΩ typ. pull-up resistor
31	MOSI	Input	SPI MOSI • SPI bridge Master Out Slave In • Internal configuration: 33kΩ typ. pull-up resistor
32	SPICLK	Input	SPI CLK • SPI bridge Clock signal • Internal configuration: 33kΩ typ. pull-up resistor
33	/SS	Input	SPI /SS • SPI bridge Slave Select. Active low • Internal configuration: 33kΩ typ. pull-up resistor
34	RQ_MIC_STOP	Output	External Microcontroller Stop Request • Internal configuration: 33kΩ typ. pull-up resistor
35	/EXT_INT	Output	PHY Layer External Interrupt • Low level active • Internal configuration: 33kΩ typ. pull-up resistor

Pin Number	Pin Name	Type	Comments
38, 39, 40, 41, 44, 45, 46, 47, 50, 51, 52, 53	EMIT(1:12)	Output	PLC Transmission ports[1]
56	AFE_HIMP	Output	Analog Front-End High-Impedance • This digital output is used by the chip to select between low-impedance and high-impedance transmission branch (when working with a “two half-H-bridge branches” analog front end configuration). This way, the system adapts its transmission external circuitry to the net impedance, improving transmission behavior. The polarity of this pin can be inverted by hardware. Please refer to the Reference Design for further information.
57	AFE_TxRx	Output	Analog Front-End Transmission/Reception • This digital output is used to select between external Transmission and Reception branches. The suitable value depends on the external circuitry configuration. The polarity of this pin can be inverted by hardware. Please refer to the Reference Design for further information.
58	VSENSE	Input	Voltage Level Sensing • This input tracks the voltage level in the power supply to avoid power supply malfunction.
59	PSENSE	Input	Power Level Sensing • This input tracks the power level in the power supply to avoid power supply malfunction.
60	VNR[2]	Input	Zero Crossing Detection Signal • This input detects the zero-crossing of the mains voltage, needed to determine proper switching times.
61	TDI[3]	Input	Test Data In • Internal configuration: 33kΩ typ. pull-up resistor
62	TMS[3]	Input	Test Mode Select • Internal configuration: 33kΩ typ. pull-up resistor
63	TDO[3]	Output	Test Data out
67	TRST[3]	Input	Test Reset • Internal configuration: 33kΩ typ. pull-up resistor
68	TCK[3]	Input	Test Clock

Pin Number	Pin Name	Type	Comments
69	RSTA	Input	Asynchronous reset • RSTA is a digital input pin used to perform a hardware reset of the ASIC • RSTA is active high • Internal configuration: 33kΩ typ. pull-down resistor
70	D_INIT[4]	Input	Initialization Signal • D_INIT is active high • Internal configuration: 33kΩ typ. pull-down resistor
75	LDO_PD	Input	LDO Power-down • This digital input is used to put the internal linear regulator into power down mode ◦ '0': Power down mode disabled ◦ '1': Power down mode enabled
76	VSS0	Power	LDO ground
77, 78	VDE0	Power	LDO 3.3v power supply
82	CLKEA[5]	Input	External clock reference • CLKEA must be connected to one terminal of a crystal (when a crystal is being used) or tied to ground if a compatible oscillator is being used
84	CLKEB[5]	I/O	External clock reference • CLKEB must be connected to one terminal of a crystal (when a crystal is being used) or to one terminal of a compatible oscillator (when a compatible oscillator is being used)
94	AGC1	Output	Automatic Gain Control 1 • This digital output is managed by AGC hardware logic to drive external circuitry if input signal attenuation is needed • Internal configuration: 33kΩ typ. pull-up resistor
95	AGC0	Output	Automatic Gain Control 0 • This digital output is managed by AGC hardware logic to drive external circuitry if input signal attenuation is needed
98, 100	AVS1, AVS2	Power	Analog ground
99, 101	AVD1, AVD2	Power	3.3v analog power
102	VRH	Input	Analog input high voltage reference

Pin Number	Pin Name	Type	Comments
103	VIN	Input	Direct-analog input voltage
104	VRL	Input	Analog input low voltage reference

Notes:
1. Different configurations allowed depending on external topology and net behavior
2. Depending on whether an isolated or a non-isolated power supply is being used, isolation of this pin should be taken into account in the circuitry design. Please refer to the Reference Design for further information.
3. This pin is part of the JTAG Boundary Scan interface and is only used for boundary scan purposes
4. During power-on, D_INIT should be released before asynchronous reset signal RSTA, in order to ensure proper system start up. Not minimum time is required between both releases, $\Delta t>0$
5. The crystal should be located as close as possible to CLKEA and CLKEB pins. Recommended value for Cx is 18pF. This value may depend on the specific crystal characteristics



4. PRIME overview

The PRIME (PoweRline Intelligent Metering Evolution) initiative was originally conceived as an answer to the need for a future-proof, cost-effective Automatic Meter Management (AMM) solution. During its evolution in the last two years, it has evolved into a solution for an entire Smart Grid environment which will contribute definitively to energy efficiency improvement and ultimately to addressing the pressing issue of climate change.

The overall performance of the system fully complies with requirements for a new, stable metering infrastructure that is set to become a fundamental part of the Smart Grids. The revolutionary openness of the PRIME solution and its focus on interoperability as a way to decrease costs in a competitive framework, has been arising an unprecedented level of interest within the industry and markets. For this very reason a decision was taken by several of the most committed parties to set up the PRIME Alliance.

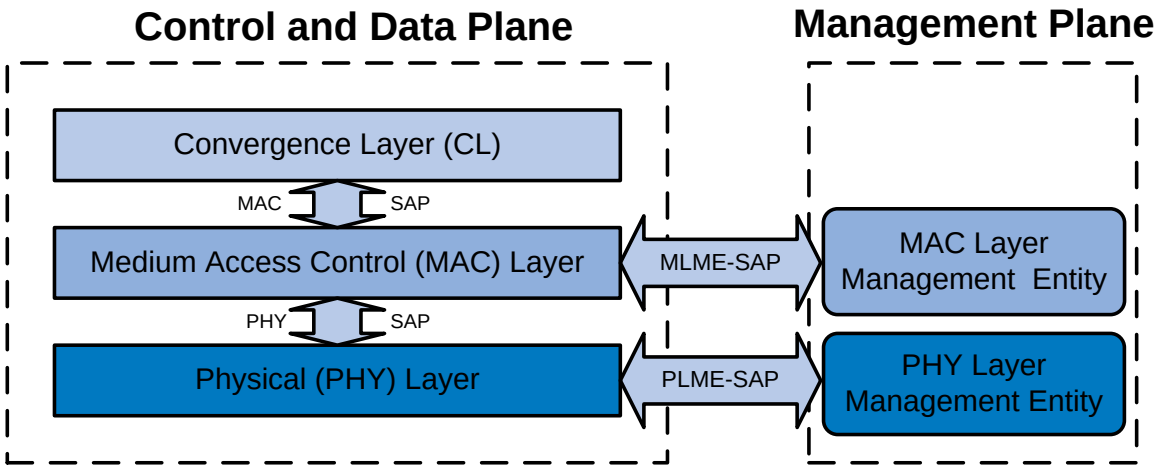
PRIME Alliance remains unique in that it shuns proprietary technologies and is the result of an open, cost-oriented effort among many different partners seeking to develop a future market for common benefit. Royalties and patents are definitely not part of the core PRIME specification. Ownership of the PRIME specification is uniquely public.

4.1 Key Features

PRIME defines lower layers of a PLC narrowband data transmission system over the electric grid. All the system has been created to be low cost and high performance.

Figure 4-1 below depicts the proposed communication layers and the scope of the specification. The proposed reference model is based on IEEE Std. 802.16 protocol layering.

Figure 4-1. PRIME layers



The service-specific **Convergence Layer** (CL) classifies traffic associating it with its proper MAC connection. This layer performs the mapping of any kind of traffic to be properly included in MAC SDUs (Service Data units). It may also include payload header suppression functions. Multiple Convergence sub-layers s are defined in order to accommodate different kinds of traffic into MAC SDUs.

The **MAC layer** provides core MAC functionalities of system access, bandwidth allocation, connection management and topology resolution. It has been defined for a connection oriented Master-Slave environment, and optimized for low voltage power line environments.

The **PHY layer** transmits and receives MAC PDUs (Protocol Data Units) between Neighbor Nodes. It is based on OFDM multiplexing in CENELEC A band and reaches up to 130 kbps raw data rate.

PRIME specifications take advantages of state of the art technologies and adapt them to the needed requirements, simplifying processes, overheads and others, to ensure performance, interoperability between devices and different implementations of elements in the system.

4.2 PRIME physical layer overview

4.2.1 Main features

PRIME PHY layer is designed to transmit and receive over power lines which were originally devised for distribution of power at 50-60Hz AC. The use of this medium for communications at higher frequencies presents some challenging technical problems:

- Distribution networks are usually made of a random variety of conductor types, and terminating into loads of different impedances. Such a network has an amplitude and phase response that varies widely with frequency. Furthermore, the channel characteristics shall also vary with time as the loads on the network change.
- Interference also affects power lines. Electric appliances with different kind of motors, switching power supplies and halogen lamps produce impulse noise that reduces the reliability of communication signals. Due to attenuation, the noise is also location dependent.

PRIME PHY layer uses a combination of approaches that ultimately allow for robust high speed, low cost communications over power lines. A simple yet powerful scheme which is based on adaptively modulated Orthogonal Frequency Division Multiplexing (OFDM), along with forward error correction and data interleaving.

A block diagram representation of a PHY transmitter is shown below in Figure 4-2:

Figure 4-2. PHY transmitter

On the transmitter side, the PHY layer receives its inputs from the Media Access Control layer. If decided by higher layers, the PHY frame after the CRC block is convolutionally encoded and interleaved; however, it will always be scrambled). The output is differentially modulated using a DBPSK, DQPSK or D8PSK scheme. The next step is OFDM, which comprises the IFFT (Inverse Fast Fourier Transform) block and the cyclic prefix generator.

4.2.2 Orthogonal Frequency Division Multiplexing (OFDM)

One of the main novelties of PRIME is that it uses an OFDM approach instead of traditional single carrier solutions that have been used in the past for narrowband power line communications.

OFDM is well known in the literature and in industry. It is currently used in xDSL technologies, terrestrial wireless distribution of television signals (DVB-T, DVB-H and more), and has also been adapted for IEEE's high rate wireless LAN Standards (802.11a and 802.11g). In less than twenty years, in fact, OFDM has developed into a popular scheme for virtually all new telecoms standards: WiMAX, DAB, DRM, 3G cellular telephony, UWB, MoCA, Broadband over Power line...

OFDM is a digital multi-carrier modulation scheme, which uses a large number of closely-spaced orthogonal subcarriers to carry data. To obtain high spectral efficiency, these subcarriers typically overlap in frequency. However the mathematical property of orthogonality allows recovering each of the subcarriers separately at the receiver, so in practice subcarriers do not interfere with each other as would be the case with traditional FDM.

Each subcarrier is modulated with a conventional modulation scheme at a low symbol rate, maintaining data rates similar to conventional single-carrier modulation schemes in the same bandwidth. In practice, OFDM signals are efficiently generated and detected using the well-known Fast Fourier Transform (FFT) algorithm.

The primary advantage of OFDM over single-carrier schemes is its ability to cope with severe channel conditions -for example, attenuation of high frequencies in long power lines, narrowband interference and frequency-selective fading due to multipath- without complex additional mechanisms (e.g. equalization filters). Channel equalization is simplified because OFDM may be viewed as using many slowly-modulated narrowband signals rather than one rapidly-modulated wideband signal.

Additionally, low symbol rate makes the use of a guard interval (or cyclic prefix) between symbols affordable, rendering it possible to handle time-spreading and eliminate intersymbol interference (ISI). For low frequencies like the ones PRIME uses, multipath is not a critical issue so cyclic prefixes will not waste a significant part of OFDM symbols.

4.3 PRIME MAC layer overview

PRIME system is composed of sub networks, each of them defined in the context of a transformer station. A sub network is a tree with two types of nodes, the Base Node and the Services Nodes.

4.3.1 Base Node

The Base Node is at the root of the tree and acts as master node that provides connectivity to the sub network. It manages the sub network resources and connections.

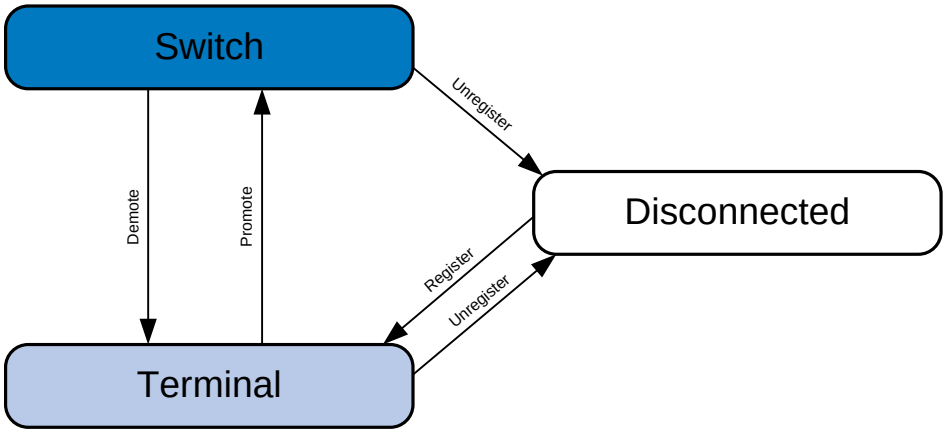
There is only one Base Node in a sub network. This Base Node is initially the sub network itself, and other nodes should follow a process of registering in order to enroll them to this sub network.

4.3.2 Service Node

Any other node of the sub network is a Service Node. Service Nodes are either leaves of the tree or branch points of the tree. These nodes start in a disconnected state and follow certain procedures to establish network connectivity. Each of these nodes is one point of the mesh of the sub network. These nodes have two responsibilities: connecting themselves to the sub network and switching the data of their neighbors in order to propagate connectivity.

Service Nodes change their behavior dynamically from “Terminal” functions to “Switch” functions and vice-versa. Changing of functional states occurs based on certain predefined events in the network.

Figure 4-3. Functional states of a Service Node



As shown in Figure 4-3, the three functional states of a Service Node are:

- **Disconnected**: Service Nodes start in a disconnected state. In this state a node is not capable of communicating or switching the traffic of another node. The primary function of a Service Node in this state is to search for an operational network in its proximity and to try to register itself to it.
- **Terminal**: In this state a Service Node is capable of communicating its traffic by establishing connections, but is not capable of switching the traffic of any other node.
- **Switch**: In this state a Service Node is capable of performing all Terminal functions. Additionally, it is capable of forwarding data to and from other devices in the sub network. It is a branch point in the tree.

The MAC layer provides all necessary features to manage PRIME networks and sub networks: addressing, synchronization (beacon management), dynamic management of the network structure (promotion and demotion of terminals), device registration management, connection setup and management, channel access arbitration, distribution of random sequences for deriving encryption keys, multicast group management...

4.4 Convergence Layer

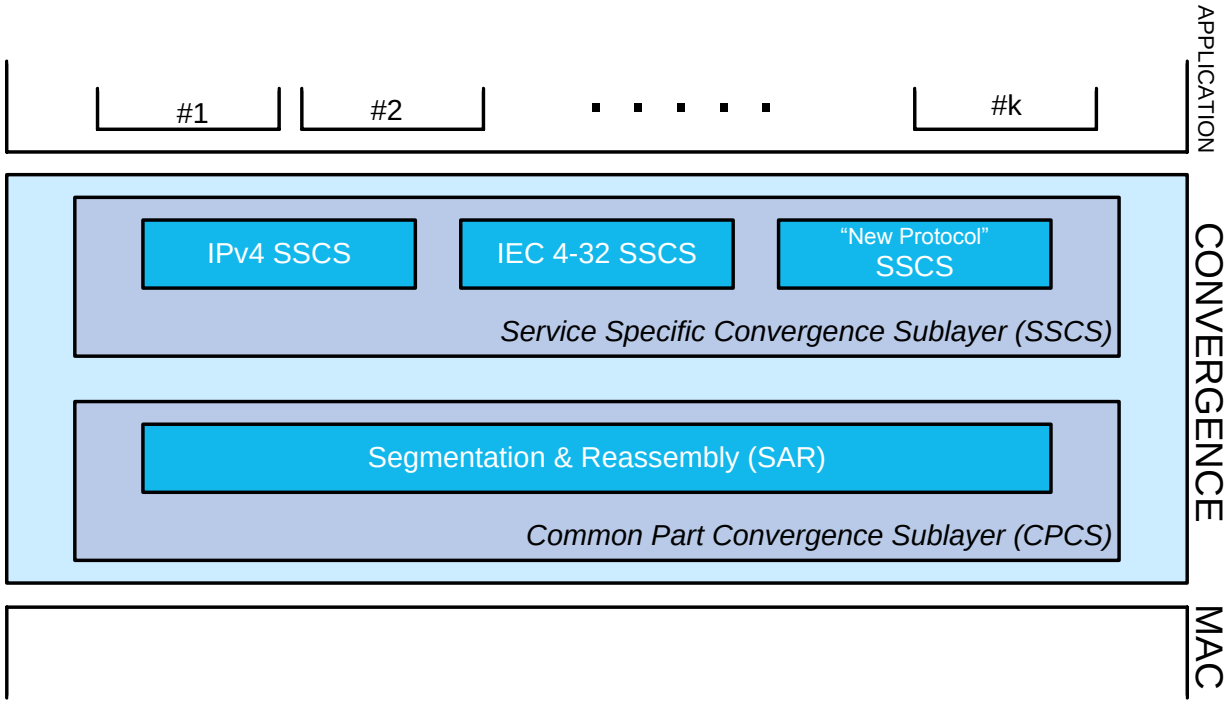
The Convergence Layer (CL) classifies traffic associating it with its proper MAC connection. This layer performs the mapping of any kind of traffic to be properly included in MAC SDUs, providing access to the core MAC functionalities of system access, bandwidth allocation, connection management and mesh topology resolution. It may also include payload header suppression functions.

The convergence layer is separated into two sub layers:

- The **Common Part Convergence Sub layer (CPCS)** provides a set of generic services.
- The **Service Specific Convergence Sub layer (SSCS)** contains services that are specific to one application layer.

There are many SSCS, typically one per application, but only one common part, as shown in Figure 4-4:

Figure 4-4. Convergence Layer

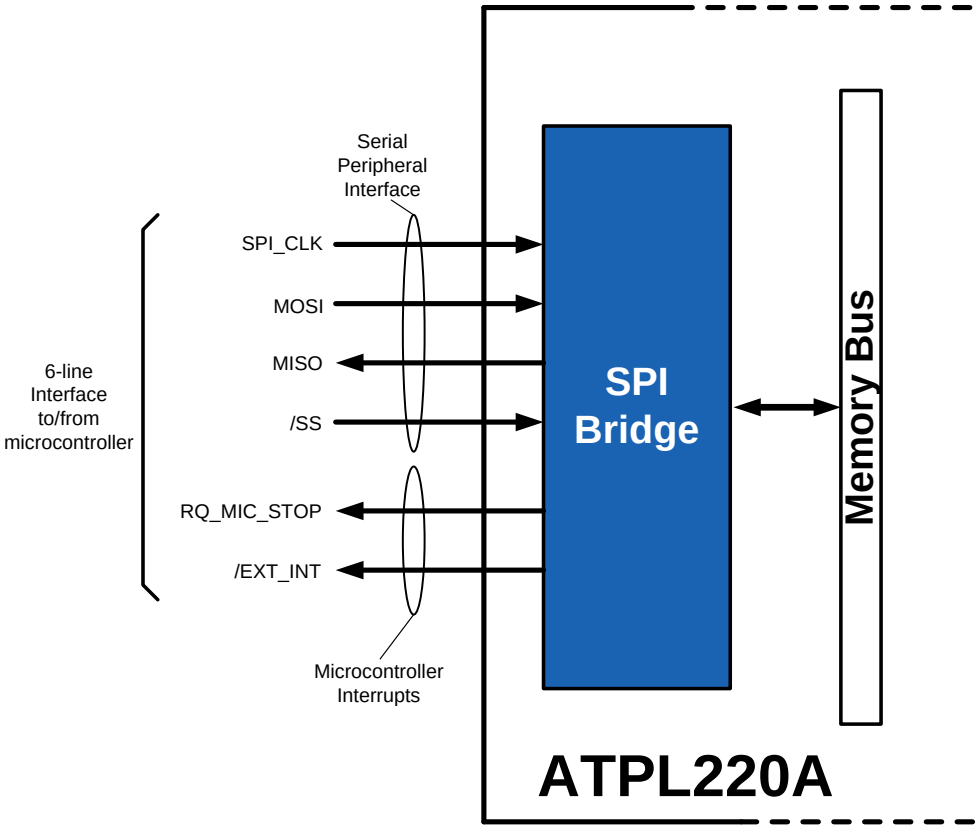


Several convergence sub layers are defined in order to accommodate different kinds of traffic into MAC SDUs, namely, IP convergence layer as a very useful and universal access to PRIME, and IEC 61334-4-32 as a link towards metering systems.

5. SPI Controller

ATPL220A has been conceived to be easily managed by an external microcontroller through a 6-line interface. This interface is comprised of a 4-line standard Serial Peripheral Interface (SPI) and 2 additional lines used as interrupts from the ATPL220A to the external microcontroller. A diagram is shown below

Figure 5-1. SPI Bridge Diagram

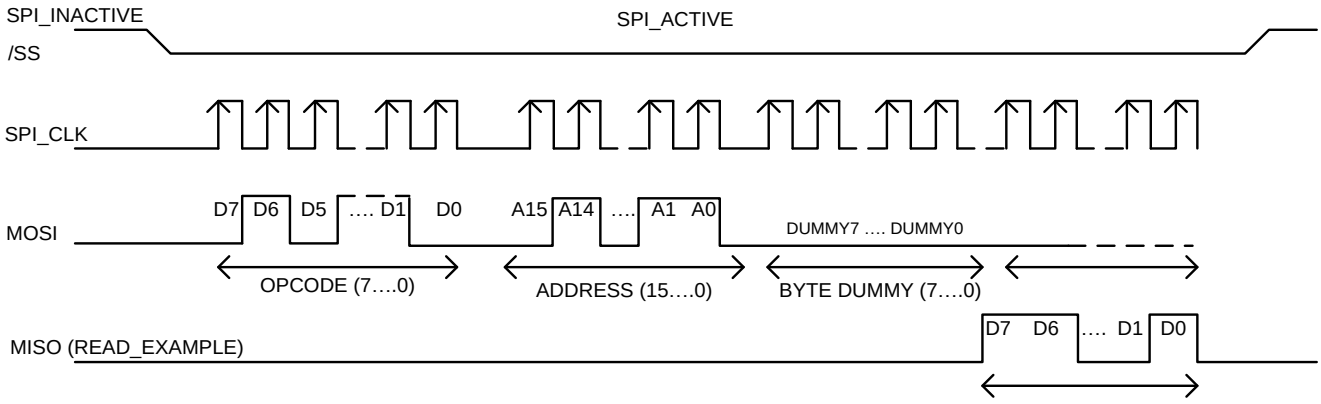


By means of this interface, the external microcontroller can access the ATPL220A internal SRAM and can carry out “write”, “read” and “mask” operations. As the ATPL220A peripheral registers are mapped in ATPL220A on-chip SRAM, the microcontroller can fully manage and control the ATPL220A (Phy layer, MAC co-processing, DMA channels, etc.) by accessing the peripheral registers (see related Peripheral Registers).

5.2 Serial Peripheral Interface

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

Figure 5-2. SPI Communication Example in ATPL220



The ATPL220A SPI allows an external device (working as a master), to communicate with the ATPL220A (working as a slave). Below is a brief description of the SPI signals:

- **/SS, Slave Select (pin no.33):** This input enables/disables the slave SPI. The ATPL220A is configured to work always as a slave. When disabled (/SS pin is tied high), the other SPI signals (SPI_CLK, MOSI and MISO) are not taken into account.
  - /SS = '0' → SPI enabled.
  - /SS = '1' → SPI disabled.

- **SPI_CLK, Serial Peripheral Interface Clock (pin no.32):** In reception (master→slave), data is read from MOSI line in the rising edge of the SPI clock. In transmission (slave→master), data is released to MISO in the falling edge of the SPI clock.

  It is recommended not to work with clock frequencies above 4MHz.

  This input only will be taken into account when /SS='0'.

- **MOSI, Master Out Slave In (pin no.31):** MOSI is the slave's data input line. Data is read from MOSI line in the rising edge of SPI_CLK.

  This input only will be taken into account when /SS='0'.

- **MISO, Master In Slave Out (pin no.30):** MISO is the slave's data output line. Data is released to MISO in the falling edge of SPI_CLK.

Furthermore, ATPL220A SPI bridge uses two additional lines to send interrupts to the host CPU:

- **RQ_MIC_STOP (pin no.34):** When receiving and transmitting messages, it is occasionally required to perform transferences between ATPL220A and its SRAM. Thus, it is necessary to stop SPI communication between the external microcontroller and the ATPL220A, giving the control to the DMA. ATPL220A chip sets RQ_MIC_STOP value to one, in order to indicate the external host an interrupt command. Once received, the external host will send an ACK command by setting /SS line to "1". Meanwhile, ATPL220A chip will poll /SS line at regular intervals until the master turns /SS line to 1. (Polling intervals are indicated by WAITING_TIME Register).

  SPI commands will be ignored by the slave until DMA releases the control by setting RQ_MIC_STOP to 0.

- **/EXT_INT (pin no.35):** This signal is an interrupt from ATPL220A Phy layer to the microcontroller. It indicates an interrupt from the physical DMA channel (see DMA section).

  In reception, every time a PLC message is received, the physical DMA channel generates two interrupts. One of them when the physical header is correctly received (two first symbols), and the other one when the message is completely received.

  In transmission, an interrupt will be generated every time a complete message has been sent.

  This signal is low level active

5.3 SPI Operation

When establishing a SPI communication (/SS line is set to '0' by the master), the first byte sent through MOSI line corresponds to the operation code. Three different operation types are defined over ATPL220A SPI. The operation codes are shown in table Table 5-1.

Table 5-1. SPI Operation Codes

Operation	Mask type	OpCode
Read	---	0x63
Write	---	0x2A
Mask	AND	0x4C
	OR	0x71
	XOR	0x6D

Following the operation code, the second and third bytes correspond to the SRAM address (16-bit address). Depending on the operation code, the master will "read data from"/"write data to"/"mask data in" that address.

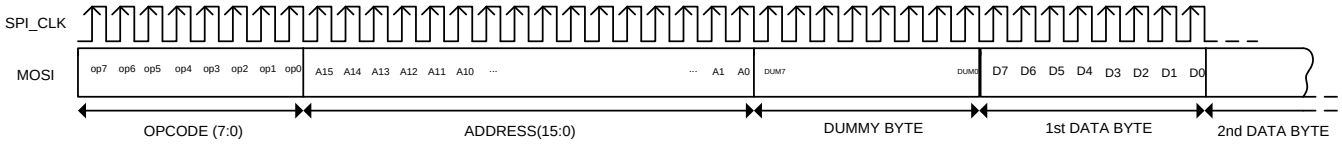
After the address, a dummy byte is sent.

Following the dummy byte, n data bytes (where n ≥ 1) are sent/received:

- If the operation code corresponds to a write operation in memory, the first data byte will be written in the specified address. If more data bytes are sent, they will be written in subsequent memory positions.
- If the operation code corresponds to a read operation from memory, the ATPL220A will output the data byte in MISO line. If the master continues sending SPI_CLK cycles, subsequent memory positions will be written in MISO line by the slave.
- If the operation code corresponds to a mask operation (AND, OR, XOR), the master will send the byte mask that have to be applied to the byte located at the specified address memory. If the master continues sending bytes, they will be applied as masks to the bytes stored in subsequent memory positions.

Bytes will be always sent with the most significant bit first.

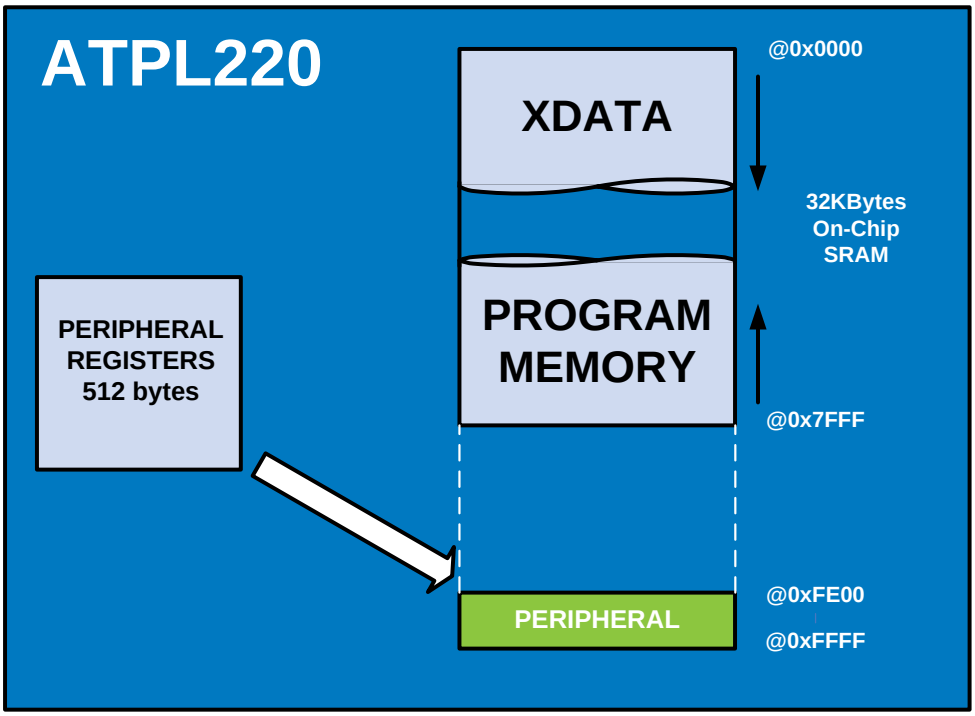
Figure 5-3. SPI Frame Example



6. Peripheral Registers

A 512 bytes space is reserved on-chip to allocate the system peripheral registers. These registers are mapped in XDATA (External Data Memory space) in addresses from FE00 to FFFF.

Figure 6-1. Peripheral Registers mapping in SRAM



A detailed description of each peripheral register can be found in its corresponding section.

7. Direct Access Memory (DMA)

ATPL220A SoC includes 2 DMA (Direct Memory Access) channels which provide an enhanced way for memory transference between the modem and the on-chip SRAM. These DMA channels are used by the physical layer and are not visible by the external microcontroller or another interface. The external microcontroller can configure DMA memory addresses (destination address in reception and source address in transmission), nevertheless the DMA channels low-level management is intended to be totally transparent to the final user.

7.1 DMA Management

DMA channels are intended to be used through a user interface.

By using a software interface, the user can perform DMA write/read operations and DMA configuration, so low-level management becomes transparent. Please see “PRIME User Help”for further information about software management.

7.2 DMA Channel Priority

Simultaneous DMA channels activation is possible, so it is needed to establish a priority for each DMA channel. It is possible for both channels to request memory access at the same time (low probability), so the channel with the highest priority will get the requested access. These are the priorities assigned:

Table 7-1. DMA channels priority

DMA Channel	Priority
PHY_RX	1
PHY_TX	0

Channel priority increases with “priority number”.

DMA channel used in reception (PHY_RX) is the most critical, so it has the highest priority,

7.3 DMA Transfer Capabilities

Access times for DMA channels are established by real-time memory transfer requirements. Every physical DMA access for these channels is 16-byte long. Time between consecutive accesses is set up by symbol data of the physical layer when needed.

7.4 DMA Interrupts

In order to inform the microcontroller about the completion of a DMA transference, a physical interrupt (/EXT_INT) is generated by hardware when the transference or a part of it is completed. This interrupt is activated in both emission and reception.

Table 7-2. DMA interrupts

Interrupt type	Internal Bit	External Signal
Physical	INT_PHY PHY_SFR(0)	/EXT_INT

7.5 DMA Flags

There are several flags activated simultaneously with DMA interruptions, that allow to know the type of DMA channel used in the transference, and if this transference is partial or complete. These flags are located at the DMA_SFR register, mapped at address 0xFE2B of the data memory.

See 7.7.2 in Registers section

7.6 Physical DMA channels

The main differences between PHY_RX (Reception physical DMA channel) and PHY_TX (Transmission physical DMA channel) channels are the direction of the transference, the interrupts generated, and the flags activated. Note that these DMA channels operate against internal registers mapped in data memory, so one of the buffers is always internal.

7.6.1 PHY_RX DMA channel

This is a dedicated DMA channel for physical data reception. The source is a 16-byte width buffer at the end of the reception branch (see PHY layer section), and the destination buffer is the data memory.

Size of the destination buffer is variable and corresponds to PPDU size (DMA destination size = PPDU length). Time between accesses depends on symbol duration, modulation schemes and physical layer processing capability.

There are two interrupts generated at reception, one of them when the physical header is correctly received (two first symbols), and the other one when the message is completely received. Then it is easy to see that DMA request size in this case correspond to the physical header size (11 bytes), which causes an interruption when the current transference size is equal to PHY header size and also activates an internal flag. For the other interruption another internal flag is activated to indicate the completion of reception.

The priority for this channel is the maximum available, because of critical reception requirements: physical data must be moved as fast as possible after symbol processing.

7.6.2 PHY_TX DMA channel

This is a dedicated DMA channel for physical data transmission. The source buffer is data memory and the destination is a 16-byte width buffer at the beginning of the transmission branch.

Size of the source buffer is also variable and corresponds to PPDU size (DMA source size = PPDU length). Time between accesses NPUM also depends on physical requirements.

For this channel there is only one interrupt available, at the end of the transmission, so it is easy to see that DMA request size in this case is equal to DMA source size. Note that this is the only DMA channel in which the end of memory transference is caused by the completion of the source buffer size, instead of the rest of the channels, in which the end of DMA is provoked by the destination buffer size. At the end of transmission, a physical interruption is generated and an internal flag is set.

The priority for this channel is lower than PHY_RX channel.

7.7 DMA Configuration Registers

7.7.1 PHY_SFR Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
PHY_SFR	BCH_ERR	CD	UMD	--	--	TXRX	--	INT_PHY

Name: PHY_SFR

Address: 0xFE2A

Access: Read/write

Reset: 0x87

- **--:** Reserved bit
- **BCH_ERR:** Busy Channel Error Flag.

  This bit is set to ‘0’ by hardware to indicate the presence of an OFDM signal at the transmission instant. Otherwise, this field value is ‘1’.

  This bit is used for returning a result of “Busy Channel” in the PHY_DATA.confirm primitive (see PRIME specification).
- **CD:** Carrier Detect bit.

  This bit is set to ‘1’ by hardware when an OFDM signal is detected, and it is active during the whole reception.

  This bit is used in channel access (CSMA-CA algorithm) for performing channel-sensing.
- **UMD:** Unsupported Modulation Scheme flag.

  This flag is set to ‘1’ by hardware every time a header with correct CRC is received, but the PROTOCOL field in this header indicates a modulation scheme not supported by the system.
- **TXRX:** Transmission order.

  When data to transmit is ready at ADDR_PHY_INI_TX in data memory, the Time value is set at TX_TIME register and then the emission level is specified at ATTENUATION register, then TXRX bit has to be set to '0' in order to init transmission.

  If this bit is read, only returns '0' when physical transmission has started. Otherwise, it returns '1'.

  The transmission will begin when TIMER_BEACON_REF is equal to TX_TIME.
- **INT_PHY:** Physical Layer interruption

  This bit is internally connected to the external microcontroller interrupt /EXT_INT.

  It is low-level active. It is set to '0' by physical layer and is cleared by writing '1' in the bit PHY_SFR(0).

7.7.2 DMA_SFR Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
DMA_SFR	--	--	--	--	DR_TX	DS_TX	DR_RX	DS_RX

Name: DMA_SFR

Address: 0xFE2B

Access: Read/write

Reset: 0x04

- **DR_TX:** Data Request flag for PHY_TX DMA channel

  This bit is always '0' because the PHY_TX buffer is only interrupted at the end of the transmission. (In reception there are two interruptions, the first one when the header is received and the other one when the complete message is receive. In transmission there is no interruption when the header is sent)

- **DS_TX:** Data Size flag for PHY_TX DMA channel

  This flag is activated when the complete size of the source buffer is transferred.

  That means that a complete message has been correctly transmitted.

  The source buffer is data memory at ADDR_PHY_INI_TX.

  The destination buffer is PHY_TX buffer.

  The transference size is the complete PPDU(PHY Protocol Data Unit) length.

- **DR_RX:** Data Request flag for PHY_RX DMA channel

  This flag is activated when the requested size of the destination buffer is already transferred.

  That means that an incoming message physical header has been correctly received.

  The requested size is fixed to 11 bytes, in accordance with the physical layer header.

- **DS_RX:** Data Size flag for PHY_RX DMA channel

  This flag is activated when the complete size of the destination buffer is transferred.

  That means that a complete message has been correctly received.

  The source buffer is PHY_RX and destination buffer is data memory at ADDR_PHY_INI_RX.

  The transference size is the complete PPDU (PHY protocol Data Unit) length.

7.7.3 PHY_TX Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
PHY_TX	PHY_TX(127:120)								@FE00
	…							…	
	PHY_TX(7: 0)								@FE0F

Name: PHY_TX

Address: 0xFE00 – 0xFE0F

Access: Read only

Reset: 0x00, …, 0x00;

- **PHY_TX:** Physical layer input buffer for transmission. The buffer size is 16 bytes in order to fit in with standard AES128 data size.

  Specific transfer from SRAM to this buffer is executed by DMA when necessary in transmission. DMA TX channel is dedicated for this type of transference.

DMA source address	=>	ADDR_PHY_INI_TX
DMA destination address	=>	PHY_TX(0)
DMA source size	=>	variable
DMA destination size	=>	16

7.7.4 PHY_RX Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
PHY_RX	PHY_RX(127:120)								@FE10
	…							…	
	PHY_RX(7: 0)								@FE1F

Name: PHY_RX

Address: 0xFE10 – 0xFE10

Access: Read only

Reset: 0x00, …, 0x00

- **PHY_RX:** Physical layer output buffer for reception. The buffer size is 16 bytes in order to fit in with standard AES128 data size.

  Specific transfer from SRAM to this buffer is executed by DMA when necessary in reception. DMA RX channel is dedicated for this type of transference.

DMA source address	=>	PHY_RX(0)
DMA destination address	=>	ADDR_PHY_INI_RX
DMA source size	=>	16
DMA destination size	=>	variable

7.7.5 ADDR_PHY_INI_RX Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ADDR_PHY_INI_RX	ADDR_PHY_INI_RX(15:8)								@0xFE20
	ADDR_PHY_INI_RX(7:0)								@0xFE21

Name: ADDR_PHY_INI_RX

Address: 0xFE20 – 0xFE21

Access: Read/write

Reset: 0x02, 0x10

- **ADDR_PHY_INI_RX:** Data memory address for reception

  This is the destination address to which DMA RX channel initiates data transfer from the physical layer

7.7.6 ADDR_PHY_INI_TX Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ADDR_PHY_INI_TX	ADDR_PHY_INI_TX(15:8)								@0xFE22
	ADDR_PHY_INI_TX(7:0)								@0xFE23

Name: ADDR_PHY_INI_TX

Address: 0xFE22 – 0xFE23

Access: Read/write

Reset: 0x00, 0x10

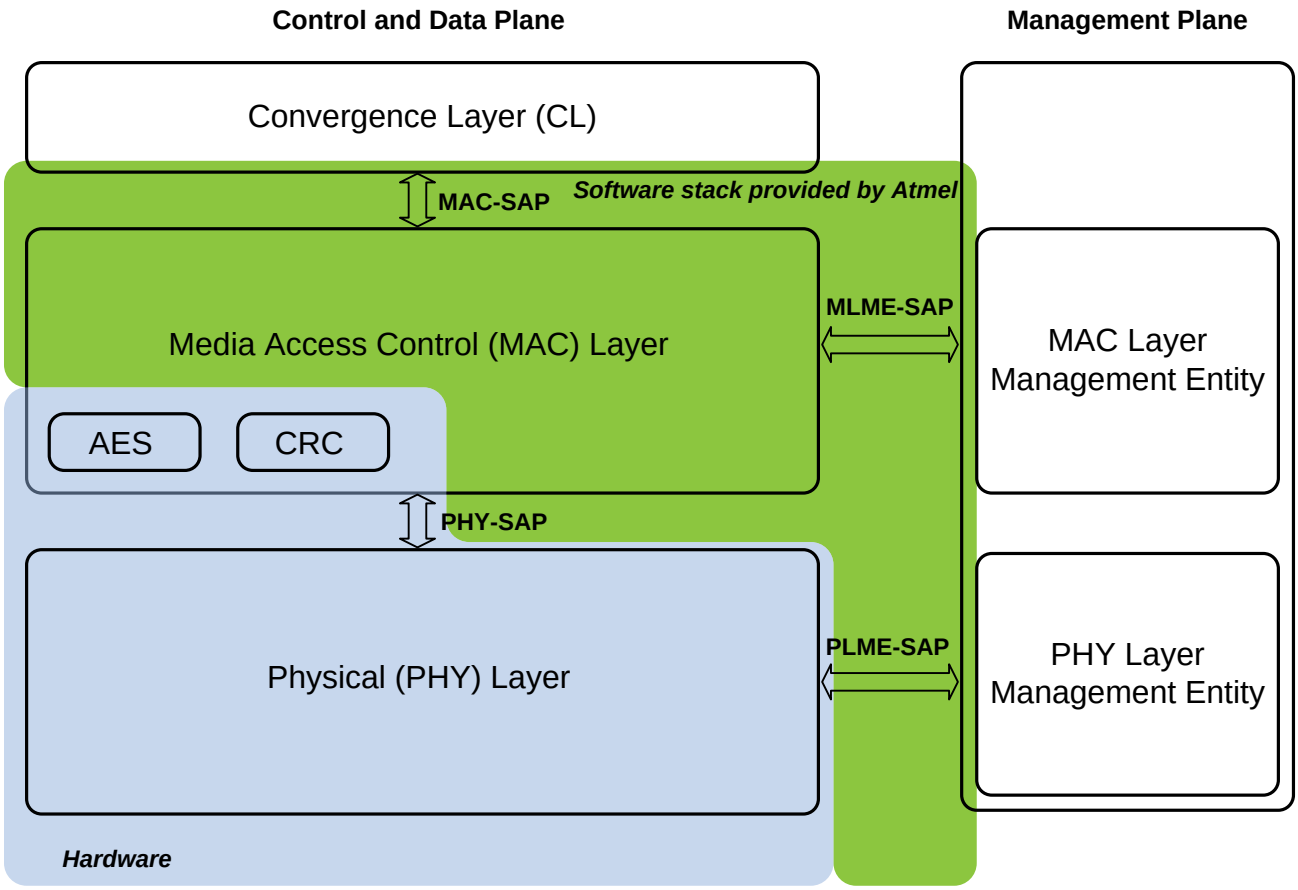
- **ADDR_PHY_INI_TX:** Data memory address for transmission

  This is the source address from which DMA TX channel initiates data transfer to the physical layer

8. ATPL220A MAC Coprocessor

The ATPL220A hardware MAC layer consists of a hardware implementation of some functionalities of the MAC Layer Entity specified in PRIME specification. These features are CRC calculation and AES128 block. So it is possible to consider this hardware as a MAC coprocessor to improve the microcontroller performance.

Figure 8-1. ATPL220A Software Stack Diagram



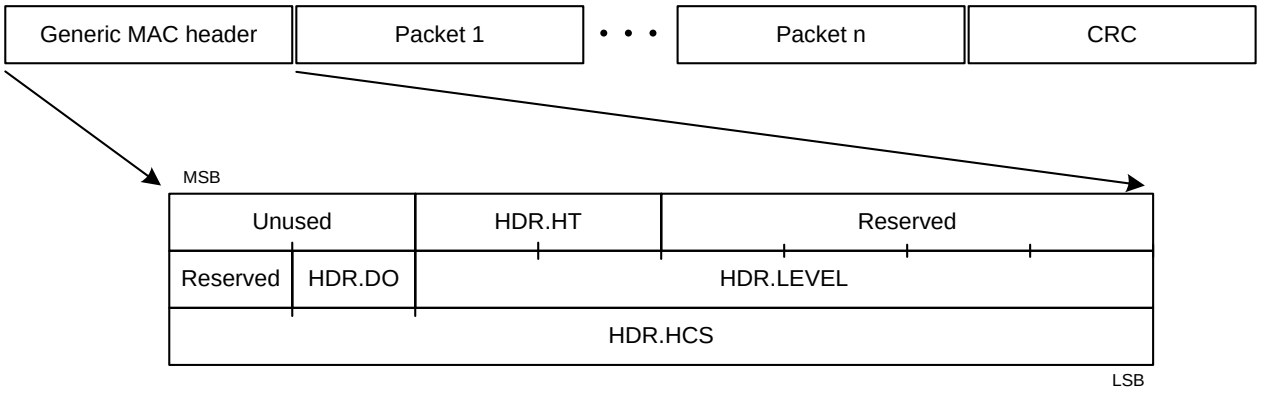
Atmel PRIME stack implements by software the rest of the MAC layer requirements and capabilities. Furthermore, the software package allows the communication with the Management Plane by means of the two Access points described by PRIME (PHY Layer Management Entity SAP and MAC Layer Management Entity SAP) and the interface to communicate MAC layer with the upper layer (Convergence Layer).

Please check the “Atmel PRIME Stack User Manual” for software package detailed description and functionality.

8.2 Cyclic Redundancy Check (CRC)

There are three types of MAC PDUs (generic, promotion and beacon) for different purposes, and each one has its own specific CRC. In ATPL220A there is a hardware implementation of every CRC type calculated by the MAC layer. This CRC hardware-calculation is enabled by default. Note that the CRC included at the physical layer is also a hardware implementation available in ATPL220A and it is also enabled by default.

Figure 8-2. Generic MAC PDU format and generic MAC header detail



In transmission all CRC bytes are real-time calculated and the last bytes of the MAC PDU are overwritten with these values, (provided that the field HT in the first byte of the MAC header in transmission data is equal to the corresponding MAC PDU type).

In reception the CRC bytes are also real-time calculated and these bytes are checked with the last bytes of the MAC PDU. If the CRC is not correct, then an error flag is activated, the complete frame is discarded, and the corresponding error counter is increased. These counters allow the MAC layer to take decisions according to error ratio.

For the Generic MAC PDU, there is an 8-bit CRC in the Generic MAC header, which corresponds to PRIME HDR.HCS. In reception if this CRC doesn't check successfully, the current frame is discarded and no interruption is generated.

This works in the same way as CRC for the PHY layer (CRC Ctrl, located in the PHY header, see PRIME specification for further information).

There is another CRC for the Generic MAC PDU which is the last field of the GPDU. It is 32 bits long and it is used to detect transmission errors. The CRC shall cover the concatenation of the SNA with the GPDU except for the CRC field itself. In reception, if the CRC is not successful then an internal flag is set and the error counter is increased.

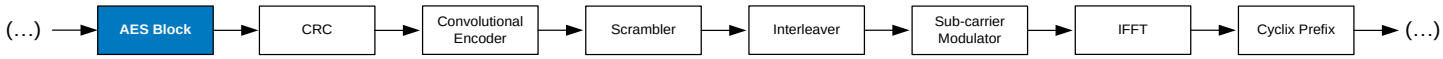
For the Promotion Needed PDU there is an 8-bit CRC, calculated with the first 13 bytes of the header. In reception, if this CRC is not correct, then an internal flag is set and the corresponding error counter is increased.

For the Beacon PDU there is a 32-bit CRC calculated with the same algorithm as the one defined for the CRC of the Generic MAC PDU. This CRC shall be calculated over the complete BPDU except for the CRC field itself. In reception, if this CRC is not successful, then an internal flag is set and the same error counter as for GPDU is increased. The hardware used for this CRC is the same as the one used for GPDU.

8.3 Advanced Encryption Standard

One of the security functionalities in PRIME is the 128-bit AES encryption of data and its associated CRC. ATPL220A includes a hardware implementation of this block, and it is used by the physical layer in real-time transmission/reception. It is possible to use this block externally as a peripheral unit, by accessing the specific registers designed to control it. Therefore there are some configurable parameters and input/output buffers to the block.

Figure 8-3. PHY Layer transmitter block diagram



There are two basic operation ways in ATPL220A when using PRIME Security Profile 1. The first one is real-time encryption and the second one is independent encryption from the PHY layer.

Real-Time Encryption: the AES128 core is integrated in the physical chain, and data is encrypted and decrypted in real-time when needed. In transmission, data is transferred to the emission buffer by means of the DMA TX channel. Then the 128 bits located in the buffer are encrypted before starting transmission (Note that Beacon PDU, Promotion PDU and Generic MAC header, as well as several control packets, are not encrypted). Data is extracted when required from this buffer until it is empty, and then a new DMA transfer is requested to fill the 16 bytes and a new encryption is executed. The key used for encryption must be set at the corresponding register, and it can vary from a packet to another.

In reception, data is obtained from the PHY layer and it is passed to the AES128 block. When the reception buffer is full with incoming data, the 128 bits are decrypted and transferred to external memory through DMA RX channel. Then the reception buffer is available again to fill with processed data.

The header is always real-time analyzed in order to know if encryption process must be applied.

Independent Encryption: the AES128 core is used as a peripheral unit, accessible with several registers mapped in external memory. In this mode, when in transmission, data must be encrypted previously to the use of the PHY_DATA.request primitive (see PRIME specification), in an independent way. In reception, data passed by the PHY layer is already encrypted and must be decrypted in a subsequent process.

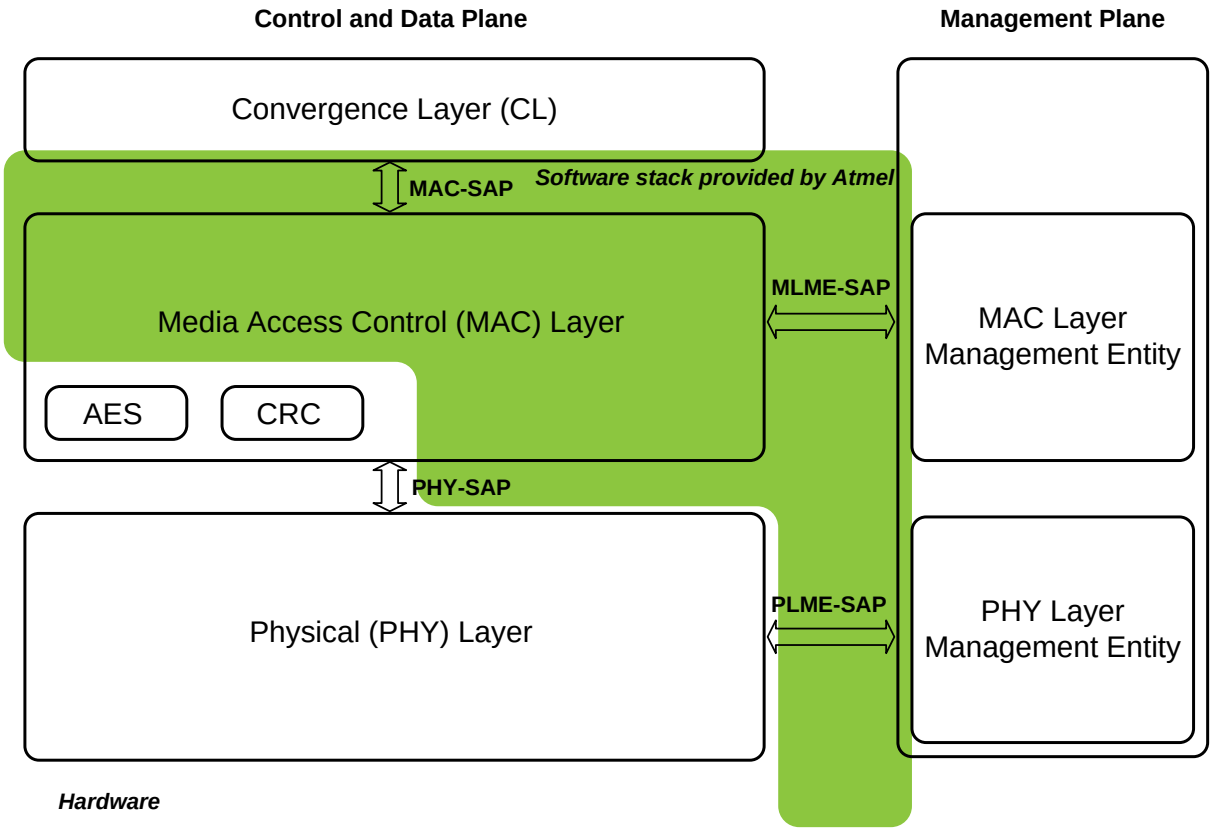
When working with AES block as a peripheral unit, automatic CRC calculation by hardware is disabled.

8.4 Atmel PRIME Software Stack

Looking for the best compromise between efficiency and versatility, Atmel has developed a PRIME software stack that implements and fulfills the capabilities of the MAC layer not carried out by ATPL220A hardware.

Atmel PRIME stack allows the final user to control the system by means of four sets of primitives, making the low level functions and the PHY-MAC interface transparent to the user.

Figure 8-4. Atmel PRIME Software Stack diagram

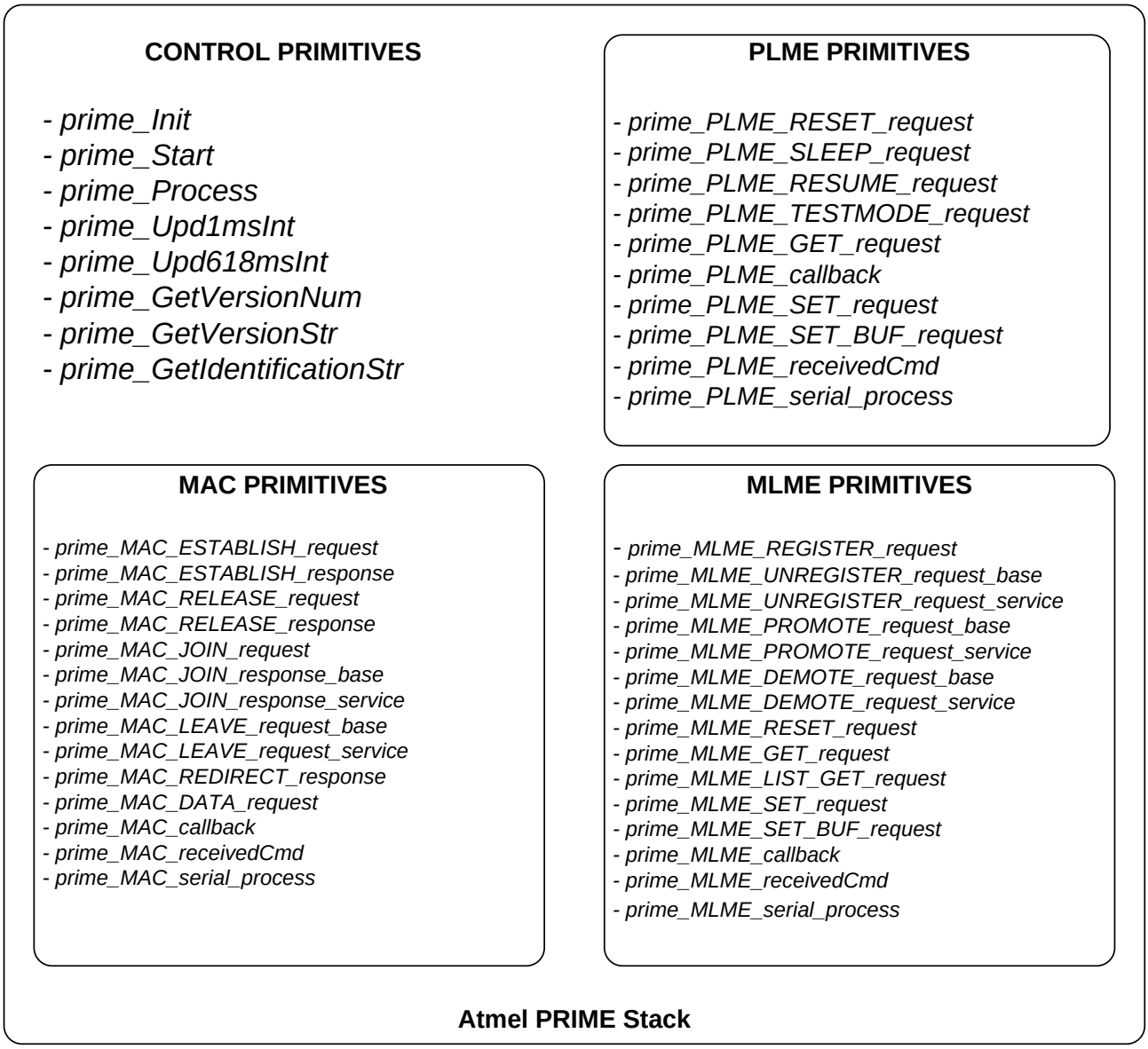


By using Atmel PRIME stack, ATPL220A PHY and MAC layers can be controlled by means of the three access points shown in the figure: MAC-SAP (MAC Service Access Point), MLME-SAP (MAC Layer Management Entity Service Access Point) and PLME-SAP (PHY Layer Management Entity Service Access point). Furthermore, there are general functions to manage the software package.

An example of high level functions that manage the software stack is shown in Figure 8-5.

Please check the “Atmel PRIME Stack User Manual” for software package detailed and updated description and functionality.

Figure 8-5. Atmel PRIME version 1.3.04.04 stack functions



8.5 MAC Coprocessor Registers

8.5.1 SNA Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
SNA	SNA(47:40)								@FE62
	…							…	
	SNA(7: 0)								@FE67

Name: SNA

Address: 0xFE62 – 0xFE67

Access: Read/write

Reset: 0x00, …, 0x00

- **SNA:** Sub Network Address

  These registers store the 48-bit Sub Network Address. When the system Sub Network Address is available, the microcontroller must write it down so the Phy layer will be able to correctly calculate the CRC's, which depend on this parameter

8.5.2 VITERBI_BER_HARD Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
VITERBI_BER_HARD	VITERBI_BER_HARD(7:0)							

Name: VITERBI_BER_HARD

Address: 0xFE36

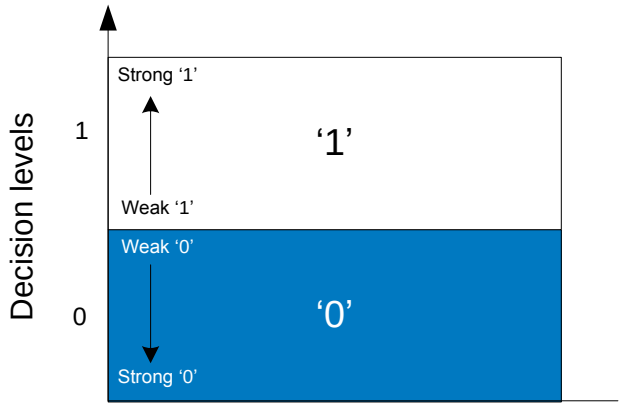
Access: Read only

Reset: 0x00

- **VITERBI_BER_HARD:** This register stores the number of errors accumulated in a message reception using Viterbi hard* decision. The value is cleared by hardware each time a new message is received.

**Hard Decision: in "hard" detection there are only two decision levels. If the received value is different than the corrected one, the error value taken is "1". Otherwise, the error value taken is "0".*

Figure 8-6. Viterbi Hard detection decision levels



From the value in VITERBI_BER_HARD register it is possible to calculate de Bit Error Rate according to the following formula:

8.5.3 VITERBI_BER_SOFT Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
VITERBI_BER_SOFT	VITERBI_BER_SOFT(7:0)							

Name: VITERBI_BER_SOFT

Address: 0xFE37

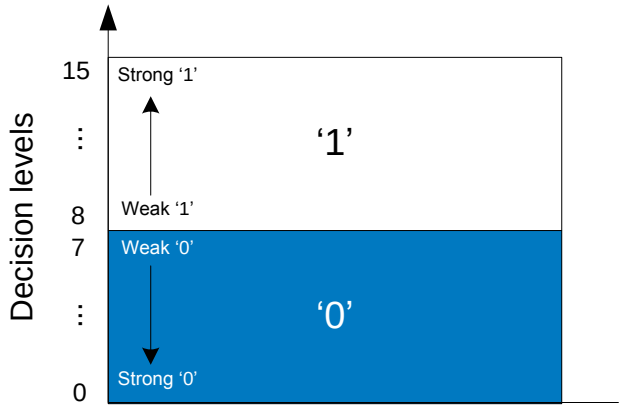
Access: Read only

Reset: 0x00

- **VITERBI_BER_SOFT:** This register stores a value proportional to the number of errors accumulated in a message reception using Viterbi soft* decision. The value is cleared by hardware each time a new message is received.

**Soft Decision: in "soft" decision there are fifteen decision levels. A strong '0' is represented by a value of "0", while a strong '1' is represented by a value of "15". The rest of values are intermediate, so "7" is used to represent a weak '0' and "8" represents a weak '1'. Soft decision calculates the error in one bit received as the distance in decision levels between the value received (a value in the range 0 to 15) and the corrected one (0 or 15).*

Figure 8-7. Viterbi Hard detection decision levels



8.5.4 ERR_CRC32_MAC Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC32_MAC	ERR_CRC32_MAC(15:8)								@0xFEBA
	ERR_CRC32_MAC(7:0)								@0xFEBB

Name: ERR_CRC32_MAC

Address: 0xFEBA – 0xFEBB

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC32_MAC:** 16-bit value that stores the number of received messages that have been discarded by an error in the MAC layer CRC32.
  Note: to clear this value, these registers must be reset by the microcontroller.

8.5.5 ERR_CRC8_MAC Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_MAC	ERR_CRC8_MAC(15:8)								@0xFEBC
	ERR_CRC8_MAC(7:0)								@0xFEBD

Name: ERR_CRC8_MAC

Address: 0xFEBC – 0xFEBD

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_MAC:** 16-bit value that stores the number of received messages that have been discarded by an error in the payload MAC layer CRC8.
  Note: to clear this value, these registers must be reset by the microcontroller.

8.5.6 ERR_CRC8_AES Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_AES	ERR_CRC8_AES(15:8)								@0xFEBE
	ERR_CRC8_AES(7:0)								@0xFEBF

Name: ERR_CRC8_AES

Address: 0xFEBE – 0xFEBF

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_AES:** 16-bit value that stores the number of received messages that have been discarded by an error in the payload AES CRC8.
  Note: to clear this value, these registers must be reset by the microcontroller.

8.5.7 ERR_CRC8_MAC_HD Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_MAC_HD	ERR_CRC8_MAC_HD(15:8)								@0xFEC0
	ERR_CRC8_MAC_HD(7:0)								@0xFEC1

Name: ERR_CRC8_MAC_HD

Address: 0xFEC0 – 0xFEC1

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_MAC_HD:** 16-bit value that stores the number of received messages that have been discarded by an error in the header MAC layer.

  Note: to clear this value, these registers must be reset by the microcontroller.

8.5.8 ERR_CRC8_PHY Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_PHY	ERR_CRC8_PHY(15:8)								@0xFEC2
	ERR_CRC8_PHY(7:0)								@0xFEC3

Name: ERR_CRC8_AES

Address: 0xFEC2 – 0xFEC3

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_PHY:** 16-bit value that stores the number of received messages that have been discarded by an error in the PHY layer CRC8.
  Note: to clear this value, these registers must be reset by the microcontroller.

8.5.9 FALSE_DET_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
FALSE_DET _CONFIG	--		ERR_CRC8 _MAC	INVALID _PROTOCOL	ERROR _LEN	ERROR_PAD _LEN	UNKNOWN _PDU	UNKNOWN _SP

Name: FALSE_DET_CONFIG

Address: 0xFEC4

Access: Read/write

Reset: 0x10

- **--:** Reserved bits
- **ERR_CRC8_MAC:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the MAC layer CRC8 present in its header is wrong.
- **INVALID_PROTOCOL:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the PROTOCOL field indicates a modulation not supported by the system.
- **ERROR_LEN:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the LEN field indicates a not valid message length.
- **ERROR_PAD_LEN:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the PAD_LEN field indicates a not valid message padding length.
- **UNKNOWN_PDU:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the HT field indicates a header type different from BEACON, PROMOTION or GENERIC.
- **UNKNOWN_SP:** If this bit is set to 1, FALSE_DET registers will increase its error counter if a received message has a correct PHY layer CRC8 but the SECURITY_PROTOCOL field is wrong.

8.5.10 FALSE_DET Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
FALSE_DET	FALSE_DET(15:8)								@0xFEC5
	FALSE_DET(7:0)								@0xFEC6

Name: FALSE_DET

Address: 0xFEC5 – 0xFEC6

Access: Read/write

Reset: 0x00, 0x00

- **FALSE_DET:** Erroneous non-discarded messages.

  16-bit value that stores the number of received messages that have not been discarded since its PHY layer CRC8 is correct, but in which there are other incorrect fields. The fields that shall be taken into account to increase the counter in case they were wrong can be selected by FALSE_DET_CONFIG register.

  Note: to clear this value, these registers must be reset by the microcontroller

8.5.11 MAX_LEN_DBPSK Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DBPSK	--		MAX_LEN_DBPSK(5:0)					

Name: MAX_LEN_DBPSK

Address: 0xFEC8

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DBPSK:** This register sets the maximum length, measured in OFDM symbols, that the system allows to receive when working with DBPSK modulation and no Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DBPSK value, the message will be discarded.

8.5.12 MAX_LEN_DBPSK_VTB Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DBPSK_VTB	--		MAX_LEN_DBPSK_VTB(5:0)					

Name: MAX_LEN_DBPSK_VTB

Address: 0xFEC9

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DBPSK_VTB:** This register sets the maximum length, measured in OFDM symbols, that the system allows to receive when working with DBPSK modulation and Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DBPSK_VTB value, the message will be discarded.

8.5.13 MAX_LEN_DQPSK Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DQPSK	--		MAX_LEN_DQPSK(5:0)					

Name: MAX_LEN_DQPSK

Address: 0xFECA

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DBPSK:** This register sets the maximum length, measured in OFDM symbols, that the system allows to receive when working with DQPSK modulation and no Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DQPSK value, the message will be discarded.

8.5.14 MAX_LEN_DQPSK_VTB Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DQPSK_VTB	--		MAX_LEN_DQPSK_VTB(5:0)					

Name: MAX_LEN_DQPSK_VTB

Address: 0xFECB

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DQPSK_VTB:** This register sets the maximum length, measured in OFDM symbols that the system allows to receive when working with DQPSK modulation and Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DQPSK_VTB value, the message will be discarded.

8.5.15 MAX_LEN_D8PSK Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_D8PSK	--		MAX_LEN_D8PSK(5:0)					

Name: MAX_LEN_D8PSK

Address: 0xFECC

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_D8PSK:** This register sets the maximum length, measured in OFDM symbols, that the system allows to receive when working with D8PSK modulation and no Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_D8PSK value, the message will be discarded.

8.5.16 MAX_LEN_D8PSK_VTB Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_D8PSK_VTB	--		MAX_LEN_D8PSK_VTB(5:0)					

Name: MAX_LEN_D8PSK_VTB

Address: 0xFECD

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_D8PSK_VTB:** This register sets the maximum length, measured in OFDM symbols that the system allows to receive when working with D8PSK modulation and Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_D8PSK_VTB value, the message will be discarded.

8.5.17 AES_PAD_LEN Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AES_PAD_LEN	--				AES_PAD_LEN(3:0)			

Name: AES_PAD_LEN

Address: 0xFE25

Access: Read/write

Reset: 0x00

- **--:** Reserved bits
- **AES_PAD_LEN:** AES protocol works over 16-bytes-lenght blocks. When a block is not 16-bytes long, this register indicates the number of padding bytes to append.

  This register takes values between 0 and 15.

  In transmission, if encryption is being used, microcontroller must write the AES padding length in this register.

  In no-encrypted transmission and in reception, the value in this register is not used.

8.5.18 AES_DATA_IN Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AES_DATA_IN	AES_DATA_IN(127:120)								@FFA0
	…							…	
	AES_DATA_IN(7: 0)								@FFAF

Name: AES_DATA_IN

Address: 0xFFA0 – 0xFFAF

Access: Read/write

Reset: 0x00, …, 0x00

- **AES_DATA_IN:** Input buffer for AES128 block.
  This buffer can be written to be encrypted/decrypted by the key in KEY_PERIPH (see 8.5.20) register.
  The resulting data could be read at AES_DATA_OUT (see 8.5.19) registers.

8.5.19 AES_DATA_OUT Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AES_DATA_OUT	AES_DATA_OUT(127:120)								@FFB0
	…							…	
	AES_DATA_OUT(7: 0)								@FFBF

Name: AES_DATA_OUT

Address: 0xFFB0 – 0xFFBF

Access: Read only

Reset: 0x00, …, 0x00

- **AES_DATA_OUT:** Output buffer for AES128 block.

  This buffer stores the result of the encryption/decryption processing of data in AES_DATA_IN (see 8.5.18) register with the key in KEY_PERIPH (see 8.5.20) register.

8.5.20 KEY_PERIPH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
KEY_PERIPH	KEY_PERIPH(127:120)								@FFC0
	…								
								…	
	KEY_PERIPH (7: 0)								@FFCF

Name: KEY_PERIPH

Address: 0xFFC0 – 0xFFCF

Access: Read/write

Reset:

KEY_PERIPH(127:120) :	0x00;	KEY_PERIPH(119:112) :	0x01;	KEY_PERIPH(111:104) :	0x02;
KEY_PERIPH(103:96) :	0x03;	KEY_PERIPH(95:88) :	0x04;	KEY_PERIPH(87:80) :	0x05;
KEY_PERIPH(79:72) :	0x06;	KEY_PERIPH(71:64) :	0x07;	KEY_PERIPH(63:56) :	0x08;
KEY_PERIPH(55:48) :	0x09;	KEY_PERIPH(47:40) :	0x0A;	KEY_PERIPH(39:32) :	0x0B;
KEY_PERIPH(31:24) :	0x0C;	KEY_PERIPH(23:16) :	0x0D;	KEY_PERIPH(15:8) :	0x0E;
KEY_PERIPH(7:0) :	0x0F;				

- **KEY_PERIPH:** Key for AES128 block when used as peripheral part.
  This key is used for encrypting/decrypting data in AES_DATA_IN registers.

8.5.21 KEY_PHY Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
KEY_PHY	KEY_PHY(127:120)								@FFD0
	…							…	
	KEY_PHY(7: 0)								@FFDF

Name: KEY_PHY

Address: 0xFFD0 – 0xFFDF

Access: Read/write

Reset:

KEY_PHY(127:120):	0x00;	KEY_PHY(119:112) :	0x01;	KEY_PHY(111:104) :	0x02;
KEY_PHY(103:96) :	0x03;	KEY_PHY(95:88) :	0x04;	KEY_PHY(87:80) :	0x05;
KEY_PHY(79:72) :	0x06;	KEY_PHY(71:64) :	0x07;	KEY_PHY(63:56) :	0x08;
KEY_PHY(55:48) :	0x09;	KEY_PHY(47:40) :	0x0A;	KEY_PHY(39:32) :	0x0B;
KEY_PHY(31:24) :	0x0C;	KEY_PHY(23:16) :	0x0D;	KEY_PHY(15:8) :	0x0E;
KEY_PHY(7:0) :	0x0F;				

- **KEY_PHY:** Key for AES128 block when used by the physical layer

  This key is used in real time encryption/decryption for Security Profile 1. When any of the DMA channels of the physical layer accesses to the memory, then this key and the input data are multiplexed to the AES128-core. Also output data is multiplexed in order to provide encrypted/decrypted data to the physical buffer.

8.5.22 AES_SFR Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AES_SFR	--					READY	START	CIPHER

Name: AES_SFR

Address: 0xFFE0

Access: Read/write

Reset: 0x00

- --: Reserved bits.
- **READY:** Flag to indicate encryption/decryption process completion.
  When the encryption/decryption has been completed, this flag is set to ‘1’.
  This flag is automatically cleared when an encryption/decryption process begins.
- **START:** When this bit is set to ‘1’, the encryption/decryption process is triggered.
  If encryption/decryption starts successfully, then this bit is automatically cleared to ‘0’.
- **CIPHER:** This field indicates if data must be encrypted or decrypted.
  - ‘0’ - Decryption mode
  - ‘1’ - Encryption mode

8.5.23 WAITING_TIME Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
WAITING_TIME	WT(7:0)							

Name: WAITING_TIME

Address: 0xFE93

Access: Read/write

Reset: 0xFF

- **WT:** This value indicates the number of clock cycles to wait before polling /SS line after a RQ_MIC_STOP has been sent to the external microcontroller. By default, the value in this register is FF, so the default waiting time is 255*1/fclk=12.75microseconds.

  Once RQ_MIC_STOP has been set high, the ATPL220A SPI controller will poll /SS line indefinitely until it goes high (/SS='1', SPI inactive).

  This value must be calculated to give the external microcontroller enough time to manage the RQ_MIC_STOP interrupt and to respond consistently driving /SS line high, thus avoiding collisions.

9. ATPL220A PRIME PHY Layer

9.1 ATPL220A PHY Layer

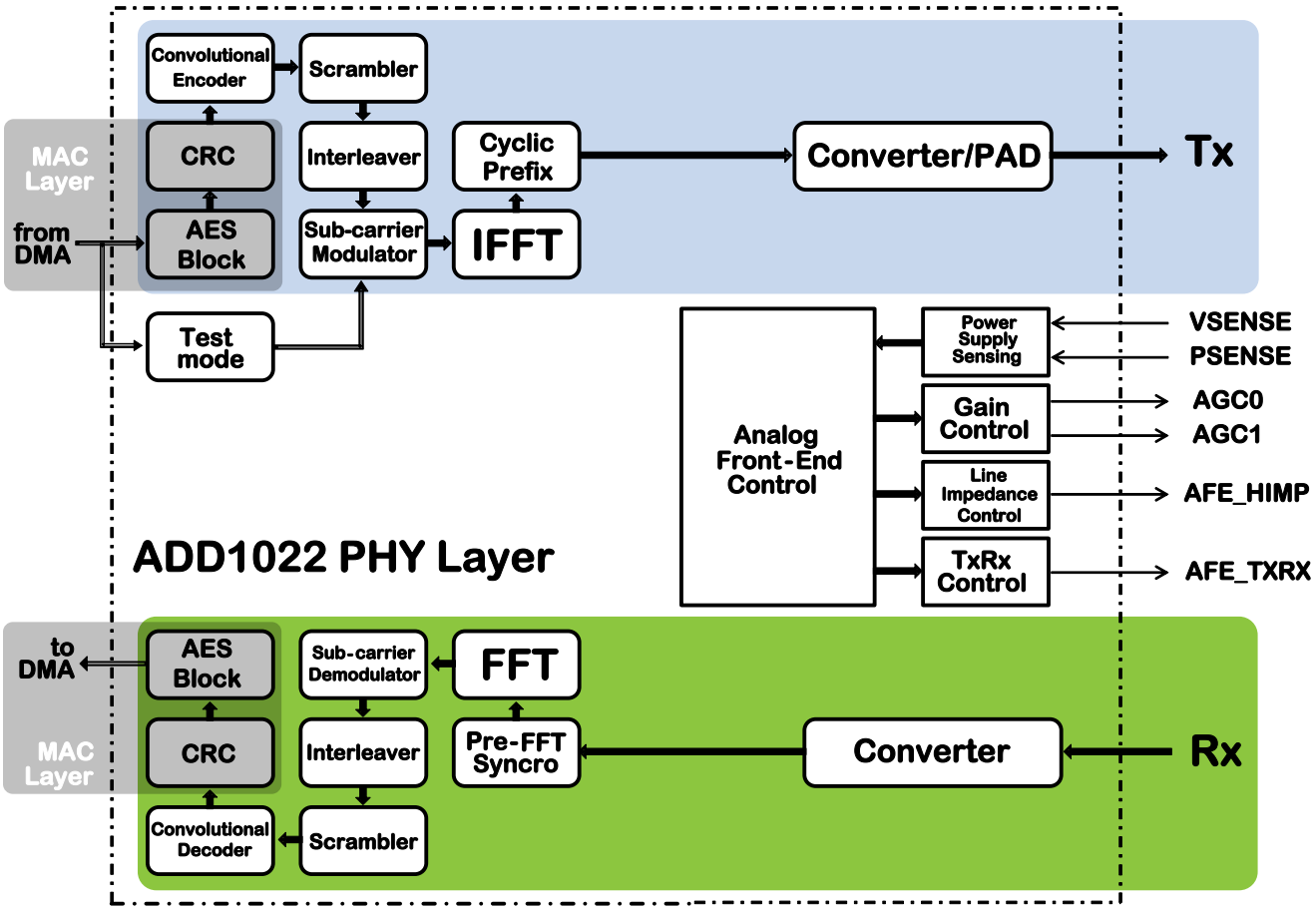
The physical layer of ATPL220A consists of a hardware implementation of the PRIME Physical Layer Entity, which is an Orthogonal Frequency Division Multiplexing (OFDM) system in the CENELEC A-band. This PHY layer transmits and receives MPDUs (MAC Protocol Data Unit) between neighbor nodes.

From the transmission point of view, the PHY layer receives its inputs from the MAC (Medium Access Control) layer, via DMA. At the end of transmission branch, data is output to the physical channel.

On the reception side, the PHY layer receives its inputs from the physical channel, and at the end of reception branch, the data flows to the MAC layer, via DMA.

A PHY layer block diagram is shown below:

Figure 9-1. ATPL220A PHY Layer Block Diagram



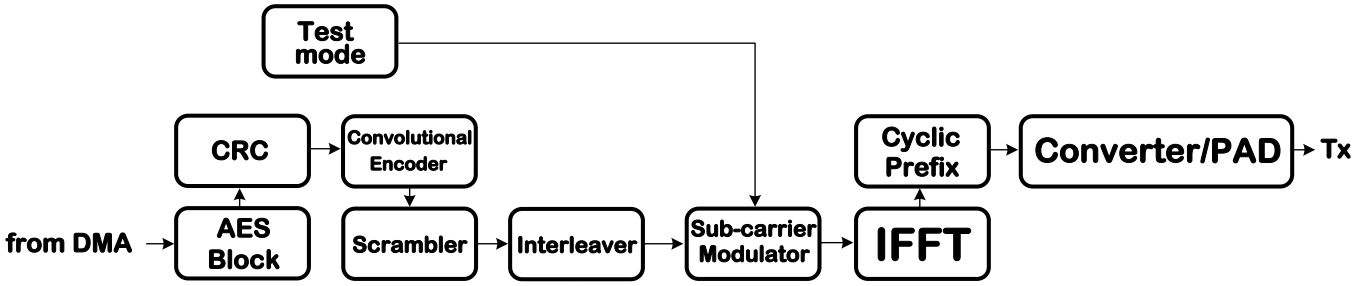
The diagram can be divided in four sub-blocks: Transmission branch, Emission branch, Analog Front End control and Carrier Detection.

9.1.2 Transmission and Reception branches

Phy layer takes data to be sent from dedicated DMA channel (PHY_TX). 128-bit AES encryption is done “on the fly”, and the Clyclic Redundancy Check (CRC) fields are hardware-generated in real time. These CRCs are properly appended to the transmission data. The rest of the chain is hardware-wired, and performs automatically all the tasks needed to send data according to PRIME specifications.

In Figure 9-2, the block diagram of the transmission brach Is shown.

Figure 9-2. Transmission branch



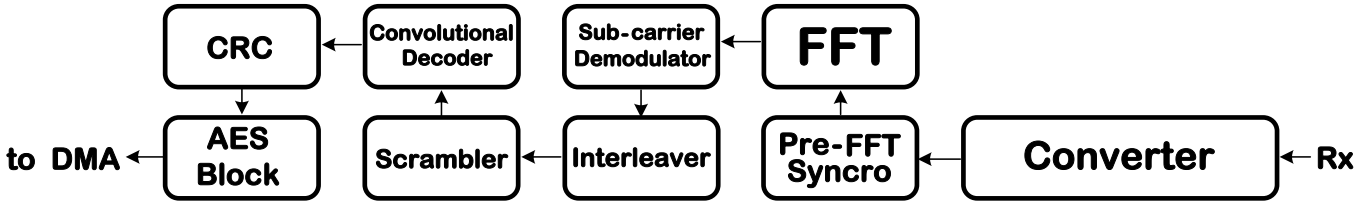
The output is differentially modulated using a BPSK/DQPSK/D8PSK scheme. After modulation, IFFT (Inverse Fourier Transform) block and cyclic prefix block allows to implement an OFDM scheme.

A Converter and a Power Amplifier Driver is the last block in the transmission branch. This block is responsible for adjusting the signal to reach the best transmission efficiency, thus reducing consumption and power dissipation.

Test mode: *When selected, test mode injects data directly to Sub-carrier modulation block. When in test mode, data can be injected continuously to the line using only a set of selected frequencies, in order to test channel behavior.*

The reception branch performs automatically all the tasks needed to process received data. Phy layer delivers data to MAC layer through the dedicated DMA channel (PHY_RX).

Figure 9-3. Reception branch



9.1.3 Carrier Detection

Looking for an easy detection of incoming messages, PRIME specification defines a chirp signal located at the beginning of the PRIME frames devised to ease synchronization in the receptor. By means of detection techniques, the receiver can know accurately when the chirp has been completely received and then the correct instant when the frame begins.

Before starting a transmission, it is also necessary to use carrier detection in order to check if another device is already emitting, thus avoiding collisions. If any device is emitting, the carrier detection triggers a microcontroller interruption and sets an internal flag, thus the transmission will be stopped.

The main drawback of this process is that chirp signal length (2.4 milliseconds) is not short enough to guarantee very low collision ratio.

To improve this drawback, the OFDM PLC Modem implements two different algorithms to detect the carrier as soon as possible, aiming to reduce collisions and improving the medium access behavior. By these early detection techniques, the system achieves low collision ratio, and the communication throughput increases significantly.

9.1.4 Analog Front End control

The Phy layer controls the Analog Front End by means of four sub-blocks:

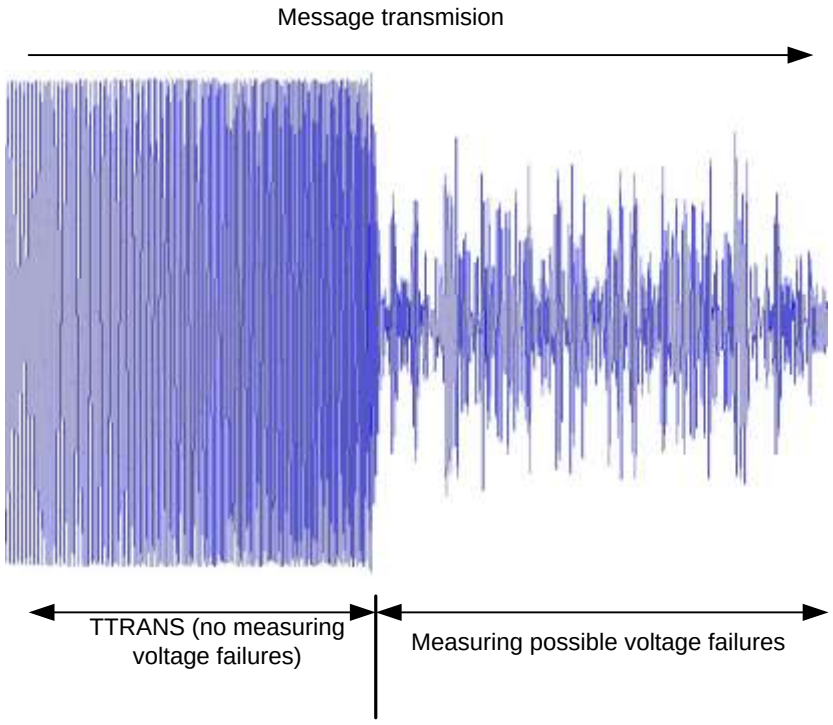
- Power Supply sensing
- Gain control
- Line Impedance control
- TxRx control

9.1.4.1 Power Supply Sensing: VSENSE and PSENSE

The power supply is continuously monitored to avoid power supply failures that could damage the supply device. This block senses the power channel using two different inputs:

- **VSENSE:** VSENSE detects whether voltage falls below 3.3v during a number of cycles while a message is being transmitted. This measurement is done after a transitory guard time (TTRANS in figure below). If a Voltage failure occurs, the transmission is shut down and sending messages again will be not possible if an internal flag (VFAILURE) is not previously cleared.

Figure 9-4. Transitory guard time in message transmission



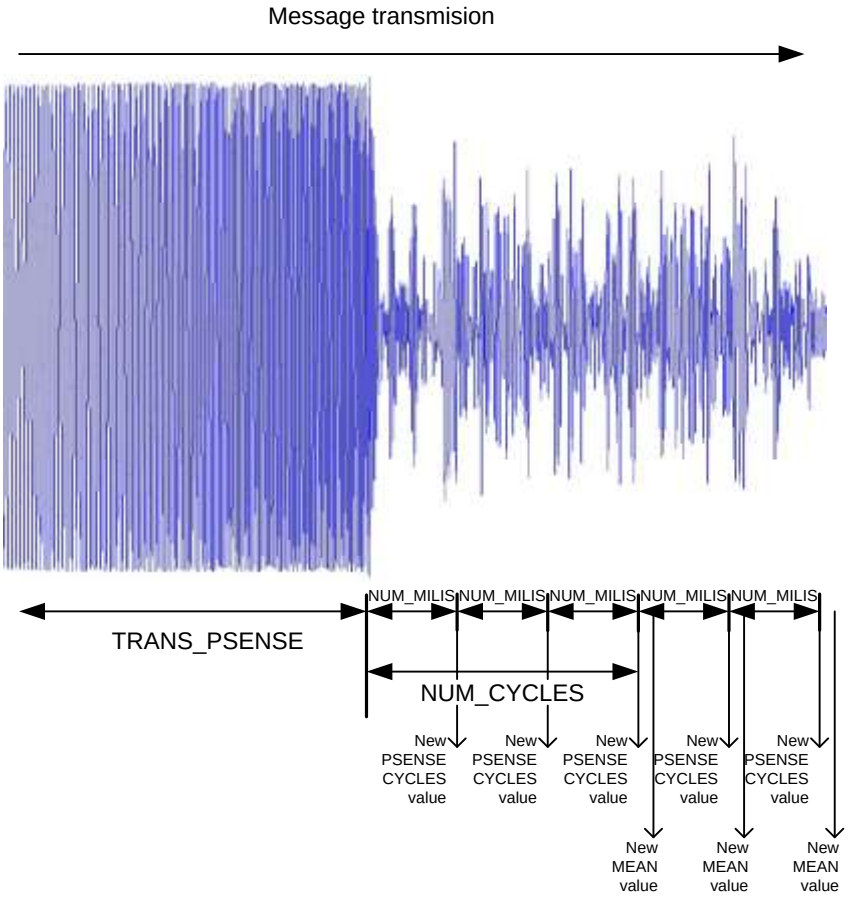
- **PSENSE:** PSENSE measures the power source current consumption, shutting down the transmission if the consumption exceeds a defined threshold (stored in MAXPOT phy layer registers, see 9.5.34).

  This measurement is done after a transitory guard time. As the current measurement varies over time, an averaging is done taking into account an average parameter (Alpha), a configurable number of cycles (NUMCYCLES, see 9.5.35) and a configurable length of each cycle (A_NUMMILIS, see 9.5.36).

If a power failure occurs, the transmission is shut down and sending messages again will be not possible if an internal flag (PFAILURE, see 9.5.22) is not previously cleared.

The system considers that a power failure has occurs when the value read from MEAN registers (see 9.5.30) is above the user-definable value stored in MAXPOT registers.

Figure 9-5. PSENSE parameters



Psense and Vsense configurations parameters are automatically set by the Phy layer.

See related peripheral registers for more information about Psense and Vsense.

9.1.4.2 Gain Control

This block implements two Automatic Gain Control outputs to adjust the received signal level to a suitable range. Both of them are set to ‘1’ when the received signal is above two system thresholds in order to activate external attenuators placed in the external analog front end.

The value of these outputs is set during the beginning of a received message and is hold until the end of the message.

AGC0 and AGC1 follow different algorithms, thus using both of them ensures a more accurate gain control.

See AGC_CONFIG register in for information about AGC configuration.

9.1.4.3 Line Impedance Control

This block modifies the configuration of the Analog Front End by means of AFE-HIMP output. When working with a suitable external configuration, the system can change the filter conditions in order to adjust its behavior to the line impedance values. See last ATPL220 reference design for further information about Line Impedance topologies.

9.1.4.4 TxRx Control

This block modifies the configuration of the Analog Front End by means of AFE-TXRX output. Thus is possible to change filter conditions between transmission/reception.

See reference design for further information about TxRx control.

9.2 PHY parameters

As described below, the PHY layer is specified by certain main parameters, which are fixed for each specific constellation/coding combination. These parameters have to be identical in a network in order to achieve compatibility.

Table 9-1. PRIME Phy main parameters

PRIME Phy parameter	Value
Base Band Clock (Hz)	250000
Subcarrier spacing (Hz)	488,28125
Number of data subcarriers	84 (header), 96 (payload)
Number of pilot subcarriers	13 (header), 1 (payload)
FFT interval (samples)	512
FFT interval (µs)	2048
Cyclic Prefix (samples)	48
Cyclic Prefix (µs)	192
Symbol interval (samples)	560
Symbol interval (µs)	2240
Preamble period (µs)	2048

Table 9-2 shows the PHY data rate during payload transmission, and maximum MSDU length for various modulation and coding combinations

Table 9-2. Phy parameters depending on the modulation

	DBPSK		DQPSK		D8PSK	
Convolutional Code (1/2)	**On**	**Off**	**On**	**Off**	**On**	**Off**
Information bits per subcarrier	0,5	1	1	2	1,5	3
Information bits per OFDM symbol	48	96	96	192	144	288
Raw data rate (kbps approx)	21,4	42,9	42,9	85,7	64,3	128,6
MAX MSDU length with 63 symbols (bits)	3016	6048	6040	12096	9064	18144

Table 9-3 shows the modulation and coding scheme and the size of the header portion of the PHY frame

Table 9-3. Header parameters

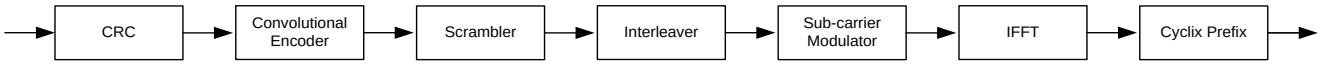
	DBPSK
Convolutional Code (1/2)	On
Information bits per subcarrier	0,5
Information bits per OFDM symbol	42

All the parameters of the physical layer such as the base band clock, subcarrier spacing, number of subcarriers...; are defined in PRIME Specification, and have to be identical in a network in order to achieve compatibility.

9.3 PHY Protocal Data Unit (PPDU) Format

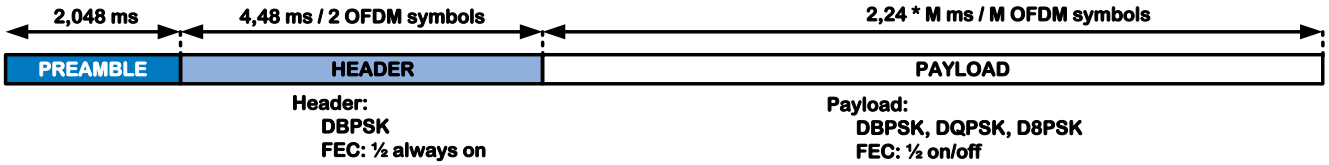
Figure 9-6 shows how OFDM symbols are transmitted in a PPDU (Physical layer Protocol Data Unit). The preamble is used at the beginning of every PPDU for synchronization purposes.

Figure 9-6. PHY layer transmitter block diagram



Phy layer adaptively modifies attenuation values applied to the whole signal. Also, additional attenuations are applied to the chirp section of the signal (preamble) and to the rest of the signal itself (header+payload), to smoothly adapt amplitude values and transitions.

Figure 9-7. PPDU OFDM symbols and duration



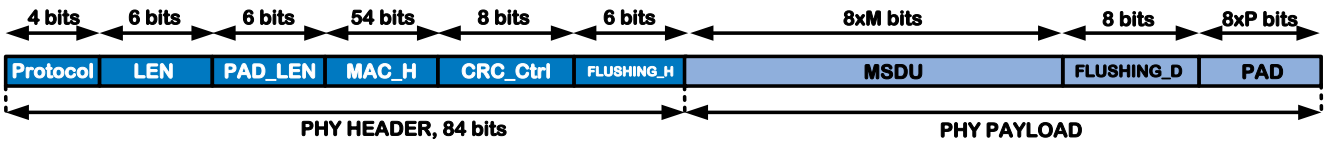
9.4 PHY Service Specification

There is an interface specified in PRIME for the PHY layer, with several primitives relative to both data and control planes.

PHY layer has a single 20-bit free-running clock measured in 10µs steps. Time measured by this clock is the one to be used in some PHY primitives to indicate a specific instant in time.

ATPL220A includes a hardware implementation of this clock, which consists of a 20-bit register. This register is read-only and it can be accessed as a 32-bit variable by the external microcontroller.

Figure 9-8. Header and payload structure



Prime specifies a complete set of primitives to manage the PHY Layer, and the PHY-SAP (PHY Service Access Point) from MAC layer. Atmel PRIME stack integrates all this functions, making them transparent to the final user and simplifying the management.

9.5 PHY Layer registers

9.5.1 PHY_SFR Register

This register is described in 7.7.1, DMA Configuration Registers section.

9.5.2 SYS_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
SYS_CONFIG	--			CONV_PD	PHY_PD	PHY_ERR_EN	PHY_ERR	PHY_RST

Name: SYS_CONFIG

Address: 0xFE2C

Access: Read/write

Reset: 0x04

- **--:** Reserved bits
- **CONV_PD:** Converter Power Down

  Microcontroller can activate internal converter power down mode by setting this bit. When internal converter is in power down mode, the system is unable to receive.

  This bit is high-level active.
- **PHY_PD:** PHY Power Down

  This bit shuts down Physical Layer clock. When in PHY power down mode, all the system blocks involved in communication remain inactive. Thus, the system will be unable to transmit or receive. The next sequence must be respected to ensure proper power down:

  Setting PHY power down mode

  1-Set Physical Layer reset (SYS_CONFIG(0)), PHY_RST='1'

  2-Set CONV_PD and PHY_PD fields

  Exiting PHY power down mode

  1-Clear CONV_PD and PHY_PD fields

  2-Clear Physical Layer reset (SYS_CONFIG(0)), PHY_RST='0'

  This bit is high-level active.
- **PHY_ERR_EN:**Physical Layer Watchdog enable

  This bit enables or disables Physical layer watchdog. Physical layer watchdog is enabled by default.

  This bit is high-level active.
- **PHY_EN:** Physical Layer Error Flag

  This flag indicates if a Physical layer error has occurred. Physical layer watchdog has a 200milliseconds sampling period. When Physical layer detects an error, it activates the Physical layer interrupt and this flag is set.

  To restore situation, microcontroller must reset Physical layer by means of PHY_RST bit (SYS_CONFIG(0)).
- **PHY_RST:** Physical Layer Reset

  This bit resets the Physical layer. To perform a Physical layer reset cycle, microcontroller must set this bit to '1' and then must clear it to '0'.

9.5.3 PHY_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
PHY_CONFIG	--		**CINR_MODE**	**PAD_LEN_AC**	**AES_EN**	**CD_MOD1_EN**	**CD_MOD2_DET**	**MAC_EN**

Name: PHY_CONFIG

Address: 0xFE68

Access: Read/write

Reset: 0x1F

- **--:** Reserved bits
- **CINR_MODE:** Carrier to Interference + Noise Ratio mode

  This bit enables/disables CINR mode when set to '1'.
  - '0': CINR mode disabled.
  - '1': CINR mode enabled.
- **PAD_LEN_AC:** This field allows the system to work with two different representations of the Phy header PAD_LEN field (PAD_LEN represented before coding or PAD_LEN represented after coding).
  - '0': PAD_LEN field in PHY header is represented before coding. This is the suitable value to fulfill PRIME specification.
  - '1': PAD_LEN field in PHY header is represented after coding.
- **AES_EN:** This field enables/disables "on the fly" AES encryption and decryption by hardware.
  - '0': "on the fly" AES encryption/decryption disabled.
  - '1': "on the fly" AES encryption/decryption enabled.
- **CD_MOD1_EN:** This field enables/disables Carrier Detection mode 1.
  - '0': Carrier Detection mode 1 disabled.
  - '1': Carrier Detection mode 1 enabled.
- **CD_MOD2_DET:** This field enables/disables Carrier Detection mode 2.
  - '0': Carrier Detection mode 2 disabled.
  - '1': Carrier Detection mode 2 enabled.
- **MAC_EN**: This field enables/disables CRC processing by hardware.
  - '0': CRC processing disabled.
  - '1': CRC processing enabled.

9.5.4 ATTENUATION Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ATTENUATION	ATTENUATION(7:0)							

Name: ATTENUATION

Address: 0xFE24

Access: Read/write

Reset: 0xFF

- **ATTENUATION:** Global attenuation for the transmitted signal (chirp+signal). The 16-bit signal level is multiplied by this 8-bit value and the result is truncated to 16 bits.
  Attenuation value = 0xFF → the transmitted signal amplitude is not attenuated.
  Attenuation value = 0x00 → the transmitted signal amplitude is nullified.

9.5.5 ATT_CHIRP Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ATT_CHIRP	ATT_CHIRP(7:0)							

Name: ATT_CHIRP

Address: 0xFE9B

Access: Read/write

Reset: 0xFF

- **ATT_CHIRP:** This register stores the attenuation value for the chirp. The 16-bit chirp data is multiplied with this 8-bit value and the 24-bit result is truncated to 16 bits.
  Attenuation value = 0xFF → the chirp amplitude is not attenuated
  Attenuation value = 0x00 → the chirp amplitude is nullified

9.5.6 ATT_SIGNAL Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ATT_SIGNAL	ATT_SIGNAL(7:0)							

Name: ATT_SIGNAL

Address: 0xFE9C

Access: Read/write

Reset: 0xFF

- **ATT_SIGNAL:** This register stores the attenuation value for the signal without the chirp section. The 16-bit chirp data is multiplied with this 8-bit value and the 24-bit result is truncated to 16 bits.
  Attenuation value = 0xFF → the signal amplitude is not attenuated
  Attenuation value = 0x00 → the signal amplitude is nullified

9.5.7 TX_TIME Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
TX_TIME	TX_TIME(19:12)								@0xFE26
	TX_TIME(11:4)								@0xFE27
	TX_TIME(3:0)				“0000”				@0xFE28
	“00000000”								@0xFE29

Name: TX_TIME

Address: 0xFE26 – 0xFE29

Access: Read/write

Reset: 0x00, …, 0x00;

- **TX_TIME:** This 20-bit value sets the time instant when the MPDU (MAC Protocol Data Unit) has to be transmitted. The time is expressed in 10µs steps.

  When writing a new value to TX_TIME register, a specific writing order must be taken, always from the most significant byte (TX_TIME(19:12) at address 0xFE26) to the least significant byte (TX_TIME(3:0) at address 0xFE28), and it is required to write the 3 bytes to avoid wrong time comparisons in transmission.

  The 20-bit TX_TIME value is managed by the microcontroller as a 4-byte variable. The TX_TIME value is aligned to the 20 most significant bits, being the 12 least significant bits padded with zeros.

  This register is used by the physical layer for being in accordance with PRIME specifications about transmission time (see PRIME spec.)

  Note: TXRX bit (PHY_SFR(2)) has to be cleared to ‘0’ in order to init transmission. Once this bit has been cleared, the transmission will start when TIMER_BEACON_REF value is equal to TX_TIME.

9.5.8 TIMER_FRAME Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
TIMER_FRAME	TIMER_FRAME(19:12)								@0xFE2D
	TIMER_FRAME(11:4)								@0xFE2E
	TIMER_FRAME(3:0)				“0000”				@0xFE2F
	“00000000”								@0xFE30

Name: TIMER_FRAME

Address: 0xFE2D – 0xFE30

Access: Read only

Reset: 0x00, …, 0x00;

- **TIMER FRAME:** Time of receipt of the preamble associated with the PSDU (PHY Service Data Unit). It is expressed in 10µs steps and is taken from the physical layer timer TIMER_BEACON_REF.

  It is set by hardware and is a read-only register.

  This register is used by the physical layer for being in accordance with PRIME specification about reception time (see PRIME specification).

  The 20-bit TIMER_FRAME value is managed by the microcontroller as a 4-byte variable. The TIMER_FRAME value is aligned to the 20 most significant bits, being the 12 least significant bits padded with zeros. This simplifies arithmetic calculations with time values.

9.5.9 TIMER_BEACON_REF Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
TIMER_BEACON_REF	TIMER_BEACON_REF(19:12)								@0xFE47
	TIMER_BEACON_REF (11:4)								@0xFE48
	TIMER_BEACON_REF (3:0)				“0000”				@0xFE49
	“00000000”								@0xFE4A

Name: TIMER_BEACON_REF

Address: 0xFE47 – 0xFE4A

Access: Read only

Reset: 0x00, …, 0x00;

- **TIMER_BEACON_REF:** Timer for the physical layer, which consists of a single 20-bit free-running clock measured in 10µs steps.

  It indefinitely increases a unit each 10 microseconds from 0 to 1048575, overflowing back to 0.

  It is set by hardware and is a read-only register.

  This register is used by the physical layer for being in accordance with PRIME specification. It is reserved 32-bit in data memory to be able to declare as 32-bit variable. The 20-bit register MSB is aligned to the 32-bit variable MSB, in order to simplify arithmetic calculations with time values.

9.5.10 RX_LEVEL Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
RX_LEVEL	RX_LEVEL(15:8)								@0xFE31
	RX_LEVEL(7:0)								@0xFE32

Name: TABLE_ELEMENT_INIT

Address: 0xFE31 – 0xFE32

Access: Read only

Reset: 0x00; 0x00

- **RX_LEVEL:** These registers store the autocorrelation level of the chirp signal.
  When the reception process has started, these registers are set by hardware.

9.5.11 RSSI_MIN Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RSSI_MIN	RSSI_MIN(7:0)							

Name: RSSI_MIN

Address: 0xFE33

Access: Read only

Reset: 0xFF

- **RSSI_MIN:** Received Signal Strength Indication Min

  This register stores the minimum RSSI value measured in the last message received.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps

9.5.12 RSSI_AVG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RSSI_AVG	RSSI_AVG(7:0)							

Name: RSSI_AVG

Address: 0xFE34

Access: Read only

Reset: 0x00

- **RSSI_AVG:** Received Signal Strength Indication Average

  This register stores the average RSSI value measured in the last message received.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps

9.5.13 RSSI_MAX Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RSSI_MAX	RSSI_MAX(7:0)							

Name: RSSI_MAX

Address: 0xFE35

Access: Read only

Reset: 0x00

- **RSSI_MAX:** Received Signal Strength Indication Max

  This register stores the maximum RSSI value measured in the last message received.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps

9.5.14 CINR_MIN Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
CINR_MIN	CINR_MIN(7:0)							

Name: CINR_MIN

Address: 0xFE38

Access: Read only

Reset: 0xFF

- **CINR_MIN:** Carrier to Interference + Noise ratio Min

  This register stores the minimum CINR value measured in the last message received.

  In order to calculate CINR properly, the algorithm takes beacon-type messages as a reference, since this message type allows knowing its content beforehand.

  The system uses a table that must be loaded with the beacon data to be received, so CINR mode must be activated (see PHY_CONFIG register) and the same procedure used to send beacons must be followed. As CINR mode is activated, physical layer will load the message in the table instead of sending it (table load time is in the order of microseconds, and is much shorter than the one used to send the message).

  Once the table is loaded, CINR must be disabled, and next messages CINR will be calculated taken the beacon loaded in the table as reference.

  The measurement is done at symbol level.

  The value is stored in ¼dB steps.

9.5.15 CINR_AVG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
CINR_AVG	CINR_AVG(7:0)							

Name: CINR_AVG

Address: 0xFE39

Access: Read only

Reset: 0x00

- **CINR_AVG:** Carrier to Interference + Noise ratio Average

  This register stores the average CINR measured in the last message received.

  In order to calculate CINR properly, the algorithm takes beacon-type messages as a reference, since this message type allows knowing its content beforehand.

  The system uses a table that must be loaded with the beacon data to be received, so CINR mode must be activated (see PHY_CONFIG register) and the same procedure used to send beacons must be followed. As CINR mode is activated, physical layer will load the message in the table instead of sending it (table load time is in the order of microseconds, and is much shorter than the one used to send the message).

  Once the table is loaded, CINR must be disabled, and next messages CINR will be calculated taken the beacon loaded in the table as reference

  The measurement is done at symbol level.

  The value is stored in ¼dB steps.

9.5.16 CINR_MAX Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
CINR_MAX	CINR_MAX(7:0)							

Name: CINR_MAX

Address: 0xFE3A

Access: Read only

Reset: 0x00

- **CINR_MAX:** Carrier to Interference + Noise ratio Max

  This register stores the maximum CINR value measured in the last message received.

  In order to calculate CINR properly, the algorithm takes beacon-type messages as a reference, since this message type allows knowing its content beforehand.

  The system uses a table that must be loaded with the beacon data to be received, so CINR mode must be activated (see PHY_CONFIG register) and the same procedure used to send beacons must be followed. As CINR mode is activated, physical layer will load the message in the table instead of sending it (table load time is in the order of microseconds, and is much shorter than the one used to send the message).

  Once the table is loaded, CINR must be disabled, and next messages CINR will be calculated taken the beacon loaded in the table as reference

  The measurement is done at symbol level.

  The value is stored in ¼dB steps.

9.5.17 EVM_HEADER Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_HEADER	EVM_HEADER(15:8)								@0xFE3B
	EVM_HEADER (7:0)								@0xFE3C

Name: EVM_HEADER

Address: 0xFE3B – 0xFE3C

Access: Read only

Reset: 0x00; 0x00

- **EVM_HEADER:** Header Error Vector Magnitude-

  These registers store in a 16-bit value the maximum error vector magnitude measured in the reception of a message header.

  The 7 MSB (EVM_HEADER(15:9)) represent the integer part in %, being the EVM_HEADER(8:0) bits the fractional part if more precision were required.

  This register is used by the physical layer for being in accordance with PRIME specification. It is reserved 32-bit in data memory to be able to declare as 32-bit variable. The 20-bit register MSB is aligned to the 32-bit variable MSB, in order to simplify arithmetic calculations with time values.

9.5.18 EVM_PAYLOAD Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_PAYLOAD	EVM_PAYLOAD(15:8)								@0xFE3D
	EVM_PAYLOAD(7:0)								@0xFE3E

Name: EVM_PAYLOAD

Address: 0xFE3D – 0xFE3E

Access: Read only

Reset: 0x00; 0x00

- **EVM_PAYLOAD:** Payload Error Vector Magnitude-

  These registers store in a 16-bit value the maximum error vector magnitude measured in the reception of a message payload.

  The 7 MSB (EVM_PAYLOAD(15:9)) represent the integer part in %, being the EVM_PAYLOAD(8:0) bits the fractional part if more precision were required.

9.5.19 EVM_HEADER_ACUM Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_HEADER_ACUM	EVM_HEADER_ACUM(19:12)								@0xFE3F
	EVM_HEADER_ACUM (11:4)								@0xFE40
	EVM_HEADER_ACUM (3:0)				“0000”				@0xFE41
	“00000000”								@0xFE42

Name: EVM_HEADER_ACUM

Address: 0xFE3F – 0xFE42

Access: Read only

Reset: 0x00, …, 0x00;

- **EVM_HEADER_ACUM:** Header Total Error Vector Magnitude Accumulator

  When receiving an OFDM symbol, the summation of all its individual carriers EVMs is calculated in order to further calculate the average EVM value. These registers store the maximum summation between the two OFDM symbols received in a message header.

9.5.20 EVM_PAYLOAD_ACUM Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_PAYLOAD_ACUM	EVM_PAYLOAD_ACUM(19:12)								@0xFE43
	EVM_PAYLOAD_ACUM(11:4)								@0xFE44
	EVM_PAYLOAD_ACUM(3:0)				“0000”				@0xFE45
	“00000000”								@0xFE46

Name: EVM_PAYLOAD_ACUM

Address: 0xFE43 – 0xFE46

Access: Read only

Reset: 0x00, …, 0x00;

- **EVM_PAYLOAD_ACUM:** Payload Total Error Vector Magnitude Accumulator

  When receiving an OFDM symbol, the summation of all its individual carriers EVMs is calculated in order to further calculate the average EVM value. These registers store the maximum summation between all the OFDM symbols received in a message payload.

9.5.21 RMS_CALC Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RMS_CALC	RMS_CALC(7:0)							

Name: RMS_CALC

Address: 0xFE58

Access: Read only

Reset: 0x00

- **RMS_CALC:** This register stores an 8-bit value which magnitude is proportional to the emitted signal amplitude.

  By measuring the amplitude of the emitted signal, the hardware can estimate the power line input impedance. Thus hardware can adjust emission configuration appropriately.

9.5.22 VSENSE_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
VSENSE_CONFIG	--				PFAILURE	PSENSE_SOFT	VFAILURE	VSENSE_EN

Name: VSENSE_CONFIG

Address: 0xFE59

Access: Read only

Reset: 0x00

- **PFAILURE:** Power Failure Flag

  This flag is set to 1 when a power failure occurs. The transmission is stopped and a new transmission is not possible if this flag is not cleared previously.

  When a power failure occurs, a consideration about decreasing voltage amplitude in the source should be taken.

  This flag must be cleared by software.

- **PSENSE_SOFT:** Current measurement is done every time a transmission takes place. With PSENSE_SOFT the system can force a continuous current measurement, including both idle and transmission states.
  - '0': Current consumption is measured every time a transmission begins (after a guard time defined by TRANS_PSENSE). NUMMILIS, NUMCYCLES and TRANS_PSENSE values must be taken into account to accurate PSENSE measurements. This is the default mode and it is the expected one when ATPL220A is working.
  - '1': Current consumption is measured both in idle and transmission states. This mode is useful for design purposes, in order to find suitable values for the current threshold (MAXPOT registers) depending on the external net requirements.
- **VFAILURE:** Voltage Failure Flag

  This flag is set to 1 when a voltage failure occurs. The transmission is stopped and a new transmission is not possible if this flag is not cleared previously.

  When a voltage failure occurs, a consideration about decreasing voltage amplitude in the source should be taken.

  This flag must be cleared by software.

- **VSENSE_EN:**VSENSE enable

  This bit enables VSENSE.
  - '0': VSENSE disabled (default).
  - '1': VSENSE enabled.

9.5.23 NUM_FAILS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
NUM_FAILS	NUM_FAILS(7:0)							

Name: NUM_FAILS

Address: 0xFE5A

Access: Read/write

Reset: 0x02

- **NUM_FAILS:** This register stores the number of 50 ns cycles (clk=20MHz) during which a voltage failure must be detected before shutting off the transmission and setting VFAILURE flag.

  This detection shall be done after a guard period set by TTRANS from the beginning of the transmission.

  Default value: 0x02 → 2 * 50 = 100ns

9.5.24 TTRANS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
TTRANS	TTRANS(7:0)							

Name: TTRANS

Address: 0xFE5B

Access: Read/write

Reset: 0x2D

- **TTRANS:** This register stores the number of 50 µs cycles (clk=20MHz) to wait from the beginning of the transmission before looking for a possible voltage failure.

  Default value: 0x2D → 45 * 50 = 2.25ms (Thus, voltage failures are not expected until the end of chirp signal period)

9.5.25 AGC0_KRSSI Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC0_KRSSI	AGC0_KRSSI(7:0)							

Name: AGC0_KRSSI

Address: 0xFE5C

Access: Read/write

Reset: 0x00

- **AGC0_KRSSI:** This register is used to correct RSSI (Received Signal Strength Indication) computation when Automatic Gain Control 0 (AGC0) is active.

9.5.26 AGC1 KRSSI Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC1_KRSSI	AGC1_KRSSI(7:0)							

Name: AGC1_KRSSI

Address: 0xFE5D

Access: Read/write

Reset: 0x00

- **AGC1_KRSSI:** This register is used to correct RSSI (Received Signal Strength Indication) computation when Automatic Gain Control 1 (AGC1) is active.

9.5.27 ZERO_CROSS_TIME Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ZERO_CROSS_TIME	ZERO_CROSS_TIME(19:12)								@0xFE69
	ZERO_CROSS_TIME (11:4)								@0xFE6A
	ZERO_CROSS_TIME (3:0)				“0000”				@0xFE6B
	“00000000”								@0xFE6C

Name: ZERO_CROSS_TIME

Address: 0xFE69 – 0xFE6C

Access: Read only

Reset: 0x00, …, 0x00;

- **ZERO_CROSS_TIME:** Instant in time at which the last zero-cross event took place. It is expressed in 10µs steps and may take values from 0 to 1e6 (20-bit effective).

  It is set by hardware and is a read-only register.

  This register is used by the physical layer for being in accordance with PRIME specification. It is reserved 32-bit in data memory to be able to declare as 32-bit variable. The 20-bit register MSB is aligned to the 32-bit variable MSB, in order to simplify arithmetic calculations with time values.

9.5.28 ZERO_CROSS_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
ZERO_CROSS_CONFIG	--					VEZC	REZC	FEZC

Name: ZERO_CROSS_CONFIG

Address: 0xFE6D

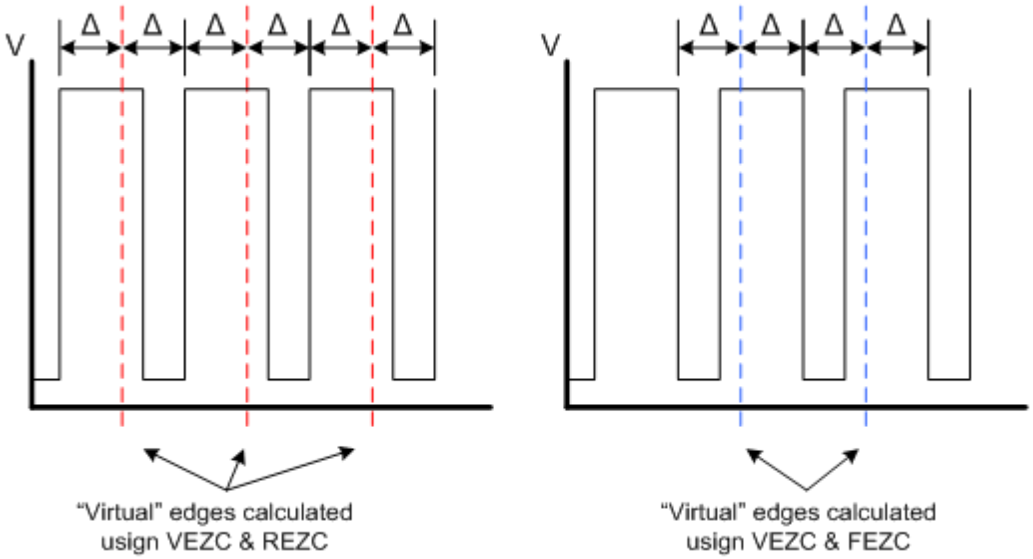
Access: Read/write

Reset: 0x06

- **--:** Reserved bits
- **VEZC:** Virtual Edge for Zero Crossing

  In this bit is equal to one, the hardware calculates the middle point between two VNR edges to calculate de zero crossing.

  This mode is used when the VNR signal duty cycle is different from 50%:



  VECZ can be used simultaneously with RECZ or FECZ.

  Using the three of them at a time is not recommended.

- **REZC**: Rising Edge for Zero Crossing

  If this bit is set to '1', the hardware uses the VNR rising edges to calculate zero-crossing.

  FEZC and REZC can be used simultaneously.

- **FEZC:** Falling Edge for Zero Crossing

  If this bit is set to '1', the hardware uses the VNR falling edges to calculate zero-crossing.

  FEZC and REZC can be used simultaneously.

9.5.29 PSENSECYCLES Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
PSENSECYCLES	--				FLAG_PSENSE	D(18:16)			@0xFE7D
	D(15:8)								@0xFE7E
	D(7:0)								@0xFE7F

Name: PSENSECYCLES

Address: 0xFE7D – 0xFE7F

Access: Read/write

Reset: 0x00, …, 0x00;

- **--:** Reserved bits
- **FLAG_SENSE:** Whenever a new power value is written in PSENSECYCLES, FLAG_PSENSE is set 1.

  This flag must be cleared by software
- **D(17:0):** Power supply consumption measurement

  The power supply line is sampled (=20MHz), and the number of logic '1' detected during NUMMILIS milliseconds is stored in this field in order to calculate power consumption.

  Note: The first valid value is written after NUMMILIS, and then a new valid value is written every NUMMILIS milliseconds.

  Note: Measurement is only active when a message transmission begins or PSENSE_SOFT bit is active (see Name:9.5.22)

9.5.30 MEAN Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
MEAN	--				FLAG_MEAN	D(18:16)			@0xFE80
	D(15:8)								@0xFE81
	D(7:0)								@0xFE82

Name: PSENSECYCLES

Address: 0xFE80 – 0xFE82

Access: Read/write

Reset: 0x00, …, 0x00;

- **--:** Reserved bits
- **FLAG_MEAN:** Whenever a new value is written in MEAN, FLAG_MEAN is set to '1'

  This flag must be cleared by software
- **D(17:0):** This value stores the average power consumption calculated from the value in PSENSECYCLES and having into account the convergence factor "A" (see A_NUMMILIS register in 9.5.36).

  Note: The first valid value is written after NUMCYCLES*NUMMILIS, and then a new valid value is written every NUMMILIS milliseconds

9.5.31 PMAX Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
PMAX	--				FLAG_PMAX	D(18:16)			@0xFE83
	D(15:8)								@0xFE84
	D(7:0)								@0xFE85

Name: PMAX

Address: 0xFE83 – 0xFE85

Access: Read/write

Reset: 0x00, …, 0x00;

- **--:** Reserved bits
- **FLAG_PMAX:** Whenever a new value is written in PMAX, FLAG_PMAX is set to '1'.

  This flag must be cleared by software
- **D(17:0):** As described in MAXPOT register (see 9.5.34), every time the average power consumption exceeds a user defined threshold value, the current transmission is cancelled.

  PMAX register stores the average power consumption value that has risen above MAXPOT threshold.

9.5.32 TRANS_PSENSE Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
TRANS_PSENSE	TRANS_PSENSE(7:0)							

Name: TRANS_PSENSE

Address: 0xFE86

Access: Read/write

Reset: 0x2B

- **TRANS_PSENSE:** This register stores the number of 50 µs cycles to wait from the beginning of a transmission before looking for a possible power failure. This guard time is taken to avoid transient period where the measurement would be inaccurate
  Default value: 0x2B → 43 * 50 = 2.15ms

9.5.33 P_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
P_TH	--					P_TH(18:16)			@0xFE87
	P_TH(15:8)								@0xFE88
	P_TH(7:0)								@0xFE89

Name: P_TH

Address: 0xFE87 – 0xFE89

Access: Read/write

Reset: 0x07, 0xFF, 0xFF.

- **--:** Reserved bits
- **P_TH:** These registers contain a user defined power threshold. When the threshold value is exceeded, a low power consumption mode is automatically activated. In this low power consumption mode, the power dissipated in the transistors decreases at the expense of distortion increasing.

9.5.34 MAXPOT Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
MAXPOT	--					MAXPOT(18:16)			@0xFE8A
	MAXPOT (15:8)								@0xFE8B
	MAXPOT (7:0)								@0xFE8C

Name: MAXPOT

Address: 0xFE8A – 0xFE8C

Access: Read/write

Reset: 0x07, 0xFF, 0xFF.

- **--:** Reserved bits
- **MAXPOT:** These registers contain a user defined power consumption threshold. When this threshold is exceeded, current transmission is cancelled.

  When the threshold is exceeded, two flags are activated:

  - POTFAILURE flag (see VSENSE_CONFIG in 9.5.22). This flag indicates that a power failure has occurred.
  - FLAG_PMAX flag (see PMAX in 9.5.31). This flag indicates that, after a power failure, the last mean power value measured has been stored in PMAX register.

  To reset both flags is enough to reset either of them, the other will be automatically reset. This will enable to start new transmissions.

9.5.35 NUMCYCLES Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
NUMCYCLES	NUMCYCLES(7:0)							

Name: NUMCYCLES

Address: 0xFE8D

Access: Read/write

Reset: 0x05

- **NUMCYCLES:** Number of cycles of measuring power before obtaining a mean value that can be taken as valid.

  Example1: If NUMCYCLES=5(cycles) and NUMMILIS=1(milliseconds), 5 power measurements will be taken during 1 millisecond each one .The first valid power measurement value will be output in the fifth millisecond.

  Example2: If NUMCYCLES=3(cycles) and NUMMILIS=20(milliseconds), 3 power measurements will be taken during 20 milliseconds each one. The first valid power measurement value will be output after 60 milliseconds.

9.5.36 A_NUMMILIS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
NUMMILIS	--	A(1:0)		NUMMILIS(4:0)				

Name: A_NUMMILIS

Address: 0xFE8E

Access: Read/write

Reset: 0x21

- **--:** Reserved bits
- **A(1:0):** Convergence Factor

  Averaging factor that sets the convergence speed of the mean calculation algorithm.

  A=00 sets quicker convergence, while A=11 sets the slowest one. A=01,10 are intermediate values.

  Note: Power supply presents high dispersion values, so NUMMILIS value must be take into account in order to select a suitable value for A. If NUMMILIS is high, the mean value can be calculated slowly, because the averaging in being calculated over a long period of time. When NUMMILIS is low, the mean value must be calculated quickly in order to obtain more accurate values.
- **NUMMILIS(4:0):** Measurement acquisition time in milliseconds

  Stores the measurement acquisition time in milliseconds.

  Example1: If NUMCYCLES=5(cycles) and NUMMILIS=1(milliseconds), 5 power measurements will be taken during 1 millisecond each one .The first valid power measurement value will be output in the fifth millisecond.

  Example2: If NUMCYCLES=3(cycles) and NUMMILIS=20(milliseconds), 3 power measurements will be taken during 20 milliseconds each one. The first valid power measurement value will be output after 60 milliseconds.

9.5.37 EMIT_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
EMIT_CONFIG	--						TR_EMIT	TWO_H_BRIDGES

Name: EMIT_CONFIG

Address: 0xFE8F

Access: Read/write

Reset: 0x03

- **TR_EMIT:** Emission mode
  This bit selects the emission mode (Internal Drive or External transistors bridge).
  - '0': Emission is done by means of internal ATPL220A driver.
  - '1': Emission is done by means of external transistors (Default).
- **TWO_H_BRIDGES:** This bit selects the number of semi-H-bridges in the external interface.
  - '0': There is only one semi-H-bridge in the external interface.
  - '1': There are two semi-H-bridges in the external interface and the field HIMP (AFE_CTL register) determines which one is active (Default).

  Semi-H-Bridges must be connected following the table below

	TWO_H_BRIDGES='0'	TWO_H_BRIDGES='1'
EMIT1	P	P1
EMIT2	P	P1
EMIT3	P	P1
EMIT4	P	N1
EMIT5	P	N1
EMIT6	P	N1
EMIT7	N	P2
EMIT8	N	P2
EMIT9	N	P2
EMIT10	N	N2
EMIT11	N	N2
EMIT12	N	N2

9.5.38 AFE_CTL Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AFE_CTL	--			HIMP	HIMP_INV	TXRX	TXRX_HARD	TXRX_INV

Name: AFE_CTL

Address: 0xFE90

Access: Read/write

Reset: 0x10

- **--:** Reserved bits
- **HIMP:** Analog Front End Impedance control bit-

  This bit selects which branch is active when working with a two half-H-bridge branches analog front end.

  - '0': "Low impedance" half-H-bridge is active (P2-N2).
  - '1': "High impedance" half-H-bridge is active (P1-N1).
- **HIMP_INV:** HIMP pin polarity control

  This field inverts the polarity of the HIMP pin output.

  Note: This field only affect to the polarity of the external pin HIMP output, the value taken from HIMP bit (AFE_CTL(4)) remains unchanged
- **TXRX:** The value stored in this bit is taken by the microcontroller in order to set the TXRX pin level.
  - '0': TXRX pin output = '0'.
  - '1': TXRX pin output = '1'.
- **TXRX_HARD:** TXRX pin control

  This field selects if the TXRX pin is software/hardware controlled.
  - '0': TXRX pin is software controlled. TXRX value is set by TXRX bit field (AFE_CTL(2)).
  - '1': TXRX pin is hardware controlled.
- **TXRX_INV:** TXRX pin polarity control

  This field inverts the polarity of the TXRX pin output

9.5.39 R Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
R1	R1(7:0)								0xFE9F
R2	R2(7:0)								0xFEA0
R3	R3(7:0)								0xFEA1
R4	R4(7:0)								0xFEA2
R5	R5(7:0)								0xFEA3
R6	R6(7:0)								0xFEA4
R7	R7(7:0)								0xFEA5
R8	R8(7:0)								0xFEA6

Name: R1 – R8

Address: 0xFE9F – 0xFEA6

Access: Read/write

Reset: 0x60; 0x60; 0x60; 0x60; 0xFF; 0xFF; 0xFF; 0xFF.

- **R:** The value in these registers strongly depends on the external circuit configuration.
  Atmel provides values to be used according with the design recommended in ATPL220A kits
  Please contact Atmel Power Line if different external configurations are going to be used

  Recommended values (according to the configuration recommended in ATPL220A kits)
  R1(7:0): 0x21
  R2(7:0): 0x20
  R3(7:0): 0x12
  R4(7:0): 0x02
  R5(7:0): 0x37
  R6(7:0): 0x77
  R7(7:0): 0x37
  R8(7:0): 0x77

  Order of precedence: In the event of a conflict between the Ri(7:0) values above and Ri(7:0) values specified in the latest documentation in an ATPL220A kit, the values in the kit documentation shall take precedence.

9.5.40 PHY_ERRORS Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
PHY_ERRORS	--			PHY_ERRORS(4:0)				

Name: PHY_ERRORS

Address: 0xFE94

Access: Read/write

Reset: 0x00

- **--:** Reserved bits
- **PHY_ERRORS:** Physical Layer Error Counter

  The system stores in these bits the number of times that a Physical layer error has occurred. Microcontroller can clear this counter to zero.

  The value stored in this register is cleared every time the register is read.

9.5.41 FFT_MODE Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
FFT_MODE	NSYM(5:0)						CONTINUOUS	TEST_MODE_EN

Name: FFT_MODE

Address: 0xFEB0

Access: Read/write

Reset: 0x00

- **NSYM:** Number of symbols to transmit

  When in continuous transmission mode, symbol data acts as a free-running buffer, increasing from 0 to NSYM-1 and overflowing back to symbol 0.
- **CONTINUOUS:** This field enables/disables continuous transmission mode.
  - '0': Continuous transmission mode disabled.
  - '1': Continuous transmission mode enabled.
- **TEST_MODE_EN:** This field enables/disables test mode
  - '0': Test mode disabled.
  - '1': Test mode enabled.

Configuration for test mode. This register is used by the physical layer to fulfill with PRIME specification (PLME_TESTMODE.request primitive and PLME_TESTMODE.confirm primitive, see PRIME specification). In this mode data provided to FFT is written in data memory at ADDR_PHY_INI_TX, codifying each value with 4 bits according to DPSK modulation mapping. The msb of the value is to indicate an input of zero when set to '1'. Each byte in data memory contains 2 input values for FFT, with the first value located at high bits. There are 97 input values for FFT, so many as the number of subcarriers, so there are 48 bytes and a half of the next byte used for codifying them. The other half of this byte (low bits) will be used for the next symbol data.

9.5.42 AGC_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC_CONFIG	--		AGC0_POL	AGC0_VALUE	AGC0_MODE	AGC1_POL	AGC1_VALUE	AGC1_MODE

Name: AGC_CONFIG

Address: 0xFEB1

Access: Read/write

Reset: 0x24

ATPL220A has implemented two Automatic Gain Control outputs in order to adjust the received signal level to a suitable range. When in “automatic” mode, both of them are set to ‘1’ when the received signal is above a 16-bit-user-definable thresholds (AGC1_TH and AGC0_TH) in order to activate external attenuators placed in the external analog front end.

The value of these outputs is set during the beginning of a received message and is hold until the end of the message.

AGC0 and AGC1 follow different algorithms, thus using both of them ensures more accurate gain control

- --: Reserved bits
- **AGC0_POL:** AGC0 polarity

  This bit sets the polarity of the AGC0 output.
  - ‘0’: Polarity is inverted.
  - ‘1’: Polarity is not inverted (default).
- **AGC0_VALUE:** AGC0 output value-

  This bit stores the value wrote by the user to be the AGC0 output.

  This bit is only taken into account when AGC0 “forced” mode is active (AGC0_MODE=’1’).

  AGC0_POL field can invert this value.
- **AGC0_MODE:** AGC0 mode

  This bit selects which AGC0 mode is being used
  - ‘0’: “Automatic” Mode. AGC0 output will be managed by the MAC, depending on saturation detected in received signal. If saturation is detected, AGC0 output will be ‘1’. Else, AGC0 output will be ‘0’. AGC0_POL field can invert this value.

    (See SAT_TH registers in 9.5.43)
  - ‘1’: “Forced” Mode. AGC0 output will be managed by the user, according to the value wrote in AGC0_VALUE field (AGC_CONFIG(4)).
- **AGC1_POL:** AGC1 polarity

  This bit sets the polarity of the AGC1 output.
  - ‘0’: Polarity is inverted.
  - ‘1’: Polarity is not inverted (default).
- **AGC1_VALUE:** AGC1 output value-

  This bit stores the value wrote by the user to be the AGC1 output.

  This bit is only taken into account when AGC1 “forced” mode is active (AGC1_MODE=’1’).

  AGC1_POL field can invert this value.

- **AGC1_MODE:** AGC1 mode

  This bit selects which AGC1 mode is being used

  - ‘0’: “Automatic” Mode. AGC1 output will be managed by the MAC, depending on saturation detected in received signal. If saturation is detected, AGC1 output will be ‘1’. Else, AGC1 output will be ‘0’. AGC1_POL field can invert this value.

    (See SAT_TH registers in 9.5.43)
  - ‘1’: “Forced” Mode. AGC1 output will be managed by the user, according to the value wrote in AGC1_VALUE field (AGC_CONFIG(4)).

9.5.43 SAT_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
SAT_TH	SAT_TH(15:8)								@0xFEB7
	SAT_TH(7:0)								@0xFEB8

Name: SAT_TH

Address: 0xFEB7 – 0xFEB8

Access: Read/write

Reset: 0x40; 0x00

- **SAT_TH:** These registers store a threshold for the PLC input-signal amplitude.

  If this threshold is exceeded, AGC thresholds (AGC0_TH and AGC1_TH) will be taken into account.

  If this threshold is not exceeded, AGC0_TH and AGC1_TH thresholds will be ignored, thus the AGC algorithm will be never triggered.

  Recommended value for Atmel reference design = 0x37AA.

9.5.44 AGC1_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AGC1_TH	AGC1_TH(15:8)								@0xFE5F
	AGC1_TH(7:0)								@0xFE60

Name: AGC1_TH

Address: 0xFE5F – 0xFE60

Access: Read/write

Reset: 0x40; 0x00

- **AGC1_TH:** AGC1 Threshold

  These registers store the 16-bit upper threshold used by the AGC1 algorithm to determine that the input signal must be attenuated.

  This threshold is only taken into account in AGC1 “automatic” mode (AGC_CONFIG.AGC1_MODE=’0’).

  This threshold is only taken into account if SAT_TH value is exceeded.

  Recommended value for Atmel reference design = 0x4A00.

9.5.45 AGC0_TH Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AGC0_TH	AGC0_TH(15:8)								@0xFEB2
	AGC0_TH(7:0)								@0xFEB3

Name: AGC0_TH

Address: 0xFEB2 – 0xFEB3

Access: Read/write

Reset: 0x10; 0x00

- **AGC0_TH:** AGC0 Threshold

  These registers store the 16-bit upper threshold used by the AGC0 algorithm to determine that the input signal must be attenuated.

  This threshold is only taken into account in AGC0 “automatic” mode (AGC_CONFIG.AGC0_MODE=’0’).

  This threshold is only taken into account if SAT_TH value is exceeded.

  Recommended value for Atmel reference design = 0x1000.

9.5.46 AGC_PADS Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
AGC_PADS	--						P46_MODE	SWITCH_AGC

Name: AGC_PADS

Address: 0xFE61

Access: Read/write

Reset: 0x00

- --: Reserved bits
- **P46_MODE:** This field controls the P4.6/T2/AGC1 output pin (pin no.94).
  - '0': Pin no.94 works as P4.6/T2 output pin.
  - '1': Pin no.94 works as AGC1 output pin.
- **SWITCH_AGC:** This bit switches the AGC0 and AGC1 outputs.
  - '0': Not switched AGC outputs.
  - '1': Switched AGC outputs.

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

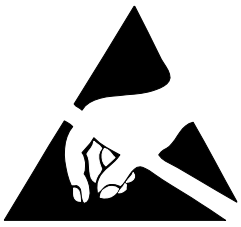
Table 10-1. ATPL220A Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	-0.5 to 4.0	V
Input Voltage	VI	-0.5 to VCC+0.5(≤4.0V)	V
Output Voltage	VO	-0.5 to VCC+0.5(<4.0V)	V
Storage Temperature	TST	-55 to 125	ºC
Junction Temperature	TJ	-40 to 125	ºC
Output Current(1)	IO	±10(2)	mA

Notes: 1. DC current that continuously flows for 10ms or more, or average DC current.

2. Applies to all the pins except EMIT pins. EMIT pins should be only used according to circuit configurations recommended by Atmel Power Line.

ATTENTION observe EDS precautions



Precautions for handling electrostatic sensitive devices should be taken into account to avoid malfunction. Charged devices and circuit boards can discharge without detection

10.2 Recommended Operating Conditions

Table 10-2. ATPL220A Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VCC	3.00	3.30	3.60	V
	VDE0	3.00	3.30	3.60	
	AVD	3.00	3.30	3.60	
Junction Temperature	TJ	-40	25	125	ºC
Ambient Temperature	TA	-40	--	85	

10.3 DC Characteristics

Table 10-3. ATPL220A DC Characteristics

Parameter	Condition	Symbol	Rating			Unit
			Min.	Typ.	Max.	
Supply Voltage		VCC	3.00	3.30	3.60	V
H-level Input Voltage (3.3v CMOS)		VIH	2.0	-	VCC+0.3	
L-level Input Voltage (3.3v CMOS)		VIL	-0.3	-	0.8	
H-level Output Voltage	3.3v I/O IOH=-100µA	VOH	VCC-0.2	-	VCC	
L-level Output Voltage	3.3v I/O IOL=100µA	VOL	0	-	0.2	
H-level Output V-I Characteristics	3.3v I/O VCC=3.3±0.3	IOH	See 10.3.2			mA
L-level Output V-I Characteristics	3.3v I/O VCC=3.3±0.3	IOL	See 10.3.2			
Internal Pull-up Resistor(1)	3.3v I/O	Rpu	10	33	80	kΩ
Internal Pull-down Resistor(1)	3.3v I/O	Rpd	10	33	80	kΩ
Junction Temperature		TJ	-40	-	125	ºC

Notes: 1. Only applicable to pins with internal pulling. See Table 2-1.

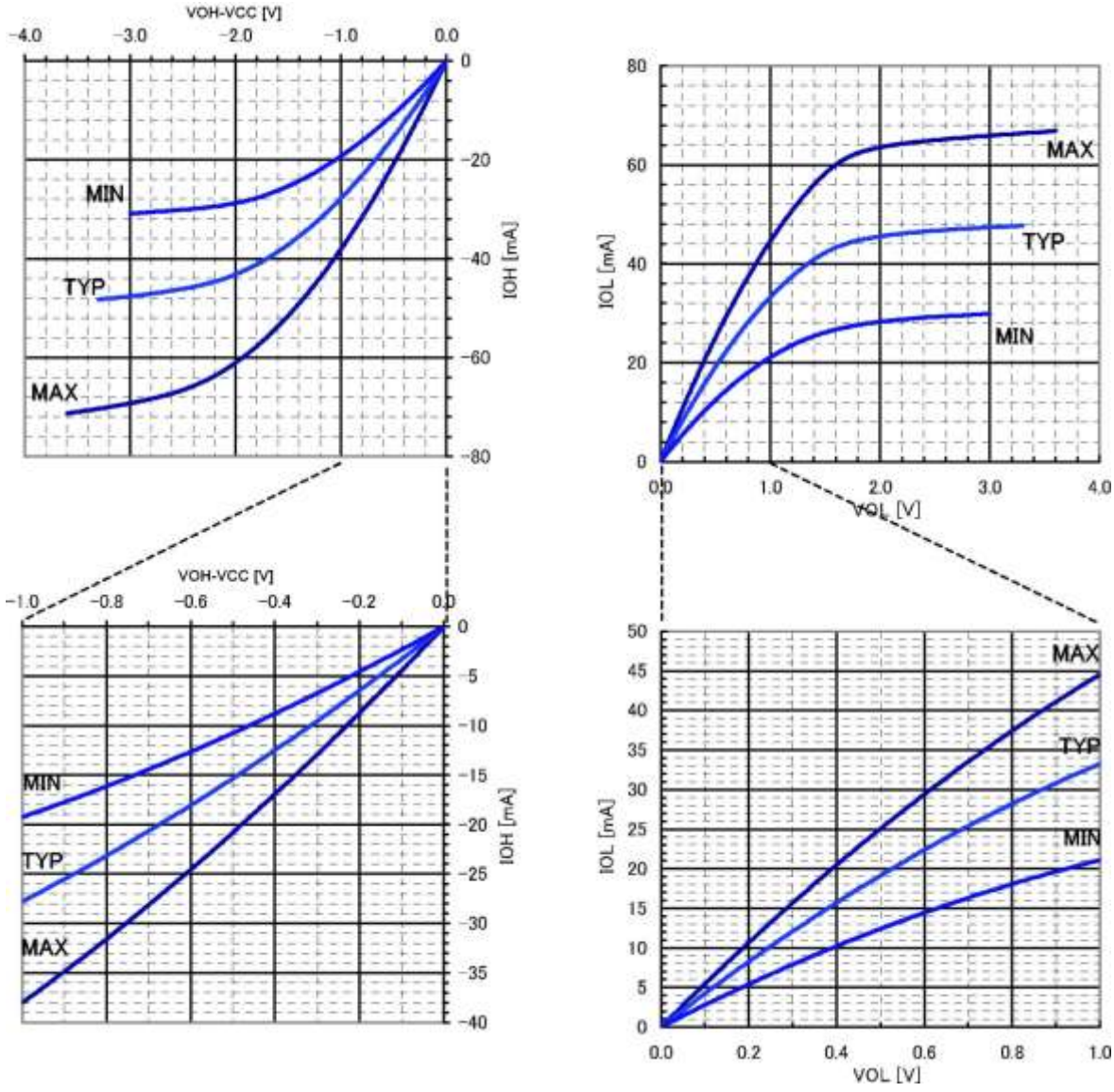
10.3.2 V-I curves

V-I Characteristics 3.3 Vstandard CMOS IO L, M type

Pins marked in Table 2-1 with Nominal Current I(mA)=±5

Condition:	MIN	Process=	Slow	Tj=	125°C	VCC=	3.0 V
	TYP	Process=Typical		Tj=	25°C	VCC=	3.3 V
	MAX	Process=Fast		Tj=	-40°C	VCC=	3.6 V

Figure 10-1. CMOS IO L and M type,V-I curves

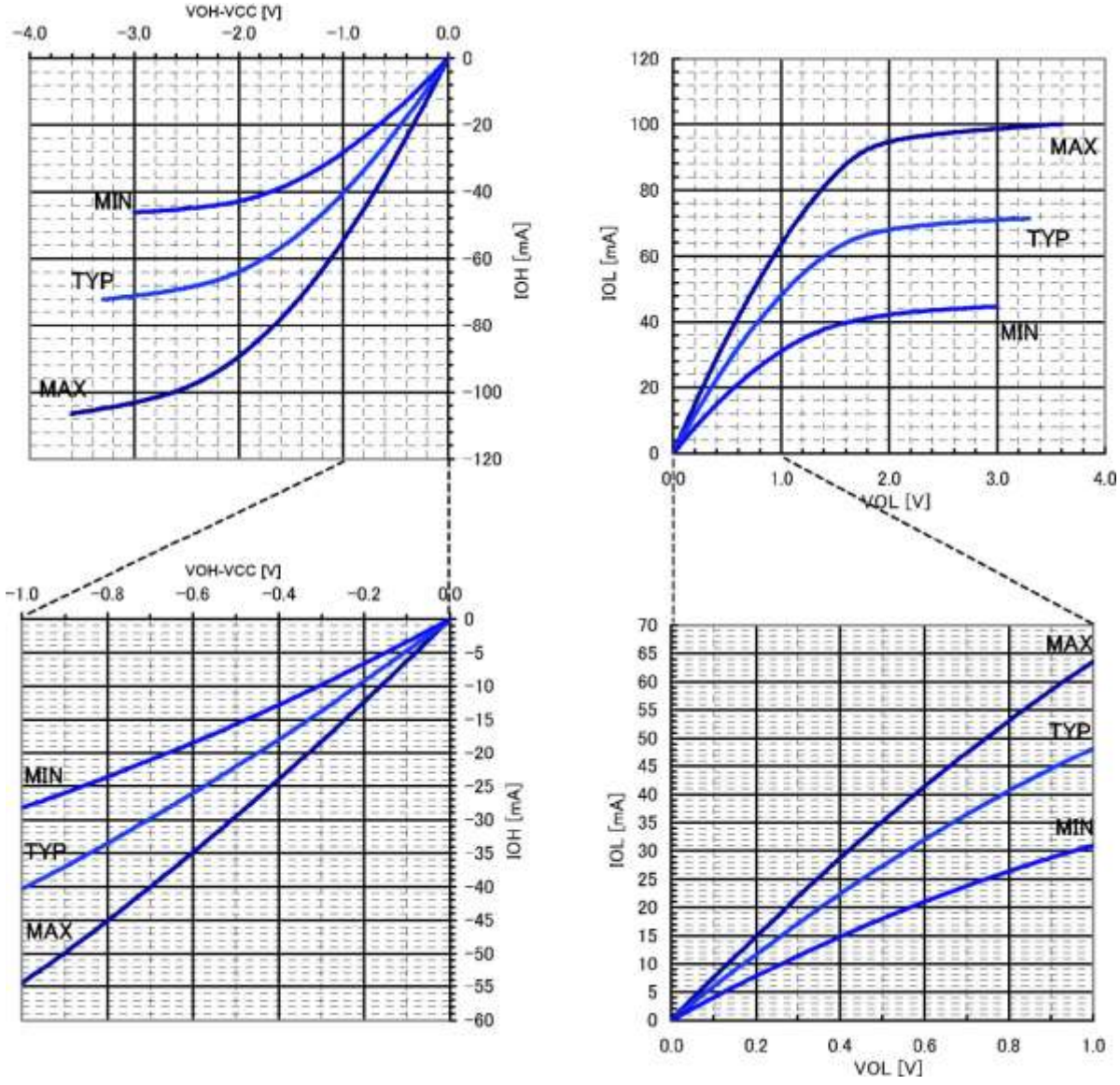


V-I Characteristics 3.3 Vstandard CMOS IO H, V type

Pins marked in Table 2-1 with Nominal Current I(mA)=±10

Condition:	MIN	Process=	Slow	Tj=	125°C	VCC=	3.0 V
	TYP	Process=Typical		Tj=	25°C	VCC=	3.3 V
	MAX	Process=Fast		Tj=	-40°C	VCC=	3.6 V

Figure 10-2. CMOS IO H and V type, V-I curves

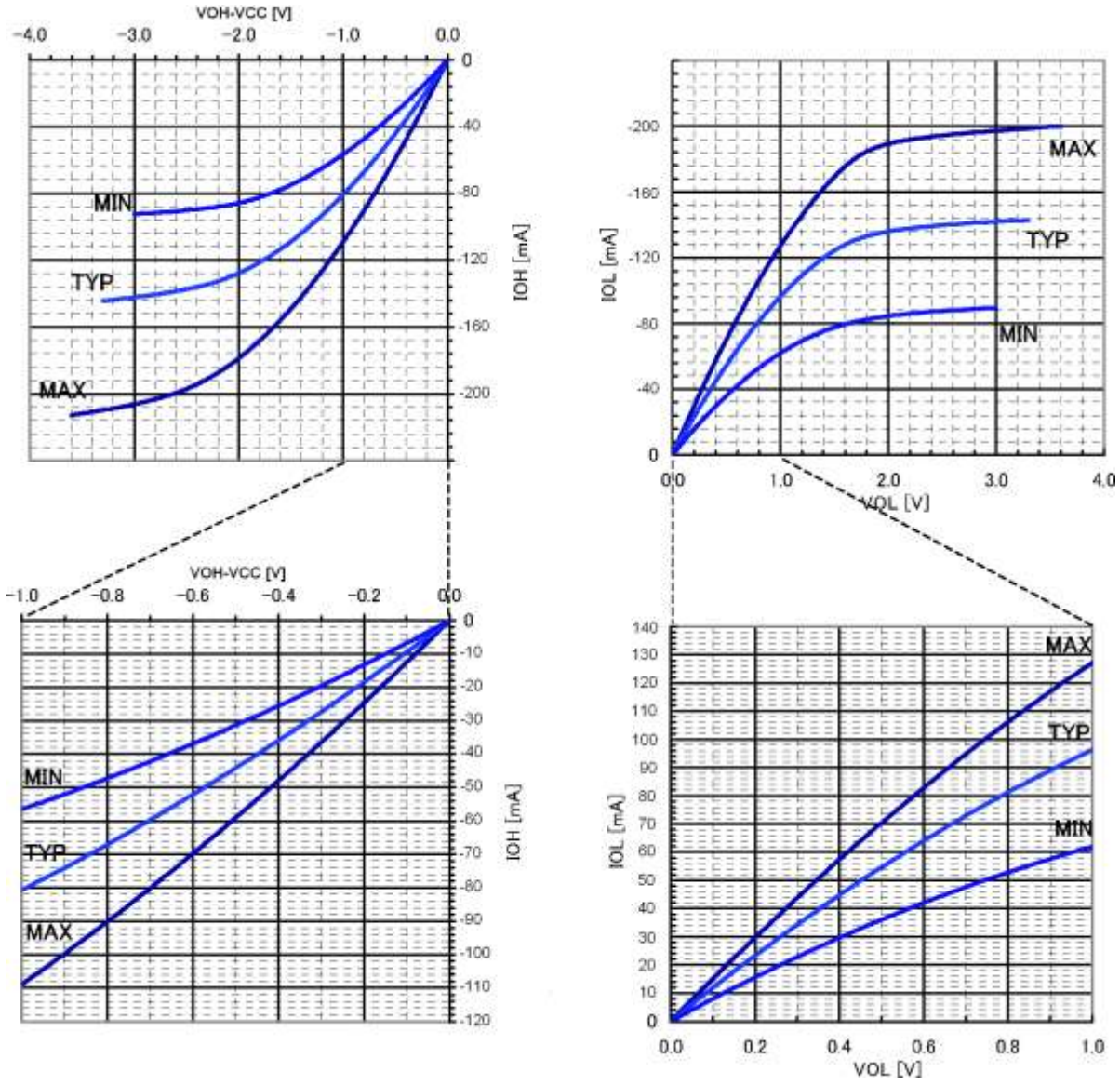


V-I Characteristics 3.3 Vstandard CMOS IO X type

Pins marked in Table 2-1 with Nominal Current I(mA)=±X

Condition:	MIN	Process=	Slow	Tj=	125°C	VCC=	3.0 V
	TYP	Process=Typical		Tj=	25°C	VCC=	3.3 V
	MAX	Process=Fast		Tj=	-40°C	VCC=	3.6 V

Figure 10-3. CMOS IO X type, V-I curves



10.4 Power Consumption

Table 10-4. ATPL220A Power Consumption

Parameter	Condition	Symbol	Rating			Unit
			Min.	Typ.	Max.	
Power Consumption	TA=25°C, VCC=3.3v	P_{25}	--	260	--	mW
Power Consumption (worst case)	TA=85°C, VCC=3.6v	P_{85}	--	--	355	--

10.5 Thermal Data

Table 10-5. ATPL220A Thermal Data

Parameter	Symbol	LQFP144	Unit
Thermal resistance junction-to-ambient steady state	$R_{Theta-ja}$	60(1)	ºC/W
		40(2)	

Notes: 1. Mounted on 2-layer PCB.
2. Mounted on 4-layer PCB.

Theta-ja is calculated based on a standard JEDEC defined environment and is not reliable indicator of a device's thermal performance in a non-JEDEC environment. The customer should always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.

10.6 Oscilator

Figure 10-4. External Crystal configuration

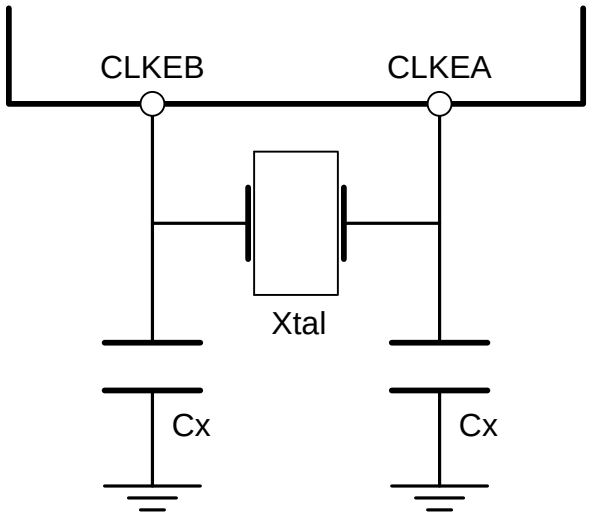
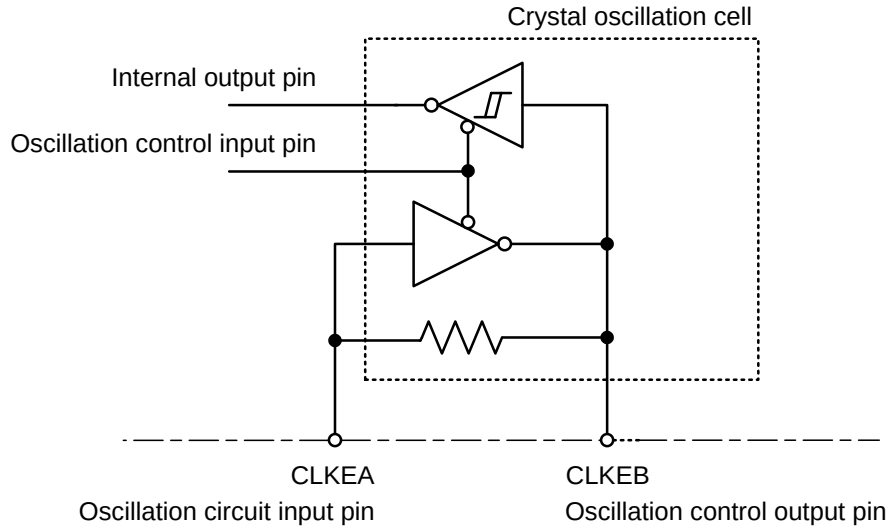


Table 10-6. External oscillator parameters

Parameter	Test Condition	Symbol	Rating			Unit
			Min.	Typ.	Max.	
Crystal Oscillator frequency	fundamental	Xtal		20		MHz
External Oscillator Capacitance	See Figure 10-4	Cx	5	18	30	pF
H-level Input Voltage		XVIH	2	-	VCC+0.3	V
L-level Input Voltage		XVIL	-0.3	-	0.8	
External Oscillator Parallel Resistance		Rp	*not needed*			Ω
External Oscillator Series Resistance		Rs	*not needed*			

Notes:
1. The crystal should be located as close as possible to CLKEB and CLKEA pins.
2. Recommended value for Cx is 18pF. This value may depend on the specific crystal characteristics.
3. Crystal Stability/Tolerance/Ageing values must be selected according to standard PRIME requirements.

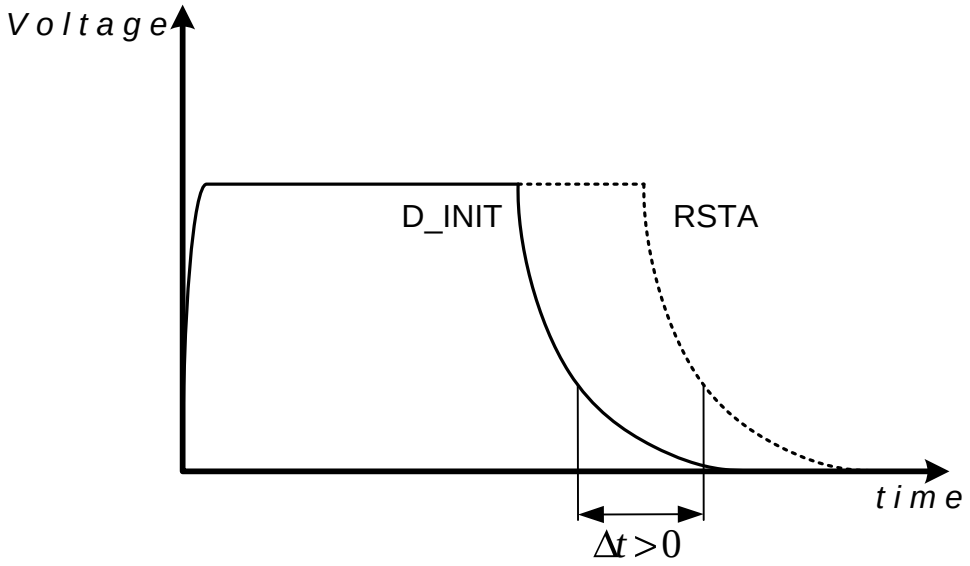
Figure 10-5. Internal Oscillator Cell



10.7 Power On

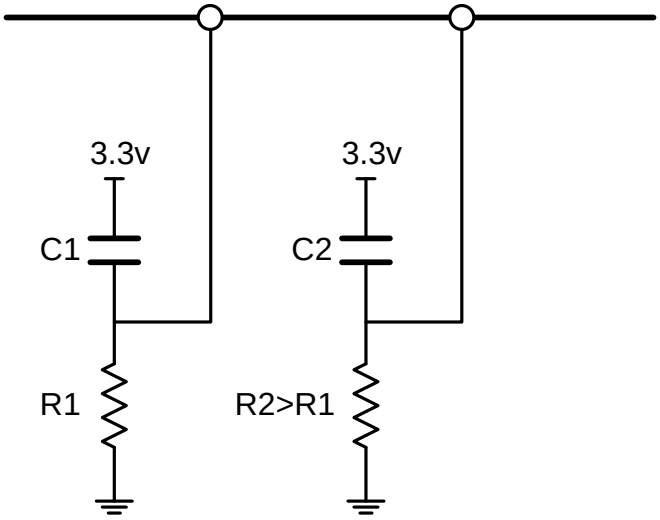
During power-on, D_INIT should be released before asynchronous reset signal RSTA in order to ensure proper system start up.

Figure 10-6. D_INIT & RSTA realease sequence during power-on



Not minimum time is required between both releases, $\Delta t > 0$, so a simple RC circuit is enough to satisfy this requirement.

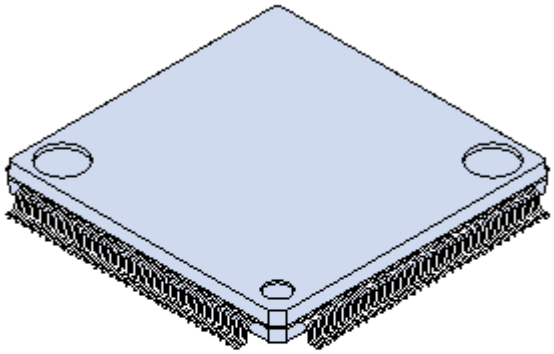
Figure 10-7. Example circuit



11. Mechanical Characteristics

Figure 11-1. 120-lead LQFP Package Mechanical Drawing

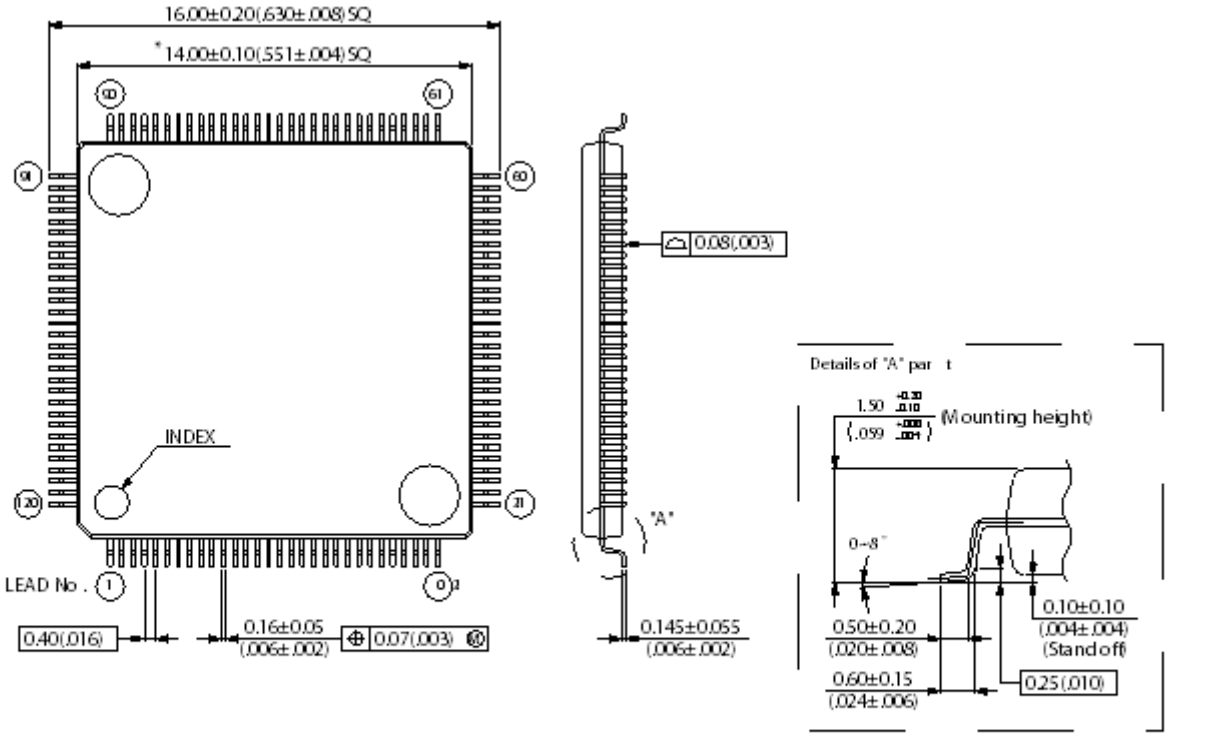
120-pin plastic LQFP



Lead pitch	0.40 mm
Package width · package length	14.0 mm · 14.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Code (Reference)	P-LFQFP120-14 · 14-0.40

120-pin plastic LQFP

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

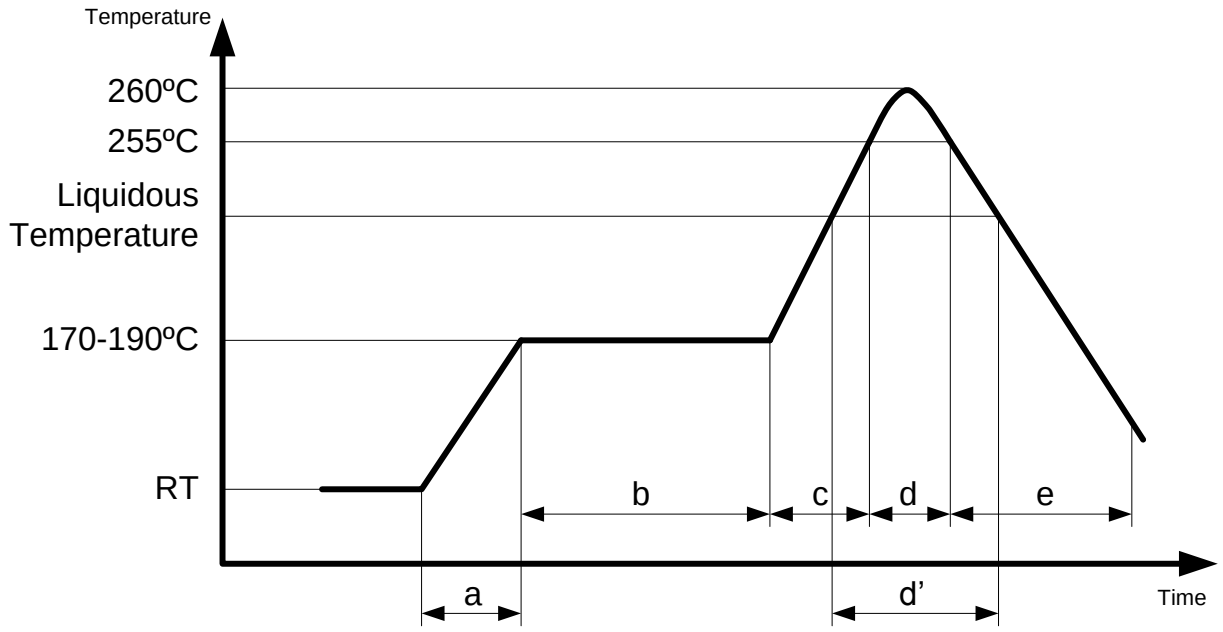
12. Recommended mounting conditions

12.1 Conditions of Standard Reflow

Table 12-1. Conditions of standard Reflow

Items	Contents	
Method	IR(Infrared Reflow)/Convection	
Times	2	
Floor Life	Before unpacking	Please use within 2 years after production
	From unpacking to second reflow	Within 8 days
	In case over period of floor life	Baking with 125ºC +/- 3ºC for 24hrs +2hrs/-0hrs is required. Then please use within 8 days. (please remember baking is up to 2 times)
Floor Life Condition	Between 5ºC and 30ºC and also below 70%RH required. (It is preferred lower humidity in the required temp range.)	

Figure 12-1. Temperature Profile



Note: H rank: 260ºC Max

a: Average ramp-up rate: 1ºC/s to 4ºC/s

b: Preheat & Soak: 170ºC to 190ºC, 60s to 180s

c: Average ramp-up rate: 1ºC/s to 4ºC

d: Peak temperature: 260ºC Max, up to 255ºC within 10s

d': Liquidous temperature: Up to 230ºC within 40s or
Up to 225ºC within 60s or
Up to 220ºC within 80s

e: Cooling: Natural cooling or forced cooling

12.2 Manual Soldering

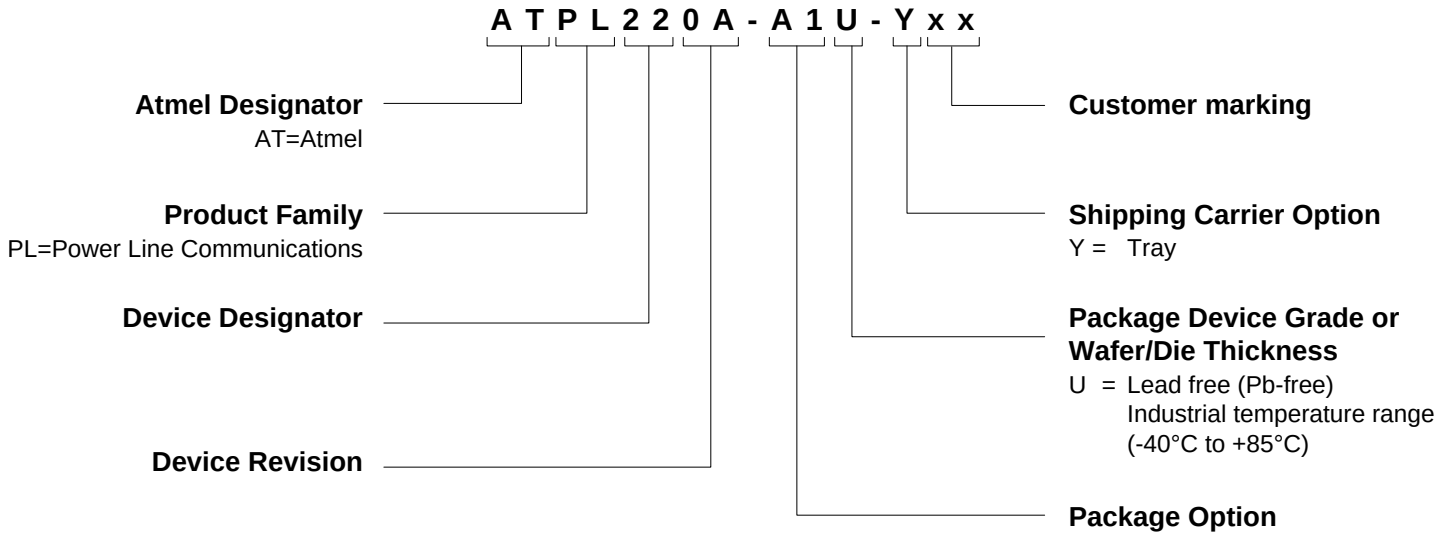
Table 12-2. Conditions of Manual Soldering

Items	Contents	
Floor life	Before unpacking	Please use within 2 years after production
	From unpacking to Manual Soldering	Within 2 years after production (No control required for moisture adsorption because it is partial heating)
Floor life condition	Between 5°C and 30°C and also below 70%RH required. (It is preferred lower humidity in the required temp range.)	
Solder Condition	Temperature of soldering iron: Max 400°C, Time: Within 5 seconds/pin *Be careful for touching package body with iron	

13. Ordering Information

Table 13-1. Atmel ATPL220A Ordering Codes

Atmel Ordering Code	Package	Package Type	Temperature Range
ATPL220A-A1U-Y	120 LQFP	Pb-Free	Industrial (-40ºC to 85º)



14. Revision History

Doc. Rev.	Date	Comments
A	07/06/2012	Initial release

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