Contents

Atmel FPGA Integrated Development System (IDS) contains the following items:

- IDS Installation Guide
- · CD-ROM containing all necessary software and online documents

Features

- Support for Industry-standard PC and Workstation Tools
- Schematic, PLD, Verilog[®] and VHDL Design Entry Supported
- Macro Libraries for AT40K/AT40KAL and AT6000 FPGA Families
- Automatic Macro Generators for AT40K and AT6000
- HDL Planner for VHDL and Verilog Entry
- Hierarchy Browser
- User Library Management
- Technology Mapping
- Multi-chip Partitioning
- Floor Planning Capability
- Graphical Constraint Entry
- Incremental Design Change
- Timing Driven Design with Advanced Static Timing Analysis
- Automatic Place and Route
- Interactive Layout Editing
- Power Calculation
- Full Back-annotation for Functional and Post-layout Simulation
- Online Tutorials for New and Advanced Users
- Applications Support
- FPGA Applications Hotline (408) 436-4119 or fpga@atmel.com
- FAQ and Application Notes at http://www.atmel.com/atmel/products/prod3.htm
- Maintenance
- Software Support for One Month is Included

Description

Atmel's Integrated Development System (IDS) lets designers create fast, predictable designs with AT40K/AT40KAL and AT6000 Series FPGAs.

Available for use with Windows[®] 98/2000, Windows NT[®] and Sun Solaris[™]/SunOS UNIX Workstation-based computers, IDS combines industry-standard software for design entry, synthesis and simulation with Atmel's proprietary software for component generation, automatic and interactive placement and routing, timing analysis and bitstream generation.

The IDS Desktop is shown in Figure 1. The Design Flow Bar provides push-button access to all the steps in the design flow. This includes opening schematic entry and synthesis tools and generating files for simulations automatically.

Figure 2 shows the HDL Planner tool which is used for VHDL and Verilog Design Entry. Figure 3 shows the Macro Generator used to generate standard components with optimal layout and performance.



Atmel FPGA Integrated Development System (IDS)







Figure 1. Integrated Development System

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FPGA IDS

Figure 2. HDL Planner Tool

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Figure 3. Macro Generator

| AT40K Macro Ge | enerators | | | | _ 🗆 |
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| NoRegister | C Register | C Disabled | | Adder-Carry Select | |
| CarryOut | O Register | Disabled | Ade | der-Ripple Carry | |
| | | | Co | mparator | |
| - | nput 💿 Outpu | t 🔿 Both | De | eductor | |
| Signed Overflov | v Pin | | In | crement/Decrement by * | 1 |
| Width 4 | Pitch 1 | Aspect Ratio | 0.50 | ncrement/Decrement by | value |
| | | · | | Multiplier-Serial Parallel | |
| Invert clock | M | Initialization Polarity | / = Low | Multiplier-Signed | |
| Reset | O Set | None | | Multiplier-Unsigned | |
| | | 1 | | Multiplier-Signed Pipelin | |
| | | | | Multiplier-Unsigned Pipe | |
| Arithmetic | Counters DSP | I/O Logic Memo | | - | |
| | | | ory 🕨 | Options | |
| Macro Name | add_r4 | | | Hard Macro | |
| Pin Map File Name | | | | Generate So | chematic |
| User Library | user.lib | | | ✓ Brpwse | Batch |
| Add to Batch | Generate | Cancel | Help | View Batch | Size 0 |
| | | | | | Ĩ |
| atch Macro Gene ability Categori | | omponent Options | | Macro Generator Components | Batch Size Indicator |

Ordering IDS and CAE Tools

When IDS is shipped, the CD contains library support and interfaces to all the listed CAE tools, see on page 6.

A month evaluation copy of Exemplar LeonardoSpectrum[®] Synthesis tool is shipped on the CD.

For other CAE tools listed, the libraries and interface are supplied on the IDS CD. For the vendor software and licensing you should go directly to the third-party vendor. Atmel does not supply these systems. Many of the listed tools have evaluation copies available on their web sites.

Simulation Libraries

A month evaluation copy of ModelSim[®] Simulator is shipped on the CD.

There are many other simulators available on the worldwide web. The IDS CD does include fully verified Verilog and VHDL VITAL[®] libraries. These can be compiled and used with any other simulation tool that is Verilog or VHDL compliant. IDS will export a Functional Netlist for pre-layout simulation and a Post-layout Netlist and SDF files for Postlayout Simulation.

The only difference with "Unsupported" tools is that there are not tutorials for these tools, and they are not fully integrated to IDS.

Annual Maintenance Agreements

Annual maintenance agreements are available for each Package Option in the Integrated Development System (IDS). The first year of maintenance is included in the purchase price – renewal is optional. Maintenance agreements give the users direct access to Atmel's experienced technical support staff and cover software upgrades that keep engineers on the leading edge of Atmel's design tools.

System Requirements

PC-based Systems

For a single-user system, IDS requires a personal computer with a 80486 or greater micro-processor equipped as follows; or better.

- 3.5-inch 1.44 MB capacity high-density disk drive (recommended)
- CD-ROM drive
- 200 MB minimum hard drive (both IDS and Viewlogic)
- 48 MB extended memory minimum (64 MB recommended for larger designs using Timing and Mapping)
- Serial interface port
- Parallel interface port
- MS-DOS, release 5.0
- Microsoft Windows 95/98/2000, NT 3.51, or NT 4.0 or higher
- VGA graphics card and display monitor
- · Windows compatible mouse
- A permanent swap space of 64 MB: refer to the Windows documentation for details on its setup
- · Sufficient disk space for file archival and management

Sun-based Systems

For a single-user system, IDS requires a Sun Sparcstation[®] workstation equipped as follows:

- CD-ROM drive (local or network)
- 200 MB (minimum) hard drive 50 MB hard disk space allocated as swap space
- 64 MB RAM
- SUNOS 4.1.2/Solaris 2.4 or higher
- X11R4/Motif 1.1.4, X11R5/Motif 1.2, or OpenWindows 3.x



CAE Tools Supported by IDS

| Vendor | Tool | Version | Туре | Platform | AT40K AT40KAL | AT6000 | Software Ordering Code | Maintenance Ordering Code |
|--|--|--------------|------------|----------|------------------|--------|--|--|
| c · · c · ® | ViewDraw [™] | 1.1+ | Schematic | PC | x | x | | See Viewlogic Table for Ordering |
| eProduct Designer® | Digital Fusion [™] | 1.1+ | Simulation | PC | x | x | On a Minuda air | |
| | ViewDraw [™] | 5.3.1 - 6.0+ | Schematic | Sun | x | x | See Viewlogic Table for Ordering | |
| Viewlogic [®] Powerview [™] | ViewSim [™] | 5.3.1 - 6.0+ | Simulation | Sun | x | x | | |
| | ViewSynthesis [™] | 5.3.1 - 6.0+ | Synthesis | Sun | x | x | - | |
| | Express [®] /Capture [®] | 9.1+ | Schematic | PC | x | x | | ATDM2100PC |
| Orcad [®] | Express [®] /Capture [®] | 9.1+ | Simulation | PC | x | x | ATDS2100PC | |
| | Express [®] /Capture [®] | 9.1+ | Synthesis | PC | x | x | - | |
| Synplicity® | Synplify [™] | 5.1.2+ | Synthesis | PC/Sun | x | | ATDS2100PC | ATDM2100PC |
| т тм | ModelSim [™] | 4.7b+ | Simulation | PC | x | x | ATDS2100PC | ATDM2100PC |
| Model Technology [™] | ModelSim [™] | 5.1+ | Simulation | Sun | x | x | ATDS2100SN | ATDM2100SN |
| | LeonardoSpectrum [™] | 3+ | Synthesis | PC | x | x | ATDS2100PC | ATDM2100PC |
| Exemplar™ | Galileo Extreme [™] | 4.1+ | Synthesis | PC/Sun | x | x | | ATDM2100SN |
| | Leonardo Extreme [™] | 4.1+ | Synthesis | PC/Sun | x | x | ATDS2100SN | |
| | FPGA Express [™] | 2.1+ | Synthesis | PC | x | x | ATDS2100PC | ATDM2100PC |
| | FPGA Compiler [™] | 3.2+ | Synthesis | Sun | x | x | ATDS2100SN | |
| Synopsys® | Design Compiler [™] | 3.2+ | Synthesis | Sun | x | x | | ATDM2100SN |
| | VSS VHDL Simulator™ | 3.2+ | Simulation | Sun | x | х | | |

AT6000 Only

| Vendor | ΤοοΙ | Version | Туре | Platform | AT6000 | Software Ordering Code | Maintenance Ordering Code |
|------------------------|-------------------------------|-----------|---------------|----------|--------|---------------------------|------------------------------|
| | Design Architect [™] | 8.2 - 8.4 | Schematic | Sun | х | | ATDM2100SN |
| | Quicksim [™] | 8.2 - 8.4 | Simulation | Sun | x | | |
| Mentor Idea Station | ENWrite [™] | 8.2 - 8.4 | | Sun | x | ATDS2100SN | |
| | ENRead [™] | 8.2 - 8.4 | | Sun | x | | |
| | SG | 8.2 - 8.4 | Schematic Gen | Sun | x | | |
| | Concept [™] | 1.6 - p4+ | Schematic | Sun | x | _ | ATDM2100SN |
| Cadence 9504 or | Verilog-XL [™] | 2.3.14+ | Simulation | Sun | x | | |
| Higher | SDF Annotator | 2.0.5 | | Sun | x | ATDS2100SN | |
| | SDF Interface | 5.0.5 | | Sun | x | | |

FPGA IDS

Design Hardware

| ATDH40M | AT40K Series FPGA Prototyping Kit (One Daughterboard included - Specify) | | | |
|---|--|--|--|--|
| ATDH40D84 | Daughter Board Attachment - 84PLCC | | | |
| ATDH40D100R Daughter Board Attachment - 100RQFP | | | | |
| ATDH40D100 | IDH40D100 Daughter Board Attachment - 100VQFP | | | |
| ATDH40D144 | Daughter Board Attachment - 144TQFP | | | |
| ATDH40D160 | Daughter Board Attachment - 160PQFP | | | |
| ATDH40D208 | Daughter Board Attachment - 208PQFP | | | |
| ATDH40D240 | Daughter Board Attachment - 240PQFP | | | |
| ATDH2000 | AT6000 Series FPGA Demonstration Board | | | |
| ATDH2080 | AT6000 Series FPGA Prototyping Kit | | | |
| ATDH2200E | AT17 Series Configurator Programming Kit (Enhanced) | | | |
| ATDH2221 | 20-pin SOIC Adapter for ATDH2200 | | | |
| ATDH2222 | 20-pin PLCC Adapter for ATDH2200 | | | |
| ATDH2223 | 8-lead SOIC Adapter for ATDH2200 | | | |
| ATDH2224 | 44-lead TQFP Adapter for ATDH2200 | | | |
| ATDH2226 | 32-lead TQFP Adapter for ATDH2200 | | | |
| ATDH2227 | 44-lead PLCC Adapter for ATDH2200 | | | |
| ATDH2225 | Standalone In-System Programming Cable | | | |





Atmel Headquarters

Corporate Headquarters 2325 Orchard Parkway San Jose, CA 95131 TEL (408) 441-0311 FAX (408) 487-2600

Europe

Atmel SarL Route des Arsenaux 41 Casa Postale 80 CH-1705 Fribourg Switzerland TEL (41) 26-426-5555 FAX (41) 26-426-5500

Asia

Atmel Asia, Ltd. Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimhatsui East Kowloon Hong Kong TEL (852) 2721-9778 FAX (852) 2722-1369

Japan

Átmel Japan K.K. 9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan TEL (81) 3-3523-3551 FAX (81) 3-3523-7581

Atmel FPGA Hotline 1-(408) 436-4119

Atmel FPGA e-mail fpga@atmel.com

FAQ

Accessible on web site

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Atmel Operations

Atmel Colorado Springs 1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 TEL (719) 576-3300 FAX (719) 540-1759

Atmel Rousset Zone Industrielle 13106 Rousset Cedex France TEL (33) 4-4253-6000 FAX (33) 4-4253-6001

Atmel Smart Card ICs Scottish Enterprise Technology Park East Kilbride, Scotland G75 0QR TEL (44) 1355-357-000 FAX (44) 1355-242-743

Atmel Grenoble

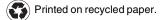
Avenue de Rochepleine BP 123 38521 Saint-Egreve Cedex France TEL (33) 4-7658-3000 FAX (33) 4-7658-3480

> *Fax-on-Demand* North America: 1-(800) 292-8635 International: 1-(408) 441-0732

e-mail literature@atmel.com

Web Site http://www.atmel.com

BBS 1-(408) 436-4309





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Microchip: ATDH2224