ATA5428

UHF ASK/FSK Transceiver

DATASHEET

Features

- Multi channel half-duplex transceiver with approximately ±2.5MHz programmable tuning range
- High FSK sensitivity: –106dBm at 20Kbit/s/–109.5dBm at 2.4Kbit/s (433.92MHz)
- High ASK sensitivity: –112.5dBm at 10Kbit/s/–116.5dBm at 2.4Kbit/s (433.92MHz)
- Low supply current: 10.5mA in RX and TX Mode (3V/TX with 5dBm)
- Data Rate: 1 to 20Kbit/s Manchester FSK, 1 to 10Kbit/s Manchester ASK
- ASK/FSK receiver uses a low-IF architecture with high selectivity, blocking, and low intermodulation (typical blocking 55dB at ±750kHz/61dB at ±1.5MHz and 70dB at ±10MHz, system I1dBCP = –30dBm/system IIP3 = –20dBm)
- 226kHz/237kHz IF frequency with 30dB image rejection and 170kHz usable IF bandwidth
- Transmitter uses closed loop fractional-N synthesizer for FSK modulation with a high PLL bandwidth and an excellent isolation between PLL/VCO and PA
- Tolerances of XTAL compensated by fractional-N synthesizer with 800Hz RF resolution
- Integrated RX/TX-switch, single-ended RF input and output
- RSSI (Received Signal Strength Indicator)
- Communication to microcontroller with SPI interface working at max.500kBit/s
- Configurable self polling and RX/TX protocol handling with FIFO-RAM buffering of received and transmitted data
- Five push button inputs and one wake-up input are active in power-down mode
- integrated XTAL capacitors
- PA efficiency: up to 38% (433.92MHz/10dBm/3V)
- Low in-band sensitivity change of typically ±1.8dB within ±58kHz center frequency change in the complete temperature and supply voltage range
- Supply voltage switch, supply voltage regulator, reset generation, clock/interrupt generation and low battery indicator for microcontroller

- Fully integrated PLL with low phase noise VCO, PLL loop filter and full support of multi-channel operation with arbitrary channel distance due to fractional-N synthesizer
- Sophisticated threshold control and quasi-peak detector circuit in the data slicer
- Power management via different operation modes
- 433.92MHz and 868.3MHz without external VCO and PLL components
- Inductive supply with voltage regulator if battery is empty (AUX mode)
- Efficient XTO start-up circuit (> –1.5kΩ worst case real start-up impedance)
- Changing of modulation type ASK/FSK and data rate without component changes
- Minimal external circuitry requirements for complete system solution
- Adjustable output power: 0 to 10dBm adjusted and stabilized with external resistor
- ESD protection at all pins (1.5kV HBM, 200V MM, 1kV FCDM)
- Supply voltage range: 2.4V to 3.6V or 4.4V to 6.6V
- Temperature range: –40°C to +85°C
- Small 7 × 7mm QFN48 package

Applications

- Consumer industrial segment
- Access control systems
- Remote control systems
- Alarm and telemetry systems
- Energy metering
- Home automation

Benefits

- Low system cost due to very high system integration level
- Only one crystal needed in system
- Less demanding specification for the microcontroller due to handling of power-down mode, delivering of clock, reset, low battery indication and complete handling of receive/transmit protocol and polling
- Single-ended design with high isolation of PLL/VCO from PA and the power supply allows a loop antenna in the remote control unit to surround the whole application

1. General Description

The Atmel® ATA5428 is a highly integrated UHF ASK/FSK multi-channel half-duplex transceiver with low power consumption supplied in a small 7 x 7mm QFN48 package. The receive part is built as a fully integrated low-IF receiver, whereas direct PLL modulation with the fractional-N synthesizer is used for FSK transmission and switching of the power amplifier for ASK transmission.

The device supports data rates of 1Kbit/s to 20Kbit/s (FSK) and 1Kbit/s to 10Kbit/s (ASK) in Manchester, Bi-phase and other codes in transparent mode. The ATA5428 can be used in the 431.5MHz to 436.5MHz and in the 862MHz to 872MHz bands. The very high system integration level results in a small number of external components needed.

Due to its blocking and selectivity performance, together with the additional 15dB to 20dB loss and the narrow bandwidth of a typical loop antenna in a remote control unit, a bulky blocking SAW is not needed in the remote control unit. Additionally, the building blocks needed for a typical remote control and access control system on both sides (the base and the mobile stations) are fully integrated.

Its digital control logic with self-polling and protocol generation enables a fast challenge-response system without using a high-performance microcontroller. Therefore, the ATA5428 contains a FIFO buffer RAM and can compose and receive the physical messages themselves. This provides more time for the microcontroller to carry out other functions such as calculating crypto algorithms, composing the logical messages, and controlling other devices. Therefore, a standard 4-/8-bit microcontroller without special periphery and clocked with the CLK output of about 4.5MHz is sufficient to control the communication link. This is especially valid for passive entry and access control systems, where within less than 100ms several challenge-response communications with arbitration of the communication partner have to be handled.

It is hence possible to design bi-directional remote control and access control systems with a fast challenge-response crypto function, with the same PCB board size and with the same current consumption as uni-directional remote control systems.

Figure 1-1. System Block Diagram

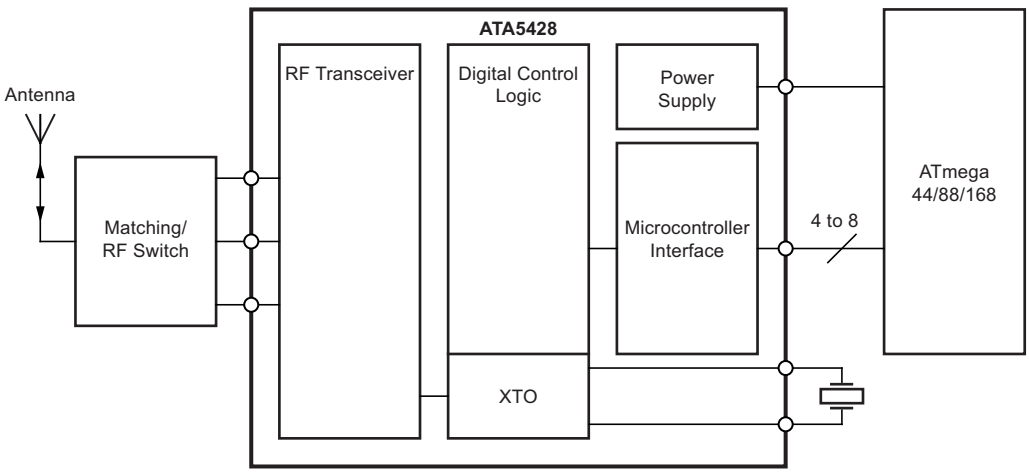


Figure 1-2. Pinning QFN48

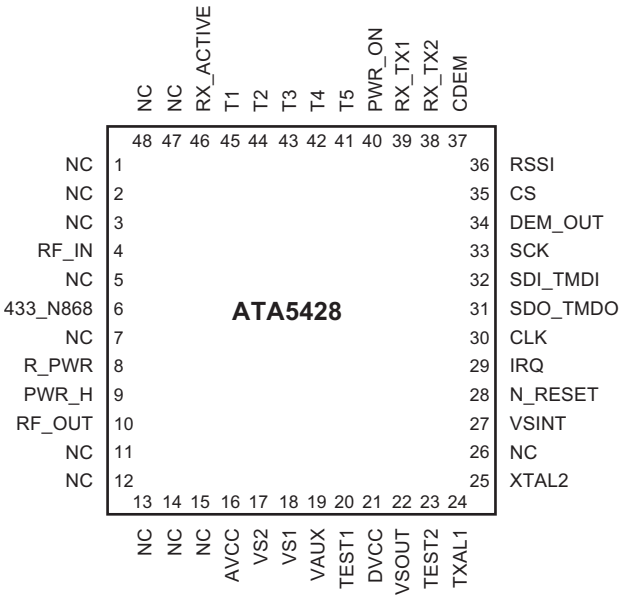


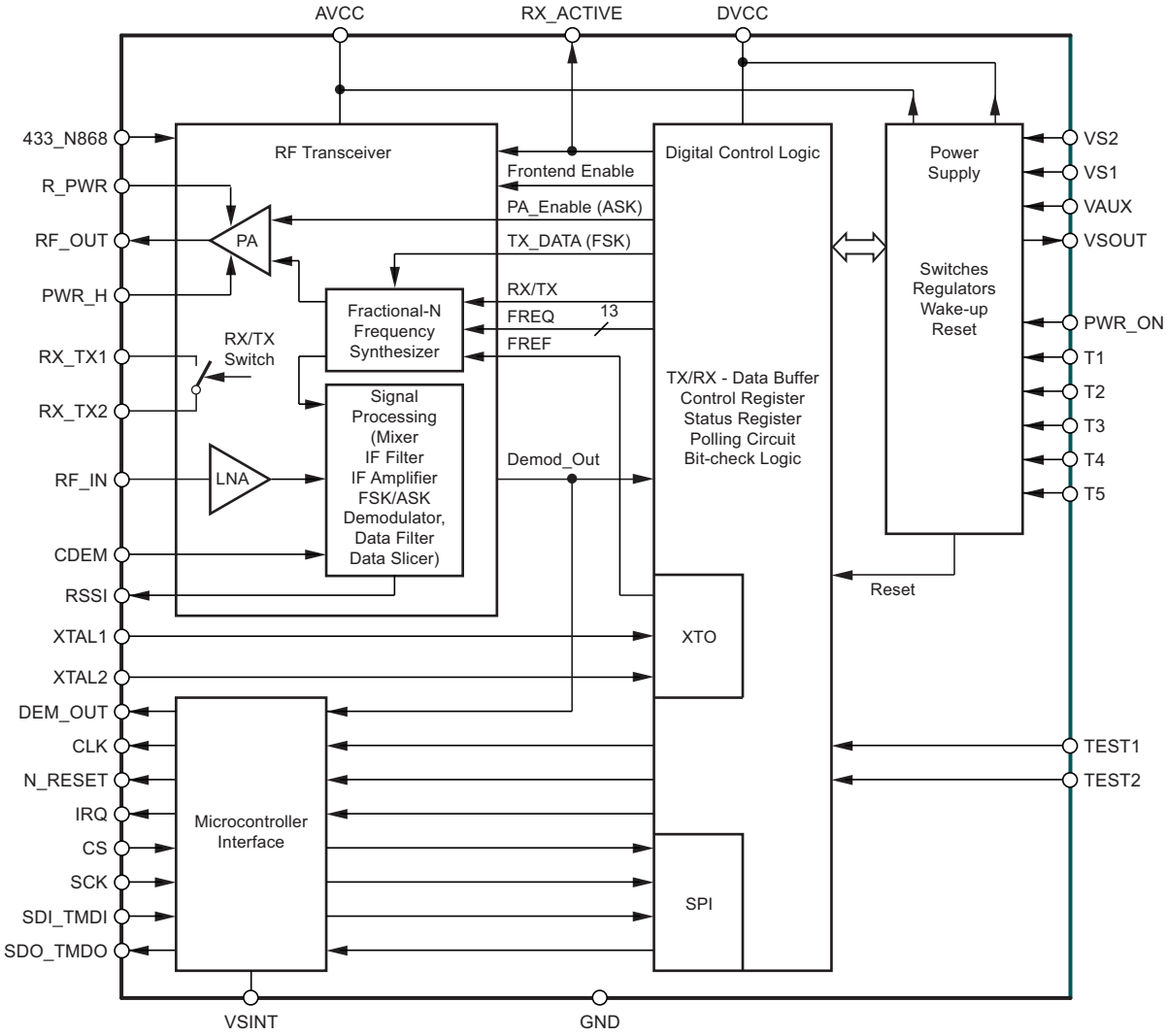
Table 1-1. Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	NC	Not connected
3	NC	Not connected
4	RF_IN	RF input
5	NC	Not connected
6	433_N868	Selects RF input/output frequency range
7	NC	Not connected
8	R_PWR	Resistor to adjust output power
9	PWR_H	Pin to select output power
10	RF_OUT	RF output
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	AVCC	Blocking of the analog voltage supply
17	VS2	Power supply input for voltage range 4.4V to 6.6V
18	VS1	Power supply input for voltage range 2.4V to 3.6V
19	VAUX	Auxiliary supply voltage input
20	TEST1	Test input, at GND during operation
21	DVCC	Blocking of the digital voltage supply
22	VSOUT	Output voltage power supply for external devices
23	TEST2	Test input, at GND during operation
24	XTAL1	Reference crystal

Table 1-1. Pin Description (Continued)

Pin	Symbol	Function
25	XTAL2	Reference crystal
26	NC	Not connected
27	VSINT	Microcontroller interface supply voltage
28	N_RESET	Output pin to reset a connected microcontroller
29	IRQ	Interrupt request
30	CLK	Clock output to connect a microcontroller
31	SDO_TMDO	Serial data out/transparent mode data out
32	SDI_TMDI	Serial data in/transparent mode data in
33	SCK	Serial clock
34	DEM_OUT	Demodulator open drain output signal
35	CS	Chip select for serial interface
36	RSSI	Output of the RSSI amplifier
37	CDEM	Capacitor to adjust the lower cut-off frequency data filter
38	RX_TX2	GND pin to decouple LNA in TX mode
39	RX_TX1	Switch pin to decouple LNA in TX mode
40	PWR_ON	Input to switch on the system (active high)
41	T5	Key input 5 (can also be used to switch on the system (active low))
42	T4	Key input 4 (can also be used to switch on the system (active low))
43	T3	Key input 3 (can also be used to switch on the system (active low))
44	T2	Key input 2 (can also be used to switch on the system (active low))
45	T1	Key input 1 (can also be used to switch on the system (active low))
46	RX_ACTIVE	Indicates RX operation mode
47	NC	Not connected
48	NC	Not connected
	GND	Ground/backplane

Figure 1-3. Block Diagram

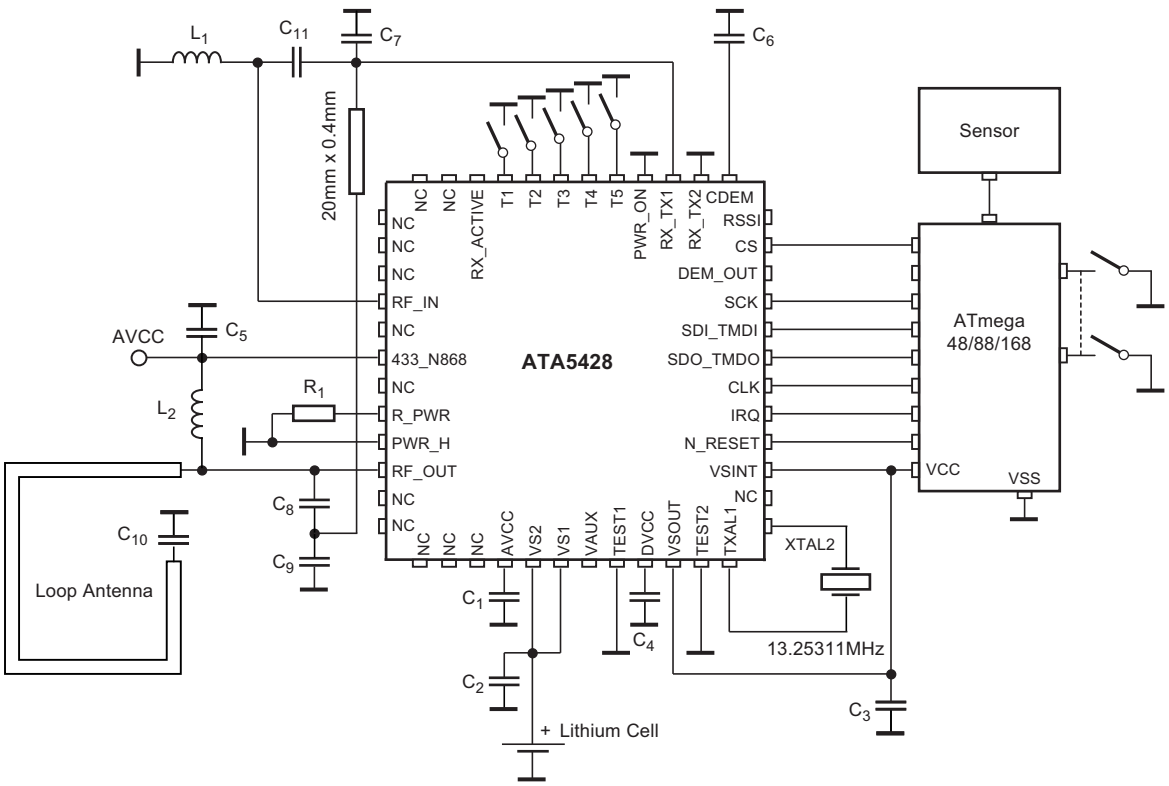


2. Application Circuits

2.1 Typical Remote Control Unit Application with 1 Li Battery (3V)

Figure 2-1 shows a typical 433.92MHz Remote Control Unit application with one battery. The external components are 11 capacitors, 1 resistor, 2 inductors and a crystal. C_1 to C_4 are 68nF voltage supply blocking capacitors. C_5 is a 10nF supply blocking capacitor. C_6 is a 15nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L1 is a matching inductor of about 5.6nH to 56nH. L_2 is a feed inductor of about 120nH. A load capacitor of 9pF for the crystal is integrated. R_1 is typically 22kΩ and sets the output power to about 5.5dBm. The loop antenna's quality factor is somewhat reduced by this application due to the quality factor of L_2 and the RX/TX switch. On the other hand, this lower quality factor is necessary to have a robust design with a bandwidth that is broad enough for production tolerances. Due to the single-ended and ground-referenced design, the loop antenna can be a free-form wire around the application as it is usually employed in remote control uni-directional systems. The ATA5428 provides sufficient isolation and robust pulling behavior of internal circuits from the supply voltage as well as an integrated VCO inductor to allow this. Since the efficiency of a loop antenna is proportional to the square of the surrounded area it is beneficial to have a large loop around the application board with a lower quality factor in order to relax the tolerance specification of the RF components and to get a high antenna efficiency in spite of their lower quality factor.

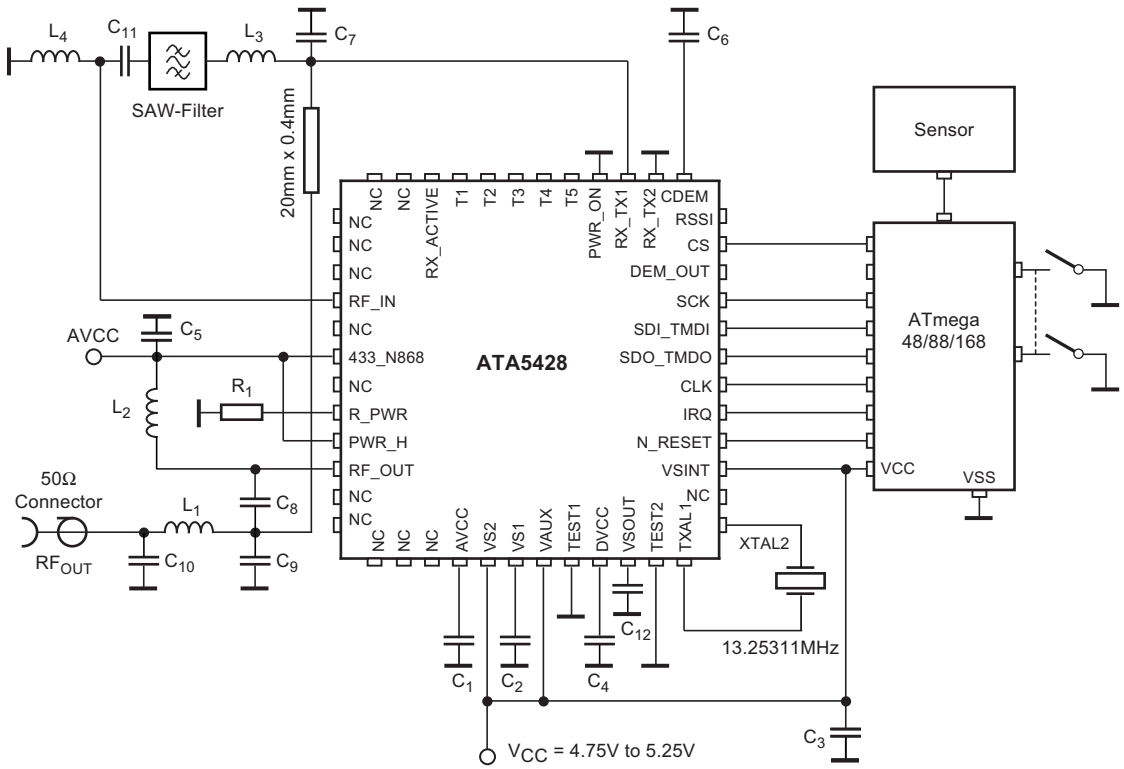
Figure 2-1. Typical Remote Control Unit Application, 433.92MHz, 1 Li Battery (3V)



2.2 Typical Base-station Application (5V)

Figure 2.2 shows a typical 433.92MHz V_{CC} = 4.75V to 5.25V Base-station Application (5V). The external components are 12 capacitors, 1 resistor, 4 inductors, a SAW filter, and a crystal. C_1 and C_3 to C_4 are 68nF voltage supply blocking capacitors. C_2 and C_{12} are 2.2µF supply blocking capacitors for the internal voltage regulators. C_5 is a 10nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L_2 to L_4 are matching inductors of about 5.6nH to 56nH. A load capacitor for the crystal of 9pF is integrated. R_1 is typically 22kΩ and sets the output power at RF_OUT to about 10dBm. Since a quarter wave or PCB antenna, which has high efficiency and wide band operation, is typically used here, it is recommended to use a SAW filter to achieve high sensitivity in case of powerful out-of-band blockers. L_1, C_9 and C_{10} together form a low-pass filter, which is needed to filter out the harmonics in the transmitted signal to meet regulations. An internally regulated voltage at pin VSOUT can be used in case the microcontroller only supports 3.3V operation, a blocking capacitor with a value of C_{12} = 2.2µF has to be connected to VSOUT in any case.

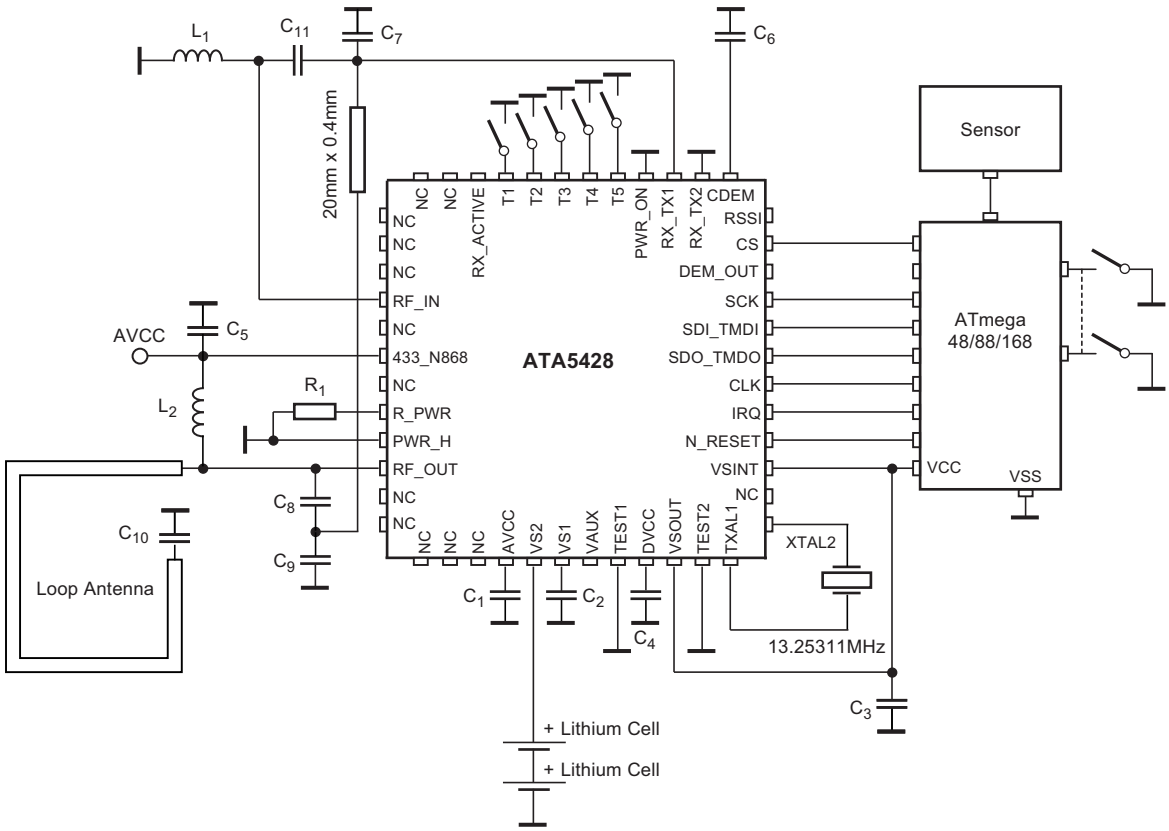
Figure 2-2. Typical Base-station Application (5V), 433.92MHz



2.3 Typical Remote Control Unit Application, 2 Li Batteries (6V)

Figure 2-3 shows a typical 433.92Hz 2 Li battery Remote Control Unit application. The external components are 11 capacitors, 1 resistor, 2 inductors and a crystal. C_1 and C_4 are 68nF voltage supply blocking capacitors. C_2 and C_3 are 2.2µF supply blocking capacitors for the internal voltage regulators. C_5 is a 10nF supply blocking capacitor. C_6 is a 15nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L_1 is a matching inductor of about 5.6nH to 56nH. L_2 is a feed inductor of about 120nH. A load capacitor for the crystal of 9pF is integrated. R_1 is typically 22kΩ and sets the output power to about 5.5dBm.

Figure 2-3. Typical Remote Control Unit Application, 433.92MHz, 2 Li Batteries (6V)



3. RF Transceiver

As seen in Figure 1-3 on page 6, the RF transceiver consists of an LNA (Low-noise Amplifier), PA (Power Amplifier), RX/TX switch, fractional-N frequency synthesizer and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter, and data slicer.

In receive mode the LNA pre-amplifies the received signal which is converted down to 226kHz (ATA5428), filtered and amplified before it is fed into an FSK/ASK demodulator, data filter, and data slicer. The RSSI (Received Signal Strength Indicator) signal and the raw digital output signal of the demodulator are available at the pins RSSI and DEM_OUT. The demodulated data signal Demod_Out is fed to the digital control logic where it is evaluated and buffered as described in section "Digital Control Logic" on page 30.

In transmit mode, the fractional-N frequency synthesizer generates the TX frequency which is fed to the PA. In ASK mode the PA is modulated by the signal PA_Enable. In FSK mode the PA is enabled and the signal TX_DATA (FSK) modulates the fractional-N frequency synthesizer. The frequency deviation is digitally controlled and internally fixed to about ±16kHz (see Table 4-1 on page 23 for exact values). The transmit data can also be buffered as described in section "Digital Control Logic" on page 30. A lock detector within the synthesizer ensures that the transmission will start only if the synthesizer is locked.

The RX/TX switch can be used to combine the LNA input and the PA output to a single antenna with a minimum of losses.

Transparent modes without buffering of RX and TX data are also available to allow protocols and coding schemes other than the internally supported Manchester encoding.

3.1 Low-IF Receiver

The receive path consists of a fully integrated low-IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage and supply current specification needed to manufacture, for example, an automotive remote control unit without the use of SAW blocking filter (see Figure 2-1 on page 7). In a Base-station Application (5V) the receiver can be used with an additional blocking SAW front-end filter as shown in Figure 2.2 on page 8.

At 433.92MHz the receiver has a typical system noise figure of 7.0dB, a system I1dBCP of -30dBm and a system IIP3 of –20dBm. There is no AGC or switching of the LNA needed; thus, a better blocking performance is achieved. This receiver uses an IF (Intermediate Frequency) of 226kHz, the typical image rejection is 30dB and the typical 3dB IF filter bandwidth is 185kHz (f_{IF} = 226kHz ±92.5kHz, f_{lo_IF} = 133.5kHz and f_{hi_IF} = 318.5kHz). The demodulator needs a signal to Gaussian noise ratio of 8dB for 20Kbit/s Manchester with ±16kHz frequency deviation in FSK mode; thus, the resulting sensitivity at 433.92MHz is typically –106dBm at 20Kbit/s Manchester.

Due to the low phase noise and spurious emissions of the synthesizer in receive mode(1) together with the eighth order integrated IF filter, the receiver has a better selectivity and blocking performance than more complex double superhet receivers but without external components and without numerous spurious receiving frequencies.

A low-IF architecture is also less sensitive to second-order intermodulation (IIP2) than direct conversion receivers, where every pulse or AM-modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second-order non-linearities.

Note: 1. –120dBC/Hz at ±1MHz and –75dBC at ±FREF at 433.92MHz

3.2 Input Matching at RF_IN

The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in the Table 3-1. The highest sensitivity is achieved with power matching of these impedances to the source impedance of 50Ω.

Table 3-1. Measured Input Impedances of the RF_IN Pin

f_{RF}/MHz	Z(RF_IN)	R_p//C_p
433.92	(32-j169)Ω	925Ω//2.1pF
868.3	(21-j78)Ω	311Ω//2.2pF

The matching of the LNA Input to 50Ω was done with the circuit shown in Figure 3-1 and with the values given in Table 3-2 on page 11. The reflection coefficients were always ≤ 10dB. Note that value changes of C_1 and L_1 may be necessary to compensate for individual board layouts. The measured typical FSK and ASK Manchester code sensitivities with a Bit Error Rate (BER) of 10^{-3} are shown in Table 3-3 on page 11 and Table 3-4 on page 11. These measurements were done with inductors having a quality factor according to Table 3-2 on page 11, resulting in estimated matching losses of 0.7dB at 433.92MHz, 0.7dB at 868.3MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with $R_{loss} = 2 \times \pi \times f \times L \times Q_L$ and the matching loss with $10 \log(1 + R_p/R_{loss})$.

With an ideal inductor, for example, the sensitivity at 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester can be improved from –106dBm to –106.7dBm. The sensitivity depends on the control logic which examines the incoming data stream. The examination limits must be programmed in control registers 5 and 6. The measurements in Table 3-3 on page 11 and Table 3-4 on page 11 are based on the values of registers 5 and 6 according to Table 9-3 on page 53.

Figure 3-1. Input Matching to 50Ω

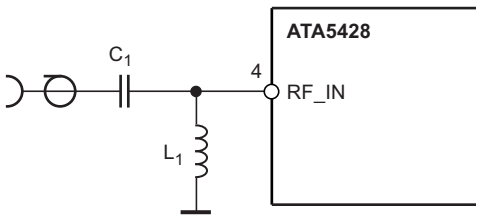


Table 3-2. Input Matching to 50Ω

f_{RF}/MHz	C_1/pF	L_1/nH	Q_{L1}
433.92	1.8	27	70
868.3	1.2	6.8	50

Table 3-3. Measured Sensitivity FSK, ±16kHz, Manchester, dBm, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.4Kbit/s	BR_Range_1 5.0Kbit/s	BR_Range_2 10Kbit/s	BR_Range_3 20Kbit/s
433.92MHz	–109.0dBm	–109.5dBm	–108.0dBm	–107.0dBm	–106.0dBm
868.3MHz	–106.0dBm	–106.5dBm	–105.5dBm	–104.0dBm	–103.5dBm

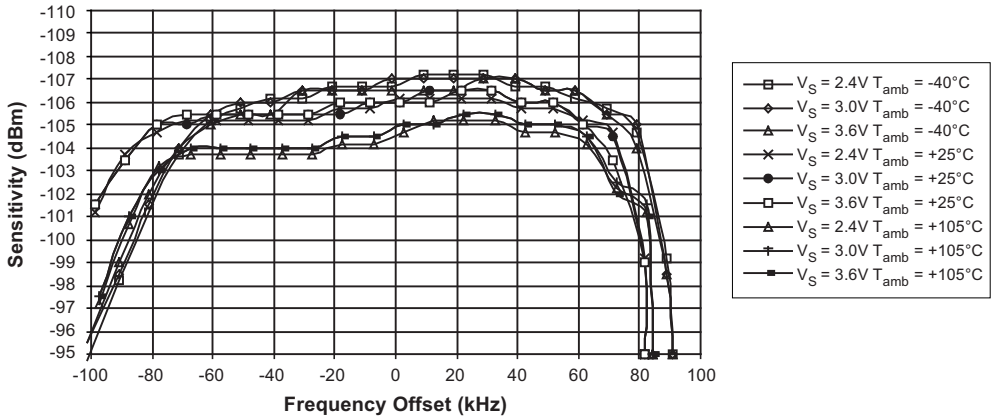
Table 3-4. Measured Sensitivity 100% ASK, Manchester, dBm, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.4Kbit/s	BR_Range_1 5.0Kbit/s	BR_Range_2 10Kbit/s
433.92MHz	–116.0dBm	–116.5dBm	–114.0dBm	–112.5dBm
868.3MHz	–112.5dBm	–113.0dBm	–111.5dBm	–109.5dBm

3.3 Sensitivity versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure and IF filter bandwidth of the receiver. Figure 3-2 shows the typical sensitivity at 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester versus the frequency offset between transmitter and receiver with T_{amb} = –40°C, +25°C and +105°C and supply voltage VS1 = VS2 = 2.4V, 3.0V and 3.6V.

Figure 3-2. Measured Sensitivity 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester versus Frequency Offset, Temperature and Supply Voltage



As can be seen in Figure 3-2 on page 12 the supply voltage has almost no influence. The temperature has an influence of about +1.5/–0.7dB, and a frequency offset of ±65kHz also influences by about ±1dB. All these influences, combined with the sensitivity of a typical IC, are then within a range of –103.7dBm and –107.3dBm over temperature, supply voltage and frequency offset which is –105.5dBm ±1.8dB. The integrated IF filter has an additional production tolerance of only ±7kHz, hence, a frequency offset between the receiver and the transmitter of ±58kHz can be accepted for XTAL and XTO tolerances.

This small sensitivity spread over supply voltage, frequency offset and temperature is very unusual in such a receiver. It is achieved by an internal, very fast and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly; if, however, the input frequency makes a larger step (for example, if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to IDLE mode and then again to RX mode. For that purpose, an automatic mode is also available. This automatic mode switches to IDLE mode and back into RX mode every time a bit error occurs (see Section 7. on page 30).

3.4 Frequency Accuracy of the Crystals

The XTO is an amplitude regulated Pierce oscillator with integrated load capacitors. The initial tolerances (due to the frequency tolerance of the XTAL, the integrated capacitors on XTAL1, XTAL2 and the XTO's initial transconductance gm) can be compensated to a value within ±0.5ppm by measuring the CLK output frequency and programming the control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33). The XTO then has a remaining influence of less than ±2ppm over temperature and supply voltage due to the band gap controlled gm of the XTO.

The needed frequency stability of the used crystals over temperature and aging is hence

±58kHz/433.92MHz – 2 × ±2.5ppm = ±128.6ppm for 433.92Mz,
±58kHz/868.3MHz – 2 × ±2.5ppm = ±61.8ppm for 868.3MHz.

Thus, the used crystals in receiver and transmitter each need to be better than ±64.3ppm for 433.92MHz, ±30.9ppm for 868.3MHz. In access control systems it may be advantageous to have a more tight tolerance at the Base-station in order to relax the requirement for the remote control unit.

3.5 RX Supply Current versus Temperature and Supply Voltage

Table 3-5 shows the typical supply current at 433.92MHz of the transceiver in RX mode versus supply voltage and temperature with VS = VS1 = VS2. As can be seen, the supply current at 2.4V and –40°C is less than the typical supply current; this is useful because this is also the operation point where a lithium cell has the worst performance. The typical supply current at 868.3MHz in RX mode is about the same as for 433.92MHz.

Table 3-5. Measured 433.92 MHz Receive Supply Current in FSK Mode

VS = VS1 = VS2	2.4V	3.0V	3.6V
T_{amb} = –40°C	8.4mA	8.8mA	9.2mA
T_{amb} = 25°C	9.9mA	10.3mA	10.8mA
T_{amb} = 85°C	10.9mA	11.3mA	11.8mA

3.6 Blocking, Selectivity

As can be seen in Figure 3-3 and Figure 3-4 on page 13, the receiver can receive signals 3dB higher than the sensitivity level in the presence of very large blockers of –47dBm/–34dBm with small frequency offsets of ±1/±10MHz.

Figure 3-3 shows narrow band blocking and Figure 3-4 wide band blocking characteristics. The measurements were done with a signal of 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester, and with a level of –106dBm + 3dB = –103dBm which is 3dB above the sensitivity level. The figures show how much larger than –103dBm a continuous wave signal can be before the BER is higher than 10^{-3}. The measurements were done at the 50Ω input according to Figure 3-1 on page 11. At 1MHz, for example, the blocker can be 56dB higher than –103dBm which is -103dBm + 56dB = –47dBm. These values, together with the good intermodulation performance, avoid the need for a SAW filter in the remote control unit application.

Figure 3-3. Narrow Band 3dB Blocking Characteristic at 433.92MHz

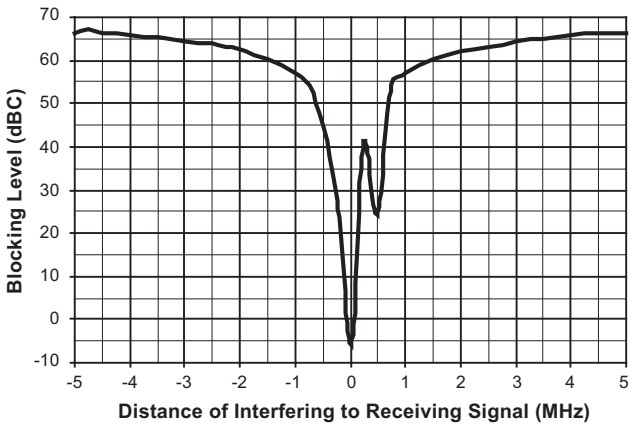


Figure 3-4. Wide Band 3dB Blocking Characteristic at 433.92MHz

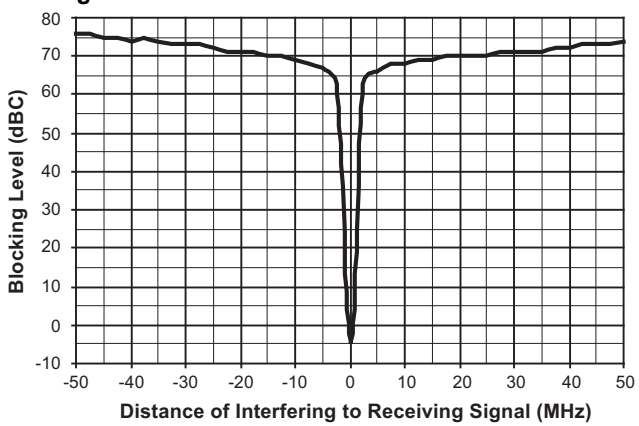


Figure 3-5 on page 14 shows the blocking measurement close to the received frequency to illustrate the selectivity and image rejection. This measurement was done 6dB above the sensitivity level with a useful signal of 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester with a level of –106dBm + 6dB = –100dBm. The figure shows to which extent a continuous wave signal can surpass –100dBm until the BER is higher than 10^{-3}. For example, at 1MHz the blocker can then be 59dB higher than –100dBm which is –100dBm + 59dB = –41dBm.

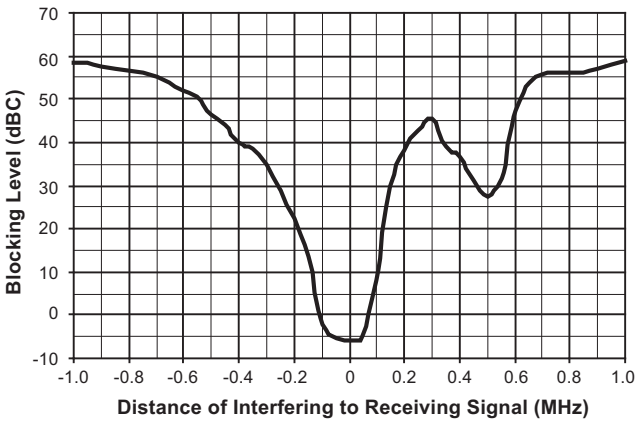
Table 3-6 on page 14 shows the blocking performance measured relative to –100dBm for some other frequencies. Note that sometimes the blocking is measured relative to the sensitivity level (dBS) instead of the carrier (dBC).

Table 3-6. Blocking 6dB Above Sensitivity Level with BER < 10^{-3}

Frequency Offset	Blocker Level	Blocking
+0.75MHz	–45dBm	55dBC/61dBS
–0.75MHz	–45dBm	55dBC/61dBS
+1.5MHz	–38dBm	62dBC/68dBS
–1.5MHz	–38dBm	62dBC/68dBS
+10MHz	–30dBm	70dBC/76dBS
–10MHz	–30dBm	70dBC/76dBS

The ATA5428 can also receive FSK and ASK modulated signals if they are much higher than the I1dBCP. It can typically receive useful signals at 10dBm. This is often referred to as the nonlinear dynamic range which is the maximum to minimum receiving signal and is 116dB for 20Kbit/s Manchester. This value is useful if two transceivers have to communicate and are very close to each other.

Figure 3-5. Close In 6dB Blocking Characteristic and Image Response at 433.92MHz



This high blocking performance even makes it possible for some applications using quarter wave whip antennas to use a simple LC band-pass filter instead of a SAW filter in the receiver.

When designing such an LC filter take into account that the 3dB blocking at 433.92MHz/2 = 216.96MHz is 43dBC and at 433.92MHz/3 = 144.64MHz is 48dBC and at 2 × (433.92MHz + 226kHz) + –226kHz = 868.066MHz/868.518MHz is 56dBC.

And especially that at 3 × (433.92MHz + 226kHz) + 226kHz = 1302.664MHz the receiver has its second LO harmonic receiving frequency with only 12dBC blocking.

3.7 In-band Disturbers, Data Filter, Quasi-peak Detector, Data Slicer

If a disturbing signal falls into the received band or a blocker is not continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. The demodulator, data filter and data slicer are important, in that case.

The data filter of the ATA5428 implies a quasi-peak detector. This results in a good suppression of the above mentioned disturbers and exhibits a good carrier to Gaussian noise performance. The required useful signal to disturbing signal ratio to be received with a BER of 10^{-3} is less than 12dB in ASK mode and less than 3dB (BR_Range_0 to BR_Range_2)/6dB (BR_Range_3) in FSK mode.

Due to the many different waveforms possible these numbers are measured for signal as well as for disturbers with peak amplitude values. Note that these values are worst case values and are valid for any type of modulation and modulating frequency of the disturbing signal as well as the receiving signal. For many combinations, lower carrier to disturbing signal ratios are needed.

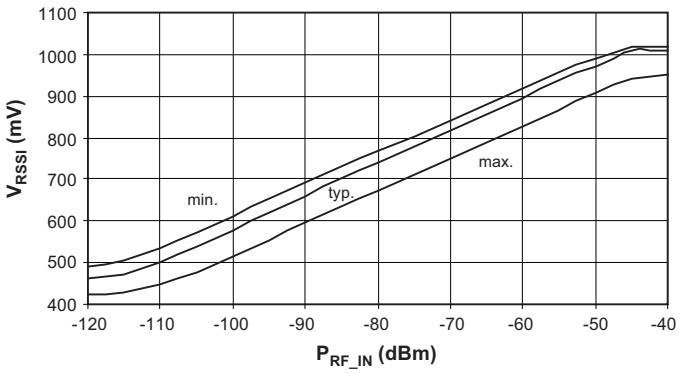
3.8 DEM_OUT Output

The internal raw output signal of the demodulator Demod_Out is available at pin DEM_OUT. DEM_OUT is an open drain output and must be connected to a pull-up resistor if it is used (typically 100kΩ) otherwise no signal is present at that pin.

3.9 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 70dB, the input power range P(RF_{IN}) is –115dBm to –45dBm and the gain is 8mV/dB. Figure 3-6 shows the RSSI characteristic of a typical device at 433.92MHz with VS1 = VS2 = 2.4V to 3.6V and T_{amb} = –40°C to +85°C with a matched input according to Table 3-2 on page 11 and Figure 3-1 on page 11. At 868.3MHz about 2.7dB more signal level is needed for the same RSSI results.

Figure 3-6. Typical RSSI Characteristic versus Temperature and Supply Voltage



3.10 Frequency Synthesizer

The synthesizer is a fully integrated fractional-N design with internal loop filters for receive and transmit mode. The XTO frequency f_{XTO} is the reference frequency FREF for the synthesizer. The bits FR0 to FR12 in control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33) are used to adjust the deviation of f_{XTO}. In transmit mode, at 433.92MHz, the carrier has a phase noise of –111dBC/Hz at 1MHz and spurious emissions at FREF of –66dBC with a high PLL loop bandwidth allowing the direct modulation of the carrier with 20Kbit/s Manchester data. Due to the closed loop modulation any spurious emissions caused by this modulation are effectively filtered out as can be seen in Figure 3-9 on page 17. In RX mode the synthesizer has a phase noise of –120dBC/Hz at 1MHz and spurious emissions of –75dBC.

The initial tolerances of the crystal oscillator due to crystal tolerances, internal capacitor tolerances and the parasitics of the board have to be compensated at manufacturing setup with control registers 2 and 3 as can be seen in Table 4-1 on page 23. The other control words for the synthesizer needed for ASK, FSK and receive/transmit switching are calculated internally. The RF (Radio Frequency) resolution is equal to the XTO frequency divided by 16384 which is 808.9Hz at 433.92MHz, 818.6Hz at 868.3MHz.

For the multi-channel system the frequency control word FREQ in control registers 2 and 3 can be programmed in the range of 1000 to 6900, this is equivalent to a programmable tuning range of ±2.5MHz hence every frequency within the 433MHz, 868MHz ISM bands can be programmed as receive and as transmit frequency, and the position of channels within these ISM bands can be chosen arbitrarily (see Table 4-1 on page 23).

Care must be taken as to the harmonics of the CLK output signal as well as to the harmonics produced by a microprocessor clocked with it, since these harmonics can disturb the reception of signals. In a single-channel system, using FREQ = 3803 to 4053 ensures that harmonics of this signal do not disturb the receive mode.

3.11 FSK/ASK Transmission

Due to the fast modulation capability of the synthesizer and the high resolution, the carrier can be internally FSK modulated, which simplifies the application of the transceiver. The deviation of the transmitted signal is ±20 digital frequency steps of the synthesizer which is equal to ±16.17kHz for 433.92MHz, ±16.37kHz for 868.3MHz.

Due to closed loop modulation with PLL filtering the modulated spectrum is very clean, meeting ETSI and CEPT regulations when using a simple LC filter for the power amplifier harmonics as it is shown in Figure 2.2 on page 8. In ASK mode the frequency is internally connected to the center of the FSK transmission and the power amplifier is switched on and off to perform the modulation. Figure 3-7 to Figure 3-9 on page 17 show the spectrum of the FSK modulation with pseudo-random data with 20Kbit/s/±16.17kHz/Manchester and 5dBm output power.

Figure 3-7. FSK-modulated TX Spectrum (433.92MHz/20Kbit/s/±16.17kHz/Manchester Code)

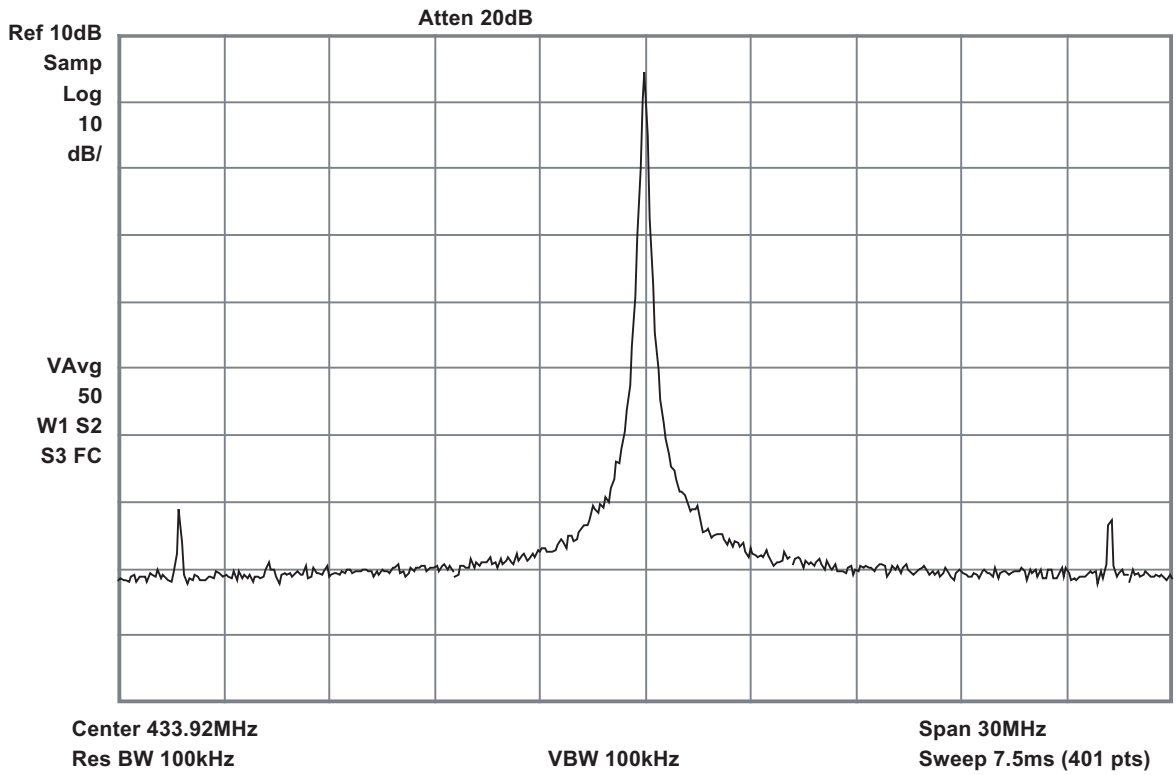


Figure 3-8. Unmodulated TX Spectrum 433.92MHz – 16.17kHz (f_{FSK_L})

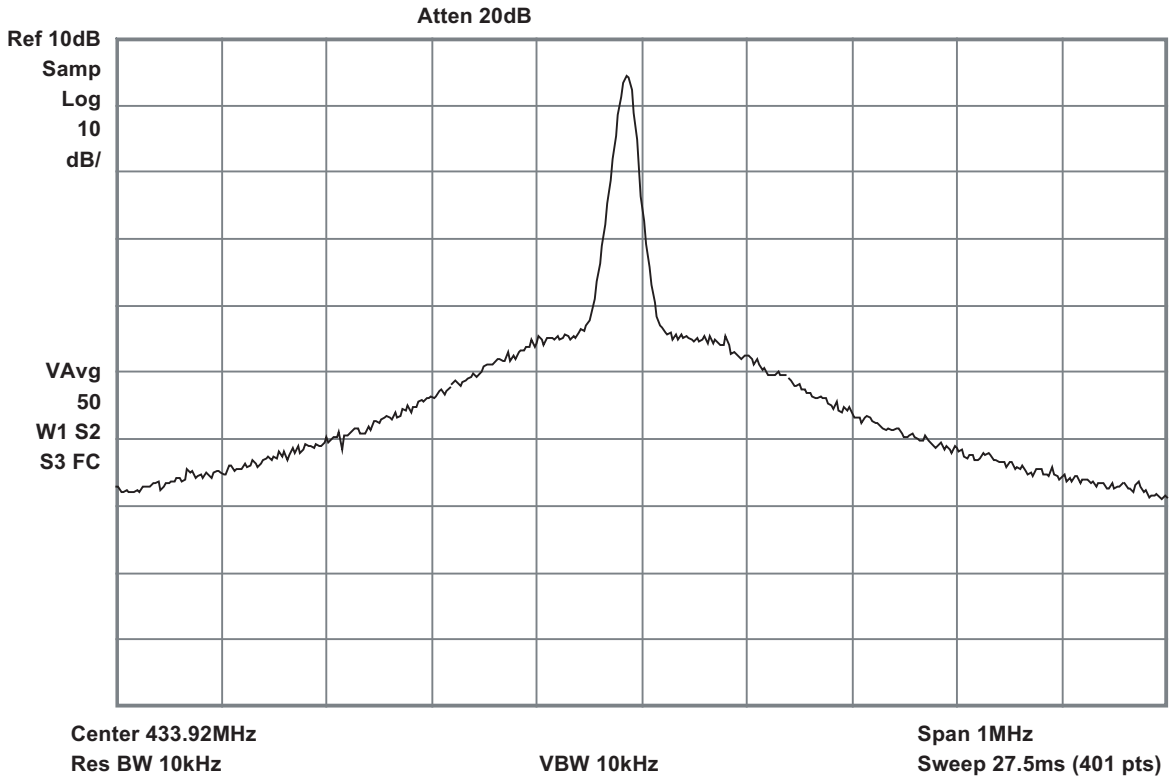
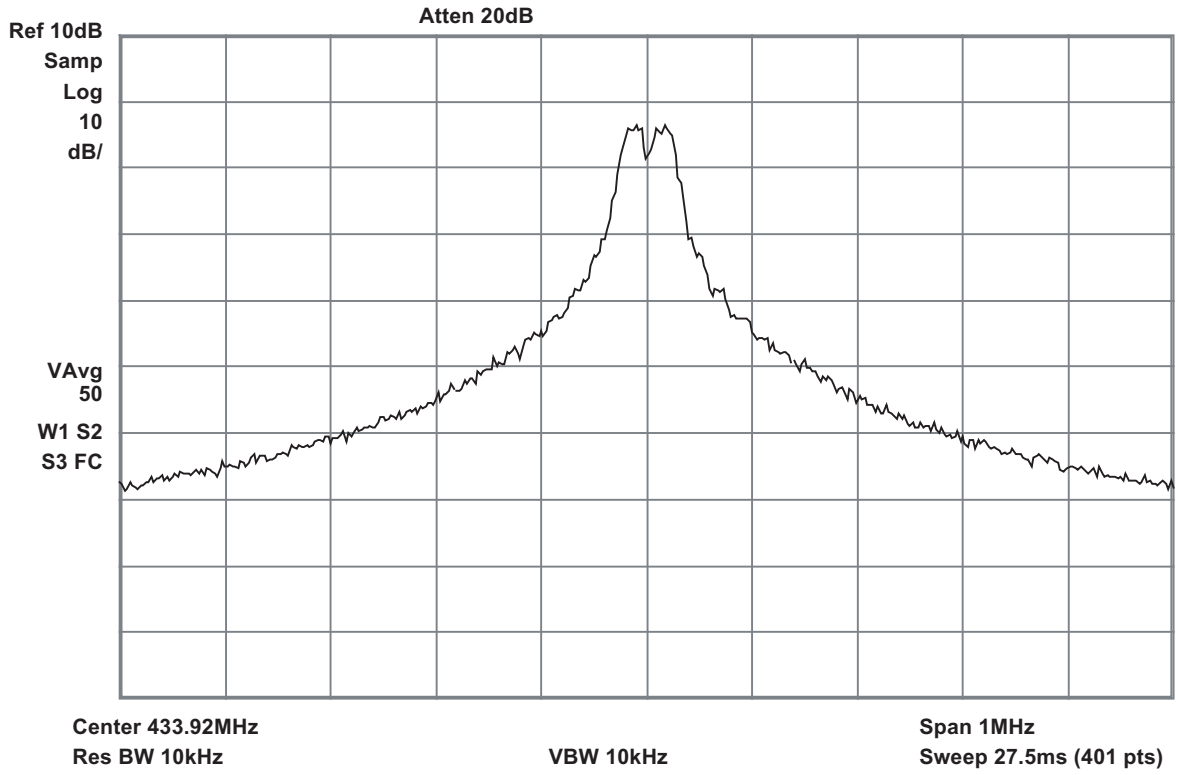


Figure 3-9. FSK-modulated TX Spectrum (433.92MHz/20Kbit/s/±16.17kHz/Manchester Code)



3.12 Output Power Setting and PA Matching at RF_OUT

The Power Amplifier (PA) is a single-ended open collector stage which delivers a current pulse which is nearly independent of supply voltage, temperature and tolerances due to band gap stabilization. Resistor R_1, see Figure 3-10, sets a reference current which controls the current in the PA. A higher resistor value results in a lower reference current, a lower output power and a lower current consumption of the PA. The usable range of R_1 is 15kΩ to 56kΩ. Pin PWR_H switches the output power range between about 0dBm to 5dBm (PWR_H = GND) and 5dBm to 10dBm (PWR_H = AVCC) by multiplying this reference current by a factor 1 (PWR_H = GND) and 2.5 (PWR_H = AVCC), which corresponds to about 5dB more output power.

If the PA is switched off in TX mode, the current consumption without output stage with VS1 = VS2 = 3V, T_{amb} = 25°C is typically 6.5mA for 868.3MHz and 6.95mA for 433.92MHz.

The maximum output power is achieved with optimum load resistances R_{Lopt} according to Table 3-7 on page 19 with compensation of the 1.0pF output capacitance of the RF_OUT pin by absorbing it into the matching network consisting of L_1, C_1, C_3 as shown in Figure 3-10 on page 18. There must also be a low resistive DC path to AVCC to deliver the DC current of the power amplifier's last stage. The matching of the PA output was done with the circuit shown in Figure 3-10 on page 18 with the values in Table 3-7 on page 19. Note that value changes of these elements may be necessary to compensate for individual board layouts.

Example:

According to Table 3-7 on page 19, with a frequency of 433.92 MHz and output power of 11dBm the overall current consumption is typically 17.8mA; hence, the PA needs 17.8mA - 6.95mA = 10.85mA in this mode, which corresponds to an overall power amplifier efficiency of the PA of $(10^{(11dBm/10)} \times 1\ mW)/(3V \times 10.85mA) \times 100\% = 38.6\%$ in this case.

Using a higher resistor in this example of $R_1 = 1.091 \times 22k\Omega = 24k\Omega$ results in 9.1% less current in the PA of 10.85mA/1.091 = 9.95mA and $10 \times \log(1.091) = 0.38dB$ less output power if using a new load resistance of $300\Omega \times 1.091 = 327\Omega$. The resulting output power is then 11dBm – 0.38dB = 10.6dBm and the overall current consumption is 6.95mA + 9.95mA = 16.9mA.

The values of Table 3-7 on page 19 were measured with standard multi-layer chip inductors with quality factors Q according to Table 3-7 on page 19. Looking to the 433.92MHz/11dBm case with the quality factor of Q_{L1} = 43 the loss in this inductor is estimated with the parallel equivalent resistance of the inductor $R_{loss} = 2 \times \pi \times f \times L \times Q_{L1}$ and the matching loss with $10 \log (1 + R_{Lopt}/R_{loss})$ which is equal to 0.32dB losses in this inductor. Taking this into account, the PA efficiency is then 42% instead of 38.6%.

Be aware that the high power mode (PWR_H = AVCC) can only be used with a supply voltage higher than 2.7V, whereas the low power mode (PWR_H = GND) can be used down to 2.4V as can be seen in the "Electrical Characteristics: General" on page 58.

The supply blocking capacitor C_2 (10nF) has to be placed close to the matching network because of the RF current flowing through it.

Figure 3-10. Power Setting and Output Matching

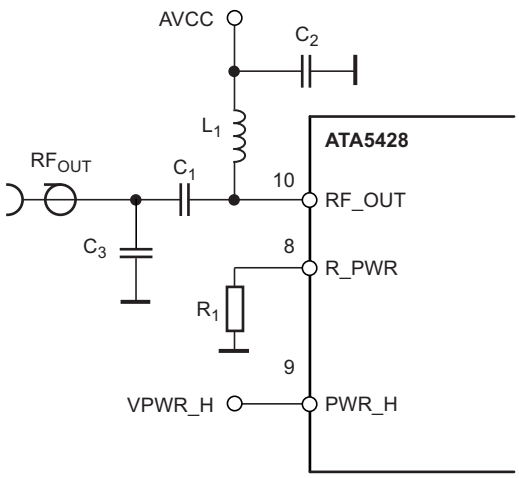


Table 3-7. Measured Output Power and Current Consumption with VS1 = VS2 = 3V, T_{amb} = 25°C

Frequency (MHz)	TX Current (mA)	Output Power (dBm)	R1 (kΩ)	VPWR_H	R_{Lopt} (Ω)	L1 (nH)	Q_{L1}	C1 (pF)	C3 (pF)
433.92	8.6	0.1	56	GND	2300	56	40	0.75	0
433.92	11.2	6.2	22	GND	890	47	38	1.5	0
433.92	17.8	11	22	AVCC	300	33	43	2.7	0
868.3	9.3	-0.3	33	GND	1170	12	58	1.0	3.3
868.3	11.5	5.4	15	GND	471	15	54	1.0	0
868.3	16.3	9.5	22	AVCC	245	10	57	1.5	0

3.13 Output Power and TX Supply Current versus Supply Voltage and Temperature

Table 3-8 shows the measurement of the output power for a typical device with VS = VS1 = VS2 in the 433.92MHz and 6.2dBm case versus temperature and supply voltage measured according to Figure 3-10 on page 18 with components according to Table 3-7. As opposed to the receiver sensitivity, the supply voltage has here the major impact on output power variations because of the large signal behavior of a power amplifier. Thus, a two battery system with voltage regulator or a 5V system shows much less variation than a 2.4V to 3.6V one battery system because the supply voltage is then well within 3.0V and 3.6V.

The reason is that the amplitude at the output RF_OUT with optimum load resistance is AVCC – 0.4V and the power is proportional to $(AVCC – 0.4V)^2$ if the load impedance is not changed. This means that the theoretical output power reduction if reducing the supply voltage from 3.0V to 2.4V is 10 log $((3V – 0.4V)^2/(2.4V – 0.4V)^2)$ = 2.2dB. Table 3-8 shows that principle behavior in the measurement. This is not the same case for higher voltages, since here increasing the supply voltage from 3V to 3.6V should theoretical increase the power by 1.8dB; but a gain of only 0.8dB in the measurement shows that the amplitude does not increase with the supply voltage because the load impedance is optimized for 3V and the output amplitude stays more constant.

Table 3-8. Measured Output Power and Supply Current at 433.92MHz, PWR_H = GND

VS =	2.4V	3.0V	3.6V
T_{amb} = –40°C	10.19mA 3.8dBm	10.19mA 5.5dBm	10.78mA 6.2dBm
T_{amb} = +25°C	10.62mA 4.6dBm	11.19mA 6.2dBm	11.79mA 7.1dBm
T_{amb} = +85°C	11.4mA 3.9dBm	12.02mA 5.5dBm	12.73mA 6.6dBm

Table 3-9 shows the relative changes of the output power of a typical device compared to 3.0V/25°C. As can be seen, a temperature change to –40°C as well as to +85°C reduces the power by less than 1dB due to the band gap regulated output current. Measurements of all the cases in Table 3-7 on page 19 over temperature and supply voltage have shown about the same relative behavior as shown in Table 3-9.

Table 3-9. Measurements of Typical Output Power Relative to 3V/25°C

VS =	2.4V	3.0V	3.6V
T_{amb} = –40°C	–2.4dB	–0.7dB	0dB
T_{amb} = +25°C	–1.6dB	0dB	+0.9dB
T_{amb} = +85°C	–2.3dB	–0.7dB	+0.4dB

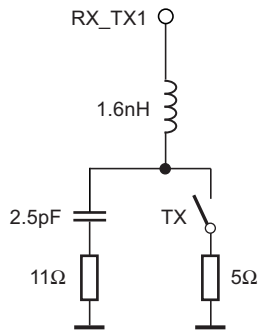
3.14 RX/TX Switch

The RX/TX switch decouples the LNA from the PA in TX mode, and directs the received power to the LNA in RX mode. To do this, it has a low impedance to GND in TX mode and a high impedance to GND in RX mode. To design a proper RX/TX decoupling, a linear simulation tool for radio frequency design together with the measured device impedances of Table 3-1 on page 10, Table 3-7 on page 19, Table 3-10 and Table 3-11 on page 21 should be used, but the exact element values have to be found on-board. Figure 3-11 shows an approximate equivalent circuit of the switch. The principal switching operation is described here according to the application of Figure 2-1 on page 7. The application of Figure 2.2 on page 8 works similarly.

Table 3-10. Impedance of the RX/TX Switch RX_TX2 Shorted to GND

Frequency	Z(RX_TX1) TX Mode	Z(RX_TX1) RX Mode
433.92MHz	(4.5 + j4.3)Ω	(10.3 – j153)Ω
868.3MHz	(5 + j9)Ω	(8.9 – j73)Ω

Figure 3-11. Equivalent Circuit of the Switch



3.15 Matching Network in TX Mode

In TX mode the 20mm long and 0.4mm wide transmission line which is much shorter than λ/4 is approximately switched in parallel to the capacitor C_9 to GND. The antenna connection between C_8 and C_9 has an impedance of about 50Ω locking from the transmission line into the loop antenna with pin RF_OUT, L_2, C_{10}, C_8 and C_9 connected (using a C_9 without the added 7.6pF as discussed later). The transmission line can be approximated with a 16nH inductor in series with a 1.5Ω resistor, the closed switch can be approximated according to Table 3-10 with the series connection of 1.6nH and 5Ω in this mode. To have a parallel resonant high impedance circuit with little RF power going into it looking from the loop antenna into the transmission line a capacitor of about 7.6pF to GND is needed at the beginning of the transmission line (this capacitor is later absorbed into C_9 which is then higher, as needed for 50Ω transformation). To keep the 50Ω impedance in RX mode at the end of this transmission line, C_7 also has to be about 7.6pF. This reduces the TX power by about 0.5dB at 433.92MHz compared to the case the where the LNA path is completely disconnected.

3.16 Matching Network in RX Mode

In RX mode the RF_OUT pin has a high impedance of about 7kΩ in parallel with 1.0pF at 433.92MHz as can be seen in Table 3-11. This, together with the losses of the inductor L_2 with 120nH and Q_{L2} = 25, gives about 3.7kΩ loss impedance at RF_OUT. Since the optimum load impedance in TX mode for the power amplifier at RF_OUT is 890Ω the loss associated with the inductor L_2 and the RF_OUT pin can be estimated to be 10 × log(1 + 890/3700) = 0.95dB compared to the optimum matched loop antenna without L_2 and RF_OUT. The switch represents, in this mode at 433.92MHz, approximately an inductor of 1.6nH in series with the parallel connection of 2.5pF and 2.0kΩ. Since the impedance level at pin RX_TX1 in RX mode is about 50Ω this only negligibly dampens the received signal (by about 0.1dB). When matching the LNA to the loop antenna, the transmission line and the 7.6pF part of C_9 have to be taken into account when choosing the values of C_{11} and L_1 so that the impedance seen from the loop antenna into the transmission line with the 7.6pF capacitor connected is 50Ω. Since the loop antenna in RX mode is loaded by the LNA input impedance, the loaded Q of the loop antenna is lowered by about a factor of 2 in RX mode; hence the antenna bandwidth is higher than in TX mode.

Table 3-11. Impedance RF_OUT Pin in RX Mode

Frequency	Z(RF_OUT)RX	R_P//C_P
433.92MHz	19Ω – j 366Ω	7kΩ//1.0pF
868.3MHz	2.8Ω – j 141Ω	7kΩ//1.3pF

Note that if matching to 50Ω, like in Figure 2.2 on page 8, a high Q wire-wound inductor with a Q > 70 should be used for L_2 to minimize its contribution to RX losses that will otherwise be dominant. The RX and TX losses will be in the range of 1.0dB there.

4. XTO

The XTO is an amplitude-regulated Pierce oscillator type with integrated load capacitances (2 × 18pF with a tolerance of ±17%) hence C_{Lmin} = 7.4pF and C_{Lmax} = 10.6pF. The XTO oscillation frequency f_{XTO} is the reference frequency FREF for the fractional-N synthesizer. When designing the system in terms of receiving and transmitting frequency offset, the accuracy of the crystal and XTO have to be considered.

The synthesizer can adjust the local oscillator frequency for the initial frequency error in f_{XTO}. This is done at nominal supply voltage and temperature with the control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33). The remaining local oscillator tolerance at nominal supply voltage and temperature is then < ±0.5ppm. The XTO's gm has very low influence of less than ±2ppm on the frequency at nominal supply voltage and temperature.

In a single channel system less than ±150ppm should be corrected to avoid that harmonics of the CLK output disturb the receive mode. If the CLK is not used or if it is carefully laid out on the application PCB (as needed for multi channel systems), more than ±150ppm can be compensated.

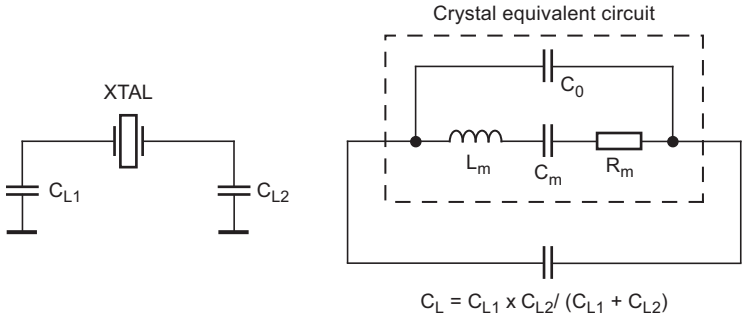
Over temperature and supply voltage, the XTO's additional pulling is only ±2ppm. The XTAL versus temperature and its aging is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances $C_{L1, 2}$ at pin XTAL1 and XTAL2. The pulling of f_{XTO} from the nominal f_{XTAL} is calculated using the following formula:

$$P = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_0 + C_{LN}) \times (C_0 + C_L)} \times 10^6 \quad \text{ppm.}$$

C_m is the crystal's motional, C_0 the shunt and C_{LN} the nominal load capacitance of the XTAL found in its data sheet. C_L is the total actual load capacitance of the crystal in the circuit and consists of C_{L1} and C_{L2} in series connection.

Figure 4-1. XTAL with Load Capacitance



With $C_m \leq 14fF$, $C_0 \geq 1.5pF$, $C_{LN} = 9pF$ and $C_L = 7.4pF$ to $10.6pF$, the pulling amounts to $P \leq \pm 100ppm$ and with $C_m \leq 7fF$, $C_0 \geq 1.5pF$, $C_{LN} = 9pF$ and $C_L = 7.4pF$ to $10.6pF$, the pulling is $P \leq \pm 50ppm$.

Since typical crystals have less than ±50ppm tolerance at 25°C, the compensation is not critical, and can in both cases be done with the ±150ppm.

C_0 of the XTAL has to be lower than $C_{Lmin}/2 = 3.7pF$ for a Pierce oscillator type in order to not enter the steep region of pulling versus load capacitance where there is a risk of an unstable oscillation.

To ensure proper start-up behavior the small signal gain, and thus the negative resistance, provided by this XTO at start is very large; for example, oscillation starts up even in worst case with a crystal series resistance of 1.5kΩ at $C_0 \leq 2.2pF$ with this XTO. The negative resistance is approximately given by

$$\mathrm{Re}\{Z_{XTOcore}\} = \mathrm{Re}\left\{\frac{Z_1 \times Z_3 + Z_2 \times Z_3 + Z_1 \times Z_2 \times Z_3 \times g_m}{Z_1 + Z_2 + Z_3 + Z_1 \times Z_2 \times g_m}\right\}$$

with Z_1, Z_2 as complex impedances at pin XTAL1 and XTAL2, hence
$Z_1 = -j/(2 \times \pi \times f_{XTO} \times C_{L1}) + 5\Omega$ and $Z_2 = -j/(2 \times \pi \times f_{XTO} \times C_{L2}) + 5\Omega$.

Z_3 consists of crystals C_0 in parallel with an internal 110 kΩ resistor hence
$Z_3 = -j/(2 \times \pi \times f_{XTO} \times C_0) /110k\Omega$, gm is the internal transconductance between XTAL1 and XTAL2 with typically 19mS at 25°C.

With $f_{XTO} = 13.5MHz$, gm = 19mS, $C_L = 9pF$, and $C_0 = 2.2pF$, this results in a negative resistance of about 2kΩ. The worst case for technological, temperature and supply voltage variations is then for $C_0 \leq 2.2pF$ always higher than 1.5kΩ.

Due to the large gain at startup, the XTO is able to meet a very low start-up time. The oscillation start-up time can be estimated with the time constant τ.

$$\tau = \frac{2}{4 \times \pi^2 \times f_m^2 \times C_m \times (\mathrm{Re}(Z_{XTOcore}) + R_m)}$$

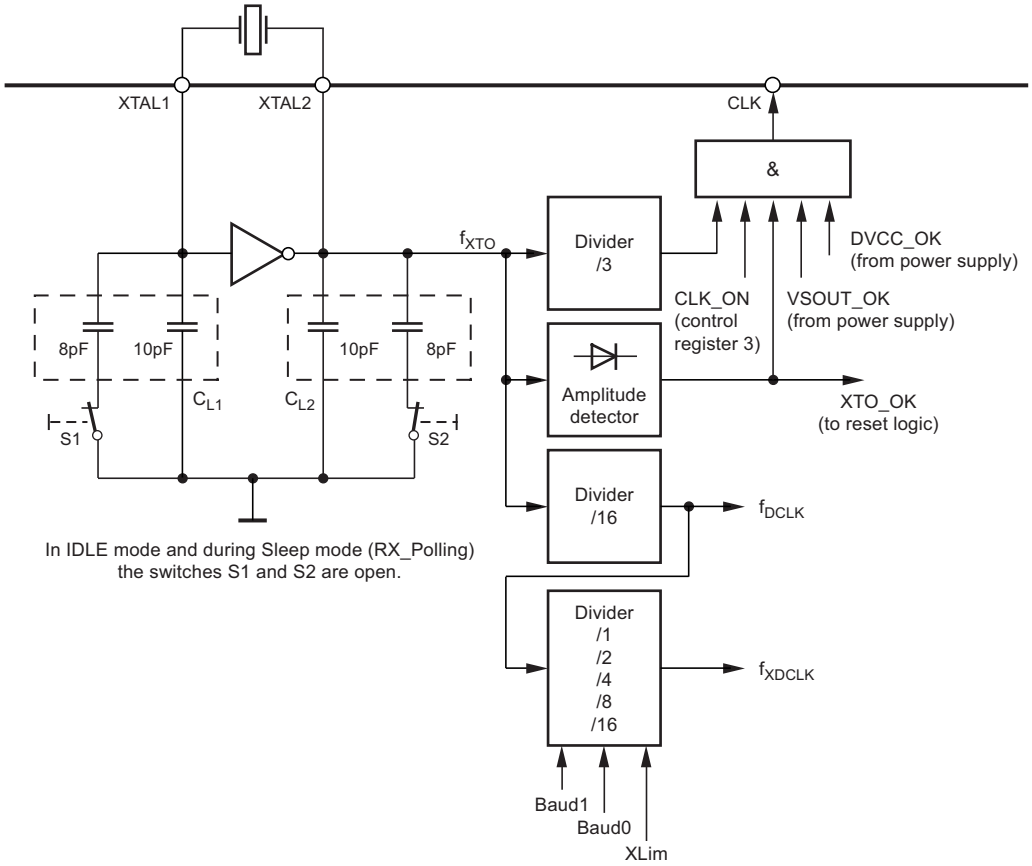
After 10τ to 20τ an amplitude detector detects the oscillation amplitude and sets XTO_OK to High if the amplitude is large enough. This sets N_RESET to High and activates the CLK output if CLK_ON in control register 3 is High (see Table 7-7 on page 32). Note that the necessary conditions of the VSOUT and DVCC voltage also have to be fulfilled (see Figure 4-2 on page 23 and Figure 5-1 on page 25).

To save current in IDLE and Sleep modes, the load capacitors are partially switched off in these modes with S1 and S2, as seen in Figure 4-2 on page 23.

It is recommended to use a crystal with $C_m = 3.0fF$ to $7.0fF$, $C_{LN} = 9pF$, $R_m < 120\Omega$ and $C_0 = 1.0pF$ to $2.2pF$.

Lower values of C_m can be used, this increases the start-up time slightly. Lower values of C_0 or higher values of C_m (up to 15fF) can also be used, this has only little influence on pulling.

Figure 4-2. XTO Block Diagram



To find the right values used in control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33), the relationship between f_{XTO} and the f_{RF} is shown in Table 4-1 on page 23. To determine the right content, the frequency at pin CLK as well as the output frequency at RF_OUT in ASK mode can be measured, then the FREQ value can be calculated according to Table 4-1 on page 23 so that f_{RF} is exactly the desired radio frequency.

Table 4-1. Calculation of f_{RF}

Frequency (MHz)	Pin 6 433_N868	CREG1 Bit(4) FS	f_{XTO} (MHz)	$f_{RF} = f_{TX\_ASK} = f_{RX}$	$f_{TX\_FSK\_L}$	$f_{TX\_FSK\_H}$	Frequency Resolution
433.92	AVCC	0	13.25311	$f_{XTO} \times \left(32.5 + \frac{FREQ + 20.5}{16384}\right)$	f_{RF} – 16.17kHz	f_{RF} + 16.17kHz	808.9Hz
868.3	GND	0	13.41191	$f_{XTO} \times \left(64.5 + \frac{FREQ + 20.5}{16384}\right)$	f_{RF} – 16.37kHz	f_{RF} + 16.37kHz	818.6Hz

The variable FREQ depends on FREQ2 and FREQ3, which are defined by the bits FR0 to FR12 in control register 2 and 3, and is calculated as follows:

FREQ = FREQ2 + FREQ3

Care must be taken to the harmonics of the CLK output signal f_{CLK} as well as to the harmonics produced by an microprocessor clocked with it, since these harmonics can disturb the reception of signals if they get to the RF input. In a single channel system, using FREQ = 3803 to 4053 ensures that the harmonics of this signal do not disturb the receive mode. In a multichannel system, the CLK signal can either be not used or carefully laid out on the application PCB. The supply voltage of the microcontroller must also be carefully blocked in a multichannel system.

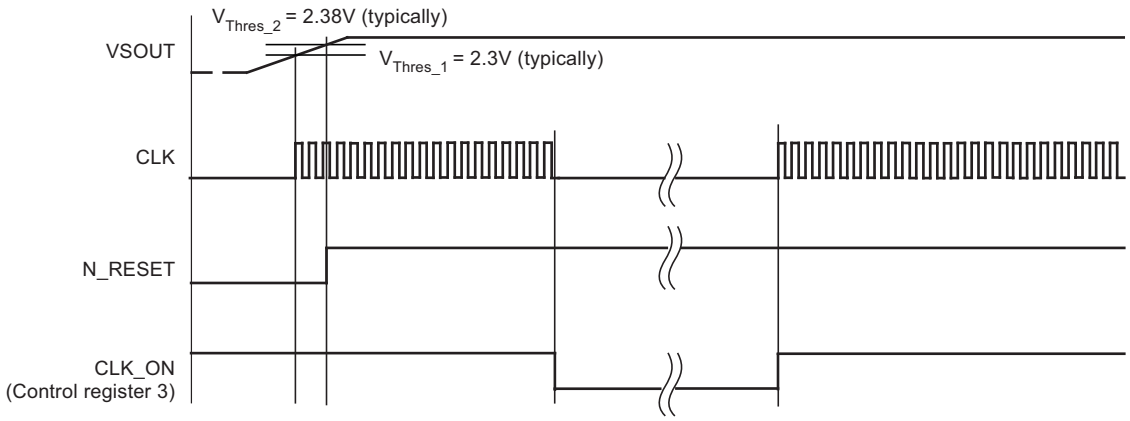
4.1 Pin CLK

Pin CLK is an output to clock a connected microcontroller. The clock frequency f_{CLK} is calculated as follows:

$$f_{CLK} = \frac{f_{XTO}}{3}$$

Because the enabling of pin CLK is asynchronous, the first clock cycle may be incomplete. The signal at CLK output has a nominal 50% duty cycle.

Figure 4-3. Clock Timing



4.2 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry is derived from one clock. As shown in Figure 4-2 on page 23, this clock cycle T_{DCLK} is derived from the crystal oscillator (XTO) in combination with a divider.

$$f_{DCLK} = \frac{f_{XTO}}{16}$$

T_{DCLK} controls the following application relevant parameters:

- Timing of the polling circuit including bit check
- TX bit rate

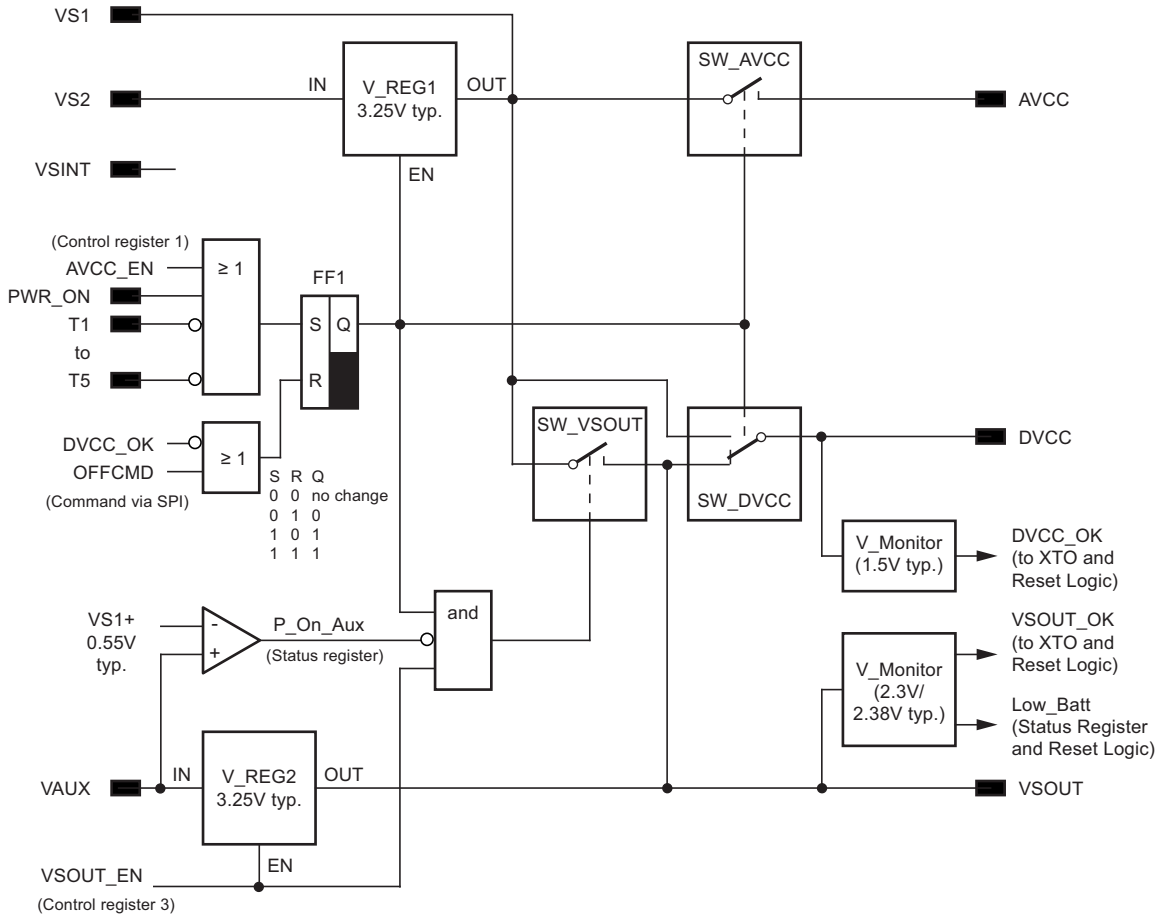
The clock cycle of the bit check and the TX bit rate depends on the selected bit-rate range (BR_Range) which is defined in control register 6 (see Table 7-20 on page 35) and XLim which is defined in control register 4 (see Table 7-13 on page 33). This clock cycle T_{XDCLK} is defined by the following formulas for further reference:

BR_Range ⇒

BR_Range 0: $T_{XDCLK} = 8 \times T_{DCLK} \times X_{Lim}$
BR_Range 1: $T_{XDCLK} = 4 \times T_{DCLK} \times X_{Lim}$
BR_Range 2: $T_{XDCLK} = 2 \times T_{DCLK} \times X_{Lim}$
BR_Range 3: $T_{XDCLK} = 1 \times T_{DCLK} \times X_{Lim}$

5. Power Supply

Figure 5-1. Power Supply



The supply voltage range of the ATA5428 is 2.4V to 3.6V or 4.4V to 6.6V.

Pin VS1 is the supply voltage input for the range 2.4V to 3.6V and is used in 1 Li battery applications (3V) using a single lithium 3V cell. Pin VS2 is the voltage input for the range 4.4V to 6.6V (2 Li battery application (6V) and Base-station Application (5V); in this case, the voltage regulator V_REG1 regulates VS1 to typically 3.25V. If the voltage regulator is active, a blocking capacitor of 2.2µF has to be connected to VS1.

Pin VAUX is an input for an additional auxiliary voltage supply and can be connected, for example, to an inductive supply (see Figure 5-6 on page 29). This input can only be used together with a rectifier or as in the application shown in Figure 2.2 on page 8 and must otherwise be left open.

Pin VSINT is the voltage input for the Microcontoller_Interface and must be connected to the power supply of the microcontroller. The voltage range of V_{VSINT} is 2.4V to 5.25V (see Figure 5-5 on page 29 and Figure 5-6 on page 29).

AVCC is the internal operation voltage of the RF transceiver and is fed by VS1 via the switch SW_AVCC. AVCC must be blocked with a 68nF capacitor (see Figure 2-1 on page 7, Figure 2.2 on page 8 and Figure 2-3 on page 9).

DVCC is the internal operation voltage of the digital control logic and is fed by VS1 or VSOUT via the switch SW_DVCC. DVCC must be blocked on pin DVCC with 68 nF (see Figure 2-1 on page 7, Figure 2.2 on page 8 and Figure 2-3 on page 9).

Pin VSOUT is a power supply output voltage for external devices (for example, microcontrollers) and is fed by VS1 via the switch SW_VSOUT, or by the auxiliary voltage supply VAUX via V_REG2. The voltage regulator V_REG2 regulates VSOUT to typically 3.25V. If the voltage regulator is active, a blocking capacitor of 2.2µF has to be connected to VSOUT. VSOUT can be switched off by the VSOUT_EN bit in control register 3 and is then reactivated by conditions found in Figure 5-2 on page 26.

Pin N_RESET is set to low if the voltage V_{VSOUT} at pin VSOUT drops below 2.3V (typically) and can be used as a reset signal for a connected microcontroller (see Figure 5-3 on page 28 and Figure 5-4 on page 28).

Pin PWR_ON is an input to switch on the transceiver (active high).

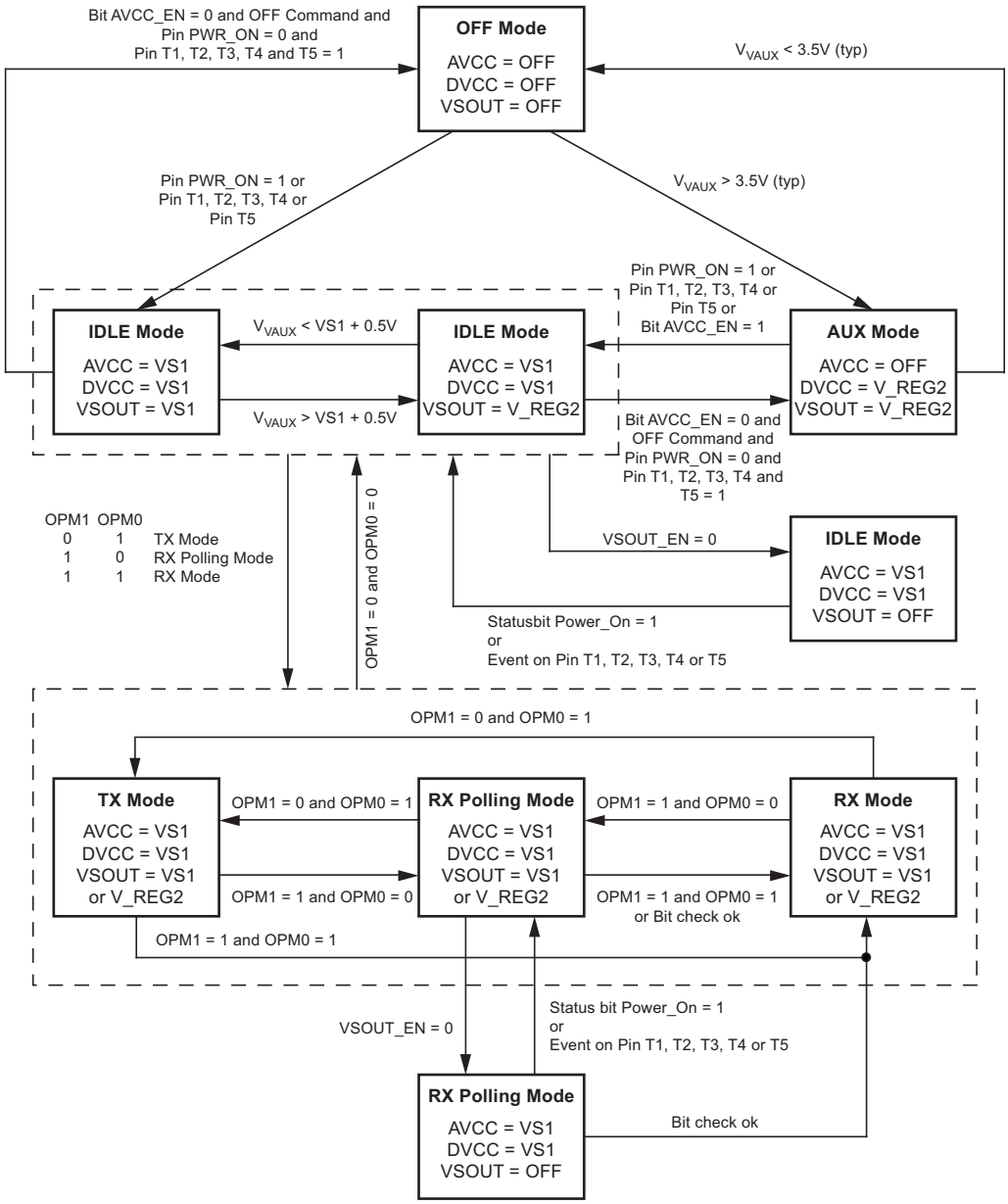
Pin T1 to T5 are inputs for push buttons and can also be used to switch on the transceiver (active low).

For current consumption reasons it is recommended to set T1 to T5 to GND, or PWR_ON to VCC only temporarily. Otherwise, an additional current flows because of a 50kΩ pull-up resistor.

There are two voltage monitors generating the following signals (see Figure 5-1 on page 25):

- DVCC_OK if DVCC > 1.5V typically
- VSOUT_OK if VSOUT > V_{Thres1} (2.3V typically)
- Low_Batt if VSOUT < V_{Thres2} (2.38V typically)

Figure 5-2. Operation Modes Flow Chart



5.1 OFF Mode

If the power supply (battery) is connected to pin VS1 and/or VS2, and if the voltage on pin VAUX V_{VAUX} < 3.5V (typically), then the transceiver is in OFF mode. In OFF mode AVCC, DVCC and VSOUT are disabled, resulting in very low power consumption (I_{S_OFF} is typically 10nA). In OFF mode the transceiver is not programmable via the 4-wire serial interface.

5.2 AUX Mode

The transceiver changes from OFF mode to AUX mode if the voltage at pin VAUX V_{VAUX} > 3.5V (typically). In AUX mode DVCC and VSOUT are connected to the auxiliary power supply input (VAUX) via the voltage regulator V_REG2. In AUX mode the transceiver is programmable via the 4-wire serial interface, but no RX or TX operations are possible because AVCC = OFF.

The state transition OFF mode to AUX mode is indicated by an interrupt at pin IRQ and the status bit P_On_Aux = 1.

5.3 IDLE Mode

In IDLE mode AVCC and DVCC are connected to the battery voltage (VS1).

From OFF mode the transceiver changes to IDLE mode if pin PWR_ON is set to 1 or pin T1, T2, T3, T4 or T5 is set to “0”. This state transition is indicated by an interrupt at pin IRQ and the status bits Power_On = 1 or ST1, ST2, ST3, ST4 or ST5 = 1.

From AUX mode the transceiver changes to IDLE mode by setting AVCC_EN = 1 in control register 1 via the 4-wire serial interface or if pin PWR_ON is set to “1” or pin T1, T2, T3, T4 or T5 is set to “0”.

VSOUT is either connected to VS1 or to the auxiliary power supply (V_REG2).

If V_{VAUX} < VS1 + 0.5V, VSOUT is connected to VS1. If V_{VAUX} > V_{S1} + 0.5V, VSOUT is connected to V_REG2 and the status bit P_On_Aux is set to “1”.

In IDLE mode, the RF transceiver is disabled and the power consumption I_{S_IDLE} is about 230 µA (VSOUT OFF and CLK output OFF and VS = VS1 = VS2 = 3V). The exact value of this current is strongly dependent on the application and the exact operation mode, therefore check the section “Electrical Characteristics: General” on page 58 for the appropriate application case.

Via the 4-wire serial interface a connected microcontroller can program the required parameter and enable the TX, RX polling or RX mode.

The transceiver can be set back to OFF mode by an OFF command via the 4-wire serial interface (the bit AVCC_EN must be set to “0”, the input level of pin PWR_ON must be “0” and pin T1, T2, T3, T4 and T5 = 1 before writing the OFF command).

Table 5-1. Control Register 1

OPM1	OPM0	Function
0	0	IDLE mode

5.4 Reset Timing and Reset Logic

If the transceiver is switched on (OFF mode to IDLE mode, OFF mode to AUX mode) DVCC and VSOUT ramp up as illustrated in Figure 5-3 on page 28 (AVCC only ramps up if the transceiver is set to the IDLE mode). The internal signal DVCC_RESET resets the digital control logic and sets the control register to default values.

A voltage monitor generates a low level at pin N_RESET until the voltage at pin VSOUT exceeds 2.38V (typically) and the start-up time of the XTO has elapsed (amplitude detector, see Figure 4-2 on page 23). After the voltage at pin VSOUT exceeds 2.3V (typically) and the start-up time of the XTO has elapsed, the output clock at pin CLK is available. Because the enabling of pin CLK is asynchronous, the first clock cycle may be incomplete.

The status bit Low_Batt is set to “1” if the voltage at pin VSOUT V_{VSOUT} drops below V_{Thres_2} (typically 2.38V). Low_Batt is set to “0” if V_{VSOUT} exceeds V_{Thres_2} and the status register is read via the 4-wire serial interface or N_RESET is set to low.

If V_{VSOUT} drops below V_{Thres_1} (typically 2.3V), N_RESET is set to low. If bit VSOUT_EN in control register 3 is “1”, a DVCC_RESET is also generated. If V_{VSOUT} was already disabled by the connected microcontroller by setting bit VSOUT_EN = 0, no DVCC_RESET is generated.

Note: If VSOUT < V_{Thres_1} (typically 2.3 V) the output of the pin CLK is low, the Microcontroller_Interface is disabled and the transceiver is not programmable via the 4-wire serial interface.

Figure 5-3. Reset Timing

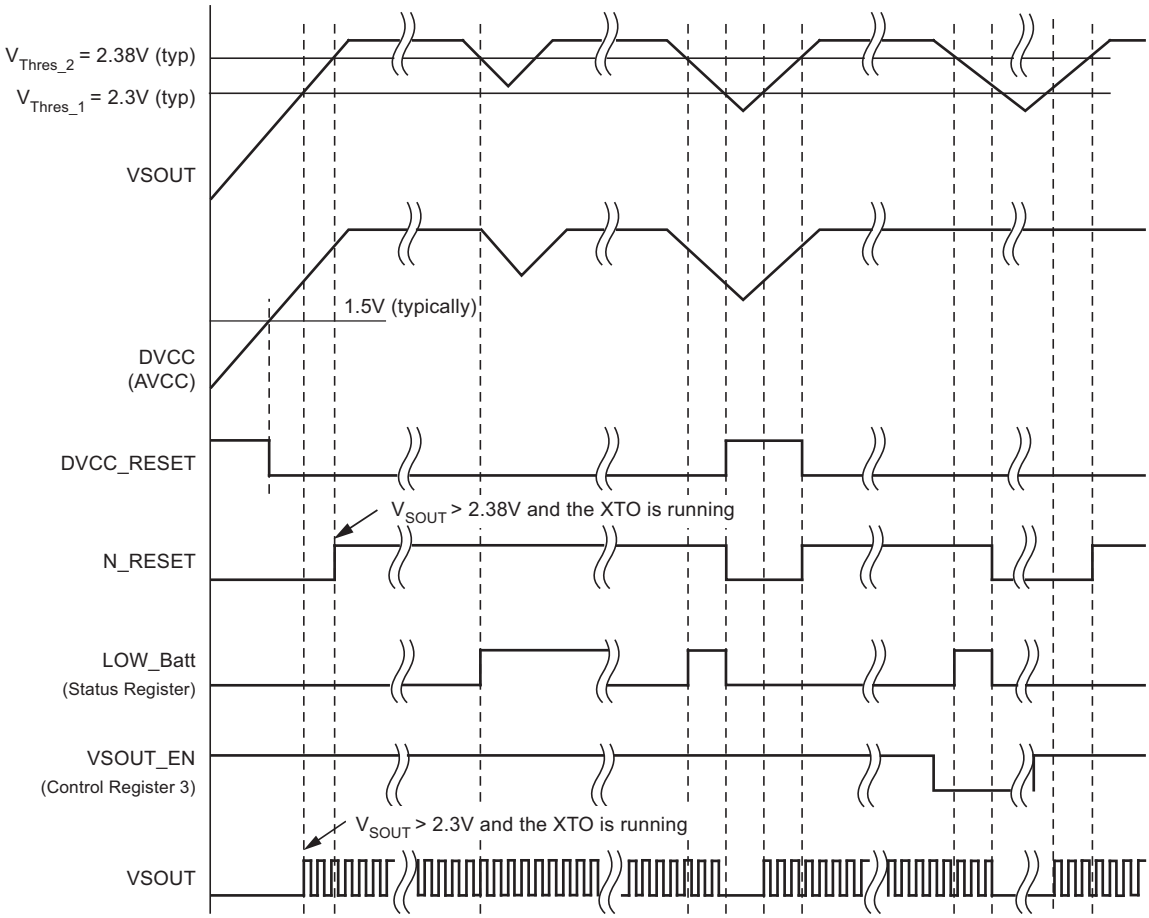
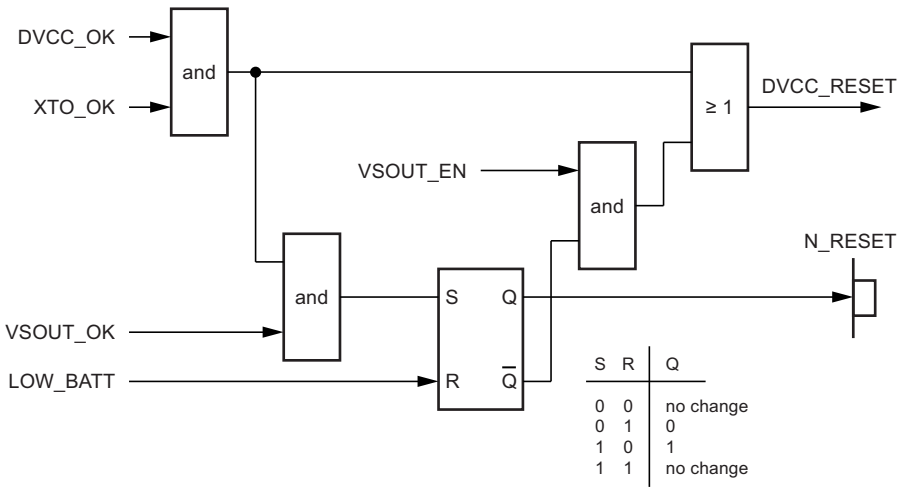


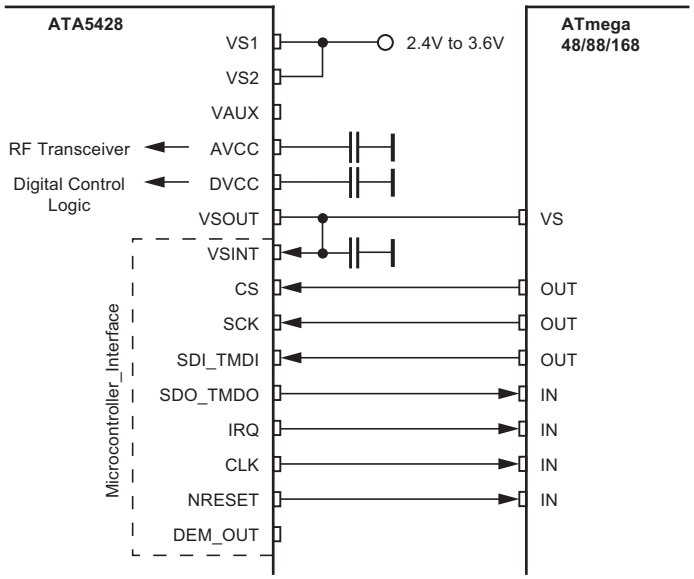
Figure 5-4. Reset Logic, SR Latch Generates the Hysteresis in the NRESET Signal



5.5 1 Li Battery Application (3V)

The supply voltage range is 2.4V to 3.6V and VAUX is not used.

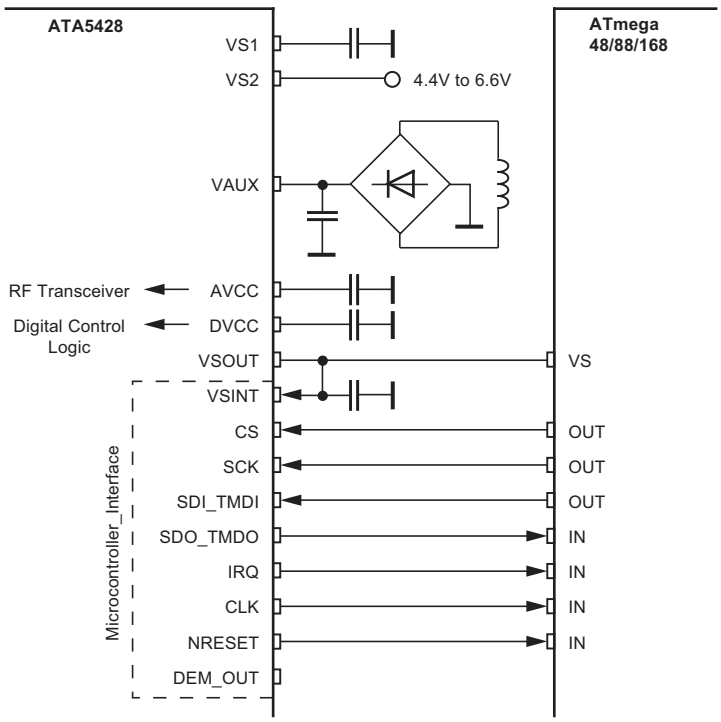
Figure 5-5. 1 Li Battery Application (3V)



5.6 2 Li Battery Application (6V)

The supply voltage range is 4.4V to 6.6V and VAUX is connected to an inductive supply.

Figure 5-6. 2 Li Battery Application (6V) with Inductive Emergency Supply



6. Microcontroller Interface

The microcontroller interface is a level converter which converts all internal digital signals that are referred to the DVCC voltage into the voltage used by the microcontroller. Therefore, the pin VSINT has to be connected to the supply voltage of the microcontroller.

This makes it possible to use the internal voltage regulator/switch at pin VSOUT as in Figure 2-1 on page 7 and Figure 2-3 on page 9 or to connect the microcontroller and the pin VSINT directly to the supply voltage of the microcontroller as in Figure 2.2 on page 8.

7. Digital Control Logic

7.1 Register Structure

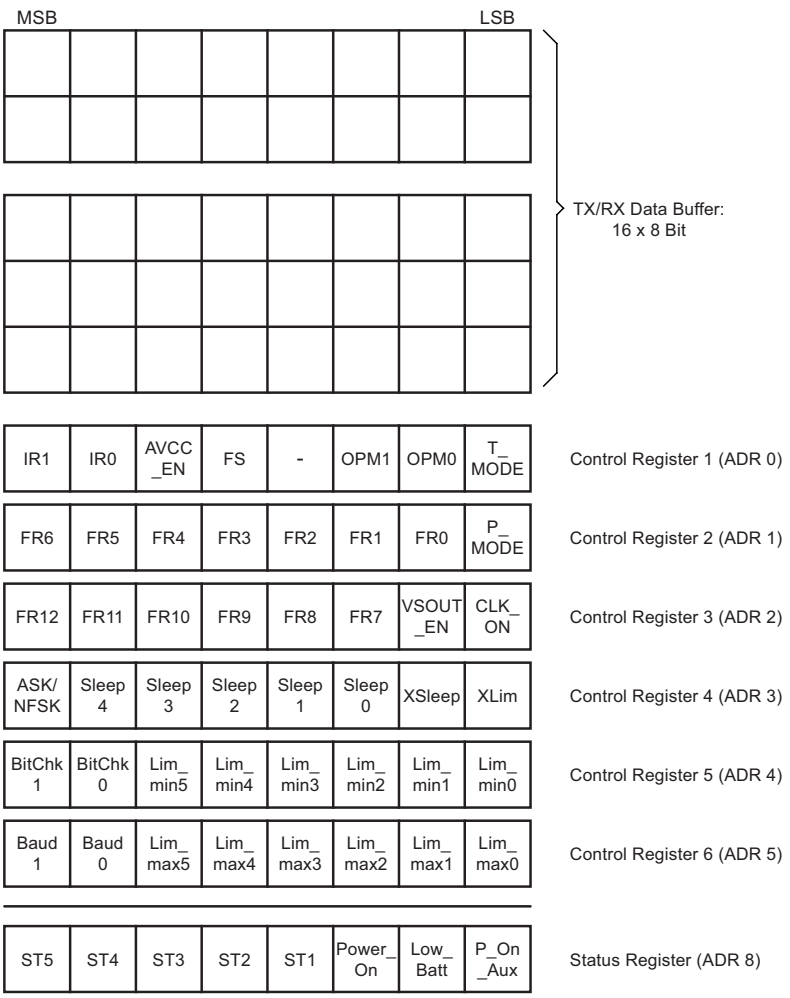
The configuration of the transceiver is stored in RAM cells. The RAM contains a 16 × 8-bit TX/RX data buffer and a 6 × 8-bit control register and is writable and readable via a 4-wire serial interface (CS, SCK, SDI_TMDI, SDO_TMDO).

The 1 × 8-bit status register is not part of the RAM and is readable via the 4-wire serial interface.

The RAM and the status information are stored as long as the transceiver is in any active mode (DVCC = VS1 or DVCC = V_REG2) and are lost when the transceiver switches to OFF mode (DVCC =OFF).

After the transceiver is turned on via pin PWR_ON = High, T1 = Low, T2 = Low, T3 = Low, T4 = Low or T5 = Low or the voltage at pin VAUX V_{VAUX} > 3.5V (typically), the control registers are in the default state.

Figure 7-1. Register Structure



7.2 TX/RX Data Buffer

The TX/RX data buffer is used to handle the data transfer during RX and TX operations.

7.3 Control Register

To use the transceiver in different applications, it can be configured by a connected microcontroller via the 4-wire serial interface.

7.3.1 Control Register 1 (ADR 0)

Table 7-1. Control Register 1 (Function of Bit 7 and Bit 6 in RX Mode)

IR1	IR0	Function (RX Mode)
0	0	Pin IRQ is set to “1” if 4 received bytes are in the TX/RX data buffer or a receiving error occurred
0	1	Pin IRQ is set to “1” if 8 received bytes are in the TX/RX data buffer or a receiving error occurred
1	0	Pin IRQ is set to “1” if 12 received bytes are in the TX/RX data buffer or a receiving error occurred (default)
1	1	Pin IRQ is set to “1” if a receiving error occurred

Table 7-2. Control Register 1 (Function of Bit 7 and Bit 6 in TX Mode)

IR1	IR0	Function (TX Mode)
0	0	Pin IRQ is set to “1” if 4 bytes remain in the TX/RX data buffer or the TX data buffer is empty
0	1	Pin IRQ is set to “1” if 8 bytes remain in the TX/RX data buffer or the TX data buffer is empty
1	0	Pin IRQ is set to “1” if 12 bytes remain in the TX/RX data buffer or the TX data buffer is empty (default)
1	1	Pin IRQ is set to “1” if the TX data buffer is empty

Table 7-3. Control Register 1 (Function of Bit 5)

AVCC_EN	Function
0	(default)

Table 7-4. Control Register 1 (Function of Bit 4)

FS	Function (RX Mode, TX Mode)
0	Selected frequency 433/868MHz (default)

Table 7-5. Control Register 1 (Function of Bit 2 and Bit 1)

OPM1	OPM0	Function
0	0	IDLE mode (default)
0	1	TX mode
1	0	RX polling mode
1	1	RX mode

Table 7-6. Control Register 1 (Function of Bit 0)

T_MODE	Function
0	TX and RX function via TX/RX data buffer (default)
1	Transparent mode, TX/RX data buffer disabled, TX modulation data stream via pin SDI_TMDI, RX modulation data stream via pin SDO_TMDO

7.3.2 Control Register 2 (ADR 1)

Table 7-7. Control Register 2 (Function of Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2 and Bit 1)

FR6 2^6	FR5 2^5	FR4 2^4	FR3 2^3	FR2 2^2	FR1 2^1	FR0 2^0	Function
0	0	0	0	0	0	0	FREQ2 = 0
0	0	0	0	0	0	1	FREQ2 = 1
.	.	.	.	.	.	.	
1	0	1	1	0	0	0	FREQ2 = 88 (default)
.	.	.	.	.	.	.	
1	1	1	1	1	1	1	FREQ2 = 127

Note: Tuning of f_{RF} LSBs (total 13 bits), frequency trimming resolution of f_{RF} is f_{XTO}/16384, which is approximately 800Hz (see section “XTO”, Table 4-1 on page 23)

Table 7-8. Control Register 2 (Function of Bit 0 in RX Mode)

P_MODE	Function (RX Mode)
0	Pin IRQ is set to “1” if the bit check is successful (default)
1	No effect on pin IRQ if the bit check is successful

Table 7-9. Control Register 2 (Function of Bit 0 in TX Mode)

P_MODE	Function (TX Mode)
0	Manchester modulator on (default)
1	Manchester modulator off (NRZ mode)

7.3.3 Control Register 3 (ADR 2)

Table 7-10. Control Register 3 (Function of Bit 7, Bit 6, Bit 5, Bit 4, Bit 3 and Bit 2)

FR12 2^{12}	FR11 2^{11}	FR10 2^{10}	FR9 2^{9}	FR8 2^{8}	FR7 2^{7}	Function
0	0	0	0	0	0	FREQ3 = 0
0	0	0	0	0	1	FREQ3 = 128
0	0	0	0	1	0	FREQ3 = 256
.	.	.	.	.	.	.
0	1	1	1	1	0	FREQ3 = 3840 (default)
.	.	.	.	.	.	.
1	1	1	1	1	0	FREQ3 = 7936
1	1	1	1	1	1	FREQ3 = 8064

Note: Tuning of f_{RF} MSBs

Table 7-11. Control Register 3 (Function of Bit 1)

VSOUT_EN	Function
0	Output voltage power supply for external devices off (pin VSOUT)
1	Output voltage power supply for external devices on (default)

Note: This bit is set to “1” if the bit check is OK (RX_Polling, RX mode), an event at pin T1, T2, T3, T4 or T5 occurs or the bit Power_On in the status register is “1”.
Setting VSOUT_EN = 0 in AUX mode is not allowed

Table 7-12. Control Register_3 (Function of Bit 0)

CLK_ON	Function
0	Clock output off (pin CLK)
1	Clock output on (default)

Note: This bit is set to “1” if the bit check is OK (RX_Polling, RX mode), an event at pin T1, T2, T3, T4 or T5 occurs or the bit Power_On in the status register is “1”.

7.3.4 Control Register 4 (ADR 3)

Table 7-13. Control Register 4 (Function of Bit 7)

ASK_NFSK	Function (TX Mode, RX Mode)
0	FSK mode (default)
1	ASK mode

Table 7-14. Control Register 4 (Function of Bit 6, Bit 5, Bit 4, Bit 3 and Bit 2)

Sleep4 2^4	Sleep3 2^3	Sleep2 2^2	Sleep1 2^1	Sleep0 2^0	Function (RX Mode) Sleep ($T_{Sleep} = Sleep \times 1024 \times T_{DCLK} \times X_{Sleep}$)
0	0	0	0	0	0
0	0	0	0	1	1
.	.	.	.	.	
0	1	0	1	0	10 ($T_{Sleep} = 10 \times 1024 \times T_{DCLK} \times X_{Sleep}$) (default)
.	.	.	.	.	
1	1	1	1	1	31

Table 7-15. Control Register 4 (Function of Bit 1)

XSleep	Function
0	X_{Sleep} = 1; extended T_{Sleep} off (default)
1	X_{Sleep} = 8; extended T_{Sleep} on

Table 7-16. Control Register 4 (Function of Bit 0)

XLim	Function
0	X_{Lim} = 1; extended T_{Lim_min}, T_{Lim_max} off (default)
1	X_{Lim} = 2; extended T_{Lim_min}, T_{Lim_max} on

7.3.5 Control Register 5 (ADR 4)

Table 7-17. Control Register 5 (Function of Bit 7 and Bit 6)

BitChk1	BitChk0	Function
0	0	$N_{Bit\text{-}check}$ = 0 (0 bits checked during bit check)
0	1	$N_{Bit\text{-}check}$ = 3 (3 bits checked during bit check) (default)
1	0	$N_{Bit\text{-}check}$ = 6 (6 bits checked during bit check)
1	1	$N_{Bit\text{-}check}$ = 9 (9 bits checked during bit check)

Table 7-18. Control Register 5 (Function of Bit 5, Bit 4, Bit 3, Bit 2, Bit 1 and Bit 0 in RX Mode)

Lim_min5	Lim_min4	Lim_min3	Lim_min2	Lim_min1	Lim_min0	Function (RX Mode) Lim_min (Lim_min < 10 are not applicable) ($T_{Lim\_min} = Lim\_min \times T_{XDCLK}$)
0	0	1	0	1	0	10
0	0	1	0	1	1	11
.	.	.	.	.	.	
0	1	0	0	0	0	16 ($T_{Lim\_min} = 16 \times T_{XDCLK}$) (default)
.	.	.	.	.	.	
1	1	1	1	1	1	63

Table 7-19. Control Register 5 (Function of Bit 5, Bit 4, Bit 3, Bit 2, Bit 1 and Bit 0 in TX Mode)

Lim_min5	Lim_min4	Lim_min3	Lim_min2	Lim_min1	Lim_min0	Function (TX Mode) Lim_min (Lim_min < 10 are not applicable) ($TX\_Bitrate = 1/((Lim\_min + 1) \times T_{XDCLK} \times 2)$)
0	0	1	0	1	0	10
0	0	1	0	1	1	11
.	.	.	.	.	.	
0	1	0	0	0	0	16 ($TX\_Bitrate = 1/((16 + 1) \times T_{XDCLK} \times 2)$) (default)
.	.	.	.	.	.	
1	1	1	1	1	1	63

7.3.6 Control Register 6 (ADR 5)

Table 7-20. Control Register 6 (Function of Bit 7 and Bit 6)

Baud1	Baud0	Function
0	0	Bit-rate range 0 (B0) 1.0 Kbit/s to 2.5 Kbit/s; $T_{XDCLK} = 8 \times T_{DCLK} \times X_{Lim}$
0	1	Bit-rate range 1 (B1) 2.0 Kbit/s to 5.0 Kbit/s; $T_{XDCLK} = 4 \times T_{DCLK} \times X_{Lim}$
1	0	Bit-rate range 2 (B2) 4.0 Kbit/s to 10.0 Kbit/s; $T_{XDCLK} = 2 \times T_{DCLK} \times X_{Lim}$; (default)
1	1	Bit-rate range 3 (B3) 8.0 Kbit/s to 20.0 Kbit/s; $T_{XDCLK} = 1 \times T_{DCLK} \times X_{Lim}$ Note that the receiver does not work with >10 Kbit/s in ASK mode

Table 7-21. Control Register 6 (Function of Bit 5, Bit 4, Bit 3, Bit 2, Bit 1 and Bit 0)

Lim_max5	Lim_max4	Lim_max3	Lim_max2	Lim_max1	Lim_max0	Function Lim_max (Lim_max < 12 is not Applicable) ($T_{Lim\_max} = (Lim\_max - 1) \times T_{XDCLK}$)
0	0	1	1	0	0	12
0	0	1	1	0	1	13
.	.	.	.	.	.	
0	1	1	1	0	0	28 ($T_{Lim\_max} = (28 - 1) \times T_{XDCLK}$) (default)
.	.	.	.	.	.	
1	1	1	1	1	1	63

7.4 Status Register

The status register indicates the current status of the transceiver and is readable via the 4-wire serial interface. Setting Power_On or P_On_Aux or an event on ST1, ST2, ST3, ST4 or ST5 is indicated by an IRQ.

Reading the status register resets the bits Power_On, Low_Batt, P_On_Aux and the IRQ.

7.4.1 Status Register (ADR 8)

Table 7-22. Status Register

Status Bit	Function
ST5	Status of pin T5 Pin T5 = 0 → ST5 = 1 Pin T5 = 1 → ST5 = 0 (see Figure 7-3 on page 38)
ST4	Status of pin T4 Pin T4 = 0 → ST4 = 1 Pin T4 = 1 → ST4 = 0 (see Figure 7-3 on page 38)
ST3	Status of pin T3 Pin T3 = 0 → ST3 = 1 Pin T3 = 1 → ST3 = 0 (see Figure 7-3 on page 38)
ST2	Status of pin T2 Pin T2 = 0 → ST2 = 1 Pin T2 = 1 → ST2 = 0 (see Figure 7-3 on page 38)
ST1	Status of pin T1 Pin T1 = 0 → ST1 = 1 Pin T1 = 1 → ST1 = 0 (see Figure 7-3 on page 38)

Table 7-22. Status Register (Continued)

Status Bit	Function
Power_On	Indicates that the transceiver was woken up by pin PWR_ON (rising edge on pin PWR_ON). During Power_On = 1, the bits VSOUT_EN and CLK_ON in control register 3 are set to “1”. (see Figure 7-4 on page 39)
Low_Batt	Indicates that output voltage on pin VSOUT is too low (V_{VSOUT} < 2.38V typically), (see Figure 7-5 on page 40)
P_On_Aux	Indicates that the auxiliary supply voltage on pin VAUX is high enough to operate. State transition: a) OFF mode → AUX mode (see Figure 5-2 on page 26) b) IDLE mode (VSOUT = VS1) → IDLE mode (VSOUT = V_REG2) (see Figure 7-6 on page 41)

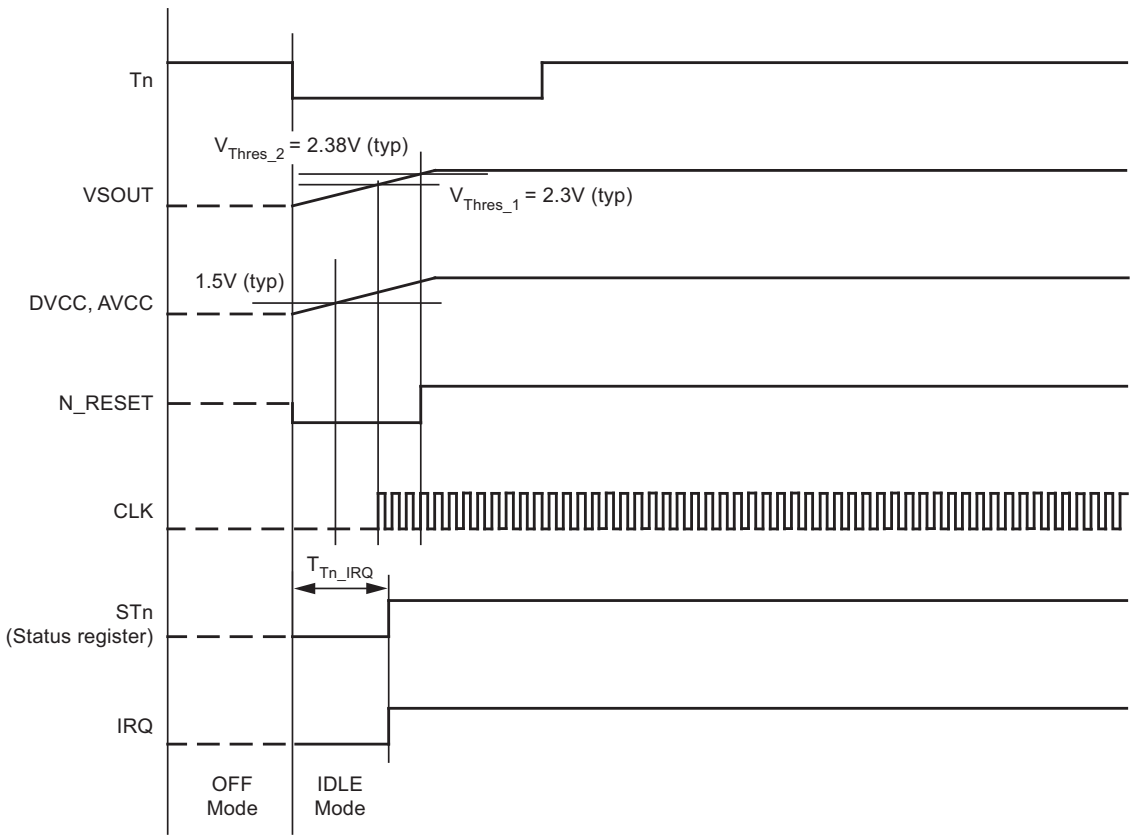
7.5 Pin Tn

To switch the transceiver from OFF to IDLE mode, pin Tn must be set to “0” (maximum 0.2 × V_{VS2}) for at least T_{Tn_IRQ} (see Figure 7-2). The transceiver recognizes the negative edge, sets pin N_RESET to low and switches on DVCC, AVCC and the power supply for external devices VSOUT.

If V_{DVCC} exceeds 1.5V (typically) and the XTO is settled, the digital control logic is active and sets the status bit STn to “1” and an interrupt is issued (T_{Tn_IRQ}).

After the voltage on pin VSOUT exceeds 2.3V (typically) and the start-up time of the XTO is elapsed, the output clock on pin CLK is available. Because the enabling of pin CLK is asynchronous, the first clock cycle may be incomplete. N_RESET is set to high if V_{VSOUT} exceeds 2.38V (typically) and the XTO is settled.

Figure 7-2. Timing Pin Tn, Status Bit STn



If the transceiver is in any active mode (IDLE, AUX, TX, RX, RX_Polling), an integrated debounce logic is active. If there is an event on pin Tn a debounce counter is set to 0 (T = 0) and started. The status is updated, an interrupt is issued and the debounce counter is stopped after reaching the counter value $T = 8195 \times T_{DCLK}$.

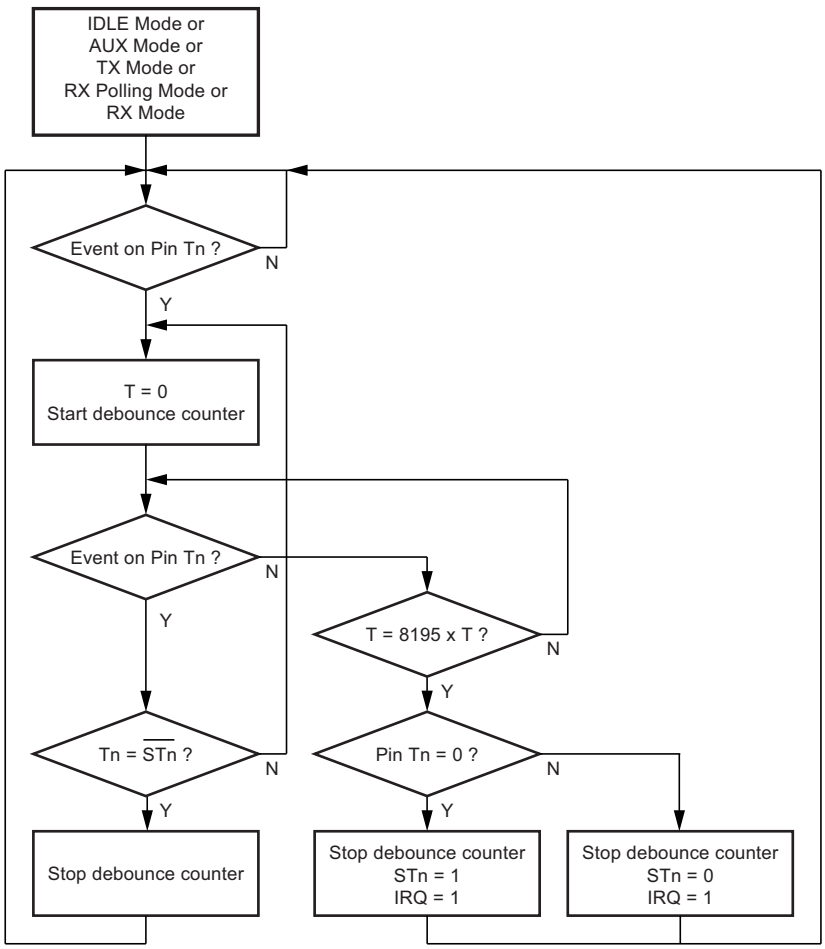
An event on the same key input before reaching $T = 8195 \times T_{DCLK}$ stops the debounce counter. An event on an other key input before reaching $T = 8195 \times T_{DCLK}$ resets and restarts the debounce counter.

While the debounce counter is running, the bits VSOUT_EN and CLK_ON in control register 3 are set to “1”.

The interrupt is deleted after reading the status register or executing the command Delete_IRQ.

If pin Tn is not used, it can be left open because of an internal pull-up resistor (typically 50kΩ).

Figure 7-3. Timing Flow Pin Tn, Status Bit STn



7.6 Pin PWR_ON

To switch the transceiver from OFF to IDLE mode, pin PWR_ON must be set to “1” (minimum $0.8 \times V_{VS2}$) for at least T_{PWR_ON} (see Figure 7-4). The transceiver recognizes the positive edge, sets pin N_RESET to low, and switches on DVCC, AVCC and the power supply for external devices VSOUT.

If V_{DVCC} exceeds 1.5V (typically) and the XTO is settled, the digital control logic is active and sets the status bit Power_On to “1” and an interrupt is issued ($T_{PWR\_ON\_IRQ\_1}$).

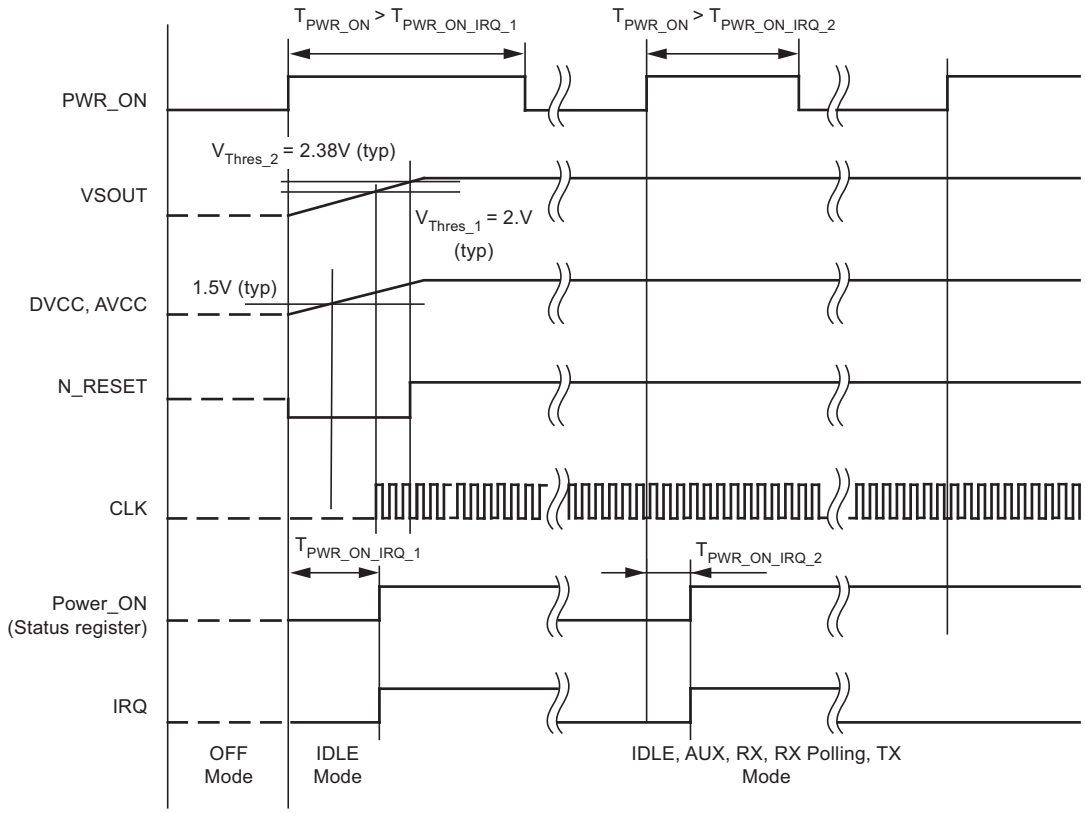
After the voltage on pin VSOUT exceeds 2.3V (typically) and the start-up time of the XTO is elapsed the output clock on pin CLK is available. Because the enabling of pin CLK is asynchronous, the first clock cycle may be incomplete. N_RESET is set to high if V_{VSOUT} exceeds 2.38V (typically) and the XTO is settled.

If the transceiver is in any active mode (IDLE, AUX, RX, RX_Polling, TX), a positive edge on pin PWR_ON sets Power_On to “1” (after $T_{PWR\_ON\_IRQ\_2}$). The state transition Power_On $0 \rightarrow 1$ generates an interrupt. If Power_On is still “1” during the positive edge on pin PWR_ON no interrupt is issued. Power_On and the interrupt are deleted after reading the status register.

During Power_On = 1, the bits VSOUT_EN and CLK_ON in control register 3 are set to “1”.

Note: It is not possible to set the transceiver to OFF mode by setting pin PWR_ON to “0”. If pin PWR_ON is not used, it must be connected to GND.

Figure 7-4. Timing Pin PWR_ON, Status Bit Power_On

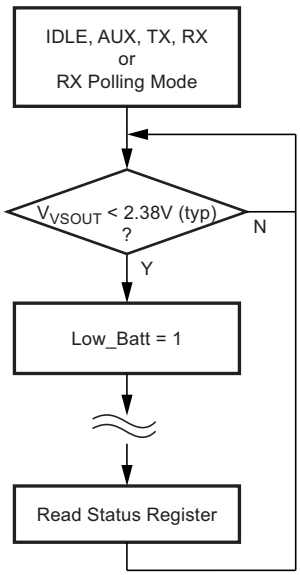


7.7 Low Battery Indicator

The status bit Low_Batt is set to “1” if the voltage V_{VSOUT} on pin VSOUT drops below 2.38V (typically).

Low_Batt is set to “0” if V_{VSOUT} exceeds V_{Thres_2} and the status register is read via the 4-wire serial interface (see Figure 5-3 on page 28).

Figure 7-5. Timing Status Bit Low_Batt



7.8 Pin VAUX

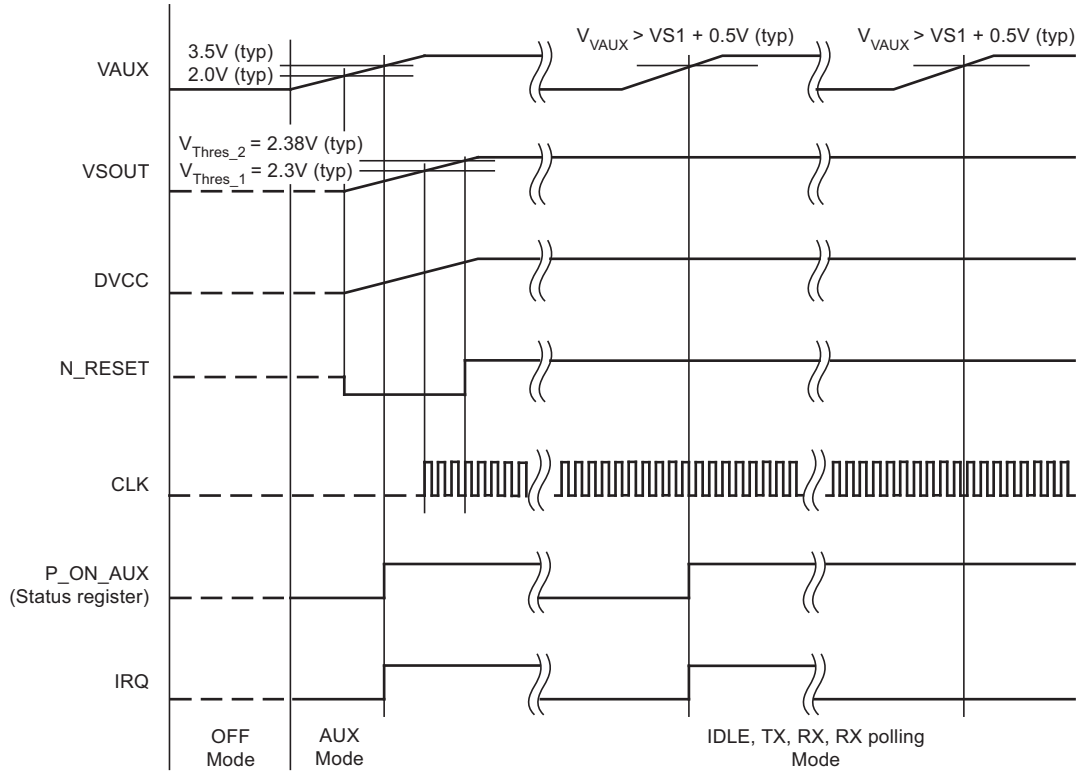
To switch the transceiver from OFF to AUX mode, the voltage V_{VAUX} on pin VAUX must exceed 3.5V (typically) (see Figure 7-6 on page 41). If V_{VAUX} exceeds 2V (typically) pin N_RESET is set to low, and DVCC and the power supply for external devices VSOUT are switched on.

If V_{VAUX} exceeds 3.5V (typically) the status bit P_On_Aux is set to “1” and an interrupt is issued.

After the voltage on pin VSOUT exceeds 2.3V (typically) and the start-up time of the XTO is elapsed, the output clock on pin CLK is available. Because the enabling of pin CLK is asynchronous, the first clock cycle may be incomplete. N_RESET is set to high if V_{VSOUT} exceeds 2.38V (typically) and the XTO is settled.

If the transceiver is in any active mode (IDLE, TX, RX, RX_Polling), a positive edge on pin VAUX and V_{VAUX} > VS1 + 0.5V sets P_On_Aux to “1”. The state transition P_On_Aux 0 → 1 generates an interrupt. If P_On_Aux is still “1” during the positive edge on pin VAUX no interrupt is issued. P_On_Aux and the interrupt are deleted after reading the status register.

Figure 7-6. Timing Pin VAUX, Status Bit P_On_Aux



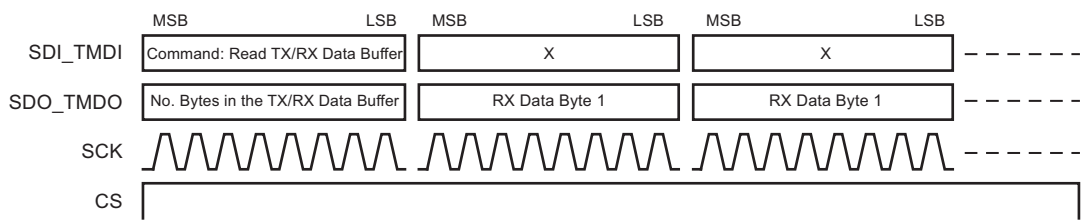
8. Transceiver Configuration

The configuration of the transceiver takes place via a 4-wire serial interface (CS, SCK, SDI_TMDI, SDO_TMDO) and is organized in 8-bit units. The configuration is initiated with an 8-bit command. While shifting the command into pin SDI_TMDI, the number of bytes in the TX/RX data buffer are available on pin SDO_TMDO. The read and write commands are followed by one or more 8-bit data units. Each 8-bit data transmission begins with the MSB. The serial interface is in the reset state if the level on pin CS = Low.

8.1 Command: Read TX/RX Data Buffer

During a RX operation, the user can read the received bytes in the TX/RX data buffer successively.

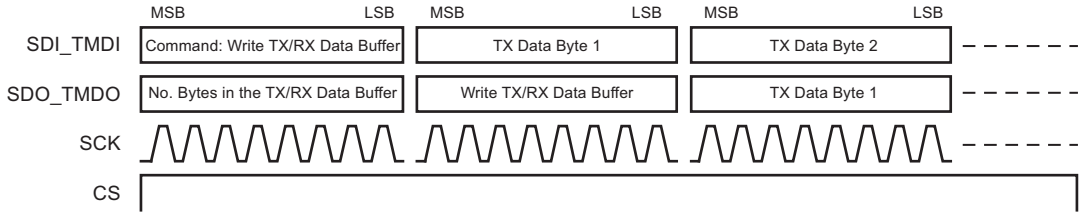
Figure 8-1. Read TX/RX Data Buffer



8.2 Command: Write TX/RX Data Buffer

During a TX operation the user can write the bytes in the TX/RX data buffer successively. An echo of the command and the TX data bytes are provided for the microcontroller on pin SDO_TMDO.

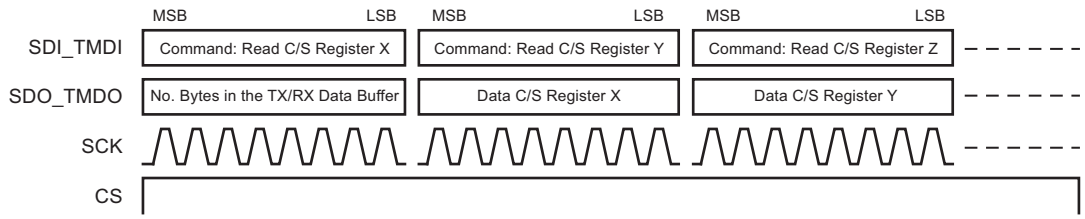
Figure 8-2. Write TX/RX Data Buffer



8.3 Command: Read Control/Status Register

The control and status registers can be read individually or successively.

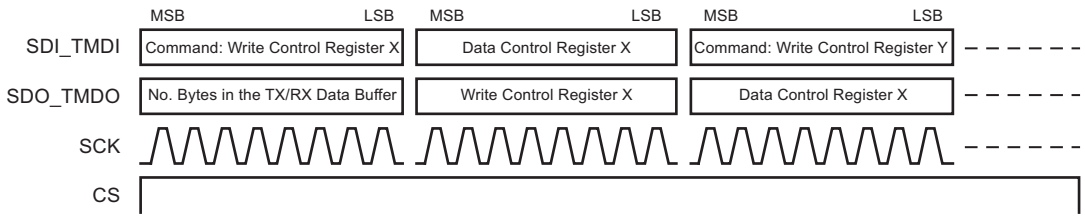
Figure 8-3. Read Control/Status Register



8.4 Command: Write Control Register

The control registers can be written individually or successively. An echo of the command and the data bytes are provided for the microcontroller on pin SDO_TMDO.

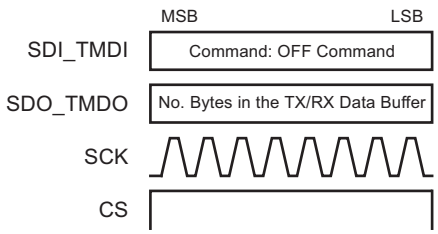
Figure 8-4. Write Control Register



8.5 Command: OFF Command

If AVCC_EN in control register 1 is “0”, the input level on pin PWR_ON is low and on the key inputs Tn is high, then the OFF command sets the transceiver in the OFF mode.

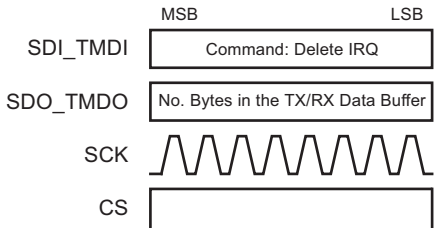
Figure 8-5. OFF Command



8.6 Command: Delete IRQ

The delete IRQ command sets pin IRQ to low.

Figure 8-6. Delete IRQ



8.7 Command Structure

The three most significant bits of the command (bit 5 to bit 7) indicate the command type. Bit 0 to bit 4 describe the target address when reading or writing a control or status register. In all other commands bit 0 to bit 4 have no effect and should be set to “0” for compatibility with future products.

Table 8-1. Command Structure

	MSB							LSB
Command	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read TX/RX data buffer	0	0	0	x	x	x	x	x
Write TX/RX data buffer	0	0	1	x	x	x	x	x
Read control/status register	0	1	0	A4	A3	A2	A1	A0
Write control register	0	1	1	A4	A3	A2	A1	A0
OFF command	1	0	0	X	X	X	X	X
Delete IRQ	1	0	1	X	X	X	X	X
Not used	1	1	0	X	X	X	X	X
Not used	1	1	1	X	X	X	X	X

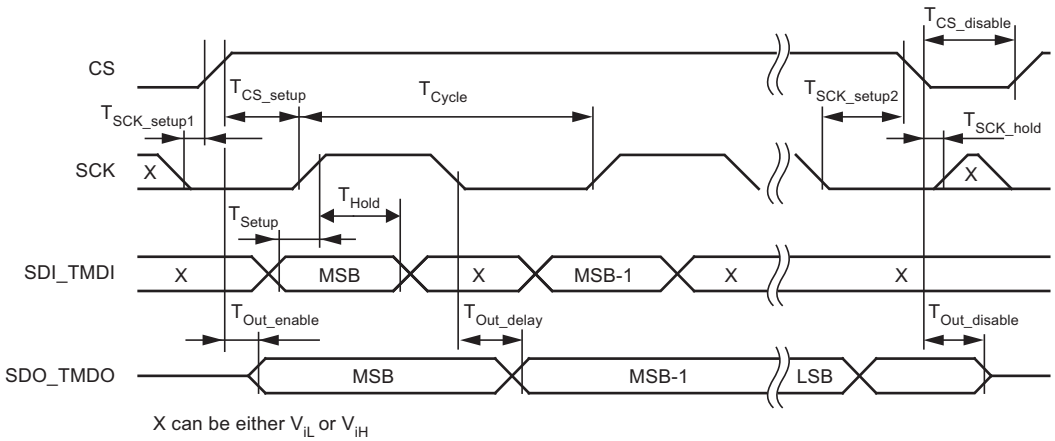
8.8 4-wire Serial Interface

The 4-wire serial interface consists of the Chip Select (CS), the Serial Clock (SCK), the Serial Data Input (SDI_TMDI) and the Serial Data Output (SDO_TMDO). Data is transmitted/received bit by bit in synchronization with the serial clock.

Note: If the output level on pin N_RESET is low, no data communication with the microcontroller is possible.

When CS is low and the transparent mode is inactive (T_MODE = 0), SDO_TMDO is in a high impedance state. When CS is low and the transparent mode is active (T_MODE = 1), the RX data stream is available on pin SDO_TMDO.

Figure 8-7. Serial Timing



9. Operation Modes

9.1 RX Operation

The transceiver is set to RX operation with the bits OPM0 and OPM1 in control register 1.

Table 9-1. Control Register 1

OPM1	OPM0	Function
1	0	RX polling mode
1	1	RX mode

The transceiver is designed to consume less than 1mA in RX operation while remaining sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected does the transceiver remain active and transfer the data to the connected microcontroller. This transfer takes place either via the TX/RX data buffer or via the pin SDO_TMDO. When there is no valid signal present, the transceiver is in sleep mode most of the time, resulting in low current consumption. This condition is called RX polling mode. A connected microcontroller can be disabled during this time.

All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate, etc.

In RX mode the RF transceiver is enabled permanently and the bit-check logic verifies the presence of a valid transmitter signal. When a valid signal is detected the transceiver transfers the data to the connected microcontroller. This transfer take place either via the TX/RX data buffer or via the pin SDO_TMDO.

9.1.1 RX Polling Mode

When the transceiver is in RX polling mode it stays in a continuous cycle of three different modes. In sleep mode the RF transceiver is disabled for the time period T_{Sleep} while consuming low current of $I_S = I_{IDLE\_X}$. During the start-up period, $T_{Startup\_PLL}$ and $T_{Startup\_Sig\_Proc}$, all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit by bit to see if it is a valid transmitter signal. If no valid signal is present, the transceiver is set back to sleep mode after the period $T_{Bit\text{-}check}$. This period varies check by check as it is a statistical process. An average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. During $T_{Startup\_PLL}$ the current consumption is $I_S = I_{Startup\_PLL\_X}$. During $T_{Startup\_Sig\_Proc}$ and $T_{Bit\text{-}check}$ the current consumption is $I_S = I_{RX\_X}$. The condition of the transceiver is indicated on pin RX_ACTIVE (see Figure 9-1 on page 46 and Figure 9-2 on page 47). The average current consumption in RX polling mode I_P is different in 1 Li battery application (3V), 2 Li battery application (6V) or Base-station Application (5V). To calculate I_P the index X must be replaced by VS1,VS2 in 1 Li battery application (3V), VS2 in 2 Li battery application (6V) or VS2,VAUX in Base-station Application (5V) (see section "Electrical Characteristics: General" on page 58).

$$I_P = \frac{I_{IDLE\_X} \times T_{Sleep} + I_{Startup\_PLL\_X} \times T_{Startup\_PLL} + I_{RX\_X} \times (T_{Startup\_Sig\_Proc} + T_{Bitcheck})}{T_{Sleep} + T_{Startup\_PLL} + T_{Startup\_Sig\_Proc} + T_{Bit\_check}}$$

To save current it is recommended that CLK and V_{VSOUT} be disabled during RX polling mode. I_P does not include the current of the Microcontroller_Interface, I_{VSINT}, or the current of an external device connected to pin VSOUT (for example, microcontroller). If CLK and/or VSOUT is enabled during RX polling mode the current consumption is calculated as follows:

$$I_{S\_Poll} = I_P + I_{VSINT} + I_{EXT}$$

During T_{Sleep}, $T_{Startup\_PLL}$ and $T_{Startup\_Sig\_Proc}$, the transceiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command, the transmitter must start the telegram with an adequate preburst. The required length of the preburst, $T_{Preburst}$, depends on the polling parameters T_{Sleep}, $T_{Startup\_PLL}$, $T_{Startup\_Sig\_Proc}$ and $T_{Bit\text{-}check}$. Thus, $T_{Bit\text{-}check}$ depends on the actual bit rate and the number of bits ($N_{Bit\text{-}check}$) to be tested.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup\_PLL} + T_{Startup\_Sig\_Proc} + T_{Bit\_check}$$

9.1.2 Sleep Mode

The length of period T_{Sleep} is defined by the 5-bit word sleep in control register 4, the extension factor X_{Sleep} defined by the bit X_{Sleep} in control register 4, and the basic clock cycle T_{DCLK}. It is calculated to be:

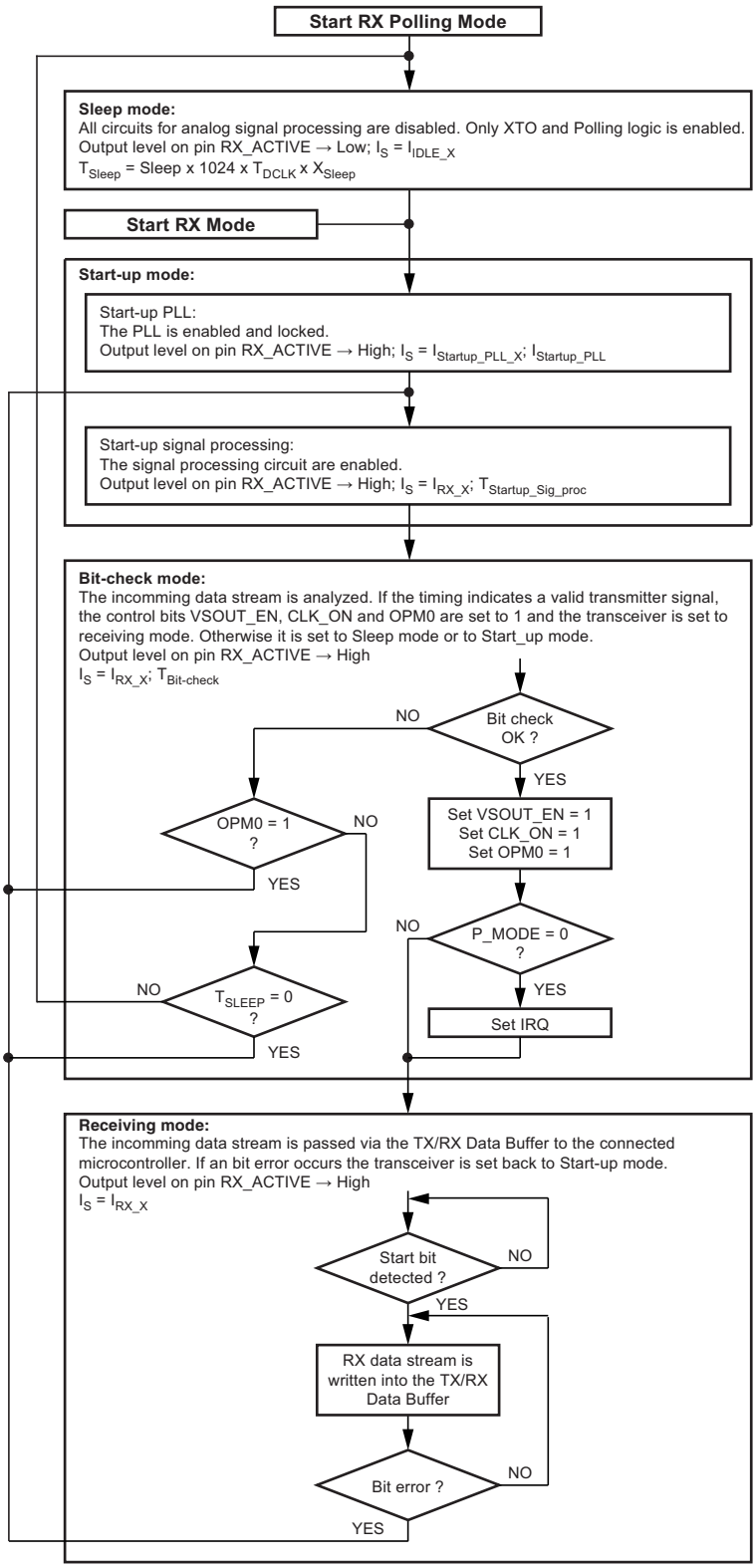
$$T_{Sleep} = Sleep \times 1024 \times T_{DCLK} \times X_{Sleep}$$

In US and European applications, the maximum value of T_{Sleep} is about 38ms if X_{Sleep} is set to 1 (which is done by setting the bit X_{Sleep} in control register 4 to "0"). The time resolution is about 1.2ms in that case. The sleep time can be extended to about 300ms by setting X_{Sleep} to 8 (which is done by setting X_{Sleep} in control register 4 to "1"), the time resolution is then about 9.6ms.

9.1.3 Start-up Mode

During $T_{Startup\_PLL}$ the PLL is enabled and starts up. If the PLL is locked, the signal processing circuit starts up ($T_{Startup\_Sig\_Proc}$). After the start-up time all circuits are in stable condition and ready to receive.

Figure 9-1. Flow Chart Polling Mode/RX Mode (T_MODE = 0, Transparent Mode Inactive)



Sleep: Defined by bits Sleep 0 to Sleep 4 in Control Register 4

X_{Sleep}: Defined by bit XSleep in Control register 4

T_{DCLK}: Basic clock cycle

$T_{Startup\_PLL}$: 798.5 x T_{DCLK} (typ)

$T_{Startup\_Sig\_Proc}$:

882 x T_{DCLK}	(BR_Range 0)
498 x T_{DCLK}	(BR_Range 1)
306 x T_{DCLK}	(BR_Range 2)
210 x T_{DCLK}	(BR_Range 3)

Is defined by the selected baud rate range and T_{DCLK} .The baud-rate range is defined by bit Baud 0 and Baud 1 in Control Register 6.

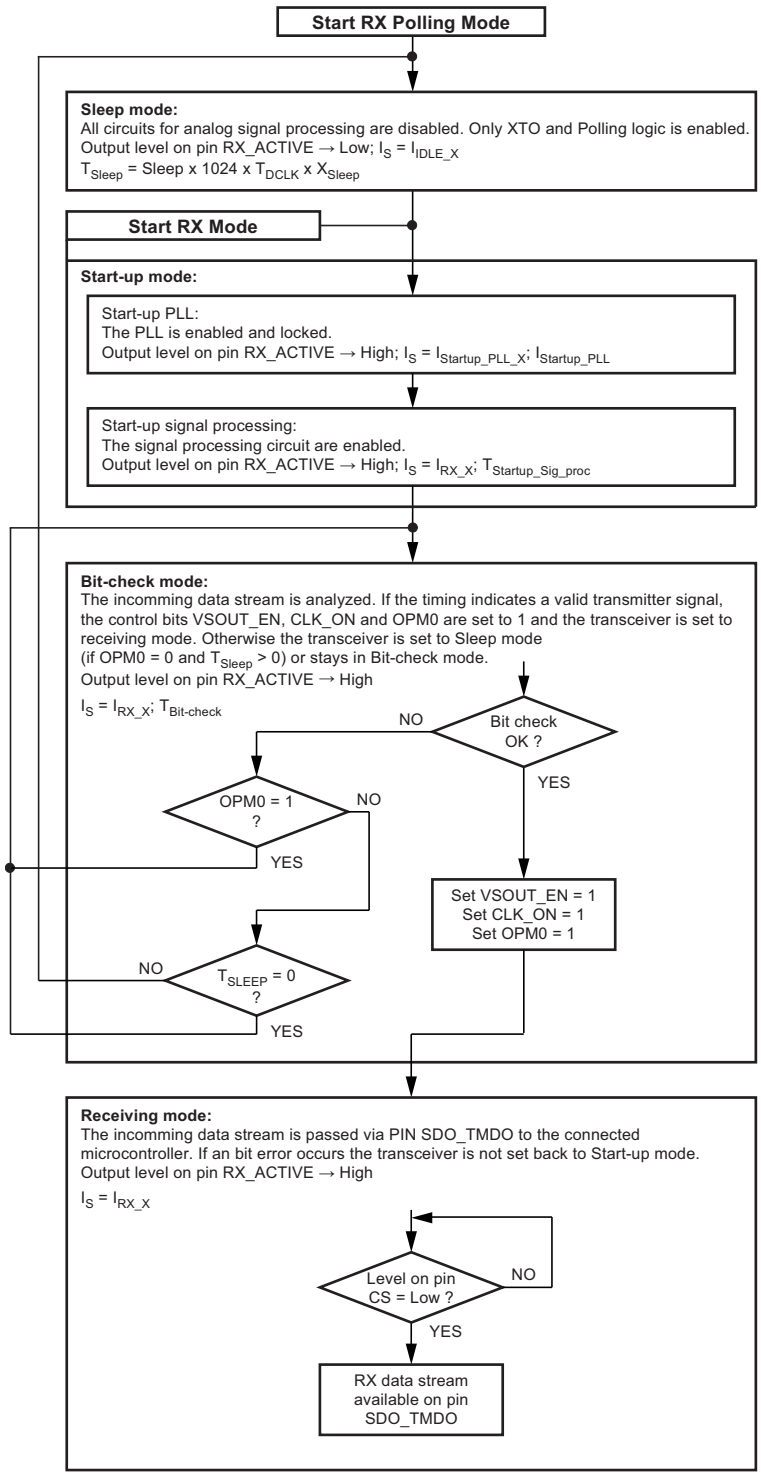
$T_{Bit\text{-}check}$: Depends on the result of the bit check.

If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}check}$) and on the utilized data rate.

If the bit check fails, the average time period for that check despends on the selected bit-rate range and on T_{XDCLK}. The bit-rate range is defined by bit Baud 0 and Baud 1 in Control Register 6.

If the transceiver detects a bit errror after a successful bit check and before the start bit is detected pin IRQ will be set to high (only if P_MODE = 0) and the transceiver is set back to start-up mode.

Figure 9-2. Flow Chart Polling Mode/RX Mode (T_MODE = 1, Transparent Mode Active)



Sleep: Defined by bits Sleep 0 to Sleep 4 in Control Register 4

X_{Sleep}: Defined by bit XSleep in control register 4

T_{DCLK}: Basic clock cycle

$T_{Startup\_PLL}$: 798.5 x T_{DCLK} (typ)

$T_{Startup\_Sig\_Proc}$:

882 x T_{DCLK}	(BR_Range 0)
498 x T_{DCLK}	(BR_Range 1)
306 x T_{DCLK}	(BR_Range 2)
210 x T_{DCLK}	(BR_Range 3)

Is defined by the selected baud rate range and T_{DCLK} .The baud-rate range is defined by bit Baud 0 and Baud 1 in Control Register 6.

$T_{Bit\text{-}check}$: Depends on the result of the bit check.

If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}check}$) and on the utilized data rate.

If the bit check fails, the average time period for that check despends on the selected bit-rate range and on T_{XDCLK}. The bit-rate range is defined by bit Baud 0 and Baud 1 in Control Register 6.

If in FSK mode the datastream is interrupted the FSK-Demodulator-PLL tends to lock out and is further not able to lock in, even there is a valid data stream available.
In this case the transceiver must be set back to IDLE mode.

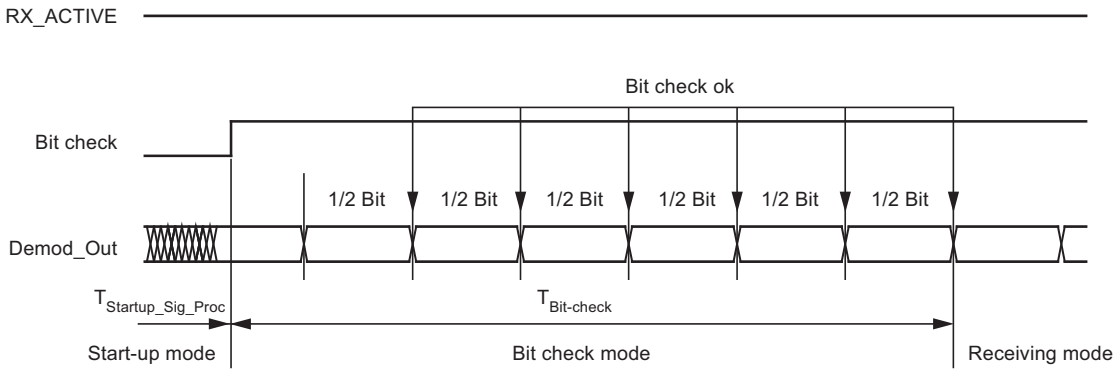
9.1.4 Bit-check Mode

In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distance between 2 signal edges are continuously compared to a programmable time window. The maximum count of this edge-to-edge test before the transceiver switches to receiving mode is also programmable.

9.1.5 Configuration of the Bit Check

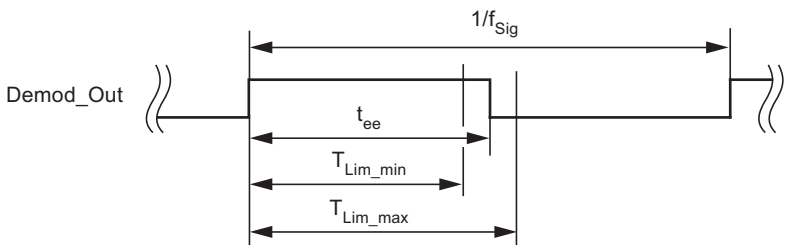
Assuming a modulation scheme that contains two edges per bit, two time frame checks verify one bit. This is valid for Manchester, Bi-phase and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable $N_{Bit\text{-}check}$ in control register 5. This implies 0, 6, 12 and 18 edge-to-edge checks, respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the transceiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In RX polling mode, the bit-check time is not dependent on $N_{Bit\text{-}check}$ if no valid signal is present. Figure 9-3 shows an example where three bits are tested successfully.

Figure 9-3. Timing Diagram for Complete Successful Bit Check (Number of Checked Bits: 3)



As seen in Figure 9-4, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time t_{ee} is in between the lower bit-check limit T_{Lim_min} and the upper bit-check limit T_{Lim_max}, the check will be continued. If t_{ee} is smaller than limit T_{Lim_min} or exceeds T_{Lim_max}, the bit check will be terminated and the transceiver switches to sleep mode.

Figure 9-4. Valid Time Window for Bit Check



For the best noise immunity, use of a low span between T_{Lim_min} and T_{Lim_max} is recommended. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst: a “11111...” or a “10101...” sequence in Manchester or Bi-phase is a good choice. A good compromise between sensitivity and susceptibility to noise regarding the expected edge-to-edge time, t_{ee}, is a time window of ±38%; to get the maximum sensitivity the time window should be ±50% and then $N_{Bit\text{-}check} \geq 6$. Using preburst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below:

$$T_{Lim\_min} = Lim\_min \times T_{XDCLK}$$
$$T_{Lim\_max} = (Lim\_max\ -1) \times T_{XDCLK}$$

Lim_min is defined by the bits Lim_min 0 to Lim_min 5 in control register 5.

Lim_max is defined by the bits Lim_max 0 to Lim_max 5 in control register 6.

Using the above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XDCLK}. The time resolution defining T_{Lim_min} and T_{Lim_max} is T_{XDCLK}. The minimum edge-to-edge time t_{ee} is defined in the section “Receiving Mode” on page 51. The lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

Figure 9-5, Figure 9-6 on page 50, and Figure 9-7 on page 50 illustrate the bit check for the bit-check limits Lim_min = 14 and Lim_max = 24. The signal processing circuits are enabled during $T_{Startup\_PLL}$ and $T_{Startup\_Sig\_Proc}$. The output of the ASK/FSK demodulator (Demod_Out) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle T_{XDCLK}.

Figure 9-5 shows how the bit check proceeds if the bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In Figure 9-6 on page 50 the bit check fails because the value CV_Lim is lower than the limit Lim_min. The bit check also fails if CV_Lim reaches Lim_max. This is illustrated in Figure 9-7 on page 50.

Figure 9-5. Timing Diagram During Bit Check

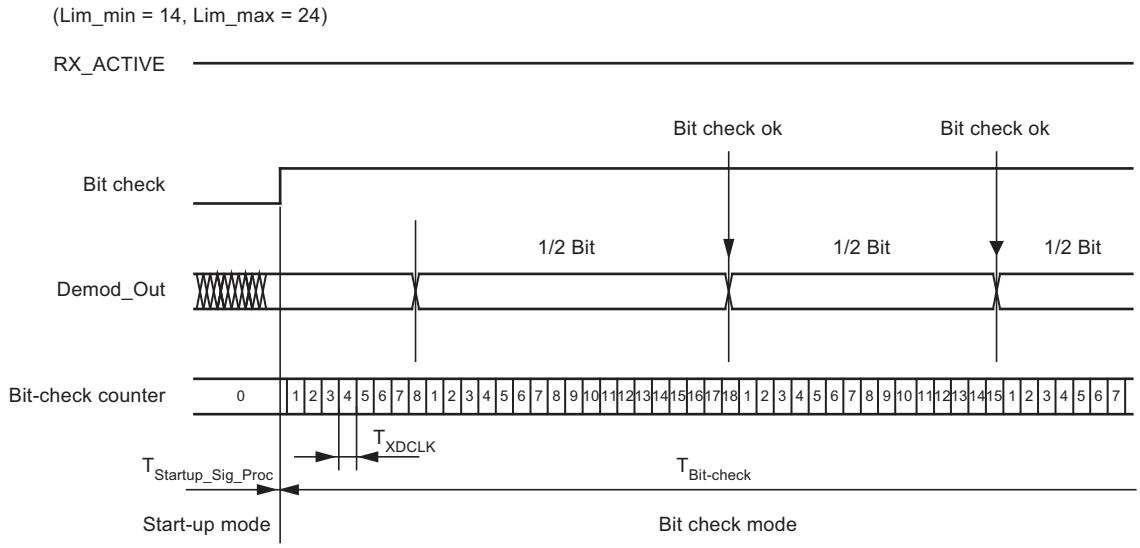


Figure 9-6. Timing Diagram for Failed Bit Check (Condition CV_Lim < Lim_min)

(Lim_min = 14, Lim_max = 24)

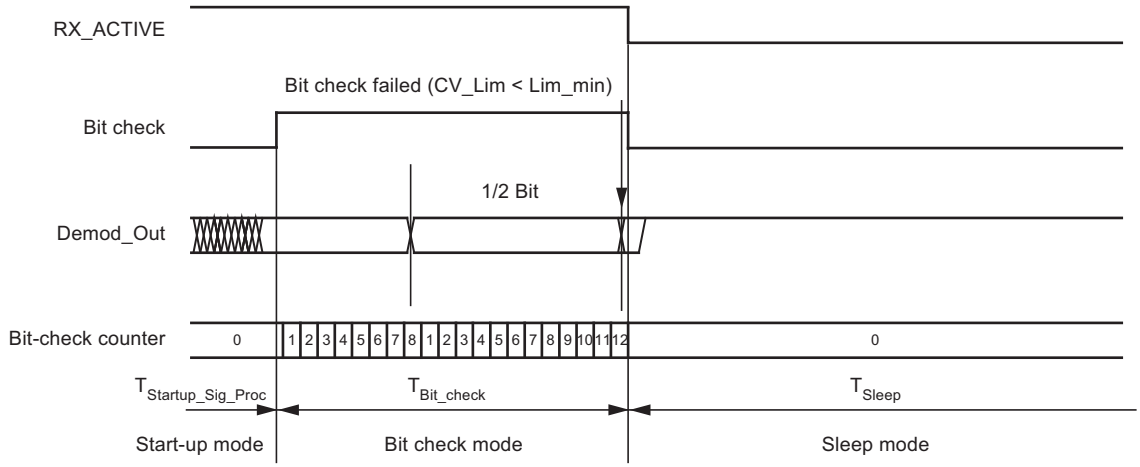
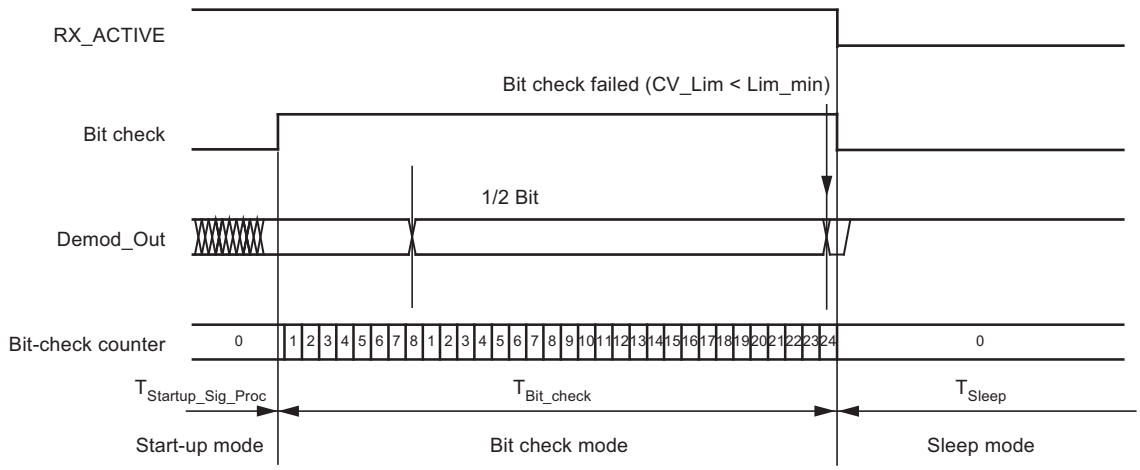


Figure 9-7. Timing Diagram for Failed Bit Check (Condition: CV_Lim ≥ Lim_max)

(Lim_min = 14, Lim_max = 24)



9.1.6 Duration of the Bit Check

If no transmitter is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected bit-rate range and on T_{XDCLK}. A higher bit-rate range causes a lower value for $T_{Bit\text{-}check}$, resulting in a lower current consumption in RX polling mode.

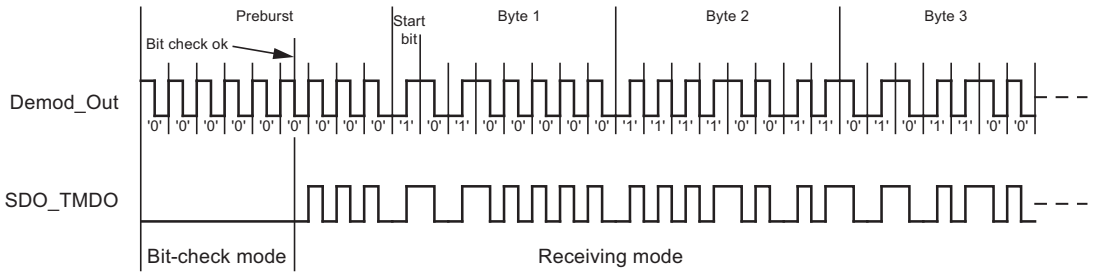
In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, f_{Signal}, and the count of the bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ therefore results in a longer period for $T_{Bit\text{-}check}$, requiring a higher value for the transmitter pre-burst, $T_{Preburst}$.

9.1.7 Receiving Mode

If the bit check was successful for all bits specified by $N_{Bit\text{-}check}$, the transceiver switches to receiving mode. To activate a connected microcontroller, the bits VSOUT_EN and CLK_ON in control register 3 are set to “1”. An interrupt is issued at pin IRQ if the control bits T_MODE = 0 and P_MODE = 0.

If the transparent mode is active (T_MODE = 1) and the level on pin CS is low (no data transfer via the serial interface), the RX data stream is available on pin SDO_TMDO (Figure 9-8).

Figure 9-8. Receiving Mode (TMODE = 1)



If the transparent mode is inactive (T_MODE = 0), the received data stream is buffered in the TX/RX data buffer (see Figure 9-9 on page 52). The TX/RX data buffer is only usable for Manchester and Bi-phase coded signals. It is always possible to transfer the data from the data buffer via the 4-wire serial interface to a microcontroller (see Figure 8-1 on page 41).

Buffering of the data stream:

After a successful bit check, the transceiver switches from bit-check mode to receiving mode. In receiving mode the TX/RX data buffer control logic is active and examines the incoming data stream. This is done, as in the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window as illustrated in Figure 9-9 on page 52. Only two time differences between two edges in Manchester and Bi-phase coded signals are valid (T and 2T).

The limits for T are the same as used for the bit check. They can be programmed in control register 5 and 6 (Lim_min, Lim_max).

The limits for 2T are calculated as follows:

Lower limit of 2T:

$$Lim\_min\_2T = (Lim\_min + Lim\_max) - (Lim\_max - Lim\_min)/2$$

$$T_{Lim\_min\_2T} = Lim\_min\_2T \times T_{XDCLK}$$

Upper limit of 2T:

$$Lim\_max\_2T = (Lim\_min + Lim\_max) + (Lim\_max - Lim\_min)/2$$

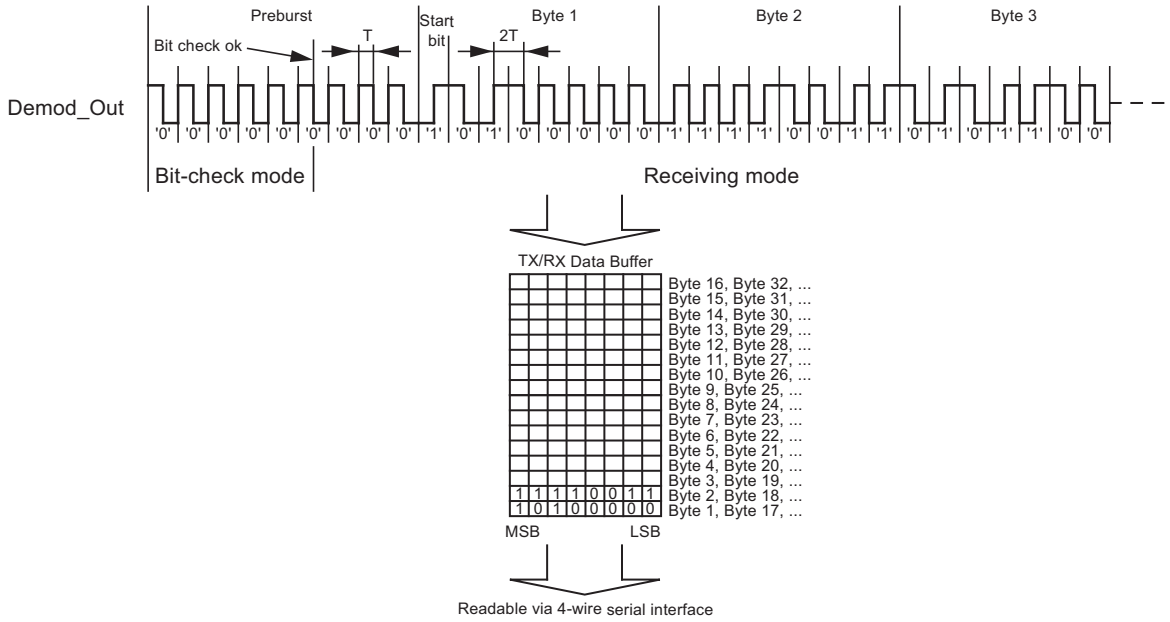
$$T_{Lim\_max\_2T} = (Lim\_max\_2T - 1) \times T_{XDCLK}$$

If the result of Lim_min_2T or Lim_max_2T is not an integer value, it will be rounded up.

If the TX/RX data buffer control logic detects the start bit, the data stream is written in the TX/RX data buffer byte by byte. The start bit is part of the first data byte and must be different from the bits of the preburst. If the preburst consists of a sequence of “00000...”, the start bit must be a “1”. If the preburst consists of a sequence of “11111...”, the start bit must be a “0”.

If the data stream consists of more than 16 bytes, a buffer overflow occurs and the TX/RX data buffer control logic overwrites the bytes already stored in the TX/RX data buffer. Therefore, it is very important to ensure that the data is read in time so that no buffer overflow occurs (see Figure 8-1 on page 41). There is a counter that indicates the number of received bytes in the TX/RX data buffer (see section “Transceiver Configuration” on page 41). If a byte is transferred to the microcontroller, the counter is decremented; if a byte is received, the counter is incremented. The counter value is available via the 4-wire serial interface. An interrupt is issued if the counter (while counting up) reaches the value defined by the control bits IR0 and IR1 in control register 1.

Figure 9-9. Receiving Mode (TMODE = 0)



If the TX/RX data buffer control logic detects a bit error, an interrupt is issued and the transceiver is set back to the start-up mode (see Figure 9-1 on page 46, Figure 9-2 on page 47 and Figure 9-10).

Bit error: a) $t_{ee} < T_{Lim\_min}$ or $T_{Lim\_max} < t_{ee} < T_{Lim\_min\_2T}$ or $t_{ee} > T_{Lim\_max\_2T}$
b) Logical error (no edge detected in the bit center)

Note: The byte consisting of the bit error will not be stored in the TX/RX data buffer. Thus, it is not available via the 4-wire serial interface.

Writing the control register 1, 4, 5 or 6 during receiving mode resets the TX/RX data buffer control logic and the counter which indicates the number of received bytes. If the bits OPM0 and OPM1 are still “1” after writing to a control register, the transceiver changes to the start-up mode (start-up signal processing).

Figure 9-10. Bit Error (TMODE = 0)

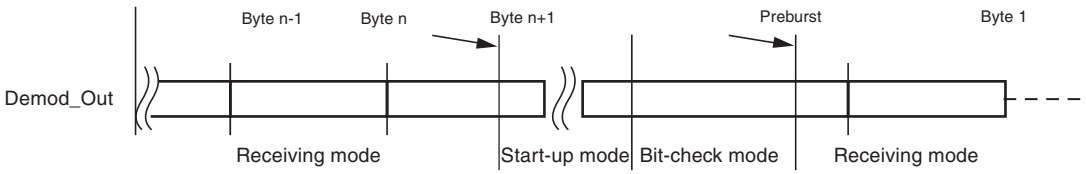


Table 9-2. RX Modulation Scheme

Mode	ASK/_NFSK	T_MODE	RF_{IN}	Bit in TX/RX Data Buffer	Level on Pin SD0_TMDO
RX	0	0	$f_{FSK\_L} \rightarrow f_{FSK\_H}$	1	X
		0	$f_{FSK\_H} \rightarrow f_{FSK\_L}$	0	X
		1	f_{FSK_H}	–	1
		1	f_{FSK_L}	–	0
	1	0	f_{ASK} off $\rightarrow$ f_{ASK} on	1	X
		0	f_{ASK} on $\rightarrow$ f_{ASK} off	0	X
		1	f_{ASK} on	–	1
		1	f_{ASK} off	–	0

9.1.8 Recommended Lim_min and Lim_max for Maximum Sensitivity

The sensitivity measurements in the section “Low-IF Receiver” in Table 3-3 on page 11 and Table 3-4 on page 11 have been done with the Lim_min and Lim_max values according to Table 9-3. These values are optimized for maximum sensitivity. Note that since these limits are optimized for sensitivity, the number of checked bits, $N_{Bit\text{-}check}$, has to be at least 6 to prevent the circuit from waking up to often in polling mode due to noise.

Table 9-3. Recommended Lim_min and Lim_max Values for Different Bit Rates

f_{RF} (f_{XTAL})/ MHz	1.0Kbit/s BR_Range_0 XLim = 1	2.4Kbit/s BR_Range_0 XLim = 0	5Kbit/s BR_Range_1 XLim = 0	10Kbit/s BR_Range_2 XLim = 0	20Kbit/s BR_Range_3 XLim = 0
433.92 (13.25311)	Lim_min = 13 (251µs) Lim_max = 38 (715µs)	Lim_min = 12 (116µs) Lim_max = 34 (319µs)	Lim_min = 11 (53µs) Lim_max = 32 (150µs)	Lim_min = 11 (27µs) Lim_max = 32 (75µs)	Lim_min = 11 (13µs) Lim_max = 32 (37µs)
868.3 (13.41191)	Lim_min = 13 (248µs) Lim_max = 38 (706µs)	Lim_min = 12 (115µs) Lim_max = 34 (315µs)	Lim_min = 11 (52µs) Lim_max = 32 (148µs)	Lim_min = 11 (26µs) Lim_max = 32 (74µs)	Lim_min = 11 (13µs) Lim_max = 32 (37µs)

9.2 TX Operation

The transceiver is set to TX operation by using the bits OPM0 and OPM1 in the control register 1.

Table 9-4. Control Register 1

OPM1	OPM0	Function
0	1	TX mode

Before activating TX mode, the TX parameters (bit rate, modulation scheme, etc.) must be selected as illustrated in Figure 9-11 on page 54. The bit rate depends on Baud 0 and Baud 1 in control register 6, Lim_min0 to Lim_min5 in control register 5 and XLIM in control register 4 (see section “Control Register” on page 31). The modulation is selected with ASK/_NFSK in control register 4. The FSK frequency deviation is fixed to about ±16kHz. If P_Mode is set to “1”, the Manchester modulator is disabled and pattern mode is active (NRZ, see Table 9-5 on page 56).

After the transceiver is set to TX mode, the start-up mode is active and the PLL is enabled. If the PLL is locked, the TX mode is active.

If the transceiver is in start-up or TX mode, the TX/RX data buffer can be loaded via the 4-wire serial interface. After the first byte is in the buffer and the TX mode is active, the transceiver starts transmitting automatically (beginning with the MSB). While transmitting it is always possible to load new data in the TX/RX data buffer. To prevent a buffer overflow or interruptions during transmitting, the user must ensure that data is loaded at the same speed as it is transmitted.

There is a counter that indicates the number of bytes to be transmitted (see section “Transceiver Configuration” on page 41). If a byte is loaded, the counter is incremented, if a byte is transmitted, the counter is decremented. The counter value is available via the 4-wire serial interface. An IRQ is issued if the counter (while counting down) reaches the value defined by the control bits IR0 and IR1 in control register 1.

Note: Writing to the control register 1, 4, 5 or 6 during TX mode resets the TX/RX data buffer and the counter which indicates the number of bytes to be transmitted.

If T_Mode in control register 1 is set to “1”, the transceiver is in TX transparent mode. In this mode the TX/RX data buffer is disabled and the TX data stream must be applied on pin SDI_TMDI. Figure 9-11 on page 54 illustrates the flow chart of the TX transparent mode.

Figure 9-11. TX Operation (T_MODE = 0)

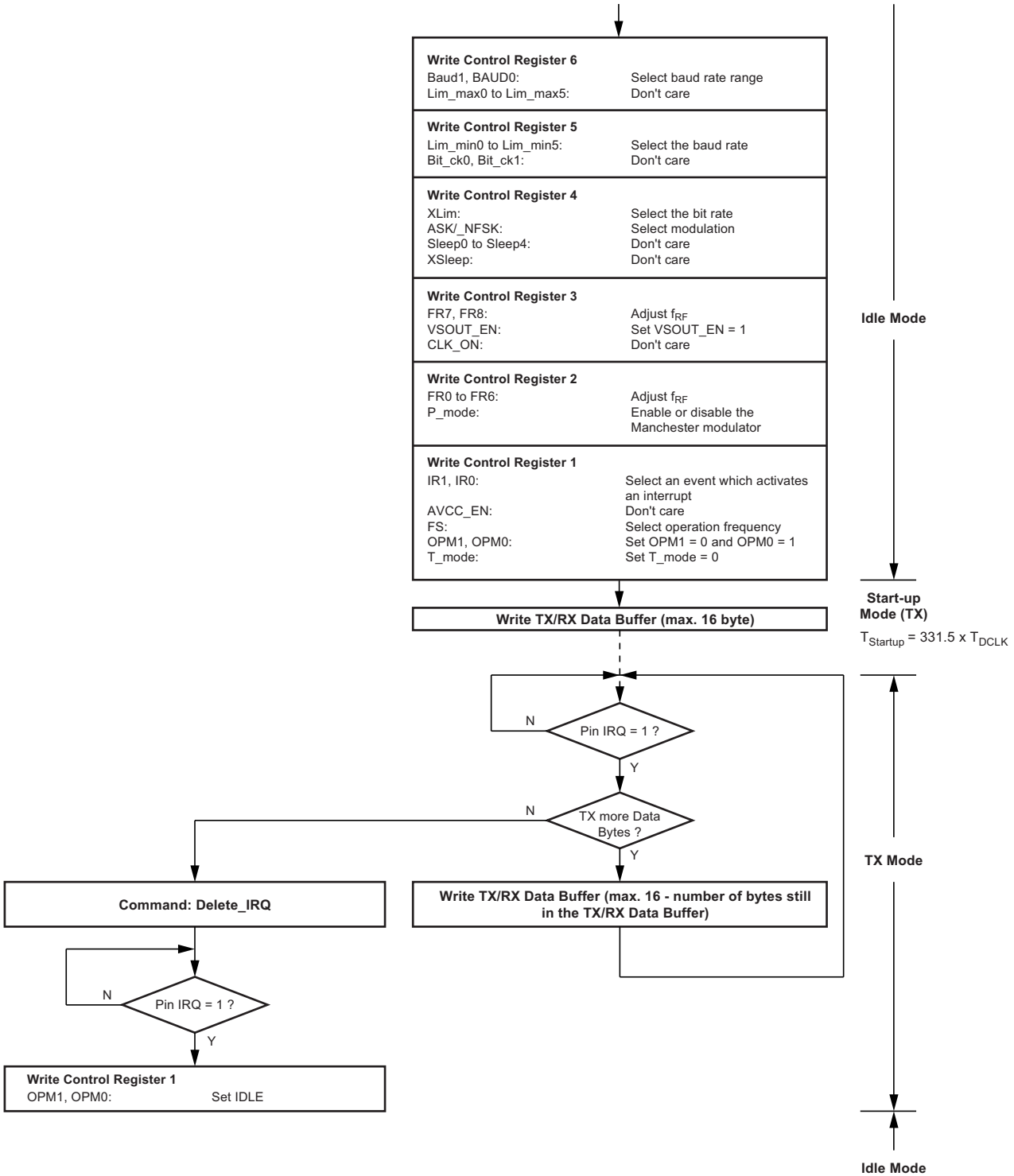


Figure 9-12. TX Transparent Mode (T_MODE = 1)

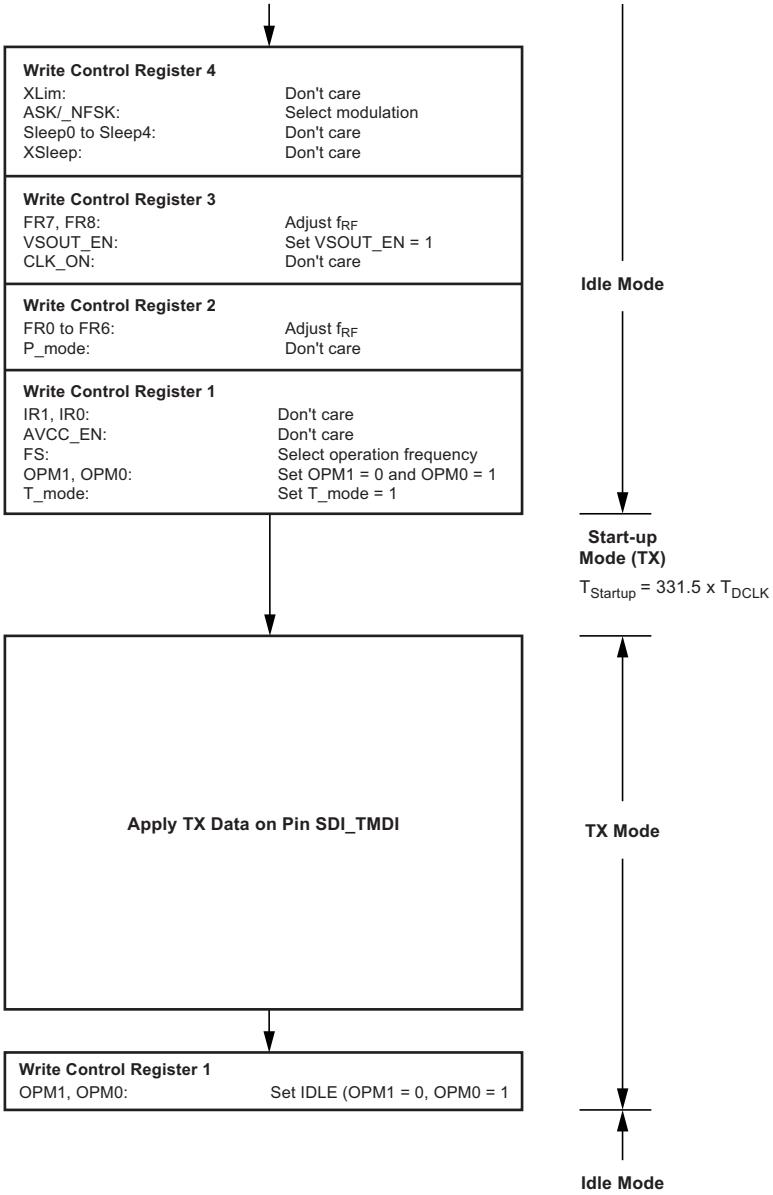


Table 9-5. TX Modulation Schemes

Mode	ASK/_NFSK	P_Mode	T_Mode	Bit in TX/RX Data Buffer	Level on Pin SDI_TMDI	RF_{OUT}
TX	0	0	0	1	X	$f_{FSK\_L} \rightarrow f_{FSK\_H}$
		0	0	0	X	$f_{FSK\_H} \rightarrow f_{FSK\_L}$
		1	0	1	X	f_{FSK_H}
		1	0	0	X	f_{FSK_L}
		X	1	X	1	f_{FSK_H}
		X	1	X	0	f_{FSK_L}
	1	0	0	1	X	f_{ASK} off $\rightarrow$ f_{ASK} on
		0	0	0	X	f_{ASK} on $\rightarrow$ f_{ASK} off
		1	0	1	X	f_{ASK} on
		1	0	0	X	f_{ASK} off
		X	1	X	1	f_{ASK} on
		X	1	X	0	f_{ASK} off

9.3 Interrupts

Via pin IRQ, the transceiver signals different operating conditions to a connected microcontroller. If a specific operating condition occurs, pin IRQ is set to high.

If an interrupt occurs, it is recommended to delete the interrupt immediately by reading the status register, so that a further potential interrupt doesn't get lost. If the Interrupt pin doesn't switch to low by reading the status register, the interrupt was triggered by the RX/TX data buffer. In this case read or write the RX/TX data buffer according to Table 9-6.

Table 9-6. Interrupt Handling

Operating Conditions Which Set Pin IRQ to High Level	Operations Which Set Pin IRQ to Low Level
Events in Status Register	
State transition of status bit STn (0 → 1; 1 → 0)	Read status register or Command Delete IRQ
Appearance of status bit Power_On (0 → 1)	
Appearance of status bit P_On_Aux (0 → 1)	
Events During TX Operation (T_MODE = 0)	
4, 8 or 12 Bytes are in the TX data buffer or the TX data buffer is empty (depends on IR0 and IR1 in control register 1).	Write TX data buffer or Write control register 1 or Write control register 4 or Write control register 5 or Write control register 6 or Command delete IRQ
Events During RX Operation (T_MODE = 0)	
4, 8 or 12 received bytes are in the RX data buffer or a receiving error is occurred (depends on IR0 and IR1 in control register 1).	Read RX data buffer(1) or Write control register 1 or Write control register 4 or Write control register 5 or Write control register 6 or Command delete IRQ
Successful bit check (P_MODE = 0)	

Note: 1. During reading of the RX/TX buffer, no IRQ is issued, due to the received bytes or a receiving error.

10. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	–55	+125	°C
Ambient temperature	T_{amb}	–40	+85	°C
Supply voltage VS2	V_{MaxVS2}	–0.3	+7.2	V
Supply voltage VS1	V_{MaxVS1}	–0.3	+4	V
Supply voltage VAUX	$V_{MaxVAUX}$	–0.3	+7.2	V
Supply voltage VSINT	$V_{MaxVSINT}$	–0.3	+5.5	V
ESD (Human Body Model ESD S 5.1) every pin	HBM	–1.5	+1.5	kV
ESD (Machine Model JEDEC A115A) every pin	MM	–200	+200	V
ESD (Field Induced Charge Device Model ESD STM 5.3.1–1999) every pin	FCDM	–1	+1	kV
Maximum input level, input matched to 50Ω	P_{in_max}		10	dBm

11. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	25	K/W

12. Electrical Characteristics: General

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RtX_TX_IDLE Mode								
1.1	RF operating frequency range	ATA5428 V_{433_N868} = AVCC	4, 10	f_{RF}	431.5		436.5	MHz	A
		ATA5428 V_{433_N868} = GND	4, 10	f_{RF}	862		872	MHz	A
1.2	Supply current OFF mode	V_{VS1} = V_{VS2} = 3V, V_{VSINT} = 0V (1 battery) and V_{VS2} = 6V (2 battery) OFF mode is not available if V_{VS2} = V_{VAUX} = 5V V_{VSINT} = 0V (base station)		I_{S_OFF}		< 10		nA	A
1.3	Supply current IDLE mode	V_{VSOUT} disabled, XTO running V_{VS1} = V_{VS2} = 3V (1 battery)		I_{S_IDLE}		220		µA	B
		V_{VS2} = 6V (2 battery)		I_{S_IDLE}		310		µA	B
		V_{VS2} = V_{VAUX} = 5V (base station)		I_{S_IDLE}		310		µA	B
1.4	System start-up time	From OFF mode to IDLE mode including reset and XTO start-up (see Figure 7-4 on page 39) XTAL: C_m = 5fF, C_0 = 1.8pF, R_m =15Ω		$T_{PWR\_ON\_IRQ\_1}$		0.3		ms	C
1.5	RX start-up time	From IDLE mode to receiving mode $N_{Bit\text{-}check}$ = 3 Bit rate = 20Kbit/s, BR_Range_3 (see Figure 9-1 on page 46, Figure 9-2 on page 47 and Figure 9-3 on page 48)		$T_{Startup\_PLL}$ + $T_{Startup\_Sig\_Proc}$ + $T_{Bit\text{-}chek}$		1.39		ms	A
1.6	TX start-up time	From IDLE mode to TX mode (see Figure 9-11 on page 54)		$T_{Startup}$		0.4		ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

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No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2	Receiver/RX Mode								
2.1	Supply current RX mode	f_{RF} = 433.92MHz	17, 18	I_{S_RX}		10.5		mA	A
		f_{RF} = 868MHz	17, 18	I_{S_RX}		10.3		mA	A
2.2	Supply current RX polling mode	T_{Sleep} = 49.45ms X_{SLEEP} = 8, Sleep = 5 Bit rate = 20Kbit/s FSK, V_{VSOUT} disabled	17, 18	I_P		444		µA	B
2.3	Input sensitivity FSK f_{RF} = 433.92MHz	FSK deviation f_{DEV} = ±16kHz limits according to Table 9-3 on page 53, BER = 10^{-3} T_{amb} = 25°C							
		Bit rate 20Kbit/s	(4)	P_{REF_FSK}	–104.0	–106.0	–107.5	dBm	B
		Bit rate 2.4bit/s	(4)	P_{REF_FSK}	–107.5	–109.5	–111.0	dBm	B
2.4	Input sensitivity ASK f_{RF} = 433.92MHz	ASK 100%, level of carrier limits according to Table 9-3 on page 53, BER = 10^{-3} T_{amb} = 25°C							
		Bit rate 10Kbit/s	(4)	P_{REF_ASK}	–110.5	–112.5	–114.0	dBm	B
		Bit rate 2.4Kbit/s	(4)	P_{REF_ASK}	–114.5	–116.5	–118.0	dBm	B
2.5	Sensitivity change at f_{RF} = 868.3MHz compared to f_{RF} = 433.92MHz	f_{RF} = 433.92 MHz to f_{RF} = 868.3 MHz $P = P_{REF\_ASK} + \Delta P_{REF1} + \Delta P_{REF2}$ $P = P_{REF\_FSK} + \Delta P_{REF1} + \Delta P_{REF2}$	(4)	ΔP_{REF1}		+2.7		dB	B
2.6	Maximum frequency offset in FSK mode	Maximum frequency difference of f_{RF} between receiver and transmitter in FSK mode (f_{RF} is the center frequency of the FSK signal with f_{DEV} = ±16kHz)	(4)	Δf_{OFFSET}	–58		+58	kHz	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

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No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2.7	Supported FSK frequency deviation	With up to 2dB loss of sensitivity. Note that the tolerable frequency offset is for f_{DEV} = ±22kHz, 6kHz lower than for f_{DEV} = ±16kHz hence Δf_{OFFSET} ≤ ±52kHz	(4)	f_{DEV}	±14	±16	±22	kHz	B
2.8	System noise figure	f_{RF} = 433.92MHz	(4)	NF		7.0		dB	B
		f_{RF} = 868.3MHz	(4)	NF		9.7		dB	B
2.9	Intermediate frequency	f_{RF} = 433.92MHz		f_{IF}		223		kHz	A
		f_{RF} = 868.3MHz		f_{IF}		226		kHz	A
2.10	System bandwidth	This value is for information only! Note that for crystal and system frequency offset calculations, Δf_{OFFSET} must be used.	(4)	SBW		185		kHz	A
2.11	System outband 2nd-order input intercept point with respect to f_{IF}	Δf_{meas1} = 1,800MHz Δf_{meas2} = 2,026MHz $f_{IF} = \Delta f_{meas2} - \Delta f_{meas1}$	(4)	IIP2		+50		dBm	C
2.12	System outband 3rd-order input intercept point	Δf_{meas1} = 1.8MHz Δf_{meas2} = 3.6MHz f_{RF} = 433.92MHz	(4)	IIP3		–21		dBm	C
		f_{RF} = 868.3MHz	(4)	IIP3		–17		dBm	C
2.13	System outband input 1dB compression point	Δf_{meas1} = 1MHz f_{RF} = 433.92MHz	(4)	I1dBCP		–30		dBm	C
		f_{RF} = 868.3MHz	(4)	I1dBCP		–27		dBm	C
2.14	LNA input impedance	f_{RF} = 433.92MHz	4	Z_{in_LNA}		(32 – j169)		Ω	C
		f_{RF} = 868.3MHz	4	Z_{in_LNA}		(21 – j78)		Ω	C
2.15	Allowable peak RF input level, ASK and FSK	BER < 10^{-3}, ASK: 100%	(4)	P_{IN_max}		+10	–10	dBm	C
		FSK: f_{DEV} = ±16kHz	(4)	P_{IN_max}		+10	–10	dBm	C
2.16	LO spurious emission at LNA_IN	f < 1GHz	(4)				–57	dBm	C
		f >1GHz	(4)				–47	dBm	C
		f_{RF} = 433.92MHz	(4)			–97		dBm	C
		f_{RF} = 868.3MHz	(4)			–84		dBm	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

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No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2.17	Image rejection	Within the complete image band	(4)		20	30		dB	A
2.18	Useful signal to interfering signal ratio	Peak level of useful signal to peak level of interferer for BER < 10^{-3} with any modulation scheme of interferer							
		FSK BR_Ranges 0, 1, 2	(4)	SNR_{FSK0-2}		2	3	dB	B
		FSK BR_Range_3	(4)	SNR_{FSK3}		4	6	dB	B
		ASK (P_{RF} < P_{RFIN_High})	(4)	SNR_{ASK}		10	12	dB	B
2.19	RSSI output	Dynamic range	(4), 36	D_{RSSI}		70		dB	A
		Lower level of range f_{RF} = 433.92MHz f_{RF} = 868.3MHz	(4), 36	P_{RFIN_Low}		 –115 –112		 dBm dBm	A
		Upper level of range f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz	(4), 36	P_{RFIN_High}		 –45 –42		 dBm dBm	A
		Gain	(4), 36		5.5	8.0	10.5	mV/dB	A
		Output voltage range	(4), 36	OV_{RSSI}	400		1100	mV	A
2.20	Output resistance RSSI pin	RX mode TX mode	36	R_{RSSI}	8 32	10 40	12.5 50	kΩ	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2.21	Blocking	Sensitivity (BER = 10^{-3}) is reduced by 6dB if a continuous wave blocking signal at ±Δf is ΔP_{Block} higher than the useful signal level (bit rate = 20 bit/s, FSK, f_{DEV} ±16kHz, Manchester code)							
		f_{RF} = 433.92MHz Δf ±0.75MHz Δf ±1.0MHz Δf ±1.5MHz Δf ±5MHz Δf ±10MHz	(4)	ΔP_{Block}		55 59 62 68 70		dBC	C
		f_{RF} = 868.3MHz Δf ±0.75MHz Δf ±1.0MHz Δf ±1.5MHz Δf ±5MHz Δf ±10MHz	(4)	ΔP_{Block}		50 53 57 67 69		dBC	C
2.22	CDEM	Capacitor connected to pin 37 (CDEM)	37		–5%	15	+5%	nF	D
3	Power Amplifier/TX Mode								
3.1	Supply current TX mode power amplifier OFF	f_{RF} = 868.3MHz		$I_{S\_TX\_PAOFF}$		6.50		mA	A
		f_{RF} = 433.92MHz		$I_{S\_TX\_PAOFF}$		6.95		mA	A
3.2	Output power 1	V_{VS1} = V_{VS2} = 3V T_{amb} = 25°C V_{PWR_H} = 0V f_{RF} = 433.92MHz R_{R_PWR} = 56kΩ R_{Lopt} = 2.3kΩ f_{RF} = 868.3MHz R_{R_PWR} = 30kΩ R_{Lopt} = 1.3kΩ RF_OUT matched to R_{Lopt} // $j/(2 \times \pi \times f_{RF} \times 1.0pF)$	(10)	P_{REF1}	–2.5	0	+2.5	dBm	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
3.3	Supply current TX mode power amplifier ON 1	PA on/0 dBm							
		f_{RF} = 433.92 MHz	17, 18	$I_{S\_TX\_PAON1}$		8.6		mA	B
		f_{RF} = 868.3 MHz	17, 18	$I_{S\_TX\_PAON1}$		9.6		mA	B
3.4	Output power 2	V_{VS1} = V_{VS2} = 3V T_{amb} = 25°C V_{PWR_H} = 0V f_{RF} = 433.92MHz R_{R_PWR} = 27kΩ R_{Lopt} = 1.1kΩ f_{RF} = 868.3MHz R_{R_PWR} = 16kΩ R_{Lopt} = 0.5kΩ RF_OUT matched to R_{Lopt}// $j/(2 \times \pi \times f_{RF} \times 1.0pF)$	(10)	P_{REF2}	3.5	5.0	6.5	dBm	B
3.5	Supply current TX mode power amplifier ON 2	PA on/5 dBm							
		f_{RF} = 433.92MHz	17, 18	$I_{S\_TX\_PAON2}$		10.5		mA	B
		f_{RF} = 868.3MHz	17, 18	$I_{S\_TX\_PAON2}$		11.2		mA	B
3.6	Output power 3	V_{VS1} = V_{VS2} = 3V T_{amb} = 25°C V_{PWR_H} = AVCC f_{RF} = 433.92MHz R_{R_PWR} = 27kΩ R_{Lopt} = 0.36kΩ f_{RF} = 868.3MHz R_{R_PWR} = 20kΩ R_{Lopt} = 0.22kΩ RF_OUT matched to R_{Lopt}// $j/(2 \times \pi \times f_{RF} \times 1.0pF)$	(10)	P_{REF3}	8.5	10	11.5	dBm	B
3.7	Supply current TX mode power amplifier ON 3	PA on/10dBm							
		f_{RF} = 433.92MHz	17, 18	$I_{S\_TX\_PAON3}$		15.8		mA	B
		f_{RF} = 868.3MHz	17, 18	$I_{S\_TX\_PAON3}$		17.3		mA	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
3.8	Output power variation for full temperature and supply voltage range	T_{amb} = –40°C to +85°C P_{out} = P_{REFX} + ΔP_{REFX} X = 1, 2 or 3 V_{VS1} = V_{VS2} = 3.0V	(10)	ΔP_{REF}		–0.8	–1.5	dB	B
		V_{VS1} = V_{VS2} = 2.7V	(10)	ΔP_{REF}			–2.5	dB	B
		V_{VS1} = V_{VS2} = 2.4V	(10)	ΔP_{REF}			–3.5	dB	B
3.9	Impedance RF_OUT in RX mode	f_{RF} = 433.92MHz	10	$Z_{RF\_OUT\_RX}$		(19 – j366)		Ω	C
		f_{RF} = 868.3MHz	10	$Z_{RF\_OUT\_RX}$		(2.8 – j141)		Ω	C
3.10	Noise floor power amplifier	at ±10MHz/at 5dBm							
		f_{RF} = 433.92MHz	(10)	L_{TX10M}		–126		dBC/Hz	C
		f_{RF} = 868.3MHz	(10)	L_{TX10M}		–125		dBC/Hz	C
3.11	ASK modulation rate	This corresponds to 10Kbit/s Manchester coding and 20Kbit/s NRZ coding		f_{Data_ASK}	1		10	kHz	C
4	XTO								
4.1	Pulling XTO due to XTO, C_{L1} and C_{L2} tolerances	Pulling at nominal temperature and supply voltage f_{XTAL} = resonant frequency of the XTAL C_0 ≥ 1.0pF R_m ≤ 120Ω	24, 25						A
		C_m ≤ 7.0fF C_m ≤ 14fF		Δf_{XTO1}	–50 –100	f_{XTAL}	+50 +100	ppm	
4.2	Transconductance XTO at start	At start-up; after start-up the amplitude is regulated to V_{PPXTAL}	24, 25	$g_{m,\ XTO}$		19		ms	B
4.3	XTO start-up time	C_0 ≤ 2.2pF C_m < 14fF R_m ≤ 120Ω	24, 25	$T_{PWR\_ON\_IRQ\_1}$		300	800	µs	A
4.4	Maximum C_0 of XTAL	Required for stable operation with internal load capacitors	24, 25	C_{0max}			3.8	pF	D
4.5	Internal capacitors	C_{L1} and C_{L2}	24, 25	C_{L1}, C_{L2}	14.8	18	21.2	pF	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
4.6	Pulling of radio frequency f_{RF} due to XTO, C_{L1} and C_{L2} versus temperature and supply changes	1.0pF ≤ C_0 ≤ 2.2pF C_m ≤ 14.0fF R_m ≤ 120Ω PLL adjusted with FREQ at nominal temperature and supply voltage	4, 10	Δf_{XTO2}	–2		+2	ppm	C
4.7	Amplitude XTAL after start-up	C_m = 5fF, C_0 = 1.8pF R_m =15Ω							
		V(XTAL1, XTAL2) peak-to-peak value	24, 25	V_{PPXTAL}		700		mVpp	C
		V(XTAL1) peak-to-peak value	24, 25	V_{PPXTAL}		350		mVpp	C
4.8	Real part of XTO impedance at start-up	C_0 ≤ 2.2pF, small signal start impedance, this value is important for crystal oscillator startup	24, 25	Re_{XTO}		–2,000	–1,500	Ω	B
4.9	Maximum series resistance R_m of XTAL after start-up	C_0 ≤ 2.2pF C_m ≤ 14fFΩ	24, 25	R_{m_max}		15	120	Ω	B
4.10	Nominal XTAL load resonant frequency	f_{RF} = 433.92MHz f_{RF} = 868.3MHz	24, 25	f_{XTAL}		113.25311 13.41191		MHz MHz MHz	D
4.11	External CLK frequency	f_{RF} = 433.92MHz CLK division ratio = 3 CLK has nominal 50% duty cycle	30	f_{CLK}		4.418		MHz	D
		f_{RF} = 868.3MHz CLK division ratio = 3 CLK has nominal 50% duty cycle	30	f_{CLK}		4.471		MHz	D
4.12	DC voltage after start-up	V_{DC}(XTAL1, XTAL2) XTO running (IDLE mode, RX mode and TX mode)	24, 25	V_{DCXTO}	–150	–30		mV	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
5	Synthesizer								
5.1	Spurious TX mode	At $\pm f_{CLK}$, CLK enabled f_{RF} = 433.92MHz f_{RF} = 868.3MHz		SP_{TX}		–68 –70		dBC	C
		At $\pm f_{XTO}$ f_{RF} = 433.92MHz f_{RF} = 868.3MHz		SP_{TX}		–66 –60		dBC	C
5.2	Spurious RX mode	At $\pm f_{CLK}$, CLK enabled f_{RF} = 433.92MHz f_{RF} = 868.3MHz		SP_{RX}		< –75 < –75		dBC	C
		At $\pm f_{XTO}$ f_{RF} = 433.92MHz f_{RF} = 868.3MHz		SP_{RX}		–75 –68		dBC	C
5.3	In loop phase noise TX mode	Measured at 20kHz distance to carrier f_{RF} = 433.92MHz f_{RF} = 868.3MHz		L_{TX20k}		–80 –75		dBC/Hz	A
5.4	Phase noise at 1M RX mode	f_{RF} = 433.92MHz f_{RF} = 868.3MHz		L_{RX1M}		–120 –113		dBC/Hz	C
5.5	Phase noise at 1M TX mode	f_{RF} = 433.92MHz f_{RF} = 868.3MHz		L_{TX1M}		–111 –107		dBC/Hz	C
5.6	Phase noise at 10M RX mode	Noise floor PLL		L_{RX10M}		–135		dBC/Hz	C
5.7	Loop bandwidth PLL TX mode	Frequency where the absolute value loop gain is equal to 1		f_{Loop_PLL}		70		kHz	B
5.8	Frequency deviation TX mode	f_{RF} = 433.92MHz f_{RF} = 868.3MHz		f_{DEV_TX}		±16.17 ±16.37		kHz	D
5.9	Frequency resolution	f_{RF} = 433.92MHz f_{RF} = 868.3MHz	4, 10	Δf_{Step_PLL}		808.9 818.6		Hz	D
5.10	FSK modulation rate	This correspond to 20Kbit/s Manchester coding and 40Kbit/s NRZ coding		f_{Data_FSK}	1		20	kHz	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
6	RX/TX Switch								
6.1	Impedance RX mode	RX mode, pin 38 with short connection to GND, f_{RF} = 0Hz (DC)	39	Z_{Switch_RX}		23000		Ω	A
		f_{RF} = 433.92MHz f_{RF} = 868.3MHz	39	Z_{Switch_RX}		(10.3 – j153) (8.9 – j73)		Ω	C
6.2	Impedance TX mode	TX mode, pin 38 with short connection to GND, f_{RF} = 0Hz (DC)	39	Z_{Switch_TX}		5		Ω	A
		f_{RF} = 433.92MHz f_{RF} = 868.3MHz	39	Z_{Switch_RX}		(4.5 + j4.3) (5 + j9)		Ω	C
7	Microcontroller Interface								
7.1	Voltage range for microcontroller interface	I_{VSINT} < 10µA if CLK is disabled and all interface pins are in stable condition and unloaded	27, 28, 29, 30, 31, 32, 33, 34, 35		2.4		5.25	V	A
7.2	CLK output rise and fall time	f_{CLK} < 4.5MHz C_L = 10pF C_L = Load capacitance on pin CLK 2.4V ≤ V_{VSINT} ≤ 5.25V 20% to 80% V_{VSINT}	30	t_{rise} t_{fall}		20 20	30 30	ns ns	B
7.4	Current consumption of the microcontroller interface	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled V_{VSOUT} disabled C_L = Load capacitance on pin CLK (All interface pins, except pin CLK, are in stable condition and unloaded)	27	I_{VSINT}	$I_{VSINT} = \frac{(C_{CLK} + C_L) \times V_{VSINT} \times f_{XTO}}{3}$ < 10µA < 10µA				
7.5	Internal equivalent capacitance	Used for current calculation	30, 27	C_{CLK}		8		pF	B

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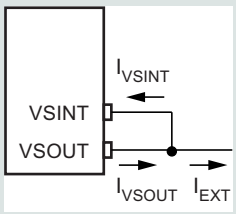
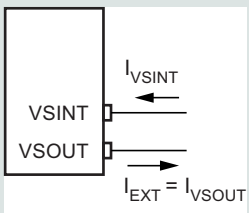
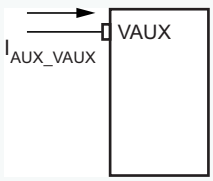
Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

12. Electrical Characteristics: General (Continued)

This device is manufactured with an industrial (not automotive) grade process and process controls. Although this device may meet certain automotive grade criteria in performance, Atmel can not recommend that this device be used in any automotive application. All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V (1-battery application), V_{VS2} = 6.0V (2-battery application) and V_{VS2} = V_{VAUX} = 5.0V (Base-station Application). Typical values are given at f_{RF} = 433.92MHz unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

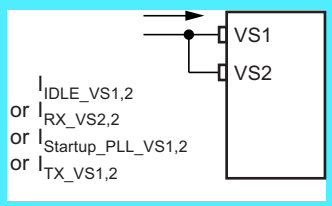
No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
8	Power Supply General Definitions and AUX Mode								
8.1	Current consumption of an external device connected to pin VSOUT	 		I_{EXT}	$I_{EXT} = I_{VSOUT} - I_{VSINT}$ $I_{EXT} = I_{VSOUT}$				
8.2	AUX mode								
8.3	Power supply output voltage	AUX mode V_{VAUX} ≥ 4V I_{VSOUT} ≤ 13.5mA (3.25V regulator mode, V_REG2, see Figure 5-1 on page 25)	22	V_{VSOUT}	2.7		3.5	V	A
8.4	Current in AUX mode on pin VAUX	I_{VSOUT} = 0 V_{VAUX} = 6V V_{VAUX} = 4V to 7V	19	I_{AUX_VAUX}		380	500 500	µA µA	B
8.5	Supply current AUX mode	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled	19, 22, 27	I_{S_AUX}	$I_{S\_AUX} = I_{AUX\_VAUX} + I_{VSINT} + I_{EXT}$ $I_{S\_AUX} = I_{AUX\_VAUX} + I_{EXT}$				
8.6	Supported voltage range VAUX		19	V_{VAUX}	4	6	7	V	

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 3-1 on page 11 with component values according to Table 3-2 on page 11 and RF_OUT matched to 50Ω according to Figure 3-10 on page 18 with component values according to Table 3-7 on page 19.

13. Electrical Characteristics: 1 Li Battery Application (3V)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V. Application according to Figure 2-1 on page 7.
f_{RF} = 433.92MHz/868.3MHz unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9	1 Li Battery Application (3V)								
9.1	Supported voltage range (every mode except high power TX mode)	1 Li battery application (3V) PWR_H = GND	17, 18	V_{VS1}, V_{VS2}	2.4		3.6	V	A
9.2	Supported voltage range (high power TX mode)	1 Li battery application (3V) PWR_H = AVCC	17, 18	V_{VS1}, V_{VS2}	2.7		3.6	V	A
9.3	Power supply output voltage	1 Li battery application (3V) V_{VS1} = V_{VS2} ≥ 2.6V VAUX open(1) I_{VSOUT} ≤ 13.5mA (no voltage regulator to stabilize V_{VSOUT}) V_{VS1} = V_{VS2} ≥ 2.425V VAUX open(1) I_{VSOUT} ≤ 1.5mA (no voltage regulator to stabilize V_{VSOUT})	22	V_{VSOUT}	2.4		V_{VS1}	V	B
9.4	Supply voltage for microcontroller interface		27	V_{VSINT}	2.4		5.25	V	A
9.5	Threshold hysteresis	V_{Thres_2} – V_{Thres_1}	22	ΔV_{Thres}	60	80	100	mV	B
9.6	Reset threshold voltage at pin VSOUT (N_RESET)		22	V_{Thres_1}	2.18	2.3	2.42	V	A
9.7	Reset threshold voltage at pin VSOUT (Low_Batt)		22	V_{Thres_2}	2.26	2.38	2.5	V	A
9.8	Supply current OFF mode	V_{VS1} = V_{VS2} ≤ 3.6V V_{VSINT} = 0V	17, 18, 22, 27	I_{S_OFF}		2	350	nA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The voltage of VAUX may rise up to 2V. The current I_{VAUX} may not exceed 100µA.

13. Electrical Characteristics: 1 Li Battery Application (3V) (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS1} = V_{VS2} = 3.0V. Application according to Figure 2-1 on page 7.
f_{RF} = 433.92MHz/868.3MHz unless otherwise specified

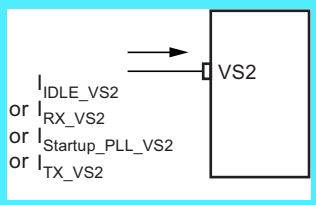
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.9	Current in IDLE mode on pin VS1 and VS2	V_{VS1} = V_{VS2} ≤ 3V I_{VSOUT} = 0 CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled V_{VSOUT} disabled	17, 18	$I_{IDLE\_VS1,2}$		312 260 225	430 370 320	µA µA µA	A B B
9.10	Supply current IDLE mode		17, 18, 22, 27	I_{S_IDLE}	$I_{S\_IDLE} = I_{IDLE\_VS1,2} + I_{VSINT} + I_{EXT}$				
9.11	Current in RX mode on pin VS1and VS2	V_{VS1} = V_{VS2} ≤ 3V I_{VSOUT} = 0	17, 18	$I_{RX\_VS1,2}$		10.5	14	mA	A
9.12	Supply current RX mode	CLK enabled V_{VSOUT} enabled	17, 18, 22, 27	I_{S_RX}	$I_{S\_RX} = I_{RX\_VS1,2} + I_{VSINT} + I_{EXT}$				
9.13	Current during $T_{Startup\_PLL}$ on pin VS1 and VS2	V_{VS1} = V_{VS2} ≤ 3V I_{VSOUT} = 0	17, 18	$I_{Startup\_PLL\_VS1,2}$		8.8	11.5	mA	C
9.14	Current in RX polling mode on pin VS1 and VS2	$I_P = \frac{I_{IDLE\_VS1,2} \times T_{SLEEP} + I_{Startup\_PLL\_VS1,2} \times T_{Startup\_PLL} + I_{RX\_VS1,2} \times (T_{Startup\_Sig\_Proc} + T_{Bitcheck})}{T_{Sleep} + T_{Startup\_PLL} + T_{Startup\_Sig\_Proc} + T_{Bitcheck}}$							
9.15	Supply current RX polling mode	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled V_{VSOUT} disabled	17, 18, 22, 27	I_{S_Poll}	$I_{S\_Poll} = I_P + I_{VSINT} + I_{EXT}$ $I_{S\_Poll} = I_P + I_{EXT}$ $I_{S\_Poll} = I_P$				
9.16	Current in TX mode on pin VS1 and VS2	V_{VS1} = V_{VS2} ≤ 3V I_{VSOUT} = 0 Pout = 5dBm/10dBm 433.92MHz/5dBm 433.92MHz/10dBm 868.3MHz/5dBm 868.3MHz/10dBm	17, 18	$I_{TX\_VS1\_VS2}$		10.4 15.8 10.5 15.8 11.2 17.3	13.5 20.6 13.5 20.5 14.5 22.5	mA	B
9.17	Supply current TX mode	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled	17, 18, 22, 27	I_{S_TX}	$I_{S\_TX} = I_{TX\_VS1,2} + I_{VSINT} + I_{EXT}$ $I_{S\_TX} = I_{TX\_VS1,2} + I_{EXT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The voltage of VAUX may rise up to 2V. The current I_{VAUX} may not exceed 100µA.

14. Electrical Characteristics: 2 Li Battery Application (6V)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS2} = 6.0V. Application according to Figure 2-3 on page 9
f_{RF} = 433.92MHz/868.3MHz unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	2 Li Battery Application (6V)								
10.1	Supported voltage range	2 Li battery application (6V)	17	V_{VS2}	4.4		6.6	V	A
10.2	Power supply output voltage	2 Li battery application (6V) V_{VS2} ≥ 4.4V VAUX open(1) I_{VSOUT} ≤ 13.5mA (3.3V regulator mode, V_REG1, see Figure 5-1 on page 25)	22	V_{VSOUT}	3.0		3.5	V	A
10.3	Supply voltage for microcontroller interface		27	V_{VSINT}	2.4		5.25	V	A
10.4	Threshold hysteresis	$V_{Thres\_2} - V_{Thres\_1}$	22	ΔV_{Thres}	60	80	100	mV	B
10.5	Reset threshold voltage at pin VSOUT (N_RESET)		22	V_{Thres_1}	2.18	2.3	2.42	V	A
10.6	Reset threshold voltage at pin VSOUT (Low_Batt)		22	V_{Thres_2}	2.26	2.38	2.5	V	A
10.7	Supply current OFF mode	V_{VS2} ≤ 6.6V V_{VSINT} = 0V	17, 22, 27	I_{S_OFF}		10	350	nA	A
10.8	Current in IDLE mode on pin VS2	V_{VS2} ≤ 6V I_{VSOUT} = 0 CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled V_{VSOUT} disabled	17	I_{IDLE_VS2}		410 348 309	560 490 430	µA µA µA	A B B
10.9	Supply current IDLE mode		17, 22, 27	I_{S_IDLE}	$I_{S\_IDLE} = I_{IDLE\_VS2} + I_{VSINT} + I_{EXT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The voltage of VAUX may rise up to 2V. The current I_{VAUX} may not exceed 100µA.

14. Electrical Characteristics: 2 Li Battery Application (6V) (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS2} = 6.0V. Application according to Figure 2-3 on page 9
f_{RF} = 433.92MHz/868.3MHz unless otherwise specified

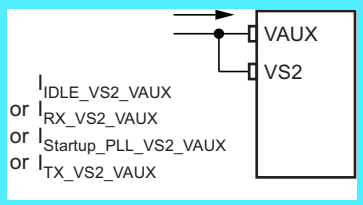
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.10	Current in RX mode on pin VS2	I_{VSOUT} = 0	17	I_{RX_VS2}		10.8	14.5	mA	B
10.11	Supply current RX mode	CLK enabled V_{VSOUT} enabled	17, 22, 27	I_{S_RX}	$I_{S\_RX} = I_{RX\_VS2} + I_{VSINT} + I_{EXT}$				
10.12	Current during $T_{Startup\_PLL}$ on pin VS2	I_{VSOUT} = 0	17	$I_{Startup\_PLL\_VS2}$		9.1	12	mA	C
10.13	Current in RX polling mode on pin VS2	$I_P = \frac{I_{IDLE\_VS2} \times T_{SLEEP} + I_{Startup\_PLL\_VS2} \times T_{Startup\_PLL} + I_{RX\_VS2} \times (T_{Startup\_Sig\_Proc} + T_{Bitcheck})}{T_{Sleep} + T_{Startup\_PLL} + T_{Startup\_Sig\_Proc} + T_{Bitcheck}}$							
10.14	Supply current RX polling mode	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled V_{VSOUT} disabled	17, 22, 27	I_{S_Poll}	$I_{S\_Poll} = I_P + I_{VSINT} + I_{EXT}$ $I_{S\_Poll} = I_P + I_{EXT}$ $I_{S\_Poll} = I_P$				
10.15	Current in TX mode on pin VS2	I_{VSOUT} = 0 P_{out} = 5dBm/10dBm 433.92MHz/5dBm 433.92MHz/10dBm 868.3MHz/5dBm 868.3MHz/10dBm	17, 19	I_{TX_VS2}		 10.9 16.3 11.6 17.8	 14.0 21.0 15.0 23.0	mA	B
10.16	Supply current TX mode	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled	17, 22, 27	I_{S_TX}	$I_{S\_TX} = I_{TX\_VS2} + I_{VSINT} + I_{EXT}$ $I_{S\_TX} = I_{TX\_VS2} + I_{EXT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The voltage of VAUX may rise up to 2V. The current I_{VAUX} may not exceed 100µA.

15. Electrical Characteristics: Base-station Application (5V)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS2} = 5.0V. Application according to Figure 2.2 on page 8 f_{RF} = 433.92MHz/868.3MHz unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11	Base-station Application (5V)							
11.1	Supported voltage range	Base-station application (5V)	17, 19, 27	V_{VS2}, V_{AUX}	4.75		5.25	V	A
11.2	Power supply output voltage	Base-station application (5V) $V_{VS2} = V_{VAUX}$ $I_{VSOUT} \leq 13.5mA$ (3.25V regulator mode, V_REG2, see Figure 5-1 on page 25)	22	V_{VSOUT}	3.0		3.5	V	A
11.3	Supply voltage for microcontroller-interface		27	V_{VSINT}	2.4		5.25	V	A
11.4	Threshold hysteresis	$V_{Thres\_2} - V_{Thres\_1}$	22	ΔV_{Thres}	60	80	100	mV	B
11.5	Reset threshold voltage at pin VSOUT (N_RESET)		22	V_{Thres_1}	2.18	2.3	2.42	V	A
11.6	Reset threshold voltage at pin VSOUT (Low_Batt)		22	V_{Thres_2}	2.26	2.38	2.5	V	A
11.7	Current in IDLE mode on pin VS2 and VAUX	I_{VSOUT} = 0 CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled V_{VSOUT} disabled	17, 19	$I_{IDLE\_VS2\_VAUX}$		444 380 310	580 500 400	µA	B
11.8	Supply current in IDLE mode		17, 19, 22, 27	I_{S_IDLE}	$I_{S\_IDLE} = I_{IDLE\_VS2\_VAUX} + I_{VSINT} + I_{EXT}$				
11.9	Current in RX mode on pin VS2 and VAUX	I_{VSOUT} = 0	17, 19	$I_{RX\_VS2\_VAUX}$		10.8	14.5	mA	B
11.10	Supply current in RX mode	CLK enabled V_{VSOUT} enabled	17, 19, 22, 27	I_{S_RX}	$I_{S\_RX} = I_{RX\_VS2\_VAUX} + I_{VSINT} + I_{EXT}$				
11.11	Current during $T_{Startup\_PLL}$ on pin VS2 and VAUX	I_{VSOUT} = 0	17, 19	$I_{Startup\_PLL\_VS2,VAUX}$		9.1	12	mA	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics: Base-station Application (5V) (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C, V_{VS2} = 5.0V. Application according to Figure 2.2 on page 8
f_{RF} = 433.92MHz/868.3MHz unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.12	Current in RX_Polling_Mode on pin VS2 and VAUX $I_P = \frac{I_{IDLE\_VS2,VAUX} \times T_{SLEEP} + I_{Startup\_PLL\_VS2,VAUX} \times T_{Startup\_PLL} + I_{RX\_VS2,VAUX} \times (T_{Startup\_Sig\_Proc} + T_{Bitcheck})}{T_{Sleep} + T_{Startup\_PLL} + T_{Startup\_Sig\_Proc} + T_{Bitcheck}}$								
11.13	Supply current in RX polling mode	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled V_{VSOUT} disabled	17, 19, 22, 27	I_{S_Poll}	$I_{S\_Poll} = I_P + I_{VSINT} + I_{EXT}$ $I_{S\_Poll} = I_P + I_{EXT}$ $I_{S\_Poll} = I_P$				
11.14	Current in TX mode on pin VS2 and VAUX	I_{VSOUT} = 0 P_{out} = 5dBm/10dBm 433.92MHz/5dBm 433.92MHz/10dBm 868.3MHz/10dBm 868.3MHz/10dBm	17, 19	$I_{TX\_VS2\_VAUX}$		10.9 16.3 11.6 17.8	14.0 21.0 15.0 23.0	mA	B
11.15	Supply current in TX mode	CLK enabled V_{VSOUT} enabled CLK disabled V_{VSOUT} enabled	17, 19, 22, 27	I_{S_TX}	$I_{S\_TX} = I_{TX\_VS2\_VAUX} + I_{VSINT} + I_{EXT}$ $I_{S\_TX} = I_{TX\_VS2\_VAUX} + I_{EXT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

16. Digital Timing Characteristics

All parameters refer to GND and are valid for T_{amb} = 25°C. V_{VS1} = V_{S2} = 3.0V (1 Li battery application (3V)), V_{VS2} = 6.0V (2 Li battery application (6V)) and V_{VS2} = 5.0V (Base-station Application(5V)) unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
12	Basic Clock Cycle of the Digital Circuitry								
12.1	Basic clock cycle			T_{DCLK}	$16/f_{XTO}$		$16/f_{XTO}$	µs	A
12.2	Extended basic clock cycle	XLIM = 0 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3 XLIM = 1 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		T_{XDCLK}	 8 4 2 1 × T_{DCLK} 16 8 4 2 × T_{DCLK}		 8 4 2 1 × T_{DCLK} 16 8 4 2 × T_{DCLK}	µs	A
13	RX Mode/RX Polling Mode								
13.1	Sleep time	Sleep and XSleep are defined in control register 4		T_{Sleep}	Sleep × X_{Sleep} × 1024 × T_{DCLK}		Sleep × X_{Sleep} × 1024 × T_{DCLK}	ms	A
13.2	Start-up PLL RX mode	from IDLE mode		$T_{Startup\_PLL}$		798.5 × T_{DCLK}	798.5 × T_{DCLK}	µs	A
13.3	Start-up signal processing	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		$T_{Startup\_Sig\_Proc}$	882 498 306 210 × T_{DCLK}		882 498 306 210 × T_{DCLK}		A
13.4	Time for bit check	Average time during polling. No RF signal applied. $f_{Signal} = 1/(2 \times t_{ee})$ Signal data rate Manchester (Lim_min and Lim_max up to ±50% of t_{ee}, see Figure 9-4 on page 48) Bit-check time for a valid input signal f_{Signal} $N_{Bit\text{-}check}$ = 0 $N_{Bit\text{-}check}$ = 3 $N_{Bit\text{-}check}$ = 6 $N_{Bit\text{-}check}$ = 9		T_{Bit_check}	 $3/f_{Signal}$ $6/f_{Signal}$ $9/f_{Signal}$	$1/f_{Signal}$	 $3.5/f_{Signal}$ $6.5/f_{Signal}$ $9.5/f_{Signal}$	ms	C
13.5	Bit-rate range	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3		BR_Range	 1.0 2.0 4.0 8.0		 2.5 5.0 10.0 20.0	Kbit/s	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

16. Digital Timing Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C. V_{VS1} = V_{S2} = 3.0V (1 Li battery application (3V)), V_{VS2} = 6.0V (2 Li battery application (6V)) and V_{VS2} = 5.0V (Base-station Application(5V)) unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13.6	Minimum time period between edges at pin SDO_TMDO in RX transparent mode	XLIM = 0 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3 XLIM = 1 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3	31	T_{DATA_min}	$10 \times T_{XDCLK}$			µs	A
13.7	Edge-to-edge time period of the data signal for full sensitivity in RX mode	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		T_{DATA}	200 100 50 25		500 250 125 62.5	µs	B
14	TX Mode								
14.1	Start-up time	From IDLE mode		$T_{Startup}$		$331.5 \times T_{DCLK}$	$331.5 \times T_{DCLK}$	µs	A
15	Configuration of the Transceiver with 4-wire Serial Interface								
15.1	CS set-up time to rising edge of SCK		33, 35	T_{CS_setup}	$1.5 \times T_{DCLK}$			µs	A
15.2	SCK cycle time		33	T_{Cycle}	2			µs	A
15.3	SDI_TMDI set-up time to rising edge of SCK		32, 33	T_{Setup}	250			ns	C
15.4	SDI_TMDI hold time from rising edge of SCK		32, 33	T_{Hold}	250			ns	C
15.5	SDO_TMDO enable time from rising edge of CS		31, 35	T_{Out_enable}			250	ns	C
15.6	SDO_TMDO output delay from falling edge of SCK	C_L = 10pF	31, 35	T_{Out_delay}			250	ns	C
15.7	SDO_TMDO disable time from falling edge of CS		31, 33	$T_{Out\_disable}$			250	ns	C
15.8	CS disable time period		35	$T_{CS\_disable}$	$1.5 \times T_{DCLK}$			µs	A
15.9	Time period SCK low to CS high		33, 35	T_{SCK_setup1}	250			ns	C
15.10	Time period SCK low to CS low		33, 35	T_{SCK_setup2}	250			ns	C
15.11	Time period CS low to SCK high		33, 35	T_{SCK_hold}	250			ns	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

16. Digital Timing Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C. V_{VS1} = V_{S2} = 3.0V (1 Li battery application (3V)), V_{VS2} = 6.0V (2 Li battery application (6V)) and V_{VS2} = 5.0V (Base-station Application(5V)) unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
16	Start Time Push Button Tn and PWR_ON Timing of Wake-up via PWR_ON or Tn								
16.1	PWR_ON high to positive edge on pin IRQ (see Figure 7-4 on page 39)	From OFF mode to IDLE mode, applications according to Figure 2-1 on page 7, Figure 2.2 on page 8 and Figure 2-3 on page 9 XTAL: C_m < 14fF (typ. 5fF) C_0 < 2.2pF (typ. 1.8pF) R_m ≤ 120Ω (typ. 15Ω) 1 Li battery application (3V) C_1 = C_2 = 68nF C_3 = C_4 = 68nF C_5 = 10nF 2 Li battery application (6V) C_1 = C_4 = 68nF C_2 = C_3 = 2.2µF C_5 = 10nF Base-station Application (5V) C_1 = C_3 = C_4 = 68nF C_2 = C_{12} = 2.2µF C_5 = 10nF	29, 40	$T_{PWR\_ON\_IRQ\_1}$		0.3 0.45 0.45	0.8 1.3 1.3	ms ms ms	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

16. Digital Timing Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = 25°C. V_{VS1} = V_{S2} = 3.0V (1 Li battery application (3V)), V_{VS2} = 6.0V (2 Li battery application (6V)) and V_{VS2} = 5.0V (Base-station Application(5V)) unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
16.2	PWR_ON high to positive edge on pin IRQ (see Figure 7-4 on page 39)	Every mode except OFF mode	29, 40	$T_{PWR\_ON\_IRQ\_2}$			$2 \times T_{DCLK}$	µs	A
16.3	Tn low to positive edge on pin IRQ (see Figure 7-2 on page 37)	From OFF mode to IDLE mode, applications according to Figure 2-1 on page 7, Figure 2.2 on page 8 and Figure 2-3 on page 9 XTAL: C_m < 14fF (typ 5fF) C_0 < 2.2pF (typ 1.8pF) R_m ≤ 120Ω (typ 15Ω) 1 Li battery application (3V) C_1 = C_2 = 68nF C_3 = C_4 = 68nF C_5 = 10nF 2 Li battery application (6V) C_1 = C_4 = 68nF C_2 = C_3 = 2.2µF C_5 = 10nF Base-station Application (5V) C_1 = C_3 = C_4 = 68nF C_2 = C_{12} = 2.2µF C_5 = 10nF	29, 41, 42, 43, 44, 45	T_{Tn_IRQ}		0.3 0.45 0.45	0.8 1.3 1.3	ms ms ms	B
16.4	Push button debounce time	Every mode except OFF mode	29, 41, 42, 43, 44, 45	$T_{Debounce}$	8195 $\times T_{DCLK}$		8195 $\times T_{DCLK}$	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

17. Digital Port Characteristics

All parameters refer to GND and are valid for T_{amb} = –40°C to +85°C, V_{VS1} = V_{S2} = 2.4V to 3.6V (1 Li battery application (3V)) and V_{VS2} = 4.4V to 6.6V (2 Li battery application (6V)) and V_{VS2} = 4.75V to 5.25V (Base-station Application (5V)). Typical values at V_{VS1} = V_{VS2} = 3V and T_{amb} = 25°C unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
17	Digital Ports								
17.1	CS input Low level input voltage	V_{VSINT} = 2.4V to 5.25V	35	V_{Il}			0.2 × V_{VSINT}	V	A
	High level input voltage	V_{VSINT} = 2.4V to 5.25V	35	V_{Ih}	0.8 × V_{VSINT}		V_{VSINT}	V	A
17.2	SCK input Low level input voltage	V_{VSINT} = 2.4V to 5.25V	33	V_{Il}			0.2 × V_{VSINT}	V	A
	High level input voltage	V_{VSINT} = 2.4V to 5.25V	33	V_{Ih}	0.8 × V_{VSINT}		V_{VSINT}	V	A
17.3	SDI_TMDI input Low level input voltage	V_{VSINT} = 2.4V to 5.25V	32	V_{Il}			0.2 × V_{VSINT}	V	A
	High level input voltage	V_{VSINT} = 2.4V to 5.25V	32	V_{Ih}	0.8 × V_{VSINT}		V_{VSINT}	V	A
17.4	TEST1 input	TEST1 input must always be directly connected to GND	20		0		0	V	
17.5	TEST2 input	TEST2 input must always be direct connected to GND	23		0		0	V	
17.6	PWR_ON input Low level input voltage	Internal pull-down with series connection of 40kΩ ±20% resistor and diode	40	V_{Il}			0.4	V	A
	High level input voltage(1)	Internal pull-down with series connection of 40kΩ ±20% resistor and diode	40	V_{Ih}	0.8 × V_{VS2}			V	A
17.7	Tn input Low level input voltage	Internal pull-up resistor of 50kΩ ±20%	41, 42, 43, 44, 45	V_{Il}			0.2 × V_{VS2}	V	A
	High level input voltage(1)	Internal pull-up resistor of 50kΩ ±20%	41, 42, 43, 44, 45	V_{Ih}	× V_{VS2} – 0.5V			V	A
17.8	433_N868 input Low level input voltage		6	V_{Il}			0.25	V	A
	Input current low		6	I_{Il}			–5	µA	A
	High level input voltage		6	V_{Ih}	1.7		AVCC	V	A
	Input current high		6	I_{Ih}			1	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. If a logic high level is applied to this pin, a minimum serial impedance of 100Ω must be ensured for proper operation over full temperature range.

17. Digital Port Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +85°C, V_{VS1} = V_{S2} = 2.4V to 3.6V (1 Li battery application (3V)) and V_{VS2} = 4.4V to 6.6V (2 Li battery application (6V)) and V_{VS2} = 4.75V to 5.25V (Base-station Application (5V)). Typical values at V_{VS1} = V_{VS2} = 3V and T_{amb} = 25°C unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
17.9	PWR_H input Low level input voltage		9	V_{Il}			0.25	V	A
	Input current low		9	I_{Il}			–5	µA	A
	High level input voltage		9	V_{Ih}	1.7		AVCC	V	A
	Input current high		9	I_{Ih}			1	µA	A
17.10	SDO_TMDO output Saturation voltage low	V_{VSINT} = 2.4V to 5.25V I_{SDO_TMDO} = 250µA	31	V_{ol}		0.15	0.4	V	B
	Saturation voltage high	V_{VSINT} = 2.4V to 5.25V I_{SDO_TMDO} = –250µA	31	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
17.11	IRQ output Saturation voltage low	V_{VSINT} = 2.4V to 5.25V I_{IRQ} = 250µA	29	V_{ol}		0.15	0.4	V	B
	Saturation voltage high	V_{VSINT} = 2.4V to 5.25V I_{IRQ} = –250µA	29	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
17.12	CLK output Saturation voltage low	V_{VSINT} = 2.4V to 5.25V I_{CLK} = 100µA internal series resistor of 1kΩ for spurious emission reduction in PLL	30	V_{ol}		0.15	0.4	V	B
	Saturation voltage high	V_{VSINT} = 2.4V to 5.25V I_{CLK} = –100µA internal series resistor of 1kΩ for spurious emission reduction in PLL	30	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
17.13	N_RESET output Saturation voltage low	V_{VSINT} = 2.4V to 5.25V I_{N_RESET} = 250µA	28	V_{ol}		0.15	0.4	V	B
	Saturation voltage high	V_{VSINT} = 2.4V to 5.25V I_{N_RESET} = –250µA	28	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
17.14	RX_ACTIVE output Saturation voltage low	V_{VSINT} = 2.4V to 5.25V I_{RX_ACTIVE} = 25µA	46	V_{ol}		0.25	0.4	V	B
	Saturation voltage high	V_{VSINT} = 2.4V to 5.25V I_{RX_ACTIVE} = –1500µA	46	V_{oh}	V_{AVCC} – 0.5	V_{AVCC} – 0.15		V	B
17.15	DEM_OUT output Saturation voltage low	Open drain output I_{DEM_OUT} = 250µA	34	V_{ol}		0.15	0.4	V	B

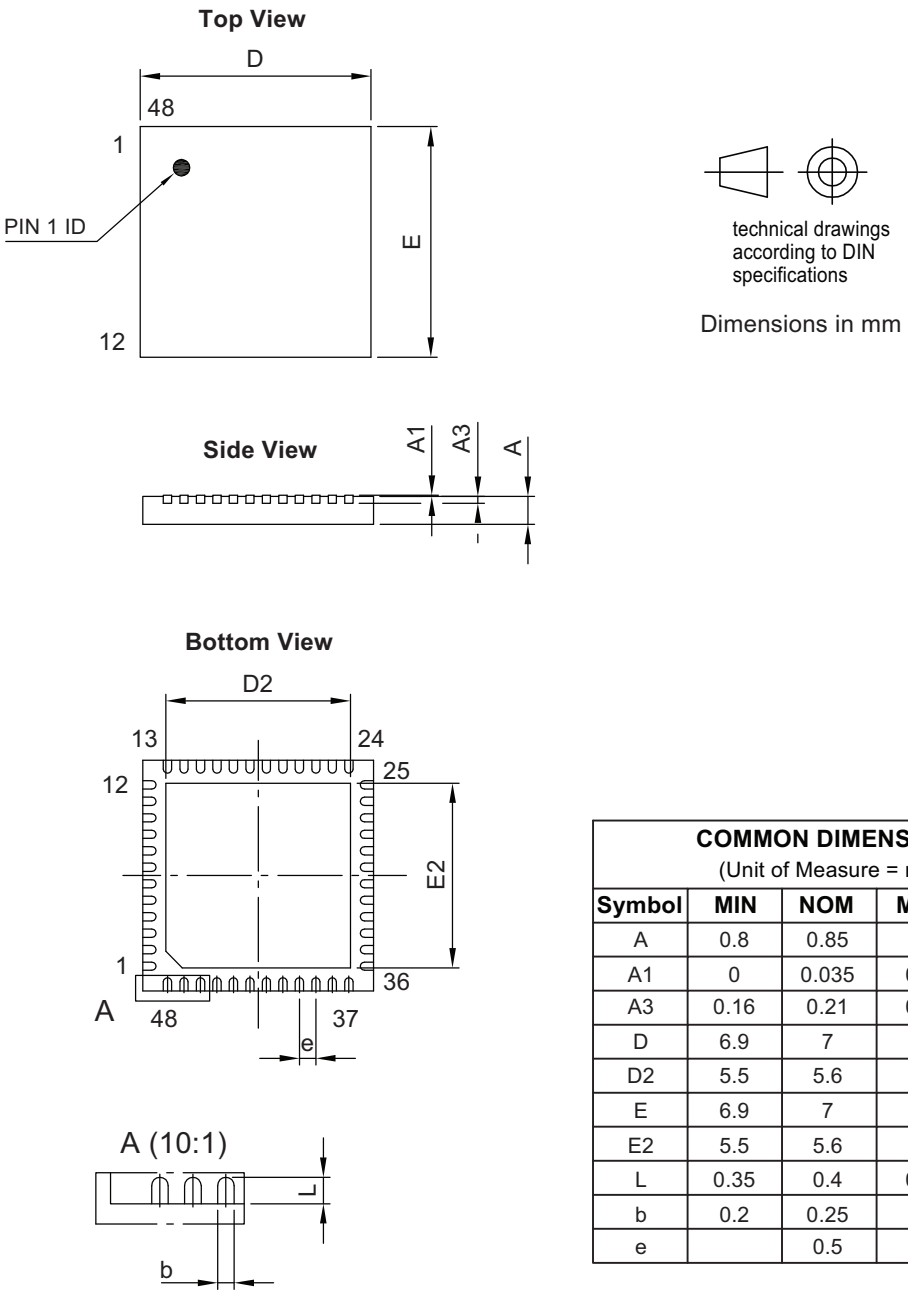
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. If a logic high level is applied to this pin, a minimum serial impedance of 100Ω must be ensured for proper operation over full temperature range.

18. Ordering Information

Extended Type Number	Package	Remarks	Delivery
ATA5428C-PLQW-1	QFN48	7mm × 7mm	Taped and reeled, MOQ 4000

19. Package Information



COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	6.9	7	7.1	
D2	5.5	5.6	5.7	
E	6.9	7	7.1	
E2	5.5	5.6	5.7	
L	0.35	0.4	0.45	
b	0.2	0.25	0.3	
e		0.5		

05/20/14

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: QFN_7x7_48L** Exposed pad 5.6x5.6		6.543-5188.03-4	1

20. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4841H-WIRE-09/14	• Section 18 “Ordering Information” on page 81 updated • Section 19 “Package Information” on page 81 updated
4841G-WIRE-03/04	• Put datasheet in the latest template
4841F-WIRE-11/12	• Section 13 “Ordering Information” on page 82 updated
4841E-WIRE-03/12	• Put datasheet in the latest template • Deleted all the cancelled Parts (ATA5423, ATA5425, ATA5429)
4841D-WIRE-10/07	• Put datasheet in the latest template
4841C-WIRE-05/06	• Put datasheet in the latest template • kBaud replaced through Kbit/s • Baud replaced through bit • Table 9-6 “Interrupt Handling” on page 65 changed

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