AT40K05AL, AT40K10AL
AT40K20AL, AT40K40AL

5K – 50K Gates Coprocessor FPGA with FreeRAM™

DATASHEET

Features

- Ultra High Performance
  - System Speeds to 100MHz
  - Array Multipliers > 50MHz
  - 10ns Flexible SRAM
  - Internal Tri-state Capability in Each Cell
- FreeRAM™
  - Flexible, Single/Dual Port, Synchronous/Asynchronous 10ns SRAM
  - 2,048 – 18,432 bits of Distributed SRAM Independent of Logic Cells
- 128 – 384 PCI Compliant I/Os
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin Locking
  - Pin-compatible with XC4000 and XC5200 FPGAs
- Eight Global Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shutdown Capability for Low Power Management
  - Global Reset/Asynchronous Reset Options
  - Four Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Re-configurability In-System
  - Unlimited Re-programmability via Serial or Parallel Modes
  - Enables Adaptive Designs
  - Enables Fast Vector Multiplier Updates
- Pin-compatible Package Options
  - Low-profile, Plastic Quad Flat Packs (LQFP and PQFP)
- User-friendly Design Tools
  - Supoorted by industry standard EDA tools such as Precision Synthesis, Leonardo Spectrum, Synplify, and Others
  - Timing Driven Placement and Routing
  - Automatic/Interactive Multi-chip Partitioning
  - Fast, Efficient Synthesis
  - Over 75 Automatic Component Generators Create 1000s of Reusable, Fully Deterministic Logic, and RAM Functions
- Supply Voltage 3.3V
- 5V I/O Tolerant

Table 1.   AT40KAL Family[1]

Device	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
Usable Gates	5K – 10K	10K – 20K	20K – 30K	40K – 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	496[1]	954[1]	1,520[1]	3,048[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1.   Packages with FCK will have eight less registers.

1.   Description

The AT40KAL is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, dual-port/single-port SRAM, eight global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 114 to 161 in industry standard packages ranging from 144-pin LQFP to 208-pin PQFP, and support 3.3V designs.

The AT40KAL is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. The Atmel design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar, and Viewlogic.

The AT40KAL can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution, and other multimedia applications.

1.1   Fast, Flexible, and Efficient SRAM

The AT40KAL FPGA offers a patented distributed 10ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, and dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

1.2   Fast, Efficient Array, and Vector Multipliers

The AT40KAL's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KAL Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

1.3 Cache Logic Design

The AT40KAL, AT6000, and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

1.4 Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach, and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35µ triple-metal, CMOS process and are 100% factory-tested. The Atmel PC- based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density, and design flexibility in an FPGA. The cells in the Atmel array are small, efficient, and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

2. The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, seeFigure 2-1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2-2. At the intersection of each repeater row and column, there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM*, with either synchronous or asynchronous operation.

> *The right-most column can only be used as single-port RAM.

Figure 2-1.   Symmetrical Array Surrounded by I/O (AT40K20AL)[1]
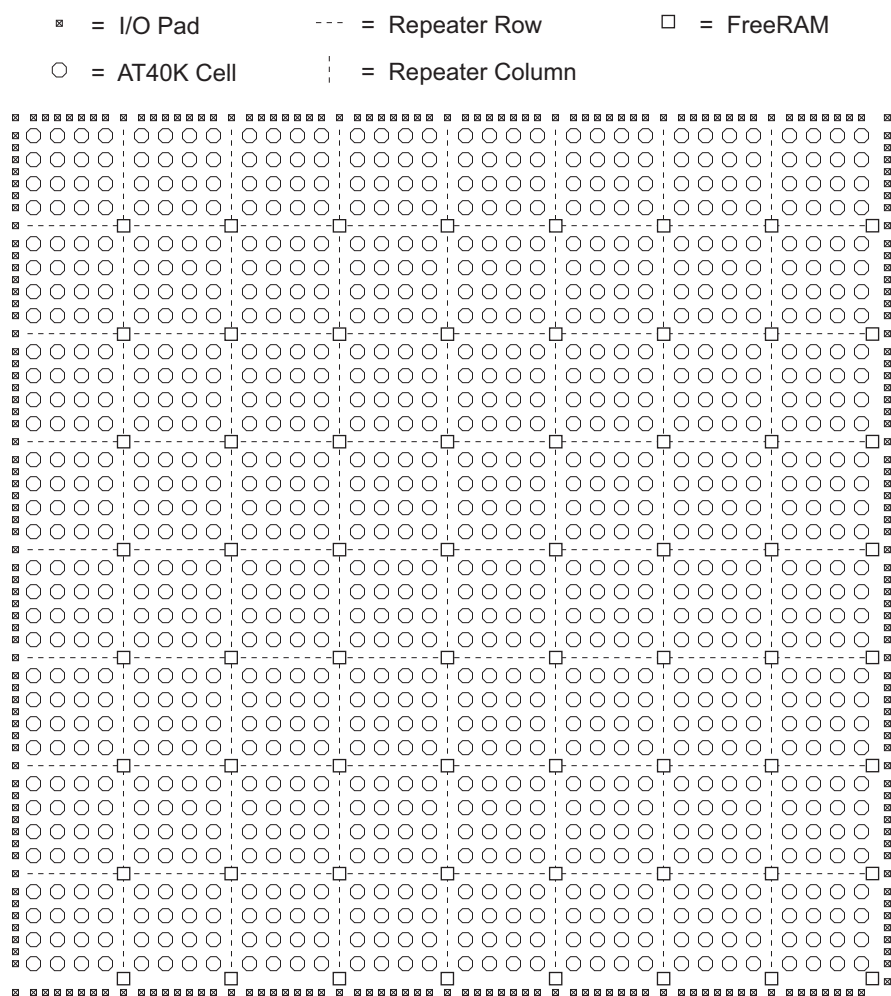
Note: 1.   AT40KAL has registered I/Os. Group enable on every sector for tri-states on obufe's.

Figure 2-2.   Floor Plan (Representative Portion)[1]
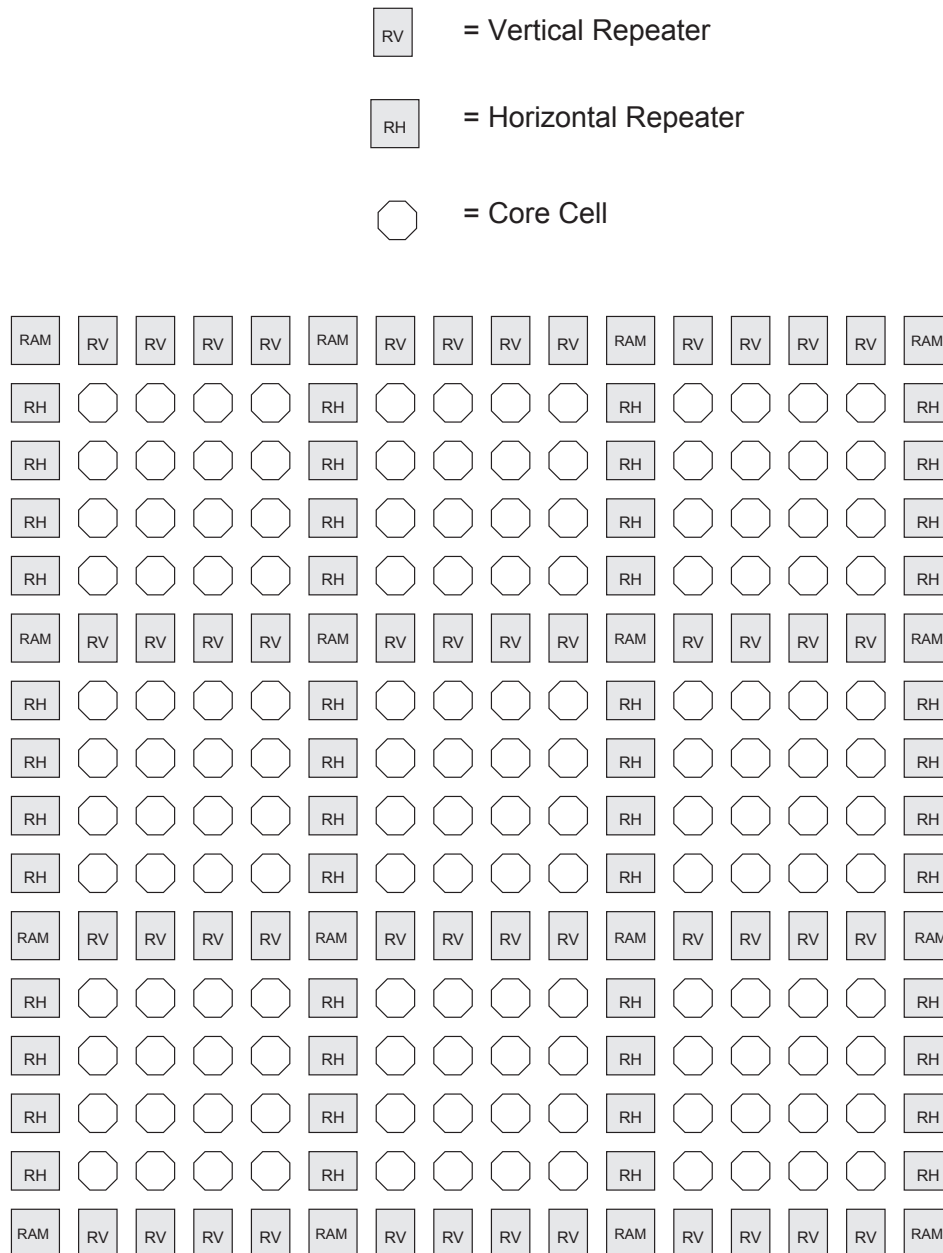
Note: 1.   Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

3.   The Busing Network

Figure 3-1 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four ce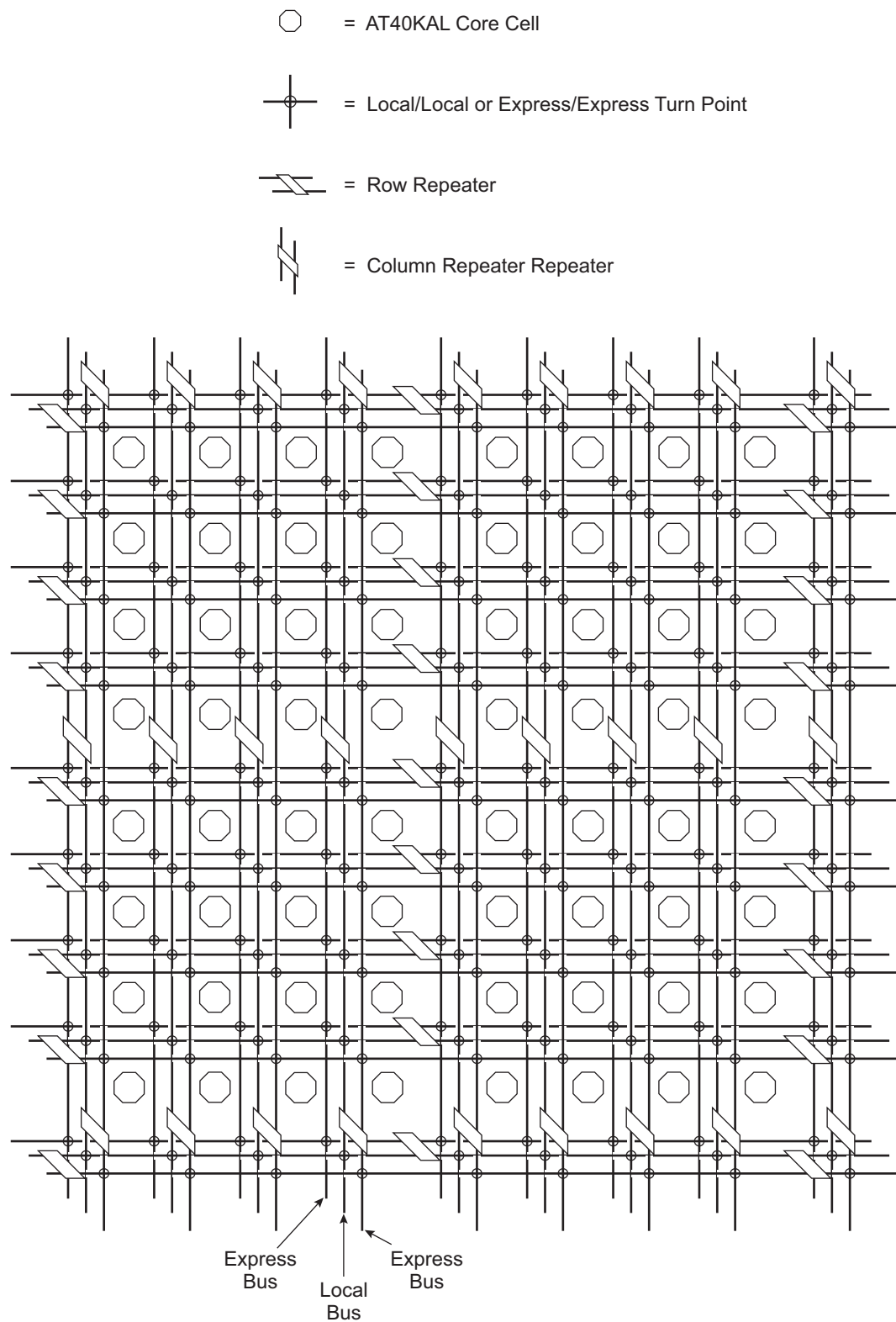lls and connects to consecutive repeaters. Each express-bus segment spans eight cells and "leapfrogs" or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40KAL are used as a dual-function resources. Table 3-1 shows which buses are used in a dual-function mode and which bus plane is used. The AT40KAL software tools are designed to accommodate dual-function buses in an efficient manner.

Table 3-1.   Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge. Bus in first column to left of RAM block.
RAM Write Enable	Express	1	Vertical	Bus full length at array edge. Bus in first column to left of RAM block.
RAM Address	Express	1 – 5	Vertical	Buses full length at array edge. Buses in second column to left of RAM block.
RAM Data In	Local	1	Horizontal	Data In connects to local bus plane 1.
RAM Data Out	Local	2	Horizontal	Data out connects to local bus plane 2.
Clocking	Express	4	Vertical	Bus half length at array edge.
Set/Reset	Express	5	Vertical	Bus half length at array edge.

Figure 3-1.   Busing Plane (One of Five)

◯   = AT40KAL Core Cell

= Local/Local or Express/Express Turn Point

= Row Repeater

= Column Repeater Repeater

Express
Bus   Express
      Local   Bus
       Bus

4.   Cell Connections

Figure 4-1(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4-1(b) depicts the connections between a cell and five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane).

Figure 4-1.   Cell Connections

(a) Cell-to-cell Connections   (b) Cell-to-bus Connections
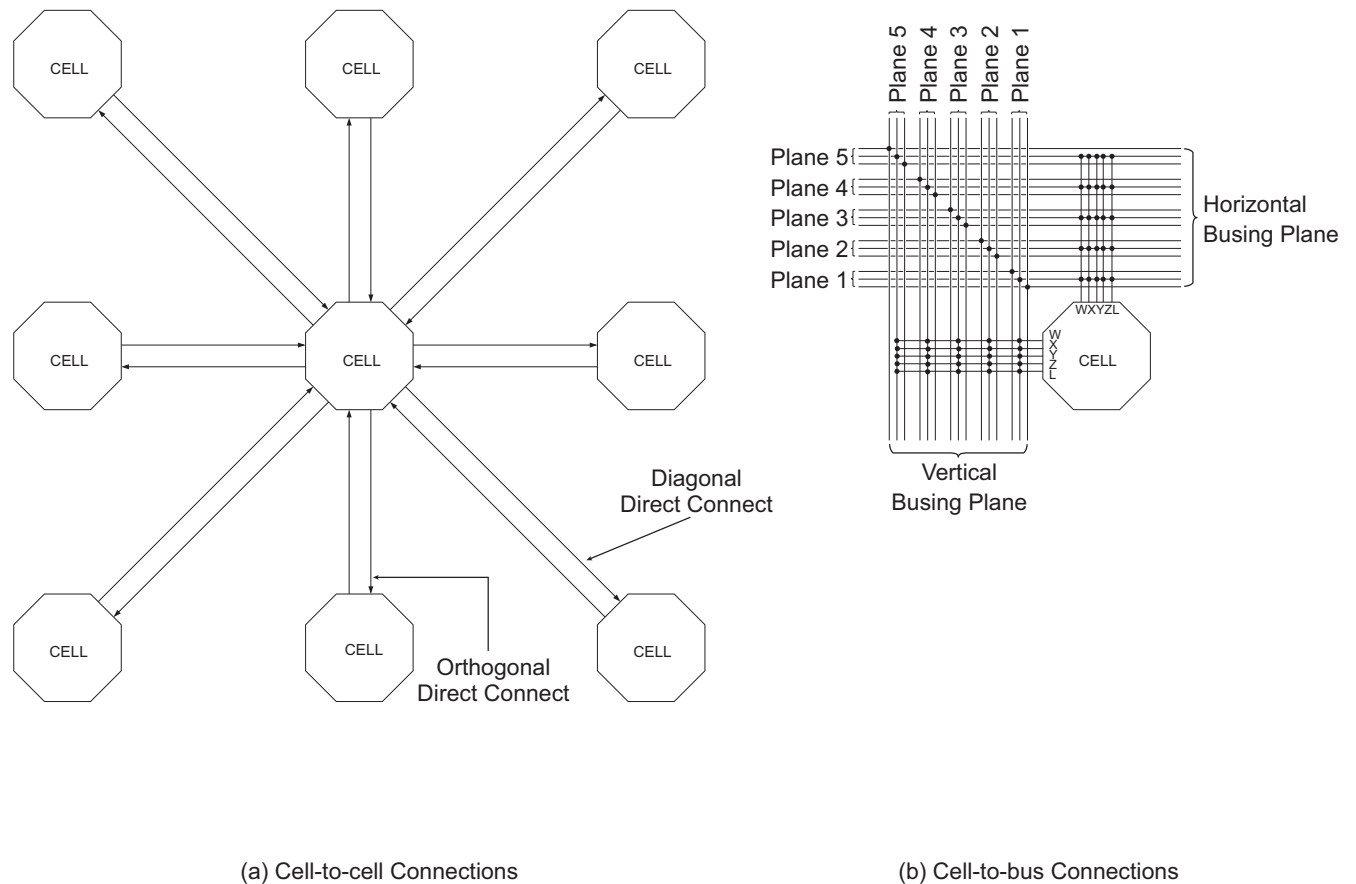
5. The Cell

Figure 5-1 depicts the AT40KAL cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n ($V_1 - V_5$) is connected to the vertical local bus in plane n. H_n ($H_1 - H_5$) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40KAL FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means any core cell can implement two functions of three inputs or one function of four inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the "front end" of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

With this functionality in each core cell, the core cell can be configured in several "modes". The core cell flexibility makes the AT40KAL architecture well suited to most digital design application areas, see Figure 5-2.

Figure 5-1.   The Cell
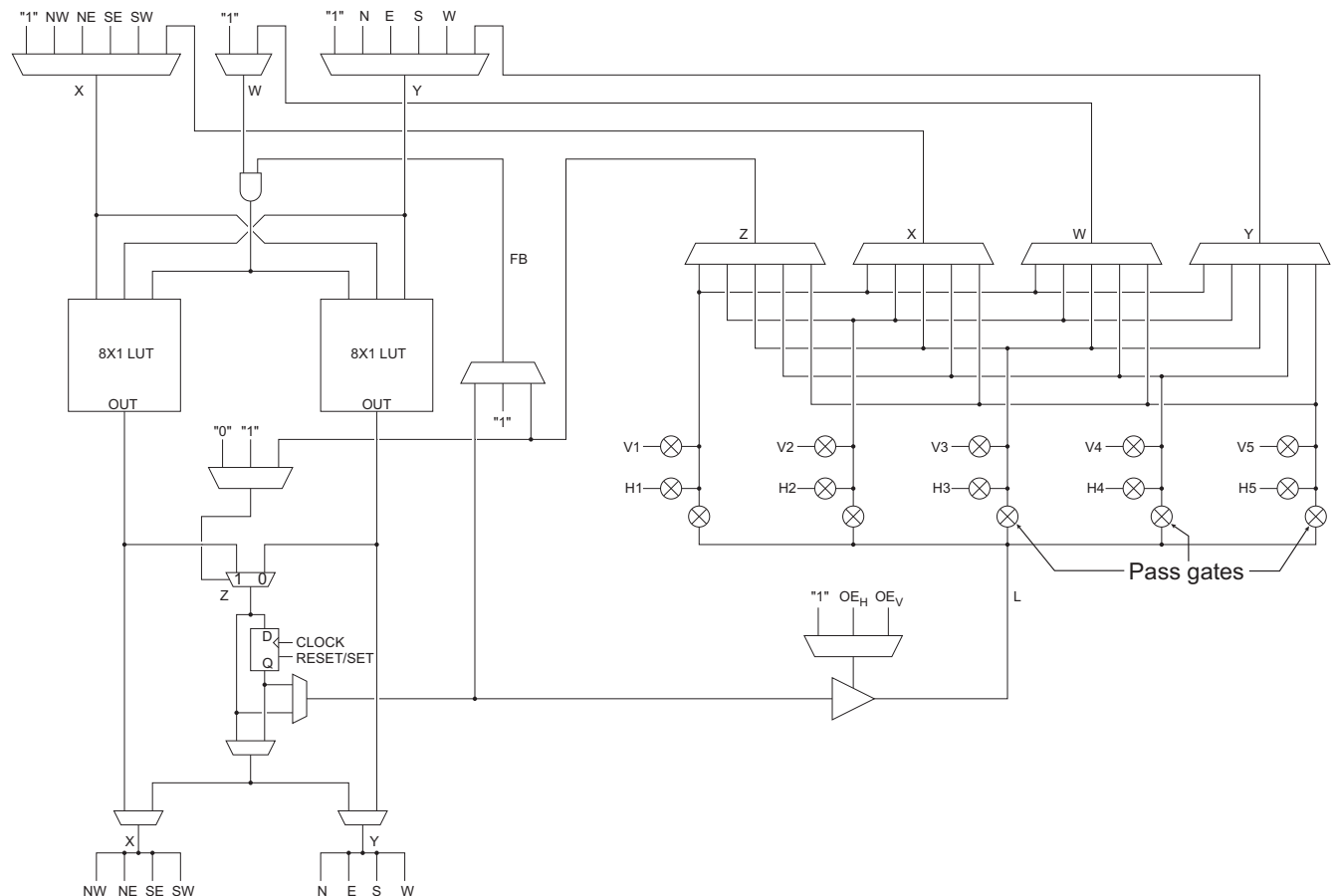
X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Figure 5-2.   Some Single Cell Modes
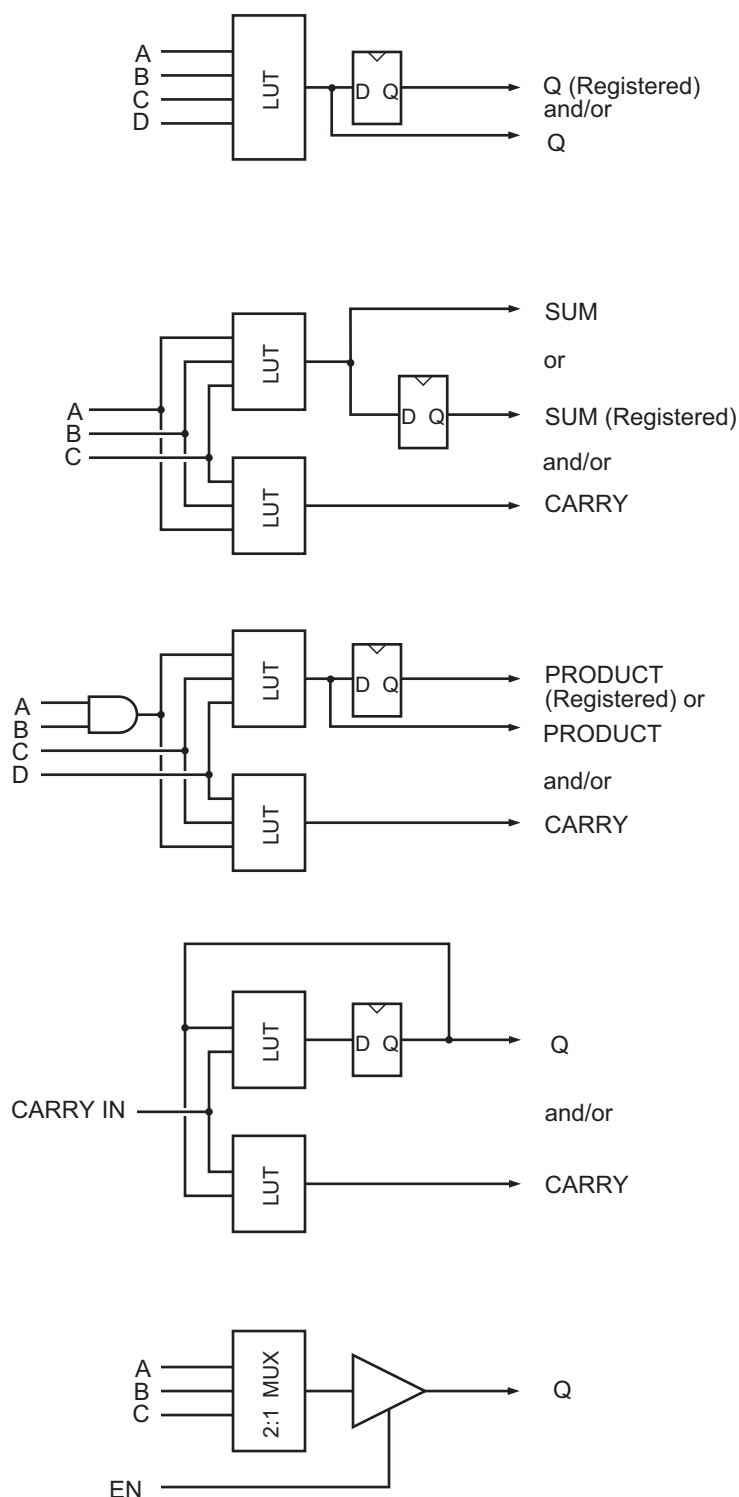
Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode. Frequently used in many designs. As can be seen in the figure, the AT40KAL core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40KAL architecture.

Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

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6.   RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array, see Figure 6-1.

- A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1).
- A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2).
- A 5-bit Input Address Bus connects to five vertical express buses in the same column.
- A 5-bit Output Address Bus connects to five vertical express buses in the same column.
- Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks.
- For the left-most RAM blocks, Aout is on the left and Ain is on the right.
- For the right-most RAM blocks, Ain is on the left and Aout is tied off; only be configured as a single port.
- For the single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port.
- The Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 6-1.   RAM Connections (One Ram Block)
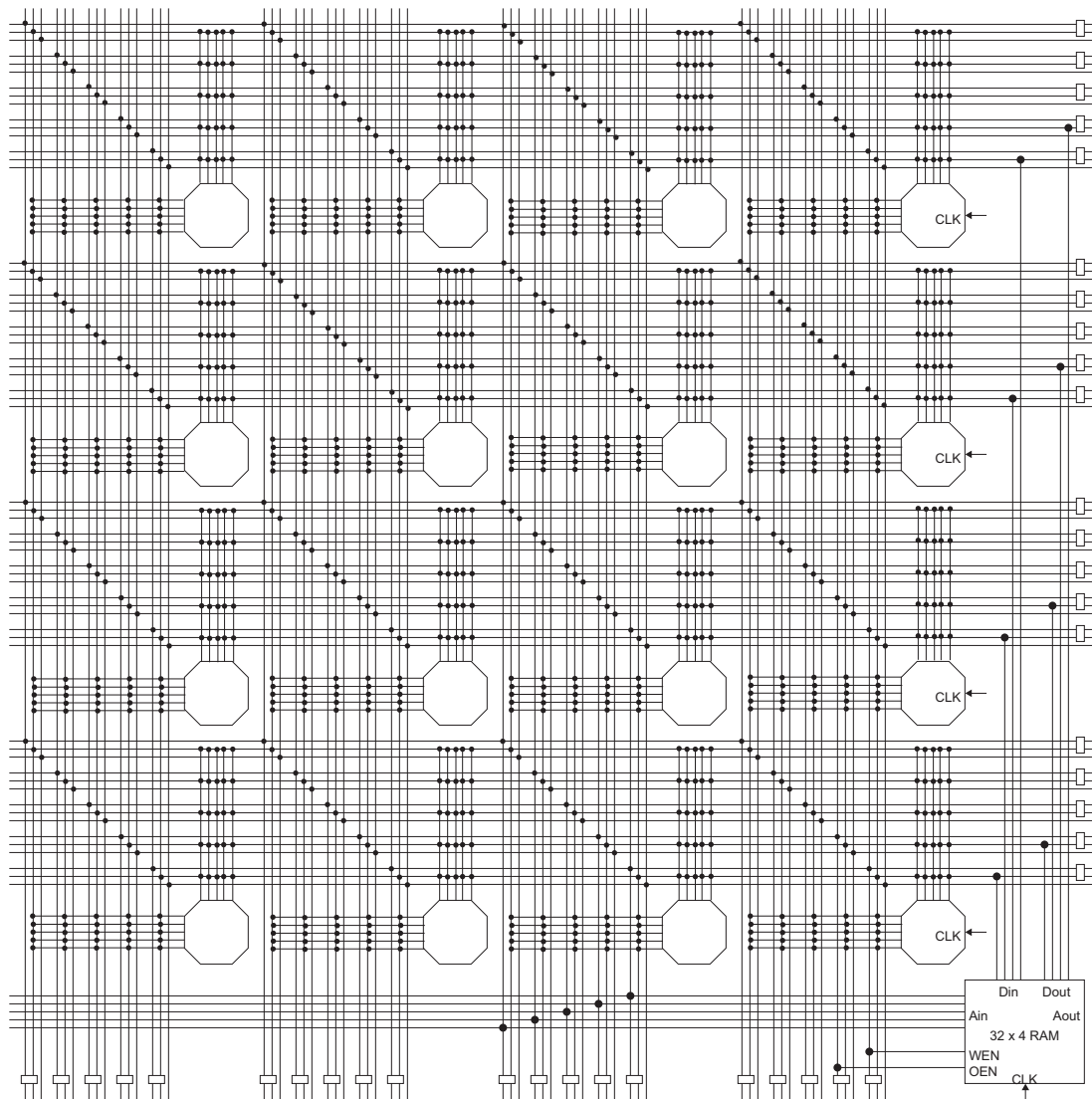
Reading and writing of the 10ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is Logic 1, data flows through; when Load is Logic 0, data is latched. These latches are used to synchronize Write Address, $\overline{\text{Write Enable Not}}$, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is Logic 1 and $\overline{\text{WE}}$ is Logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is Logic 0 or $\overline{\text{WE}}$ is Logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select one (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the "AT40K/40KAL Configuration Series" application note at www.atmel.com).

Figure 6-2.   RAM Logic
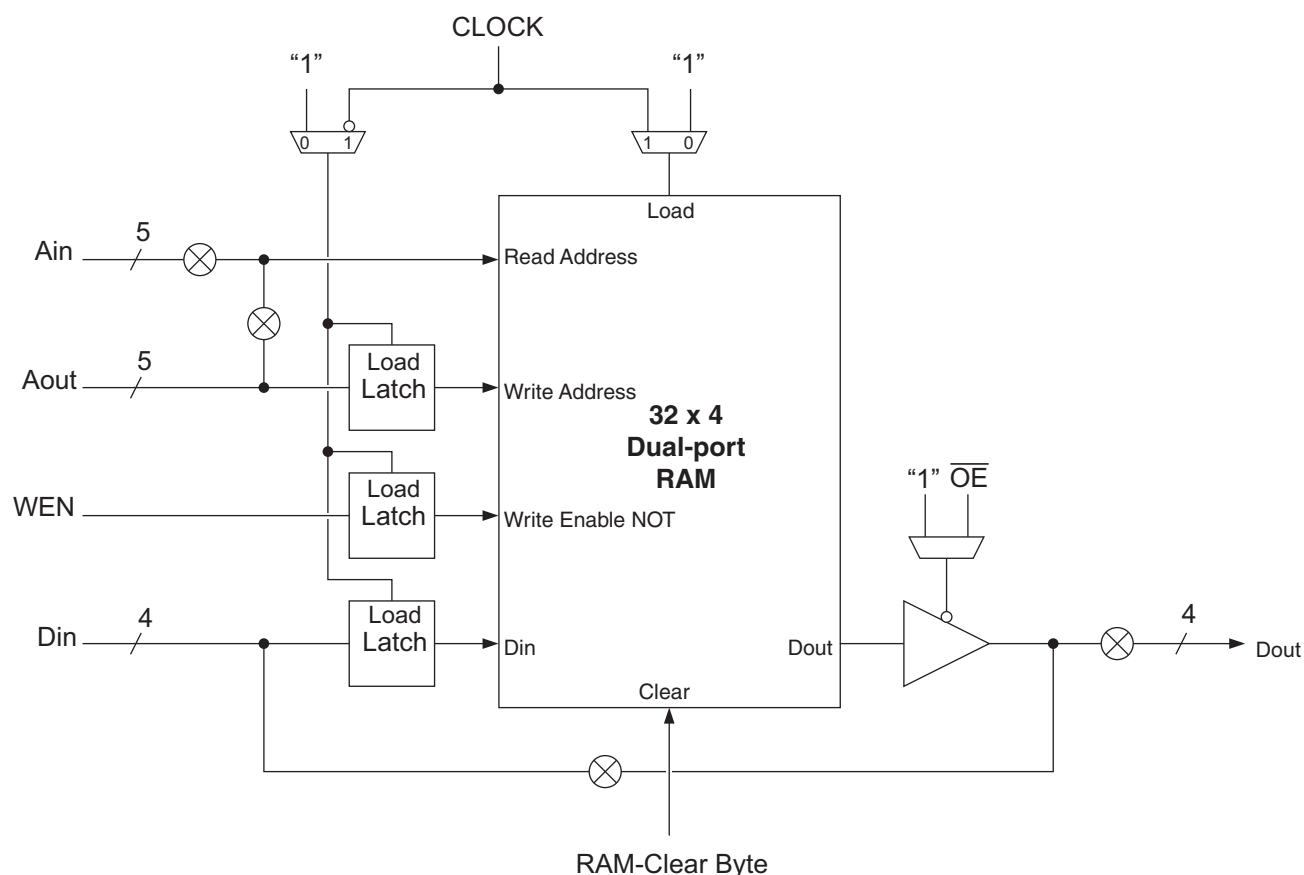
Figure 6-3 shows an example of a RAM macro constructed using the AT40KAL FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM.

> The very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

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Figure 6-3. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)
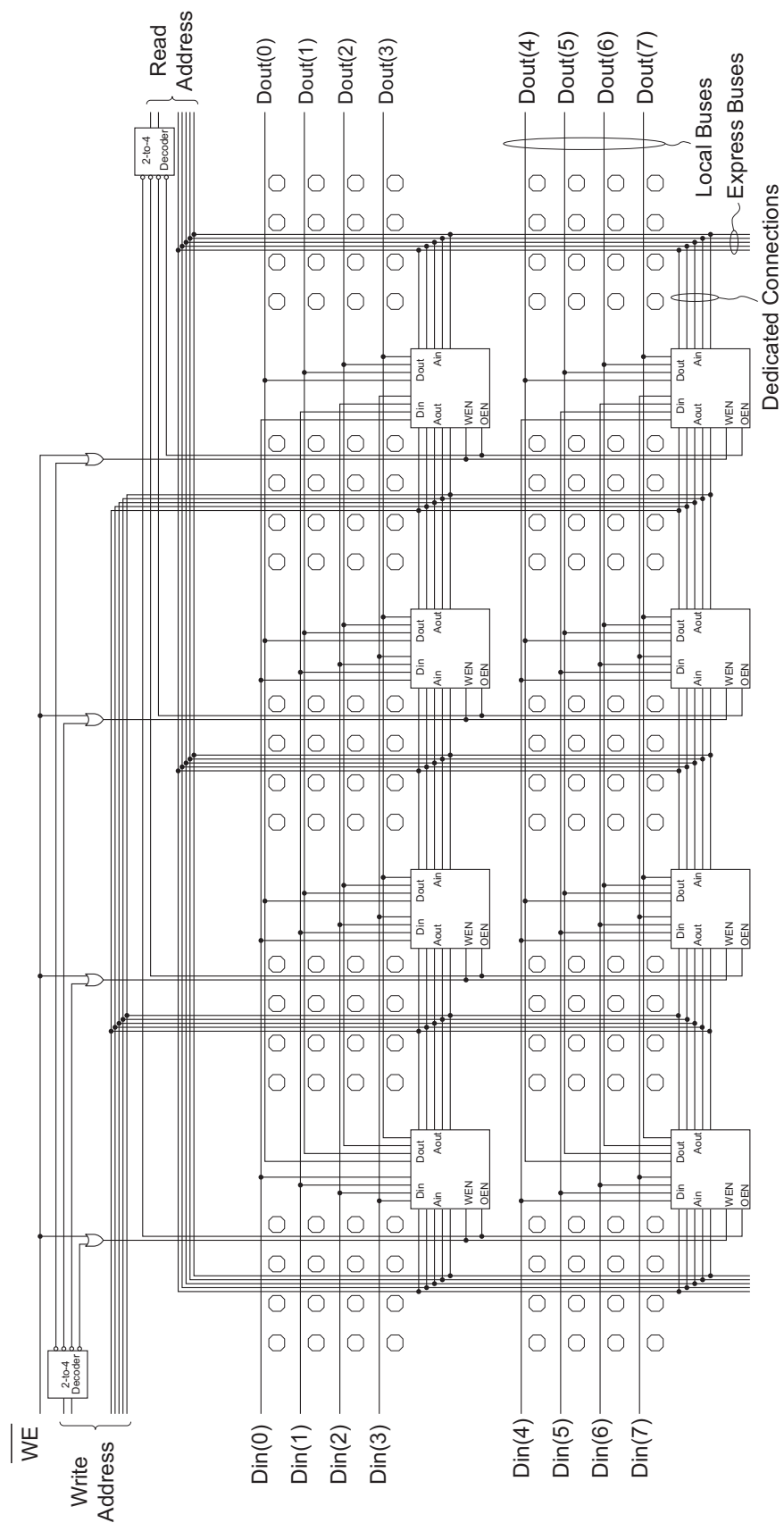
7. Clocking Scheme

There are eight Global Clock buses (GCK1 – GCK8) on the AT40KAL FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 – FCK4), two per edge column of the array for PCI specification. For AT40KAL FPGAs, even the derived clocks can be routed through the Global network. Access points are provided in the corners of the array to route the derived clocks into the global clock network. The IDS software tools handle derived clocks to global clock connections automatically if used.

Each column of an array has a "Column Clock mux" and a "Sector Clock mux". The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to zero, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus, see Figure 7-1. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant zero is provided to each register's clock pins. After configuration on power-up, the registers either set or reset, depending on the user's choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 7-1.   Clocking (for One Column of Cells)

FCK (2 per Edge Column of the Array)

GCK1 - GCK8

Column Clock Mux

Sector Clock Mux

Global Clock Line
(Buried)

Express Bus
(Plane 4; Half Length at Edge)

"1"

"1"

Repeater

Sector Clock Mux

"1"

"1"
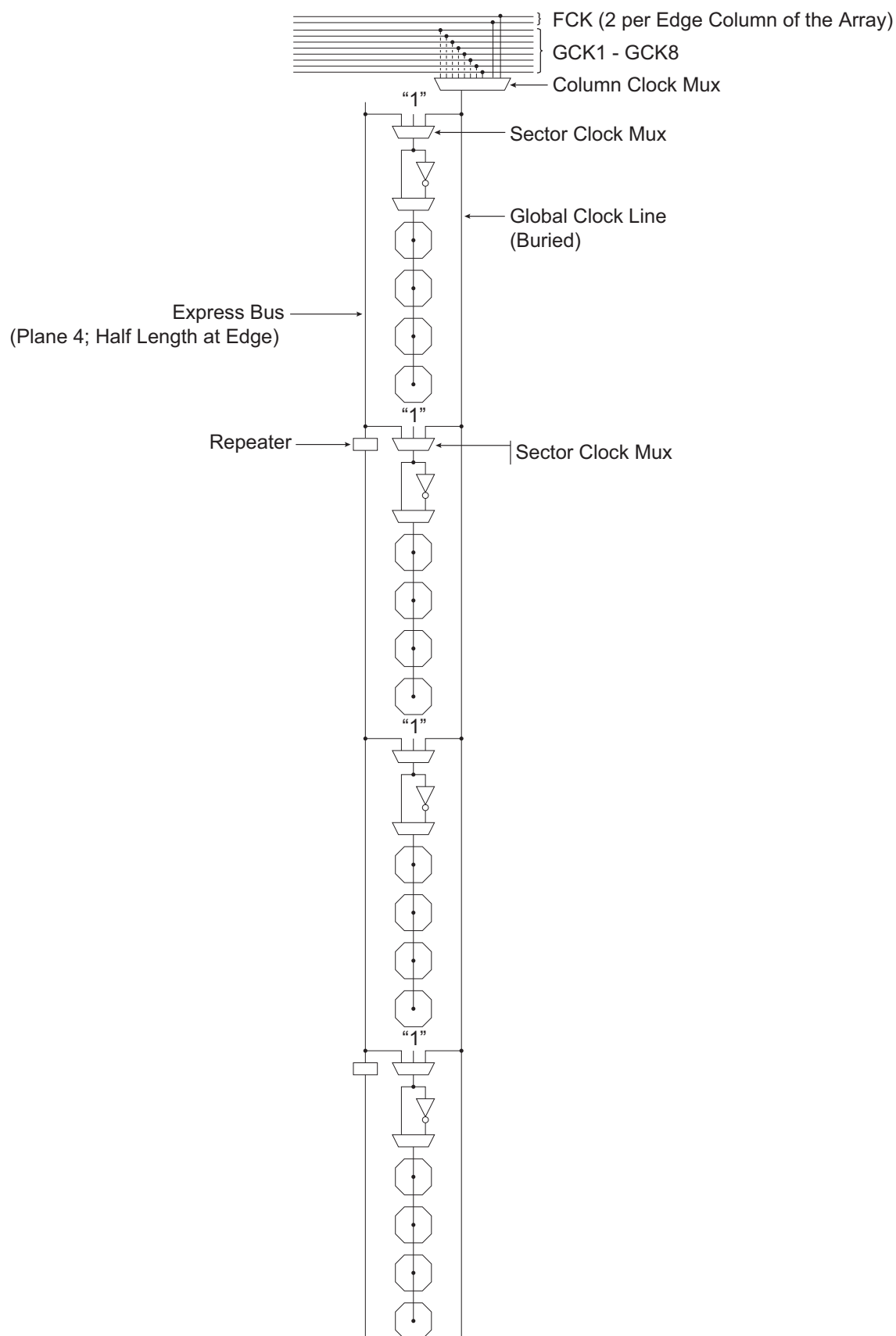
8. Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 8-1. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (Logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a Logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

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Figure 8-1.   Set/Reset (for One Column of Cells)

Each Cell has a Programmable Set or Reset

Sector Set/Reset Mux

Repeater

"1"

Global Set/Reset Line (Buried)

"1"

Express Bus
(Plane 5; Half Length at Edge)

"1"

"1"

Any User I/O can Drive Global Set/Reset Lone
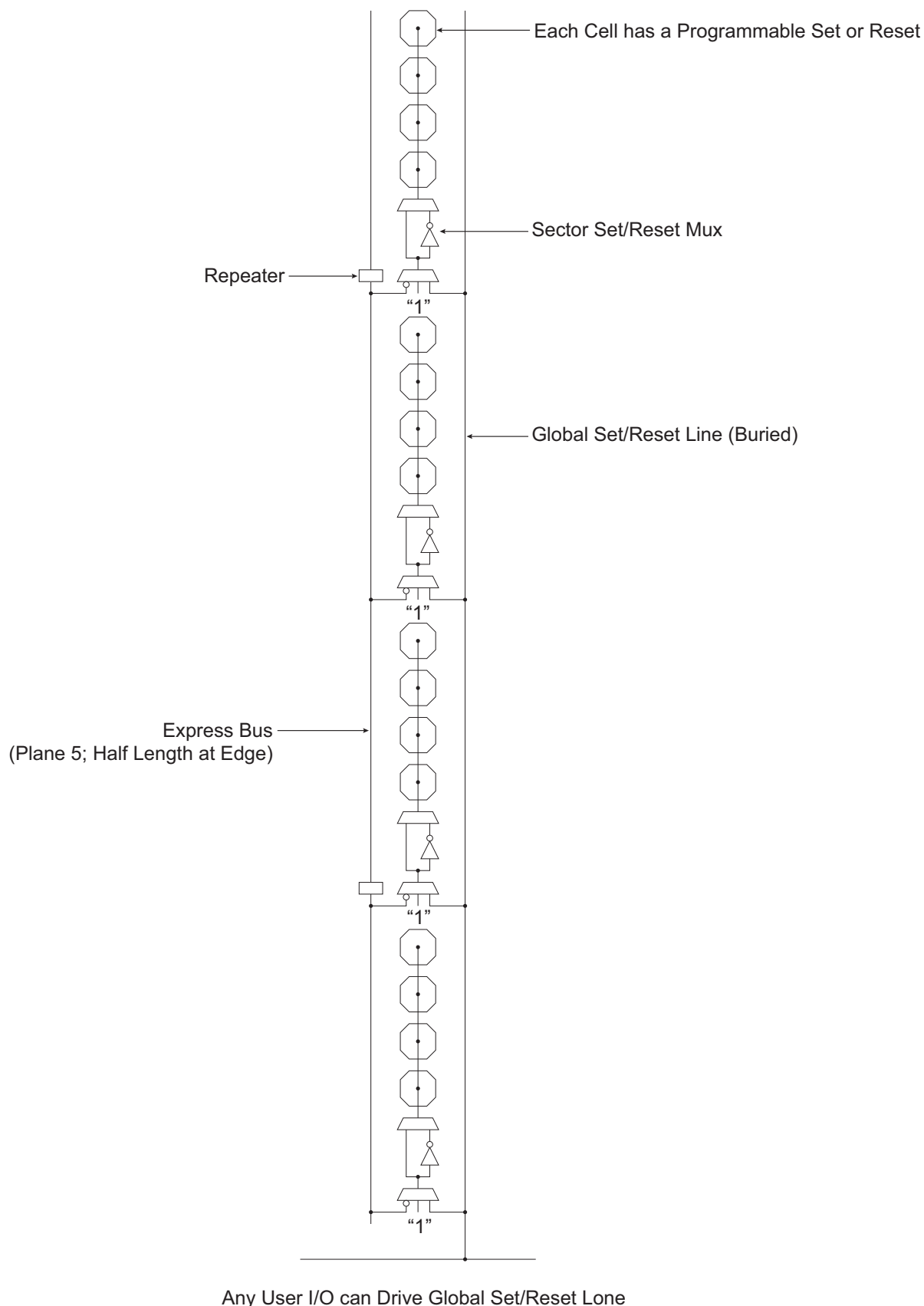
9. I/O Structure

9.1 Registered I/Os and Group Enable

The AT40KAL has registered I/Os and group enable every sector for tri-states on obuf's.

9.1.1 PAD

The I/O pad is the one that connects the I/O to the outside world.

Not all I/Os have pads: the ones without pads are called Unbonded I/Os. The number of unbonded I/Os varies with the device size and package. These unbonded I/Os are used to perform a variety of bus turns at the edge of the array.

9.1.2 PULL-UP/PULL-DOWN

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak one or zero level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The input stage of each I/O cell has a number of parameters that can be programmed either as properties in schematic entry or in the I/O Pad Attributes editor in IDS.

9.1.3 CMOS

The threshold level is a CMOS-compatible level.

9.1.4 SCHMITT

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 1V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

9.1.5 DELAYS

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

9.1.6 DRIVE

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW (using IDS tool). The FAST setting has the highest drive capability (20 mA at 5V) buffer and the fastest slew rate. MEDIUM produces a medium drive (14 mA at 5V) buffer, while SLOW yields a standard (6 mA at 5V) buffer.

9.1.7 TRI-STATE

The output of each I/O can be made tri-state (0, 1 or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O's Source Selection mux. Of course, the output can be normal (0 or 1), as well.

9.1.8 SOURCE SELECTION MUX

The Source Selection mux selects the source for the output signal of an I/O.

9.2 Primary, Secondary, and Corner I/Os

The AT40KAL has three kinds of I/Os:

- Primary I/O
- Secondary I/O
- Corner I/O

Every edge cell except corner cells on the AT40KAL has access to one Primary I/O and two Secondary I/Os.

9.2.1 Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figure 9-1.

9.2.2 Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 9-2.

9.2.3 Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os:

- 2 Primary
- 2 Secondary
- 1 Corner I/O

Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KAL FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 9-3.

Figure 9-1. West Primary I/O (Mirrored for East I/O)
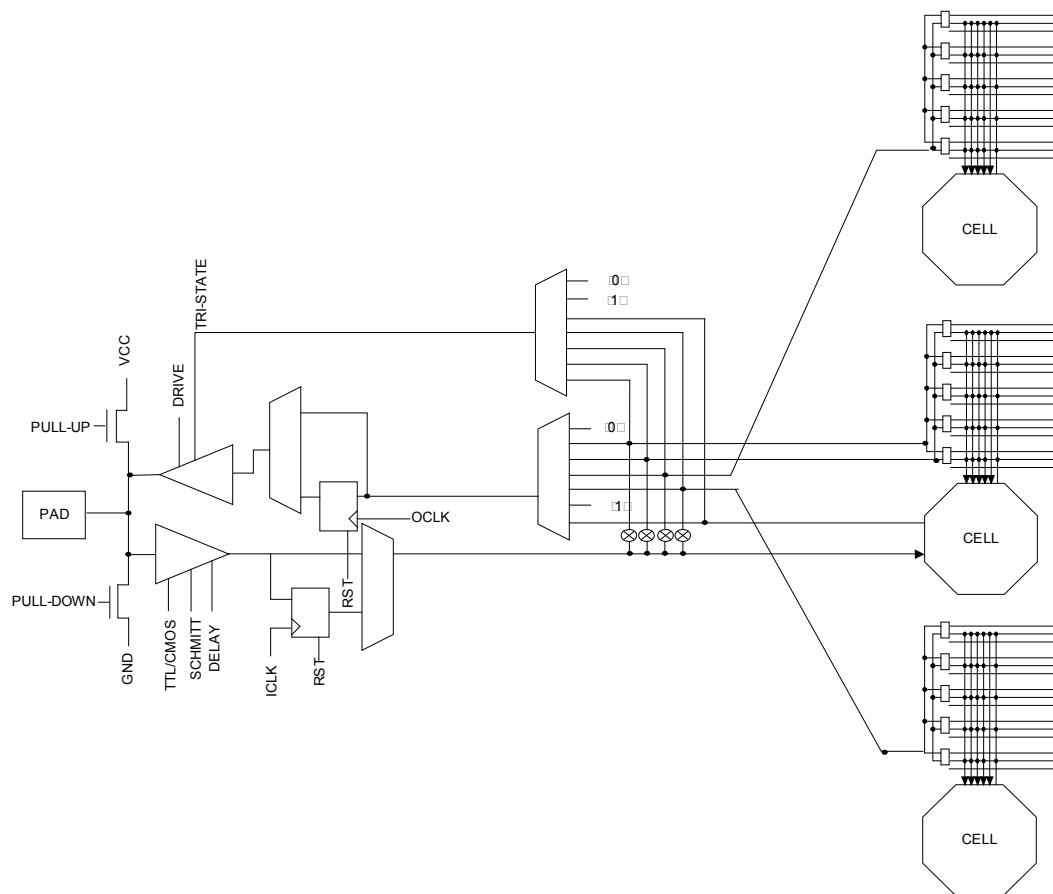
Figure 9-2. West Secondary I/O (Mirrored for East I/O)
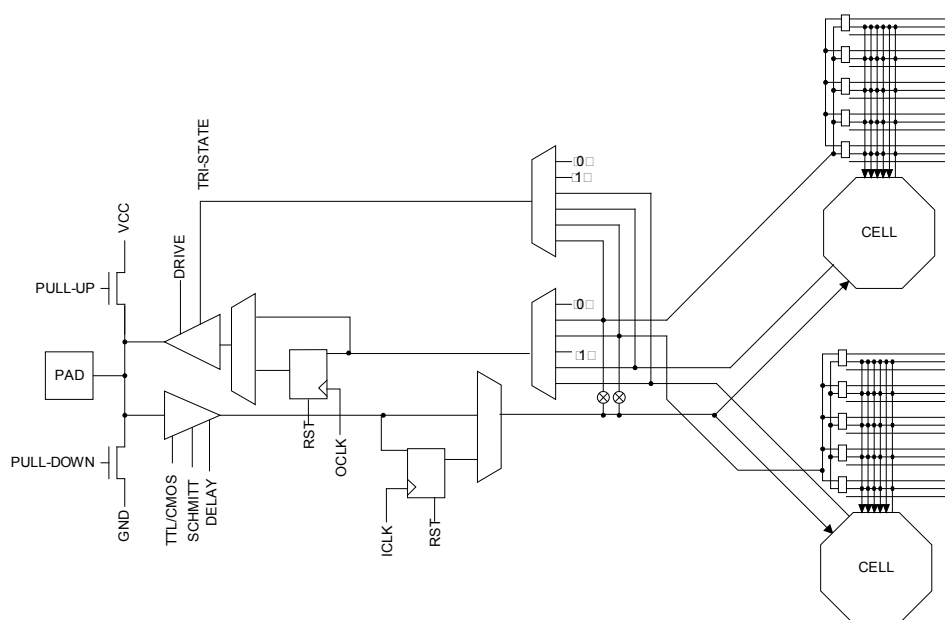
Figure 9-3.   Northwest Corner I/O (Similar NE/SE/SW Corners)
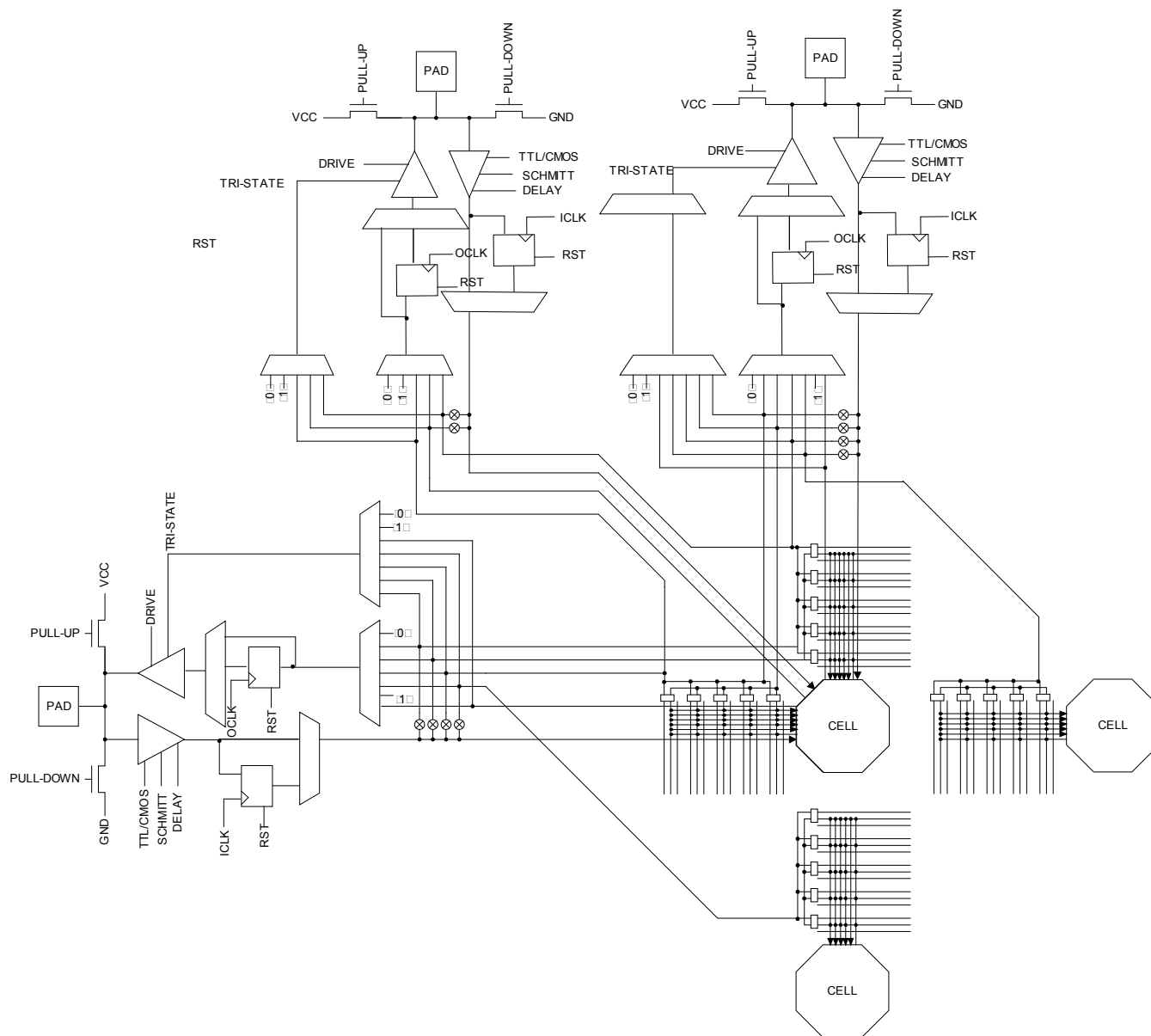
10. Absolute Maximum Ratings: 3.3V Commercial/Industrial*

Operating Temperature . . . . -55°C to +125°C

Storage Temperature . . . . -65°C to +150°C

Voltage on Any Pin
with Respect to Ground . . . .-0.5V to V_{CC} +7V

Supply Voltage (V_{CC}). . . . .-0.5V to +7.0V

ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF). 2000V

*Notice: Stresses beyond those listed under Absolute
Maximum Ratings may cause permanent damage to
the device. This is a stress rating only and functional
operation of the device at these or any other
conditions beyond those listed under operating
conditions is not implied. Exposure to Absolute
Maximum Rating conditions for extended periods of
time may affect device reliability.

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11. Electrical Characteristics

11.1 DC and AC Operating Range: 3.3V Operation

	Commercial	Industrial
Operating Temperature (Case)	0°C to 70°C	-40°C to 85°C
V_{CC} Power Supply	3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS) — High (V_{IHC})	70% to 100% V_{CC}	70% to 100% V_{CC}
Input Voltage Level (CMOS) — Low (V_{ILC})	0 to 30% V_{CC}	0 to 30% V_{CC}

11.2 DC Characteristics: 3.3V Operation Commercial/Industrial

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	0.7 V_{CC}		5.5V	V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
V_{OH}	High-level Output Voltage	I_{OH} = 4mA, V_{CC} = V_{CC} Minimum	2.1			V
V_{OH}	High-level Output Voltage	I_{OH} = 12mA, V_{CC} = 3.0V	2.1			V
V_{OH}	High-level Output Voltage	I_{OH} = 16mA, V_{CC} = 3.0V	2.1			V
V_{OL}	Low-level Output Voltage	I_{OL} = -4mA, V_{CC} = 3.0V			0.4	V
V_{OL}	Low-level Output Voltage	I_{OL} = -12mA, V_{CC} = 3.0V			0.4	V
V_{OL}	Low-level Output Voltage	I_{OL} = -16mA, V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10	µA
I_{IH}	High-level Input Current	With Pull-down, V_{IN} = V_{CC}	75	150	300	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10			µA
I_{IL}	Low-level Input Current	With Pull-up, V_{IN} = V_{SS}	-300	-150	-75	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without Pull-down, V_{IN} = V_{CC} Maximum			10	µA
I_{OZH}	High-level Tri-state Output Leakage Current	With Pull-down, V_{IN} = V_{CC} Maximum	75	150	300	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without Pull-up, V_{IN} = V_{SS}	-10			mA
I_{OZL}	Low-level Tri-state Output Leakage Current	With Pull-up, V_{IN} = V_{SS}	CON = -500µA TO -125µA	-150	CON = -500µA TO -125µA	µA
I_{CC}	Standby Current Consumption	Standby, Unprogrammed		0.6	1	mA
C_{IN}	Input Capacitance	All Pins			10	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

11.3 Power-On Power Supply Requirements

Atmel FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time.

Table 11-1.   Power-On Power Supply Requirements[1]

Device	Description	Maximum Current[2][3]
AT40K05AL	Maximum Current Supply	50mA
AT40K10AL		
AT40K20AL	Maximum Current Supply	100mA
AT40K40AL		

Notes: 1. This specification applies to Commercial and Industrial grade products only.
  2. Devices are guaranteed to initialize properly at 50% of the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
  3. Ramp-up time is measured from 0VDC to 3.6VDC. Peak current required lasts less than 2ms, and occurs near the internal power on reset threshold voltage.

11.4 AC Timing Characteristics: 3.3V Operation

Table 11-2. Core

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-1	Units	Notes
2-input Gate	t_{PD} (Maximum)	x/y → x/y	1.8	ns	1 Unit Load
3-input Gate	t_{PD} (Maximum)	x/y/z → x/y	2.1	ns	1 Unit Load
		x/y/w → x/y	2.2		
4-input Gate	t_{PD} (Maximum)	x/y/w/z → x/y	2.2	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	y → y	1.4	ns	1 Unit Load
		x → y	1.7		
		y → x	1.8		
		x → x	1.5		
		w → y	2.2		
		w → x	2.3		
		z → y	2.3		
		z → x	1.7		
DFF	t_{PD} (Maximum)	q → x/y	1.8	ns	1 Unit Load
		R → x/y	2.2		
		S → x/y	2.2		
		q → w	1.8		
Incremental -> L	t_{PD} (Maximum)	x/y → L	1.5	ns	1 Unit Load
Local Output Enable	t_{PZX} (Maximum)	oe → L	1.4	ns	1 Unit Load
			1.8		

Table 11-3. **Repeaters and IO** [1][2]

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-1	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L → E	1.3	ns	1 Unit Load
		E → E			
		L → L			
		E → L			
		E → IO	0.8		
		L → IO			
IO					
Input	t_{PD} (Maximum)	pad → x/y	1.2	ns	No Extra Delay
			3.6		1 Extra Delay
			7.3		2 Extra Delays
			10.8		3 Extra Delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L → pad	5.9	ns	50pf Load
Output, Medium	t_{PD} (Maximum)	x/y/E/L → pad	4.8	ns	50pf Load
Output, Fast	t_{PD} (Maximum)	x/y/E/L → pad	3.9	ns	50pf Load
Output, Slow	t_{PZX} (Maximum)	oe → pad	6.2	ns	50pf Load
			1.3		
Output, Medium	t_{PZX} (Maximum)	oe → pad	4.8	ns	50pf Load
			1.9		
Output, Fast	t_{PZX} (Maximum)	oe → pad	3.7	ns	50pf Load
			1.6		

Notes: 1. All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}.
2. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

AT40KAL Series FPGA [Datasheet]
Atmel-2818G-FPGA-AT40KAL-Series-Datasheet_092013

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Table 11-4.   Global Clocks and Set/Reset [1]

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	Device	-1	Units	Notes
GCLK Input Buffer	t_{PD} (Maximum)	pad → clock	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	1.1 1.2 1.2 1.4	ns	Rising Edge Clock
FCLK Input Buffer	t_{PD} (Maximum)	pad → clock	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	0.7 0.8 0.8 0.8	ns	Rising Edge Clock
Clock Column Driver	t_{PD} (Maximum)	clock → colclk	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	0.8 0.9 1.0 1.1	ns	Rising Edge Clock
Clock Sector Driver	t_{PD} (Maximum)	colclk → secclk	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	0.5	ns	Rising Edge Clock
GSRN Input Buffer	t_{PD} (Maximum)	pad → GSRN	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	3.0 3.7 4.3 5.6	ns	From Any Pad to Global Set/Reset Network
Global Clock to Output	t_{PD} (Maximum)	clock pad → out	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	8.3 8.4 8.6 8.8	ns	Rising Edge Clock Fully Loaded Clock Tree Rising Edge DFF 20mA Output Buffer 50pf Pin Load
Fast Clock to Output	t_{PD} (Maximum)	clock pad → out	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	7.9 8.0 8.1 8.3	ns	Rising Edge Clock Fully Loaded Clock Tree Rising Edge DFF 20mA Output Buffer 50pf Pin Load

Note: 1.   Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Table 11-5.   Async and Sync RAM

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-1	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	
	t_{WEL} (Minimum)	we	5.0		Pulse width low
	t_{WEH} (Minimum)	we	5.0		Pulse width high
	t_{AWS} (Minimum)	wr addr setup → we	5.3		
	t_{AWH} (Minimum)	wr addr hold → we	0.0		
	t_{DS} (Minimum)	din setup → we	5.0		
	t_{DH} (Minimum)	din hold → we	0.0		
Write/Read	t_{DD} (Maximum)	din → dout	8.7	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr → dout	6.3	ns	
	t_{OZX} (Maximum)	oe → dout	2.9		
	t_{OXZ} (Maximum)	oe → dout	3.5		
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
	t_{CLKL} (Minimum)	clk	5.0		Pulse width low
	t_{CLKH} (Minimum)	clk	5.0		Pulse width high
	t_{WCS} (Minimum)	we setup → clk	3.2		
	t_{WCH} (Minimum)	we hold → clk	0.0		
	t_{ACS} (Minimum)	wr addr setup → clk	5.0		
	t_{ACH} (Minimum)	wr addr hold → clk	0.0		
	t_{DCS} (Minimum)	wr data setup → clk	3.9		
	t_{DCH} (Minimum)	wr data hold → clk	0.0		
Write/Read	t_{CD} (Maximum)	clk → dout	5.8	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr → dout	6.3	ns	
	t_{OZX} (Maximum)	oe → dout	2.9		
			3.5		

Notes: 1.   CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.

2.   Buffer delay is to a pad voltage of 1.5V with one output switching.

3.   Parameter based on characterization and simulation; not tested in production.

4.   Exact power calculation is available in Atmel FPGA Designer software.

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11.5 FreeRAM Asynchronous Timing Characteristics

11.5.1 Single-port Write/Read
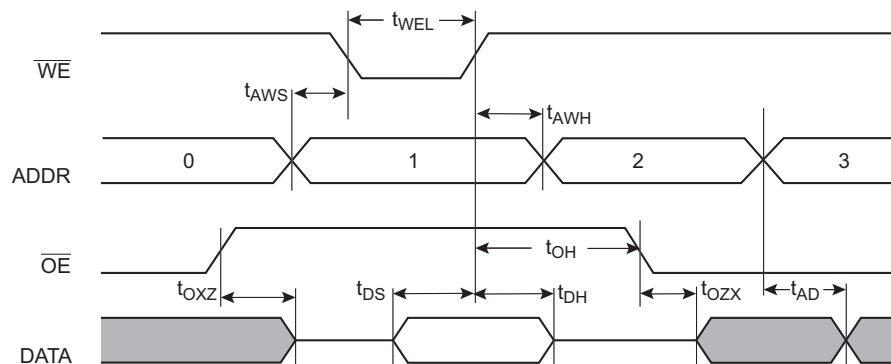
11.5.2 Dual-port Write with Read
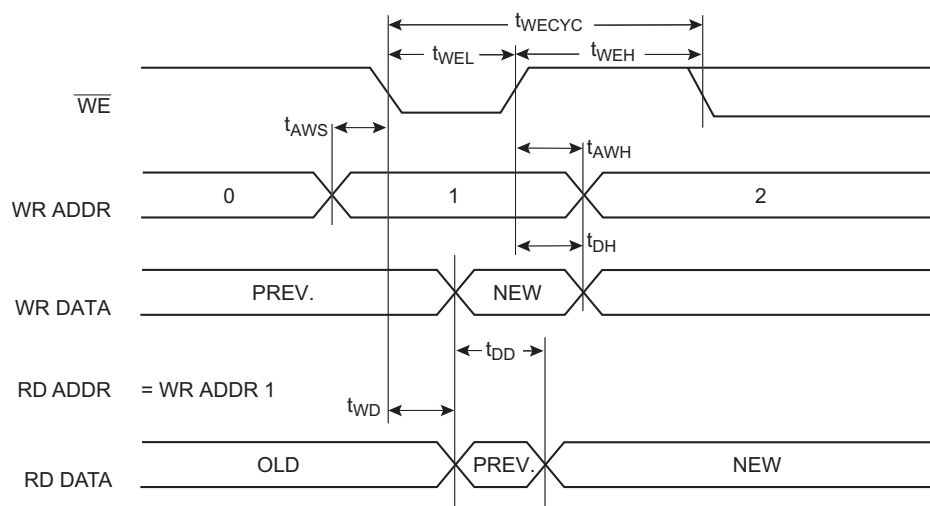
11.5.3 Dual-port Read
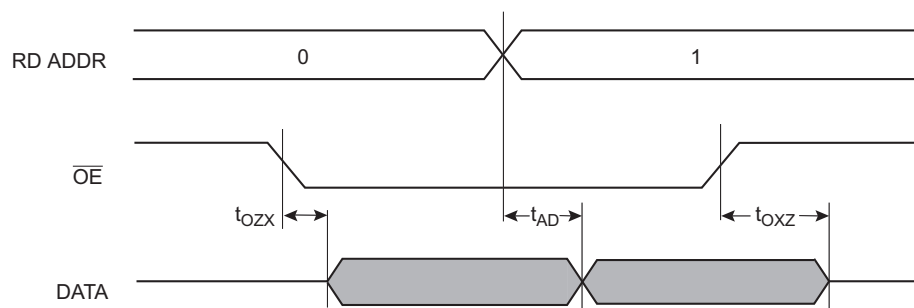
11.6 FreeRAM Synchronous Timing Characteristics

11.6.1 Single-port Write/Read
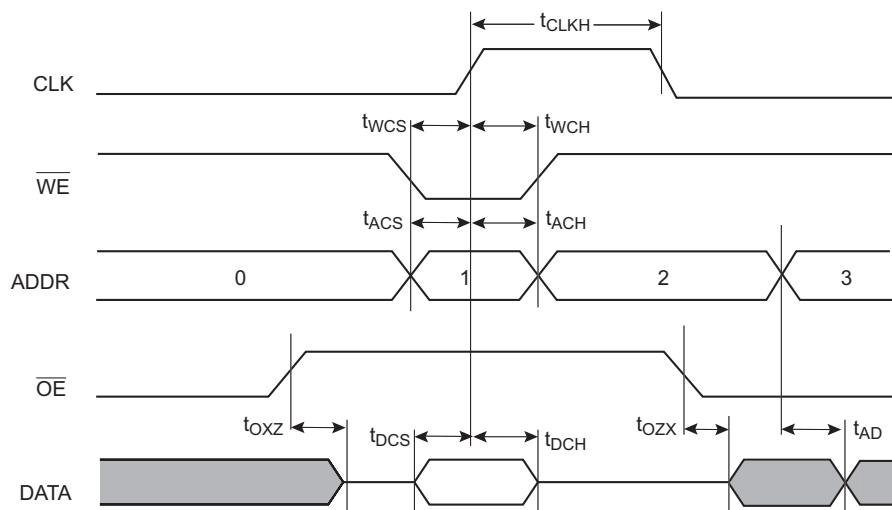
11.6.2 Dual-port Write with Read
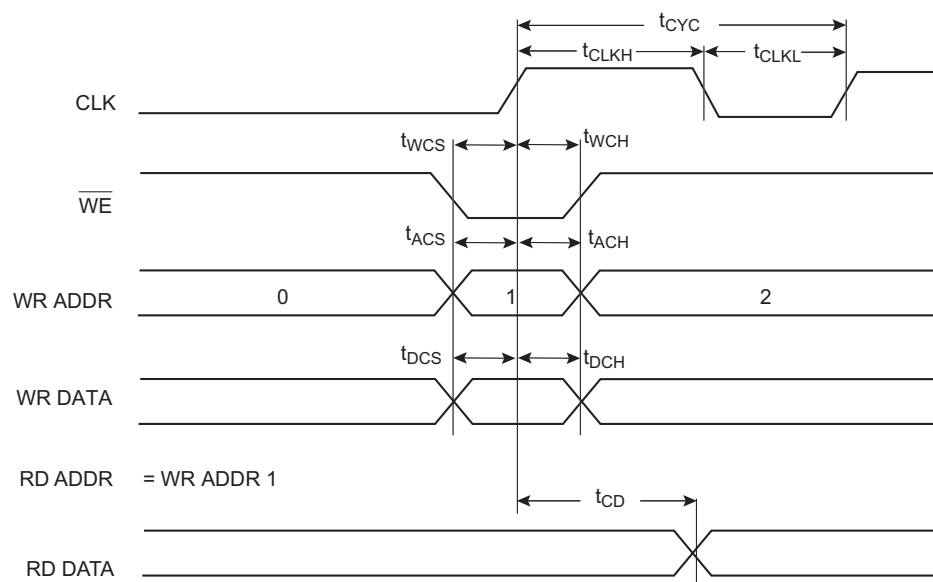
11.6.3 Dual-port Read

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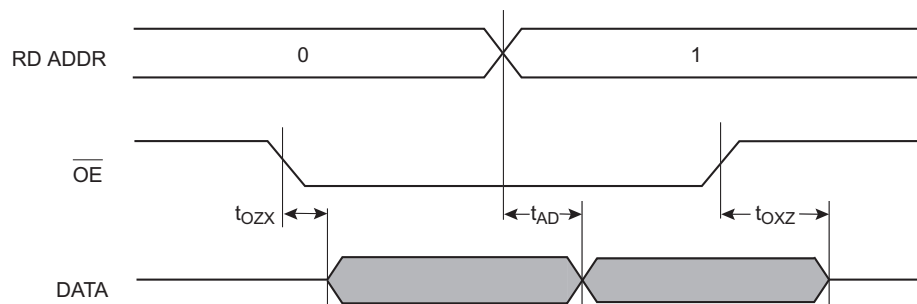
Table 11-6.   Left Side (Top to Bottom)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	12	1	1	2	1
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	2	2	4	2
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	3	3	5	3
I/O3	I/O3	I/O3	I/O3			4	6	4
I/O4	I/O4	I/O4	I/O4			5	7	5
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	4	6	8	6
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	5	7	9	7
			GND					
			I/O7					
			I/O8					
			I/O9					
			I/O10					
		I/O7	I/O11					
		I/O8	I/O12					
		VCC	VCC					
		GND	GND					
			I/O13					
			I/O14					
I/O7	I/O7	I/O9	I/O15				10	8
I/O8	I/O8	I/O10	I/O16				11	9
	I/O9	I/O11	I/O17				12	10
	I/O10	I/O12	I/O18				13	11
			GND					
			I/O19					
			I/O20					
	I/O11	I/O13	I/O21					12
	I/O12	I/O14	I/O22					13
		I/O15	I/O23					
		I/O16	I/O24					
GND	GND	GND	GND			8	14	14

Note: 1.   On-chip tri-state

Table 11-6.   Left Side (Top to Bottom) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O9, FCK1	I/O13, FCK1	I/O17, FCK1	I/O25, FCK1			9	15	15
I/O10	I/O14	I/O18	I/O26			10	16	16
I/O11 (A20)	I/O15 (A20)	I/O19 (A20)	I/O27 (A20)	17	6	11	17	17
I/O12 (A21)	I/O16 (A21)	I/O20 (A21)	I/O28 (A21)	18	7	12	18	18
	VCC	VCC	VCC					19
	I/O17	I/O21	I/O29					20
	I/O18	I/O22	I/O30					21
			GND					
			I/O31					
			I/O32					
			I/O33					
			I/O34					
		I/O23	I/O35					
		I/O24	I/O36					
		GND	GND					22
			VCC					
			I/O37					
			I/O38					
		I/O25	I/O39					
		I/O26	I/O40					
	I/O19	I/O27	I/O41				19	23
	I/O20	I/O28	I/O42				20	24
			GND					
I/O13	I/O21	I/O29	I/O43			13	21	25
I/O14	I/O22	I/O30	I/O44		8	14	22	26
			I/O45					
			I/O46					
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	9	15	23	27
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	10	16	24	28
GND	GND	GND	GND	21	11	17	25	29

Note: 1.   On-chip tri-state

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Table 11-6. Left Side (Top to Bottom) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	22	12	18	26	30
I/O17	I/O25	I/O33	I/O49	23	13	19	27	31
I/O18	I/O26	I/O34	I/O50	24	14	20	28	32
			I/O51					
			I/O52					
I/O19	I/O27	I/O35	I/O53		15	21	29	33
I/O20	I/O28	I/O36	I/O54			22	30	34
			GND					
	I/O29	I/O37	I/O55				31	35
	I/O30	I/O38	I/O56				32	36
		I/O39	I/O57					
		I/O40	I/O58					
			I/O59					
			I/O60					
			VCC					
		GND	GND					37
		I/O41	I/O61					
		I/O42	I/O62					
			I/O63					
			I/O64					
			I/O65					
			I/O66					
			GND					
	I/O31	I/O43	I/O67					38
	I/O32	I/O44	I/O68					39
	VCC	VCC	VCC					40
I/O21	I/O33	I/O45	I/O69	25	16	23	33	41
I/O22	I/O34	I/O46	I/O70	26	17	24	34	42
I/O23	I/O35	I/O47	I/O71			25	35	43
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2			26	36	44
GND	GND	GND	GND			27	37	45
		I/O49	I/O73					

Note: 1.   On-chip tri-state

Table 11-6.   Left Side (Top to Bottom) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
		I/O50	I/O74					
	I/O37	I/O51	I/O75					46
	I/O38	I/O52	I/O76					47
			I/O77					
			I/O78					
			GND					
			I/O79					
			I/O80					
	I/O39	I/O53	I/O81				38	48
	I/O40	I/O54	I/O82				39	49
I/O25	I/O41	I/O55	I/O83				40	50
I/O26	I/O42	I/O56	I/O84				41	51
		GND	GND					
		VCC	VCC					
		I/O57	I/O85					
		I/O58	I/O86					
			I/O87					
			I/O88					
I/O27	I/O43	I/O59	I/O89	27	18	28	42	52
I/O28	I/O44	I/O60	I/O90		19	29	43	53
			GND					
			I/O91					
			I/O92					
I/O29	I/O45	I/O61	I/O93			30	44	54
I/O30	I/O46	I/O62	I/O94			31	45	55
I/O31 (OTS)[1]	I/O47 (OTS)[1]	I/O63 (OTS)[1]	I/O95 (OTS)[1]	28	20	32	46	56
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	21	33	47	57
M1	M1	M1	M1	30	22	34	48	58
GND	GND	GND	GND	31	23	35	49	59
M0	M0	M0	M0	32	24	36	50	60

Note: 1.   On-chip tri-state

AT40KAL Series FPGA [Datasheet]
Atmel-2818G-FPGA-AT40KAL-Series-Datasheet_092013

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Table 11-7.   Bottom Side (Left to Right)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	33	25	37	55	61
M2	M2	M2	M2	34	26	38	56	62
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	27	39	57	63
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	28	40	58	64
I/O35	I/O51	I/O67	I/O99			41	59	65
I/O36	I/O52	I/O68	I/O100			42	60	66
I/O37	I/O53	I/O69	I/O101		29	43	61	67
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	30	44	62	68
			GND					
			I/O103					
			I/O104					
			I/O105					
			I/O106					
		I/O71	I/O107					
		I/O72	I/O108					
		VCC	VCC					
		GND	GND					
I/O39	I/O55	I/O73	I/O109				63	69
I/O40	I/O56	I/O74	I/O110				64	70
	I/O57	I/O75	I/O111				65	71
	I/O58	I/O76	I/O112				66	72
			I/O113					
			I/O114					
			GND					
		I/O77	I/O115					
		I/O78	I/O116					
	I/O59	I/O79	I/O117					73
	I/O60	I/O80	I/O118					74
			I/O119					
			I/O120					
GND	GND	GND	GND			45	67	75
I/O41	I/O61	I/O81	I/O121			46	68	76

Table 11-7. Bottom Side (Left to Right) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O42	I/O62	I/O82	I/O122			47	69	77
I/O43	I/O63	I/O83	I/O123	38	31	48	70	78
I/O44	I/O64	I/O84	I/O124	39	32	49	71	79
	VCC	VCC	VCC					80
	I/O65	I/O85	I/O125				72	81
	I/O66	I/O86	I/O126				73	82
			GND					
			I/O127					
			I/O128					
			I/O129					
			I/O130					
		I/O87	I/O131					
		I/O88	I/O132					
		GND	GND					83
			VCC					
		I/O89	I/O133					
		I/O90	I/O134					
	I/O67	I/O91	I/O135					84
	I/O68	I/O92	I/O136					85
I/O45	I/O69	I/O93	I/O137		33	50	74	86
I/O46	I/O70	I/O94	I/O138		34	51	75	87
			GND					
			I/O139					
			I/O140					
			I/O141					
			I/O142					
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	35	52	76	88
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	36	53	77	89
VCC	VCC	VCC	VCC	42	37	54	78	90
GND	GND	GND	GND	43	38	55	79	91
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	39	56	80	92

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Table 11-7. Bottom Side (Left to Right) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	40	57	81	93
			I/O147					
			I/O148					
			I/O149					
			I/O150					
			GND					
I/O51	I/O75	I/O99	I/O151		41	58	82	94
I/O52	I/O76	I/O100	I/O152		42	59	83	95
	I/O77	I/O101	I/O153				84	96
	I/O78	I/O102	I/O154				85	97
		I/O103	I/O155					
		I/O104	I/O156					
			VCC					
		GND	GND					98
		I/O105	I/O157					
		I/O106	I/O158					
			I/O159					
			I/O160					
			I/O161					
			I/O162					
			GND					
	I/O79	I/O107	I/O163					99
	I/O80	I/O108	I/O164					100
	VCC	VCC	VCC					101
I/O53 (D12)	I/O81 (D12)	I/O109 (D12)	I/O165 (D12)	46	43	60	86	102
I/O54 (D11)	I/O82 (D11)	I/O110 (D11)	I/O166 (D11)	47	44	61	87	103
I/O55	I/O83	I/O111	I/O167			62	88	104
I/O56	I/O84	I/O112	I/O168			63	89	105
GND	GND	GND	GND			64	90	106
		I/O113	I/O169					
		I/O114	I/O170					
	I/O85	I/O115	I/O171					107

Table 11-7.   Bottom Side (Left to Right) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O86	I/O116	I/O172					108
			I/O173					
			I/O174					
			GND					
			I/O175					
			I/O176					
	I/O87	I/O117	I/O177				91	109
	I/O88	I/O118	I/O178				92	110
I/O57	I/O89	I/O119	I/O179				93	111
I/O58	I/O90	I/O120	I/O180				94	112
		GND	GND					
		VCC	VCC					
		I/O121	I/O181					
		I/O122	I/O182					
I/O59 (D10)	I/O91 (D10)	I/O123 (D10)	I/O183 (D10)	48	45	65	95	113
I/O60 (D9)	I/O92 (D9)	I/O124 (D9)	I/O184 (D9)	49	46	66	96	114
			I/O185					
			I/O186					
			GND					
			I/O187					
			I/O188					
I/O61	I/O93	I/O125	I/O189			67	97	115
I/O62	I/O94	I/O126	I/O190			68	98	116
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	47	69	99	117
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192, GCK4	51	48	70	100	118
GND	GND	GND	GND	52	49	71	101	119
$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	53	50	72	103	120

Table 11-8. Right Side (Bottom to Top)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	54	51	73	106	121
RESET	RESET	RESET	RESET	55	52	74	108	122
I/O65 (D7)	I/O97 (D7)	I/O129 (D7)	I/O193 (D7)	56	53	75	109	123
I/O66, GCK5	I/O98, GCK5	I/O130, GCK5	I/O194, GCK5	57	54	76	110	124
I/O67	I/O99	I/O131	I/O195			77	111	125
I/O68	I/O100	I/O132	I/O196			78	112	126
		I/O133	I/O197					
		I/O134	I/O198					
			GND					
	I/O101	I/O135	I/O199					127
	I/O102	I/O136	I/O200					128
			I/O201					
			I/O202					
			I/O203					
			I/O204					
		VCC	VCC					
		GND	GND					
I/O69 (D6)	I/O103 (D6)	I/O137 (D6)	I/O205 (D6)	58	55	79	113	129
I/O70	I/O104	I/O138	I/O206		56	80	114	130
I/O71	I/O105	I/O139	I/O207				115	131
I/O72	I/O106	I/O140	I/O208				116	132
			I/O209					
			I/O210					
			GND					
			I/O211					
			I/O212					
	I/O107	I/O141	I/O213				117	133
	I/O108	I/O142	I/O214				118	134
		I/O143	I/O215					
		I/O144	I/O216					
GND	GND	GND	GND			81	119	135
	I/O109	I/O145	I/O217					136

Table 11-8.   Right Side (Bottom to Top) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O110	I/O146	I/O218					137
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3			82	120	138
I/O74	I/O112	I/O148	I/O220			83	121	139
	VCC	VCC	VCC					140
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	57	84	122	141
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	58	85	123	142
			GND					
			I/O223					
			I/O224					
			I/O225					
			I/O226					
		I/O151	I/O227					
		I/O152	I/O228					
		GND	GND					143
			VCC					
			I/O229					
			I/O230					
		I/O153	I/O231					
		I/O154	I/O232					
	I/O115	I/O155	I/O233				124	144
	I/O116	I/O156	I/O234				125	145
			GND					
I/O77	I/O117	I/O157	I/O235		59	86	126	146
I/O78	I/O118	I/O158	I/O236		60	87	127	147
			I/O237					
			I/O238					
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	61	88	128	148
I/O80	I/O120	I/O160	I/O240	62	62	89	129	149
VCC	VCC	VCC	VCC	63	63	90	130	150
GND	GND	GND	GND	64	64	91	131	151
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	65	92	132	152

AT40KAL Series FPGA [Datasheet]
Atmel-2818G-FPGA-AT40KAL-Series-Datasheet_092013

Atmel

Table 11-8.   Right Side (Bottom to Top) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O82 ($\overline{\text{CHECK}}$)	I/O122 ($\overline{\text{CHECK}}$)	I/O162 ($\overline{\text{CHECK}}$)	I/O242 ($\overline{\text{CHECK}}$)	66	66	93	133	153
			I/O243					
			I/O244					
I/O83	I/O123	I/O163	I/O245		67	94	134	154
I/O84	I/O124	I/O164	I/O246			95	135	155
			GND					
	I/O125	I/O165	I/O247				136	156
	I/O126	I/O166	I/O248				137	157
		I/O167	I/O249					
		I/O168	I/O250					
			I/O251					
			I/O252					
			VCC					
		GND	GND					158
		I/O169	I/O253					
		I/O170	I/O254					
			I/O255					
			I/O256					
			I/O257					
			I/O258					
			GND					
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	68	96	138	159
I/O86	I/O128	I/O172	I/O260	68	69	97	139	160
	VCC	VCC	VCC					161
I/O87	I/O129	I/O173	I/O261			98	140	162
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4			99	141	163
	I/O131	I/O175	I/O263					164
	I/O132	I/O176	I/O264					165
GND	GND	GND	GND			100	142	166
		I/O177	I/O265					
		I/O178	I/O266					
	I/O133	I/O179	I/O267					167

Table 11-8. Right Side (Bottom to Top) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O134	I/O180	I/O268					168
			I/O269					
			I/O270					
			GND					
	I/O135	I/O181	I/O271				143	169
	I/O136	I/O182	I/O272				144	170
I/O89	I/O137	I/O183	I/O273				145	171
I/O90	I/O138	I/O184	I/O274				146	172
			I/O275					
			I/O276					
		GND	GND					
		VCC	VCC					
I/O91 (D1)	I/O139 (D1)	I/O185 (D1)	I/O277 (D1)	69	70	101	147	173
I/O92	I/O140	I/O186	I/O278	70	71	102	148	174
			I/O279					
			I/O280					
			I/O281					
			I/O282					
			GND					
		I/O187	I/O283					
		I/O188	I/O284					
I/O93	I/O141	I/O189	I/O285			103	149	175
I/O94	I/O142	I/O190	I/O286			104	150	176
I/O95 (D0)	I/O143 (D0)	I/O191 (D0)	I/O287 (D0)	71	72	105	151	177
I/O96, GCK6 ($\overline{\text{CSOUT}}$)	I/O144, GCK6 ($\overline{\text{CSOUT}}$)	I/O192, GCK6 ($\overline{\text{CSOUT}}$)	I/O288, GCK6 ($\overline{\text{CSOUT}}$)	72	73	106	152	178
CCLK	CCLK	CCLK	CCLK	73	74	107	153	179
VCC	VCC	VCC	VCC	74	75	108	154	180
TSTCLK	TSTCLK	TSTCLK	TSTCLK	75	76	109	159	181

Table 11-9.   Top Side (Right to Left)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	76	77	110	160	182
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	78	111	161	183
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	79	112	162	184
I/O99	I/O147	I/O195	I/O291			113	163	185
I/O100	I/O148	I/O196	I/O292			114	164	186
			I/O293					
			I/O294					
			GND					
			I/O295					
			I/O296					
I/O101 ($\overline{CS1}$,A2)	I/O149 ($\overline{CS1}$,A2)	I/O197 ($\overline{CS1}$,A2)	I/O297 ($\overline{CS1}$,A2)	79	80	115	165	187
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	81	116	166	188
		I/O199	I/O299					
		I/O200	I/O300					
		VCC	VCC					
		GND	GND					
	I/O151[1]	I/O201[1]	I/O301[1]	75[1] NC	76[1] NC	109[1] NC	159[1] NC	189[1] NC
	I/O152	I/O202	I/O302					190
I/O103	I/O153	I/O203	I/O303			117	167	191
I/O104[1]	I/O154	I/O204	I/O304				168	192
			I/O305					
			I/O306					
			GND					
			I/O307					
			I/O308					
	I/O155	I/O205	I/O309				169	193
	I/O156	I/O206	I/O310				170	194
		I/O207	I/O311					195
		I/O208	I/O312					

Note: 1.   Shared with TSTCLK. No Connect.

Table 11-9.   Top Side (Right to Left) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND			118	171	196
I/O105	I/O157	I/O209	I/O313			119	172	197
I/O106	I/O158	I/O210	I/O314			120	173	198
	I/O159	I/O211	I/O315					199
	I/O160	I/O212	I/O316					200
	VCC	VCC	VCC					201
		I/O213	I/O317					
		I/O214	I/O318					
			GND					
			I/O319					
			I/O320					
			I/O321					
			I/O322					
		I/O215	I/O323					
		I/O216	I/O324					
		GND	GND					
			VCC					
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	82	121	174	202
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	83	122	175	203
	I/O163	I/O219	I/O327				176	205
	I/O164	I/O220	I/O328				177	206
I/O109	I/O165	I/O221	I/O329		84	123	178	207
I/O110	I/O166	I/O222	I/O330		85	124	179	208
			GND					
			I/O331					
			I/O332					
			I/O333					
			I/O334					
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	86	125	180	209
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	87	126	181	210
GND	GND	GND	GND	1	88	127	182	211

Note: 1.   Shared with TSTCLK. No Connect.

Table 11-9.   Top Side (Right to Left) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	2	89	128	183	212
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	90	129	184	213
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	91	130	185	214
			I/O339					
			I/O340					
			I/O341					
			I/O342					
			GND					
I/O115	I/O171	I/O227	I/O343		92	131	186	215
I/O116	I/O172	I/O228	I/O344		93	132	187	216
	I/O173	I/O229	I/O345				188	217
	I/O174	I/O230	I/O346				189	218
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	94	133	190	220
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	95	134	191	221
			VCC					
		GND	GND					
		I/O233	I/O349					
		I/O234	I/O350					
			I/O351					
			I/O352					
			I/O353					
			I/O354					
			GND					
		I/O235	I/O355					
		I/O236	I/O356					
	VCC	VCC	VCC					222
	I/O177	I/O237	I/O357					223
	I/O178	I/O238	I/O358					224
I/O119	I/O179	I/O239	I/O359			135	192	225
I/O120	I/O180	I/O240	I/O360			136	193	226
GND	GND	GND	GND			137	194	227

Note: 1.   Shared with TSTCLK. No Connect.

Table 11-9. Top Side (Right to Left) (Continued)

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
		I/O241	I/O361					
		I/O242	I/O362					
	I/O181	I/O243	I/O363				195	228
	I/O182	I/O244	I/O364				196	229
			I/O365					
			I/O366					
			GND					
			I/O367					
			I/O368					
I/O121	I/O183	I/O245	I/O369				197	230
I/O122	I/O184	I/O246	I/O370				198	231
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	96	138	199	232
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	97	139	200	233
		GND	GND					
		VCC	VCC					
		I/O249	I/O373					
		I/O250	I/O374					
			I/O375					
			I/O376					
			I/O377					
			I/O378					
			GND					
	I/O187	I/O251	I/O379					234
	I/O188	I/O252	I/O380					235
I/O125	I/O189	I/O253	I/O381			140	201	236
I/O126	I/O190	I/O254	I/O382			141	202	237
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	98	142	203	238
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	99	143	204	239
VCC	VCC	VCC	VCC	11	100	144	205	240

Note: 1. Shared with TSTCLK. No Connect.

12. Part/Package Availability and User I/O Counts (Including Dual-function Pins)

Package[1]	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
144 LQFP	114	114	114	—
208 PQFP	—	—	—	161

Note: 1. Devices in same package are pin-to-pin compatible.

Package Type	
144AA	144-lead, Low-profile (1.4mm) Plastic Quad Flat Package (LQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)

13. AT40KAL Series Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range
5,000 - 10,000	3.3V	1	AT40K05AL-1BQU	144AA	Industrial (-40°C to 85°C)
10,000 - 20,000			AT40K10AL-1BQU		
20,000 - 30,000			AT40K20AL-1BQU		
40,000 - 50,000			AT40K40AL-1DQU	208Q1	

14. Packaging Information

14.1 144AA — 144-lead LQFP

Top View

Bottom View

Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	1.35	1.40	1.45	
D	22.00 BSC			
D1	20.00 BSC			Note 2
E	22.00 BSC			
E1	20.00 BSC			Note 2
b	0.17	0.22	0.27	
C	0.09	–	0.20	
L	0.45	0.60	0.75	
e	0.50 TYP			

Notes: 1. This package conforms to JEDEC reference MS-026, Variation BFB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/19/2011

	Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **144AA**, 144-lead, 20 x 20 x 1.4mm Body, 0.50mm lead pitch, 2.0mm footprint, Low-profile Plastic Quad Flat Package (LQFP)	**GPC** AEI	**DRAWING NO.** 144AA	**REV.** D

14.2   208Q1 — 208-lead PQFP

Top View

Side View

Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D	30.60 BSC			
D1	28.00 BSC			2, 3
E	30.60 BSC			
E1	28.00 BSC			2, 3
e	0.50 BSC			
b	0.17	–	0.27	4
L1	1.30 REF			

Notes: 1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-1, for proper dimensions, tolerances, datums, etc.
  2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
  3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

03/10/05

Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	**DRAWING NO.** 208Q1	**REV.** C

15. Revision History

Doc. Rev.	Date	Comments
G	09/2013	Update Features section, AMR table, Part/Package Availablilty and User I/O Counts table, Ordering table, and document template and Atmel logos. Remove 84 PLCC, 100 TQFP, 240 PQFP package options. Update 144L1 to 144AA LQFP package.
F	07/2006	Add Green (Pb/Halide-free/RoHS Compliant) 144-lead LQFP.

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