APPLICATION NOTE

Application Hints for ATA5723/ATA5724/ATA5728

ATA5723/ATA5724/ATA5728

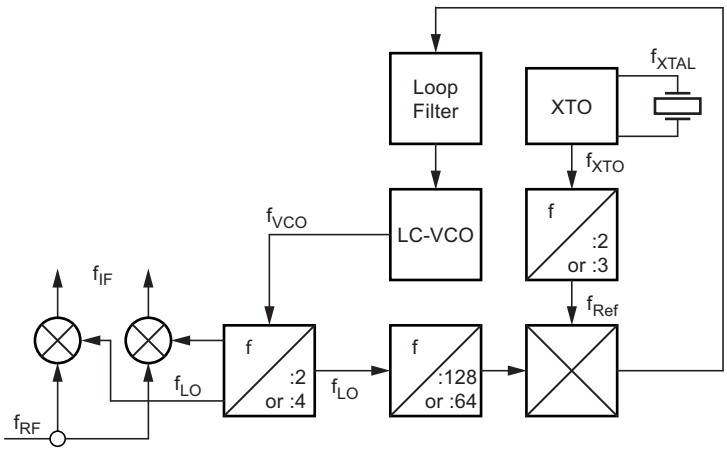
Introduction

The UHF receiver ATA5723, ATA5724, and ATA5728 are designed specially for automotive application like Remote Keyless Entry as well as Tire Pressure Monitoring System. These receivers are upgrades of ATA5743 and ATA5760. They have compatible pinning that allows the development of one layout for applications in three different ISM (industrial Scientific Medical) frequency bands. The frequency ranges are 312.5MHz to 317.5MHz, 431.5MHz to 436.5MHz and 868MHz to 870MHz. Another benefit of the receiver is the reuse of the software from Atmel®'s older receiver, the ATA5743. Additional features include the RSSI output, the pierce crystal oscillator achieving a better oscillation margin, an improved sensitivity as well as the image rejection.

The purpose of this application note is to give a designer some hints how to start developing a receiver module with ATA5723/ATA5724/ATA5728.

Calculating the Required Crystal Frequency

Figure 1. System Block Diagram for the Receivers Containing the Internal Frequency Generation and Processing (Synthesizer)



A reference frequency (f_{Ref}) in the receiver is based on the crystal oscillator's frequency (f_{XTO}), the loaded crystal resonance frequency (f_{XTAL}) respectively. The defined reference frequency is:

For ATA5723: $$f_{Ref} = \frac{f_{XTO}}{3}$$ Equation 1

For ATA5724: $$f_{Ref} = \frac{f_{XTO}}{2}$$ Equation 2

For ATA5728: $$f_{Ref} = \frac{f_{XTO}}{2}$$ Equation 3

The fixed intermediate frequencies (IF) for the receivers are:

IF of ATA5723 is 987kHz

IF of ATA5724 is 987kHz

IF of ATA5728 is 947.8kHz

The local oscillator frequency (f_{LO}) can be calculated as:

$f_{LO} = f_{RF} - f_{IF}$ Equation 4

The correlation between local oscillator frequency (f_{LO}) and the Voltage Oscillator frequency (f_{VCO}) is:

For ATA5723: $$f_{LO} = \frac{f_{VCO}}{4}$$ Equation 5

For ATA5724: $$f_{LO} = \frac{f_{VCO}}{4}$$ Equation 6

For ATA5728: $$f_{LO} = \frac{f_{VCO}}{2}$$ Equation 7

The reference frequency (f_{Ref}) will be compared with the local oscillator frequency divided by a factor of 64 or 128.

For ATA5723: $$f_{Ref} = \frac{f_{LO}}{64}$$ Equation 8

For ATA5724: $$f_{Ref} = \frac{f_{LO}}{64}$$ Equation 9

For ATA5728: $$f_{Ref} = \frac{f_{LO}}{128}$$ Equation 10

Using the aforementioned formulas, the crystal frequency for the receivers can be calculated as follows:

For ATA5723: $$f_{XTAL} = \frac{(f_{RF} - f_{IF}) \times 3}{64}$$ Equation 11

For ATA5724: $$f_{XTAL} = \frac{(f_{RF} - f_{IF}) \times 2}{64}$$ Equation 12

For ATA5728: $$f_{XTAL} = \frac{(f_{RF} - f_{IF}) \times 2}{128}$$ Equation 13

Example:

1. For the 315 MHz receiving frequency (ATA5723) the crystal frequency required can be calculated as follows:

   f_{RF} = 315MHz
   f_{IF} = 987kHz

   $$f_{XTAL} = \frac{(315\text{MHz} - 987\text{kHz}) \times 3}{64} = 14.71935938\text{MHz}$$

2. For the 433.92MHz receiving frequency (ATA5724) the crystal frequency required can be calculated as follows:

   f_{RF} = 433.92MHz
   f_{IF} = 987kHz

   $$f_{XTAL} = \frac{(433.92\text{MHz} - 987\text{kHz}) \times 2}{64} = 13.52915625$$

3. For the 868.3MHz receiving frequency (ATA5728) the crystal frequency required can be calculated as follows:

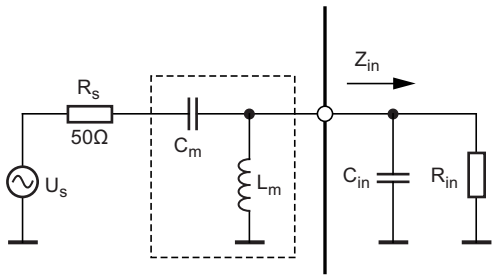
   f_{RF} = 868.3MHz
   f_{IF} = 947.8kHz

   $$f_{XTAL} = \frac{(868.3\text{MHz} - 947.8\text{kHz}) \times 2}{128} = 13.55237813\text{MHz}$$

1. Matching the Receiver Input to the 50Ω

The input matching for the optimal sensitivity is matching to 50Ω. This can be achieved with the LC high-pass filter combination. Figure 1-1 shows an LC matching network, the equivalent circuit of the receiver's input and the 50Ω generator source. This section provides some mathematical correlations, which help to find the start values in the tuning of the matching values to 50Ω impedance. The determined start values are used for the matching of Atmel's development boards. The results of the demo boards' matching will be shown.

Figure 1-1. LC Matching Network to 50Ω



The first important step is to find out the input impedance of the receivers and convert it into an equivalent parallel circuit. The input impedance of the receiver is listed below:

ATA5723 → Z_{in} = 26.97 – j158.7Ω at 315MHz

ATA5724 → Z_{in} = 19.3 – j113.3Ω at 433.92MHz

ATA5728 → Z_{in} = 14.15 – j73.53Ω at 868.3MHz

The admittance of the receiver (B_{in}) can be estimated from the impedance Z_{in}.

$$B_{in} = \frac{1}{Z_{in}} \qquad \text{Equation 14}$$

The input resistance R_{in} is:

$$R_{in} = \frac{1}{Re\{B_{in}\}} \qquad \text{Equation 15}$$

Thus the reactance of the parallel input capacitance C_{in} can be given as:

$$X_{in} = \frac{1}{Im\{B_{in}\}} \qquad \text{Equation 16}$$

Using equation 17, the quality factor of the matching network (Q_m) can be estimated.

$$Q_m = \sqrt{\frac{R_{in}}{R_s} + 1} \qquad \text{Equation 17}$$

The matching capacitance is derived from the reactance of the matching network and can be given as:

$$C_m = \frac{1}{2\pi f X_m} \qquad \text{Equation 18}$$

The ideal inductor value can be calculated with equation 19:

$$L_m = \frac{X_{in} - X_m}{2\pi f(X_{in} + X_m)} \qquad \text{Equation 19}$$

From the equations 18 and 19 the start values of the matching elements for tuning purpose can be calculated:

ATA5723 at 315 MHz would be: L_m = 46.8nH (≈47nH); C_m = 2.36pF (≈2.2pF)

ATA5724 at 433.92 MHz would be: L_m = 25.9nH (≈27nH); C_m = 2.05pF (≈2pF)

ATA5728 at 868.3 MHz would be: L_m = 8.87nH (≈8.2nH); C_m = 1.38pF (≈1.5pF)

The optimal matching values after tuning are:

ATA5723 at 315MHz is: L_m = 39nH; C_m = 3pF

ATA5724 at 433.92MHz is: L_m = 22nH; C_m = 2.2pF

ATA5728 at 868.3MHz is: L_m = 5.6nH; C_m = 1.8pF

Figure 1-2, Figure 1-3 and Figure 1-4 show the input impedances of the receivers during the matching progress.

Note: Smith chart:
- The red curve shows the input impedance without matching elements.
- The green curve illustrates the theoretical receiver input impedance with the determined start values for the tuning.
- The blue curve shows the measured input impedance after tuning progress.

Rectangular diagram:
- The blue curve illustrates the theoretical receiver input impedance with the determined start values for the tuning.
- The red curve shows the measured input impedance after tuning progress.

Figure 1-2. Input Impedance of ATA5723 before and after Matching

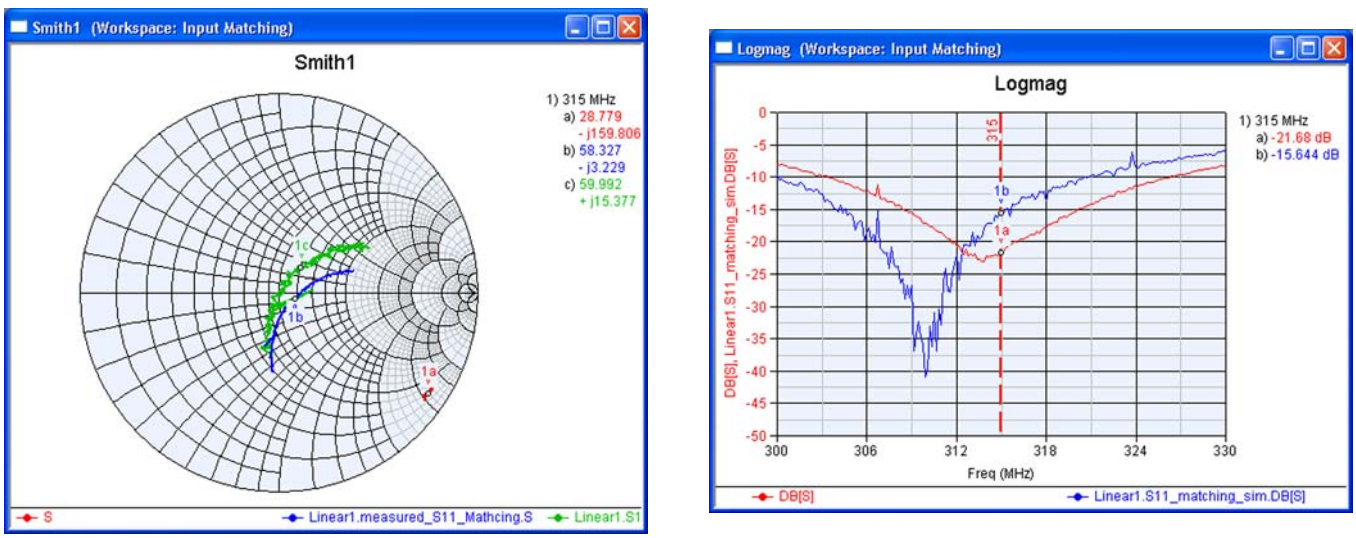


Figure 1-3. Input Impedance of ATA5724 before and after Matching

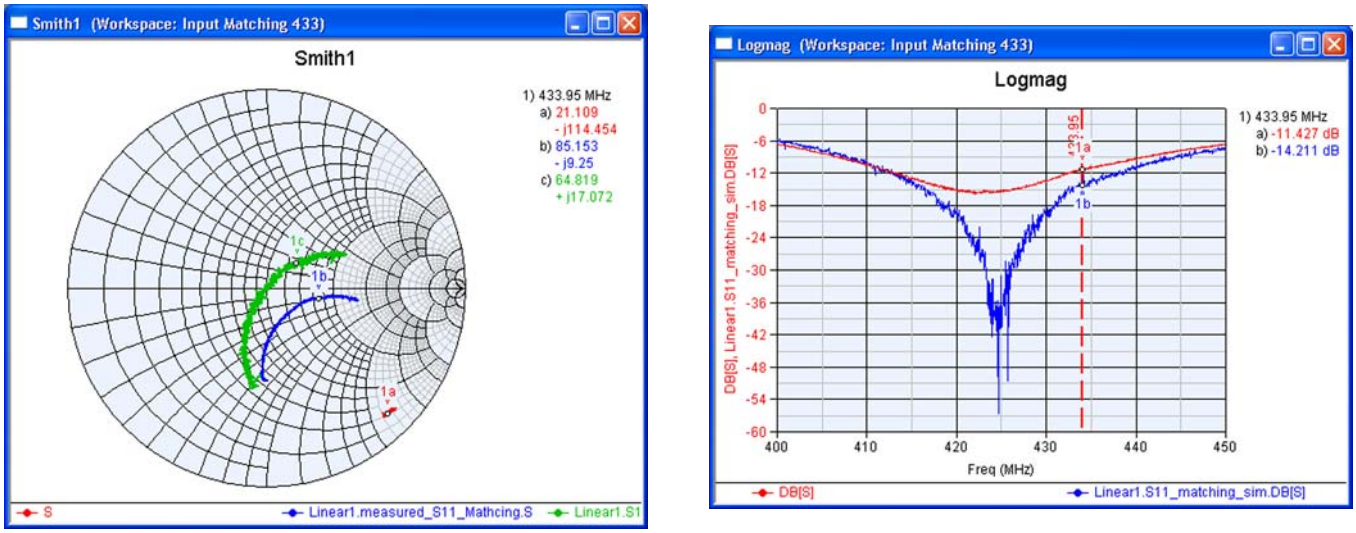
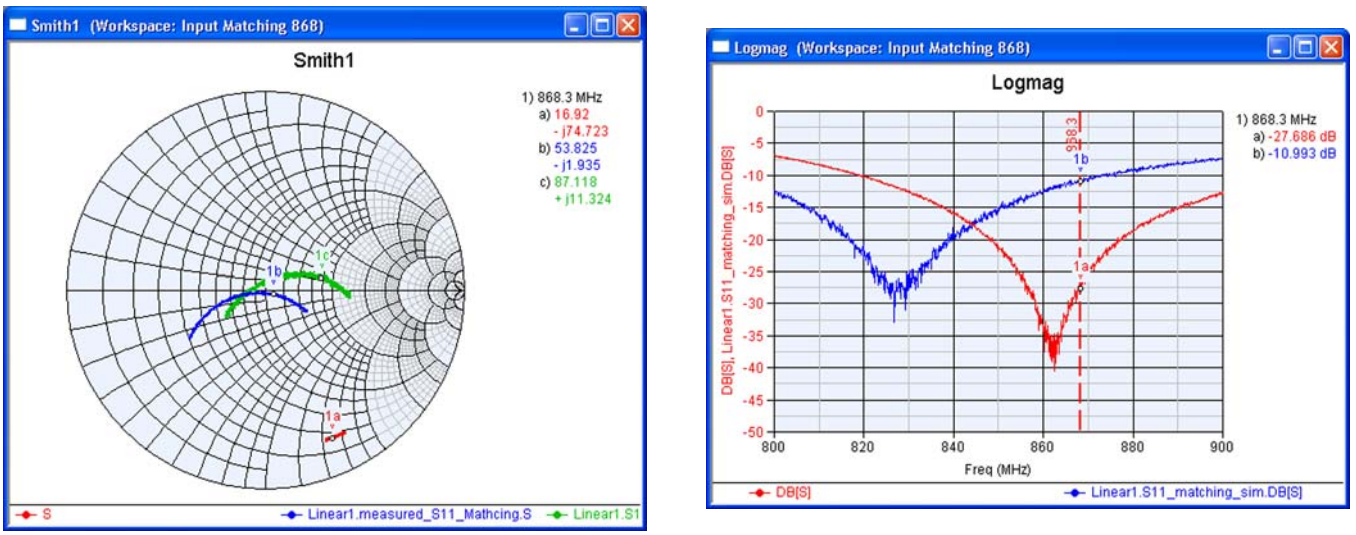


Figure 1-4. Input Impedance of ATA5728 before and after Matching



2. Development Board

Atmel's receiver development boards can be ordered with the SAP number ATA5723-DK, ATA5724-DK and ATA5728-DK. The development boards contain an interface to the mother boards ATAB-RFMB or ATAB-STK-F. The connection with the mother boards allows the receivers to be configured with a personal computer via the serial data interface. Figure 2-1 shows the schematic of the development boards. Figure 2-2 to Figure 2-4 show the layout of the development board. The bill of material is listed in the Table 2-1 on page 10.

Figure 2-1. Schematic of Atmel's Development Board

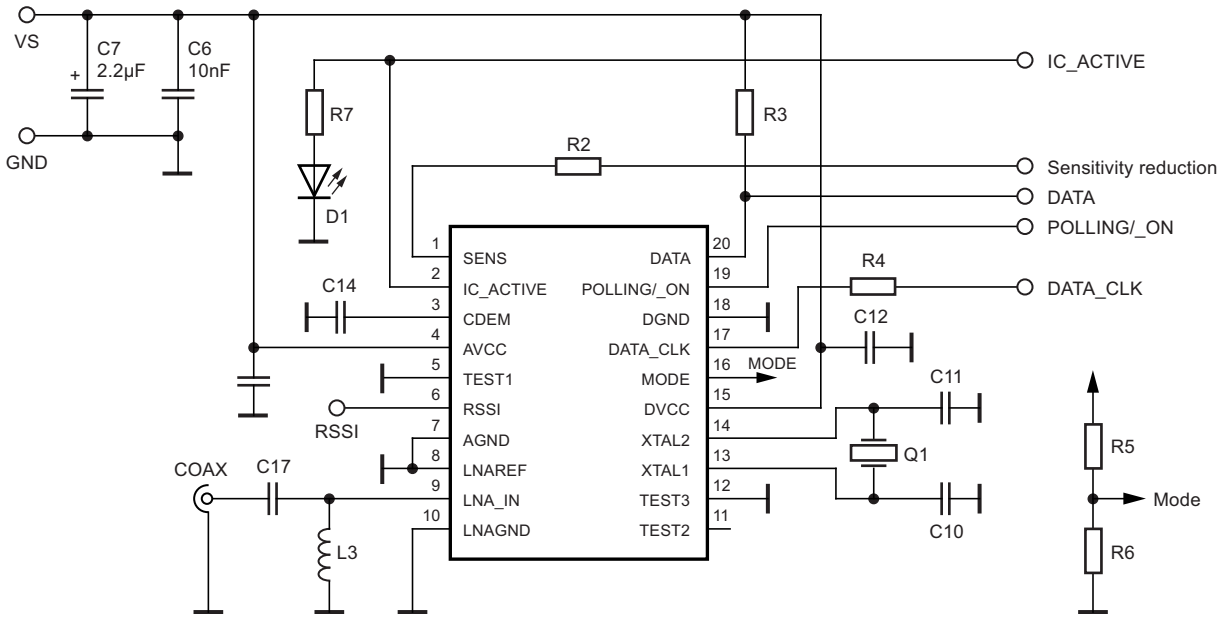


Figure 2-2. Layout of Atmel's Development Board (Top Layer)

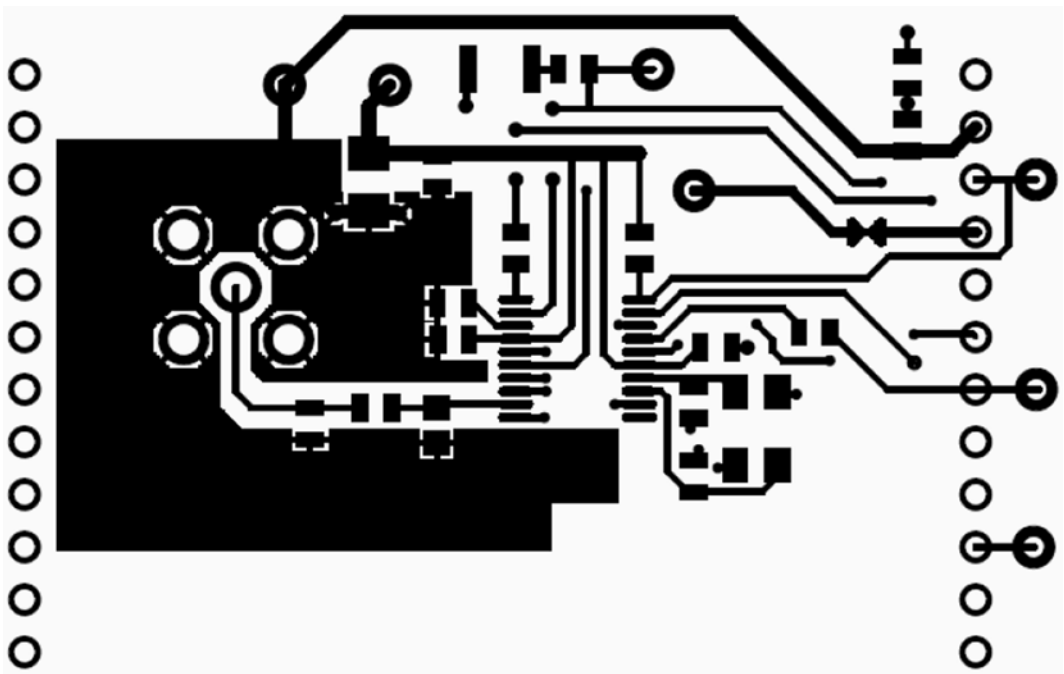


Figure 2-3. Layout of Atmel's Development Board (Bottom Layer)

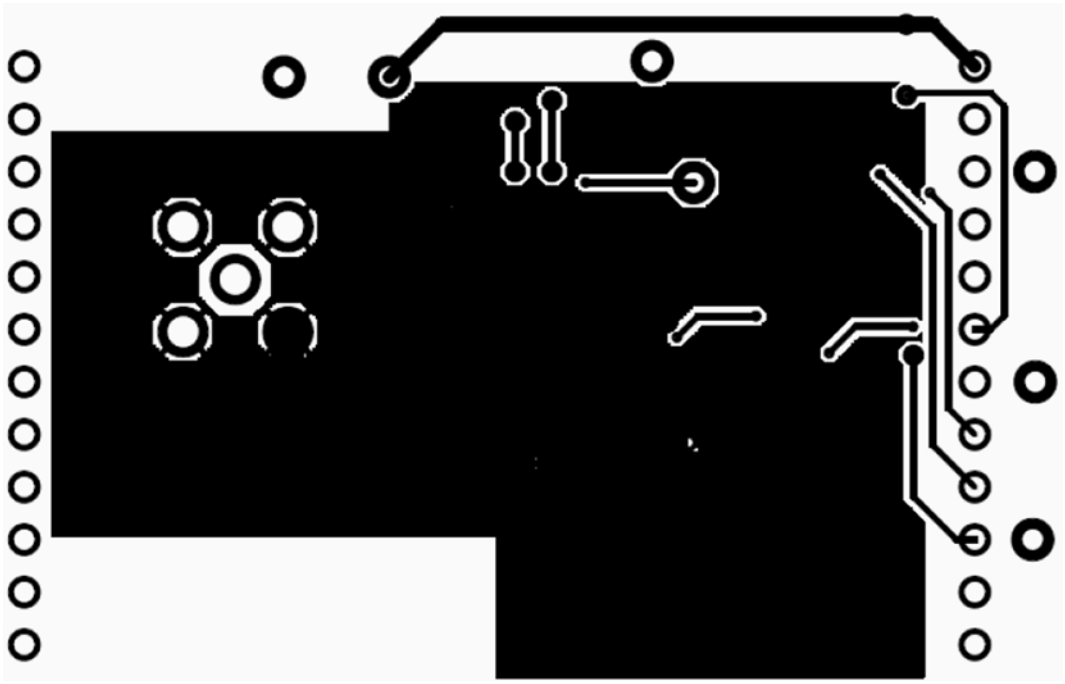
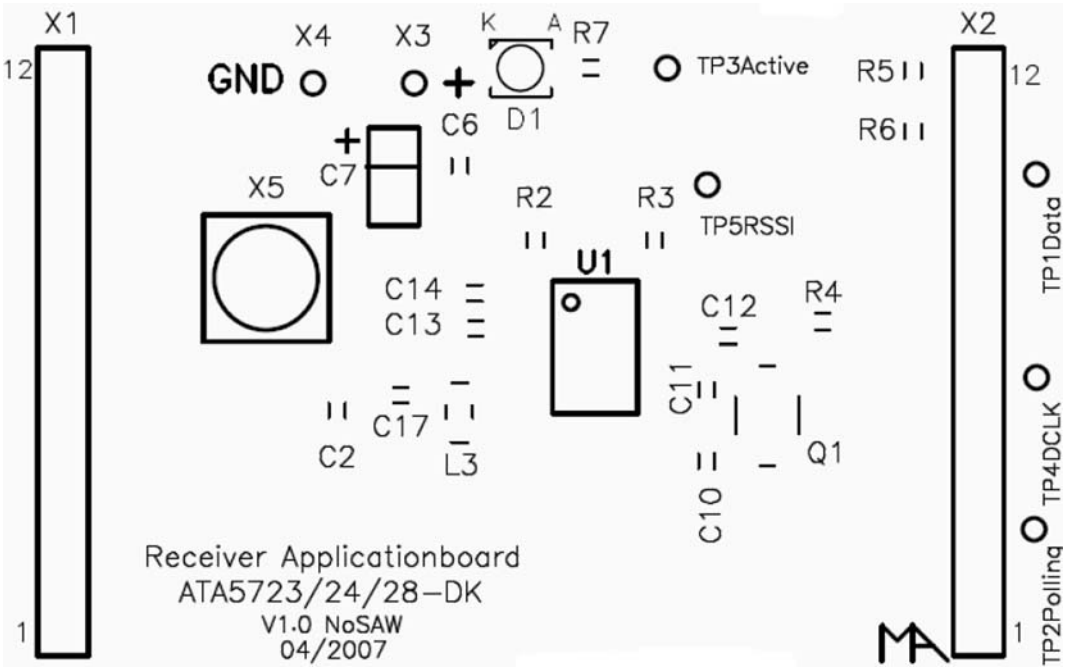


Figure 2-4. Layout of Atmel's Development Board (Designator Layer)



Layout hints for a general application using the receivers:

1. The blocking capacitors (for AVCC and DVCC) must be placed as near as possible to the IC.
2. If the signal from the DATA_CLK will be used and connected to a microprocessor, the trace for this connection must be designed as short as possible and as far as possible from the crystal area. Figure 2-5 shows an ineffectual design for the DATA CLK trace.
3. If the trace between DATA_CLK and the microprocessor is relative long, a resistor can be inserted in series into the trace. This is particularly useful if EMC and coupling effects are a design issue.

Figure 2-5. An Example of a Bad Wiring of the DATA_CLCK Trace

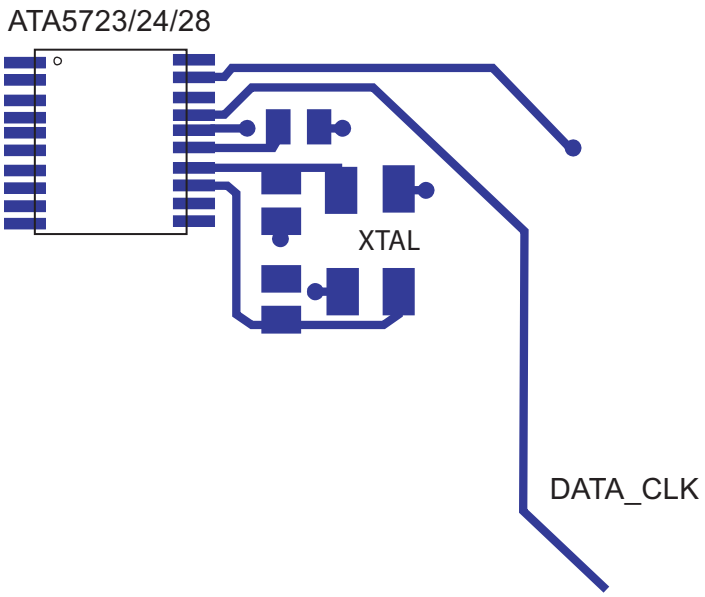


Table 2-1. Bill of Material of the Development Boards

Component List ATA5723/24/28-DK V1.0									
Components	pcs	315MHz	433MHz	868MHz	Value	Tolerance	Material/Series	Housing	Manufacture/ Distributor
U1	1	x			ATA5723			SS020	Atmel®
			x		ATA5724			SS020	Atmel
				x	ATA5728			SS020	Atmel
R2	1	x	x	x	56k	5%	SMD	0603	
R3	1	x	x	x	8.2k	5%	SMD	0603	
R4	1	x	x	x	0		SMD	0603	
R5	1		x	x	10k	5%	SMD	0603	
R6	1	x			10k	5%	SMD	0603	
R7	1	x	x	x	1.8k	5%	SMD	0603	
C2					n.m.				
C6, C12, C13	3	x	x	x	10nF	10%	X7R	0603	Murata®
C7	1	x	x	x	2.2µ/35V	20%	Tantal	Size 3528 mm/BfB	
C10, C11	2	x	x	x	18pF	5%	COG	0603	Murata
C14	1	x	x	x	39n	10%	X7R	0603	Murata
C17	1	x			3pF	5%	COG	0603	Murata
			x		2.2pF	5%	COG	0603	Murata
				x	1.8pF	5%	COG	0603	Murata
D1	1	x	x	x	x	TLMD3100		P-LCC-2 (sizeB)	Vishay®
L3	1	x			39nH	5%	FSL	LL1608	TOKO®
			x		22nH	5%	FSL	LL1608	TOKO
				x	5.6nH	5%	FSL	LL1608	TOKO
Q1	1	x			14.71875MHz			Metal lid 5mm × 3.2mm	KDS
			x		13.528MHz				
				x	13.55234MHz				
X1, X2	2	x	x	x	Row connector		800-10-012-10-001	12 pins/ 0.1” pitch	CAB
X5		x	x	x	SMB connector		R114 426 000		Radiall®
TP1Data, TP2Polling, TP3Active, TP4DCLK, TP5RSSI	5	x	x	x	Pin connector - white		240-333	Single pin	Farnell
X3	1	x	x	x	Pin connector - red		240-345		
X4	1	x	x	x	Pin connector - black		240-333		
PCB	1				ATA5723/24/28-DK V1.0 NoSAW		FR4/1.5 mm		Wagner

3. Evaluation of Receivers using ATA5723/24/28-DK and RF Design Kit Software

One of the benefits of using the receiver ATA5723/24/28 is the reuse of the ATA5743/60 software.

For evaluation with the Atmel's RF Design Kit software up to V1.05, the designer can use the existing settings of ATA5743 (ATA5760), as follow:

- Choose receiver setting "T5743 (315MHz)" for configuration of ATA5723
- Choose receiver setting "T5743 (433MHz)" for configuration of ATA5724
- Choose receiver setting "T5760 (868MHz)" for configuration of ATA5728

With the RF Design Kit software V1.06 the optimum settings for the receiver are implemented. The suitable receiver settings are described by receiver type as well as the operating frequency under the Receiver pull down menu, as follow:

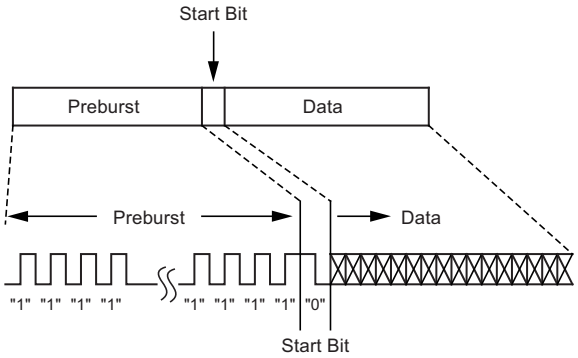
- The setting "ATA5723 (315MHz)"
- The setting "ATA5724 (433MHz)"
- The setting "ATA5728 (868MHz)"

For a more detailed description of the RF Design Kit software and ATAB-RFMB (ATAB-STK-F), please refer to the application notes "ATAK57xx and ATAK862xx hardware description" and "ATAK57xx, ATAK57xx-F, ATAK862xx and ATAK862xx-F software description". The documents also explain how to evaluate the RF system Link between Atmel's receivers and suitable transmitter products.

4. Consideration of the Transmission Protocol

Manchester coding is required for the optimal operation of the receivers. Therefore the explanation in this section assumes that the telegram of the system is Manchester encoded. For a general application, the recommended protocol will consist of preburst, start bit, and data. The preburst is the first part of the telegram with an identical number of bits, “111111…” as well as “00000…”. The start bit is defined by changing the bit from “1” to “0” (or from “0” to “1”). Figure 4-1 illustrates this protocol.

Figure 4-1. The Recommended Protocol (Manchester Coding)



Preburst length is very important item in the definition of the protocol timing. This value depends on the defined sleep time, start-up time of the receiver, the number of the bit check and last but not least the start-up time of the microcontroller.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bit\text{-}check} + T_{Startup\_uC} \qquad \text{Equation 20}$$

The following is an example for the definition of the preburst length. It is assumed that the system has the following requirements.

- Receiving frequency: 433.92MHz
- Data rate: 1kBps (Manchester)
- Sleep time: 12.71ms
- Number of the bit check: 3
- Start-up time of the microcontroller: 1ms

The maximum time for the bit check ($N_{Bit\text{-}Check}$ = 3) will be estimated as $3.5/f_{sig}$. In case of 1kBps the $T_{Bit\text{-}Ckeck}$ = 3.5ms.

The startup time for BR_Range0 is 1.827ms ($T_{Startup}$).

$T_{Preburst} \geq 12.71ms + 1.827ms + 3.5ms + 1ms = 19.037ms$

$T_{Preburst} \geq 19.037ms$, which a means minimum 20 bits (Manchester) are only necessary for the preburst. For security the number of preburst bits can be defined as 25 bits.

5. Bit Check Limits

The basic of the bit check processing is the internally measurement of the timing between EDGE to EDGE (please see Figure 5-1) on the demodulator output. T_{Lim_min} and T_{Lim_max} create the time window for bit check processing. Both values can be set in the Limit Register of the receiver.

Figure 5-1. Valid Time Window for Bit Check

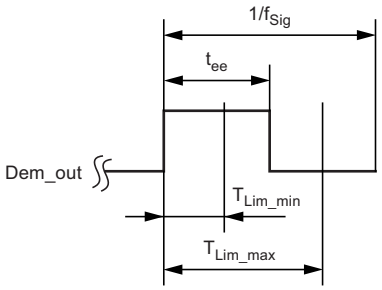
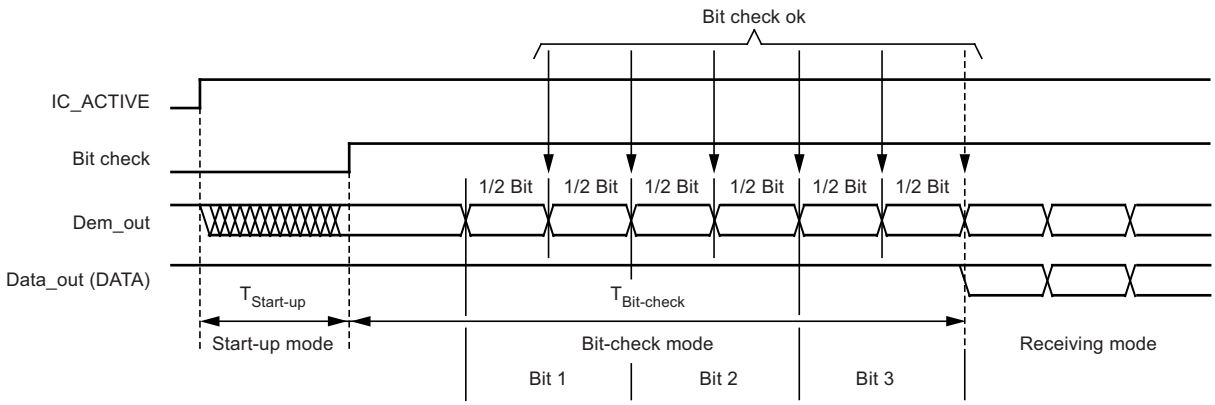


Figure 5-2 shows an example of a successful bit check with the NBit_Check = 3. The number of bit check means here the number of Manchester encoded bit. If the bit check is successful the receiver leaves the bit check mode and the data will be transferred to the pin DATA (receiving mode).

Figure 5-2. Successful Bit Check Processing with Bit Check = 3



Note: ½ Bit here means ½ Manchester encoded Bit

Figure 5-3. Failed Bit Check Processing

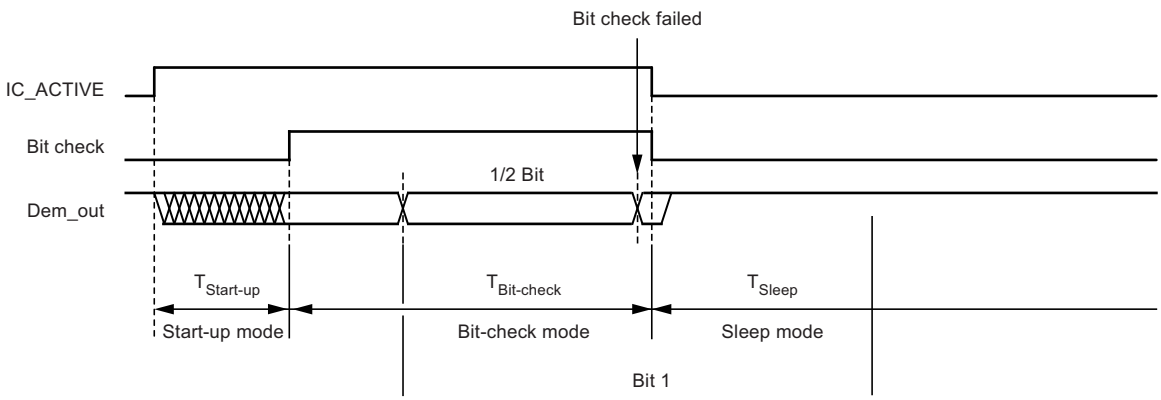


Figure 5-3 shows a failed bit check. As soon as the bit check failed, the receiver breaks the bit check processing and goes into the sleep mode.

The limits of the bit check must be defined very carefully because these values determine both the wake-up behavior and the sensitivity of the receiver. The limit values must be set such that the receiver will not be woken up by noise and the sensitivity will not be reduced. The calculation of the limit must consider the jitter effect of the signal, which occurs in case of a weak input signal. The best compromise between the sensitivity and the susceptibility to noise will be achieved with a bit check's valid time window between ±25% to ±30%.

The equations 21 and 22 show the correlation between the bit check's time limit and the setting values in the LIMIT register.

$T_{lim\_min} = Lim\_min \times T_{xclk}$ Equation 21

$T_{lim\_max} = (Lim\_max\text{-}1) \times T_{xclk}$ Equation 22

Note: Lim_Min and Lim_max are the values set in the LIMIT register.
T_{XCLK} is the extended basic clock cycle for the different data ranges
- T_{XCLK} for BR_Range0 is $8xT_{CLK}$
- T_{XCLK} for BR_Range1 is $4xT_{CLK}$
- T_{XCLK} for BR_Range2 is $2xT_{CLK}$
- T_{XCLK} for BR_Range3 is $1xT_{CLK}$
- T_{CLK} is the basic clock cycle and derived from the crystal frequency. For ATA5723, this value will be defined as $30/f_{XTO}$, whereas for ATA5724/28 the value is $28/f_{XTO}$.

In addition to the bit check limits, there are 2 other important limit values in respect to the time violation of the Manchester coding, the Lim_min2T and Lim_max2T. The values will be internally calculated based on the values of Lim_min and Lim_max.

$Lim\_min2T = (Lim\_min + Lim\_max) - (Lim\_max\text{-}Lim\_min) \times 0.5$ Equation 23

$Lim\_max2T = (Lim\_min + Lim\_max) + (Lim\_max\text{-}Lim\_min) \times 0.5$ Equation 24

For the example calculation in this section T_{lim_min} and T_{lim_max} are defined with ±25% of the $0.5 \times T_{sig}$. The values T_{lim_min2T} and T_{lim_max2T} must be calculated with ±12.5% of T_{sig}.

$T_{lim\_min} = 0.75/(2 \times f_{sig}) \rightarrow \quad Lim\_min = 0.75/(2 \times f_{sig} \times T_{XCLK})$

$T_{lim\_max} = 1.25/(2 \times f_{sig}) \rightarrow \quad Lim\_max = [1.25/(2 \times f_{sig} \times T_{XCLK})] + 1$

$Lim\_min2T = [3.5/(4 \times f_{sig} \times T_{XCLK})] + 0.5$

$Lim\_max2T = [4.5/(4 \times f_{sig} \times T_{XCLK})] + 1.5$

5.1 Calculating the Limit Values Due to the Tolerance on the Transmitted Data Rate

For the calculation, the data rate including tolerance must be converted into periods. Assume the tolerance of the data rate is x% and the data rate's frequency is f_x (the period of the data rate (T_x) is $1/f_x$).

The frequency range for the data rate is given by:

$$f_x \times \left(1 - \left[\frac{x}{100}\right]\right) \leq f_x \leq f_x \times \left(1 + \left[\frac{x}{100}\right]\right) \quad \text{Equation 25}$$

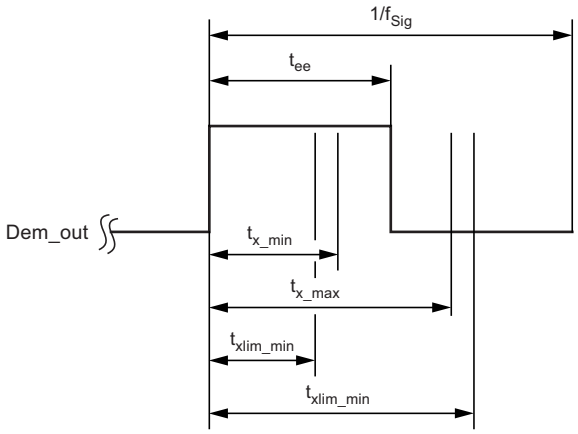
The period range of the data rate will be:

$$\frac{1}{f_x \times \left(1 - \left[\frac{x}{100}\right]\right)} \geq \frac{1}{f_x} \geq \frac{1}{f_x \times \left(1 + \left[\frac{x}{100}\right]\right)} \quad \text{Equation 26}$$

$$T_x \times \left(\frac{1}{1 - \left[\frac{x}{100}\right]}\right) \geq T_x \geq T_x \times \left(\frac{1}{1 + \left[\frac{x}{100}\right]}\right) \quad \text{Equation 27}$$

Figure 5-4 shows the setting of the time limit required for a successful bit check.

Figure 5-4. The Required Time Limit Ranges for a Successful Bit Check



Note: Notes to Figure 5-4:
- t_{x_min} and t_{x_max} are the possible jitter of the data rate to be received.
- t_{xlim_min} and t_{xlim_max} are the limit values that must be set for an optimal bit check, when the tolerance of the data rate is taken into account.

$$f_x = \frac{T_x}{2} \rightarrow t_{x\_min} = \frac{T_x}{2} \times \left(\frac{1}{1 + \left[\frac{x}{100} \right]} \right) \quad \text{Equation 28}$$

$$t_{x\_max} = \frac{T_x}{2} \times \left(\frac{1}{1 - \left[\frac{x}{100} \right]} \right) \quad \text{Equation 29}$$

The recommended 25% of the limit values:

$$t_{xlim\_min} = 0.75 \times \frac{T_x}{2} \times \left(\frac{1}{1 + \left[\frac{x}{100} \right]} \right) \quad \text{Equation 30}$$

$$t_{xlim\_max} = 1{,}25 \times \frac{T_x}{2} \times \left(\frac{1}{1 - \left[\frac{x}{100} \right]} \right) \quad \text{Equation 31}$$

The values of the limit_2T will be calculated internally as follows (±12.5%):

$$t_{xlim\_min\ 2T} = 0.875 \times T_x \times \left(\frac{1}{1 + \left[\frac{x}{100} \right]} \right) \quad \text{Equation 32}$$

$$t_{xlim\_max\ 2T} = 1.125 \times T_x \times \left(\frac{1}{1 - \left[\frac{x}{100} \right]} \right) \quad \text{Equation 33}$$

5.2 Example

Data rate = 2.2kBit/s (f_{sig}) with a tolerance of ±5%

T_{xclk} = 8.278µs ≈ 8.3µs (for receiving frequency at 433.92MHz)

$$2200 \times \left(1 - \left[\frac{5}{100}\right]\right) \leq f_x \leq 2200 \times \left(1 + \left[\frac{5}{100}\right]\right) \Rightarrow 2090\text{Hz} \leq f_x \leq 2310\text{Hz}$$

$$T_x \times \left(\frac{1}{1 - \left[\frac{x}{100}\right]}\right) \geq T_x \geq T_x \times \left(\frac{1}{1 + \left[\frac{x}{100}\right]}\right) \Rightarrow 478.47\mu\text{s} \geq T_x \geq 432.9\mu\text{s}$$

The tolerance of the data rate's period is –4.8% and +5.3%.

$$t_{xlim\_min} = 0.75 \times \frac{T_x}{2} \times \left(\frac{1}{1 + \left[\frac{x}{100}\right]}\right) = 0.75 \times \frac{432.9}{2} = 162.34\mu\text{s}$$

$$t_{xlim\_max} = 1.25 \times \frac{T_x}{2} \times \left(\frac{1}{1 - \left[\frac{x}{100}\right]}\right) = 1.25 \times \frac{478.47}{2} = 299.04\mu\text{s}$$

$$t_{xlim\_min\ 2T} = 0.875 \times T_x \times \left(\frac{1}{1 + \left[\frac{x}{100}\right]}\right) = 0.875 \times 432.9 = 378.79\mu\text{s}$$

$$t_{xlim\_max\ 2T} = 1.125 \times T_x \times \left(\frac{1}{1 - \left[\frac{x}{100}\right]}\right) = 1.125 \times 478.47 = 538.28\mu\text{s}$$

The possible setting Lim_min = 17 and Lim_max = 39 in the Limit register means:

T_{Lim_min} = 17 × 8.3µs = 141.1µs

T_{Lim_max} = (39 – 1) × 8.3µs = 315.4µs

The values are optimal for the bit check because:

$T_{lim\_min} < t_{xlim\_min}$ and $T_{lim\_max} > t_{xlim\_max}$

The limit setting is also optimal for the perfect Manchester coding:

Lim_min2T = 45 T_{lim_min2T} = 373.5µs < t_{xlim_min2T}

Lim_max2T = 67 T_{lim_max2T} = 556.1µs > t_{xlim_max2T}

6. DATA filter

The data filter circuitry of the analog signal processing is mostly integrated except for the external capacitor CDEM, which determines the lower cut-off frequency of the data filter (f_{cu_DF}) together with the internal resistor of 30kΩ. The capacitor's value must set according to the desired data ranges. The upper cut-off frequency (f_{u_DF}) is defined automatically by the setting of the BR_Range. Equation 34 shows the calculation of the lower cut-off frequency.

$$f_{CU\_DF} = \frac{1}{2\pi \times 30\ k\Omega \times CDEM} \qquad \text{Equation 34}$$

Table 6-1. The Recommended CDEM Value of the Related Data Filter's Cut-off Frequency

	CDEM	Lower cut-off Frequency	Upper cut-off Frequency
BR_Range0	39nF	0.136kHz	3.4kHz
BR_Range1	22nF	0.241kHz	6kHz
BR_Range2	12nF	0.442kHz	10kHz
BR_Range3	8.2nF	0.647kHz	19kHz

7. IC_ACTIVE for LNA

The pin IC_ACTIVE is designed to signal the status of the receiver, i.e., if the receiver is in sleep mode or active (receiving) mode. Therefore, this pin can be also used to control the biasing of an external preamplifier to boost the sensitivity of the receiver. The pin is specified for a current consumption of 1 mA. Therefore, is the pin is suitable only for biasing of the preamplifier and can not drive the preamplifier's supply current. The saturation voltage of the pin is specified as a typical value of 4.85V and minimum value of 4.6V.

8. The External Circuitry of Pin DATA

8.1 Determining the Pull-up Resistor Depends on the Load Capacitance

The load capacitance on the pin must be taken into account as this can influence the signal quality passed through this pin. Depending on the load capacitance on the pin and the data rate, the pull-up resistor on that pin must be properly determined. Table 8-1 shows the resistor ranges for different data rate ranges for two load capacitance values.

Table 8-1. The Recommended Pull-up Resistor (Datasheet Page 32, Table 14-1)

-	BR_range	Applicable R_{pup}
$C_L \le 1nF$	B0	1.6kΩ to 47kΩ
	B1	1.6kΩ to 22kΩ
	B2	1.6kΩ to 12kΩ
	B3	1.6kΩ to 5.6kΩ
$C_L \le 100pF$	B0	1.6kΩ to 470kΩ
	B1	1.6kΩ to 220kΩ
	B2	1.6kΩ to 120kΩ
	B3	1.6kΩ to 56kΩ

8.2 Some Hints for Connecting the Pin Data Directly to another Control Module

The following conditions can be found in some automotive applications,

- The receiver module doesn't have its own microprocessor. The programming of the receiver as well as the received data processing will be performed by another control module.
- The only connection between the receiver module and the control module is the data interface on pin 20, which is connected directly to the power supply over a pull-up resistor.

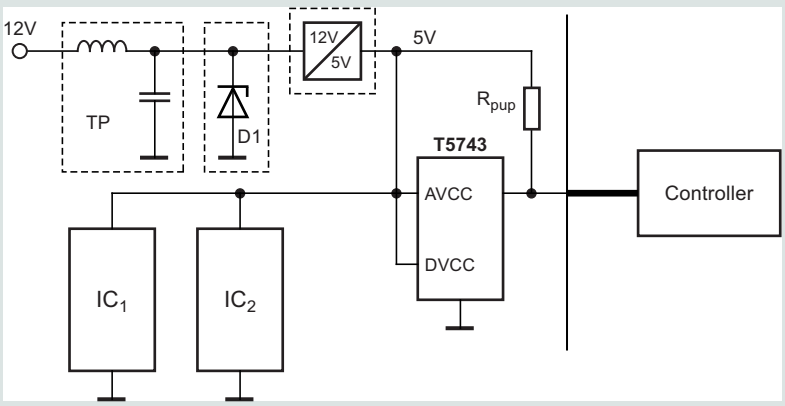
For this type of application, the receiver circuitry must be protected against both load dump and jump start.

8.2.1 Principle Circuit for Protection against Load Dump and Jump Start

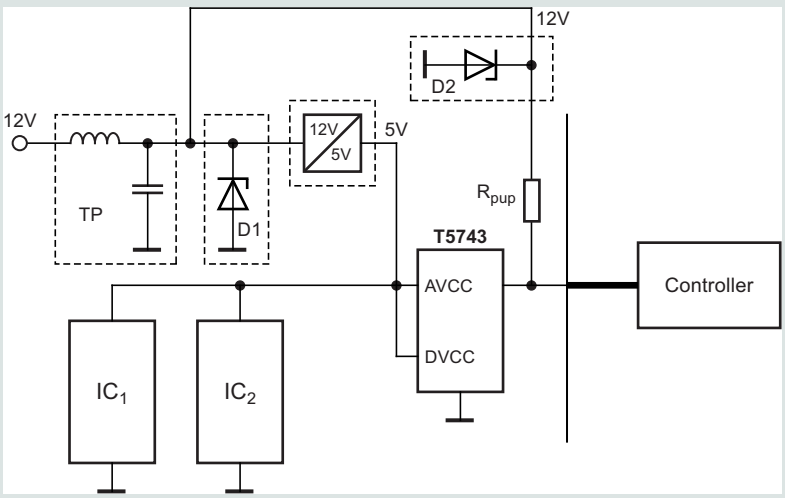
Figure 8-1 type 1 and type 2 give two possibilities for a protecting circuit. In the first circuit type 1, the protection will be performed by the LC low-pass filter, the protection diode (D1) as well as the voltage regulator. Depending on the needs, the inductor can be replaced by a resistor. A TVS (Transient Voltage Suppressor) diode is optimal for D1. In some cases a Zener diode can be used also.

Figure 8-1. Principle Circuit of a Protection against Load Dump and Jump Start

Type 1



Type 2

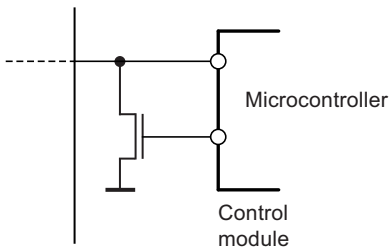


In the circuit type 2 the pull up resistor is connected directly to the 12V power supply instead of 5V regulated power supply. A protecting diode D2 must be placed between the power supply line and the pull-up resistor protecting the data out.

8.2.2 Shifting of the Ground Potential

A “relatively” long connection between the receiver (pin data) and the control module can cause a fail of programming because of a different ground potential between the control module and the receiver module. This “shift” of the ground potential could distort the signal low level decision. If the receiver can not detect the low level set by the microprocessor, the circuit can not be programmed successfully. Generally the pin data can recognize a signal voltage $0.35 \times V_S = 0.35 \times 5V$ d 1.7V as “LOW”. This must be secured also in case of production variations. One possible solution would be to use a switch transistor in the control module, as illustrated in Figure 8-2.

Figure 8-2. Principle Application Circuit with a Switch Transistor Controlling the Serial Data Interface of the Receiver



9. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9118C-AUTO-05/15	• Put document in the latest template
9118B-AUTO-09/08	• Section 2 “Calculating the Required Crystal Frequency” on page 2 updated • Section 5 “Evaluation of Receivers using ATA5723/24/28-DK and RF Design Kit Software” on page 12 updated

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