ZL40292

20-Output DB2000Q Buffer with Ultra-Low Additive Jitter

Features

- Fully Compliant with Intel DB2000Q Specification
- 20 Low-Power Push-Pull HCSL PCIe Outputs
- Ultra-Low Additive Jitter: 20 fs Maximum in DB2000Q Band, 10 fs Maximum for PCIe Gen 5.0, 6.5 fs Maximum for PCIe Gen 6.0
- Supports Clock Frequencies from 0 MHz to 250 MHz
- Supports 3.3V Power Supplies
- Embedded Low Droput (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output-to-Output Skew of 50 ps
- SMBus Interface
- Eight OE Pins
- Embedded Series Terminations Adjusted for 85Ω Differential Transmission Line
- Transparent for Spread-Spectrum Clock

Applications

- PCIe Gen1/2/3/4/5/6 Clock Distribution
- Intel QPI
- Servers
- Storage and Data Centers
- Switches and Routers

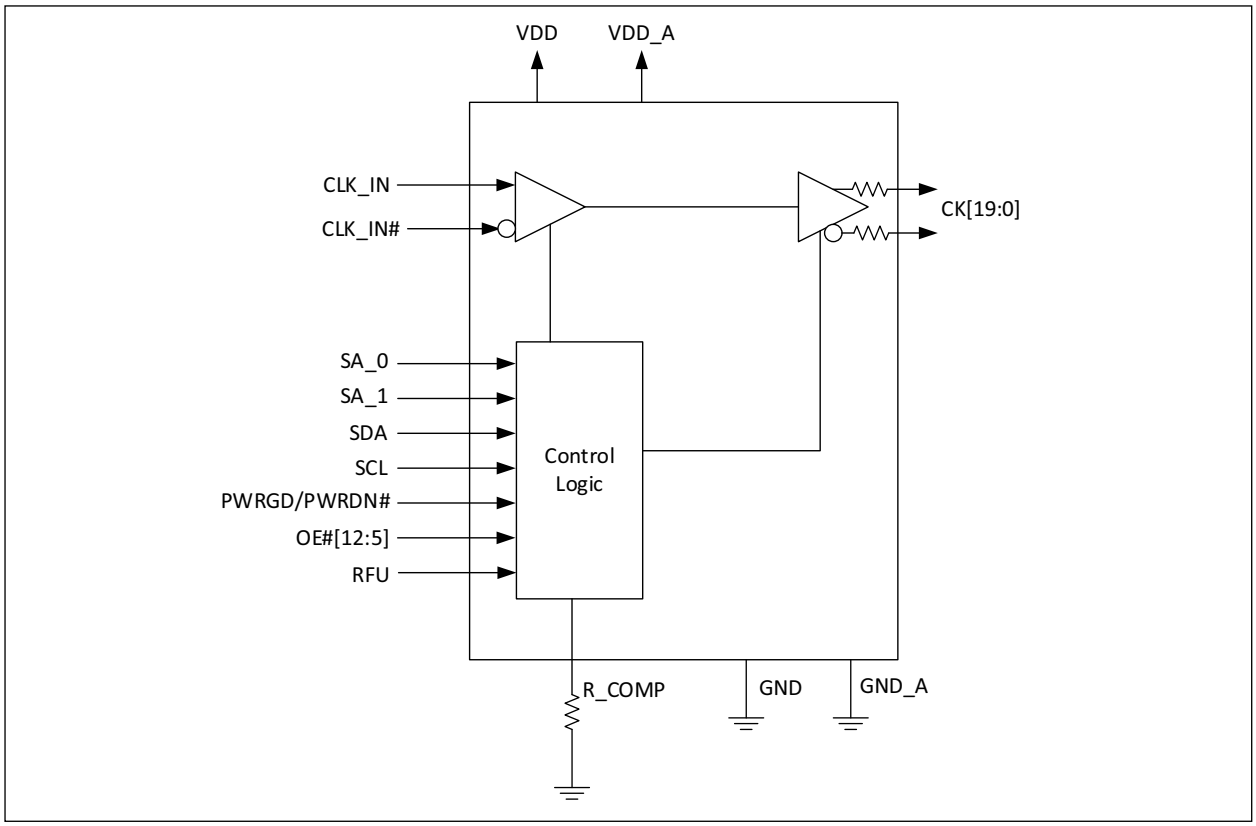

FIGURE 0-1: *Functional Block Diagram.*

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1.0 PIN DESCRIPTION AND CONFIGURATION

The ZL40292 is packaged in a 10 mm x 10 mm, 72-lead VQFN.

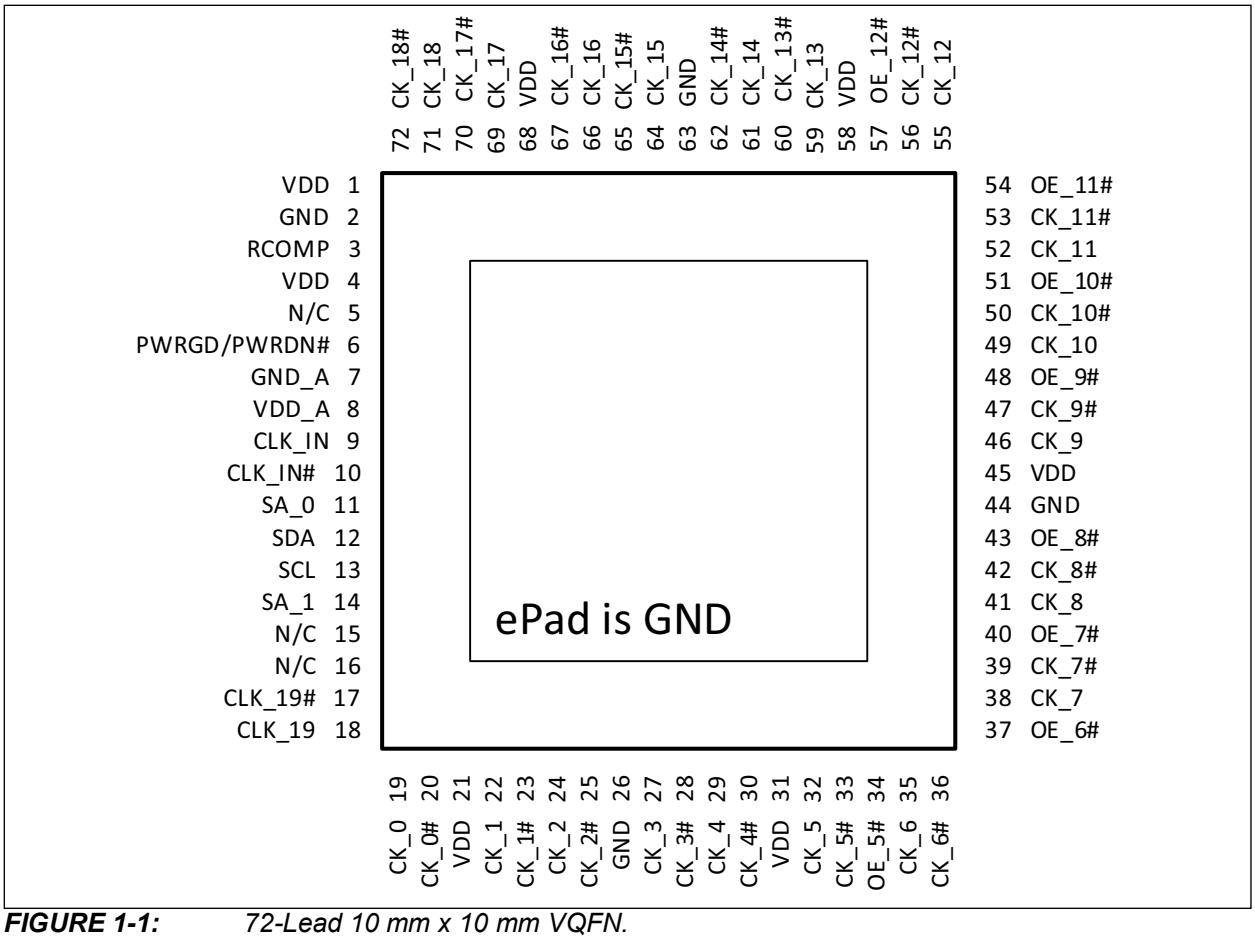


FIGURE 1-1: *72-Lead 10 mm x 10 mm VQFN.*

1.1 Pin Descriptions

The I/O column uses the following symbols: I – input, I_{PU} – input with 120 kΩ internal pull-up resistor, I_{PD} – input with 300 kΩ internal pull-down resistor, O – output, I/O – Input/Output Drain pin, NC – No connect pin, P – power supply pin, I_{TRI} – Tri-level input pin biased to VDD/2 by internal 120 kΩ pull-up and 120 kΩ pull-down resistor.

TABLE 1-1: PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
Input Reference			
9	CLK_IN	I	**Input Differential or Single-Ended Reference** Input frequency range 0 Hz to 250 MHz.
10	CLK_IN#		
Output Clocks			
19	CK_0	O	**Ultra-Low Additive Jitter Differential Outputs 0 to 19** Output frequency range 0 Hz to 250 MHz.
20	CK_0#		
22	CK_1		
23	CK_1#		
24	CK_2		
25	CK_2#		
27	CK_3		
28	CK_3#		
29	CK_4		
30	CK_4#		
32	CK_5		
33	CK_5#		
35	CK_6		
36	CK_6#		
38	CK_7		
39	CK_7#		
41	CK_8		
42	CK_8#		
46	CK_9		
47	CK_9#		
49	CK_10		
50	CK_10#		
52	CK_11		
53	CK_11#		
55	CK_12		
56	CK_12#		
59	CK_13		
60	CK_13#		
61	CK_14		
62	CK_14#		
64	CK_15		
65	CK_15#		
66	CK_16		
67	CK_16#		
69	CK_17		

TABLE 1-1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type	Description
70	CK_17#	O	**Ultra-Low Additive Jitter Differential Outputs 0 to 19** Output frequency range 0 Hz to 250 MHz.
71	CK_18		
72	CK_18#		
17	CK_19		
18	CK_19#		
Hardware Control			
34	OE_5#	I_{PD}	**Output Enable** Logic level on these pins enables/disables the corresponding output.
37	OE_6#		
40	OE_7#		
43	OE_8#		
48	OE_9#		
51	OE_10#		**OE_n#** / **CK_n/n#**
54	OE_11#		0 / Active
57	OE_12#		1 / Low/Low both pulled low by 42.5Ω resistor
6	PWRGD/ PWRDN#	I	**Power-up/Power-down.**
3	R_COMP	I	**Not used.**
SMBus Control			
13	SCL	I	**SMBus client clock input.**
12	SDA	I/O	**Input/Open-drain SMBus data.**
11	SA_0	I_{TRI}	**Tri-level address selection inputs.**
14	SA_1		
Power and Ground			
1	VDD	P	**Positive Supply Voltage** Connect to 3.3V supply.
4			
21			
31			
45			
58			
68			
8	VDD_A	P	**Positive Analog Supply Voltage** Connect 3.3V power supply.
2	GND	P	**Ground** Connect to ground.
26			
44			
63			
7	GND_A	P	**Analog Ground** Connect to ground
ePad	GND	P	**Ground** Connect to ground
No Connect Pins			
5	NC	—	**No Connect.** These pins are not connected to the die. Leave them open. One of these pins might be used for future modifications of DB2000Q spec. The current DB2000Q v1.0 standard calls for RFU (Reserved for Future Upgrades) pin but does not assign it to any pin number.
15			
16			

2.0 FUNCTIONAL DESCRIPTION

The ZL40292 is an ultra-low additive jitter, low-power, 1 to 20 fanout buffer that is fully compliant with Intel DB2000Q Standard.

The device operates from 3.3V±5% supply, as per Intel spec. Its operation is ensured over the industrial temperature range of –40°C to +85°C.

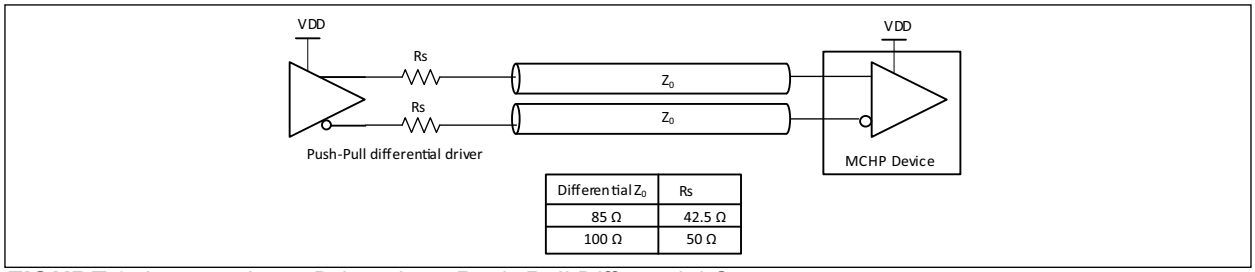
2.1 Clock Inputs

The following block diagrams show how to terminate different signals fed to the ZL40292 inputs.

The device input can be fed with transmission lines of any impedance. Examples below show only 50Ω single-ended, 85Ω differential, and 100Ω differential, which are the most common ones in practice. Figure 2-1 and Figure 2-2 show how to terminate the input when driven from a push-pull and traditional HCSL drivers, respectively.

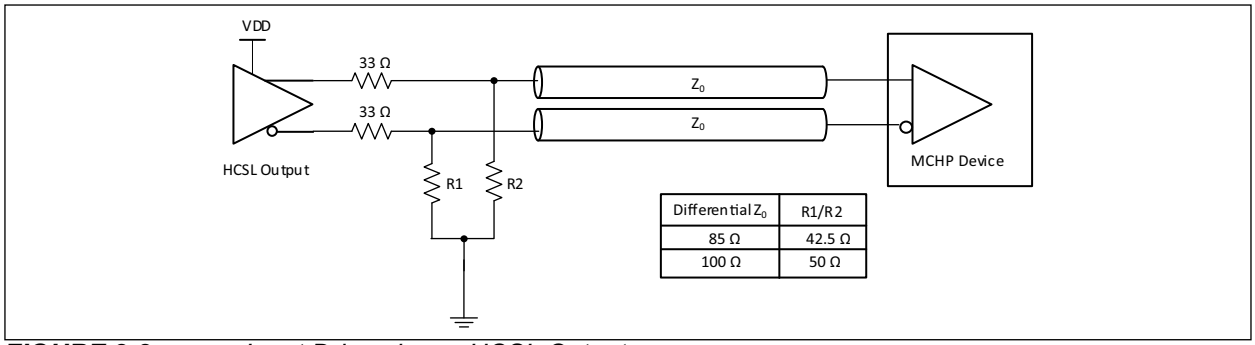
Figure 2-3 shows how to terminate a single-ended output, such as LVCMOS. This example assumes 50Ω transmission line, which is the most common for single-ended CMOS signaling. Resistors R1 and R2 are chosen to provide 50Ω termination and proper biasing and $R_O + R_S$ ideally should be 50Ω so that the transmission line is terminated at both ends with its characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Figure 2-3). The source resistors of R_S = 270Ω could be used for standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.



Differential Z_0	Rs
85 Ω	42.5 Ω
100 Ω	50 Ω

FIGURE 2-1: *Input Driven by a Push-Pull Differential Output.*



Differential Z_0	R1/R2
85 Ω	42.5 Ω
100 Ω	50 Ω

FIGURE 2-2: *Input Driven by an HCSL Output.*

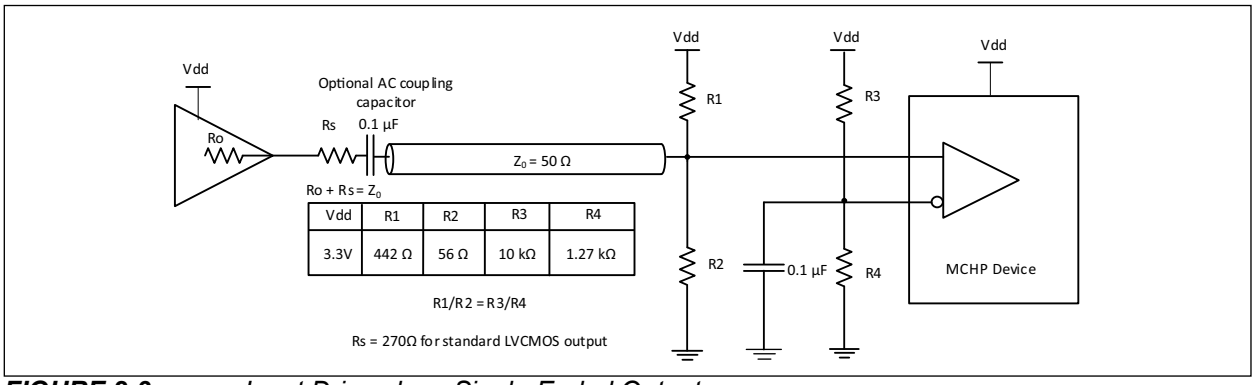


FIGURE 2-3: *Input Driven by a Single-Ended Output.*

2.2 Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 2-4. This provides significant saving relative to traditional current based HCSL outputs which require four resistors per differential pair (80 resistors for 20 outputs).

Embedded series termination resistors are matched for 85Ω differential transmission line.

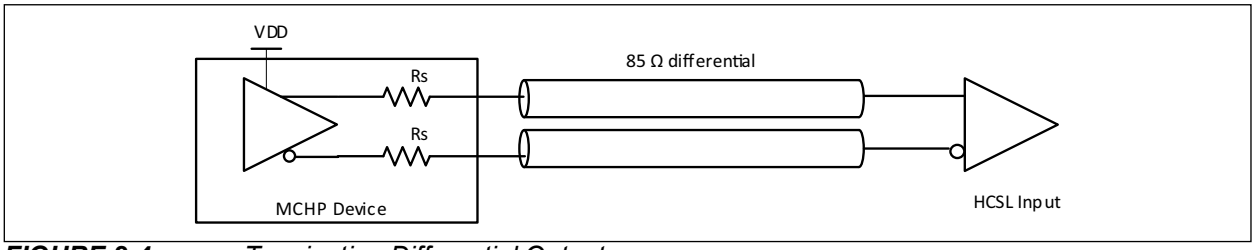


FIGURE 2-4: *Terminating Differential Outputs.*

2.3 Termination of Unused Outputs

Unused outputs should be left unconnected.

2.4 Power Supply Filtering

Each power pin (VDDA and VDD) should be decoupled with a 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board, each power supply could be further insulated with low DC resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Figure 2-5 shows recommended decoupling.

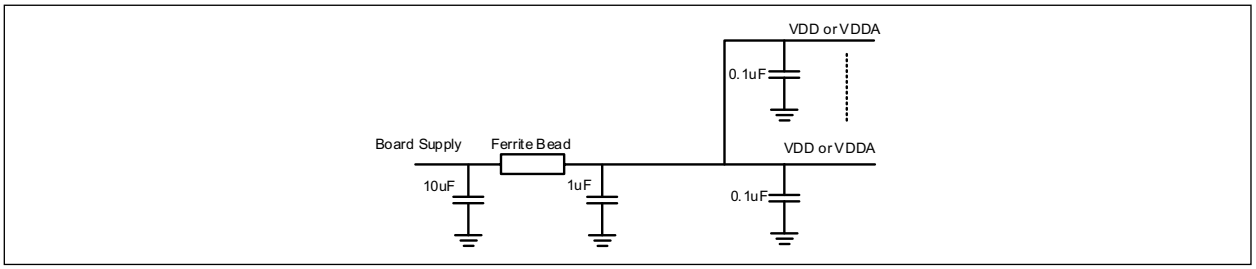


FIGURE 2-5: *Power Supply Filtering.*

2.5 OE# and Output Enables (Control Register)

Each output can be individually enabled or disabled by SMBus control register bits or via OE# pin. The OE# pins are asynchronous asserted-low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

OE# pins are mapped to CK[12:5] outputs.

Note that the logic level for assertion or de-assertion is different in software than it is on hardware. This follows hardware default nomenclature for communication channels (e.g., output is enabled if OE# pin is pulled low) and still maintains software programming logic (e.g., output is enabled if OE register is true).

Refer to Table 2-1 for the truth table for enabling and disabling outputs via hardware and software. Note that both the control register bit must be a '1' AND the OE# pin must be a '0' for the output to be active.

TABLE 2-1: OE FUNCTIONALITY

Inputs		OE# Hardware Pins and Control Register Bits			
PWRGD/ PWRDN#	CK_IN/ CK_IN#	SMBUS Enable Bit	OE# Pin	CK/CK# [12:5]	CK/CK# [4:0] and [19:13]
0	X	X	X	0	0
1	Running	0	X	0	0
		1	0	Running	Running
		1	1	0	Running

2.6 OE# Assertion (Transition from '1' to '0')

All differential outputs that were disabled are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 0 to 10 CK clock periods.

2.7 OE# De-Assertion (Transition from '0' to '1')

The impact of de-asserting OE# is each corresponding output will transition from normal operation to disabled in a glitch free manner. A minimum of four valid clocks will be provided after the de-assertion of OE#. The maximum latency from the de-assertion to disabled outputs is 10 CK clock periods.

2.8 PWRGD/PWRDN#

PWRGD is asserted high and de-asserted low. De-assertion of PWRGD (pulling the signal low) is equivalent to indicating a power-down condition. PWRGD (assertion) is used by the ZL40292 to sample initial configurations such as SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin which is used to disable (drive low/low) all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDN# is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

The assertion and de-assertion of PWRDN# is asynchronous.

Disabling of the CK_IN input clock prior to assertion of PWRDN# is an undefined mode and not recommended. Operation in this mode may result in glitches.

TABLE 2-2: PWRGD/PWRDN# FUNCTIONALITY

PWRGD/PWRDN#	CK	CK#
0	Low	Low
1	Normal	Normal

2.9 PWRDN# Assertion

When PWRDN# is sampled low by two consecutive rising edges of CK#, all differential outputs will be disabled on the next CK# high-to-low transition.

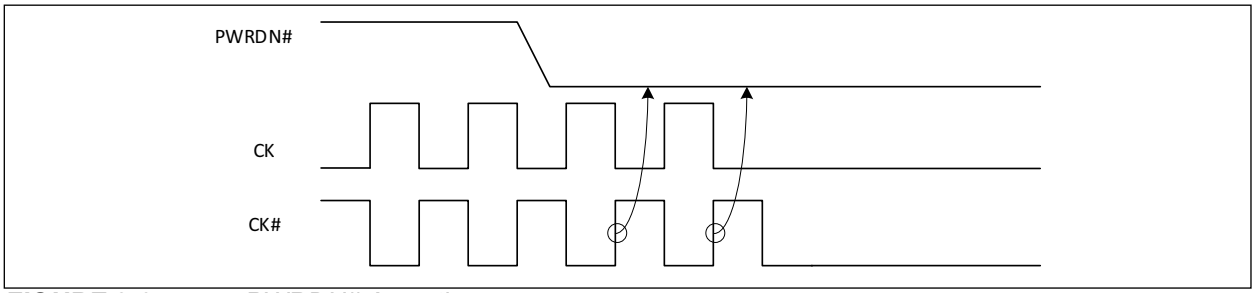


FIGURE 2-6: *PWRDN# Assertion.*

2.10 PWRGD Assertion

PWRGD to the clock buffer should not be asserted before V_{DD} reaches $V_{DD(MIN)}$. Prior to $V_{DD(MIN)}$, it is recommended to hold PWRGD low (less than 0.5V).

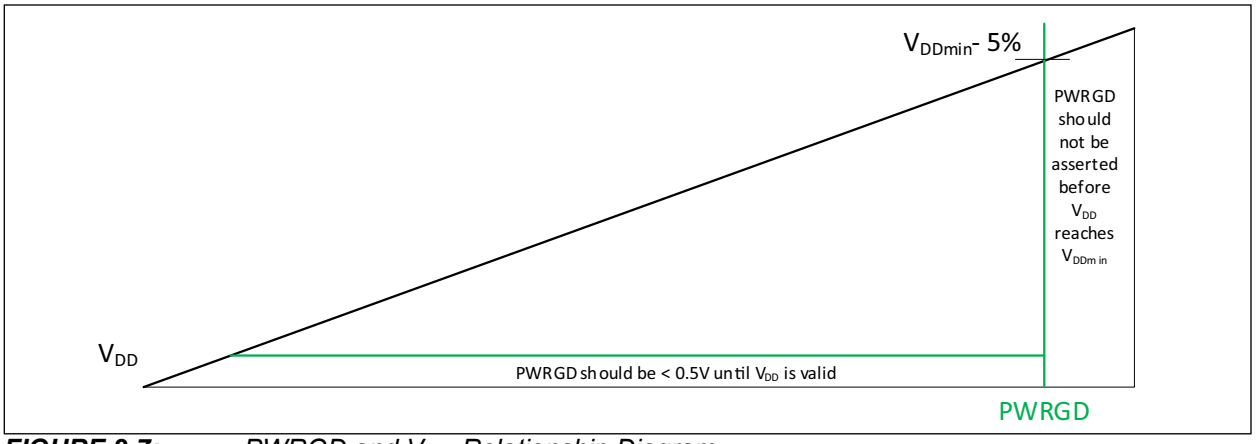


FIGURE 2-7: *PWRGD and V_{DD} Relationship Diagram.*

The power-up latency t_{STABLE} is to be less than 1.8 ms. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal to the time that stable clocks are output from the buffer chip. All differential outputs stopped in a disabled condition resulting from power down must be driven high in less than 300 µs of PWRGD assertion to a voltage greater than 200 mV.

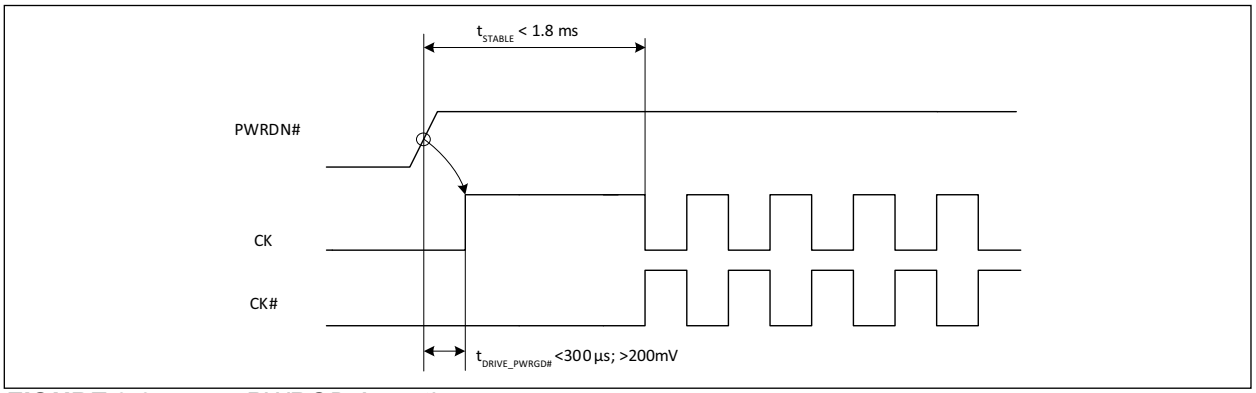


FIGURE 2-8: *PWRGD Assertion.*

2.11 Programming via SMBus

The address selection is done via SA_0 and SA_1 tri-level hardware pins, which select the appropriate address for the device. The two tri-level input pins that can configure the ZL40292 to nine different addresses (refer to Table 4-2 for `VIL_Tri`, `VIM_Tri`, `VIH_Tri` signal level).

TABLE 2-3: SMBUS ADDRESSES

SA_1	SA_0	SMBus Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

2.12 SMBus Byte Read/Write

Reading or writing a register in a SMBus slave device in byte mode always involves specifying the register number.

Read. The standard byte read is as shown in Figure 2-9. It is an extension of the byte write. The write start condition is repeated, then the client device starts sending data, and the host acknowledges it until the last byte is sent. The host terminates the transfer with a NAK, then a stop condition. For byte operation, the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

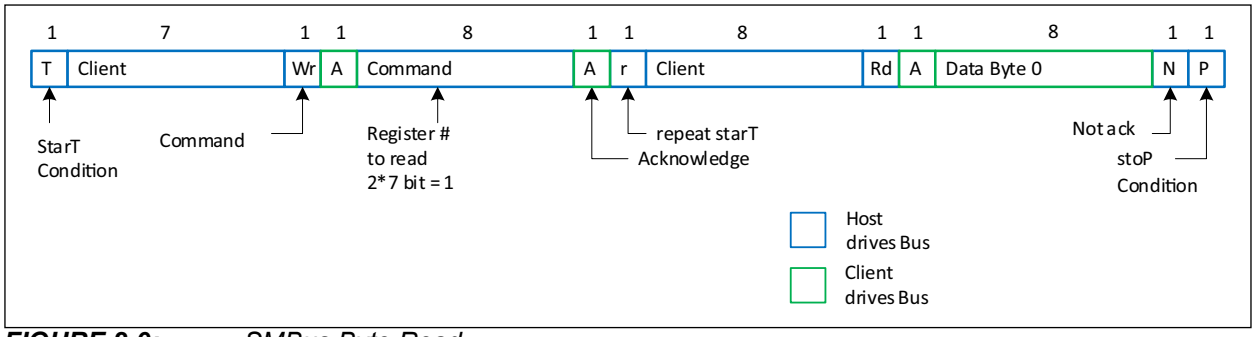


FIGURE 2-9: *SMBus Byte Read.*

Write. Figure 2-10 illustrates a simple typical byte write. For byte operation, the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count. The count can be between 1 and 32. It cannot be zero nor exceed 32.

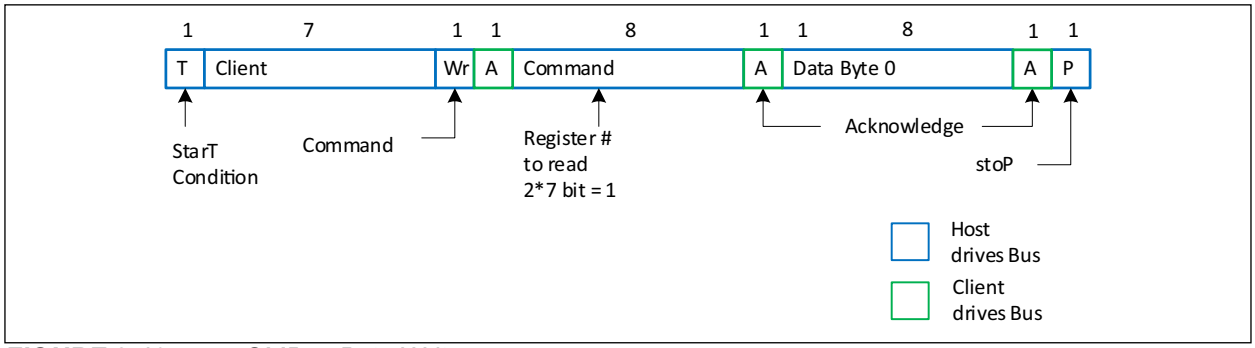


FIGURE 2-10: *SMBus Byte Write.*

2.13 SMBus Block Read/Write

Read. After the client address is sent with the R/W condition bit set, the command byte is sent with the MSB = 0. The client Ack's the register index in the command byte. The host sends a repeat start function. After the client Ack's this, the client sends the number of bytes it wants to transfer (>0 and <33). The host Ack's each byte, except the last, and sends a stop function.

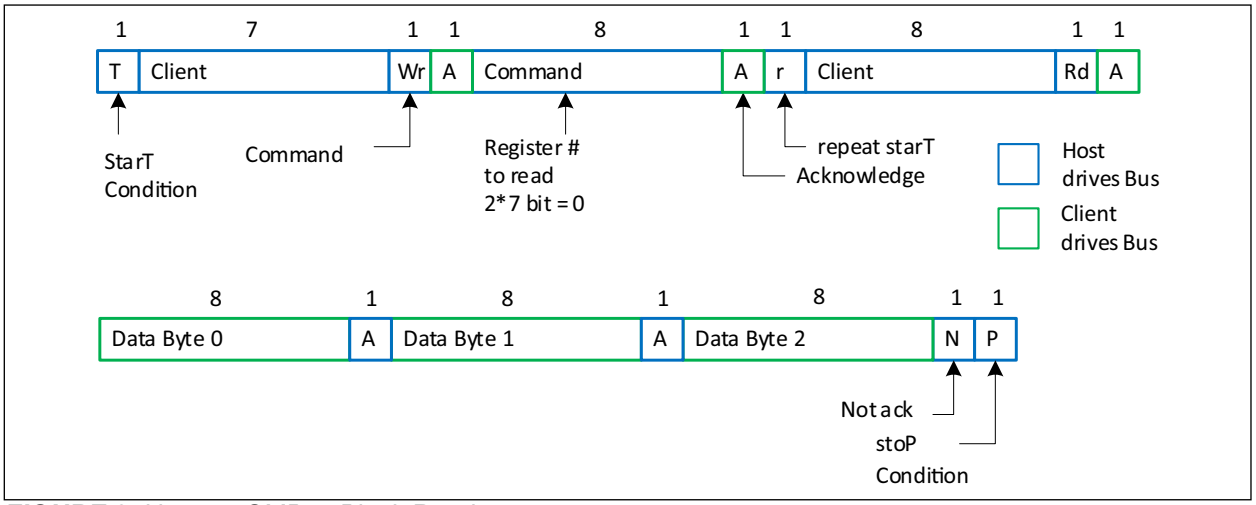


FIGURE 2-11: *SMBus Block Read.*

Write. After the client address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate at which register to start the transfer. If the command byte is 00h, the client device will be compatible with existing block mode client devices. The next byte of a write must be the count of bytes that the host will transfer to the client device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the client device. The client device always acknowledges each byte received. The transfer is terminated after the client sends the Ack and the host sends a stop function.

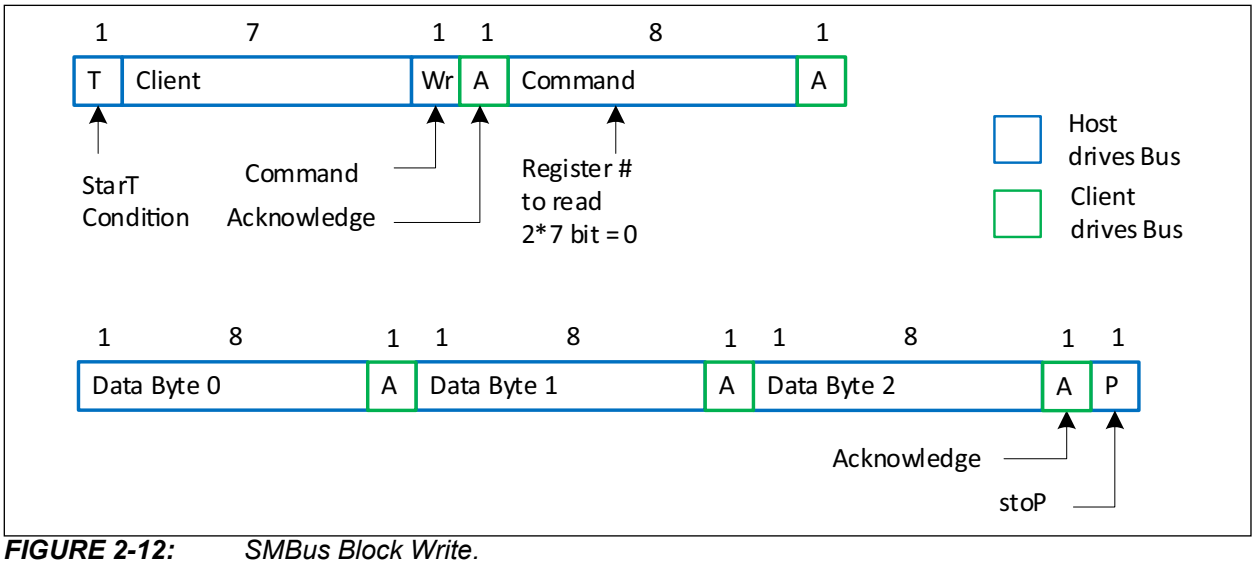


FIGURE 2-12: *SMBus Block Write.*

3.0 REGISTER MAP

TABLE 3-1: BYTE 0: OUTPUT ENABLE

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved	—	—	—	0	—
1	Reserved	—	—	—	0	—
2	Reserved	—	—	—	0	—
3	Output Enable CK 16	Low	Enabled	R/W	1	CK[16]
4	Output Enable CK 17	Low	Enabled	R/W	1	CK[17]
5	Output Enable CK 18	Low	Enabled	R/W	1	CK[18]
6	Output Enable CK 19	Low	Enabled	R/W	1	CK[19]
7	Reserved	—	—	—	0	—

TABLE 3-2: BYTE 1: OUTPUT ENABLE CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK 0	Low	Enabled	R/W	1	CK[0]
1	Output Enable CK 1	Low	Enabled	R/W	1	CK[1]
2	Output Enable CK 2	Low	Enabled	R/W	1	CK[2]
3	Output Enable CK 3	Low	Enabled	R/W	1	CK[3]
4	Output Enable CK 4	Low	Enabled	R/W	1	CK[4]
5	Output Enable CK 5	Low	Enabled	R/W	1	CK[5]
6	Output Enable CK 6	Low	Enabled	R/W	1	CK[6]
7	Output Enable CK 7	Low	Enabled	R/W	1	CK[7]

TABLE 3-3: BYTE 2: OUTPUT ENABLE CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK 8	Low	Enabled	R/W	1	CK[8]
1	Output Enable CK 9	Low	Enabled	R/W	1	CK[9]
2	Output Enable CK 10	Low	Enabled	R/W	1	CK[10]
3	Output Enable CK 11	Low	Enabled	R/W	1	CK[11]
4	Output Enable CK 12	Low	Enabled	R/W	1	CK[12]
5	Output Enable CK 13	Low	Enabled	R/W	1	CK[13]
6	Output Enable CK 14	Low	Enabled	R/W	1	CK[14]
7	Output Enable CK 15	Low	Enabled	R/W	1	CK[15]

TABLE 3-4: BYTE 3: OE# PIN REALTIME READBACK CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Realtime Readback of OE_5#	OE_5# Low	OE_5# High	R	Realtime	CK[5]
1	Realtime Readback of OE_6#	OE_6# Low	OE_6# High	R	Realtime	CK[6]
2	Realtime Readback of OE_7#	OE_7# Low	OE_7# High	R	Realtime	CK[7]
3	Realtime Readback of OE_8#	OE_8# Low	OE_8# High	R	Realtime	CK[8]
4	Realtime Readback of OE_9#	OE_9# Low	OE_9# High	R	Realtime	CK[9]

TABLE 3-4: BYTE 3: OE# PIN REALTIME READBACK CONTROL REGISTER (CONTINUED)

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
5	Realtime Readback of OE_10#	OE_10# Low	OE_10# High	R	Realtime	CK[10]
6	Realtime Readback of OE_11#	OE_11# Low	OE_11# High	R	Realtime	CK[11]
7	Realtime Readback of OE_12#	OE_12# Low	OE_12# High	R	Realtime	CK[12]

TABLE 3-5: BYTE 4: RESERVED CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved	—	—	—	0	—
1	Reserved	—	—	—	0	—
2	Reserved	—	—	—	0	—
3	Reserved	—	—	—	0	—
4	Reserved	—	—	—	0	—
5	Reserved	—	—	—	0	—
6	Reserved	—	—	—	0	—
7	Reserved	—	—	—	0	—

TABLE 3-6: BYTE 5: VENDOR/REVISION IDENTIFICATION CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Vendor ID Bit 0	—	—	R	1	—
1	Vendor ID Bit 1	—	—	R	1	—
2	Vendor ID Bit 2	—	—	R	0	—
3	Vendor ID Bit 3	—	—	R	0	—
4	Revision Code Bit 0	—	—	R	0	—
5	Revision Code Bit 1	—	—	R	1	—
6	Revision Code Bit 2	—	—	R	0	—
7	Revision Code Bit 3	—	—	R	0	—

TABLE 3-7: BYTE 6: DEVICE ID CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Device ID 0	—	—	R	0	—
1	Device ID 1	—	—	R	0	—
2	Device ID 2	—	—	R	1	—
3	Device ID 3	—	—	R	1	—
4	Device ID 4	—	—	R	1	—
5	Device ID 5	—	—	R	0	—
6	Device ID 6	—	—	R	1	—
7	Device ID 7 (MSB)	—	—	R	0	—

TABLE 3-8: BYTE 7: BYTE COUNT REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	BC0 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
1	BC1 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
2	BC2 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
3	BC3 - Writing to this register configures how many bytes will be read back	—	—	RW	1	—
4	BC4 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
5	BC5 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
6	Reserved	—	—	—	0	—
7	Reserved	—	—	—	0	—

NOTES:

4.0 AC AND DC ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2, Note 3)				
Parameter	**Symbol**	**Min.**	**Max.**	**Notes**
3.3V Core Supply Voltage	V_{DDA}	—	4.6V	Note 6
3.3V I/O Supply Voltage	V_{DD}	—	4.6V	Note 6
3.3V Input High Voltage	V_{IH}	—	4.6V	Note 4, Note 6
3.3V Input Low Voltage	V_{IL}	–0.5V	—	Note 6
Storage Temperature Range	T_S	–65°C	+150°C	Note 6
Input ESD Protection	V_{DD_IN}	2000V	—	Note 5

Note 1: Exceeding these values may cause permanent damage.

2: Functional operation under these conditions is not implied.

3: Voltages are with respect to ground (GND) unless otherwise stated.

4: Maximum V_{IH} is not to exceed maximum V_{DD}.

5: Human body model.

6: Consult manufacturer regarding extended operation in excess of normal DC operating parameters.

4.2 DC Electrical Specification

TABLE 4-2: DC OPERATING CHARACTERISTICS

(Note 1)					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Notes**
3.3V Core Supply Voltage	V_{DD_A}	3.135V	3.3V	3.465V	—
3.3V I/O Supply Voltage	V_{DD}	3.135V	3.3V	3.465V	—
3.3V Input High Voltage	V_{IH}	2.0V	—	V_{DD} + 0.3V	—
3.3V Input Low Voltage	V_{IL}	V_{DD} – 0.3V	—	0.8V	—
Input Leakage Current	I_{IL}	–5 µA	—	+5 µA	—
Input Low Voltage, 3-Level CMOS Input	V_{IL3}	V_{DD} – 0.3V	—	0.9V	—
Input Midrange Voltage, 3-Level CMOS Input	V_{IM3}	1.3V	—	1.8V	—
Input High Voltage, 3-Level CMOS Input	V_{IH3}	2.4V	—	V_{DD}	—
Input Capacitance	C_{IN}	—	—	4.5 pF	Note 2
Output Capacitance	C_{OUT}	—	—	4.5 pF	Note 2
Ambient Operating Temperature Range	T_A	–40°C	—	+85°C	—

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.

2: For parasitic simulation, use IBIS model.

TABLE 4-3: DIFFERENTIAL DC OUTPUT CHARACTERISTICS

(Note 1)

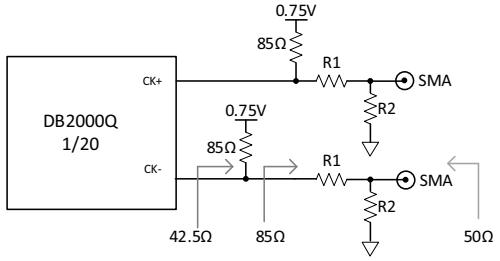
Parameter	Symbol	Min.	Max.	Notes
Maximum Voltage (overshoot)	V_{OVS}	—	V_{HIGH} + 75 mV	Note 1
Maximum Voltage (undershoot)	V_{UDS}	—	V_{LOW} – 75 mV	
Voltage High	V_{HIGH}	225 mV	270 mV	
Voltage Low	V_{LOW}	10 mV	150 mV	
Absolute Crossing Point Voltages	V_{CROSS_ABS}	130 mV	200 mV	
Relative Crossing Point Voltages	V_{CROSS_REL}	—	35 mV	
Output Buffer Differential Impedance	DiffZ	85Ω –5%	85Ω +5%	
Output Buffer Differential Impedance	DiffZCrossing	85Ω –20%	85Ω +20%	

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.

2: Measured into DC test load. See Figure 4-1.

3: Measured at V_{OL}/V_{OH}.

4: Measured during a transition.



Eq1. R1 + (R2||50Ω) = 85Ω

Eq2. ((42.5Ω || 85Ω) + R1)||R2 = 50Ω

R1 = 47.8Ω, standard 1% value R1 = 47Ω
R2 = 145.8Ω, standard 1% value R2 = 147Ω

FIGURE 4-1: *Figure 15.DC Test Load (as per DB2000Q Specification).*

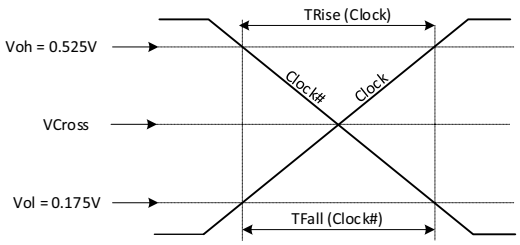


FIGURE 4-2: *Single-Ended Measurement Points for t_{RISE} and t_{FALL}.*

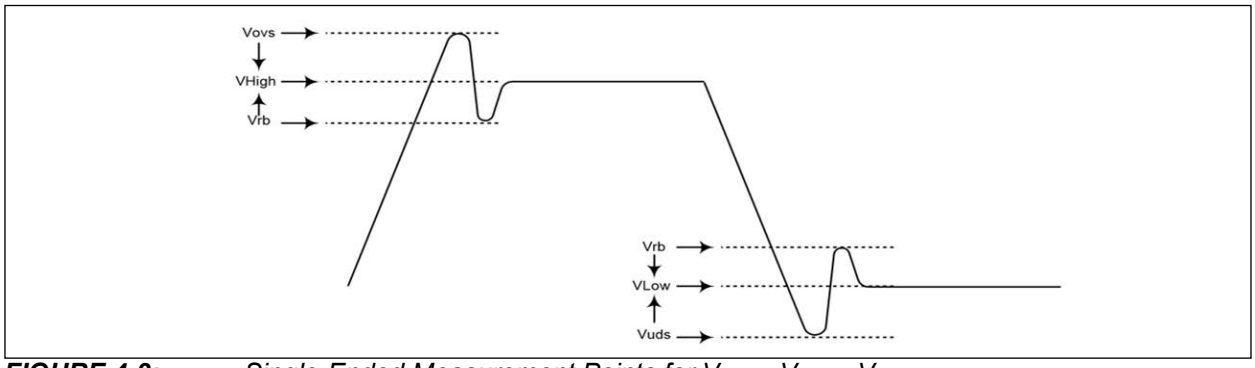


FIGURE 4-3: *Single-Ended Measurement Points for V_{OVS}, V_{UDS}, V_{RB}.*

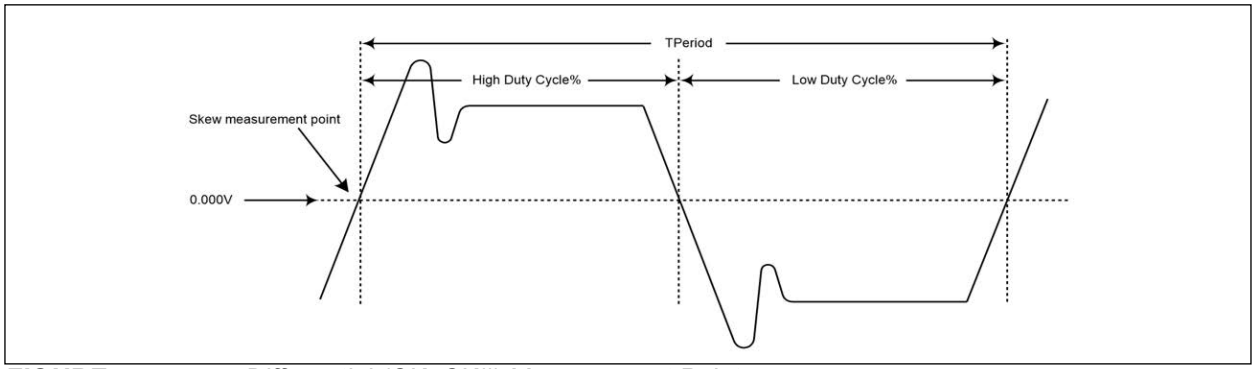


FIGURE 4-4: *Differential (CK, CK#) Measurement Points.*

4.3 AC Electrical Specification

TABLE 4-4: POWER NOISE TOLERANCE

(Note 1)					
VDD Electrical Noise Range	**Symbol**	**Min.**	**Typ.**	**Max.**	**Notes**
f_{NOISE} = 12 kHz to 20 MHz	N_{VDD_MID}	100 mV_{PP}	—	—	Note 2, Note 3, Note 4
f_{NOISE} > 20 MHz	N_{VDD_HIGH}	50 mV_{PP}	—	—	Note 2, Note 3, Note 4
f_{NOISE} = 12 kHz to 20 MHz	$N_{VDD\_A\_MID}$	40 mV_{PP}	—	—	Note 2, Note 3, Note 4
f_{NOISE} > 20 MHz	$N_{VDD\_A\_HIGH}$	20 mV_{PP}	—	—	Note 2, Note 3, Note 4

Note 1: The device meets all specification in the presence of noise specified in this table.

2: Jitter and electrical characteristics are met with specified AC noise present on any of the power pins.

3: Over the specified frequency range, a single sinusoid tone should be assumed swept as the worst case.

4: Maximum measured frequency for VDD was 650 kHz and for VDD_A the maximum frequency was 900 kHz due to limitation of the test setup.

TABLE 4-5: SKEW AND JITTER

Parameter	Symbol	Min.	Typ.	Max.	Notes
Input-to-Output Delay	I/O_{DELAY}	0.9 ns	—	1.5 ns	Note 1, Note 3
Output-to-Output Skew	O/O_{DELAY}	—	—	50 ps	Note 1, Note 2
RMS Additive Jitter as per DB2000Q Spec	AJ_{RMS}	—	15 fs_{RMS}	20 fs_{RMS}	Note 1, Note 2, Note 4
Peak-to-Peak Additive Jitter	$AJ_{RMS(PP)}$	—	—	0.7 ps	Note 1, Note 2
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$t_{jPCIe\_1.0}$	—	0.7 ps_{RMS}	0.8 ps_{RMS}	Note 1, Note 2
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$t_{jPCIe\_2.0\_high}$	—	75 fs_{RMS}	94 fs_{RMS}	Note 1, Note 2
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$t_{jPCIe\_2.0\_low}$	—	20 fs_{RMS}	28 fs_{RMS}	Note 1, Note 2
Additive Jitter as per PCIe 2.0 mid band (5 MHz to 16 MHz)	$t_{jPCIe\_2.0\_mid}$	—	59 fs_{RMS}	74 fs_{RMS}	Note 1, Note 2
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	19 fs_{RMS}	24 fs_{RMS}	Note 1, Note 2
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	19 fs_{RMS}	24 fs_{RMS}	Note 1, Note 2
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	7.5 fs_{RMS}	10 fs_{RMS}	Note 1, Note 2
Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 MHz to 1.0 MHz, CDR for 64 GT/s CC)	$t_{jPCIe\_6.0}$	—	5 fs_{RMS}	6.5 fs_{RMS}	Note 1, Note 2
Additive jitter as per Intel QPI 9.6 Gbps	t_{jQPI}	—	35 fs_{RMS}	45 fs_{RMS}	Note 1, Note 2
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	49 fs_{RMS}	62 fs_{RMS}	Note 1, Note 2 (100 MHz clock)
		—	40 fs_{RMS}	54 fs_{RMS}	Note 1, Note 2 (133 MHz clock)
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	52 fs_{RMS}	65 fs_{RMS}	Note 1, Note 2 (100 MHz clock)
		—	42 fs_{RMS}	56 fs_{RMS}	Note 1, Note 2 (133 MHz clock)
Noise floor	N_F	—	–164 dBc/Hz	–163 dBc/Hz	Note 1, Note 2 (100 MHz clock)
		—	–163 dBc/Hz	–162 dBc/Hz	Note 1, Note 2 (133 MHz clock)

Note 1: Measured into AC test load as per Figure 4-5.

2: Measured from differential crossing point to differential crossing point.

3: Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

4: Integrated after the measurement filter. See Intel DB2000Q specification Jitter Measurement section for the measurement filter details.

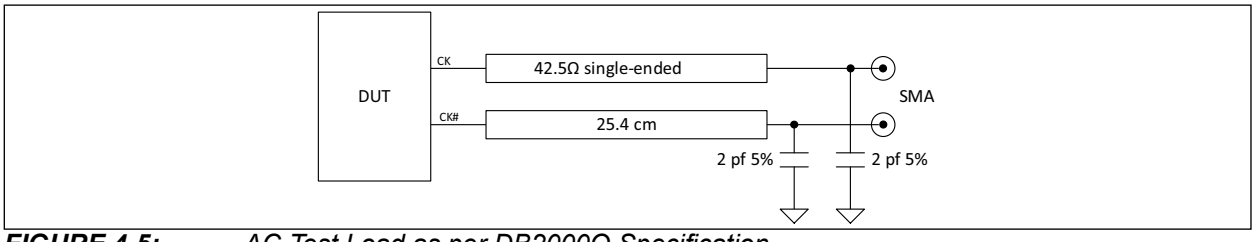


FIGURE 4-5: *AC Test Load as per DB2000Q Specification.*

TABLE 4-6: DIFFERENTIAL OUTPUT CLOCK AC CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Notes
Clock Stabilization Time from PWRGD	t_{STAB}	—	0.1 ms	—
Edge Rate at V_{CROSS}	—	2.75V/ns	5V/ns	Note 1
Slew Rate at V_{CROSS}	—	—	5%V	Note 1

Note 1: Measured into AC test load as per Figure 4-5.

TABLE 4-7: DIFFERENTIAL INPUT CLOCK AC CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Notes
Edge Rate	Input_Slew_Rate	0.7V/ns	—	—
Total Variation of V_{CROSS} over all Edges	Total_Δ_V_{CROSS}	—	140 mV	—
Input Voltage	V_{IN}	200 mV_{DIFF}	—	—

TABLE 4-8: CURRENT CONSUMPTION

Parameter	Condition	Symbol	Min.	Typ.	Max.	Notes
Active Mode Supply Current	f_{IN} = 100 MHz All CK_xP/N outputs enabled	I_{DDPG}	—	196 mA	210 mA	Note 1, Note 2
	f_{IN} = 100 MHz All CK_xP/N outputs disabled		—	46 mA	50 mA	Note 1, Note 3
	f_{IN} = 133 MHz All CK_xP/N outputs enabled		—	203 mA	220 mA	Note 1, Note 2
	f_{IN} = 133 MHz All CK_xP/N outputs disabled		—	46 mA	51 mA	Note 1, Note 3
Power Down Mode Supply Current	f_{IN} = 100 MHz	I_{DDPD}	—	21 mA	25 mA	Note 1, Note 4
	f_{IN} = 133 MHz		—	22 mA	26 mA	Note 1, Note 4

Note 1: V_{DD} = 3.3V +5%.

2: Device operating in active mode (Pin PWRGD/PWRDN_N = 1) with all 20 CK_xP/N outputs enabled (all OE_xN pin = 0, all OCR1, OCR2, OCR3 register OEx bits = 1).

3: Device operating in active mode (Pin PWRGD/PWRDN_N = 1) with all 20 CK_xP/N outputs disabled (all OCR1, OCR2, OCR3 register OEx bits = 0).

4: Device operating in low power mode (Pin PWRGD/PWRDN_N=0).

4.4 SMBus Electrical Characteristics

TABLE 4-9: SMBUS ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Notes
Nominal Bus Voltage	$V_{DD(SMB)}$	2.7V	5.5V	Note 1
Input Low Voltage	V_{IL}	—	0.8V	—
Input High Voltage	V_{IH}	2.1V	$V_{DD(SMB)}$	—
Output Low Voltage	V_{OL}	—	0.4V	At $I_{PULLUP(MAX)}$
Input Leakage Current	I_{LEAK}	—	±10 µA	—
Current Sinking at $V_{OL(MAX)}$	I_{PULLUP}	4 mA	—	—
Pin Capacitive Load	C_I	—	10 pF	—
Signal Noise Immunity from 10 MHz to 100 MHz	V_{NOISE}	300 mV_{PP}	—	—
Noise Spike Suppression Time	t_{SPIKE}	0 ns	50 ns	Note 3
SMBus Operating Frequency	f_{SMB}	10 kHz	100 kHz	100 kHz Mode
		10 kHz	400 kHz	400 kHz Mode
Bus Freetime between Stop and Start Condition	t_{BUF}	4.7 µs	—	100 kHz Mode
		1.3 µs	—	400 kHz Mode
Hold Time after (Repeated) Start Condition After this period, the first clock is generated.	$t_{HD:STA}$	4.0 µs	—	100 kHz Mode
		0.6 µs	—	400 kHz Mode
Repeated Start Condition Setup Time	$t_{SU:STA}$	4.7 µs	—	100 kHz Mode
		0.6 µs	—	400 kHz Mode
Stop Condition Setup Time	$t_{SU:STO}$	4.0 µs	—	100 kHz Mode
		0.6 µs	—	400 kHz Mode
Data Hold Time	$t_{HD:DAT}$	300 ns	—	—
Data Setup Time	$t_{SU:DAT}$	250 ns	—	100 kHz Mode
		100 ns	—	400 kHz Mode
Clock Low Period	t_{LOW}	4.7 µs	—	100 kHz Mode
		1.3 µs	—	400 kHz Mode
Clock High Period	t_{HIGH}	4.0 µs	50 µs	100 kHz Mode
		0.6 µs	50 µs	400 kHz Mode
Clock/Data Fall Time	t_f	—	300 ns	Note 2
Clock/Data Rise Time	t_r	—	1000 ns	100 kHz Mode, Note 2
		—	300 ns	400 kHz Mode, Note 2

Note 1: 3V to 5V ±10%.

2: Rise and fall time is defined as follows:
$t_r = (V_{IL(MAX)} - 0.15)$ to $(V_{IH(MIN)} + 0.15)$
$t_f = (V_{IH(MIN)} + 0.15)$ to $(V_{IL(MAX)} - 0.15)$

3: Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

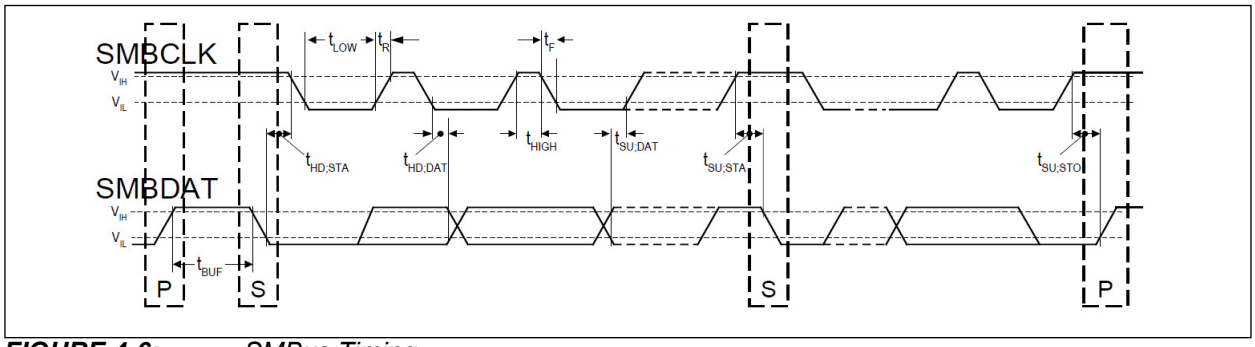


FIGURE 4-6: *SMBus Timing.*

TABLE 4-10: 10 MM X 10 MM VQFN THERMAL PROPERTIES

Parameter	Symbol	Value	Conditions
Maximum Ambient Temperature	$T_{A(MAX)}$	85°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	125°C	—
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	22.6°C/W	Still air
		18.7°C/W	1 m/s airflow
		16.9°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance	θ_{JB}	9.7°C/W	—
Junction to Case Thermal Resistance	θ_{JC}	12.4°C/W	—
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	5.1°C/W	Still air
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	0.4°C/W	Still air

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package).

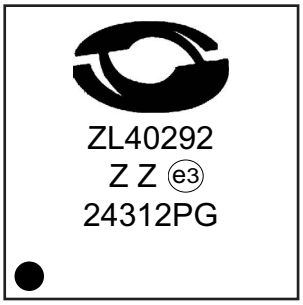
NOTES:

5.0 PACKAGE OUTLINE

5.1 Package Marking Information

72-Lead VQFN*

Example



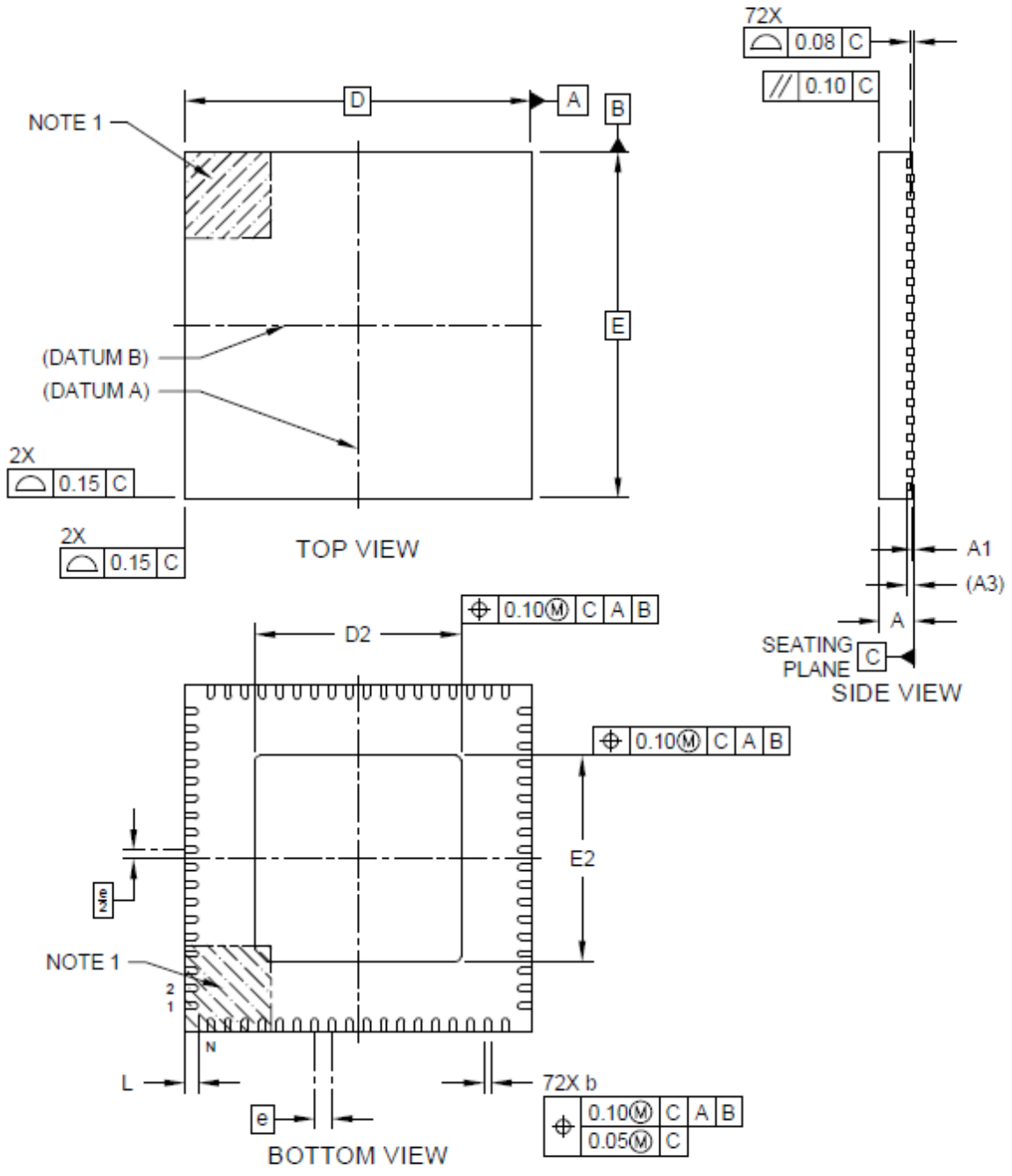
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

72-Lead Very Thin Plastic Quad Flat, No Lead Package (LNC) - 10x10x1.0 mm Body [VQFN] with 5.95x5.95 Exposed Pad; Microsemi Legacy Package

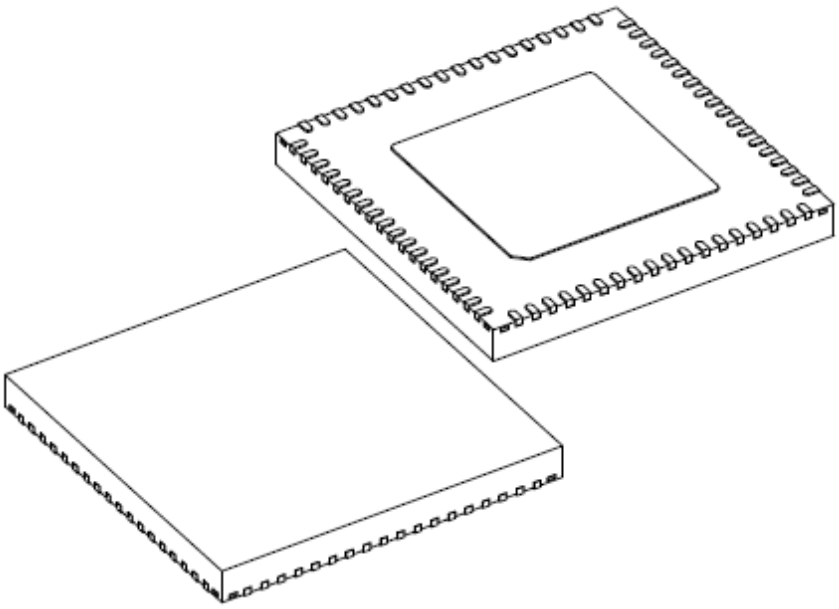
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25387 Rev A Sheet 1 of 2

72-Lead Very Thin Plastic Quad Flat, No Lead Package (LNC) - 10x10x1.0 mm Body [VQFN] with 5.95x5.95 Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		72	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.20REF	
Overall Length	D		10.00 BSC	
Exposed Pad Length	D2	5.85	5.95	6.05
Overall Width	E		10.00 BSC	
Exposed Pad Width	E2	5.85	5.95	6.05
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25387 Rev A Sheet 2 of 2

72-Lead Very Thin Plastic Quad Flat, No Lead Package (LNC) - 10x10x1.0 mm Body [VQFN] with 5.95x5.95 Exposed Pad; Microsemi Legacy Package

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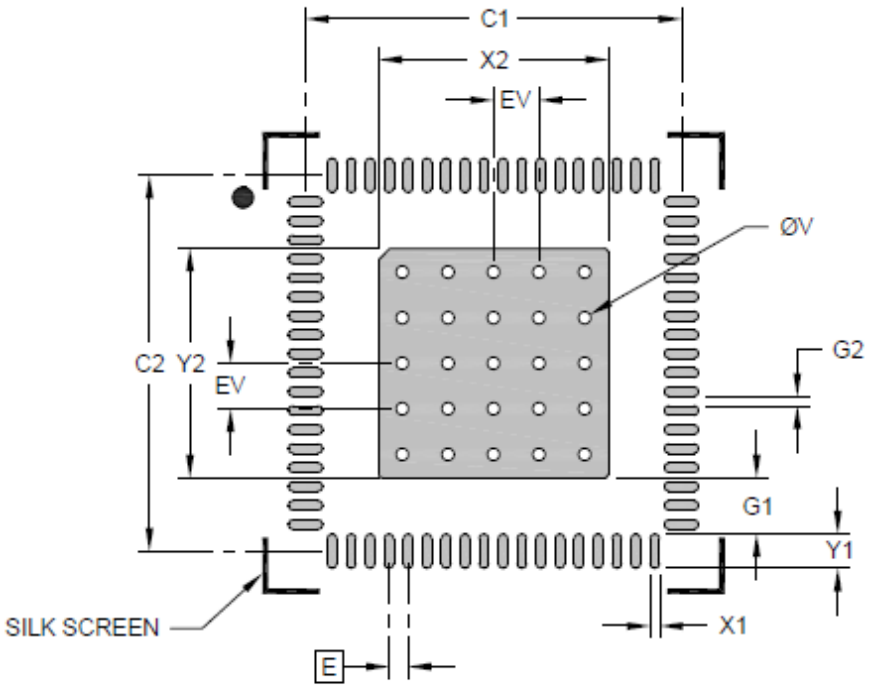

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			6.05
Optional Center Pad Length	Y2			6.05
Contact Pad Spacing	C1		9.90	
Contact Pad Spacing	C2		9.90	
Contact Pad Width (Xnn)	X1			0.25
Contact Pad Length (Xnn)	Y1			0.90
Contact Pad to Center Pad (Xnn)	G1	1.48		
Contact Pad to Contact Pad (Xnn)	G2	0.25		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27387 Rev A

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006911A (07-30-24)	—	Converted Microsemi data sheet ZL40292 to Microchip DS20006911A. Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	X	X
Device	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL40292: 20-Output DB2000Q Buffer with Ultra-Low Additive Jitter
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 72-Lead 10 mm x 10 mm VQFN Package
Media Type:	G = 168/Tray F = 2,000/Reel
Finish:	1 = Pb Free with Matte Sn Lead Finish Equating to RoHS e3

Examples:

a) ZL40292LDG1: ZL40292, Leadless Chip Carrier, 72-Lead VQFN Package, 168/ Tray, Pb Free with Matte Sn Lead Finish Equating to RoHS e3

b) ZL40292LDF1: ZL40292, Leadless Chip Carrier, 72-Lead VQFN Package, 2,000/ Reel, Pb Free with Matte Sn Lead Finish Equating to RoHS e3

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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