ZL40272

Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/ LVPECL Fanout Buffer with Per-Output Enable Control

Features

- 3-to-1 input Multiplexer: Two Inputs Accept Any Differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a Single-Ended Signal and the Third Input Accepts a Crystal or a Single-Ended Signal
- Twelve Differential HCSL/LVDS/LVPECL Outputs
- Ultra-Low Additive Jitter: 24 fs (Integration Band: 12 kHz to 20 MHz at 625 MHz Clock Frequency)
- Supports Clock Frequencies from 0 GHz to 1.5 GHz
- Supports 2.5V or 3.3V Power Supplies on HCSL/ LVDS/LVPECL Outputs
- Embedded Low Drop Out (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output to Output Skew of 50 ps
- Device Controlled via I^2C or Hardware Control Pins
- Factory Configurable Default Settings via OTP
- Transparent for Spread Spectrum Clock

Applications

- PCIe Gen1/2/3/4/5 Clock Distribution
- Wired Communications: OTN, SONET/SDH, GE, 10 GE, FC, and 10G FC
- General Purpose Clock Distribution
- Low Jitter Clock Trees
- Logic Translation
- Clock and Data Signal Restoration
- Wireless Communications
- High Performance Microprocessor Clock Distribution
- Test Equipment

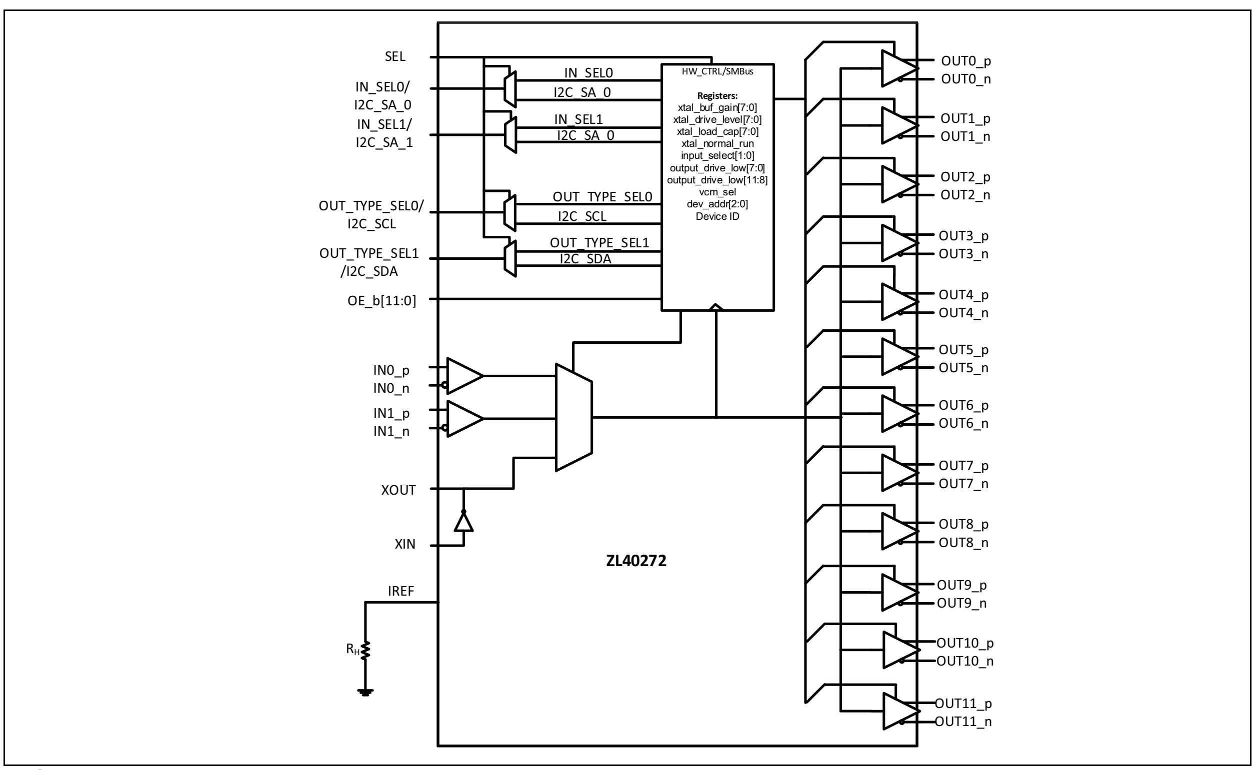

FIGURE 0-1: Functional Block Diagram.

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1.0 PIN DESCRIPTION AND CONFIGURATION

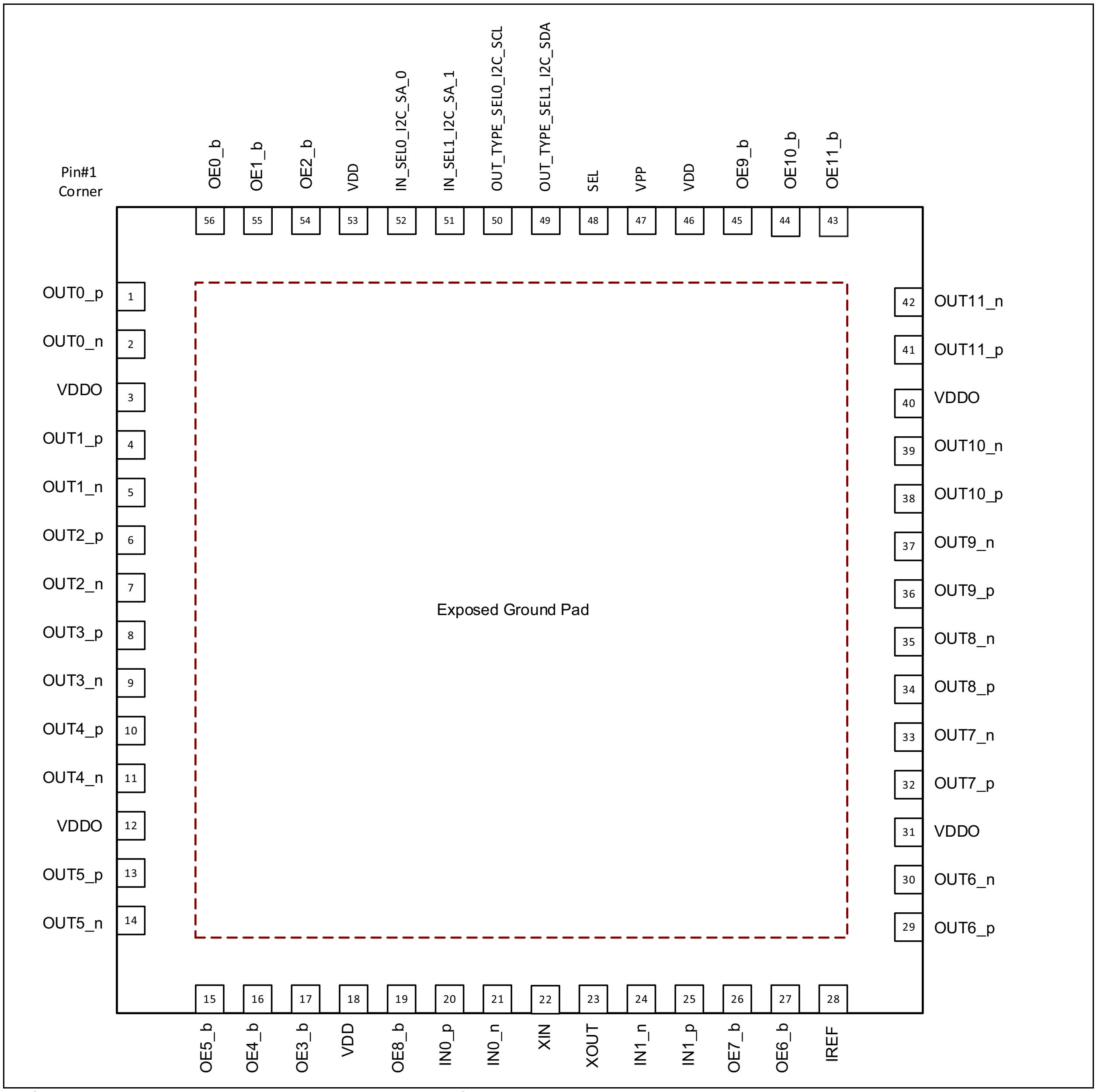


FIGURE 1-1: *56-Lead 8 mm x 8 mm QFN.*

All device inputs and outputs are LVPECL, unless described otherwise. The I/O column uses the following symbols: I – input, IPU – input with 300 kΩ internal pull-up resistor, IPD – input with 300 kΩ internal pull-down resistor, IAPU – input with 31 kΩ internal pull-up resistor, IAPD – input with 30 kΩ internal pull-down resistor, IAPU/APD – input biased to $V_{DD}/2$ with 60 kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/OOD – Input/Open-Drain Output pin, NC – No connect, P – power supply pin.

TABLE 1-1: PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Description
Input References			
20	IN0_p	I_{APD}	**Differential/Single-Ended References 0 and 1** Input frequency range from 0 Hz to 1.5 GHz. Non-inverting inputs (_p) are pulled down with internal 30 kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60 kΩ internal resistors (30 kΩ equivalent) to keep inverting input voltages at $V_{DD}/2$ when inverting inputs are left floating (device fed with a single-ended reference).
21	IN0_n	$I_{APU/APD}$	
25	IN1_p	I_{APD}	
24	IN1_n	$I_{APU/APD}$	
Output Clocks			
1	OUT0_p	O	**Ultra-Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 11** Output frequency range 0 Hz to 1.5 GHz In I^2C bus controlled mode (SEL pin pulled high on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output is programmable via I^2C Bus In Hardware control mode (SEL pin pulled low on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output is controlled via OUT_TYPE_SEL0/1 pins.
2	OUT0_n		
4	OUT1_p		
5	OUT1_n		
6	OUT2_p		
7	OUT2_n		
8	OUT3_p		
9	OUT3_n		
10	OUT4_p		
11	OUT4_n		
13	OUT5_p		
14	OUT5_n		
29	OUT6_p		
30	OUT6_n		
32	OUT7_p		
33	OUT7_n		
34	OUT8_p		
35	OUT8_n		
36	OUT9_p		
37	OUT9_n		
38	OUT10_p		
39	OUT10_n		
41	OUT11_p		
42	OUT11_n		

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th colspan="3">Description</th></tr>
<tr><td colspan="6">Control</td></tr>
<tr><td rowspan="6">52</td><td rowspan="6">IN_SEL0/
I2C_SA_0</td><td rowspan="6">I_{PD}</td><td colspan="3">Input Select 0 or I²C Address. When SEL pin is low, this pin is Input Select 0 hardware control input. When SEL pin is high, this pin together with pin 51 provides address for I²C Bus. This pin is pulled-down with 300 kΩ resistor.</td></tr>
<tr><td>IN_SEL1</td><td>IN_SEL0</td><td>OUTN</td></tr>
<tr><td>0</td><td>0</td><td>Input 0 (IN0)</td></tr>
<tr><td>0</td><td>1</td><td>Input 1 (IN1)</td></tr>
<tr><td>1</td><td>0</td><td>Crystal Oscillator or Overdrive</td></tr>
<tr><td>1</td><td>1</td><td>Crystal Bypass</td></tr>
<tr><td>51</td><td>IN_SEL1/
I2C_SA_1</td><td>I_{PD}</td><td colspan="3">Input Select 1 or Serial Interface Input. When SEL pin is low, this pin is Input Select 1 hardware control pin. When SEL pin is high, this pin together with pin 45 provides address for I²C Bus.
This pin is pulled down with 300 kΩ resistor.</td></tr>
<tr><td rowspan="6">50</td><td rowspan="6">OUT_TYPE_-
SEL0
/I2C_SCL</td><td rowspan="6">I/O</td><td colspan="3">Output Signal Type or I²C Bus Clock.
When SEL pin is low, this pin and pin 49 selects output type.
When SEL pin is high, this pin is I²C Bus Clock.</td></tr>
<tr><td>OUT_TYPE_SEL_1</td><td>OUT_TYPE_SEL_0</td><td>Output [11:0]</td></tr>
<tr><td>0</td><td>0</td><td>HCSL</td></tr>
<tr><td>0</td><td>1</td><td>LVDS</td></tr>
<tr><td>1</td><td>0</td><td>LVPECL</td></tr>
<tr><td>1</td><td>1</td><td>High-Z (disabled)</td></tr>
<tr><td>49</td><td>OUT_TYPE_-
SEL1
/I2C_SDA</td><td>I
I/O_{OD}</td><td colspan="3">Output Signal Type or I²C Bus I/O Data
When SEL pin is low, this pin and pin 50 selects output type.
When SEL pin is high, this pin is an I/O pin (Input/Open-Drain) for I²C Bus.</td></tr>
<tr><td>56</td><td>OE0_b</td><td rowspan="12">I_{PD}</td><td colspan="3" rowspan="12">Output Enable Control.
When OEn_b is low, the output n where n = {0,..,11} is active.
When OEn_b is high, the output is disabled (High-Z)
OEn_b pins are pulled-down with 300 kΩ resistor</td></tr>
<tr><td>55</td><td>OE1_b</td></tr>
<tr><td>54</td><td>OE2_b</td></tr>
<tr><td>17</td><td>OE3_b</td></tr>
<tr><td>16</td><td>OE4_b</td></tr>
<tr><td>15</td><td>OE5_b</td></tr>
<tr><td>27</td><td>OE6_b</td></tr>
<tr><td>26</td><td>OE7_b</td></tr>
<tr><td>19</td><td>OE8_b</td></tr>
<tr><td>45</td><td>OE9_b</td></tr>
<tr><td>44</td><td>OE10_b</td></tr>
<tr><td>43</td><td>OE11_b</td></tr>
<tr><td colspan="6">Crystal Oscillator</td></tr>
<tr><td>22</td><td>XIN</td><td>I</td><td colspan="3">Crystal Oscillator Input or Crystal Bypass Mode or Crystal Over-drive Mode:
If crystal circuit is not used, pull-down this pin or connect it to the ground.</td></tr>
<tr><td>23</td><td>XOUT</td><td>O</td><td colspan="3">Crystal Oscillator Output</td></tr>
</table>

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	Type	Description
Hardware/I²C Bus Control selection			
48	SEL	I	**Select Control.** When this pin is low, the device is controlled via hardware pins, IN_-SEL0/1 and OE. When this pin is high, the device is controlled via I^2C Bus port. Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.
28	IREF	I	**Output Current Select.** Connect this pin to the ground via resistor R: HCSL/LVDS/LVPECL for 100Ω differential transmission line: R = 536Ω HCSL for 85 Ω differential transmission line: R = 422Ω
Power and Ground			
18 46 53	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply.
3 12 31 40	VDDO	P	**Positive Supply Voltage for Differential Outputs.** Connect to 3.3V or 2.5V power supply. These pins power up differential outputs OUT[11:0]_p/n.
47	VPP	P	**Positive Supply Voltage for Programming OTP Memory.** This pin is used for generating custom configurations on ATE. Connect to ground for normal operation.
ePad	GND	P	**Ground.** Connect to the ground.

NOTES:

2.0 FUNCTIONAL DESCRIPTION

The ZL40272 is an I^2C Bus programmable or hardware pin controlled low additive jitter, low power 3 x 12 HCSL/LVDS/LVPECL fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single-ended (LVPECL or LVCMOS) format; the third input can accept a single-ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building a crystal oscillator are built into the device, such as load capacitance, series resistors, and shunt resistors.

The ZL40272 has twelve HCSL/LVDS/LVPECL outputs that can be powered from a 3.3V or 2.5V supply. Each output can be independently enabled/disabled via OEn_b pins or via I^2C Bus. The type of each output driver can be programmed to be LVPECL, HCSL or LVDS. Hence, the device can be configured to support different signaling formats depending on the application.

The device operates from 2.5V ±5% or 3.3V ±5% supply. Its operation is guaranteed over the industrial temperature range of –40°C to +85°C.

2.1 Clock Inputs

The following block diagrams show how to terminate different signals fed to the ZL40272 inputs.

The device has programmable common mode input voltage. The common mode voltage can be programmed in COMMODSEL register at address 0x0C:

COMMODSEL.vcm_sel = 1 (default) for inputs with common mode between 0V and 1V, such as HCSL.

COMMODSEL.vcm_sel = 0 for inputs with common mode voltage between 1V and 2V, such as LVPECL and LVDS.

For devices intended to be used in hardware pin controlled mode, the default common mode voltage can be changed in factory by programming OTP.

Figure 2-1 shows how to terminate a single-ended output such as LVCMOS. Resistors R1 and R2 should present 50Ω equivalent resistance to the line and $R_O + R_S$ should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance (standard LVCMOS output, for example), the value of series resistor R_S should be increased. This will reduce the voltage swing at the input, but this should be fine as long as the input voltage swing requirement is not violated (Table 9). The source resistors of R_S = 330Ω could be used for a standard LVCMOS driver. This will provide 471 mV of voltage swing for 3.3V LVCMOS driver with the peak load current of (3.3V* 0.85) *(1/(330Ω + 50Ω)) = 7.3 mA for common mode voltage biased at 0.5V. For common mode voltage of $V_{DD}/2$, the peak current will be lower.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

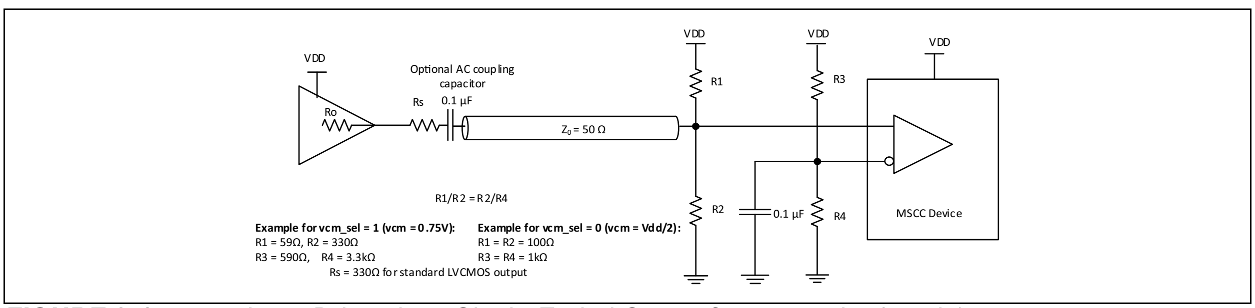


FIGURE 2-1: *Input Driven by a Single-Ended Output for vcm_sel = 0 and 1.*

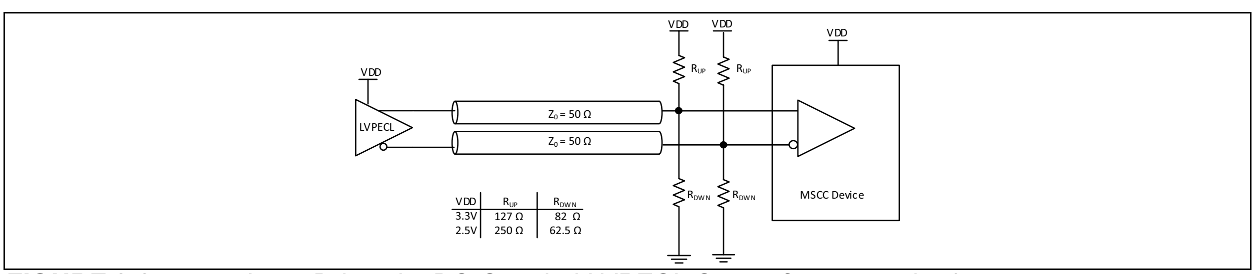


FIGURE 2-2: *Input Driven by DC-Coupled LVPECL Output for vcm_sel = 0.*

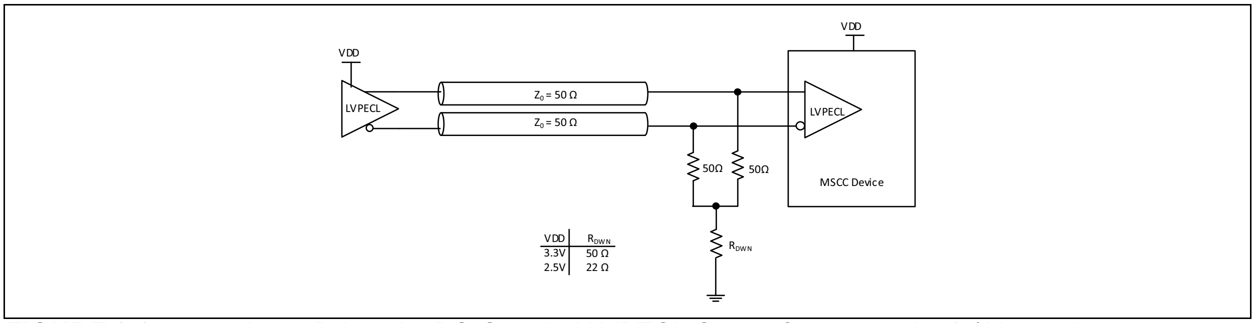


FIGURE 2-3: *Input Driven by DC-Coupled LVPECL Output for vcm_sel = 0 (Alternative Termination).*

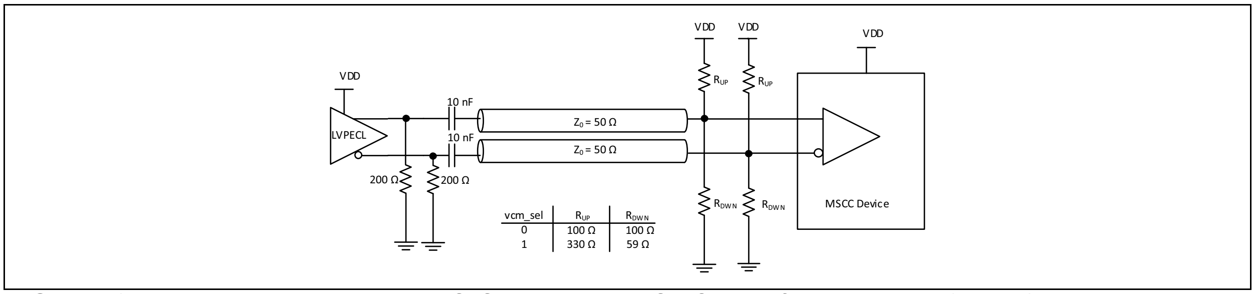


FIGURE 2-4: *Input Driven by AC-Coupled LVPECL Output for vcm_sel = 0 and 1.*

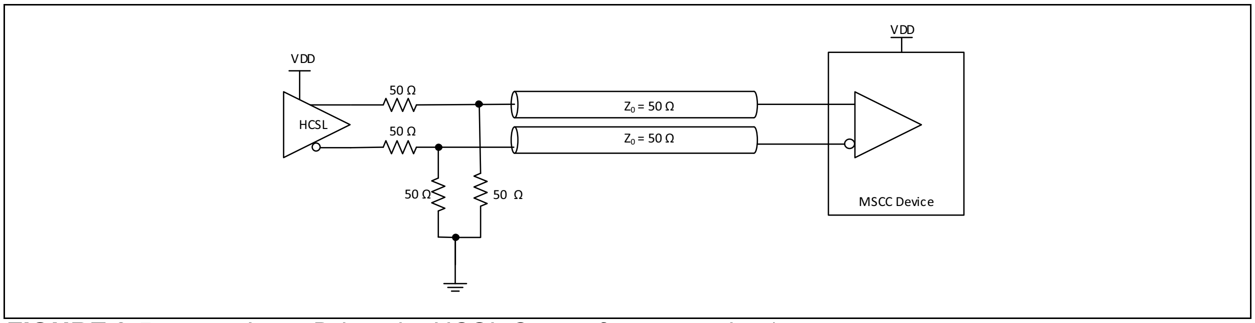


FIGURE 2-5: *Input Driven by HCSL Output for vcm_sel = 1.*

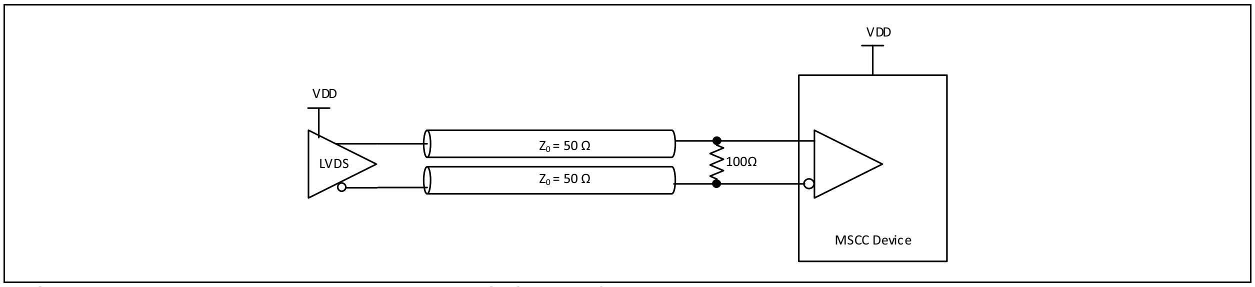


FIGURE 2-6: *Input Driven by LVDS Output for vcm_sel = 0.*

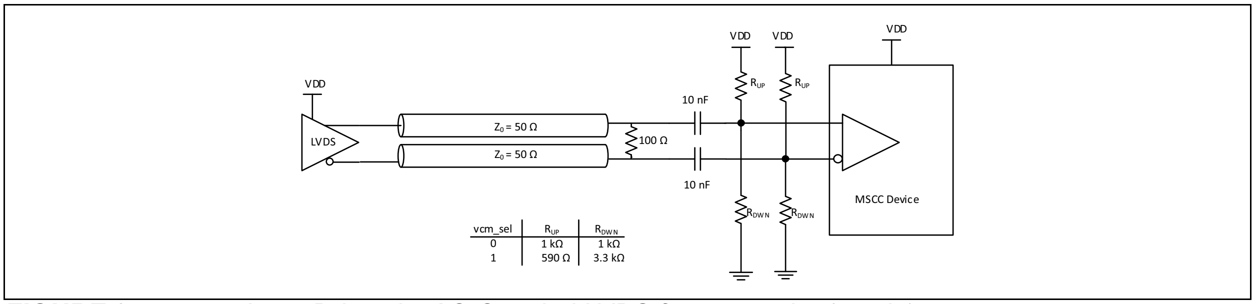


FIGURE 2-7: *Input Driven by AC-Coupled LVDS for vcm_sel = 0 and 1.*

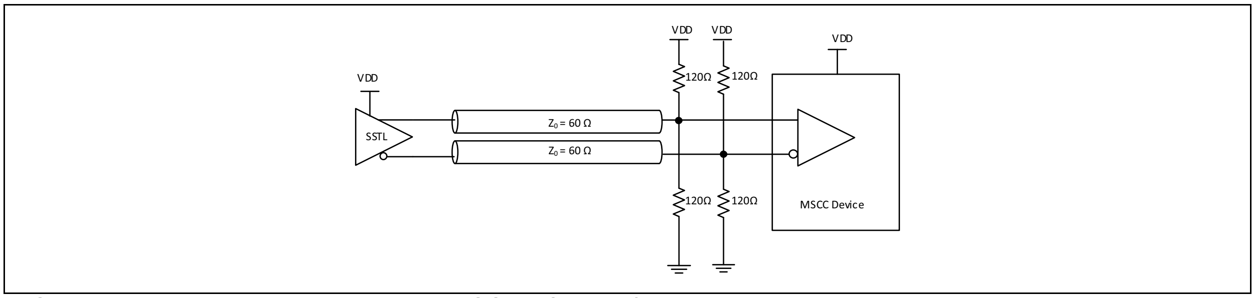


FIGURE 2-8: *Input Driven by an SSTL Output for vcm_sel = 1.*

2.2 Clock Outputs

Differential outputs LVPECL, LVDS, and HCSL should have same termination as corresponding outputs described in previous section.

The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single-ended output (for example, driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 2-9. This is to provide a nominal common mode impedance of 10Ω or higher, which is typical for differential terminations.

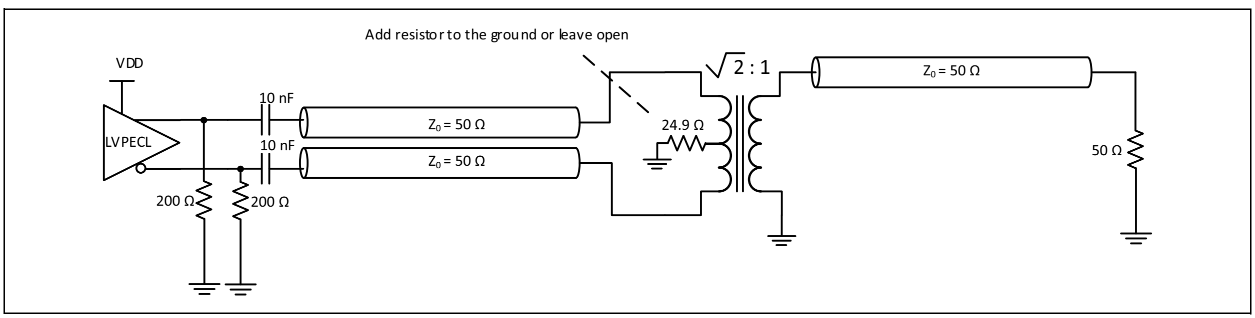


FIGURE 2-9: *Driving a Load via Transformer.*

2.3 Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8 MHz to 160 MHz. To be able support crystal resonators with different characteristics, all internal components are programmable.

The load capacitors can be programmed from 0 pF to 21.75 pF (4 pF default) with resolution of 0.25 pF, which not only meets load requirement for most crystal resonator but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in five steps and series resistor can be adjusted as parallel combination of seven different resistors: 0Ω, 10.5Ω, 21Ω, 42Ω, 84Ω, 161Ω, and 312Ω. (84Ω default) Although the first resistor is 0Ω, the series resistance R_S will be slightly higher than 0Ω due to parasitic resistance of the switch that connects to the resistor. Hence, the minimum series resistance is achieved when all seven resistors are connected in parallel. The shunt resistor is fixed and its value is 500 kΩ.

In Hardware Controlled mode, the capacitive load is set at 4 pF, internal series resistance to 84Ω and they cannot be changed. For Crystals that require higher load or series resistance, additional capacitance and/or series resistance can be added externally as shown in the Figure 2-10.

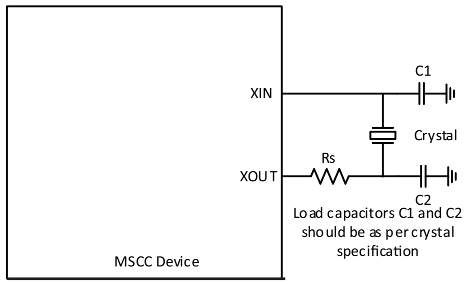


FIGURE 2-10: Crystal Oscillator Circuit in Hardware Controlled Mode.

2.4 Termination of Unused Inputs and Outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by a 1 kΩ resistor. Unused outputs should be left unconnected.

2.5 Power Consumption

The device total power consumption can be calculated as:

EQUATION 2-1:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_\mathrm{DIFF}}$$

Where:

$P_S = V_{DD} \times I_S$: is the core power consumed by input buffers. If XTAL is running this power, it should be set to zero. The static current (I_S) is specified in Table 4-2.

$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$: is the core power consumption of the XTAL circuit. The current of the XTAL circuit is provided in Table 4-2. If XTAL is not used, the power consumption is equal to zero.

$P_C = V_{DDO} \times I_{DD\_CM}$: Common output power shared among all twelve outputs. The current I_{DD_CM} is specified in Table 4-2.

$P_{O\_DIFF} = V_{DDO} \times (I_{DD\_LVDS} \times N_1 + I_{DD\_LVPECL} \times N_2 + I_{DD\_HCSL} \times N_3)$: Output power where the output current are specified in Table 4-2. N_1, N_2, and N_3 are the number of enabled LVPECL, LVDS, and HCSL outputs respectively and $N_1 + N_2 + N_3$ is less than or equal to 12.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption.

EQUATION 2-2:

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where:

N_1, N_2, N_3 = The number of enabled LVPECL, LVDS and HSCL outputs respectively. Because there are twelve differential outputs N1 + N2 + N3 will be less or equal to 12.

$P_{LVPECL} = (V_{SW} / 50\Omega) \times (V_{SW} + V_B)$: V_{SW} is the voltage swing of the LVPECL output. V_B is the LVPECL bias voltage equal to $V_{DD} - 2V$.

$P_{LVDS} = V_{SW} / 100\Omega$: V_{SW} is the voltage swing of the LVDS output.

$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (50\Omega + 50\Omega)$: V_{SW} is the voltage swing of the HCSL output. 50Ω is the termination resistance and 50Ω is the series resistance of the HCSL output.

2.6 Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with a 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board, each power supply could be further insulated with a low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent components from the noise generated from the device. Figure 2-11 shows recommended decoupling for each power pin.

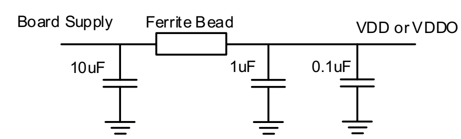


FIGURE 2-11: Power Supply Filtering.

2.7 Power Supplies and Power-Up Sequence

The device has two different power supplies: VDD and VDDO, which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1-1.

The device is not sensitive to the power-up sequence. For example, a commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence).

2.8 Host Interface

ZL40272 can be controlled via hardware pins (SEL pin tied low) or via I^2C Bus (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on-the-fly.

2.8.1 HARDWARE CONTROL MODE

In this mode, ZL40272 is controlled via Input Select pins (IN_SEL[1:0]) that select which one of three inputs is fed to outputs as show in Table 2-1, OUT_TYPE_SEL[1:0] pins which select signal level (HCSL, LVDS, LVPECL or Hi-Z) and output enable pins (OE_b) for each output as shown in Table 2-2.

All input control pins have low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and VDD (2.5V or 3.3V).

TABLE 2-1: INPUT CLOCK SELECTION

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN (crystal input pin)

TABLE 2-2: OUTPUT TYPE SELECTION

OE_N_b	OUT_TYPE_SEL[1:0]	Output
0	00	HCSL
0	01	LVDS
0	10	LVPECL
1	00 or 01 or 10	High-Z (on output N)
X	11	High-Z (on all outputs)

Output is disabled synchronously and depending of the input frequency it can take up to 5 clock cycles to disable the output ($t_2 - t_1 \leq 5*T$, where T is the input clock period) as shown in Figure 2-12.

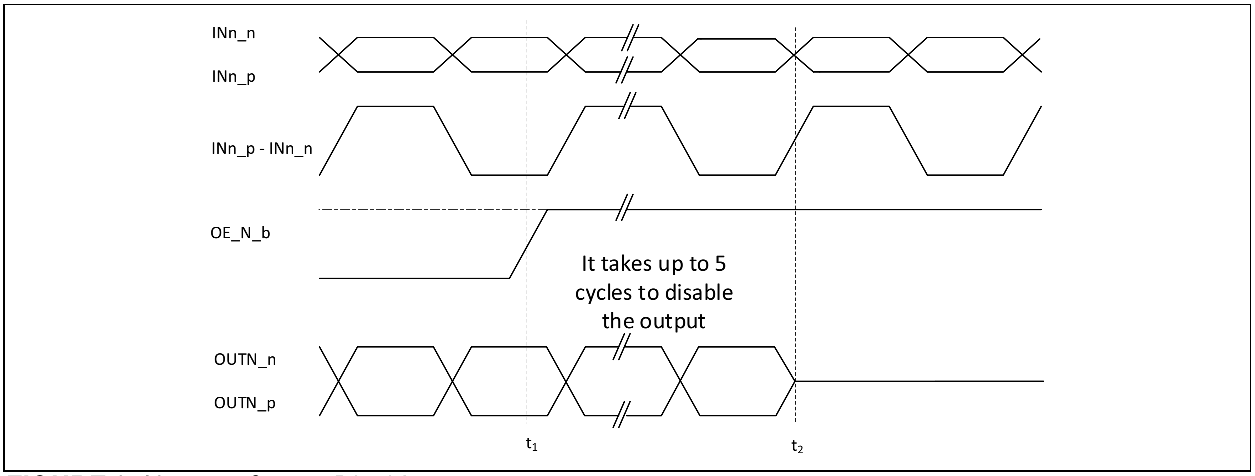


FIGURE 2-12: *Output Disable.*

Any outputs can be enabled by pulling the corresponding OE_b pin low. As soon as OE_N_b pin goes low (t_1) the output N will go from high-Z to low (OUTN_p = low, OUTN_n = high) and will start to track the input after up to 5 input clock cycles ($t_2 - t_1 \leq 5*T$, where T is the input clock period) depending on the frequency of the input clock as shown in Figure 2-13.

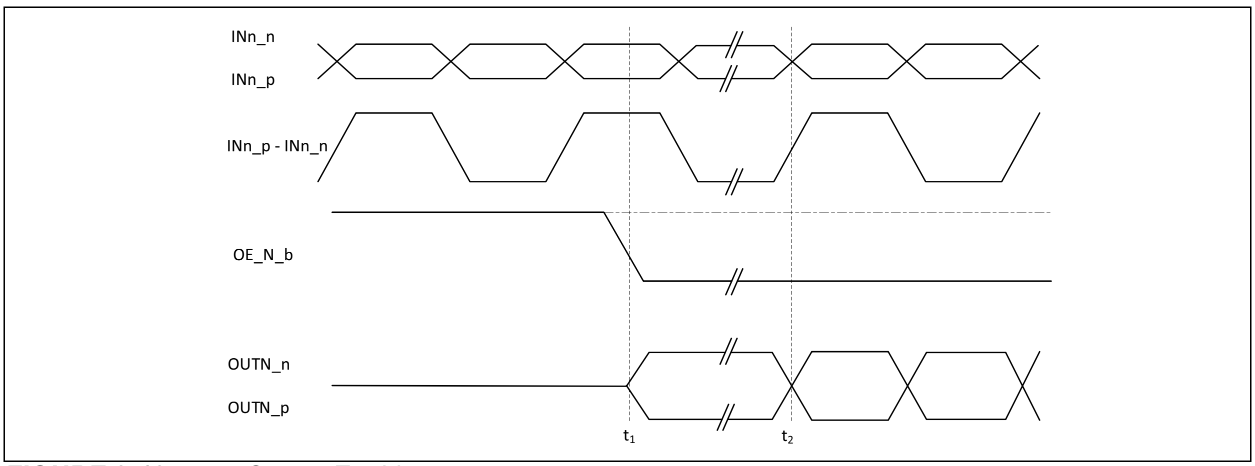


FIGURE 2-13: *Output Enable.*

2.8.2 I²C BUS CONTROL MODE

ZL40272 is controlled via four pin I²C Bus slave interface as shown in the following figure.

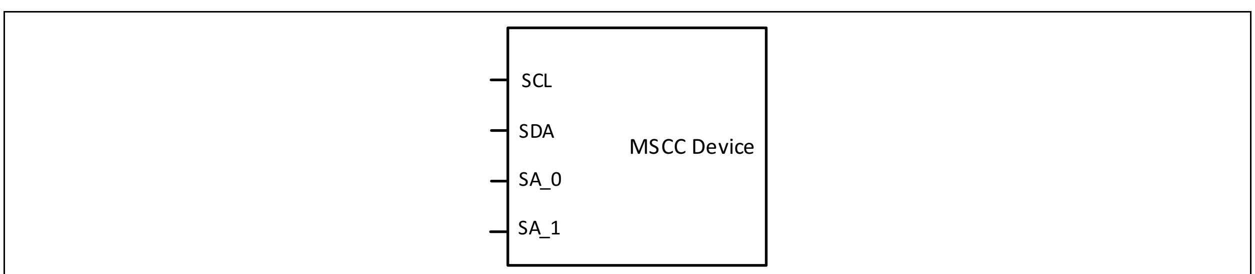


FIGURE 2-14: *I²C Bus Slave Interface.*

The address selection is done via SA_0 and SA_1 hardware pins, which select the appropriate address for the device.

TABLE 2-3: I²C BUS ADDRESS TABLE

SA_1	SA_0	I²C Bus Address
0	0	0x34
0	1	0x35
1	0	0x36
1	1	0x37

2.9 I²C Bus Byte Read/Write

Reading or writing a register or registers in a I²C Bus slave device is MSB first and LSB last in one-byte blocks.

The access from I²C master starts with the start condition followed by the slave address and the write indicator bit. This is then followed by the command byte which in bits [6:0] contains the address of the register to be accessed for byte mode or the first register to be accessed in the burst mode. The most significant bit in the command byte must be set to 1.

Byte Read. The standard byte read is as shown in Figure 2-15. The command byte is followed the slave address and read indication bit. The device (slave) will respond by sending the requested byte.

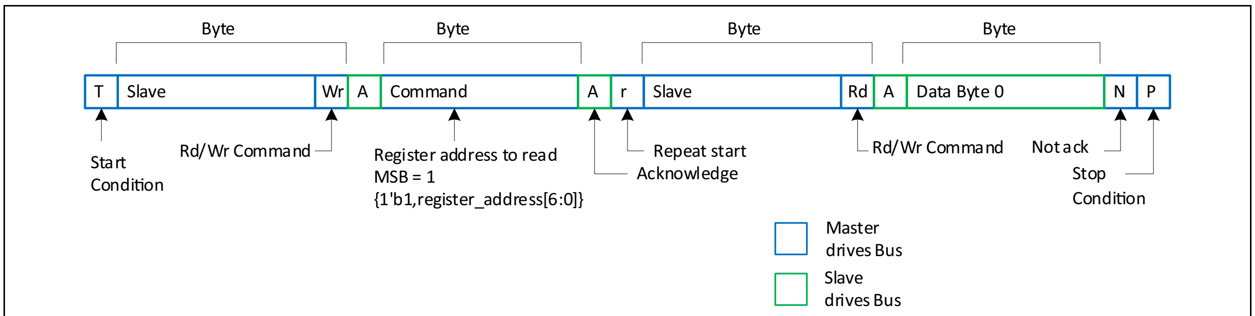


FIGURE 2-15: I²C Bus Byte Read.

Write. Figure 2-16 illustrates the standard byte write After the written byte has been acknowledged by the device, the master will assert the stop signal.

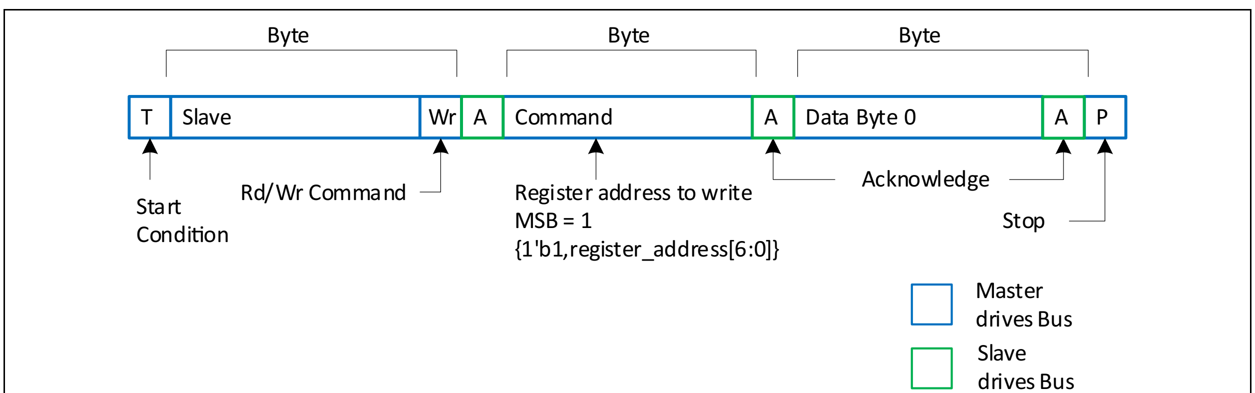


FIGURE 2-16: I²C Bus Byte Write.

2.10 I²C Bus Burst Read/Write

Burst Read and Write are very similar to Byte Read and Write.

Burst Read. Figure 2-17 illustrates the Burst Read. The I²C master acknowledges after each received byte and finally sends a Not Acknowledge (NACK) followed with Stop Condition.

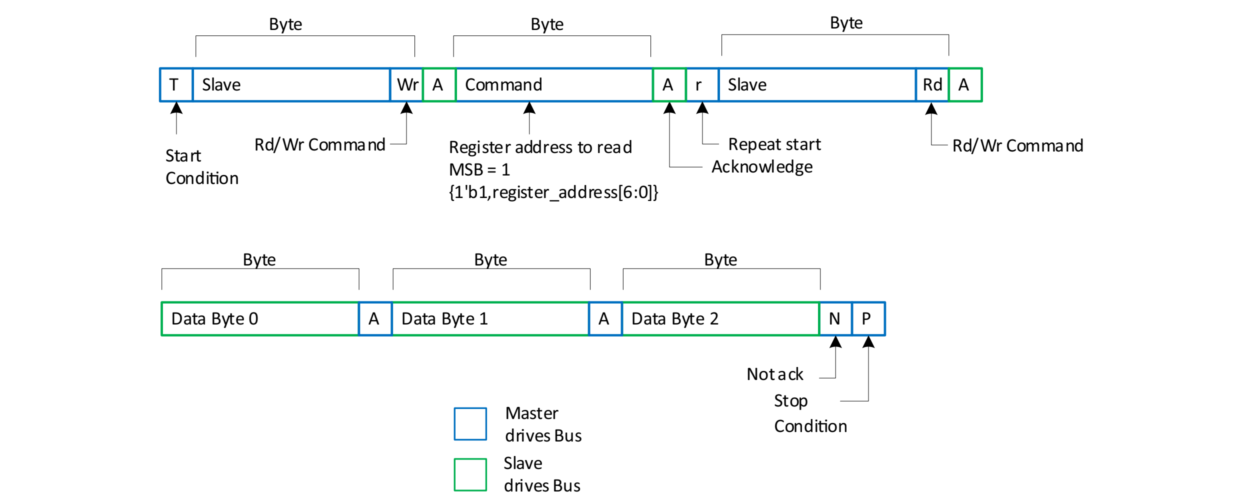


FIGURE 2-17: *I²C Bus Burst Read.*

Burst Write. Figure 2-18 illustrates the Burst Write. The I²C master will send the Stop Condition after the last data byte.

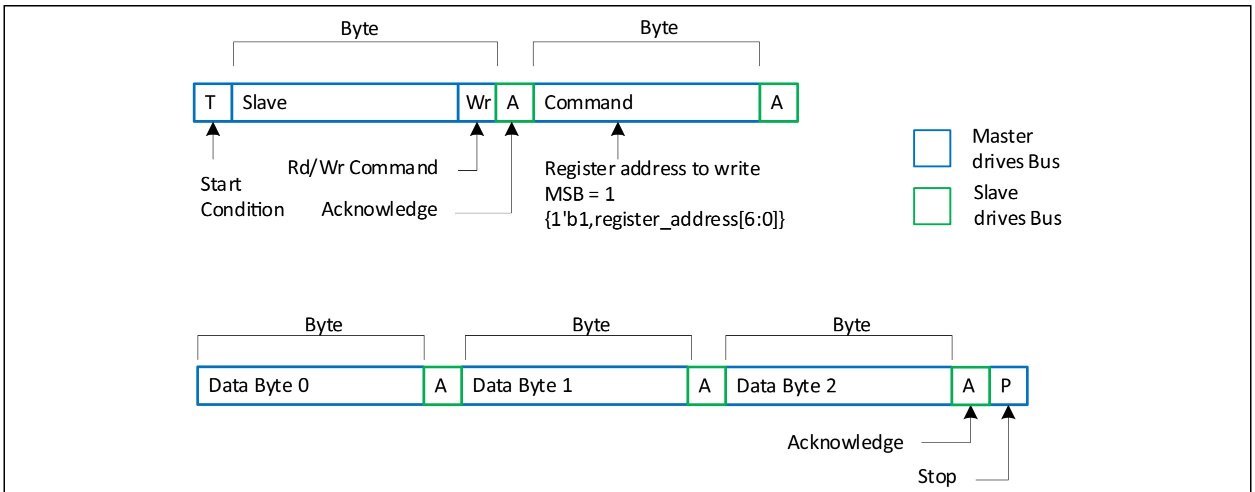


FIGURE 2-18: *I²C Bus Burst Write.*

2.11 Typical Phase Noise Characteristics

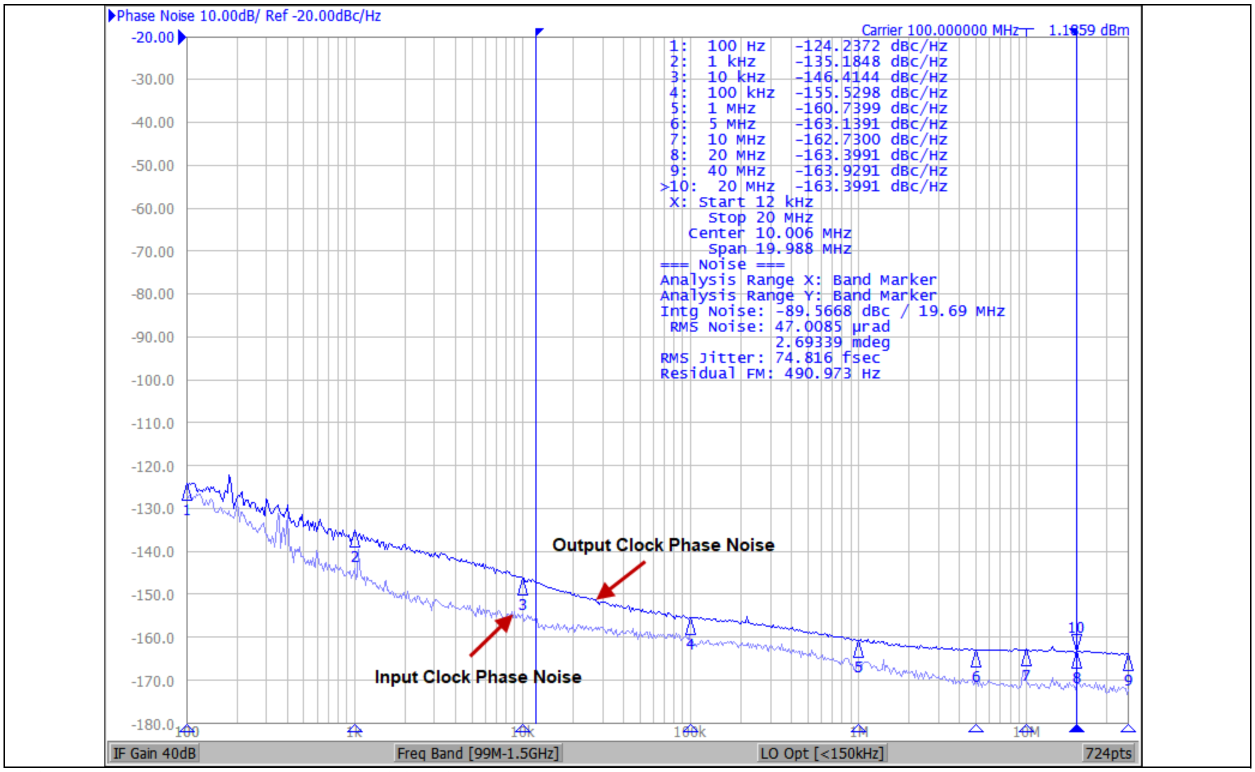


FIGURE 2-19: *100 MHz HCSL Output Phase Noise.*

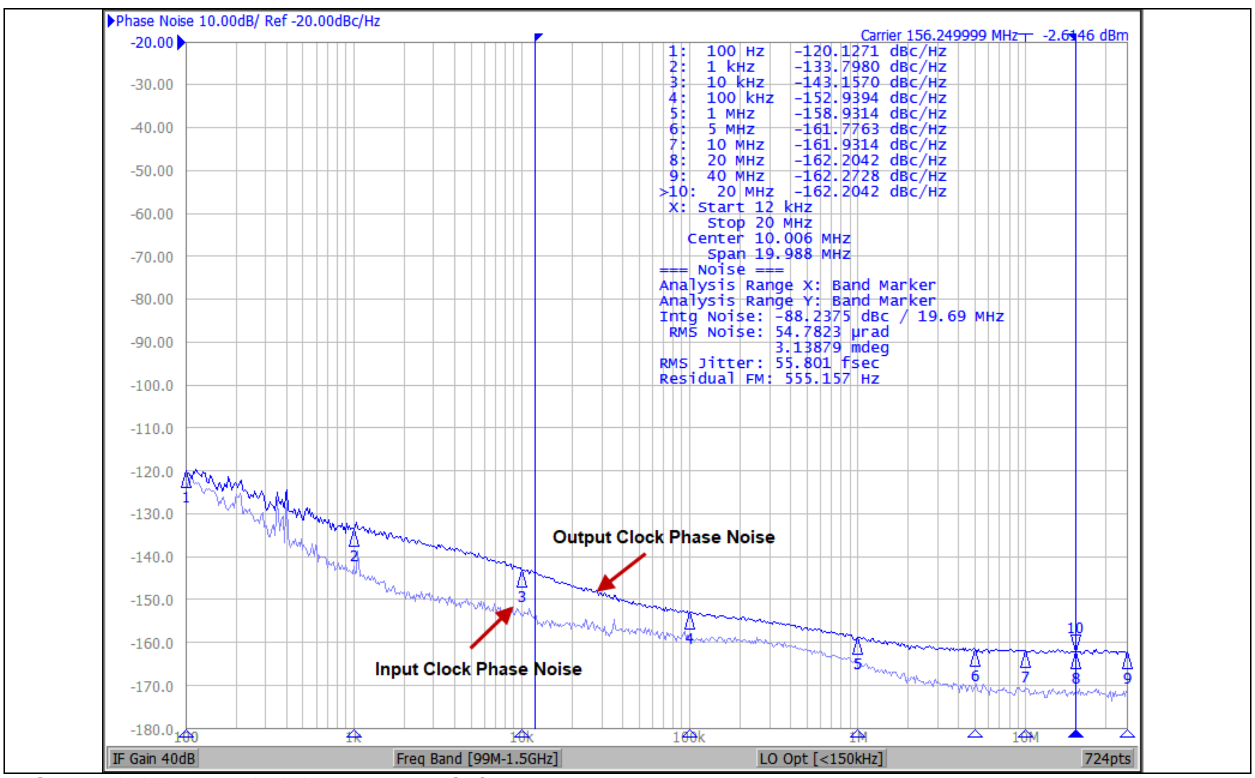


FIGURE 2-20: *156.25 MHz LVDS Output Phase Noise.*

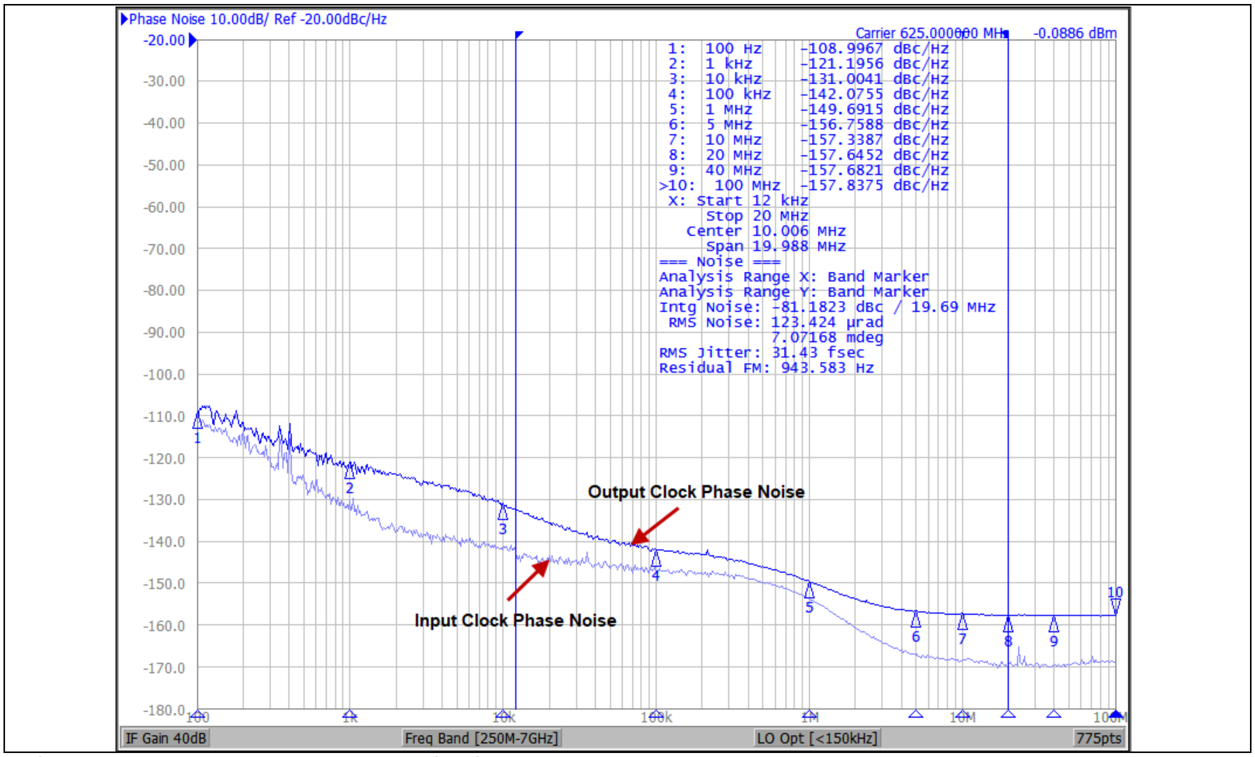


FIGURE 2-21: *625 MHz LVPECL Output Phase Noise.*

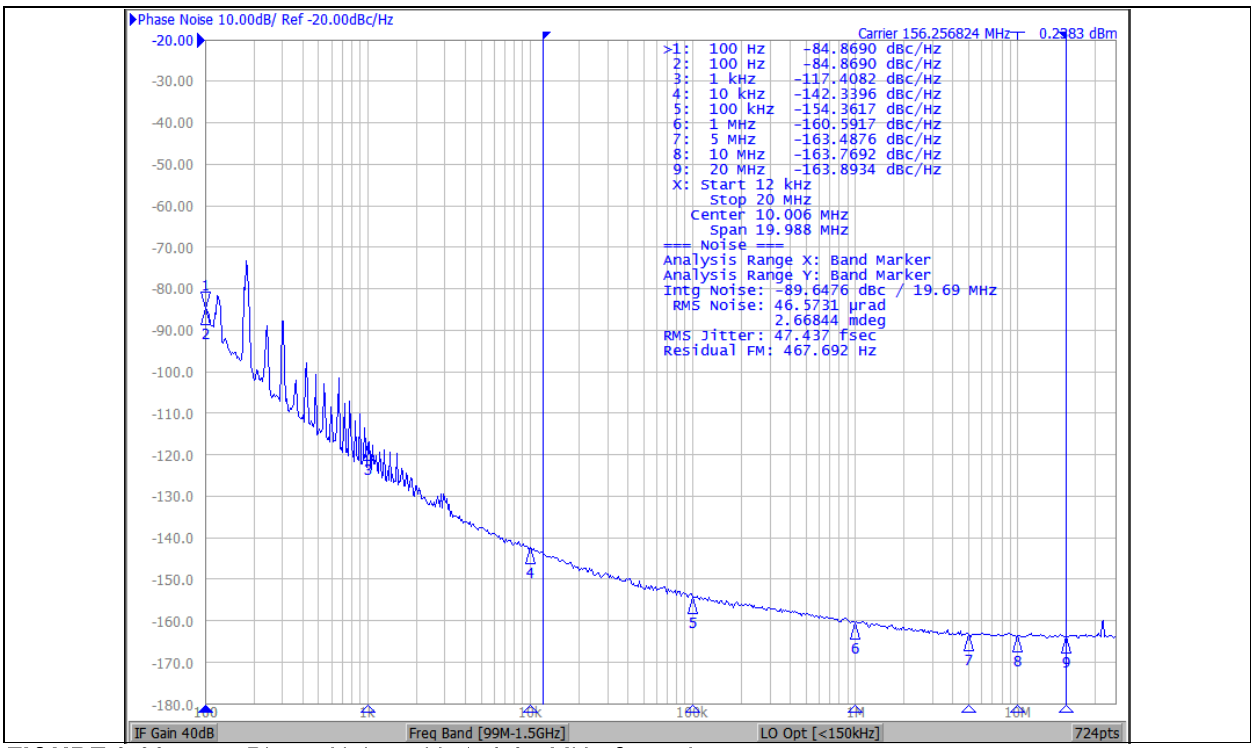


FIGURE 2-22: *Phase Noise with 156.25 MHz Crystal.*

3.0 REGISTER MAP

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device. The default settings can be modified via factory programmable OTP memory.

TABLE 3-1: REGISTER MAP

Address I^2C A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[7:0]
01	XTALDL	xtal_drive_level[7:0]
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	OUTLOWALL	out_low_all
05	INSEL	input_select[1:0]
06	—	Not used.
07	DRVTYPE0	driver_type[7:0] (differential output OUT3, OUT2, OUT1, OUT0)
08	DRVTYPE1	driver_type[15:8] (differential output OUT7, OUT6, OUT5, OUT4)
09	DRVTYPE2	driver_type[23:16] (differential output OUT11, OUT10, OUT9, OUT8)
0A	OUTLOW0	output_drive_low[7:0]
0B	OUTLOW1	output_drive_low[11:8]
0C	COMMODSEL	vcm_sel
0D	—	Not used.
0E	DEVADDR	dev_addr[2:0]
0F	Reserved	Reserved
10	Reserved	Reserved
11	DEVICEID	Device Identification
12-1F	Reserved	Reserved

TABLE 3-2: 0X00 XTALBG - XTAL BUFFER GAIN

Bit	Name	Description	Type	Reset
7:0	xtal_buf_gain[7:0]	Programs crystal buffer (inverting amplifier) gain. Every bit pair (bits: 01, 23, 45, 67) of this register correspond to additional equal gain block which can be added (bits set) or removed (bits cleared). Minimum gain is 0x00 (default) and 0xFF is maximum gain When reference input mode is “bypass XTAL mode” or “differential input modes” with HIGH xtal_normal_run bit, the buffer is disabled and follows “Input Selection”. When xtal_normal_run bit is LOW, XTAL buffer is in the “xtal forced run” mode and keep running. 8’b0000_0000: default crystal buffer strength. 8’b0000_0011: enable additional buffer strength 8’b0000_1100: enable additional buffer strength 8’b0011_0000: enable additional buffer strength 8’b1100_0000: enable additional buffer strength	RW	FF

TABLE 3-3: 0X01 XTALDL - XTAL DRIVE LEVEL

Bit	Name	Description	Type	Reset
7:0	xtal_drive_level[7:0]	Internal damping resistance of crystal circuit to limit external crystal's drive level µW. The value of damping resistor is determined by crystal's motion resistance of crystal's equivalent circuit. Drive level should be lower than crystal manufacturer's specification. Crystal's equivalent values should be requested to the manufacturer, (motion resistance and shunt capacitance). The selected resistors are connected to XOUT. Multiple bit combinations available by 7-bit control. Because they use parallel connections, 0xFF is the smallest resistance and 0x01 is the highest resistance. 8'b0000_0000: disable all resistors 8'b0000_0001: 312Ω resistor 8'b0000_0010: 161Ω resistor 8'b0000_0100: 84Ω resistor 8'b0000_1000: 42Ω resistor 8'b0001_0000: 21Ω resistor 8'b0010_0000: 10.5Ω resistor 8'b0100_0000: 0Ω connection 8'b1000_0000: not used	RW	04

TABLE 3-4: 0X02 XTALLC - XTAL LOAD CAPACITANCE

Bit	Name	Description	Type	Reset
7:0	xtal_load_cap[7:0]	Internal load capacitance of crystal circuit (0 pF to 21.75 pF with the resolution of 0.25 pF). XIN and XOUT have each capacitor connected to GND. Multiple bit combinations available between 8 capacitors. 8'b0000_0000: disable all xtal load capacitors 8'b0000_0001: enable capacitor 0.25 pF 8'b0000_0010: enable capacitor 0.5 pF 8'b0000_0100: enable capacitor 1 pF 8'b0000_1000: enable capacitor 2 pF 8'b0001_0000: enable capacitor 2 pF 8'b0010_0000: enable capacitor 4 pF 8'b0100_0000: enable capacitor 4 pF 8'b1000_0000: enable capacitor 8 pF	RW	40

TABLE 3-5: 0X03 XTALNR - XTAL NORMAL RUN

Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	0000000
0	xtal_normal_run	When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance--XO circuit is running only when it is needed. When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required.	RW	1

TABLE 3-6: 0X04 OUTLOWALL - OUTPUT LOW ALL

Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	0000000
0	out_low_all	OUTLOWALL affects OUTLOW0 and OUTLOW1 registers. 1'b0: Output0 to Output11 are according to their driver_type[n+1, n] values 1'b1: Output0 to Output11 will drive logic LOW. OTP value load to this bit and/or I^2C write to this bit in the SCM mode, will affect all the values at OUTLOW0 and OUTLOW1 registers. In other words, loading value of 1'b0 from OTP or writing it from I^2C, will cause all values in OUTLOW0 and OUTLOW1 registers to be 0's. Same thing for 1'b1. In SCM, the output_low values per output are controlled individually by accessing the bits in OUTLOW0 and OUTLOW1 registers. However, any subsequent write to this bit will affect the values in those registers (OUTLOW0 and OUTLOW1)	RW	0

TABLE 3-7: 0X05 INSEL - INPUT SELECT REGISTER

Bit	Name	Description	Type	Reset
7:2	Unused	Unused	R	000000
1:0	input_select[1:0]	Input reference clock selection. Proper external coupling and termination are required. 2'b00: differential input from IN0_p and IN0_n 2'b01: differential input from IN1_p and IN1_n 2'b10: fundamental XTAL mode with XIN and XOUT (Use internal crystal oscillator circuits) or XTAL overdrive mode (single-ended clock signal fed to XIN) 2'b11: XTAL bypass mode (single-ended clock signal with XIN and disabled internal crystal buffer circuit in the analog block)		00

TABLE 3-8: 0X07 DRVTYPE0 - OUTPUT TYPE SELECT (OUTPUTS 0 TO 3)

Bit	Name	Description	Type	Reset
7:6	driver_type[7:6]	Output driver type of differential OUT3. The same bit configuration with OUT0.	RW	11
5:4	driver_type[5:4]	Output driver type of differential OUT2. The same bit configuration with OUT0.	RW	11
3:2	driver_type[3:2]	Output driver type of differential OUT1. The same bit configuration with OUT0.	RW	11
1:0	driver_type[1:0]	Output driver type of differential OUT0. 2’b00: HCSL outputs 2’b01: LVDS outputs 2’b10: LVPECL outputs 2’b11: Outputs disabled	RW	11

TABLE 3-9: 0X08 DRVTYPE1 - OUTPUT TYPE SELECT (OUTPUTS 4 TO 7)

Bit	Name	Description	Type	Reset
7:6	driver_type[15:14]	Output driver type of differential OUT7. The same bit configuration with OUT0.	RW	11
5:4	driver_type[13:12]	Output driver type of differential OUT6. The same bit configuration with OUT0.	RW	11
3:2	driver_type[11:10]	Output driver type of differential OUT5. The same bit configuration with OUT0.	RW	11
1:0	driver_type[9:8]	Output driver type of differential OUT4. The same bit configuration with OUT0.	RW	11

TABLE 3-10: 0X09 DRVTYPE2 - OUTPUT TYPE SELECT (OUTPUTS 8 TO 11)

Bit	Name	Description	Type	Reset
7:6	driver_type[23:22]	Output driver type of differential OUT11. The same bit configuration with OUT0.	RW	11
5:4	driver_type[21:20]	Output driver type of differential OUT10. The same bit configuration with OUT0.	RW	11
3:2	driver_type[19:18]	Output driver type of differential OUT9. The same bit configuration with OUT0.	RW	11
1:0	driver_type[17:16]	Output driver type of differential OUT8. The same bit configuration with OUT0.	RW	11

TABLE 3-11: 0X0A OUTLOW0 - OUTPUT DRIVE LOW (OUTPUTS 0 TO 7)

Bit	Name	Description	Type	Reset
7	output_drive_low[7]	Output driver type of differential OUT7. The same bit configuration with OUT0.	RW	0
6	output_drive_low[6]	Output driver type of differential OUT6. The same bit configuration with OUT0.	RW	0
5	output_drive_low[5]	Output driver type of differential OUT5. The same bit configuration with OUT0.	RW	0
4	output_drive_low[4]	Output driver type of differential OUT4. The same bit configuration with OUT0.	RW	0
3	output_drive_low[3]	Output driver type of differential OUT3. The same bit configuration with OUT0.	RW	0
2	output_drive_low[2]	Output driver type of differential OUT2. The same bit configuration with OUT0.	RW	0
1	output_drive_low[1]	Output driver type of differential OUT1. The same bit configuration with OUT0.	RW	0
0	output_drive_low[0]	When this bit is set to 1, and when OUT0 is enabled, the OUT0_p will drive low and OUT0_n will drive high voltage levels for corresponding type of the output. For example, if output type for OUT0 is set to HCSL (driver_type = 2'b00), the OUT0_p will drive 0V and OUT0_n will drive 0.75V. When OUT0 is in high-Z mode (driver_type[1:0] = 2'b11), this bit is ignored and the output will stay high-Z. If this bit is set to 0, drive low function is disabled. **output_drive_low[0] driver_type[1:0] OUT0** 0 00 HCSL 0 01 LVDS 0 10 LVPECL 0 11 Hi-Z 1 00 HCSL_drive_low 1 01 LVDS_drive_low 1 10 LVPECL_drive_low 1 11 Hi-Z	RW	0

TABLE 3-12: 0X0B OUTLOW1 - OUTPUT DRIVE LOW (OUTPUTS 8 TO 11)

Bit	Name	Description	Type	Reset
7:4	Unused	Unused	R	0
3	output_drive_low[11]	Output driver type of differential OUT11. The same bit configuration with OUT0.		
2	output_drive_low[10]	Output driver type of differential OUT10. The same bit configuration with OUT0.		

TABLE 3-12: 0X0B OUTLOW1 - OUTPUT DRIVE LOW (OUTPUTS 8 TO 11) (CONTINUED)

Bit	Name	Description	Type	Reset
1	output_drive_low[9]	Output driver type of differential OUT9. The same bit configuration with OUT0.		
0	output_drive_low[8]	Output driver type of differential OUT8. The same bit configuration with OUT0.		

TABLE 3-13: 0X0C COMMODSEL - COMMON MODE SELECT

Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	0000000
0	vcm_sel	The bit determines the range of the input VCM 1'b0: the input VCM is from 1V to 2V 1'b1: the input VCM is from 0.1V to 0.8V (for HCSL format)	RW	1

TABLE 3-14: 0X0E DEVADDR - I²C BUS SLAVE DEVICE ADDRESS

Bit	Name	Description	Type	Reset
7:3	Unused	Unused	R	00000
2:0	dev_addr[2:0]	These three bits contributes as the following to the 7 bits of the I²C Bus slave address {2'b01, dev_addr[2:0],SA1,SA0}, where SA0 and SA1 are from pins IN_SEL0_I2C_SA_0 and IN_SEL0_I2C_SA_0 respectively.	RW	101

TABLE 3-15: 0X11 DEVID - DEVICE IDENTIFICATION

Bit	Name	Description	Type	Reset
7:5	Unused	Unused	R	000
4:0	dev_id	Device ID	RO	00011

4.0 ELECTRICAL CHARACTERISTICS

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS

Note 1, Note 2, Note 3

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	–0.5	+4.6	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	–0.5	+3.5	V
Storage Temperature Range	T_{ST}	–55	+125	°C

Note 1: Exceeding these values may cause permanent damage.
2: Functional operation under these conditions is not implied.
3: Voltages are with respect to ground (GND) unless otherwise stated.

TABLE 4-2: RECOMMENDED OPERATING CONDITIONS

Note 1, Note 2

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage 3.3V	V_{DD}/V_{DDO}	3.135	3.3	3.465	V
Supply Voltage 2.5V	V_{DD}/V_{DDO}	2.375	2.5	2.625	V
Operating Temperature	T_A	–40	+25	+85	°C
Input Voltage	$V_{DD\text{-}IN}$	–0.3	—	V_{DD} + 0.3	V

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.
2: The device core supports two power supply modes (3.3V and 2.5V).

TABLE 4-3: CURRENT CONSUMPTION

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Core Device Current (all outputs and XTAL disabled)	$I_{S\_3.3V}$	—	163	197	mA	V_{DD} = 3.3V+5%
	$I_{S\_2.5V}$	—	153	187	mA	V_{DD} = 2.5V+5%
Core Device Current (all outputs disabled) XTAL Circuit Enabled with 25 MHz Crystal Connected between XIN and XOUT	$I_{DD\_XTAL\_3.3V}$	—	128	154	mA	V_{DD} = 3.3V+5%
	$I_{DD\_XTAL\_2.5V}$	—	124	150	mA	V_{DD} = 2.5V+5%
Common Output Current	$I_{DD\_CM\_3.3V}$	—	17.9	18.9	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_CM\_2.5V}$	—	16.6	17.5	mA	V_{DDO} = 2.5V+5%
Current Dissipation per LVPECL Output	$I_{DD\_LVPECL\_3.3V}$	—	21.5	25.7	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_LVPECL\_2.5V}$	—	21.5	25.6	mA	V_{DDO} = 2.5V+5%
Current Dissipation per LVDS Output	$I_{DD\_LVDSL\_3.3V}$	—	6.73	8	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_LVDS\_2.5V}$	—	6.87	7.83	mA	V_{DDO} = 2.5V+5%
Current Dissipation per HCSL Output (IREF pin pulled down with 422Ω)	$I_{DD\_85HCSL\_3.3V}$	—	21	22.8	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_85HCSL\_2.5V}$	—	20	21.4	mA	V_{DDO} = 2.5V+5%
Current Dissipation per HCSL Output (IREF pin pulled down with 536Ω)	$I_{DD\_100HCSL\_3.3V}$	—	17.6	19.2	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_100HCSL\_2.5V}$	—	17	18.4	mA	V_{DDO} = 2.5V+5%

TABLE 4-4: INPUT CHARACTERISTICS

Note 1, Note 2, Note 3

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
CMOS High-Level Input Voltage for Control Inputs	V_{CIH}	1.05	—	—	V	—
CMOS Low-Level Input Voltage for Control Inputs	V_{CIL}	—	—	0.45	V	—
CMOS Input Leakage Current for Control Inputs (includes current due to pull down resistors)	I_{IL}	–25	—	50	µA	$V_I = V_{DD}$ or 0V
Differential Input Common Mode Voltage for IN0_p/n and IN1_p/n	V_{CM}	1	—	2	V	vcm_sel bit = 0 (reg 0x0C)
Differential Input Common Mode Voltage for IN0_p/n and IN1_p/n (HCSL common mode)	V_{CM}	0.1	—	0.8	V	vcm_sel bit = 1 (reg 0x0C)
Differential Input Voltage Swing for IN0_p/n and IN1_p/n; f < 1 GHz	V_{ID}	0.15	—	1.3	V	—
Differential Input Voltage Swing for IN0_p/n and IN1_p/n for 1 GHz < f < 1.5 GHz	V_{ID}	0.35	—	1.3	V	—
Differential Input Leakage Current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	–150	—	150	µA	V_I = 2V or 0V
Single-Ended Input Voltage for IN0_p and IN1_p	V_{SI}	–0.3	—	2.7	V	—
Single-Ended Input Common Mode Voltage (IN0_p and IN1_p)	V_{SIC}	1	—	2	V	vcm_sel bit = 0 (reg 0x0C)
Single-Ended Input Common Mode Voltage (IN0_p and IN1_p) (HCSL common mode)	V_{SIC}	0.1	—	0.8	V	vcm_sel bit = 1 (reg 0x0C)
Single-Ended Input Voltage Swing for IN0_p and IN1_p	V_{SID}	0.3	—	0.8	V	—
Input Frequency (differential)	f_{IN}	0	—	1500	MHz	—
Input Frequency (single-ended)	f_{IN_SE}	0	—	400	MHz	—
Input Duty Cycle	DC	35	—	65	%	—
Input Slew Rate	t_{SLEW}	—	2	—	V/ns	—
Input Pull-Up/Pull-Down Resistance for IN0_p/IN0_n and IN1_p/IN1_n	R_{PU}/R_{PD}	—	60	—	kΩ	—
Input Pull-Down Resistance for INx_p	R_{PD}	—	30	—	kΩ	—
Control Input (OE_b[11:0]) Pull-Down Resistance	R_{PDD}	—	300	—	kΩ	—
Input Multiplexer Isolation IN0_p/n to IN1_p/n and Vice-Versa. Power on Both Inputs 0 dBm, f_{OFFSET} > 50 kHz	I_{SO}	—	–90	—	dBc	f_{IN} = 100 MHz
		—	–75	—		f_{IN} = 200 MHz
		—	–61	—		f_{IN} = 400 MHz
		—	–52	—		f_{IN} = 800 MHz

Note 1: Values are over Recommended Operating Conditions.

2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

3: Input mux isolation is measured as amplitude of f_{OFFSET} spur in dBc on the output clock phase noise plot (1) low frequency only.

TABLE 4-5: CRYSTAL OSCILLATOR CHARACTERISTICS

Note 1, Note 2

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Mode of Oscillation	—	Fundamental				—
Frequency	f	8	—	160	MHz	—
On-Chip Load Capacitance in I²C Bus Controlled Mode	C_L	0	—	21.75	pF	Programmable
On-Chip Load Capacitance in Pin Controlled Mode	C_L	—	4	—	pF	Fixed
On-Chip Series Resistor in I²C Bus Controlled Mode	R_S	0	—	312	Ω	Programmable
On-Chip Series Resistor in Pin Controlled Mode	R_S	—	84	—	Ω	Fixed
On-Chip Shunt Resistor	R	—	500	—	kΩ	—
Frequency in Overdrive Mode (Note 3)	f_{OV}	0.1	—	250	MHz	Functional, but may not meet AC parameters. Minimum depends on AC coupling capacitor (0.1 µF assumed).
Frequency in Bypass Mode (Note 4)	f_{BP}	0	—	250	MHz	Functional, but may not meet AC parameters.

Note 1: Values are over Recommended Operating Conditions.
2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).
3: Maximum input level is 2V.
4: Maximum output level is V_{DD}.

TABLE 4-6: POWER SUPPLY REJECTION RATIO FOR $V_{DD} = V_{DDO}$ = 3.3V

Note 1, Note 2, Note 3

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
PSRR for LVPECL Output	$PSRR_{LVPECL}$	—	–79	—	dBc	f_{IN} = 156.25 MHz
		—	–81	—		f_{IN} = 312.5 MHz
		—	–84	—		f_{IN} = 625 MHz
PSRR for LVDS Output	$PSRR_{LVDS}$	—	–91	—	dBc	f_{IN} = 156.25 MHz
		—	–88	—		f_{IN} = 312.5 MHz
		—	–81	—		f_{IN} = 625 MHz
PSRR for HCSL Output	$PSRR_{HCSL}$	—	–95	—	dBc	f_{IN} = 100 MHz
		—	–93	—		f_{IN} = 133 MHz
		—	–84	—		f_{IN} = 400 MHz

Note 1: Values are over Recommended Operating Conditions.
2: Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mV_{PP}.
3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 4-7: POWER SUPPLY REJECTION RATIO FOR V_{DD} = V_{DDO} = 2.5V

Note 1, Note 2, Note 3

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
PSRR for LVPECL Output	$PSRR_{LVPECL}$	—	–82	—	dBC	f_{IN} = 156.25 MHz
		—	–71	—		f_{IN} = 312.5 MHz
		—	–68	—		f_{IN} = 625 MHz
PSRR for LVDS Output	$PSRR_{LVDS}$	—	–97	—	dBc	f_{IN} = 156.25 MHz
		—	–79	—		f_{IN} = 312.5 MHz
		—	–78	—		f_{IN} = 625 MHz
PSRR for HCSL Output	$PSRR_{HCSL}$	—	–89	—	dBc	f_{IN} = 100 MHz
		—	–94	—		f_{IN} = 133 MHz
		—	–82	—		f_{IN} = 400 MHz

Note 1: Values are over Recommended Operating Conditions.

2: Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mV_{PP}.

3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 4-8: LVPECL OUTPUT CHARACTERISTICS FOR V_{DDO} = 3.3V

Note 1

Characteristics	Symbol	Min	Typ.	Max.	Units	Notes
Output High Voltage	V_{LVPECL_OH}	1.9	2.08	2.5	V	DC Measurement
Output Low Voltage	V_{LVPECL_OL}	1.2	1.36	1.7	V	DC Measurement
Output Differential Swing (Note 2)	V_{LVPECL_SW}	0.6	0.72	0.9	V	DC Measurement
Variation of V_{LVPECL_SW} for Complementary Output States	ΔV_{LVPECL_SW}	0	0.02	0.07	V	—
Common Mode Output	V_{CM}	1.6	1.72	2.1	V	—
Output Frequency when $V_{LVPECL\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output Frequency when $V_{LVPECL\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1500	MHz	—
Rise or Fall Time (20% to 80%)	t_r, t_f	—	110	170	ps	—
Output Frequency	f_O	0	—	1500	MHz	—
Output-to-Output Skew	t_{OOSK}	—	—	40	ps	—
Device-to-Device Output Skew	t_{DOOSK}	—	—	120	ps	—
Input-to-Output Delay	t_{IOD}	0.8	1	1.2	ns	—
Output Enable Time	t_{EN}	—	—	5	cycles	—
Output Disable Time	t_{DIS}	—	—	5	cycles	—
Additive RMS Jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	63	81	fs	Input clock: 100 MHz
		—	41	56		Input clock: 156.25 MHz
		—	21	32		Input clock: 625 MHz
Additive RMS Jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	67	89	fs	Input clock: 100 MHz
		—	46	67		Input clock: 156.25 MHz
		—	27	46		Input clock: 625 MHz

TABLE 4-8: LVPECL OUTPUT CHARACTERISTICS FOR V_{DDO} = 3.3V (CONTINUED)

Note 1

Characteristics	Symbol	Min	Typ.	Max.	Units	Notes
Noise Floor	N_F	—	–163	–161	dBc/Hz	Input clock: 100 MHz
		—	–163	–161		Input clock: 156.25 MHz
		—	–158	–156		Input clock: 625 MHz

Note 1: Values are over Recommended Operating Conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} – V_{OL})$ sometimes used in some data sheets.

TABLE 4-9: LVPECL OUTPUT CHARACTERISTICS FOR V_{DDO} = 2.5V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output High Voltage	V_{LVPECL_OH}	1.1	1.28	1.7	V	DC Measurement
Output Low Voltage	V_{LVPECL_OL}	0.4	0.57	0.9	V	DC Measurement
Output Differential Swing (Note 2)	V_{LVPECL_SW}	0.6	0.71	1	V	DC Measurement
Variation of V_{LVPECL_SW} for Complementary Output States	ΔV_{LVPECL_SW}	0	0.02	0.05	V	—
Common Mode Output	V_{CM}	0.8	0.92	1.2	V	—
Output Frequency when $V_{LVPECL\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output Frequency when $V_{LVPECL\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1500	MHz	—
Rise or Fall Time (20% to 80%)	t_r, t_f	—	120	170	ps	—
Output Frequency	f_O	0	—	1500	MHz	—
Output-to-Output Skew	t_{OOSK}	—	—	40	ps	—
Device-to-Device Output Skew	t_{DOOSK}	—	—	120	ps	—
Input-to-Output Delay	t_{IOD}	0.8	1	1.2	ns	—
Output Enable Time	t_{EN}	—	—	5	cycles	—
Output Disable Time	t_{DIS}	—	—	5	cycles	—
Additive RMS Jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	60	77	fs	Input clock: 100 MHz
		—	40	55		Input clock: 156.25 MHz
		—	21	33		Input clock: 625 MHz
Additive RMS Jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	64	86	fs	Input clock: 100 MHz
		—	45	89		Input clock: 156.25 MHz
		—	27	47		Input clock: 625 MHz

TABLE 4-9: LVPECL OUTPUT CHARACTERISTICS FOR V_{DDO} = 2.5V (CONTINUED)

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Noise Floor	N_F	—	–164	–162	dBc/Hz	Input clock: 100 MHz
		—	–164	–161		Input clock: 156.25 MHz
		—	–158	–156		Input clock: 625 MHz

Note 1: Values are over Recommended Operating Conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} – V_{OL})$ sometimes used in some data sheets.

TABLE 4-10: LVDS OUTPUTS FOR V_{DDO} = 3.3V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output High Voltage	V_{LVDS_OH}	1.3	1.39	1.48	V	DC Measurement
Output Low Voltage	V_{LVDS_OL}	1.0	1.07	1.15	V	DC Measurement
Output Differential Swing (Note 2)	V_{LVDS_SW}	0.25	0.32	0.39	V	DC Measurement
Variation of V_{LVDS_SW} for Complementary Output States	ΔV_{LVDS_SW}	0	0.002	0.01	V	—
Common Mode Output	V_{CM}	1.15	1.23	1.3	V	—
Variation of VCM for Complementary Output States	ΔV_{CM}	0	0.001	0.01	V	—
Output Frequency when $V_{LVDS\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output Frequency when $V_{LVDS\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1500	MHz	—
Rise or Fall Time (20% to 80%)	t_r, t_f	—	110	170	ps	—
Output Frequency	f_O	0	—	1500	MHz	—
Output-to-Output Skew	t_{OOSK}	—	—	20	ps	—
Device-to-Device Output Skew	t_{DOOSK}	—	—	130	ps	—
Input-to-Output Delay	t_{IOD}	0.8	1	1.2	ns	—
Output Short Circuit Current Single-Ended	I_S	–24	—	24	mA	Single-ended outputs shorted to GND
Output Short Circuit Current Differential	I_{SD}	–24	—	24	mA	Complementary outputs shorted
Output Enable Time	t_{EN}	—	—	5	cycles	—
Output Disable Time	t_{DIS}	—	—	5	cycles	—
Additive RMS Jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	87	102	fs	Input clock: 100 MHz
		—	46	58		Input clock: 156.25 MHz
		—	21	32		Input clock: 625 MHz

TABLE 4-10: LVDS OUTPUTS FOR V_{DDO} = 3.3V (CONTINUED)

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Additive RMS Jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	91	108	fs	Input clock: 100 MHz
		—	51	69		Input clock: 156.25 MHz
		—	27	48		Input clock: 625 MHz
Noise Floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–162	–161		Input clock: 156.25 MHz
		—	–158	–156		Input clock: 625 MHz

Note 1: Values are over Recommended Operating Conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} - V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} - V_{OL})$ sometimes used in some data sheets.

TABLE 4-11: LVDS OUTPUTS FOR V_{DDO} = 2.5V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output High Voltage	V_{LVDS_OH}	1.3	1.4	1.5	V	DC Measurement
Output Low Voltage	V_{LVDS_OL}	0.97	1.05	1.13	V	DC Measurement
Output Differential Swing (Note 2)	V_{LVDS_SW}	0.25	0.35	0.44	V	DC Measurement
Variation of V_{LVDS_SW} for Complementary Output States	ΔV_{LVDS_SW}	0	0.001	0.01	V	—
Common Mode Output	V_{CM}	1.15	1.23	1.3	V	—
Variation of VCM for Complementary Output States	ΔV_{CM}	0	0.001	0.01	V	—
Output Frequency when $V_{LVDS\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output Frequency when $V_{LVDS\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1500	MHz	—
Rise or Fall Time (20% to 80%)	t_r, t_f	—	110	170	ps	—
Output Frequency	f_O	0	—	1500	MHz	—
Output-to-Output Skew	t_{OOSK}	—	—	20	ps	—
Device-to-Device Output Skew	t_{DOOSK}	—	—	130	ps	—
Input-to-Output Delay	t_{IOD}	0.8	1	1.2	ns	—
Output Short Circuit Current Single-Ended	I_S	–24	—	24	mA	Single-ended outputs shorted to GND
Output Short Circuit Current Differential	I_{SD}	–24	—	24	mA	Complementary outputs shorted
Output Enable Time	t_{EN}	—	—	3	cycles	—
Output Disable Time	t_{DIS}	—	—	3	cycles	—

TABLE 4-11: LVDS OUTPUTS FOR V_{DDO} = 2.5V (CONTINUED)

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Additive RMS Jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	81	100	fs	Input clock: 100 MHz
		—	44	58		Input clock: 156.25 MHz
		—	21	34		Input clock: 625 MHz
Additive RMS Jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	85	107	fs	Input clock: 100 MHz
		—	48	70		Input clock: 156.25 MHz
		—	27	50		Input clock: 625 MHz
Noise Floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–163	–161		Input clock: 156.25 MHz
		—	–158	–156		Input clock: 625 MHz

Note 1: Values are over Recommended Operating Conditions.

2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH} – V_{OL})$ used in some data sheets.

TABLE 4-12: HCSL OUTPUTS (PCIe ELECTRICAL CHARACTERISTICS) FOR V_{DDO} = 3.3V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Rising Edge Rate	Rise_Rate	1.4	1.75	4	V/ns	Note 3, Note 4
Falling Edge Rate	Fall_Rate	1.4	1.75	4	V/ns	Note 3, Note 4
Differential High Voltage	V_{IH}	0.6	—	—	V	Note 3
Differential Low Voltage	V_{IL}	—	—	–0.6	V	Note 3
Single-Ended High Voltage	V_{SIH}	0.65	0.75	0.85	V	DC Measurement
Single-Ended Low Voltage	V_{SIL}	–20	0	20	mV	DC Measurement
Absolute Crossing Voltage	V_{CROSS}	0.25	—	0.55	V	Note 2, Note 5, Note 6
Variation of V_{CROSS} over All Rising Clock Edges	ΔV_{CROSS}	—	—	0.140	V	Note 2, Note 5, Note 10
Ringback Voltage Margin	V_{RB}	–0.55	—	0.55	V	Note 3, Note 12
Time before V_{RB} is Allowed	t_{STABLE}	4.6	—	—	ns	Note 3, Note 12
Cycle-to-Cycle Additive Jitter	t_{JCC}	—	4.6	5.8	ps_{PP}	Note 3
Absolute Maximum Voltage	V_{MAX}	—	—	1.15	V	Note 2, Note 8
Absolute Minimum Voltage	V_{MIN}	–0.3	—	—	V	Note 2, Note 9
Output Duty Cycle (When Input has 50% of Duty Cycle)	ODC	48	50	52	%	Note 3
Rising to Falling Edge Matching	r/f match	—	—	20	%	Note 2, Note 13
Clock Source DC Impedance (CK)	$Z_{C\text{-}DC\_CK}$	—	50	—	Ω	DC Measurement, Note 2

TABLE 4-12: HCSL OUTPUTS (PCIe ELECTRICAL CHARACTERISTICS) FOR V_{DDO} = 3.3V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Clock Source DC Impedance (CK#)	$Z_{C\text{-}DC\_CK\#}$	—	50	—	Ω	DC Measurement, Note 2
Output Frequency	f_{OUT}	0	—	400	MHz	—
Output-to-Output Skew	t_{OOSK}	—	—	50	ps	—
Device-to-Device Output Skew	t_{DOOSK}	—	—	129	ps	—
Input-to-Output Delay	t_{IOD}	0.8	1	1.2	ps	—
Output Enable Time	t_{EN}	—	—	5	cycles	—
Output Disable Time	t_{DIS}	—	—	5	cycles	—

Note 1: Values are over Recommended Operating Conditions.

2: Measurement taken from single-ended waveform.

3: Measurement taken from differential waveform.

4: Measured from –150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 28.

5: Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK#. See Figure 25.

6: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 25.

7: This requirement, from PCI Express Base Specification, Revision 4.0 is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

8: Defined as the maximum instantaneous voltage including overshoot. See Figure 25.

9: Defined as the minimum instantaneous voltage including undershoot. See Figure 25.

10: Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 26.

11: The PPM requirement from PCI Express Base Specification, Revision 4.0 is related to clock generation devices. This requirement is not applicable to buffers because the buffer’s output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

12: t_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after 20 rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 29.

13: Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cross point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 27.

TABLE 4-13: HCSL (PCIe) JITTER PERFORMANCE FOR V_{DDO} = 3.3V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$t_{jPCIe\_1.0}$	—	99	122	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 High Band (1.5 MHz to 50 MHz)	$t_{jPCIe\_2.0\_high}$	—	98	120	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 Low Band (10 kHz to 1.5 MHz)	$t_{jPCIe\_2.0\_low}$	—	26	36	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 Mid Band (5 MHz to 16 MHz)	$t_{jPCIe\_2.0\_mid}$	—	77	94	fs_{RMS}	Input clock: 100 MHz

TABLE 4-13: HCSL (PCIe) JITTER PERFORMANCE FOR V_{DDO} = 3.3V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	24	30	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	24	30	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	10	12	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per Intel QPI 9.6 Gbps	t_{jQPI}	—	45	55	fs_{RMS}	Input clock: 100 MHz
Additive RMS Jitter in 1 MHz to 20 MHz Band	$t_{j\_1M\_20M}$	—	64	75	fs_{RMS}	Input clock: 100 MHz
		—	48	60		Input clock: 133 MHz
		—	26	33		Input clock: 400 MHz
Additive RMS Jitter in 12 kHz to 20 MHz Band	$t_{j\_12k\_20M}$	—	68	83	fs_{RMS}	Input clock: 100 MHz
		—	52	66		Input clock: 133 MHz
		—	31	43		Input clock: 400 MHz
Noise Floor	NF	—	–163	–161	dBc/Hz	Input clock: 100 MHz
		—	–164	–162		Input clock: 133 MHz
		—	–160	–158		Input clock: 400 MHz

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-14: HCSL OUTPUTS (PCIe ELECTRICAL CHARACTERISTICS) FOR V_{DDO} = 2.5V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Rising Edge Rate	Rise_Rate	1.4	1.75	4	V/ns	Note 3, Note 4
Falling Edge Rate	Fall_Rate	1.4	1.75	4	V/ns	Note 3, Note 4
Differential High Voltage	V_{IH}	0.6	—	—	V	Note 3
Differential Low Voltage	V_{IL}	—	—	–0.6	V	Note 3
Single-Ended High Voltage	V_{SIH}	0.65	0.75	0.85	V	DC Measurement
Single-Ended Low Voltage	V_{SIL}	–20	0	20	mV	DC Measurement
Absolute Crossing Voltage	V_{CROSS}	0.25	—	0.55	V	Note 2, Note 5, Note 6
Variation of V_{CROSS} over All Rising Clock Edges	ΔV_{CROSS}	—	—	0.140	V	Note 2, Note 5, Note 10
Ringback Voltage Margin	V_{RB}	–0.55	—	0.55	V	Note 3, Note 12
Time before V_{RB} is Allowed	t_{STABLE}	4.6	—	—	ns	Note 3, Note 12
Cycle-to-Cycle Additive Jitter	t_{JCC}	—	4.6	5.8	ps_{PP}	Note 3

TABLE 4-14: HCSL OUTPUTS (PCIe ELECTRICAL CHARACTERISTICS) FOR V_{DDO} = 2.5V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Absolute Maximum Voltage	V_{MAX}	—	—	1.15	V	Note 2, Note 8
Absolute Minimum Voltage	V_{MIN}	–0.3	—	—	V	Note 2, Note 9
Output Duty Cycle (When Input has 50% of Duty Cycle)	ODC	48	50	52	%	Note 3
Rising to Falling Edge Matching	r/f match	—	—	20	%	Note 2, Note 13
Clock Source DC Impedance (CK)	$Z_{C\text{-}DC\_CK}$	—	50	—	Ω	DC Measurement, Note 2
Clock Source DC Impedance (CK#)	$Z_{C\text{-}DC\_CK\#}$	—	50	—	Ω	DC Measurement, Note 2
Output Frequency	f_{OUT}	0	—	400	MHz	—
Output-to-Output Skew	t_{OOSK}	—	—	50	ps	—
Device-to-Device Output Skew	t_{DOOSK}	—	—	129	ps	—
Input-to-Output Delay	t_{IOD}	0.8	1	1.2	ps	—
Output Enable Time	t_{EN}	—	—	5	cycles	—
Output Disable Time	t_{DIS}	—	—	5	cycles	—

Note 1: Values are over Recommended Operating Conditions.

2: Measurement taken from single-ended waveform.

3: Measurement taken from differential waveform.

4: Measured from –150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 28.

5: Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK#. See Figure 25.

6: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 25.

7: This requirement, from PCI Express Base Specification, Revision 4.0 is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

8: Defined as the maximum instantaneous voltage including overshoot. See Figure 25.

9: Defined as the minimum instantaneous voltage including undershoot. See Figure 25.

10: Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 26.

11: The PPM requirement from PCI Express Base Specification, Revision 4.0 is related to clock generation devices. This requirement is not applicable to buffers because the buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

12: t_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after 20 rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 29.

13: Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cross point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 27.

TABLE 4-15: HCSL (PCIe) JITTER PERFORMANCE FOR V_{DDO} = 2.5V

Note 1

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$t_{jPCIe\_1.0}$	—	86	110	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 High Band (1.5 MHz to 50 MHz)	$t_{jPCIe\_2.0\_high}$	—	85	108	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 Low Band (10 kHz to 1.5 MHz)	$t_{jPCIe\_2.0\_low}$	—	23	38	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 Mid Band (5 MHz to 16 MHz)	$t_{jPCIe\_2.0\_mid}$	—	67	85	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	21	27	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	21	27	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	8	11	fs_{RMS}	Input clock: 100 MHz
Additive Jitter as per Intel QPI 9.6 Gbps	t_{jQPI}	—	40	50	fs_{RMS}	Input clock: 100 MHz
Additive RMS Jitter in 1 MHz to 20 MHz Band	$t_{j\_1M\_20M}$	—	56	70	fs_{RMS}	Input clock: 100 MHz
		—	45	58		Input clock: 133 MHz
		—	25	34		Input clock: 400 MHz
Additive RMS Jitter in 12 kHz to 20 MHz Band	$t_{j\_12k\_20M}$	—	60	77	fs_{RMS}	Input clock: 100 MHz
		—	49	65		Input clock: 133 MHz
		—	30	45		Input clock: 400 MHz
Noise Floor	NF	—	–164	–161	dBc/Hz	Input clock: 100 MHz
		—	–164	–162		Input clock: 133 MHz
		—	–160	–158		Input clock: 400 MHz

Note 1: Values are over Recommended Operating Conditions.

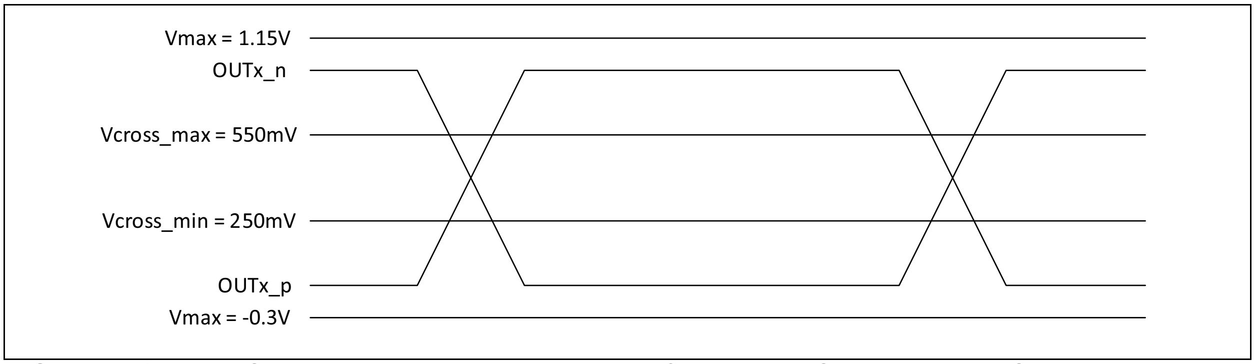


FIGURE 4-1: *Single-Ended Measurement Points for Absolute Cross Point and Swing.*

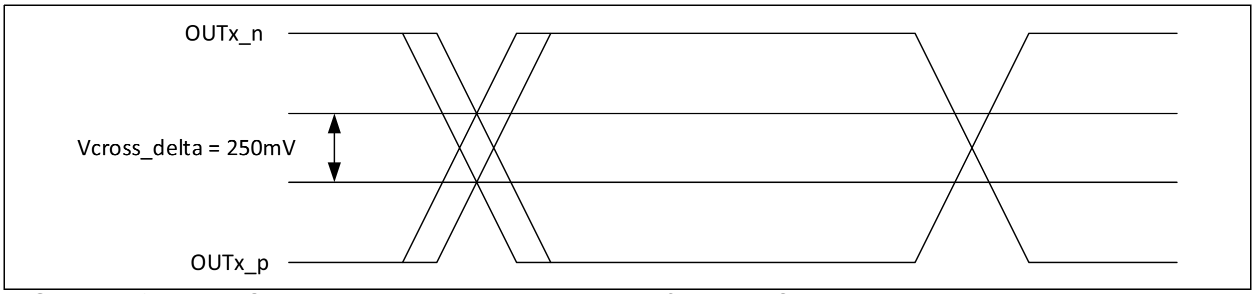


FIGURE 4-2: *Single-Ended Measurement Points for Delta Cross Point.*

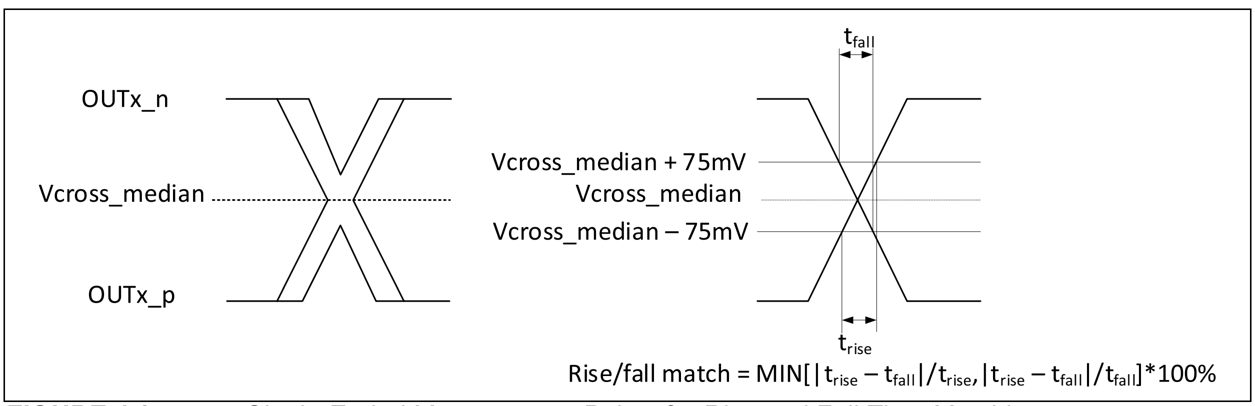


FIGURE 4-3: *Single-Ended Measurement Points for Rise and Fall Time Matching.*

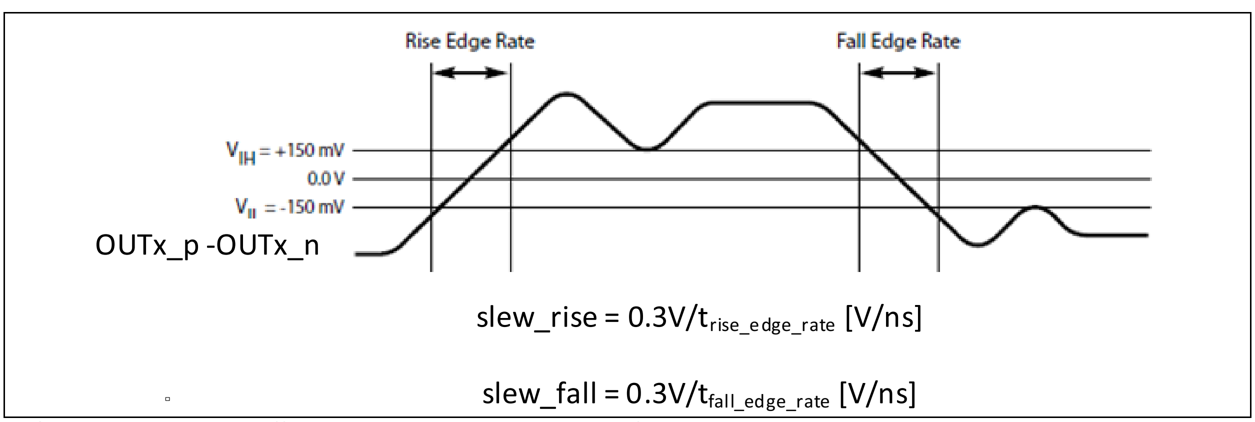


FIGURE 4-4: *Differential Measurement Points for Rise and Fall Time.*

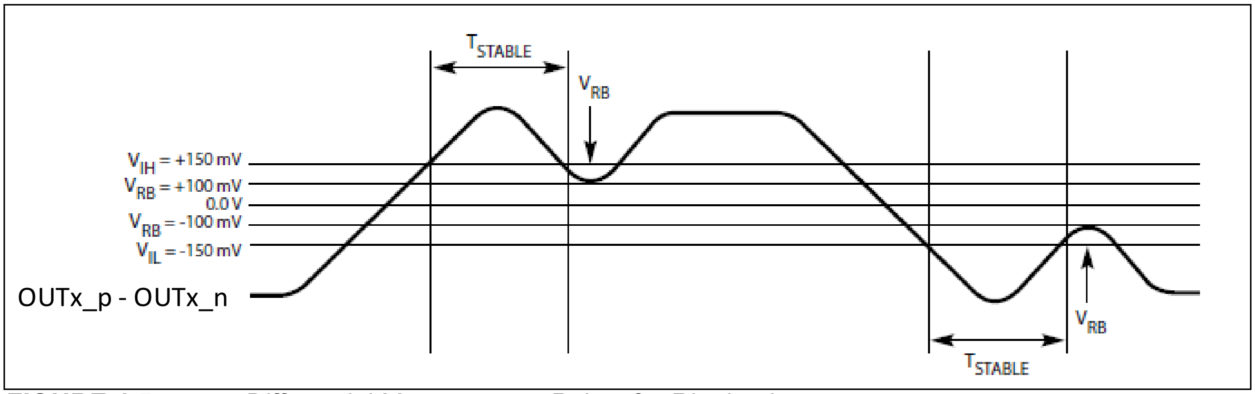


FIGURE 4-5: *Differential Measurement Points for Ringback.*

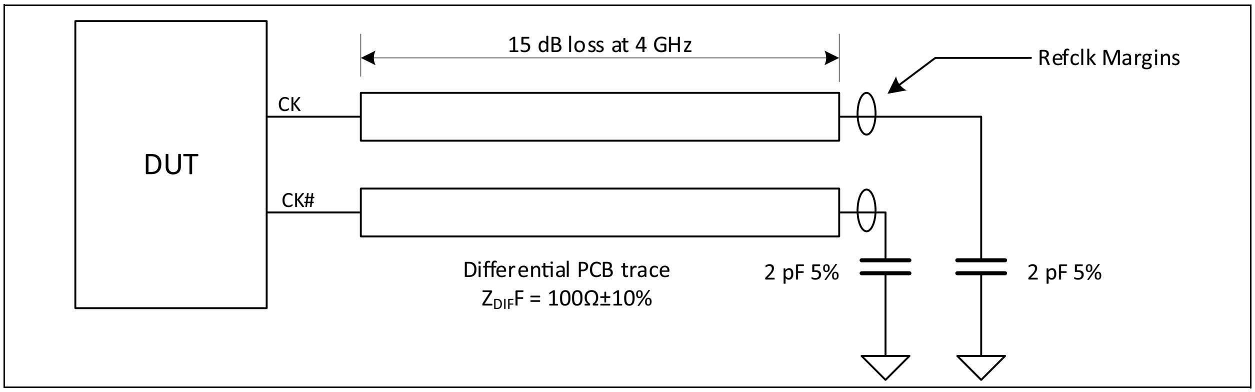


FIGURE 4-6: *PCIe Test Circuit.*

TABLE 4-16: LVPECL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	265	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	213	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–102	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–127	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–153	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–158	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–158	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–158	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–96	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–122	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–151	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-17: LVDS OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	172	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	177	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–102	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–126	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–153	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–160	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–161	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–160	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–96	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–123	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–152	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–161	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–161	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-18: HCSL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	235	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	143	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–102	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–126	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–153	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–158	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–159	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–158	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–97	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–123	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–153	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–162	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–162	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-19: LVPECL OUTPUT PHASE NOISE WITH 125 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	62	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	67	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–95	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–124	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–144	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–155	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–161	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–161	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@10 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–164	—	dBc/Hz	@20 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–95	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–125	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–143	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–154	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–162	—	dBc/Hz	@10 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@20 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-20: LVDS OUTPUT PHASE NOISE WITH 125 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	74	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	75	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–93	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–124	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–145	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–155	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–159	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–159	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–161	—	dBc/Hz	@10 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–162	—	dBc/Hz	@20 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–95	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–124	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–144	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–155	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–159	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–159	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–161	—	dBc/Hz	@10 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–161	—	dBc/Hz	@20 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-21: HCSL OUTPUT PHASE NOISE WITH 125 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	60	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	63	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–93	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–125	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–145	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–156	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–161	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–160	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@10 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@20 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–94	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–124	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–144	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–156	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–161	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@10 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@20 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-22: LVPECL OUTPUT PHASE NOISE WITH 156.25 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	49	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	53	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–86	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–117	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–141	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–153	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–160	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@10 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–164	—	dBc/Hz	@20 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–85	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–119	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–142	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–154	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–162	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@10 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@20 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-23: LVDS OUTPUT PHASE NOISE WITH 156.25 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	53	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	55	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–85	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–118	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–143	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–154	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–160	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–162	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@10 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@20 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–87	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–119	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–142	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–154	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–159	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–162	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–162	—	dBc/Hz	@10 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–162	—	dBc/Hz	@20 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-24: HCSL OUTPUT PHASE NOISE WITH 156.25 MHZ XTAL

Note 1

Characteristics	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 5 MHz Band	—	48	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	50	—	fs	V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise Floor	—	–85	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–117	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–143	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–155	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–161	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–163	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–164	—	dBc/Hz	@10 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–164	—	dBc/Hz	@20 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
	—	–86	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–119	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–142	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–154	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–160	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@10 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V
	—	–163	—	dBc/Hz	@20 MHz, V_{DD} = 2.5V, V_{DDO} = 2.5V

Note 1: Values are over Recommended Operating Conditions.

TABLE 4-25: I^2C BUS ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Nominal Bus Voltage	VDD_{I2C}	2.375	—	5.5	V	Note 1
Input Low Voltage	V_{IL}	—	—	0.7	V	—
Input High Voltage	V_{IH}	1.5	—	VDD_{I2C}	V	—
Output Low Voltage	V_{OL}	—	—	0.4	V	At $I_{PULLUP(MAX)}$
Input Leakage Current	I_{LEAK}	—	—	±10	µA	—
Current Sinking at $V_{OL(MAX)}$	I_{PULLUP}	4	—	—	mA	—
Pin Capacitive Load	C_L	—	—	1	pF	—
Signal Noise Immunity from 10 MHz to 100 MHz	V_{NOISE}	300	—	—	mV_{PP}	—
Noise Spike Suppression Time	t_{SPIKE}	0	—	50	ns	Note 3
I^2C Bus Operating Frequency	f_{OC}	0	—	400	kHz	—
Bus Free Time between Start and Stop Conditions	t_{BUF}	1.3	—	—	µs	—
Hold Time after (Repeated) Start Condition	$t_{HD:STA}$	0.6	—	—	µs	After this period, the first clock is generated
Repeated Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	µs	—
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	0	—	0.9	µs	Note 4
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	—
Detect Clock Low Timeout	$t_{TIMEOUT}$	25	—	35	ms	—
Clock Low Period	t_{LOW}	1.3	—	—	µs	—
Clock High Period	t_{HIGH}	0.6	—	—	µs	—
Clock/Data Fall Time	t_F	20 + 0.1*Cb	—	250	ns	Note 2
Clock /Data Rise Time	t_R	20 + 0.1*Cb	—	250	ns	Note 2

Note 1: 3V to 5V ±10%

2: Rise and fall time is defined as follows: $t_R = (V_{IL(MAX)} – 0.15)$ to $(V_{IH(MIN)} + 0.15)$; $t_F = (V_{IH(MIN)} – 0.15)$ to $(V_{IL(MAX)} + 0.15)$

3: Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

4: The maximum hold time has to be less than the maximum data valid or data valid acknowledge time as per Table 10, note [4] of I^2C bus Rev. 6 specification.

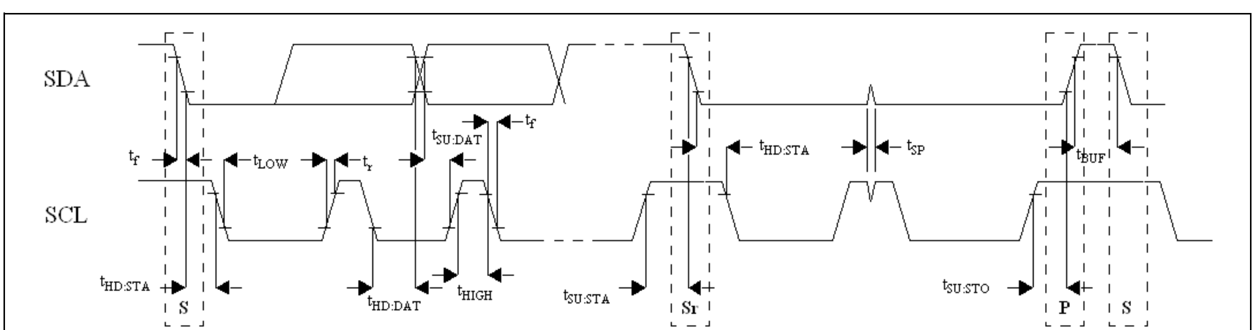


FIGURE 4-7: I^2C Bus Timing.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Ambient Temperature	$T_{A(MAX)}$	—	—	+85	°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	—
Package Thermal Resistance, 8x8 QFN-56Ld						
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	—	19.5	—	°C/W	Still-air
		—	15.7	—	°C/W	1 m/s airflow
		—	13.9	—	°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance	θ_{JB}	—	6.3	—	°C/W	—
Junction to Case Thermal Resistance	θ_{JC}	—	11	—	°C/W	—
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	—	3.6	—	°C/W	Still-air
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	—	0.2	—	°C/W	Still-air

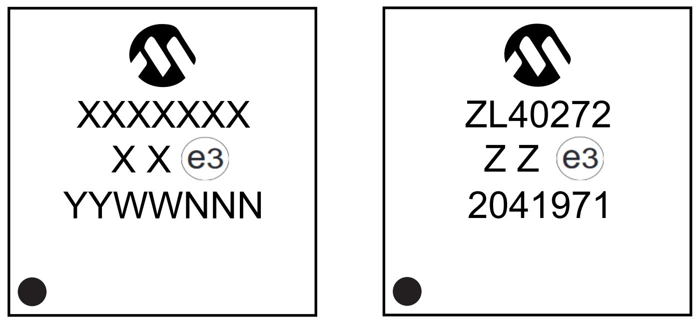
Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 8-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

5.0 PACKAGE OUTLINE

5.1 Package Marking Information

56-Lead QFN*   Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

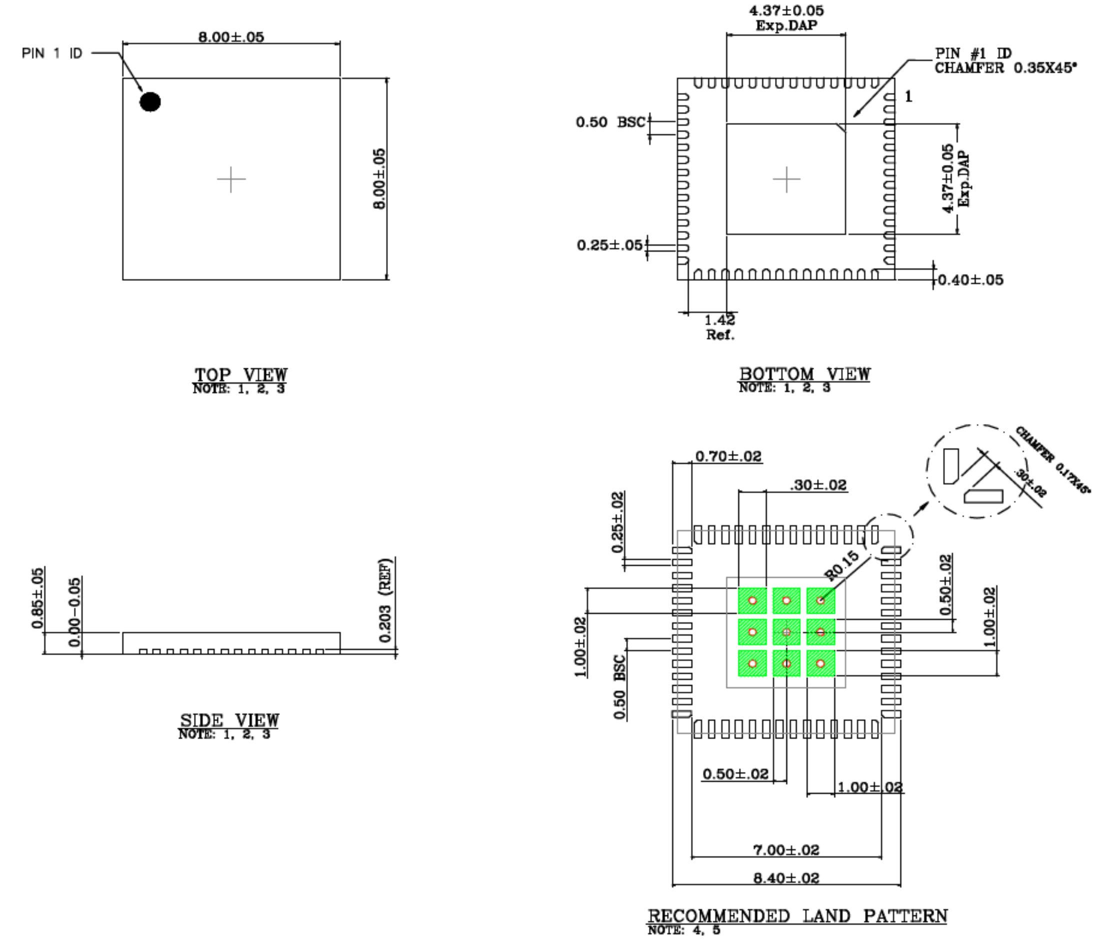
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

56-Lead 8 mm x 8 mm QFN Package Outline and Recommended Land Pattern

TITLE
56 LEAD QFN 8.0x8.0mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN88-56LD-PL-1	**UNIT**	MM
Lead Frame Type	AgCu	**Lead Finish**	Matte Tin



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARK.
4. RED CIRCLES IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. PITCH IS 1.25mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.0x1.0mm, SPACING IS 0.25mm.

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006408A (09-09-20)	—	Converted Microsemi data sheet ZL40272 to Microchip DS20006408A. Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL40272: Low-Skew, Low Additive Jitter, 12 Output HCSL/ LVDS/LVPECL Fanout Buffer with Per-Output Enable Control
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 56-Lead 8 mm x 8 mm QFN
Media Type:	G = 260/Tray F = 2,700/Reel
Finish:	1 = Pb Free with Matte Sn lead finish, RoHS e3 Compliant

Examples:

a) ZL40272LDG1:
Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control, Leadless Chip Carrier, 56-Lead QFN, 260/Tray, Pb Free with Matte Sn lead finish, RoHS e3 Compliant

b) ZL40272LDF1:
Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control, Leadless Chip Carrier, 56-Lead QFN, 2,700/Reel, Pb Free with Matte Sn lead finish, RoHS e3 Compliant

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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