ZL40264

Four Output Ultra-Low Additive Phase Noise PCIe, Gen 1 to 6, and UPI/QPI Fanout Buffer

Features

- One Differential Input which Accepts Any Differential Format
- Four Differential HCSL Outputs
- Ultra-Low Additive Jitter: 33 fs (in 12 kHz to 20 MHz Integration Band at 491.52 MHz Clock Frequency)
- Supports Clock Frequencies from 0 MHz to 600 MHz
- Supports 2.5V or 3.3V Power Supplies for HCSL Outputs
- Embedded Low Drop Out (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output to Output Skew of 50 ps
- Individual Output Enable Pin for Each Differential Pair
- Transfers Spread-Spectrum without Attenuation

Applications

- PCI Express Generation 1/2/3/4/5/6 Clock Distribution
- UPI/QPI Clock Distribution
- Low Jitter Clock Trees
- Logic Translation
- Clock and Data Signal Restoration
- High-Performance Microprocessor Clock Distribution
- Test Equipment

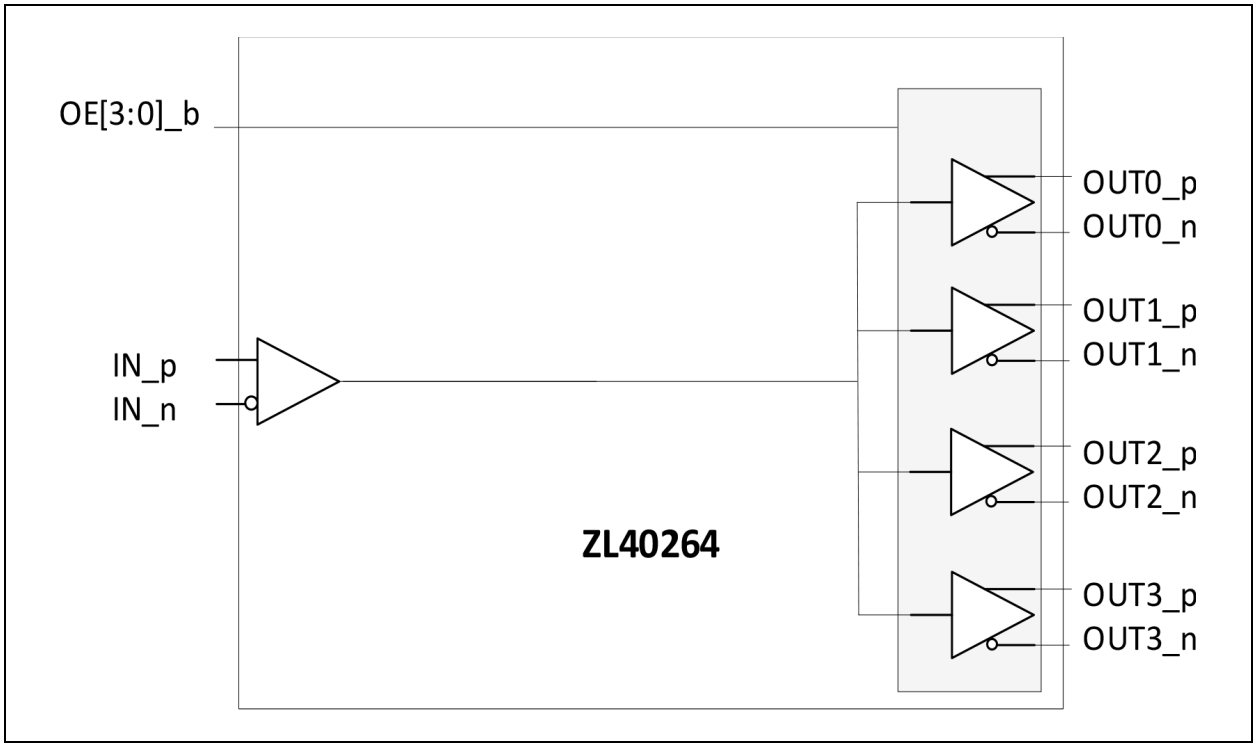

FIGURE 0-1: *Functional Block Diagram.*

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TABLE OF CONTENTS

List of Figures

List of Tables

1.0 PIN DESCRIPTION AND CONFIGURATION

The device is packaged in a 4 mm × 4 mm 20-lead VQFN with 2.125 mm exposed pad.

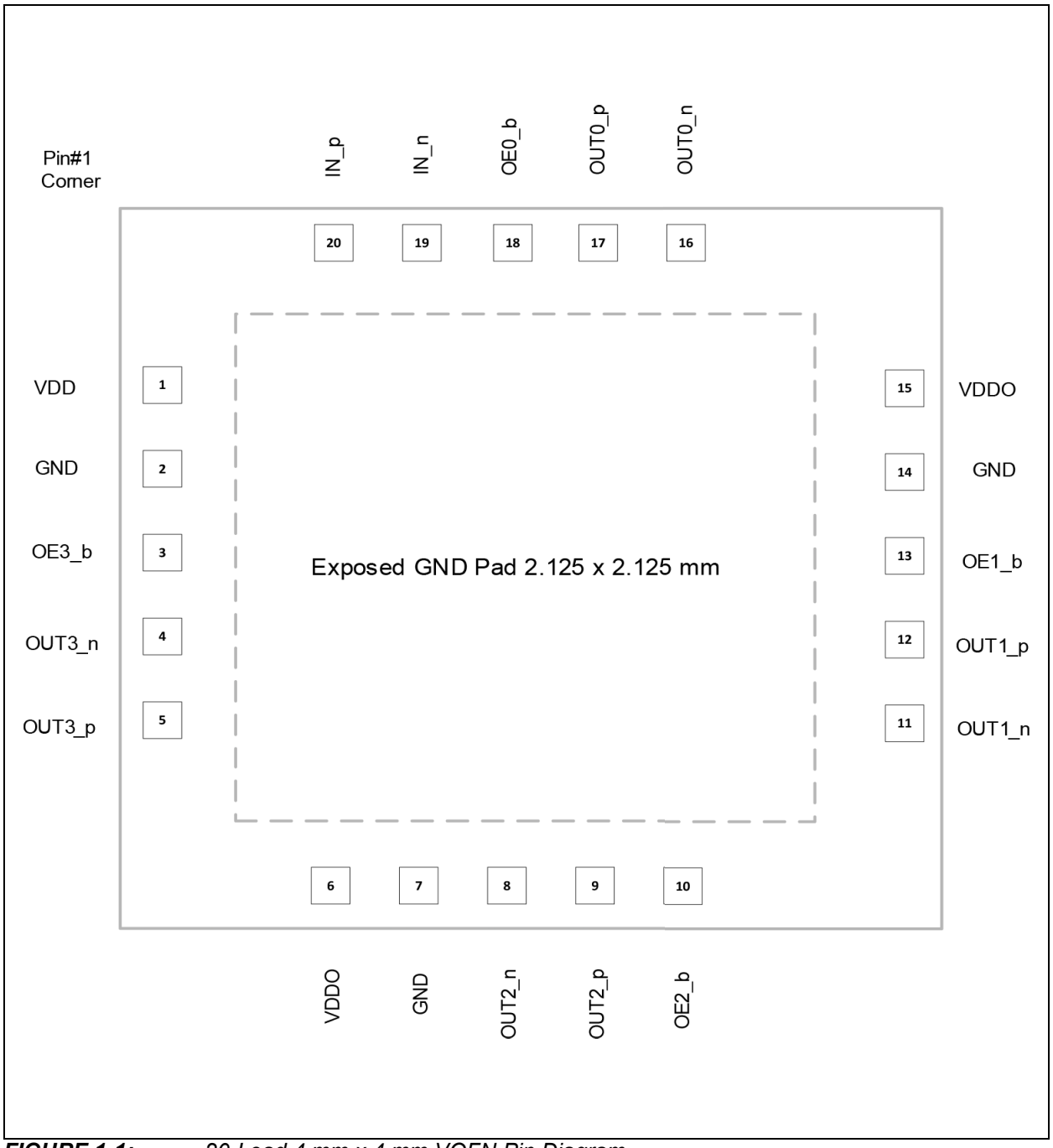


FIGURE 1-1: *20-Lead 4 mm x 4 mm VQFN Pin Diagram.*

1.1 Pin Descriptions

All device inputs and outputs are HCSL unless described otherwise.

The I/O column uses the following symbols: I – input, IPU – input with 300 kΩ internal pull-up resistor, I_{PD} – input with 300 kΩ internal pull-down resistor, I_{APU} – input with 31 kΩ internal pull-up resistor, I_{APD} – input with 30 kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased to VDD/2 with 60 kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC – No connect pin, P – power supply pin.

TABLE 1-1: PIN DESCRIPTION

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td colspan="5">Input Reference</td></tr>
<tr><td>20</td><td>IN0_p</td><td rowspan="2">I_{APD}
$I_{APU/APD}$</td><td colspan="2" rowspan="2">Input Differential or Single Ended Reference

Input frequency range 0 Hz to 600 MHz.

Non-inverting inputs (_p) are pulled down with internal 30 kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60 kΩ internal resistors (30 kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).</td></tr>
<tr><td>19</td><td>IN0_n</td></tr>
<tr><td colspan="5">Output Clocks</td></tr>
<tr><td>17</td><td>OUT0_p</td><td rowspan="8">O</td><td colspan="2" rowspan="8">Ultra-Low Additive Jitter Differential HCSL Outputs 0 to 1

Output frequency range 0 MHz to 600 MHz.</td></tr>
<tr><td>16</td><td>OUT0_n</td></tr>
<tr><td>12</td><td>OUT1_p</td></tr>
<tr><td>11</td><td>OUT1_n</td></tr>
<tr><td>9</td><td>OUT2_p</td></tr>
<tr><td>8</td><td>OUT2_n</td></tr>
<tr><td>5</td><td>OUT3_p</td></tr>
<tr><td>4</td><td>OUT3_n</td></tr>
<tr><td colspan="5">Control</td></tr>
<tr><td>18</td><td>OE0_b</td><td rowspan="5">I_{PD}</td><td colspan="2" rowspan="2">Output Enable. Logic level on these pins enables/disables corresponding outputs.</td></tr>
<tr><td>13</td><td>OE1_b</td></tr>
<tr><td rowspan="2">10</td><td rowspan="2">OE2_b</td><td>OEn_b</td><td>OUTn_p/n</td></tr>
<tr><td>0</td><td>Active</td></tr>
<tr><td>3</td><td>OE3_b</td><td>1</td><td>High-Z (outputs p/n will be low/low because of 50 Ω shunt resistors—see recommended output termination)</td></tr>
<tr><td colspan="5">Power and Ground</td></tr>
<tr><td>1</td><td>VDD</td><td>P</td><td colspan="2">Positive Supply Voltage. Connect to 3.3V or 2.5V supply.</td></tr>
<tr><td>6</td><td rowspan="2">VDDO</td><td rowspan="2">P</td><td colspan="2" rowspan="2">Positive Supply Voltage for Differential Outputs. Connect 3.3V or 2.5V power supply. VDDO does not have to be connected to the same voltage level as VDD.</td></tr>
<tr><td>15</td></tr>
<tr><td>2</td><td rowspan="4">GND</td><td rowspan="4">P</td><td colspan="2" rowspan="4">Ground. Connect to the ground.</td></tr>
<tr><td>7</td></tr>
<tr><td>14</td></tr>
<tr><td>E-Pad</td></tr>
</table>

NOTES:

2.0 FUNCTIONAL DESCRIPTION

The ZL40264 is an ultra-low additive jitter, low power 1 to 4 HCSL fanout buffer.

The device operates from 2.5V±5% or 3.3V±5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

2.1 Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40264 inputs.
Figure 2-1 and Figure 2-2 show how to terminate the input when driven from an HCSL driver.
The input buffer in ZL40264 in a native HCSL receiver so other differential formats need to be AC coupled as shown in Figure 2-3 and Figure 2-4 for LVPECL and LVDS signals respectively.

The resistors R1, R2, R3, and R4 in Figure 2-3 are used for biasing, termination and hysteresis. The resistor pairs (R1, R2) and (R3, R4) are different to add 20 mV to 30 mV of hysteresis. The hysteresis prevents the device from generating random transitions when input is not driven. If the input is driven all the time with a clock, then pairs (R1, R2) and (R2, R4) can be identical. That is, R3 = R1 and R4 = R2.

The resistors R1, R2, R3, and R4 in Figure 2-4 are used for biasing and hysteresis. Same as above, the hysteresis prevents the device from generating random transitions when input is not driven. If the input is driven all the time with a clock, then pairs (R1, R2) and (R2, R4) can be identical. That is, R3 = R1 and R4 = R2. The 100Ω termination resistor is placed before AC coupling capacitors, because some LVDS drivers need a DC path between p and n outputs. If the LVDS driver does not need the DC path, the 100Ω resistor can be placed after the AC coupling capacitors.

Figure 2-5 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and R_O + R_S should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance.

If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 3-4). The source resistors of R_S = 270Ω could be used for standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) × (1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance, both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

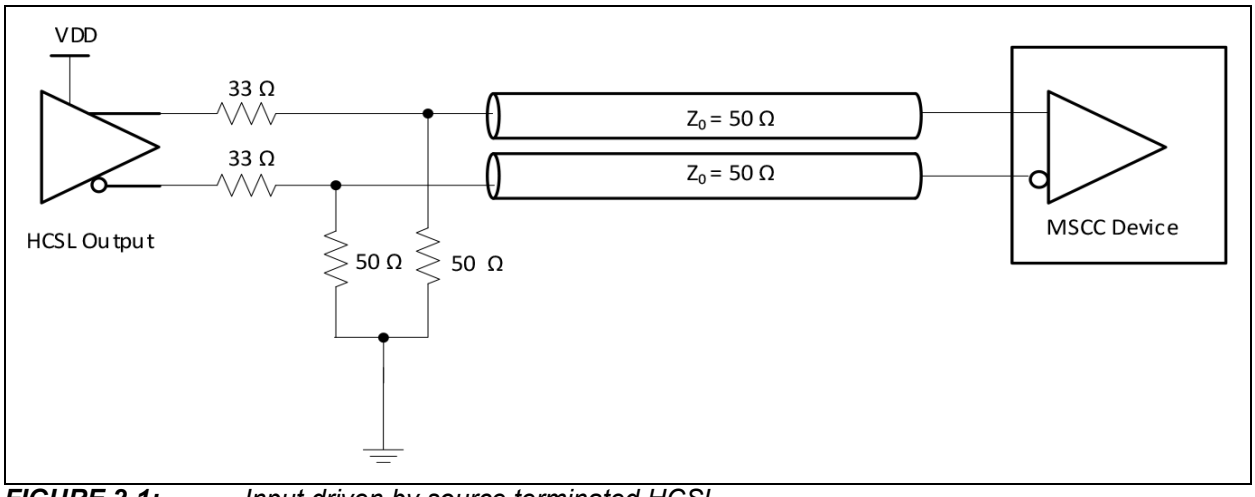


FIGURE 2-1: *Input driven by source terminated HCSL.*

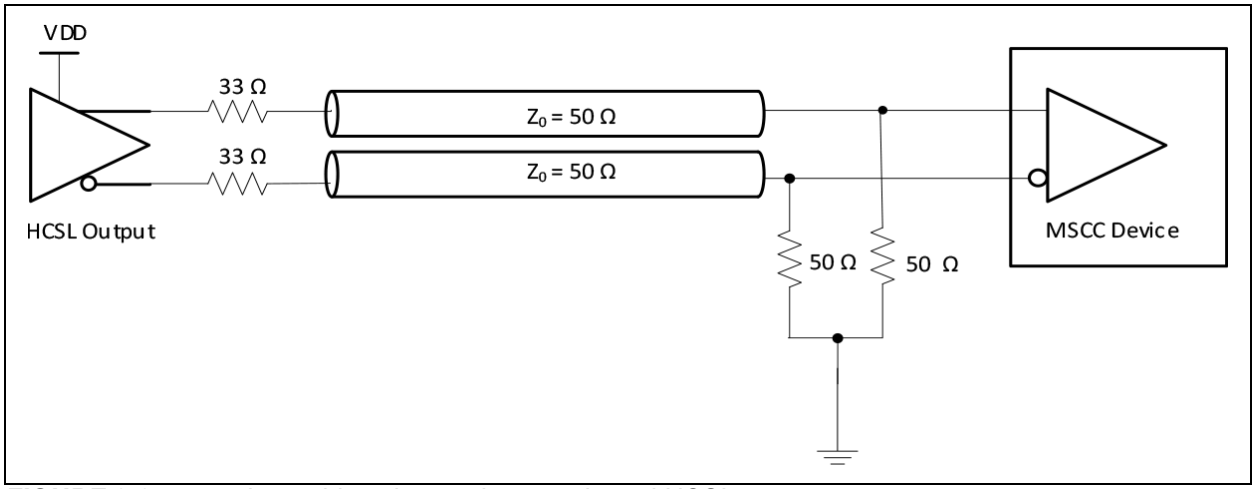


FIGURE 2-2: *Input driven by receiver terminated HCSL.*

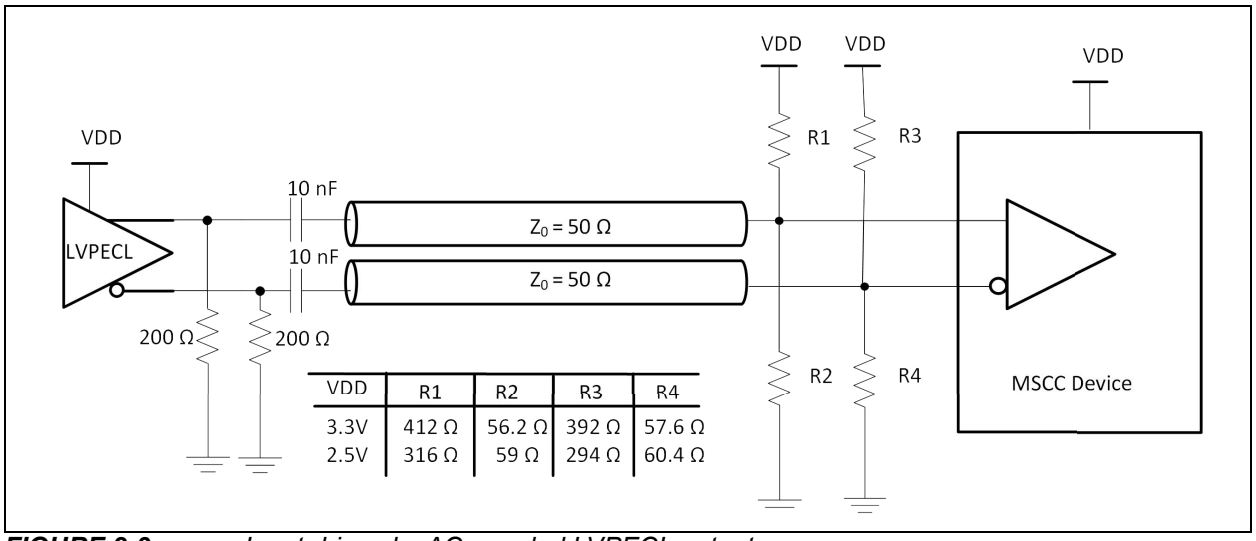


FIGURE 2-3: *Input driven by AC-coupled LVPECL output.*

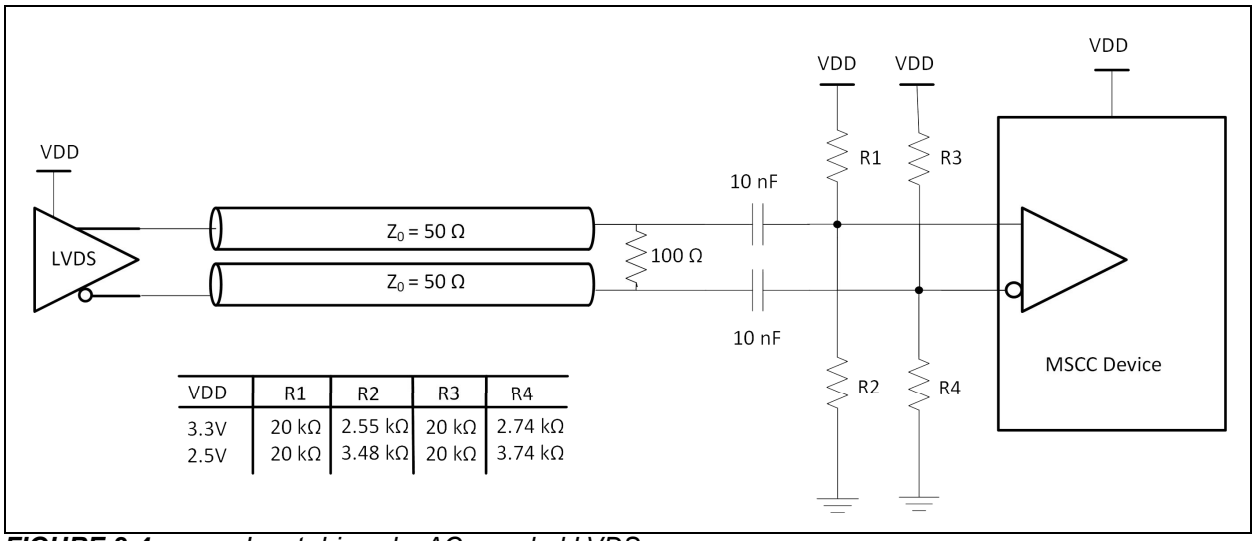


FIGURE 2-4: *Input driven by AC-coupled LVDS.*

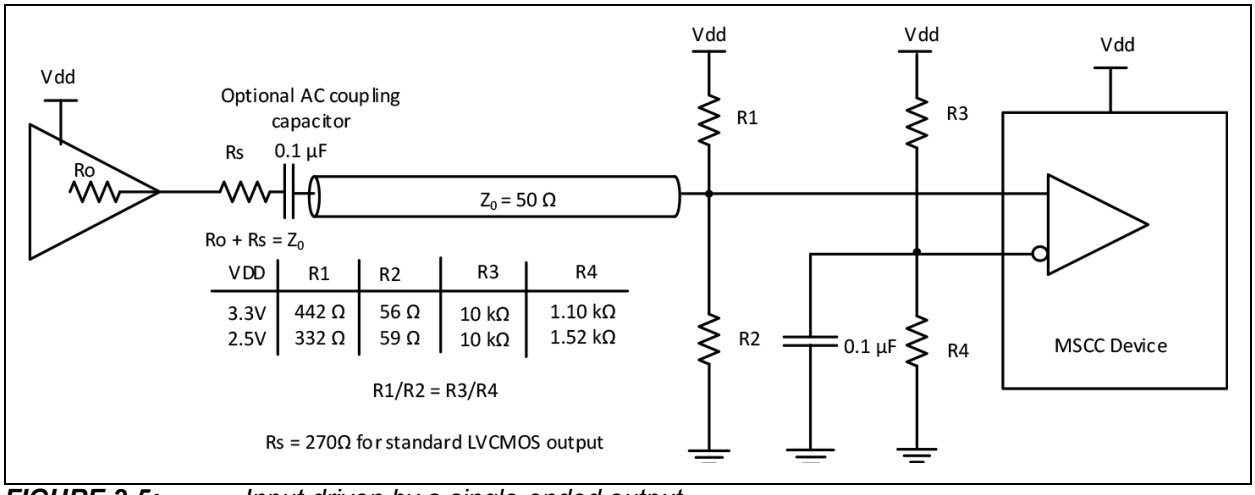


FIGURE 2-5: *Input driven by a single-ended output.*

2.2 Clock Outputs

Differential HCSL outputs should be terminated as shown in Figure 2-6 or Figure 2-7.

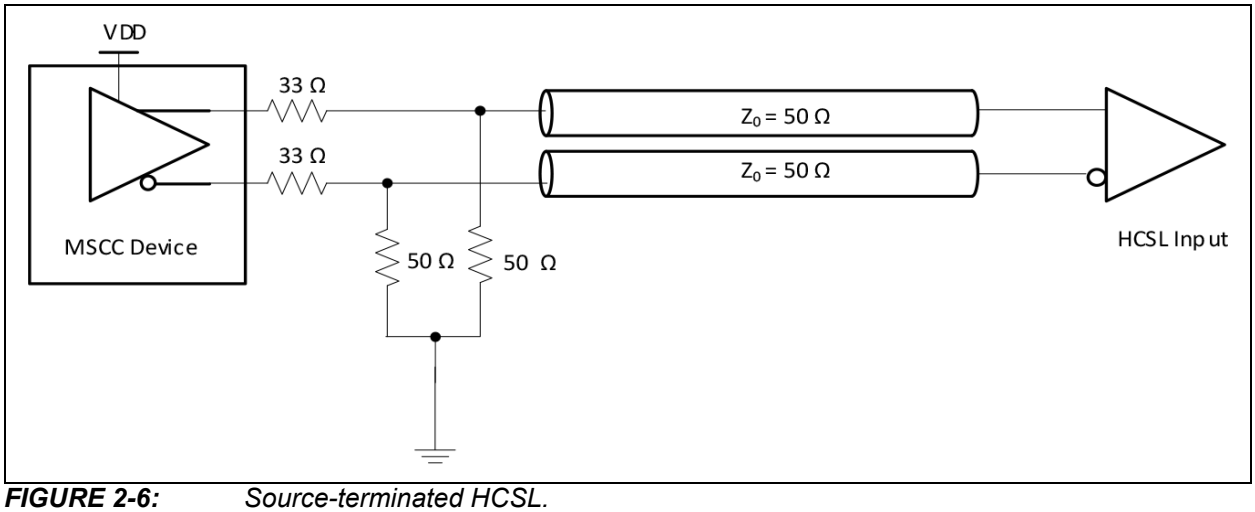


FIGURE 2-6: *Source-terminated HCSL.*

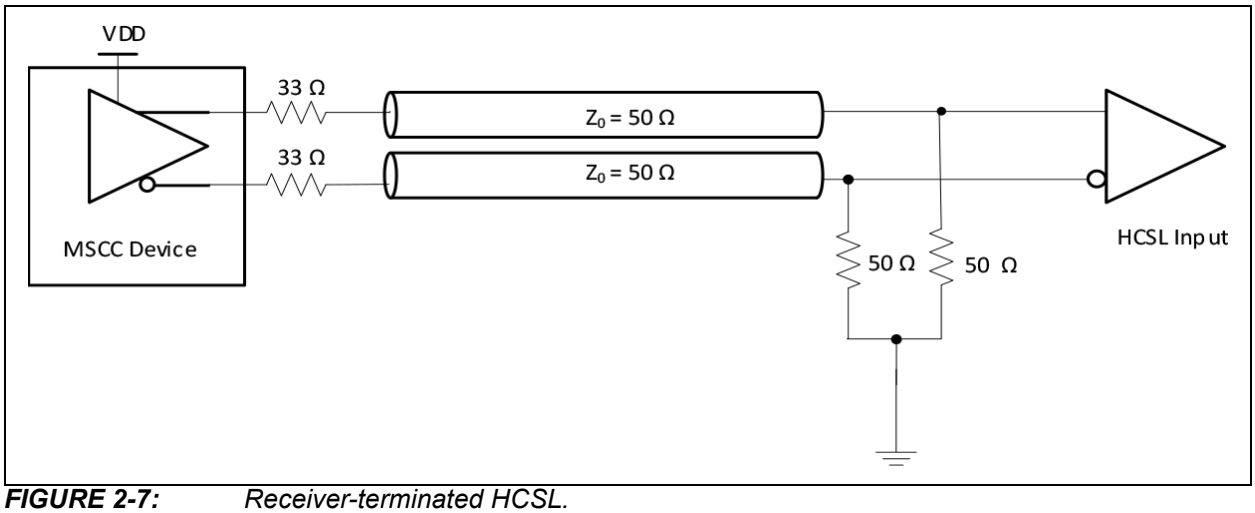


FIGURE 2-7: *Receiver-terminated HCSL.*

2.3 Termination of Unused Inputs and Outputs

Unused outputs should be left unconnected.

2.4 Power Consumption

The device total power consumption can be calculated as:

EQUATION 2-1:

$$P_T = P_S + P_C + P_{O\_DIFF}$$

Where:

$P_S = V_{DD} \times I_S$	Core power consumed by the input buffer. The static current (IS) is specified in Table 3-3.
$P_C = V_{DDO} \times I_{DD\_CM}$	Common output power shared among four outputs. The current IDD_CM is specified in Table 3-3.
$P_{O\_DIF} = V_{DDO} \times I_{DD\_HCSL} \times N$	Output power where output current per output (IDD_HCSL) is specified in Table 3-3. N is number of enabled outputs.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption:

EQUATION 2-2:

$$P_D = P_T - N \times P_{HCSL}$$

Where:

$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (50\Omega + 33\Omega)$	V_{SW} is voltage swing of HCSL output. 50Ω is termination resistance and 33Ω is series resistance of the HCSL output.

2.5 Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board, each power supply could optionally be further insulated with low resistance ferrite bead with 10 µF and 1 µF capacitors. Figure 2-8 shows the standard and optional decoupling method.

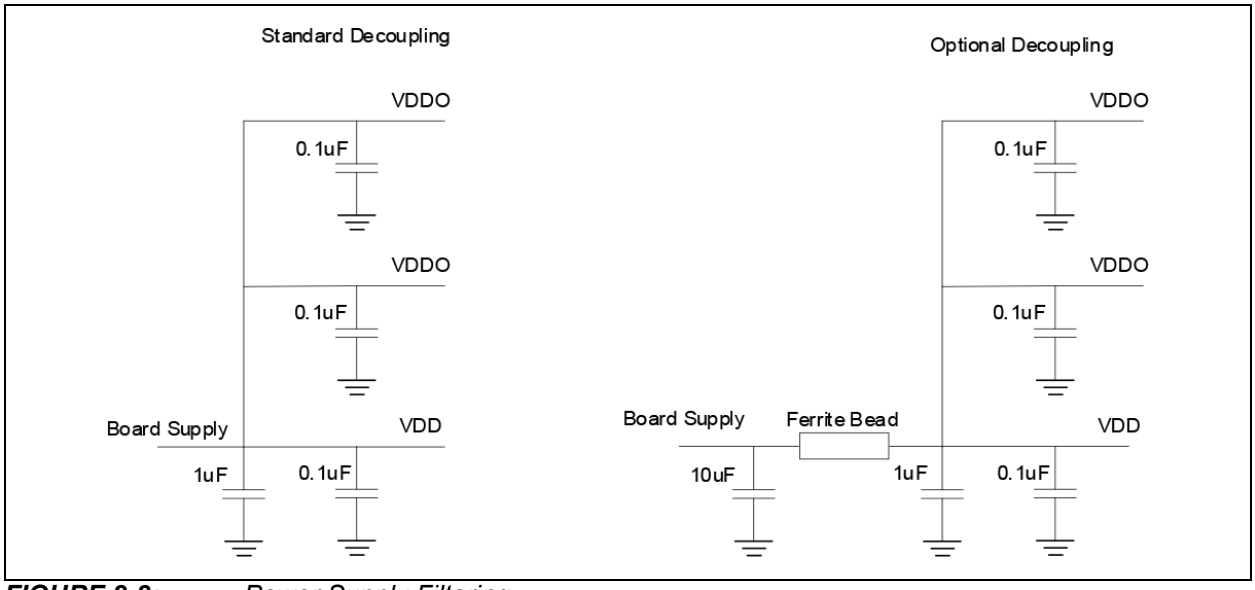


FIGURE 2-8: *Power Supply Filtering.*

2.6 Power Supplies and Power-up Sequence

The device has two different power supplies: VDD and VDDO which should always be connected to the same voltage supply. Voltages supported by each of these power supplies are specified in Table 3-2.

VDD and VDDO should always be turned on and off at the same time.

2.7 Device Control

ZL40264 outputs are controlled via OE[3:0]_b pins. When an OE_b pin is low the corresponding outputs will be active and when this pin is high the output will be high-Z. When the output driver is in high-Z mode, the output pins will be pulled low via external 50Ω HCSL termination resistors.

2.8 Typical phase noise performance

The following plots show typical phase noise performance for 100 MHz, 133 MHz, 400 MHz, and 491.52 MHz clocks respectively.

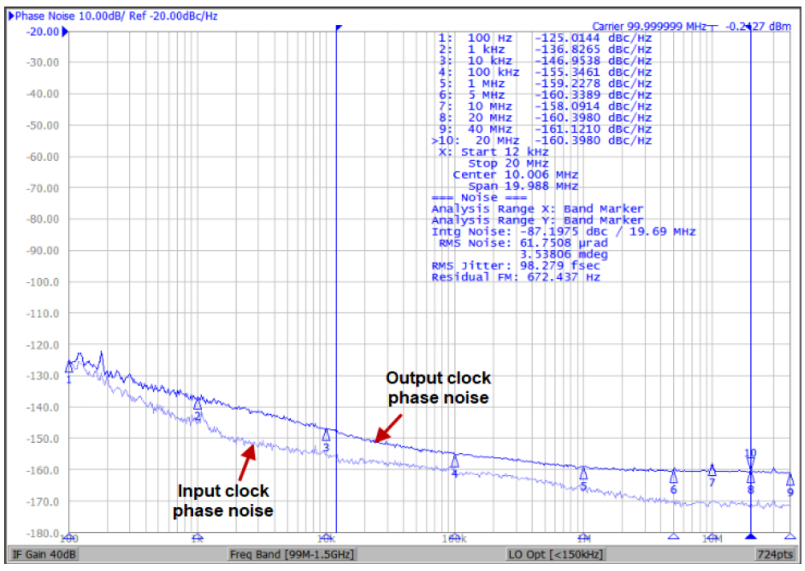


FIGURE 2-9: *100 MHz HCSL Phase Noise.*

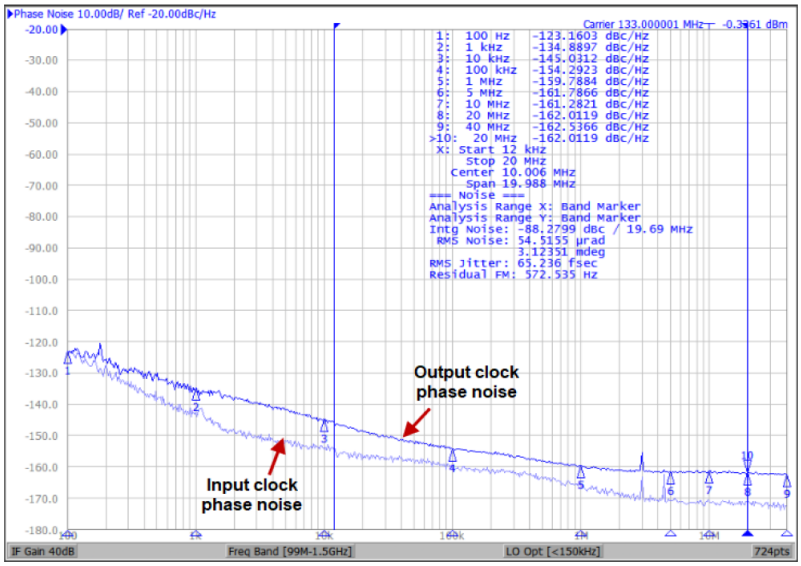


FIGURE 2-10: *133 MHz HCSL Phase Noise.*

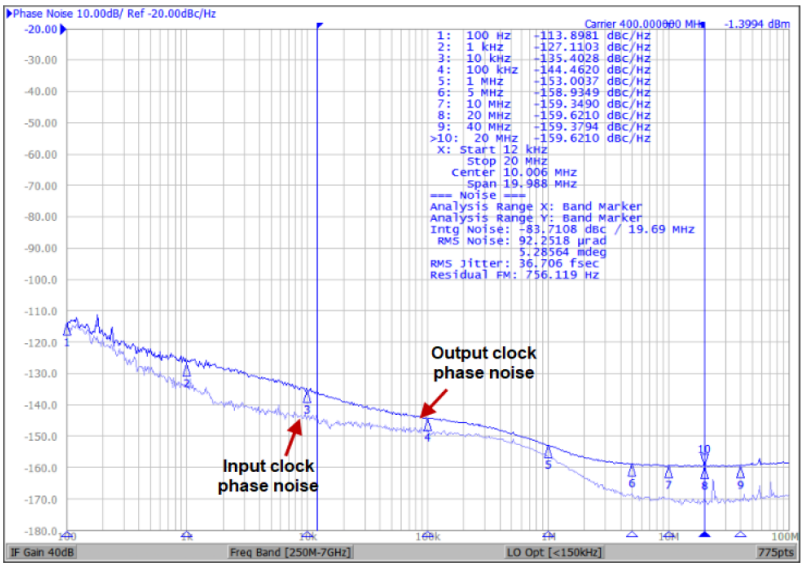


FIGURE 2-11: *400 MHz HCSL Phase Noise.*

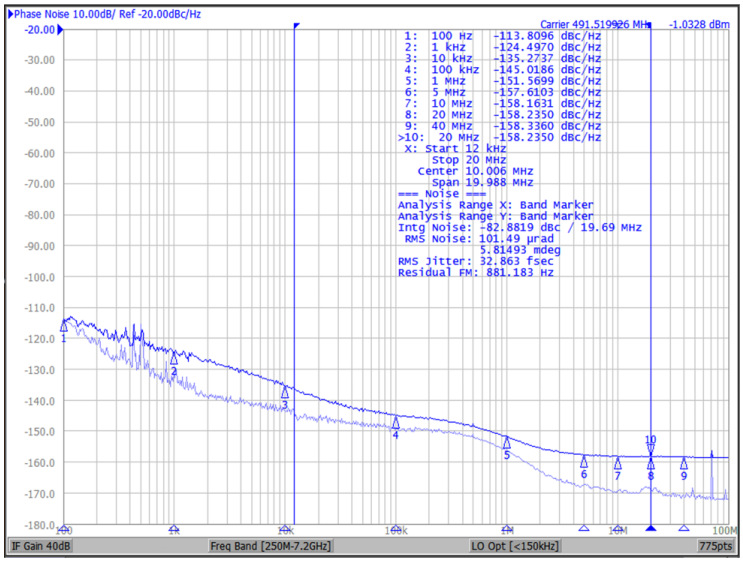


FIGURE 2-12: *491.52 MHz HCSL Phase Noise.*

NOTES:

3.0 AC AND DC ELECTRICAL CHARACTERISTICS

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2, Note 3)

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	–0.5	4.6	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	–0.5	3.5	V
Storage Temperature Range	T_{ST}	–55	125	°C

Note 1: Exceeding these values may cause permanent damage.

2: Functional operation under these conditions is not implied.

3: Voltages are with respect to ground (GND) unless otherwise stated.

TABLE 3-2: RECOMMENDED OPERATING RATINGS

(Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	3.135	3.30	3.465	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	2.375	2.50	2.625	V
Operating Temperature	T_A	–40	25	85	°C
Input Voltage	V_{DD-IN}	–0.3	—	V_{DD} + 0.3	V

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.

2: The device core supports two power supply modes (3.3V and 2.5V).

TABLE 3-3: CURRENT CONSUMPTION

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Core device current	$I_{S\_3.3V}$	—	49	53	mA	V_{DD} = 3.3V+5%
	$I_{S\_2.5V}$	—	48	53	mA	V_{DD} = 2.5V+5%
Common output current	$I_{DD\_CM\_3.3V}$	—	5.24	5.82	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_CM\_2.5V}$	—	4.72	5.32	mA	V_{DDO} = 2.5V+5%
Current dissipation per HCSL output	$I_{DD\_HCSL\_3.3V}$	—	14.92	17.18	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_HCSL\_2.5V}$	—	14.61	16.62	mA	V_{DDO} = 2.5V+5%

TABLE 3-4: INPUT CHARACTERISTICS

Note 1, Note 2, Note 3						
Parameter	**Symbol**	**Min**	**Typ.**	**Max**	**Units**	**Condition**
CMOS high-level input voltage for control inputs	$V_{CIH\_3.3V}$	0.7 × V_{DD}	—	—	V	V_{DD} = 3.3V
	$V_{CIH\_2.5V}$	0.8 × V_{DD}	—	—	V	V_{DD} = 3.3V
CMOS low-level input voltage for control inputs	V_{CIL}	—	—	0.32 × V_{DD}	V	—
CMOS input leakage current for control inputs (includes current due to pull down resistors)	I_{IL}	–25	—	50	µA	V_I = V_{DD} or 0V
Differential input common mode voltage for IN_p/n	V_{CM}	0.1	—	0.8	V	—
Differential input voltage for IN_p/n	V_{ID}	0.2	—	VDD + 0.3	V	—
Differential input leakage current for IN_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	–150	—	150	µA	V_I = 2V or 0V
Single ended input voltage for IN_p	V_{SI}	–0.3	—	2.7	V	V_{DD} = 3.3V or 2.5V
Single ended input common mode voltage IN_p	V_{SIC}	0.1	—	0.8	V	V_{DD} = 3.3V or 2.5V
Single ended input voltage swing for IN_p	V_{SID}	0.3	—	1.3	V	V_{DD} = 3.3V or 2.5V
Input frequency (differential)	f_{IN}	0	—	600	MHz	—
Input duty cycle (400 MHz input clock)	dc	35	—	65	%	Note 4
Input slew rate	slew	0.6	2	—	V/ns	—
Input pull-up/pull-down resistance	R_{PU}/R_{PD}	—	60	—	kΩ	—
Input pull-down resistance for IN_p	R_{PD}	—	30	—	kΩ	—
Control input (OE_b) pull-down resistance	R_{PDOE}	—	300	—	kΩ	—

Note 1: Values are over recommended operating conditions.

2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

3: Low frequency only.

4: Minimum and maximum duty cycles should be scaled for different input frequencies. For example, a 10 MHz input clock would have the minimum duty cycle of 1% and the maximum duty cycle of 99%.

TABLE 3-5: POWER SUPPLY REJECTION RATIO FOR VDD = VDDO = 3.3V

Note 1, Note 2, Note 3

Parameter	Symbol	Min	Typ.	Max	Units	Condition
PSRR for HCSL output	$PSRR_{HCSL}$	—	–80.7	—	dBc	f_{IN} = 100 MHz
			–76.4			f_{IN} = 133 MHz
			–66.5			f_{IN} = 400 MHz

Note 1: Values are over recommended operating conditions.

2: Noise injected to V_{DD}/V_{DDO} power supply with frequency 100 kHz and amplitude 100 mVpp.

3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 3-6: POWER SUPPLY REJECTION RATIO FOR VDD = VDDO = 2.5V

Note 1, Note 2, Note 3

Parameter	Symbol	Min	Typ.	Max	Units	Condition
PSRR for HCSL output	$PSRR_{HCSL}$	—	–73.5	—	dBc	f_{IN} = 100 MHz
			–69.8			f_{IN} = 133 MHz
			–61.2			f_{IN} = 400 MHz

Note 1: Values are over recommended operating conditions.

2: Noise injected to V_{DD}/V_{DDO} power supply with frequency 100 kHz and amplitude 100 mVpp.

3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 3-7: HCSL OUTPUTS FOR VDDO = 3.3V

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Rising edge rate	rise_rate	1.3	1.7	2	V/ns	Note 3, Note 4
Falling edge rate	fall_rate	1.3	1.7	2	V/ns	Note 3, Note 4
Differential high voltage	V_{IH}	0.6	—	0.9	V	Note 3
Differential low voltage	V_{IL}	–0.9	—	–0.6	V	Note 3
Single ended high voltage	V_{SIH}	0.6	0.74	0.85	V	DC Measurement
Single ended low voltage	V_{SIL}	–0.01	0	0.01	V	DC Measurement
Absolute crossing voltage	V_{CROSS}	0.26	0.32	0.38	V	Note 2, Note 5, Note 6
Variation of V_{CROSS} over all rising clock edges	ΔV_{CROSS}	0.039	0.050	0.061	V	Note 2, Note 5, Note 10
Ring back voltage margin	V_{RB}	0.534	0.674	0.809	V	Note 3, Note 12
Time before V_{RB} is allowed	t_{STABLE}	4.6	—	—	ns	Note 3, Note 12
Cycle-to-cycle additive jitter	T_{JCC}	—	6.5	8.1	ps peak-to-peak	Note 3
Absolute maximum voltage	V_{MAX}	—	—	0.92	—	Note 2, Note 8
Absolute minimum voltage	V_{MIN}	–0.05	—	—	—	Note 2, Note 9
Output duty-cycle (when input has 50% duty-cycle)	duty_cycle	48	50	52	%	Note 3
Rising to falling edge matching	r/f match	—	—	15	%	Note 2, Note 13
Clock source DC impedance (CK)	$Z_{C\text{-}DC\_CK}$	49	50	51	Ω	DC Measurement Note 2, Note 14)
Clock source DC impedance (CK#)	$Z_{C\text{-}DC\_CK\#}$	49	50	51	Ω	DC Measurement Note 2, Note 14
Output frequency	F_{MAX}	0	—	600	MHz	—

TABLE 3-7: HCSL OUTPUTS FOR VDDO = 3.3V (CONTINUED)

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Output-to-output skew	t_{OOSK}	—	—	50	ps	—
Device-to-device output skew	t_{DOOSK}	—	—	129	ps	—
Input-to-output delay	t_{IOD}	0.75	0.84	1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	2	cycles	—

Note 1: Values are over recommended operating conditions.

2: Measurement taken from single ended waveform.

3: Measurement taken from differential waveform.

4: Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 3-4.

5: Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK#. See Figure 3-1.

6: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 3-1.

7: This requirement—from PCI Express Base Specification, Revision 4.0—is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

8: Defined as the maximum instantaneous voltage including overshoot. See Figure 3-1.

9: Defined as the minimum instantaneous voltage including undershoot. See Figure 3-1.

10: Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 3-2.

11: The PPM requirement—from PCIe Express Base Specification, Revision 4.0—is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

12: The t_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after 20 rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 3-5.

13: Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cros point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 3-3.

14: Clock DC impedance tolerance depends only on the tolerance of external 50Ω shunt resistors used in HCSL. The test used resistors with ±1% tolerance.

TABLE 3-8: HCSL (PCIE) JITTER PERFORMANCE FOR VDDO = 3.3V

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$T_{PCIe\_1.0}$	—	1.2	1.45	ps pk-pk	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$T_{PCIe\_2.0\_high}$	—	134	163	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$T_{PCIe\_2.0\_low}$	—	31	48	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 mid band (5 MHz to 16 MHz)	$T_{PCIe\_2.0\_mid}$	—	105	130	fs RMS	Input clock: 100 MHz

TABLE 3-8: HCSL (PCIE) JITTER PERFORMANCE FOR VDDO = 3.3V (CONTINUED)

Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{PCIe\_3.0}$	—	33	41	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{PCIe\_4.0}$	—	33	41	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$T_{PCIe\_5.0}$	—	13	16	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 MHz to 1 MHz, CDR for 64 GT/s CC)	$T_{PCIe\_6.0}$	—	8	10	fs RMS	Input clock: 100 MHz
Additive Jitter as per Intel QPI 9.6 Gbps	T_{PCIe}	—	61	75	fs RMS	Input clock: 100 MHz
Additive RMS Jitter in 1 MHz to 20 MHz Band	$T_{j\_1M\_20M}$	—	87	106	fs RMS	Input clock: 100 MHz
		—	56	68		Input clock: 133 MHz
		—	26	34		Input clock: 400 MHz
		—	25	32		Input clock: 491.52 MHz
Additive RMS Jitter in 12 kHz to 20 MHz Band	$T_{j\_12k\_20M}$	—	91	112	fs RMS	Input clock: 100 MHz
		—	60	75		Input clock: 133 MHz
		—	32	48		Input clock: 400 MHz
		—	30	43		Input clock: 491.52 MHz
Noise Floor	NF	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–162	–161		Input clock: 133 MHz
		—	–160	–157		Input clock: 400 MHz
		—	–158	–155		Input clock: 491.52 MHz

Note 1: Values are over recommended operating conditions.

TABLE 3-9: HCSL OUTPUTS FOR VDDO = 2.5V

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Rising edge rate	rise_rate	1.3	1.6	1.9	V/ns	Note 2, Note 3
Falling edge rate	fall_rate	1.3	1.6	1.9	Vms	Note 2, Note 3
Differential high voltage	V_{IH}	0.6	—	0.9	V	Note 2
Differential low voltage	V_{IL}	–0.9	—	–0.6	V	Note 2
Single-ended high voltage	V_{SIH}	0.58	0.71	0.84	V	DC measurement
Single-ended low voltage	V_{SIL}	–0.01	0	0.01	V	DC measurement
Absolute crossing voltage	V_{CROSS}	0.25	0.31	0.37	V	Note 1, Note 4, Note 5
Variation of V_{CROSS} over all rising clock edges	ΔV_{CROSS}	0.04	0.05	0.06	V	Note 1, Note 4, Note 9
Ring back voltage margin	V_{RB}	0.514	0.660	0.791	V	Note 2, Note 11
Time before VRB is allowed	t_{STABLE}	4.6	—	—	ns	Note 2, Note 11
Additive cycle-to-cycle jitter	T_{JCC}	—	5.5	7.1	ps peak-to-peak	Note 2
Absolute maximum voltage	V_{MAX}	—	—	0.90		Note 1, Note 7
Absolute minimum voltage	V_{MIN}	–0.05	—	—		Note 1, Note 8
Output duty-cycle (when input has 50% duty-cycle)	duty_cycle	48	50	52	%	Note 2

TABLE 3-9: HCSL OUTPUTS FOR VDDO = 2.5V (CONTINUED)

Note 1						
Parameter	**Symbol**	**Min**	**Typ.**	**Max**	**Units**	**Condition**
Rising to falling edge matching	r/f match	—	—	15	%	Note 1, Note 12
Clock source DC impedance (CK)	$Z_{C\text{-}DC\_CK}$	49	50	51	Ω	DC measurement, Note 1, Note 13
Clock source DC impedance (CK#)	$Z_{C\text{-}DC\_CK\#}$	0	50	51	Ω	DC measurement, Note 1, Note 13
Output frequency	F_{MAX}	—	—	600	MHz	—
Output-to-output skew	t_{OOSK}	—	—	50	ps	—
Device-to-device output skew	t_{DOOSK}	0.75	—	129	ps	—
Input-to-output delay	t_{OPD}	—	0.85	1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—

Note 1: Values are over recommended operating conditions.

2: Measurement taken from single ended waveform.

3: Measurement taken from differential waveform.

4: Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 3-4.

5: Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK#. See Figure 3-1.

6: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 3-1.

7: This requirement—from PCI Express Base Specification, Revision 4.0—is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

8: Defined as the maximum instantaneous voltage including overshoot. See Figure 3-1.

9: Defined as the minimum instantaneous voltage including undershoot. See Figure 3-1.

10: Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 3-2.

11: The PPM requirement—from PCIe Express Base Specification, Revision 4.0—is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

12: The t_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after 20 rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 3-5.

13: Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cros point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 3-3.

14: Clock DC impedance tolerance depends only on the tolerance of external 50Ω shunt resistors used in HCSL. The test used resistors with ±1% tolerance.

TABLE 3-10: HCSL (PCIE) JITTER PERFORMANCE FOR VDDO = 2.5V

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$T_{jPCIe\_1.0}$	—	1.03	1.27	ps pk-pk	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$T_{jPCIe\_2.0\_high}$	—	115	143	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$T_{jPCIe\_2.0\_low}$	—	28	46	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 mid band (5 MHz to 16 MHz)	$T_{jPCIe\_2.0\_mid}$	—	91	113	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIe\_3.0}$	—	29	36	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIe\_4.0}$	—	29	36	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$T_{jPCIe\_5.0}$	—	11	14	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 MHz to 1 MHz, CDR for 64 GT/s CC)	$T_{jPCIe\_6.0}$	—	7	9	fs RMS	Input clock: 100 MHz
Additive Jitter as per Intel QPI 9.6 Gbps	T_{jQPI}	—	53	67	fs RMS	Input clock: 100 MHz
Additive RMS Jitter in 1 MHz to 20 MHz band	$T_{j\_1M\_20M}$	—	75	94	fs RMS	Input clock: 100 MHz
		—	51	64		Input clock: 133 MHz
		—	26	33		Input clock: 400 MHz
		—	25	32		Input clock: 491.52 MHz
Additive RMS Jitter in 12 kHz to 20 MHz band	$T_{j\_12k\_20M}$	—	79	99	fs RMS	Input clock: 100 MHz
		—	55	68		Input clock: 133 MHz
		—	32	47		Input clock: 400 MHz
		—	30	43		Input clock: 491.52 MHz
Noise floor	N_F	—	–162	–159	dBc/Hz	Input clock: 100 MHz
		—	–163	–161		Input clock: 133 MHz
		—	–160	–158		Input clock: 400 MHz
		—	–158	–155		Input clock: 491.52 MHz

Note 1: Values are over recommended operating conditions.

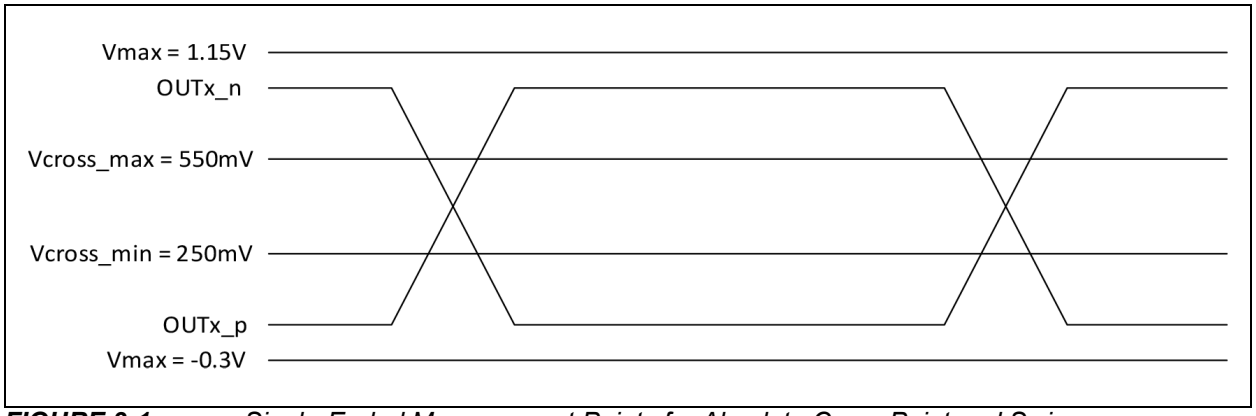


FIGURE 3-1: *Single-Ended Measurement Points for Absolute Cross Point and Swing.*

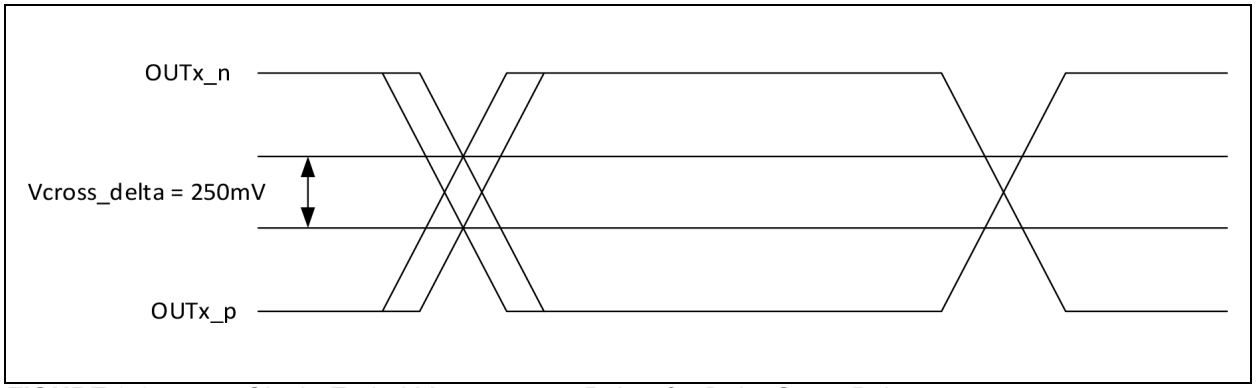


FIGURE 3-2: *Single-Ended Measurement Points for Delta Cross Point.*

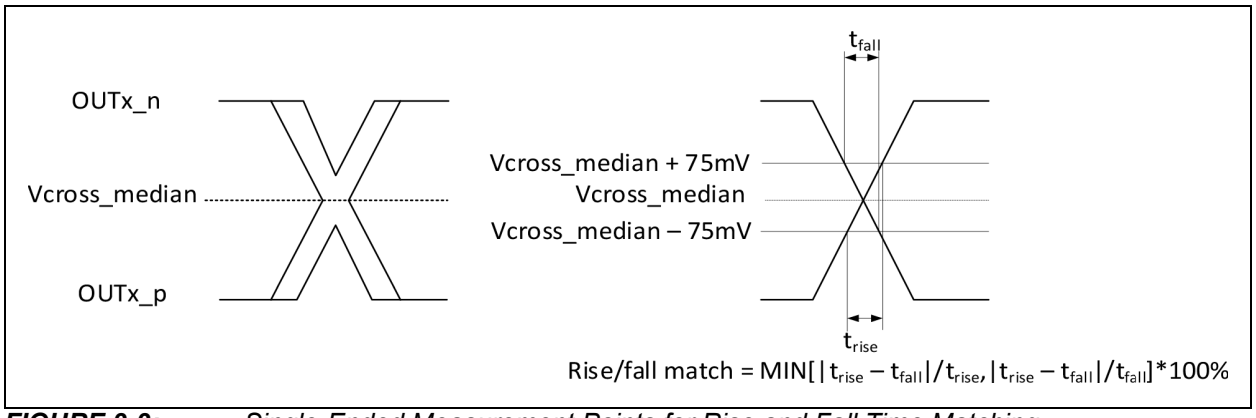


FIGURE 3-3: *Single-Ended Measurement Points for Rise and Fall Time Matching.*

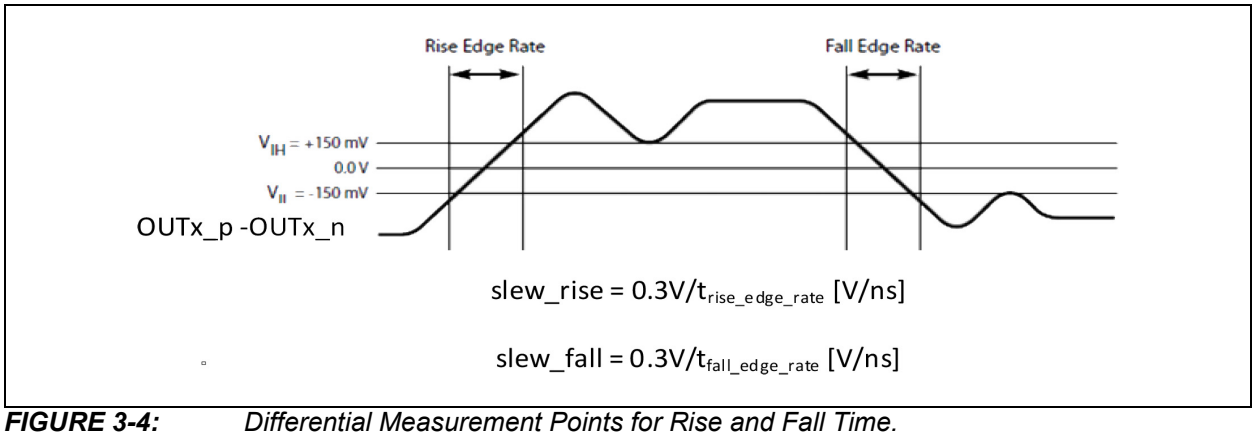


FIGURE 3-4: *Differential Measurement Points for Rise and Fall Time.*

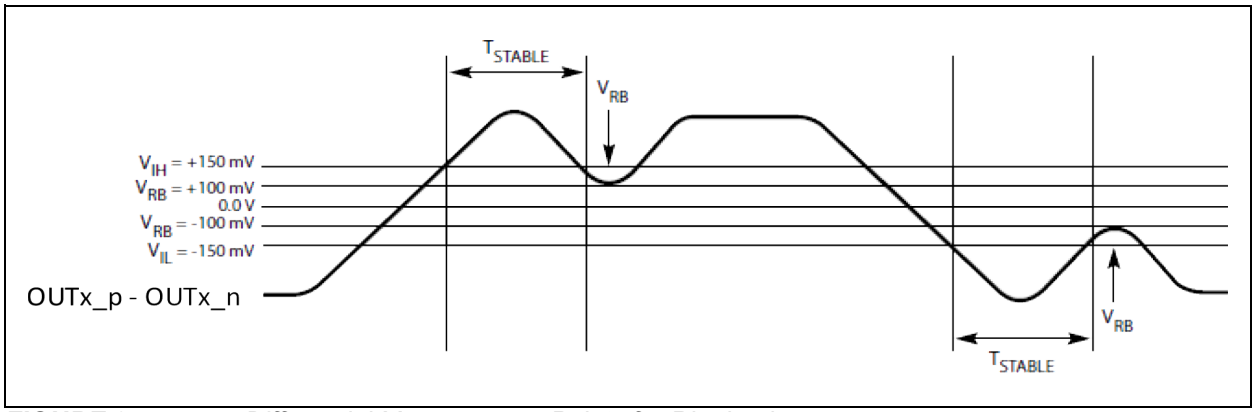


FIGURE 3-5: *Differential Measurement Points for Ringback.*

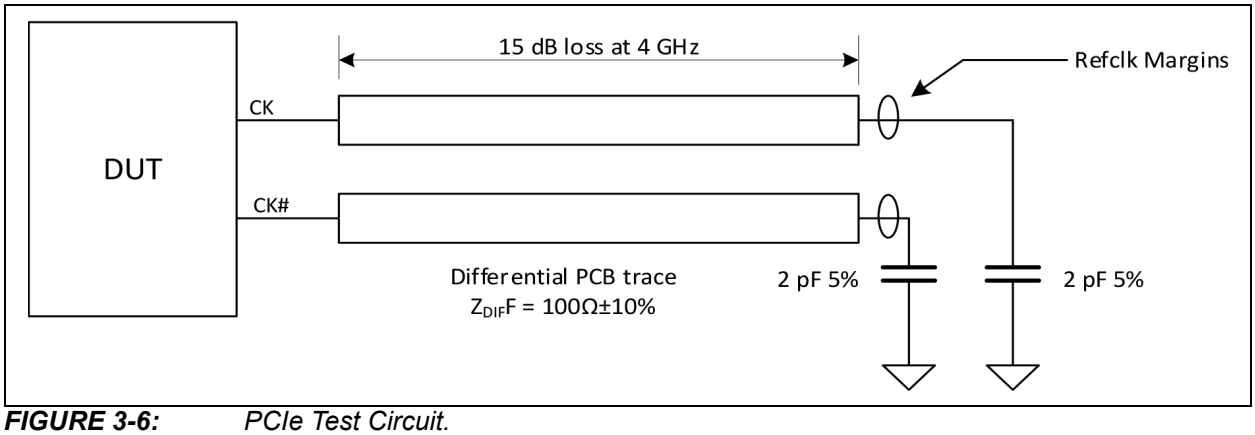


FIGURE 3-6: *PCIe Test Circuit.*

TABLE 3-11: 4 MM × 4 MM VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Value	Units	Condition
Maximum ambient temperature	T_A	85	°C	—
Maximum junction temperature	T_{JMAX}	125	°C	—
Junction-to-ambient thermal resistance (Note 1)	θ_{JA}	34	°C/W	Still air
		28.9		1 m/s airflow
		27.0		2.5 m/s airflow
Junction-to-board thermal resistance	θ_{JB}	15.4	°C/W	—
Junction-to-case thermal resistance	θ_{JC}	25.9	°C/W	—
Junction-to-pad thermal resistance	θ_{JP}	8.1	°C/W	Still air
Junction-to-top-center thermal characterization parameter	Ψ_{JT}	1.0	°C/W	Still air

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package).

TABLE 3-12: HCSL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

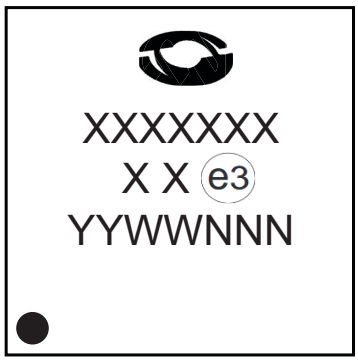
Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$T_{J\_12M\_5M}$	—	235	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	143	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	N_F	—	–102	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–126	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–153	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–158	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–159	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–158	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–97	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–123	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–153	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–162	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–162	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–163	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

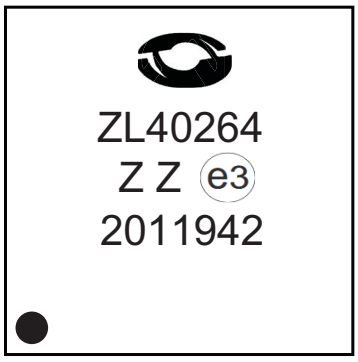
4.0 PACKAGE OUTLINE

4.1 Package Marking Information

20-Lead VQFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

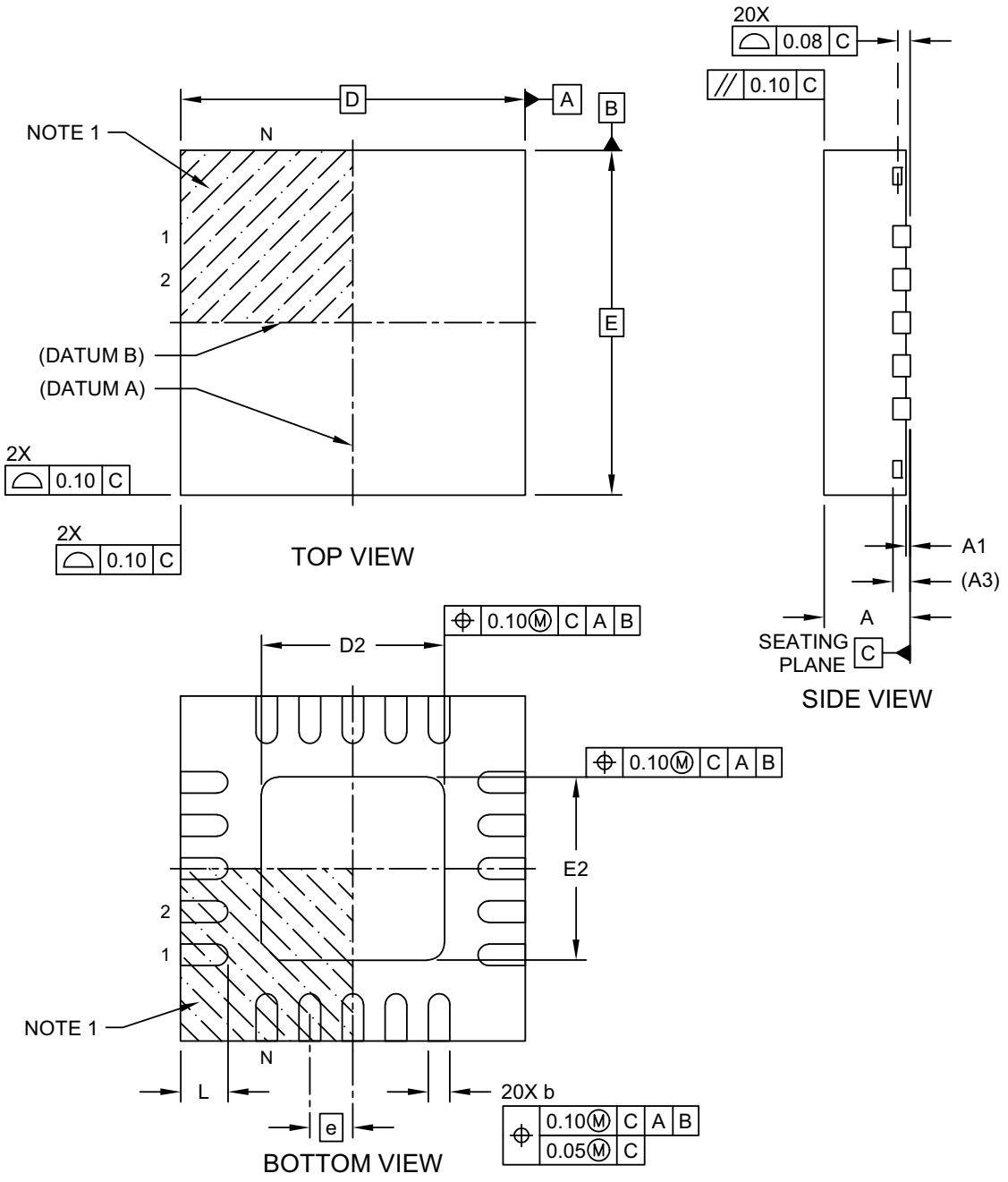
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space: 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N.

20-Lead 4 mm × 4 mm VQFN with 2.125 mm Exposed Pad (LWC) Package Outline and Recommended Landing Pattern

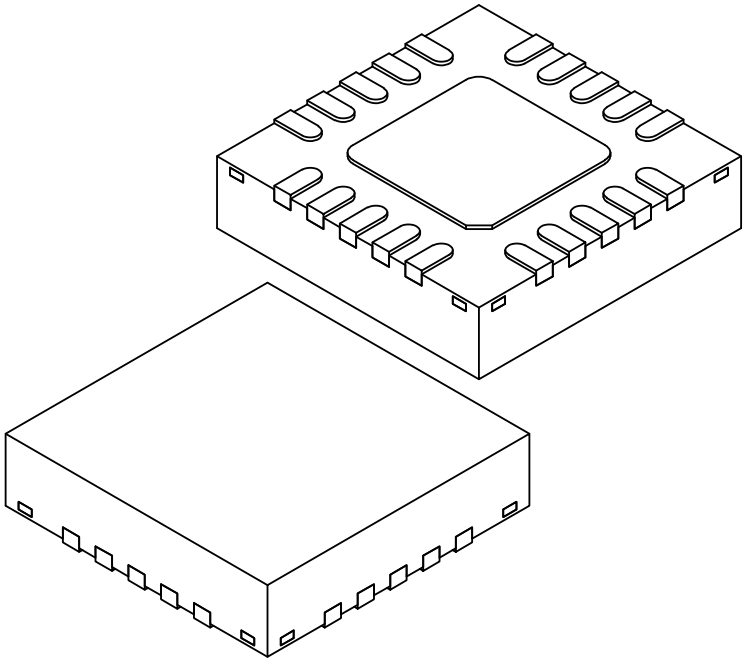
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25395 Rev A Sheet 1 of 2

20-Lead 4 mm × 4 mm VQFN with 2.125 mm Exposed Pad (LWC) Package Outline and Recommended Landing Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.025	2.125	2.225
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.025	2.125	2.225
Terminal Width	b	0.20	0.25	0.32
Terminal Length	L	0.45	0.55	0.65

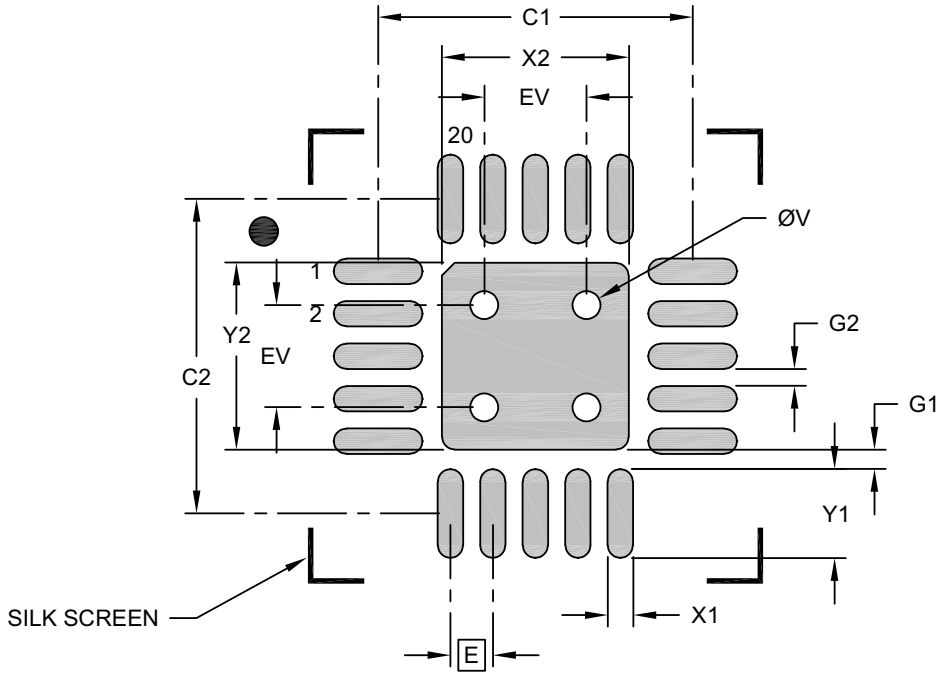
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25395 Rev A Sheet 2 of 2

20-Lead 4 mm × 4 mm VQFN with 2.125 mm Exposed Pad (LWC) Package Outline and Recommended Landing Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.20
Optional Center Pad Length	Y2			2.20
Contact Pad Spacing	C1		3.70	
Contact Pad Spacing	C2		3.70	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			1.05
Contact Pad to Center Pad (X20)	G1	0.23		
Contact Pad to Contact Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27395 Rev A

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006788A (07-2024)	—	Converted Microsemi data sheet ZL40264 to Microchip DS20006788A. Figures 2-4 and 2-5 updated. Added Figure 2-12. Updated multiple tables throughout Section 3. Minor text and table changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	XX	X
Device	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL40264: Four Output Ultra-Low Additive Phase Noise PCIe, Gen 1 to 5, and UPI/QPI Fanout Buffer
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 20-Lead VQFN Package with E-Pad
Media Type:	G = 490/Tray F = 4,000/Tape & Reel
Finish:	1 = Pb Free with Matte Sn Lead Finish Equating to RoHS e3

Examples:

a) ZL40264LDG1: Low Skew, Low Additive Jitter, Leadless Chip Carrier, 48-Lead VQFN Package, 490/Tray and Pb Free with Matte Sn Lead Finish Equating to RoHS e3

b) ZL40264LDF1: Low Skew, Low Additive Jitter, Leadless Chip Carrier, 48-Lead VQFN Package, 4,000/Reel and Pb Free with Matte Sn Lead Finish Equating to RoHS e3

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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