ZL40241

Ten LVCMOS Output Low Additive Jitter Fanout Buffer

Features

- 3-to-1 Input Multiplexer: Two Inputs Accept Any Differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a Single Ended Signal and the Third Input Accepts a Crystal or a Single Ended Signal
- Ten 1.5V/1.8V/2.5V/3.3V LVCMOS Outputs
- Supports Frequencies from 0 MHz to 200 MHz
- Supports Crystals from 8 MHz to 60 MHz
- Ultra-Low Additive Jitter: 17 fs (12 kHz to 20 MHz)
- Ultra-Low Noise Floor of -170 dBc/Hz
- Supports 2.5V or 3.3V Power Supplies
- Output to Output Skew of 30 ps (Typical)
- Input to Output Delay of 2 ns (Typical)

Applications

- General Purpose Clock Distribution
- Low Jitter Clock Trees
- Logic Translation
- Clock and Data Signal Restoration
- Wired and Wireless Communications
- High Performance Microprocessor Clock Distribution
- Medical Imaging
- Test Equipment

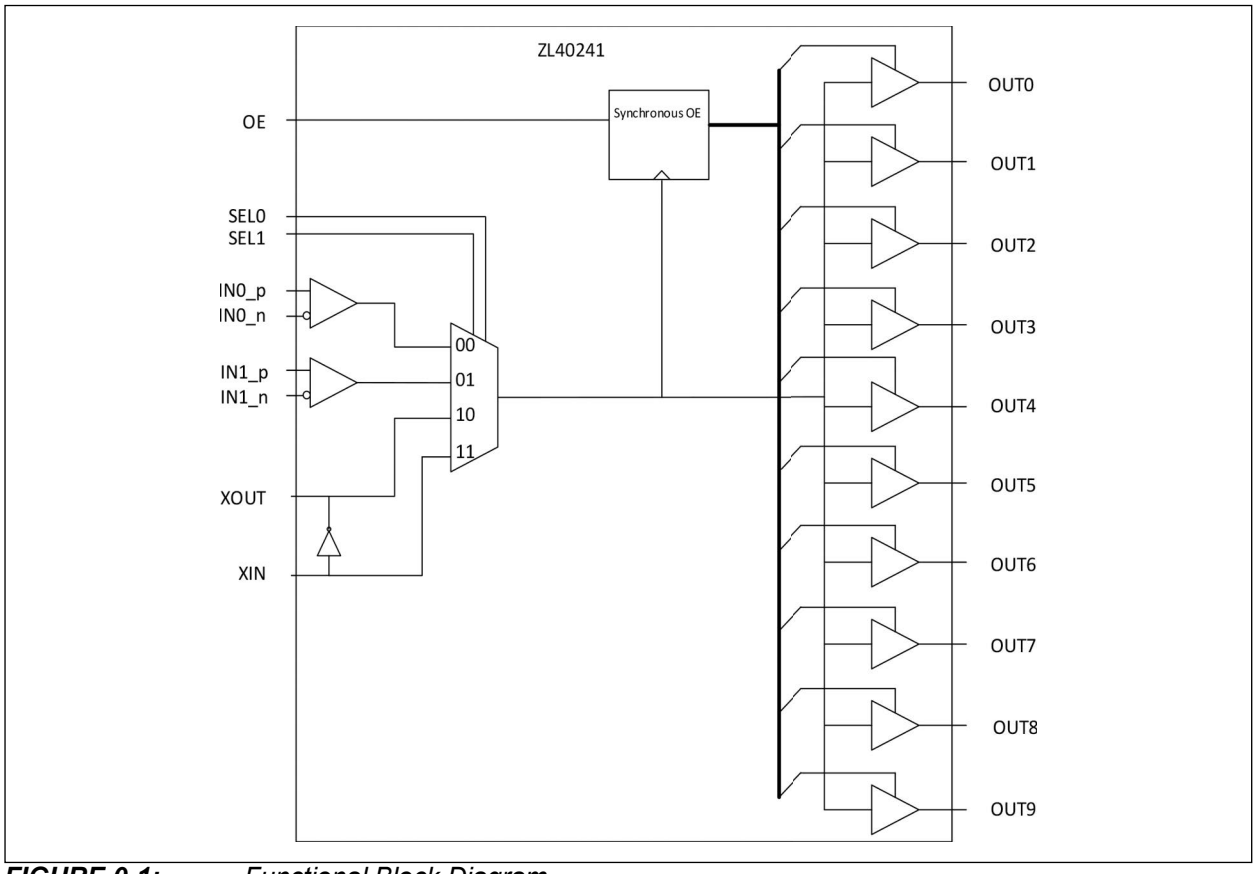

FIGURE 0-1: *Functional Block Diagram.*

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1.0 PIN DESCRIPTION AND CONFIGURATION

The device is packaged in a 5 mm × 5 mm 32-lead VQFN.

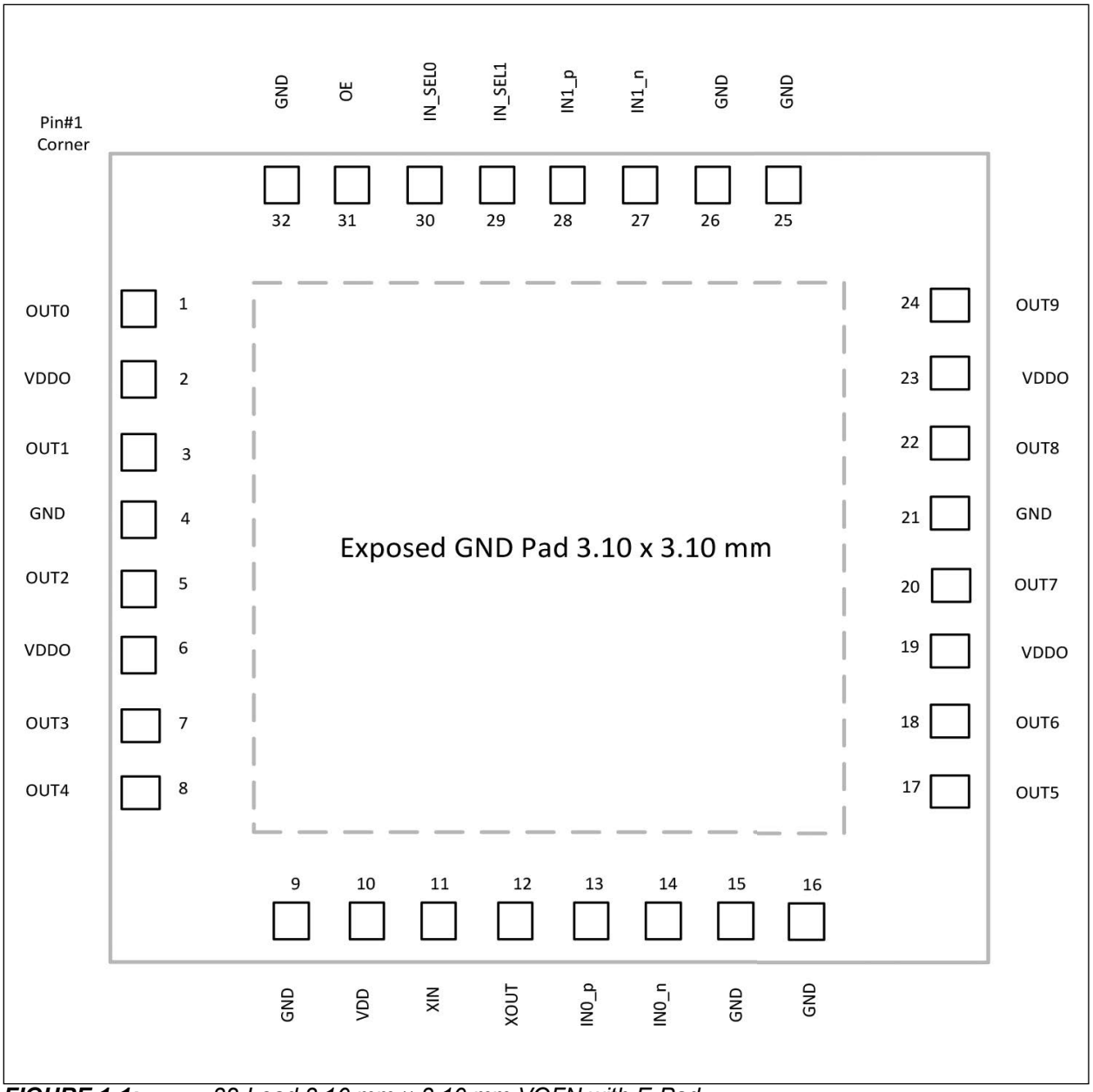


FIGURE 1-1: *32-Lead 3.10 mm × 3.10 mm VQFN with E-Pad.*

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300 kΩ internal pull-up resistor, I_{PD} – input with 300 kΩ internal pull-down resistor, I_{APU} – input with 30 kΩ internal pull-up resistor, I_{APD} – input with 30 kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased at VDD/2 with 60 kΩ internal pull-up and 60 kΩ pull-down resistors, O – output, I/O – Input/Output pin, P – power supply pin.

TABLE 1-1: PIN DESCRIPTIONS

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Input References</td></tr>
<tr><td>13</td><td>IN0_p</td><td>I_{APD}</td><td rowspan="4">Input Differential or Single Ended References 0 and 1

Input frequency range 0 Hz to 200 MHz.

Non inverting inputs (_p) are pulled down with internal 30 kΩ pull-down resistors. Inverting inputs (_n) are biased at VDD/2 with 60 kΩ pull-up and pull-down resistors to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).</td></tr>
<tr><td>14</td><td>IN0_n</td><td>$I_{APU/APD}$</td></tr>
<tr><td>28</td><td>IN1_p</td><td>I_{APD}</td></tr>
<tr><td>27</td><td>IN1_n</td><td>$I_{APU/APD}$</td></tr>
<tr><td colspan="4">Output Clocks</td></tr>
<tr><td>1</td><td>OUT0</td><td rowspan="10">O</td><td rowspan="10">Ultra Low Additive Jitter LVCMOS Outputs 0 to 9

Output frequency range 0 Hz to 200 MHz.</td></tr>
<tr><td>3</td><td>OUT1</td></tr>
<tr><td>5</td><td>OUT2</td></tr>
<tr><td>7</td><td>OUT3</td></tr>
<tr><td>8</td><td>OUT4</td></tr>
<tr><td>17</td><td>OUT5</td></tr>
<tr><td>18</td><td>OUT6</td></tr>
<tr><td>20</td><td>OUT7</td></tr>
<tr><td>22</td><td>OUT8</td></tr>
<tr><td>24</td><td>OUT9</td></tr>
<tr><td colspan="4">Control</td></tr>
<tr><td rowspan="6">30
29</td><td rowspan="6">IN_SEL0
IN_SEL1</td><td rowspan="6">I_{PD}</td><td>Input Select Pins. Logic level on these pins selects which input will be passed to the output.</td></tr>
<tr><td>IN_SEL1 | IN_SEL0 | OUTN</td></tr>
<tr><td>0 | 0 | Input 0 (IN0)</td></tr>
<tr><td>0 | 1 | Input 1 (IN1)</td></tr>
<tr><td>1 | 0 | Crystal Oscillator or Overdrive</td></tr>
<tr><td>1 | 1 | Crystal Bypass</td></tr>
<tr><td>31</td><td>OE</td><td>I_{PD}</td><td>Output Enable. When high outputs are enabled. When low outputs are high-Z.</td></tr>
<tr><td colspan="4">Crystal Oscillator</td></tr>
<tr><td>11</td><td>XIN</td><td>I</td><td>Crystal Oscillator Input or Crystal Bypass Mode or Crystal Overdrive Mode. If crystal oscillator is not used pull down this pin or connect it to ground.</td></tr>
<tr><td>12</td><td>XOUT</td><td>O</td><td>Crystal Oscillator Output.</td></tr>
<tr><td colspan="4">Power and Ground</td></tr>
<tr><td>10</td><td>VDD</td><td>P</td><td>Positive Supply Voltage. Connect to 3.3V or 2.5V supply. VDD voltage must be higher or equal to VDDO.</td></tr>
</table>

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	Type	Description
2	VDDO	P	**Positive Supply Voltage for LVCMOS Outputs.** Connect 3.3V, 2.5V, 1.8V or 1.5V power supply.
6			
19			
23			
4	GND	P	**Ground.** Connect to ground.
9			
15			
16			
21			
25			
26			
32			
E-Pad			

2.0 FUNCTIONAL DESCRIPTION

The ZL40241 is a programmable or hardware pin controlled low additive jitter, low power 3 × 10 LVCMOS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins.

The ZL40241 has ten LVCMOS outputs which can be powered from 3.3V, 2.5V, 1.8V, or 1.5V supply. Output can be synchronously enabled/disabled via OE pin.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

2.1 Clock Inputs

The following block diagrams show how to terminate different signals fed to the ZL40241 inputs. Figure 2-1 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each so that the transmission line is terminated with matched impedance (50Ω). However, if the driving strength of the output driver is not sufficient resistor values should be increased.

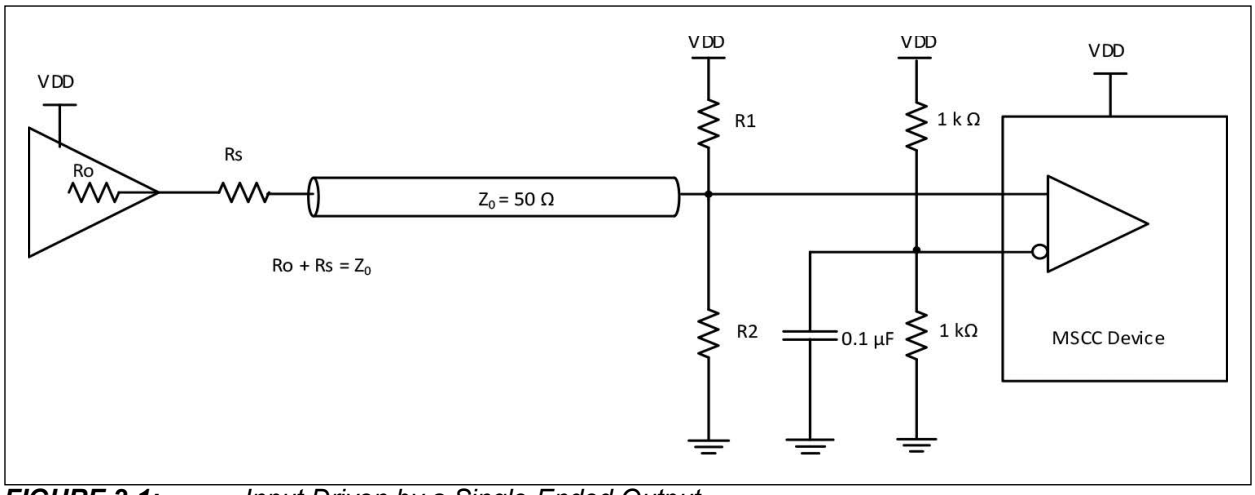


FIGURE 2-1: *Input Driven by a Single-Ended Output.*

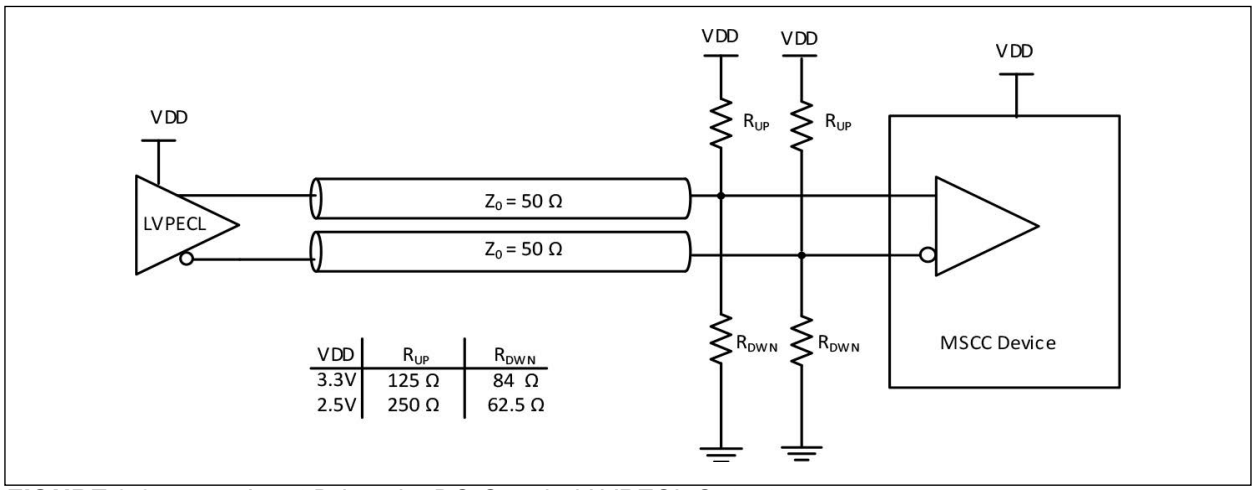


FIGURE 2-2: *Input Driven by DC-Coupled LVPECL Output.*

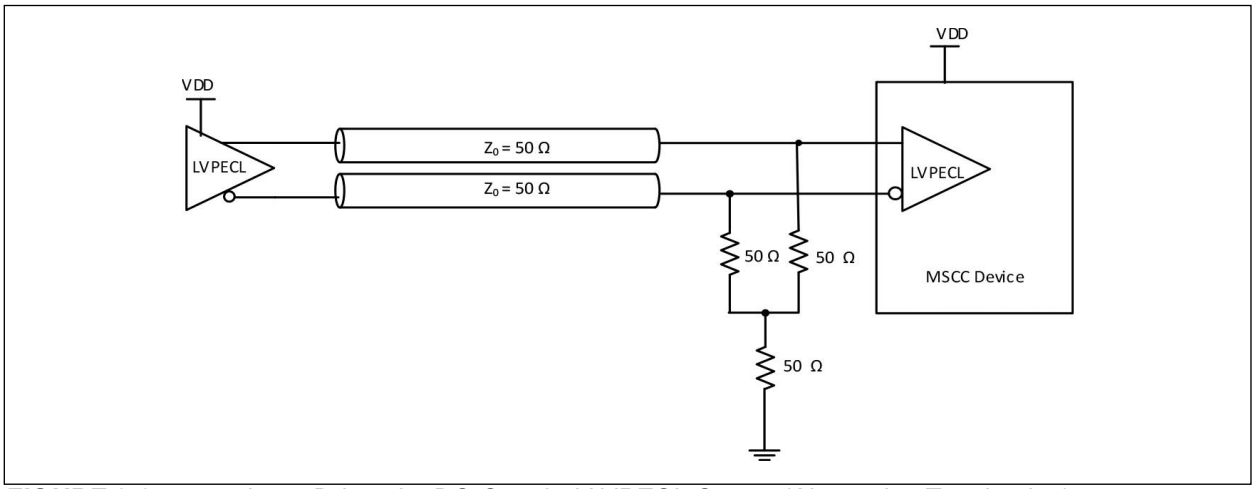


FIGURE 2-3: *Input Driven by DC-Coupled LVPECL Output (Alternative Termination).*

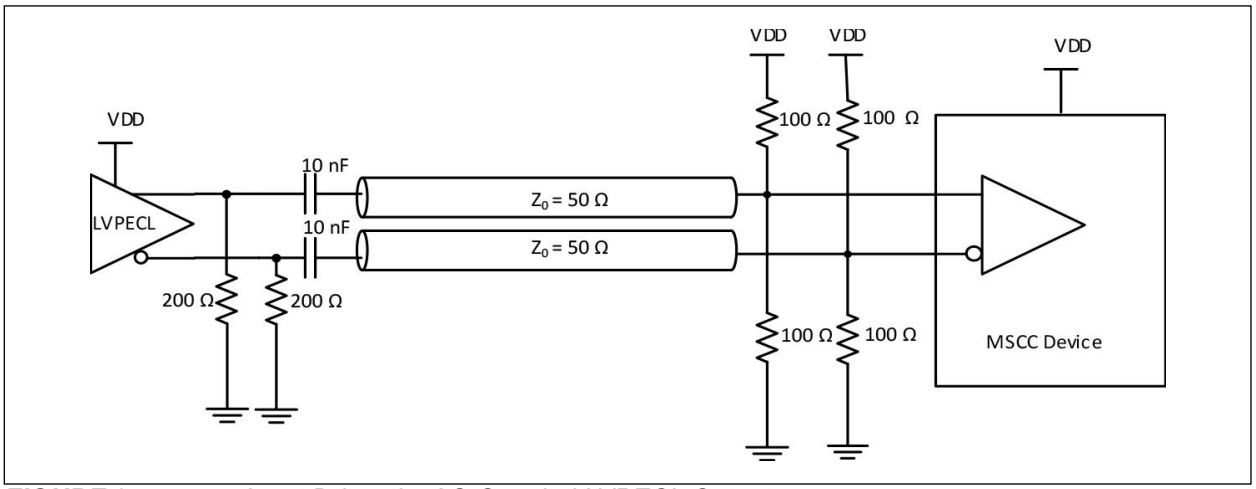


FIGURE 2-4: *Input Driven by AC-Coupled LVPECL Output.*

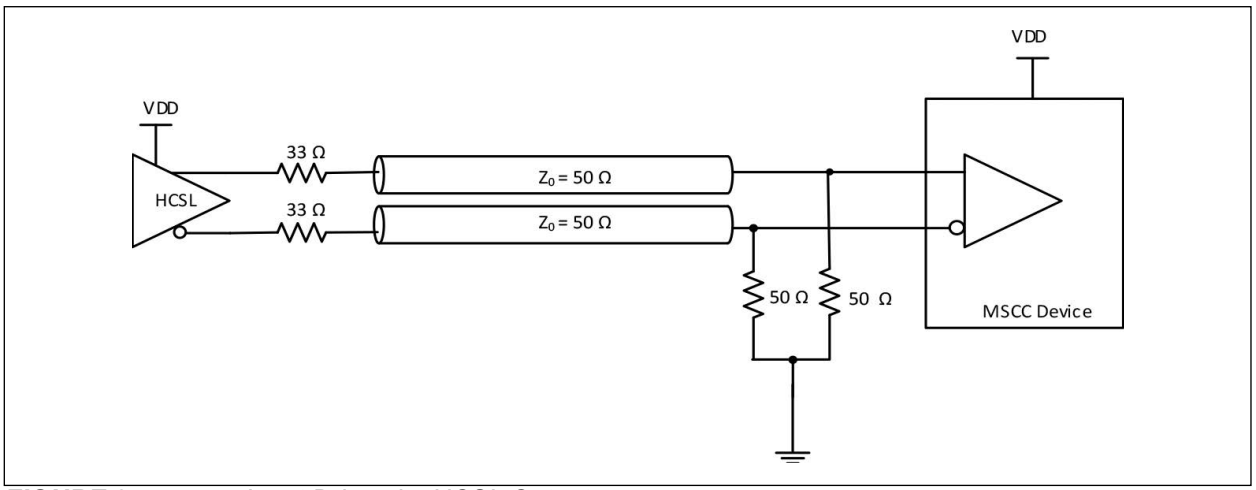


FIGURE 2-5: *Input Driven by HCSL Output.*

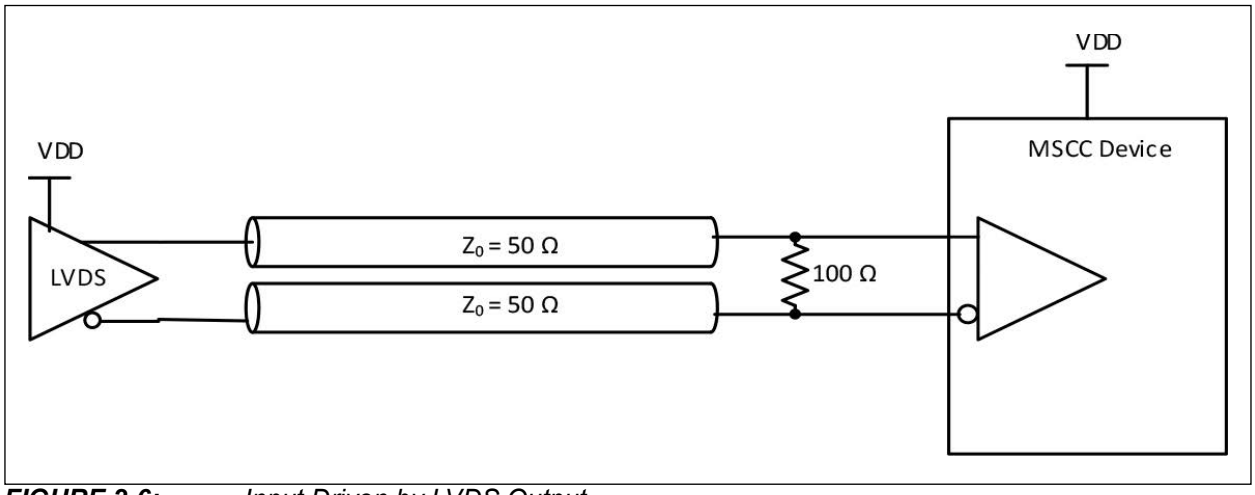


FIGURE 2-6: *Input Driven by LVDS Output.*

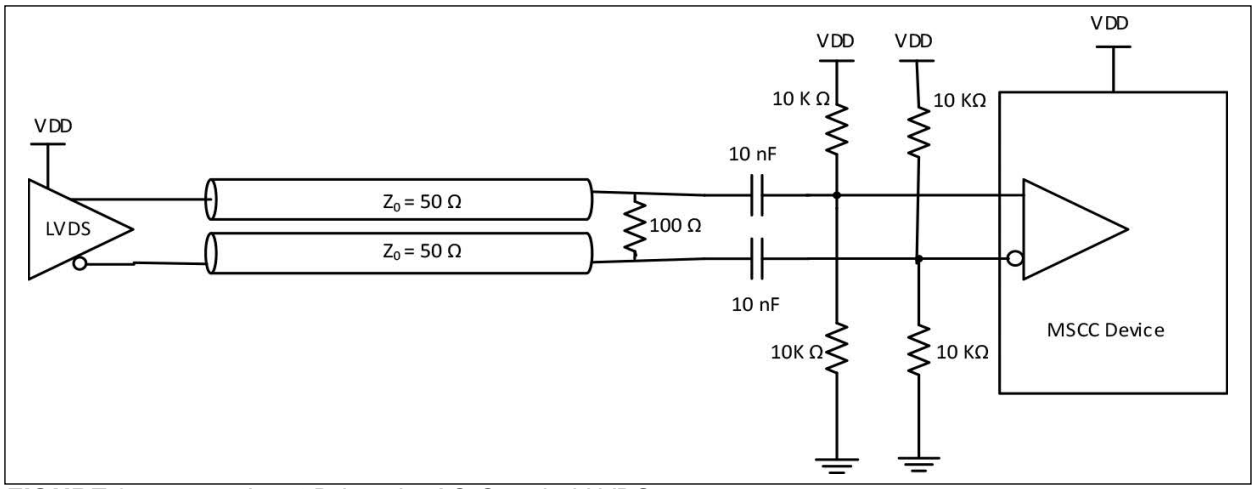


FIGURE 2-7: *Input Driven by AC-Coupled LVDS.*

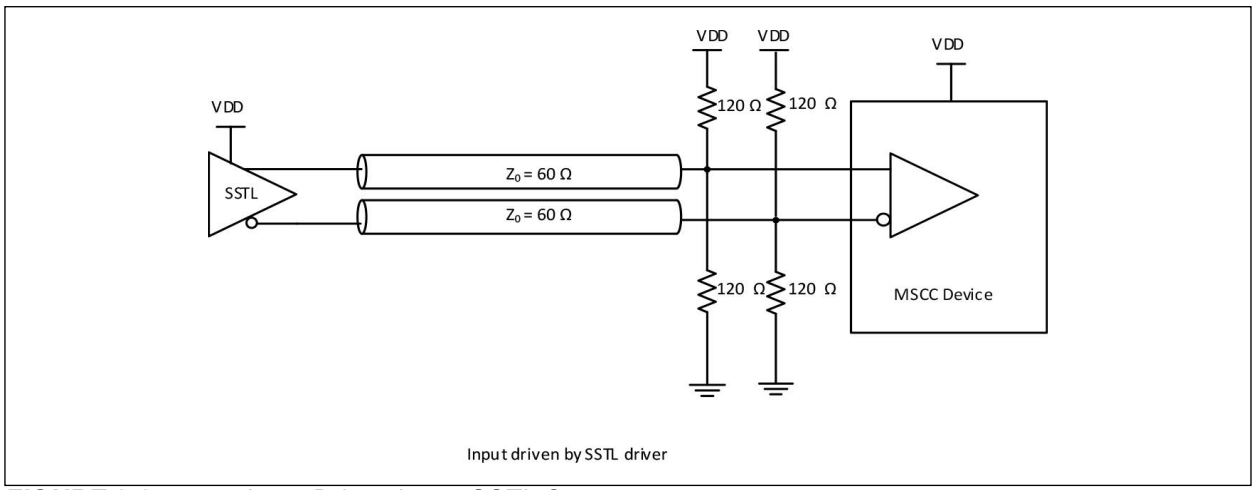


FIGURE 2-8: *Input Driven by an SSTL Output.*

2.2 Clock Outputs

LVCMOS outputs require only series termination resistor whose value is depending on LVCMOS output voltage as shown in Figure 2-9.

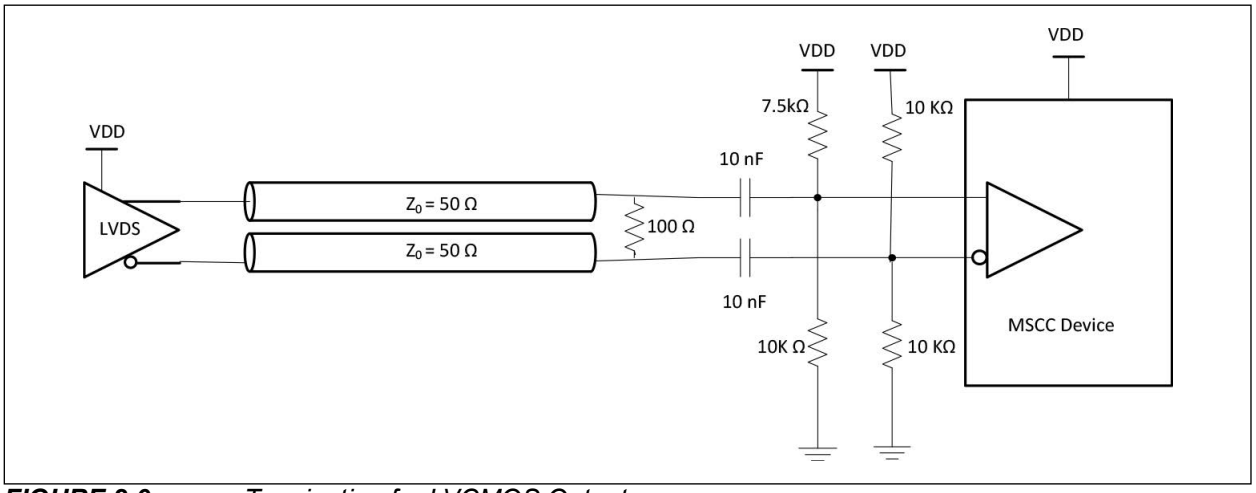


FIGURE 2-9: *Termination for LVCMOS Outputs.*

2.3 Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8 MHz to 160 MHz. Load capacitors C1 and C2 shall be selected as per crystal vendor recommendation. Shunt resistor is implemented inside the device. If the crystal is not used, connect XIN pin to ground.

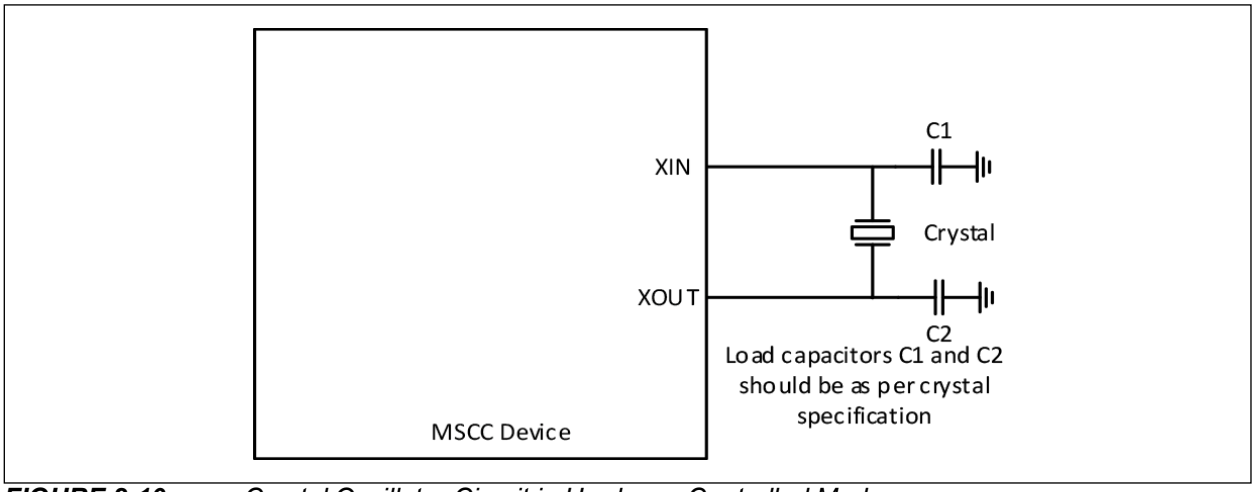


FIGURE 2-10: *Crystal Oscillator Circuit in Hardware Controlled Mode.*

The phase noise plot for 25 MHz crystal is shown in Figure 2-11. The phase noise floor of the device is below 170 dBc/Hz as can be seen on the figure.

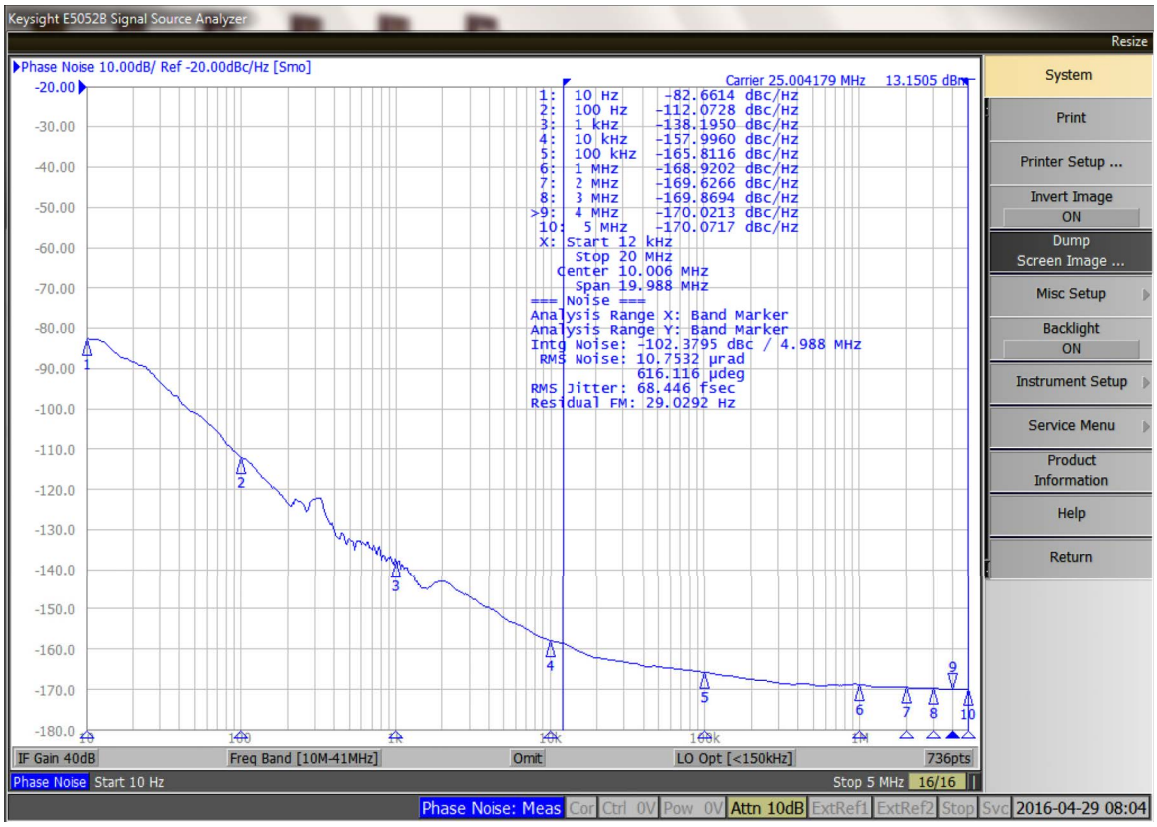


FIGURE 2-11: *Phase Noise Plot with 25 MHz Crystal.*

2.4 Termination of Unused Inputs and Outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1 KΩ resistor. Unused outputs should be left unconnected.

2.5 Power Consumption

The total device power consumption can be calculated as:

EQUATION 2-1:

$$P_T = P_S + P_{XTAL} + P_C + P_D$$

Where:

$P_S = V_{DD} \times I_S$	This is static power consumed by input buffers. If XTAL is running, this power should be set to zero. The static current (I_S) is specified in Table 3-2.
$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$	This is the power consumption of the XTAL circuit. The current of the XTAL circuit is provided in Table 3-2. If XTAL is not used, the power consumption is equal to zero.
$P_C = V_{DDO} \times I_{DDC}$	Common output power shared among all ten outputs. The current I_{DDC} is specified inTable 3-2.
$P_D = V_{DDO} \times (I_{DD} \times n \times f / 100\ MHz + V_{DD} \times C_{LOAD} \times f \times n)$	Dynamic power where dynamic current (I_{DD}) is specified in Table 3-2. C_{LOAD} is capacitive load driven by an output, f is frequency of hte output clock and n is number of active outputs.

The power consumption for different clock frequencies and power supply voltages can be quickly estimated from Figure 2-12, Figure 2-13, and Figure 2-14.

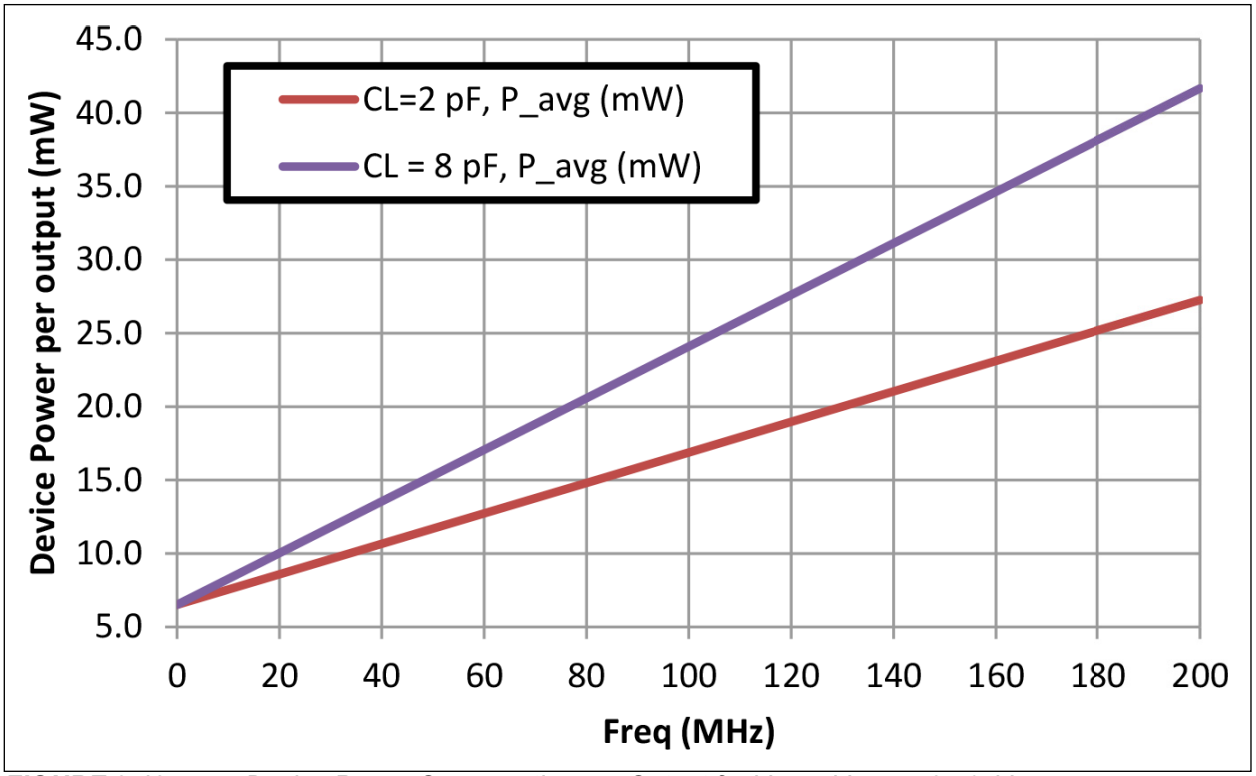


FIGURE 2-12: *Device Power Consumption per Output for V_{DD} = V_{DDO} = 3.465V.*

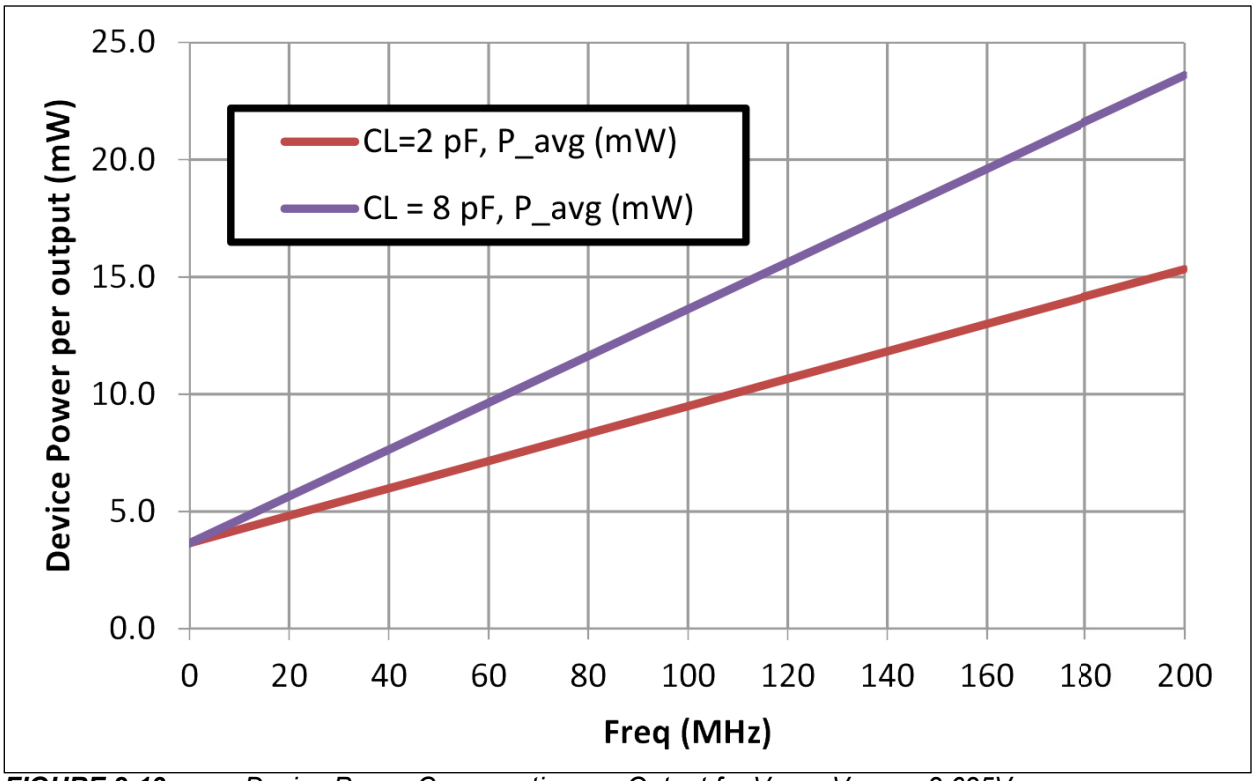


FIGURE 2-13: *Device Power Consumption per Output for V_{DD} = V_{DDO} = 2.625V.*

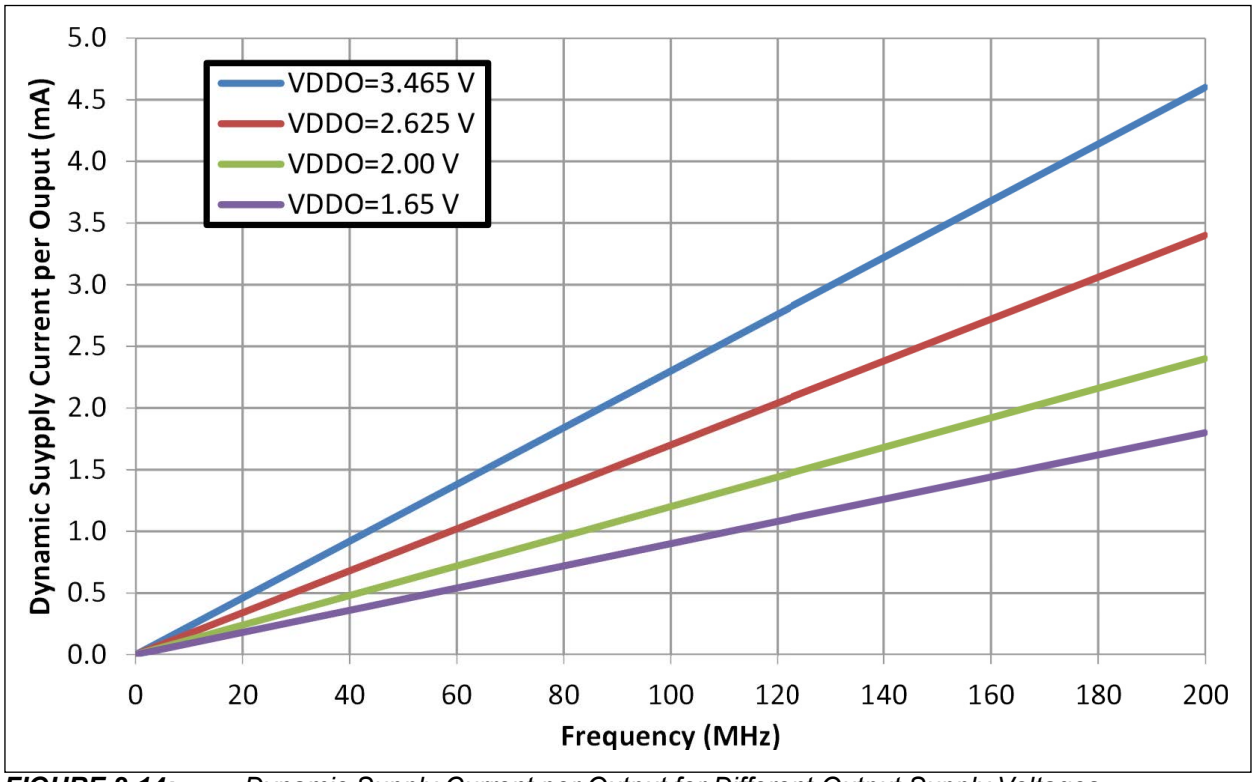


FIGURE 2-14: *Dynamic Supply Current per Output for Different Output Supply Voltages.*

2.6 Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board, each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Figure 2-15 shows the recommended decoupling for each power pin.

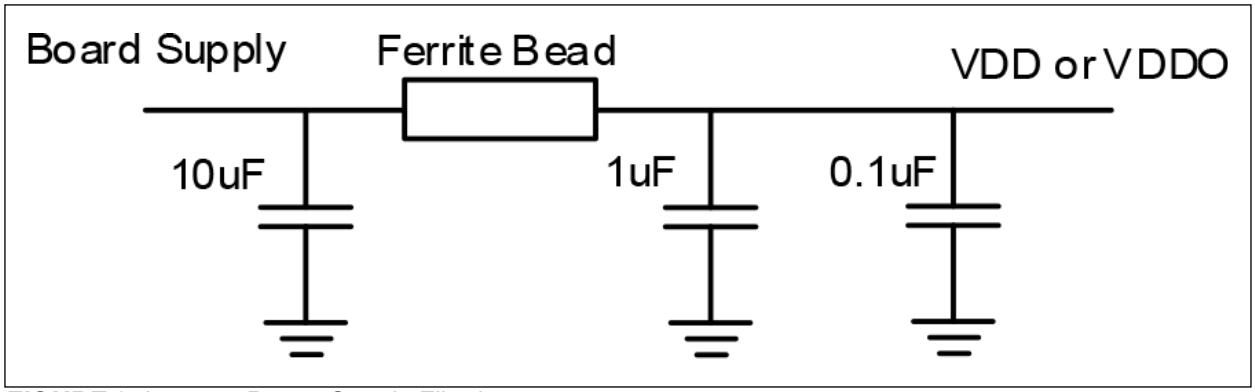


FIGURE 2-15: *Power Supply Filtering.*

2.7 Device Control

ZL30241 is controlled via Output Enable (OE) and Input Select (SEL0/1) input pins.

NOTES:

3.0 ELECTRICAL CHARACTERISTICS

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS (Note 1, Note 2, Note 3)

Parameter	Symbol	Min.	Max.	Units
Supply voltage, 3.3V	V_{DD}/V_{DDO}	–0.5	+4.6	V
Supply voltage, 2.5V	V_{DD}/V_{DDO}	–0.5	+4.6	V
Supply voltage, 1.8V	V_{DDO}	–0.5	+2.5	V
Supply voltage, 1.5V	V_{DDO}	–0.5	+2.0	V
Storage temperature range	T_{ST}	–55	+125.0	°C

Note 1: Exceeding these values may cause permanent damage.

2: Functional operation under these conditions is not implied.

3: Voltages are with respect to ground (GND) unless otherwise stated.

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS (Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage, 3.3V	V_{DD}/V_{DDO}	3.135	3.300	3.465	V
Supply voltage, 2.5V	V_{DD}/V_{DDO}	2.375	2.500	2.625	V
Supply voltage, 1.8V	V_{DDO}	1.600	1.800	2.000	V
Supply voltage, 1.5V	V_{DDO}	1.350	1.500	1.650	V
Operating temperature	T_A	–40.000	+25.000	+85.000	°C
Input voltage	V_{DD-IN}	–0.300	—	V_{DD} + 0.300	V

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.

2: The device supports two power supply modes (3.3V and 2.5V).

TABLE 3-3: CURRENT CONSUMPTION

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Static device current	$I_{S\_3.3V}$	—	15	18	mA	V_{DD} = 3.465V
	$I_{S\_2.5V}$	—	12	15	mA	V_{DD} = 2.625V
Device current with 25 MHz XTAL input	$I_{DD\_XTAL\_3.3V}$	—	24	27	mA	V_{DD} = 3.465V
	$I_{DD\_XTAL\_2.5V}$	—	18	20	mA	V_{DD} = 2.625V
Dynamic current per output (f = 100MHz), Note 1, Note 2 Needs to be scaled for different frequencies by f/100 MHz, Driving Strength = 1 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$	—	4.2	4.7	mA	V_{DD} = 3.465V
	$I_{DD\_2.5V}$	—	3.0	3.5	mA	V_{DD} = 2.625V
	$I_{DD\_1.8V}$	—	2.1	2.4	mA	V_{DD} = 2.000V
	$I_{DD\_1.5V}$	—	1.6	1.8	mA	V_{DD} = 1.650V
Dynamic current per output (f = 100MHz), Note 1, Note 2 Needs to be scaled for different frequencies by f/100 MHz, Driving Strength = 0 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$	—	2.3	3.0	mA	V_{DD} = 3.465V
	$I_{DD\_2.5V}$	—	1.7	1.8	mA	V_{DD} = 2.625V
	$I_{DD\_1.8V}$	—	1.2	1.3	mA	V_{DD} = 2.000V
	$I_{DD\_1.5V}$	—	0.9	1.0	mA	V_{DD} = 1.650V

Note 1: Needs to be scaled for different frequencies by f/100 MHz.

2: To calculate total power consumption use following formula: $P = (I_S + I_{DD\_XTAL}) \times V_{DD} + (I_{DDC} + I_{DD} \times n \times f/100\ MHz + V_{DDO} \times C_{LOAD} \times f \times n) \times V_{DDO}$, where I_{DD_XTAL}: should be set to zero if XTAL is not used or Is should be set to zero if XTAL is used. Also, n = number of active outputs; f = frequency of the clock; C_{LOAD} = capacitive load driven by an output.

3: This current is consumed by device whenever one or more outputs are enabled. It is independent of the number of active outputs.

TABLE 3-3: CURRENT CONSUMPTION (CONTINUED)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Common output current, Note 3	$I_{DD\_3.3V}$	—	3.8	8.0	mA	V_{DD} = 3.465V
	$I_{DD\_2.5V}$	—	1.9	3.3	mA	V_{DD} = 2.625V
	$I_{DD\_1.8V}$	—	1.2	1.7	mA	V_{DD} = 2.000V
	$I_{DD\_1.5V}$	—	1.0	1.4	mA	V_{DD} = 1.650V

Note 1: Needs to be scaled for different frequencies by f/100 MHz.

2: To calculate total power consumption use following formula: $P = (I_S + I_{DD\_XTAL}) \times V_{DD} + (I_{DDC} + I_{DD} \times n \times f/100\ MHz + V_{DDO} \times C_{LOAD} \times f \times n) \times V_{DDO}$, where I_{DD_XTAL}: should be set to zero if XTAL is not used or Is should be set to zero if XTAL is used. Also, n = number of active outputs; f = frequency of the clock; C_{LOAD} = capacitive load driven by an output.

3: This current is consumed by device whenever one or more outputs are enabled. It is independent of the number of active outputs.

TABLE 3-4: INPUT CHARACTERISTICS (Note 1, Note 2)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
CMOS high-level input voltage for SPI_CLK, SPI_CS and SPI_SDI	V_{CIH}	1.20	—	—	V	—
CMOS low-level input voltage for SPI_CLK, SPI_CS and SPI_SDI	V_{CIL}	—	—	0.45	V	—
CMOS input leakage current for SPI_CLK, SPI_CS and SPI_SDI, Note 3	I_{IL}	–40	—	10	µA	VI = VDD or 0 V
Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	0.5	—	V_{DD} – 0.85	V	—
Differential input voltage difference for IN0_p/n and IN1_p/n	V_{ID}	0.15	—	1.3	V	—
Differential input leakage current for IN0_p/n and IN1_p/n (includes current in pull-up and pull-down resistors), Note 4	I_{IL}	–200	—	100	µA	VI = VDD or 0 V
Single ended input high voltage for IN_0_p and IN_1_p	V_{SIH}	2	—	V_{DD} + 0.3	V	VDD = 3.3V+/-5%
		1.6	—	V_{DD} + 0.3	V	VDD = 2.5V+/-5%
Single ended input low voltage for IN_0_p and IN_1_p	V_{SIL}	–0.3	—	1.3	V	VDD = 3.3V+/-5%
		–0.3	—	0.9	V	VDD = 2.5V+/-5%
Input frequency	f_{IN}	0	—	200	MHz	—
Input duty cycle (200 MHz Input Clock)	DC	35	—	65	%	Note 5
Input slew rate	slew	—	2	—	V/ns	—
Input pull-up/pull-down resistance	R_{PU}/R_{PD}	—	60 kΩ	—	kΩ	—
Input pull-down resistance (INx_p)	R_{PD}	—	30 kΩ	—	kΩ	—

Note 1: Values are over recommended operating conditions.

2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

3: CMOS input leakage is due to 300 kΩ pull-up/pull-down resistors.

4: Differential input leakage is due to 60 kΩ pull-up/pull-down resistors INx_n and due to 30 kΩ pull-down resistor for INx_p.

5: Minimum and maximum duty cycles should be scaled for different input frequencies. For example, a 10 MHz input clock would have the minimum duty cycle of 2% and the maximum duty cycle of 98%.

TABLE 3-5: CRYSTAL OSCILLATOR CHARACTERISTICS (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Mode of oscillation	mode	Fundamental			—	—
Frequency	f	8	—	160	MHz	—
On chip shunt resistor	R	—	0.5	—	MΩ	—
On chip capacitance	C	—	12	—	pF	—
Frequency in overdrive mode, Note 2	f_{OV}	0.1	—	200	MHz	Functional but may not meet AC parameters. Minimum depends on AC coupling. Capacitor (0.1 uF assumed).
Frequency in bypass mode, Note 3	f_{BP}	—	—	200	MHz	Functional but may not meet AC parameters.

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

2: Maximum input level is 2.0V.

3: Maximum output level is V_{DD}.

TABLE 3-6: LVCMOS OUTPUT CHARACTERISTICS (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output high voltage	V_{OH}	0.8 × V_{DDO}	—	—	V	V_{DDO} = 3.3V±5%
		0.8 × V_{DDO}	—	—	V	V_{DDO} = 2.5V±5%
		0.7 × V_{DDO}	—	—	V	V_{DDO} = 1.8V±10%
		0.7 × V_{DDO}	—	—	V	V_{DDO} = 1.5V±10%
Output low voltage	V_{OL}	—	—	0.2 × V_{DDO}	V	V_{DDO} = 3.3V±5%
		—	—	0.2 × V_{DDO}	V	V_{DDO} = 2.5V±5%
		—	—	0.3 × V_{DDO}	V	V_{DDO} = 1.8V±10%
		—	—	0.3 × V_{DDO}	V	V_{DDO} = 1.5V±10%
Output impedance	R_O	—	17	—	Ω	V_{DDO} = 3.3V
		—	21	—	Ω	V_{DDO} = 2.5V
		—	30	—	Ω	V_{DDO} = 1.8V
		—	42	—	Ω	V_{DDO} = 1.5V
Output slew rate, rise or fall (20% to 80%)	t_r, t_f	3.19	5.14	6.33	V/ns	V_{DDO} = 3.3V±5%
		1.72	3.74	4.61	V/ns	V_{DDO} = 2.5V±5%
		1.64	2.52	3.32	V/ns	V_{DDO} = 1.8V±10%
		1.20	1.96	2.54	V/ns	V_{DDO} = 1.5V±10%
Output frequency	F_O	0	—	200	MHz	—
Output duty cycle		50.26	—	53.18	%	Input. duty-cycle 50%
Output enable or disable time		—	—	2	cycle	—
Output to output skew	t_{OOSK}	—	—	27	ps	—
Device-to-device output skew	t_{DOOSK}	—	—	1.6	ns	—
Input to output delay	t_{IOD}	1.15	2.09	2.54	ns	VDD = 3.3V
		1.57	2.27	2.77	ns	VDD = 2.5V
Input multiplexer isolation	ISO	75	—	—	dB	Tested with 125 MHz clocks

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V). Load 50Ω to V_{DDO}/2.

TABLE 3-7: LVCMOS OUTPUT ADDITIVE JITTER AND PHASE NOISE (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
System level additive jitter, Note 2		—	17	—	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, single ended input
		—	31	—	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, single ended input
		—	22	—	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, differential input
		—	37	—	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, differential input
Additive jitter, Note 3, Note 4		—	45.18	93.11	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, single ended input
		—	80.46	126.92	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, single ended input
		—	39.95	68.98	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, differential input
		—	67.18	117.26	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, differential input
Phase noise floor (VDD = 3.3V, VDDO = 3.3V)		—	–145.08	–138.67	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–152.46	–145.82	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–160.67	–155.66	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–162.66	–160.55	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–162.71	–160.19	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input
		—	–145.34	–137.83	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–152.60	–146.93	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–161.06	–156.99	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–163.22	–160.84	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–163.38	–161.42	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

2: System level additive jitter is calculated as $J_{RMS\_SYS\_AJ} = J_{RMS\_OUT} - J_{RMS\_IN}$.

3: Additive jitter is calculated as $J_{RMS\_\_AJ} = \text{sqrt}\ (J_{RMS\_OUT}^2 - J_{RMS\_IN}^2)$ where jitter is integrated in 12 kHz to 20 MHz band.

4: Tester measures jitter at 156.25 MHz. Since this frequency won't appear in the data sheet, it should be removed from the PPGT. Data sheet jitter is guaranteed by lab char. The ATE jitter measurement will be used to screen outliers only, with limits based on ATE distribution.

TABLE 3-7: LVCMOS OUTPUT ADDITIVE JITTER AND PHASE NOISE (Note 1) (CONTINUED)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Phase noise floor (VDD = 2.5V, VDDO = 2.5V)		—	–139.93	–134.59	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–147.22	–144.21	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–157.11	–154.78	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–160.58	–158.21	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–160.78	–158.19	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input
		—	–141.69	–134.26	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–149.19	–144.73	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–158.66	–156.22	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–161.60	–159.32	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–161.85	–159.36	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

2: System level additive jitter is calculated as $J_{RMS\_SYS\_AJ} = J_{RMS\_OUT} - J_{RMS\_IN}$.

3: Additive jitter is calculated as $J_{RMS\_\_AJ}$ = sqrt ($J_{RMS\_OUT}^2$ - $J_{RMS\_IN}^2$) where jitter is integrated in 12 kHz to 20 MHz band.

4: Tester measures jitter at 156.25 MHz. Since this frequency won't appear in the data sheet, it should be removed from the PPGT. Data sheet jitter is guaranteed by lab char. The ATE jitter measurement will be used to screen outliers only, with limits based on ATE distribution.

TABLE 3-8: LVCMOS OUTPUT JITTER PHASE NOISE WITH 25 MHZ XTAL (NOTE 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 20 MHz band		—	72.63	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	87.59	—	fs	V_{DD} = 2.5V; V_{DDO} = 2.5V
Phase noise floor		—	–75.96	—	dBc/Hz	@10 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–107.50	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–132.34	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–157.36	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–165.82	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–168.85	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–168.88	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–70.52	—	dBc/Hz	@10 Hz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–102.60	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–129.14	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–153.93	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–164.00	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–167.34	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–167.41	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V; V_{DDO} = 2.5V

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V). XTAL frequency is 25 MHz.

TABLE 3-9: 5 MM × 5 MM VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Conditions	Value	Units
Maximum ambient temperature	T_A	—	85	°C
Maximum junction temperature	$T_{J(MAX)}$	—	125	°C
Junction to ambient thermal resistance, Note 1	θ_{JA}	Still air	26.8	°C/W
		1 m/s airflow	21.8	°C/W
		2.5 m/s airflow	19.9	°C/W
Junction to board thermal resistance	θ_{JB}	—	10.8	°C/W
Junction to case thermal resistance	θ_{JC}	—	19.5	°C/W
Junction to pad thermal resistance, Note 2	θ_{JP}	Still air	6.5	°C/W
Junction to top-center thermal characterization parameter	ψ_{JT}	Still air	0.6	°C/W

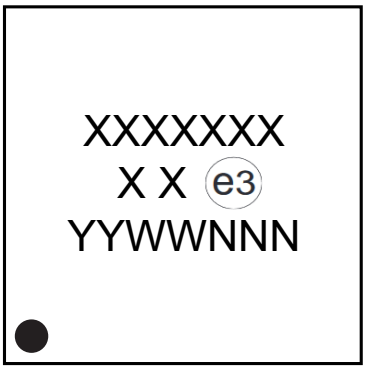
Note 1: θ_{JA} is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power.

2: θ_{JP} is the thermal resistance from junction to the center exposed pad on the bottom of the package.

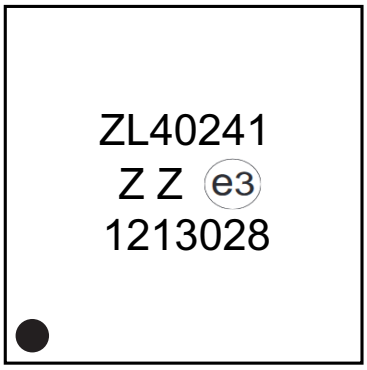
4.0 PACKAGE OUTLINE

4.1 Package Marking Information

32-Lead QFN*



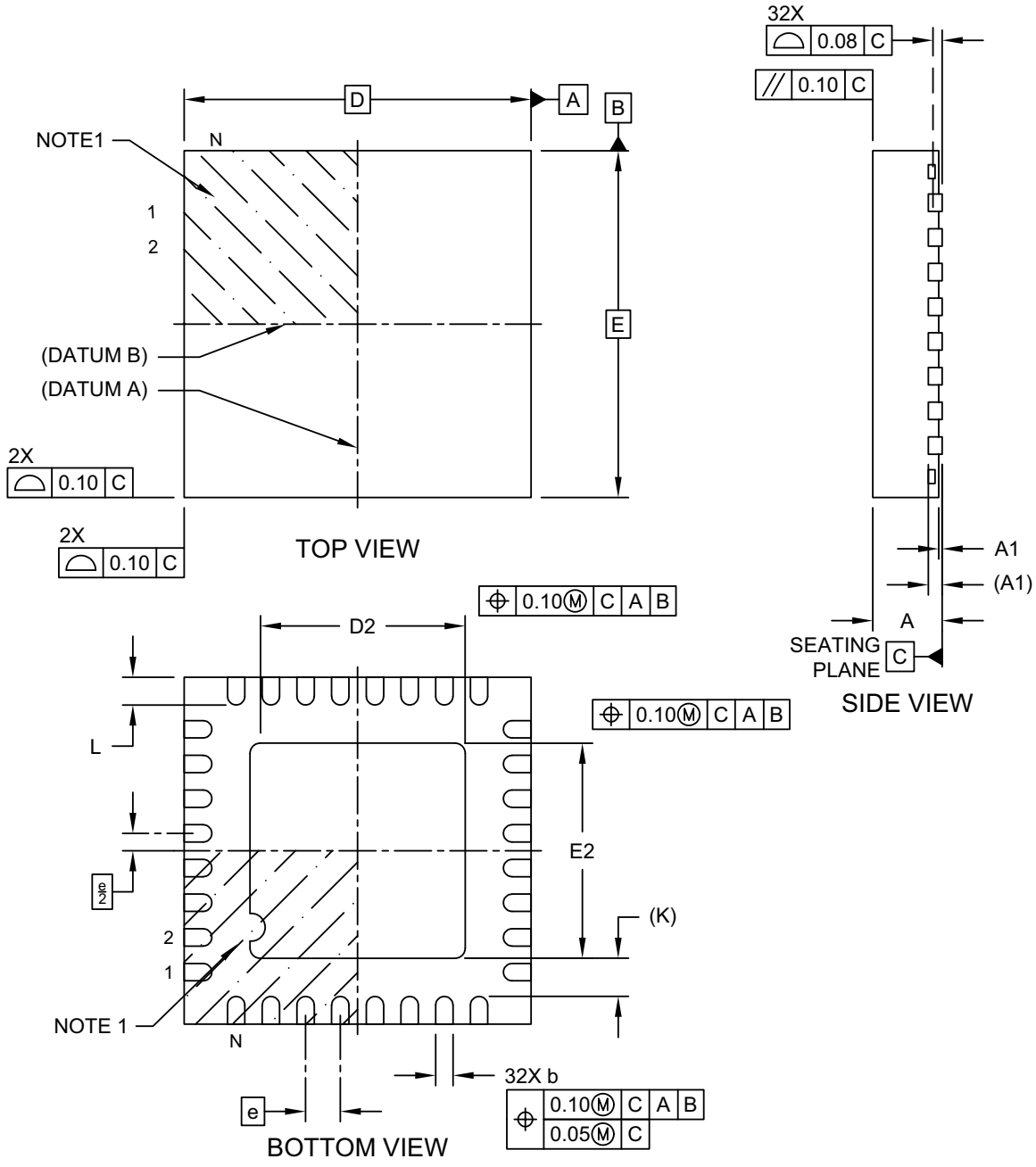
Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

32-Lead 5 mm x 5 mm VQFN Package Outline and Recommended Land Pattern

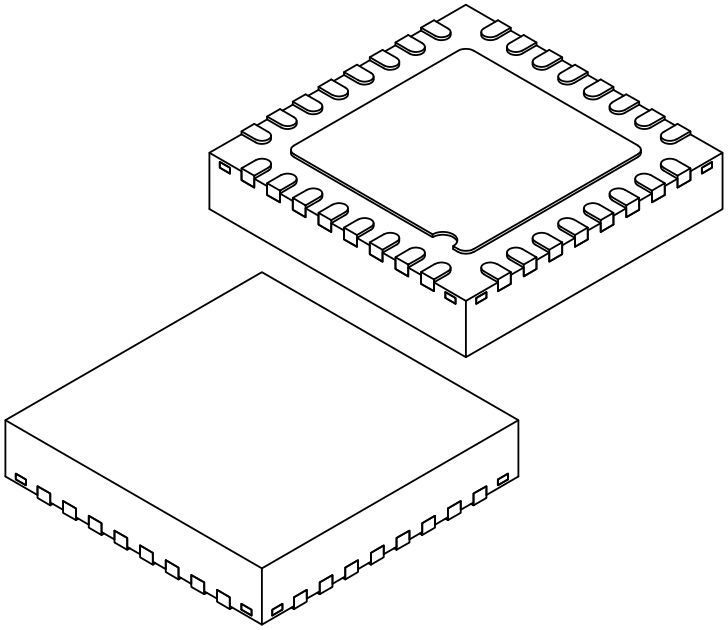
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25400 Rev A Sheet 1 of 2

32-Lead 5 mm x 5 mm VQFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.00	3.10	3.20
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.00	3.10	3.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	–	–

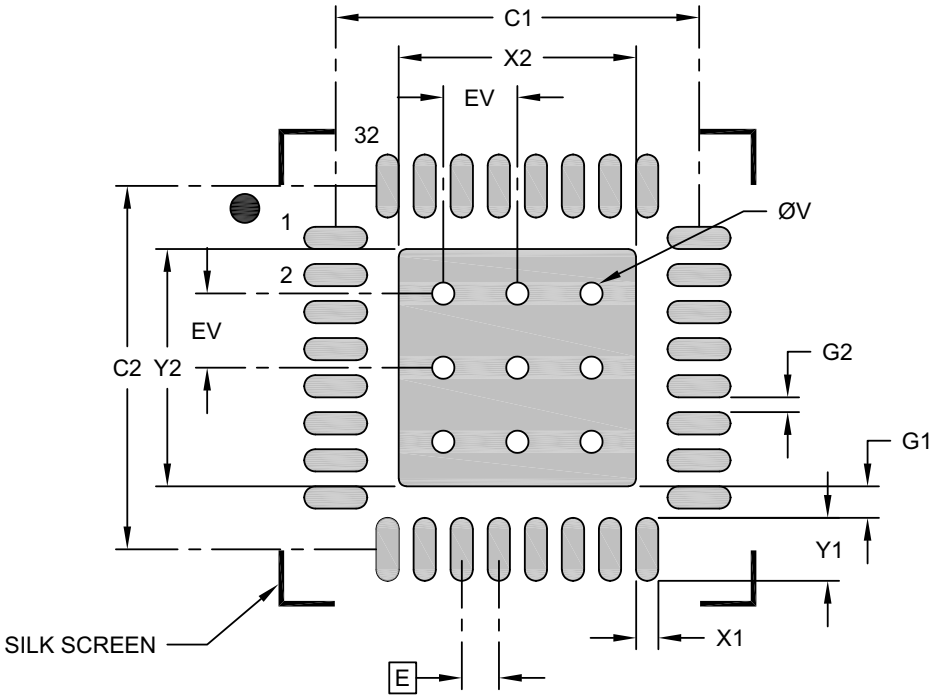
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25400 Rev A Sheet 2 of 2

32-Lead 5 mm x 5 mm VQFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.20
Optional Center Pad Length	Y2			3.20
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27400 Rev A

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006783A (11-2023)	Various	Converted Microsemi data sheet ZL40241 to Microchip DS20006783A. Updated Figure 2-9 as requested by Applications. Minor text changes throughout.
DS20006783B (02-2025)	Table 3-4	Updated input duty cycle row and added note 5 to Table 3-4.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL40241: Ten LVCMOS Output Low Additive Jitter Fanout Buffer
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 32-Lead 5 mm x 5 mm VQFN
Media Type:	G = 490/Tray F = 4,000/Reel
Finish:	1 = Pb Free with Matte Sn Lead Finish, RoHS e3 Compliant

Examples:

a) ZL40241LDG1:

Ten LVCMOS Output Low Additive Jitter Fanout Buffer, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 490/Tray, Pb Free with Matte Sn Lead Finish, RoHS e3 Compliant

b) ZL40241LDF1:

Ten LVCMOS Output Low Additive Jitter Fanout Buffer, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 4,000/Reel, Pb Free with Matte Sn Lead Finish, RoHS e3 Compliant

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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