

## Features

### Inputs/Outputs

- Accepts differential or single-ended input
  - LVPECL, LVDS, CML, HCSL, LVCMOS
- Two precision LVDS outputs
- Operating frequency up to 750 MHz

### Power

- Options for 2.5 V or 3.3 V power supply
- Current consumption of 44 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply noise rejection

### Performance

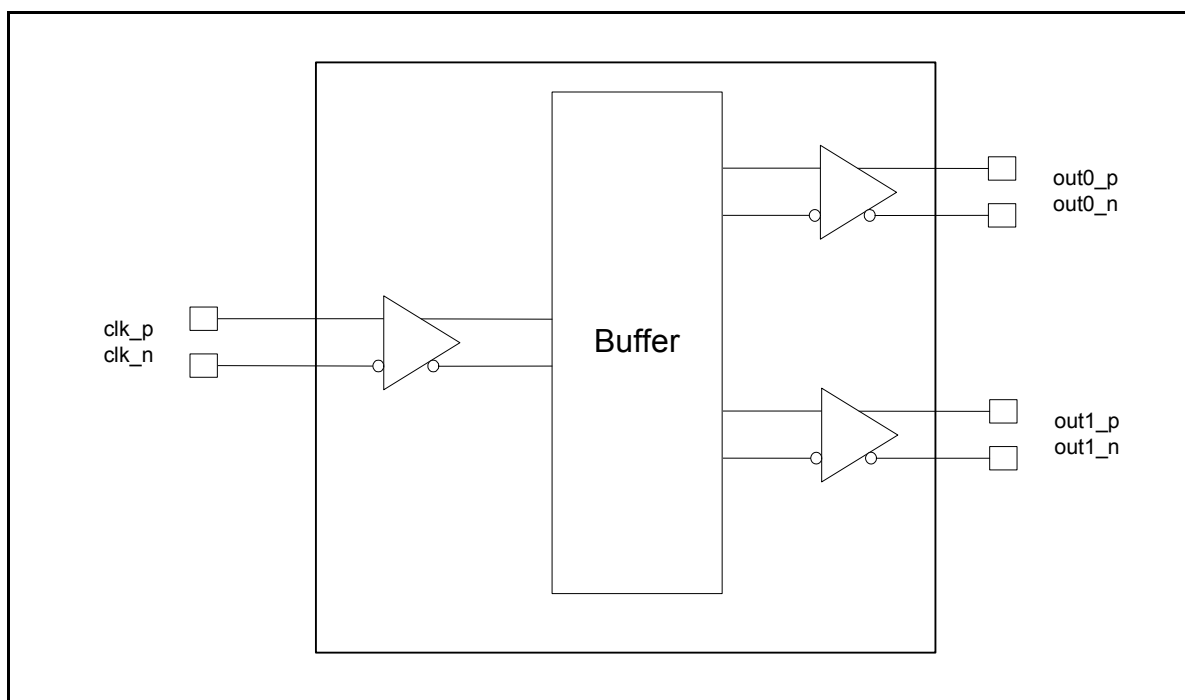
- Ultra low additive jitter of 92 fs RMS

## Ordering Information

|                        |            |               |
|------------------------|------------|---------------|
| ZL40212LDG1            | 16 Pin QFN | Trays         |
| ZL40212LDF1            | 16 Pin QFN | Tape and Reel |
| Matte Tin              |            |               |
| Package size: 3 x 3 mm |            |               |
| -40°C to +85°C         |            |               |

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- Wireless communications
- High performance micro-processor clock distribution



**Figure 1 - Functional Block Diagram**

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## 1.0 Package Description

The device is packaged in a 16 pin QFN

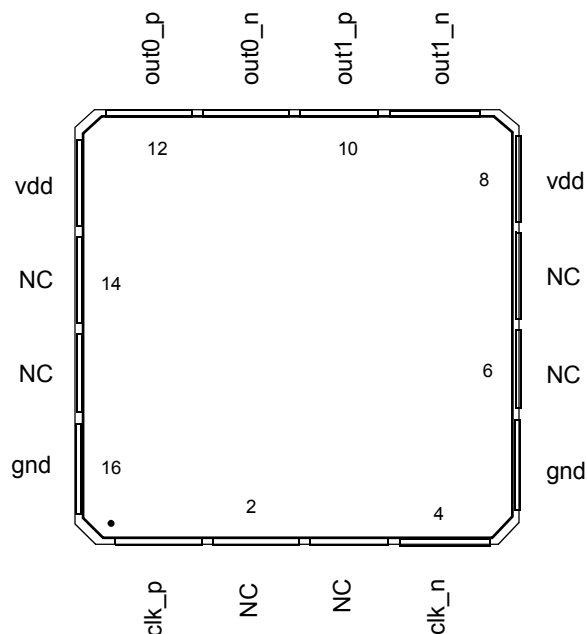


Figure 2 - Pin Connections

## 2.0 Pin Description

| Pin #                    | Name                             | Description                                                                                                                                              |
|--------------------------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 4                     | clk_p, clk_n,                    | <b>Differential Input (Analog Input).</b> Differential (or singled ended) input signals. For all input signal configuration see "Clock Inputs" on page 5 |
| 12, 11,<br>10, 9         | out0_p, out0_n<br>out1_p, out1_n | <b>Differential Output (Analog Output).</b> Differential outputs.                                                                                        |
| 8, 13                    | vdd                              | <b>Positive Supply Voltage.</b> 2.5 V <sub>DC</sub> or 3.3 V <sub>DC</sub> nominal.                                                                      |
| 5, 16                    | gnd                              | <b>Ground.</b> 0 V.                                                                                                                                      |
| 2, 3,<br>6, 7,<br>14, 15 | NC                               | <b>No Connection.</b> Leave unconnected.                                                                                                                 |

### 3.0 Functional Description

The ZL40212 is an LVDS clock fanout buffer with two identical output clock drivers capable of operating at frequencies up to 750MHz.

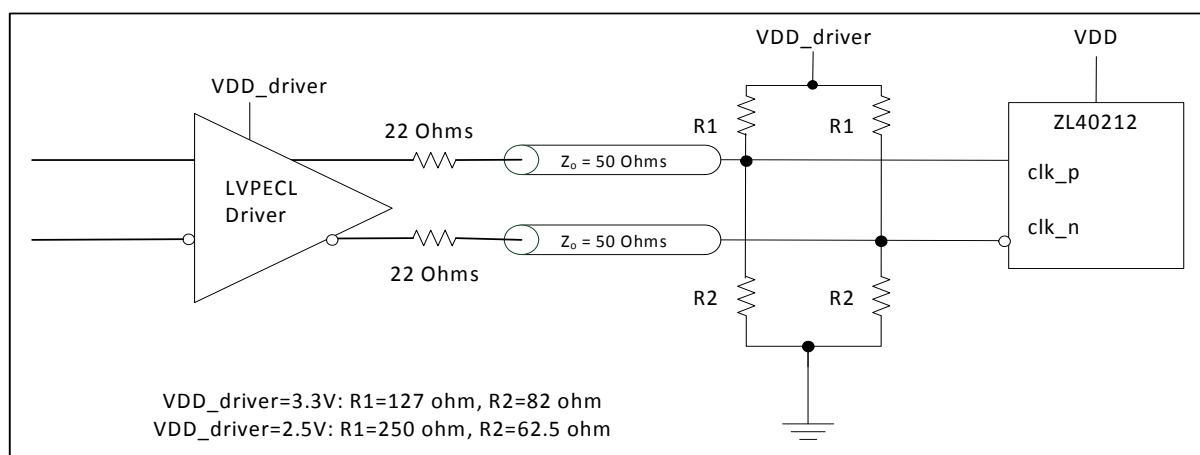
Inputs to the ZL40212 are externally terminated to allow use of precision termination components and to allow full flexibility of input termination. The ZL40212 can accept DC or AC coupled LVPECL, LVDS, CML or HCSL input signals; single ended input signals can also be accepted. A pin compatible device with internal termination is also available.

The ZL40212 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V $\pm$ 5% or 3.3V $\pm$ 5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

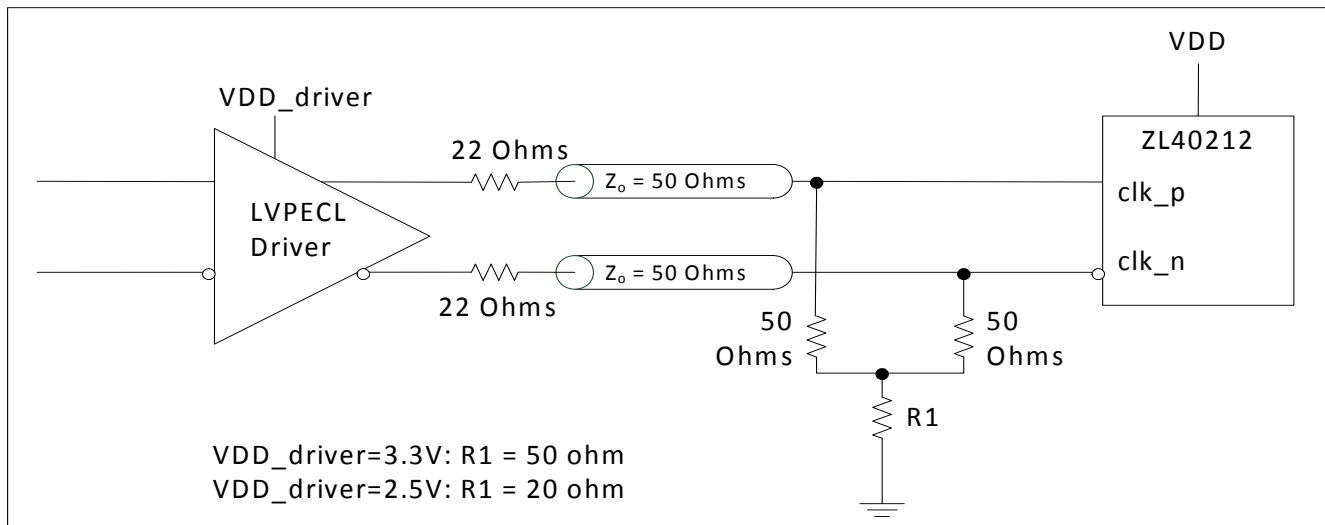
The device block diagram is shown in Figure 1; its operation is described in the following sections.

#### 3.1 Clock Inputs

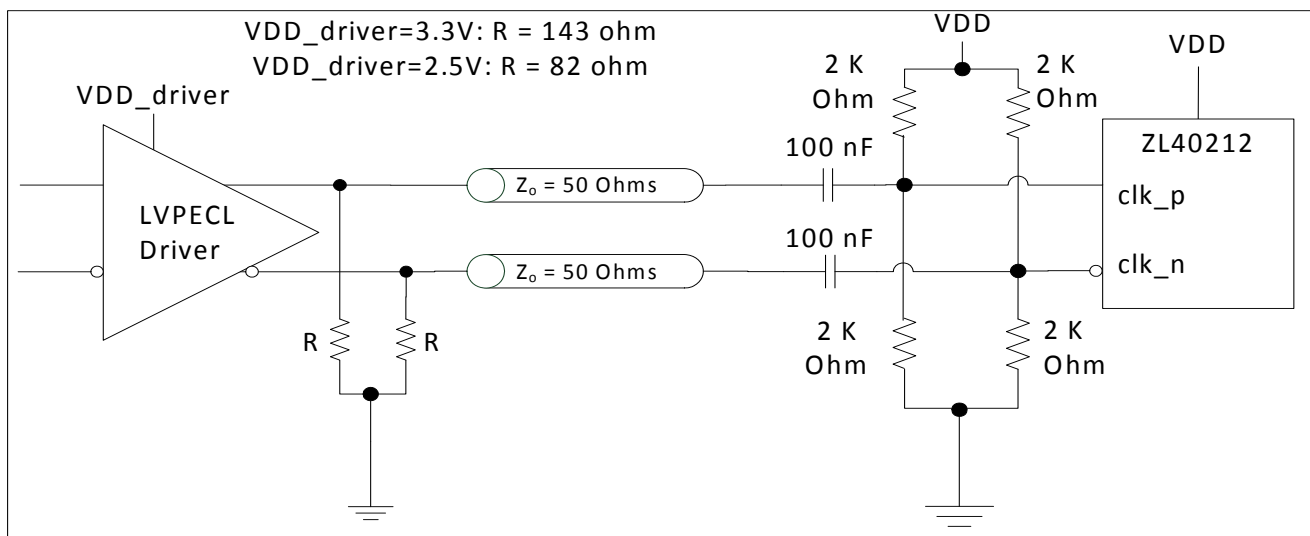
The ZL40212 is adaptable to support different types of differential and single-ended input signals depending on the passive components used in the input termination. The application diagrams in the following figures allow the ZL40212 to accept LVPECL, LVDS, CML, HCSL and single-ended inputs.



**Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent**



**Figure 4 - LVPECL Input DC Coupled Parallel Termination**



**Figure 5 - LVPECL Input AC Coupled Termination**

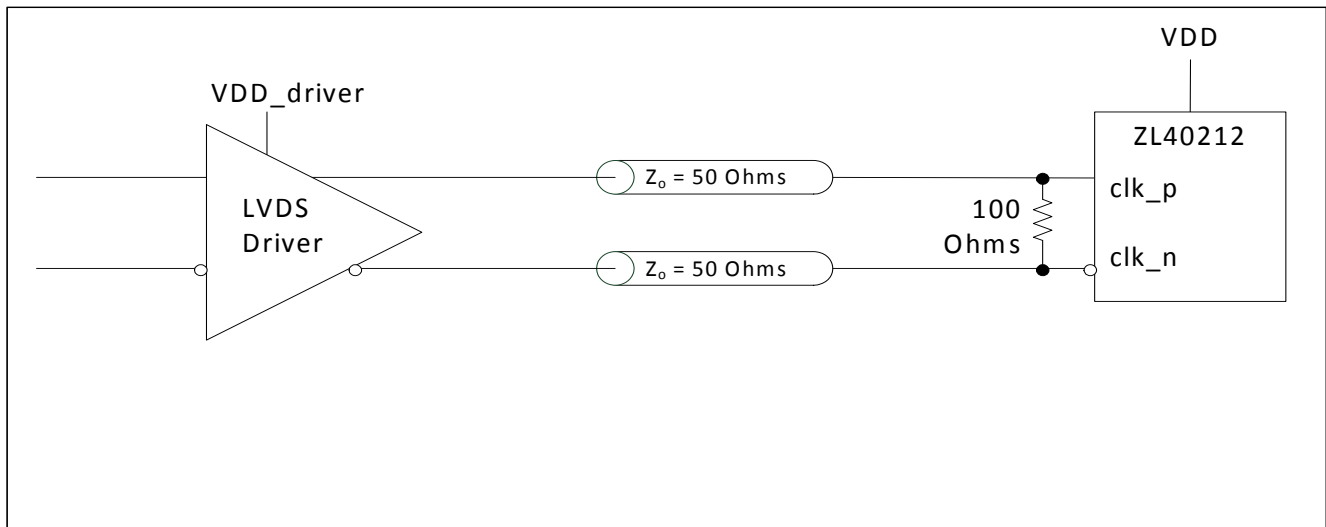


Figure 6 - LVDS Input DC Coupled

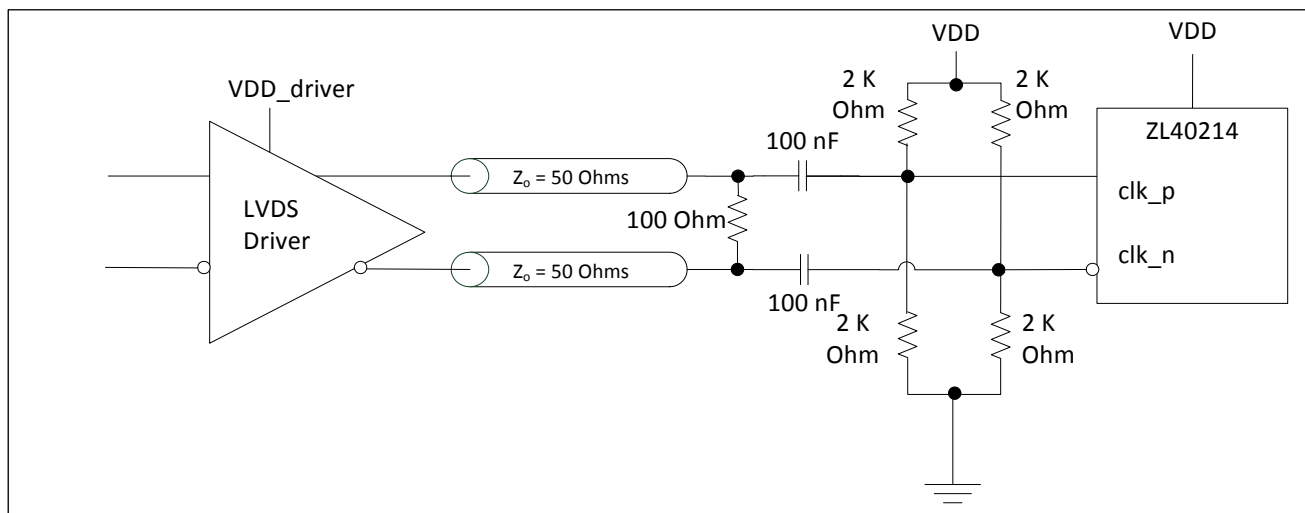


Figure 7 - LVDS Input AC Coupled

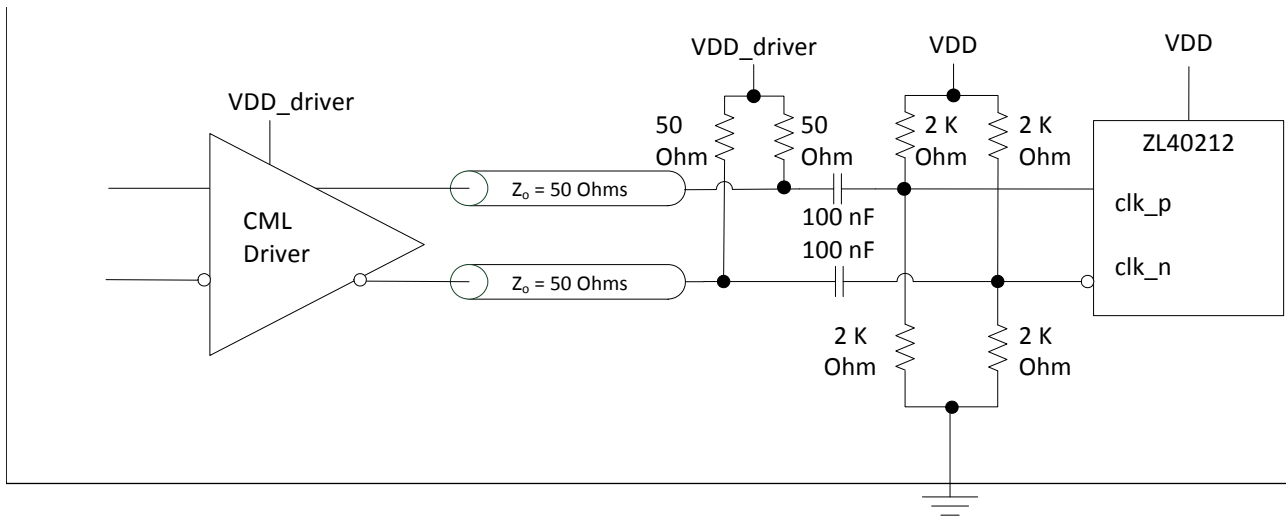


Figure 8 - CML Input AC Coupled

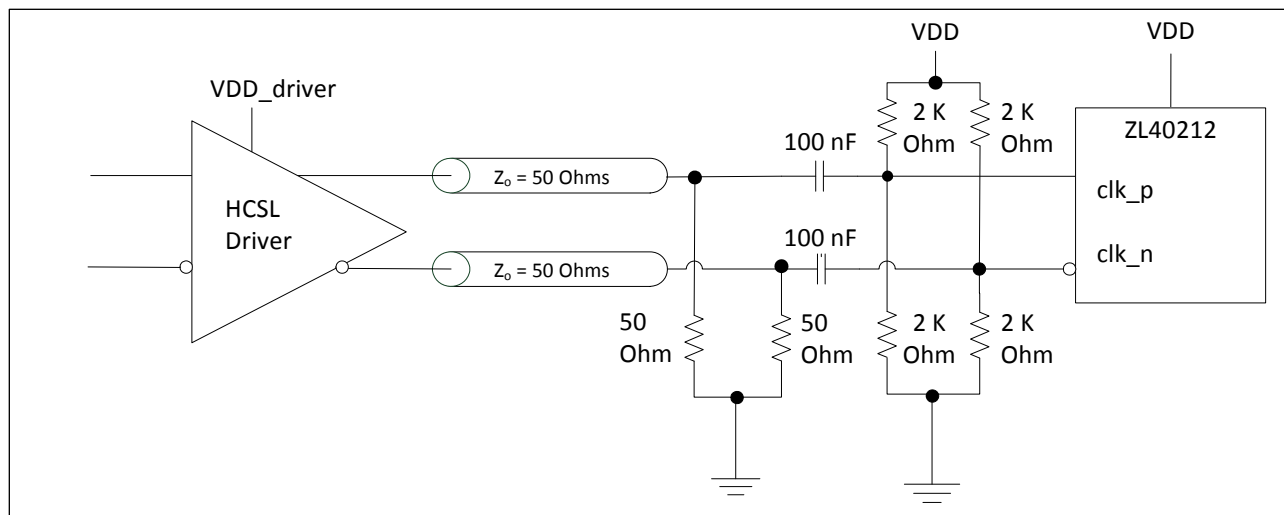
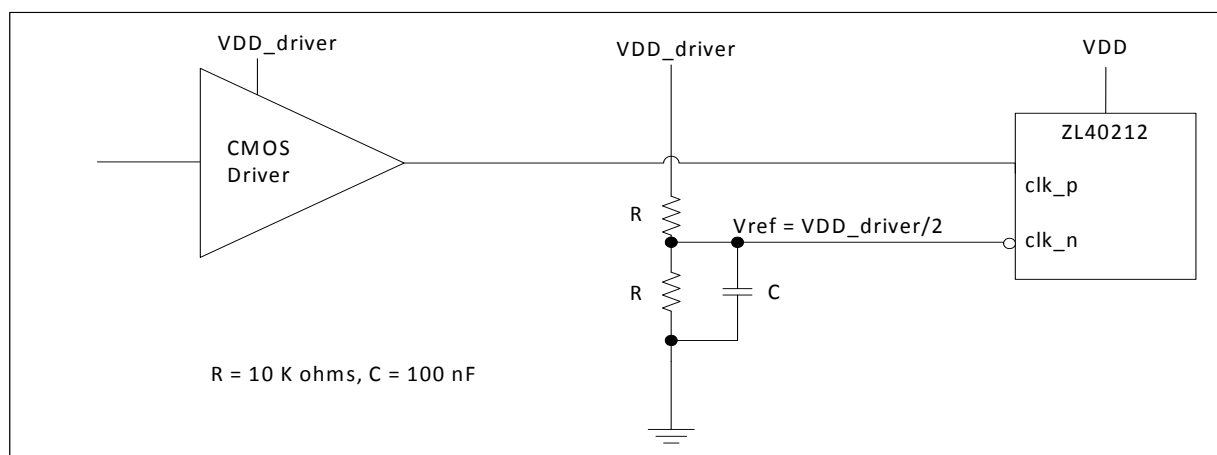
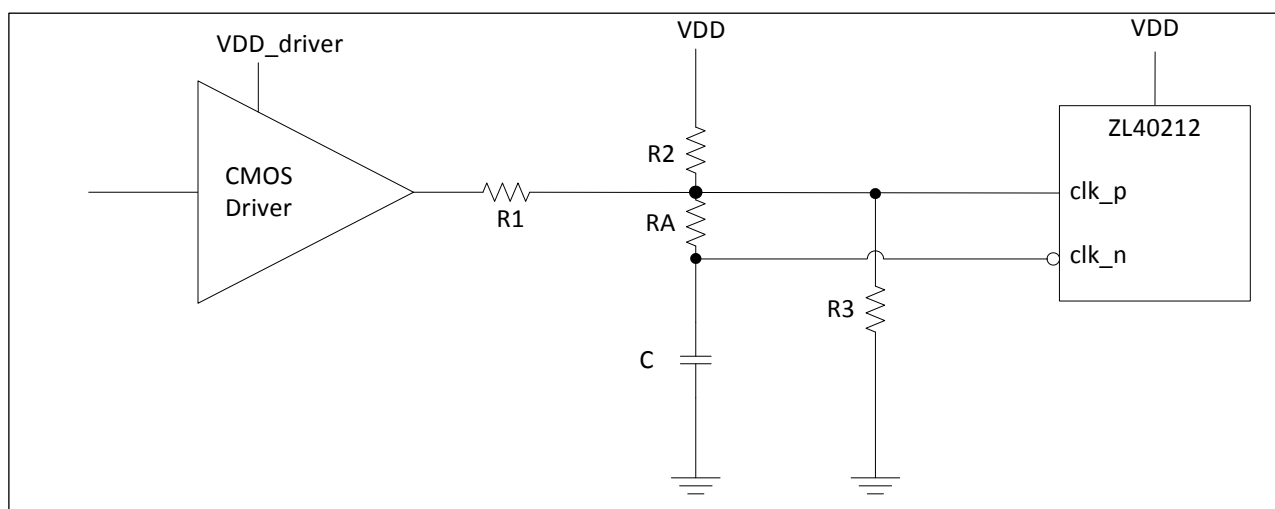


Figure 9 - HCSL Input AC Coupled





**Figure 10 - CMOS Input DC Coupled Referenced to  $VDD/2$**



**Figure 11 - CMOS Input DC Coupled Referenced to Ground**

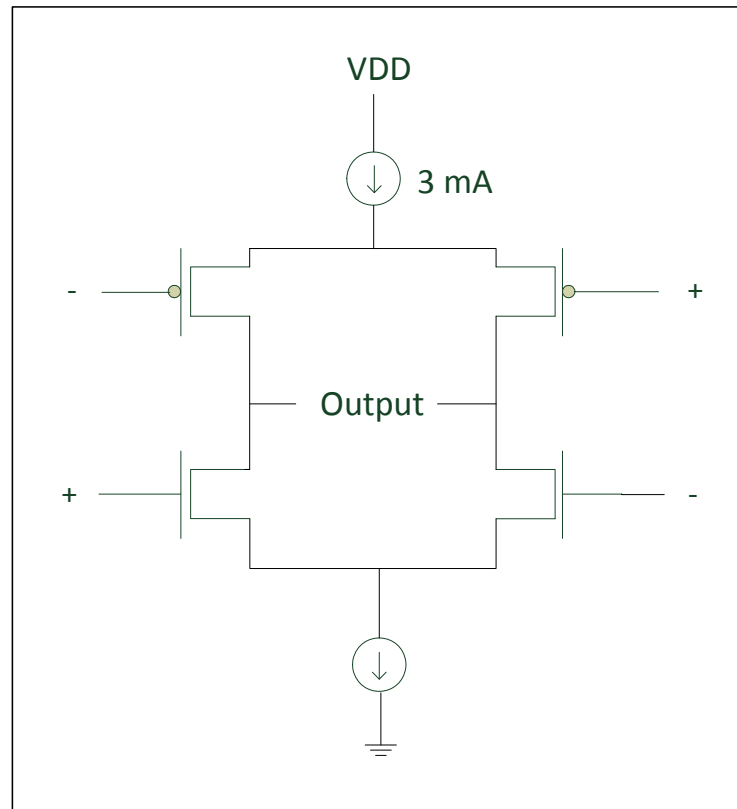
| VDD_driver | R1 (kΩ) | R2 (kΩ) | R3 (kΩ) | RA (kΩ) | C (pF) |
|------------|---------|---------|---------|---------|--------|
| 1.5        | 1.25    | 3.075   | open    | 10      | 10     |
| 1.8        | 1       | 3.8     | open    | 10      | 10     |
| 2.5        | 0.33    | 4.2     | open    | 10      | 10     |
| 3.3        | 0.75    | open    | 4.2     | 10      | 10     |

**Table 1 - Component Values for Single Ended Input Reference to Ground**

\* For frequencies below 100 MHz, increase C to avoid signal integrity issues.

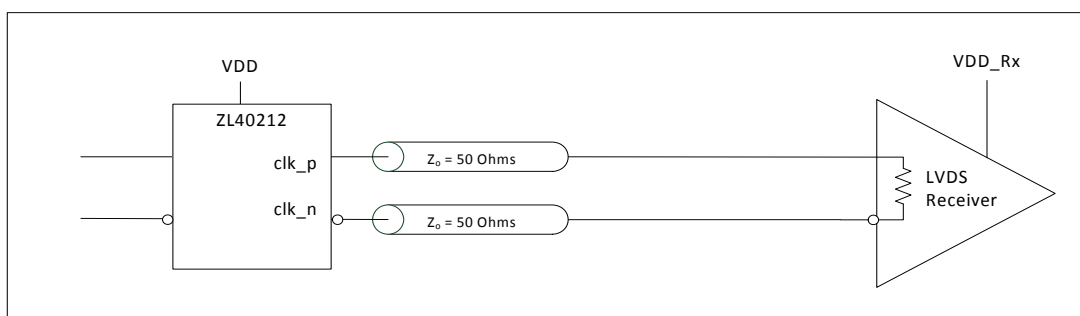
### 3.2 Clock Outputs

LVDS has lower signal swing than LVPECL which results in a low power consumption. A simplified diagram for the LVDS output stage is shown in Figure 12.

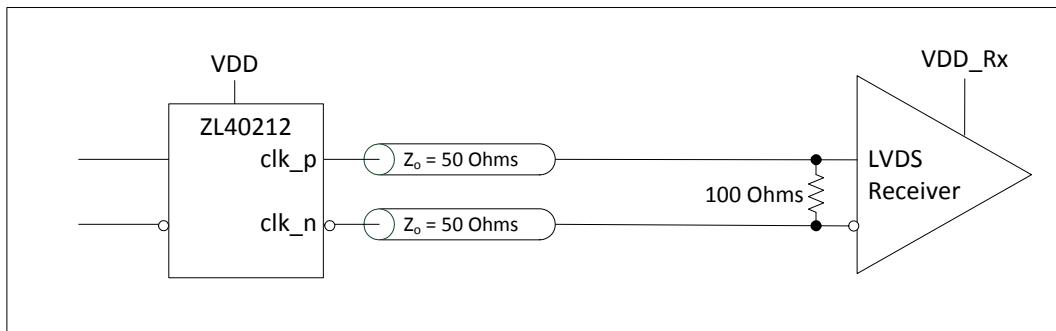


**Figure 12 - Simplified LVDS Output Driver**

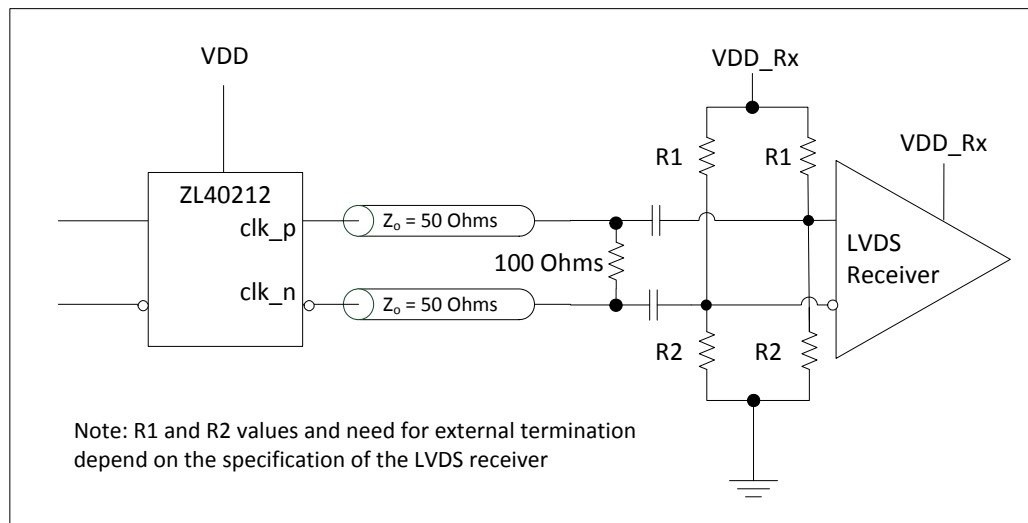
The methods to terminate the ZL40212 drivers are shown in the following figures.



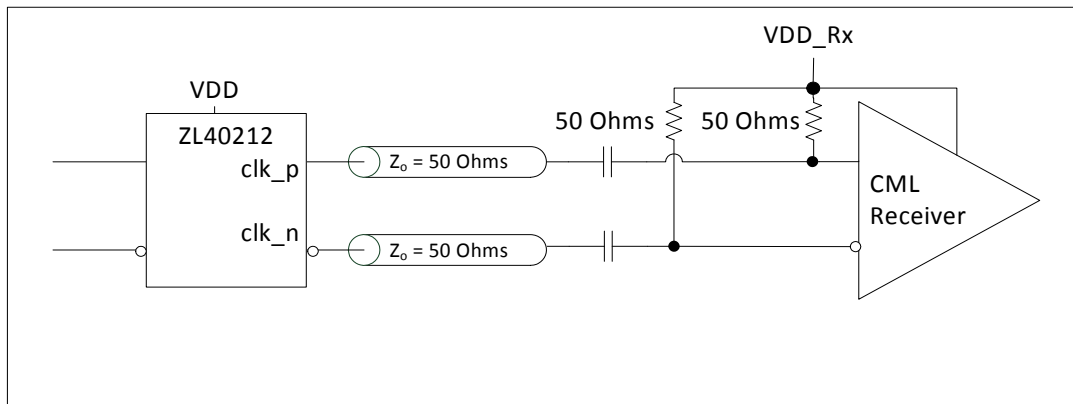
**Figure 13 - LVDS DC Coupled Termination (Internal Receiver Termination)**



**Figure 14 - LVDS DC Coupled Termination (External Receiver Termination)**



**Figure 15 - LVDS AC Coupled Termination**

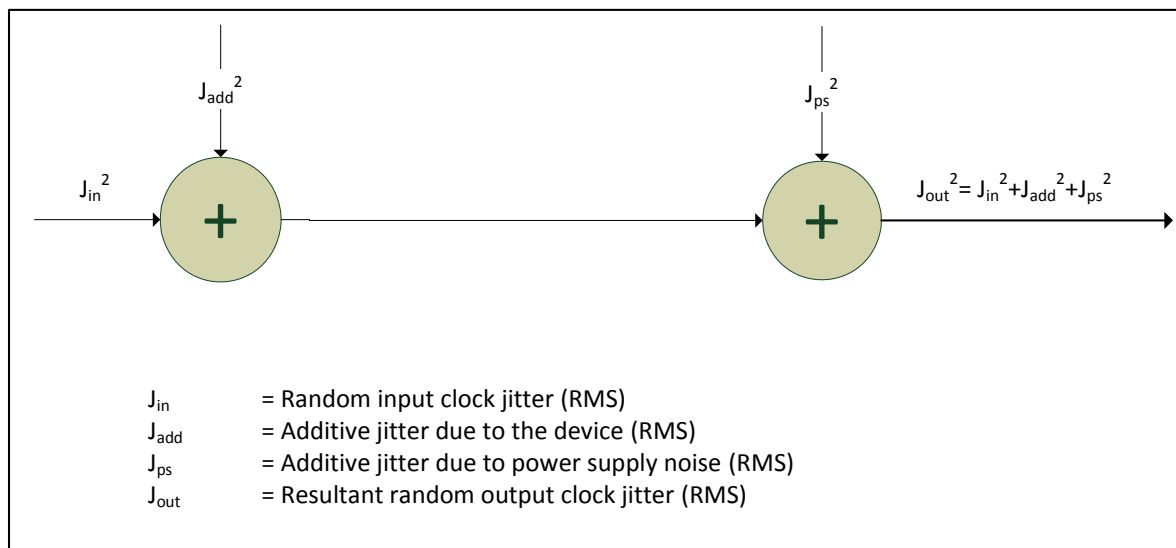


**Figure 16 - LVDS AC Output Termination for CML Inputs**

### 3.3 Device Additive Jitter

The ZL40212 clock fanout buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40212 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40212 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources, but they are not shown in Figure 17.



**Figure 17 - Additive Jitter**

### 3.4 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

#### 3.4.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40212 is equipped with a low drop out (LDO) power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The LDO regulator on the ZL40212 allows this device to have superior performance even in the presence of external noise sources. The on-chip measures in combination with the simple recommended power supply filtering and PCB layout minimize the additive jitter from power supply noise.

The performance of these clock buffers in the presence of power supply noise is detailed in ZLAN-403, "Power Supply Rejection in Clock Buffers" which is available from Applications Engineering.

#### 3.4.2 Power supply filtering

For optimal jitter performance, the device should be isolated from the power planes connected to its power supply pins as shown in Figure 18.

- 10  $\mu$ F capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1  $\mu$ F capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins
- a 0.3 ohm resistor is recommended for the filter shown in Figure 18

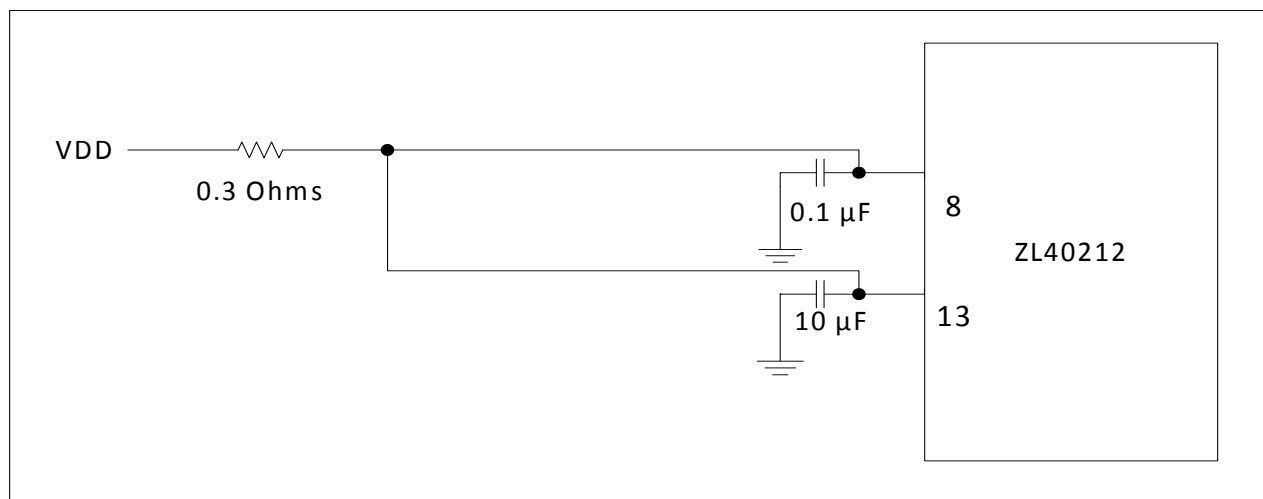


Figure 18 - Decoupling Connections for Power Pins

#### 3.4.3 PCB layout considerations

The power nets in Figure 18 can be implemented either as a plane island or routed power topology without changing the overall jitter performance of the device.

## 4.0 AC and DC Electrical Characteristics

### Absolute Maximum Ratings\*

|   | Parameter                  | Sym.        | Min. | Max.     | Units |
|---|----------------------------|-------------|------|----------|-------|
| 1 | Supply voltage             | $V_{DD\_R}$ | -0.5 | 4.6      | V     |
| 2 | Voltage on any digital pin | $V_{PIN}$   | -0.5 | $V_{DD}$ | V     |
| 3 | Soldering temperature      | T           |      | 260      | °C    |
| 4 | Storage temperature        | $T_{ST}$    | -55  | 125      | °C    |
| 5 | Junction temperature       | $T_j$       |      | 125      | °C    |
| 6 | Voltage on input pin       | $V_{input}$ |      | $V_{DD}$ | V     |
| 7 | Input capacitance each pin | $C_p$       |      | 500      | fF    |

\* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

\* Voltages are with respect to ground (GND) unless otherwise stated

### Recommended Operating Conditions\*

|   | Characteristics           | Sym.       | Min.  | Typ. | Max.  | Units |
|---|---------------------------|------------|-------|------|-------|-------|
| 1 | Supply voltage 2.5 V mode | $V_{DD25}$ | 2.375 | 2.5  | 2.625 | V     |
| 2 | Supply voltage 3.3 V mode | $V_{DD33}$ | 3.135 | 3.3  | 3.465 | V     |
| 3 | Operating temperature     | $T_A$      | -40   | 25   | 85    | °C    |

\* Voltages are with respect to ground (GND) unless otherwise stated

### DC Electrical Characteristics - Current Consumption

|   | Characteristics                                               | Sym.           | Min. | Typ. | Max. | Units | Notes |
|---|---------------------------------------------------------------|----------------|------|------|------|-------|-------|
| 1 | Supply current LVDS drivers - loaded (all outputs are active) | $I_{dd\_load}$ |      | 44   |      | mA    |       |

### DC Electrical Characteristics - Inputs and outputs - for 2.5/3.3 V supply

|   | Characteristics                                    | Sym.      | Min. | Typ. | Max.  | Units | Notes     |
|---|----------------------------------------------------|-----------|------|------|-------|-------|-----------|
| 1 | LVDS Differential input common mode supply voltage | $V_{ICM}$ | 1.1  |      | 1.6   | V     | for 2.5 V |
| 2 | LVDS Differential input common mode supply voltage | $V_{ICM}$ | 1.1  |      | 2.0   | V     | for 3.3 V |
| 3 | LVDS Differential input voltage                    | $V_{ID}$  | 0.25 |      | 1     | V     |           |
| 4 | LVDS output differential voltage*                  | $V_{OD}$  | 0.25 | 0.30 | 0.40  | V     |           |
| 5 | LVDS output common mode voltage                    | $V_{CM}$  | 1.1  | 1.25 | 1.375 | V     |           |

\* The VOD parameter was measured from 125 to 750 MHz.



Figure 19 - Differential Output Voltage Parameter

AC Electrical Characteristics\* - Inputs and Outputs (see Figure 20) - for 2.5/3.3 V supply.

|   | Characteristics                         | Sym.              | Min. | Typ. | Max. | Units   | Notes |
|---|-----------------------------------------|-------------------|------|------|------|---------|-------|
| 1 | Maximum Operating Frequency             | $1/t_p$           |      |      | 750  | MHz     |       |
| 2 | input to output clock propagation delay | $t_{pd}$          | 0    | 1    | 2    | ns      |       |
| 3 | output to output skew                   | $t_{out2out}$     |      | 50   | 100  | ps      |       |
| 4 | part to part output skew                | $t_{part2part}$   |      | 80   | 300  | ps      |       |
| 5 | Output clock Duty Cycle degradation     | $t_{PWH}/t_{PWL}$ | -5   | 0    | 5    | Percent |       |
| 6 | LVDS Output clock slew rate             | $r_{sl}$          | 0.55 |      |      | V/ns    |       |

\* Supply voltage and operating temperature are as per Recommended Operating Conditions

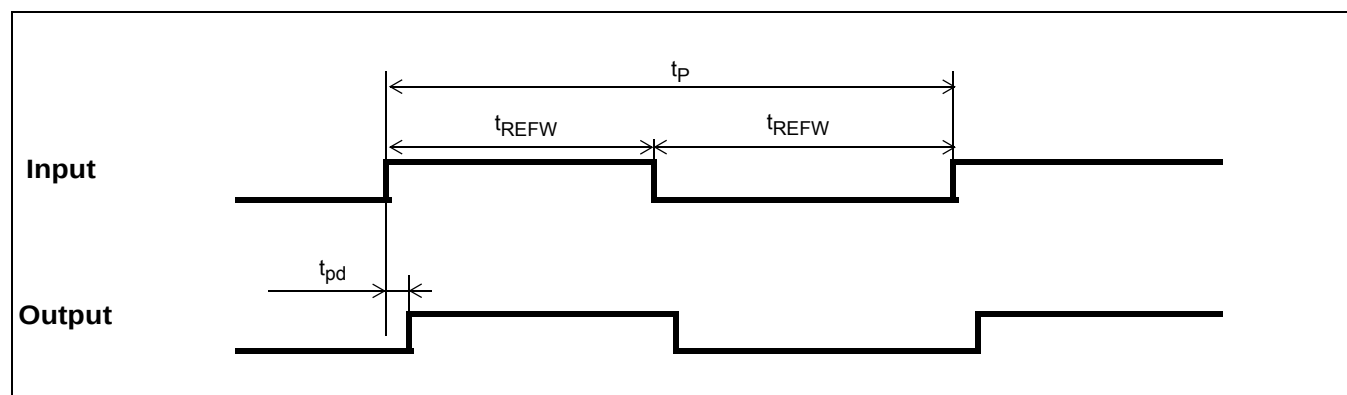


Figure 20 - Input To Output Timing



## 5.0 Performance Characterization

### Additive Jitter at 2.5 V\*

|   | Output Frequency (MHz) | Jitter Measurement Filter | Typical (fs) | Notes |
|---|------------------------|---------------------------|--------------|-------|
| 1 | 125                    | 12 kHz - 20 MHz           | 134          |       |
| 2 | 212.5                  | 12 kHz - 20 MHz           | 120          |       |
| 3 | 311.04                 | 12 kHz - 20 MHz           | 104          |       |
| 4 | 425                    | 12 kHz - 20 MHz           | 105          |       |
| 5 | 500                    | 12 kHz - 20 MHz           | 91           |       |
| 6 | 622.08                 | 12 kHz - 20 MHz           | 91           |       |
| 7 | 750                    | 12 kHz - 20 MHz           | 92           |       |

\*The values in this table were taken with an approximate input slew rate of 0.8 V/ns

### Additive Jitter at 3.3 V\*

|   | Output Frequency (MHz) | Jitter Measurement Filter | Typical (fs) | Notes |
|---|------------------------|---------------------------|--------------|-------|
| 1 | 125                    | 12 kHz - 20 MHz           | 135          |       |
| 2 | 212.5                  | 12 kHz - 20 MHz           | 122          |       |
| 3 | 311.04                 | 12 kHz - 20 MHz           | 106          |       |
| 4 | 425                    | 12 kHz - 20 MHz           | 106          |       |
| 5 | 500                    | 12 kHz - 20 MHz           | 94           |       |
| 6 | 622.08                 | 12 kHz - 20 MHz           | 92           |       |
| 7 | 750                    | 12 kHz - 20 MHz           | 93           |       |

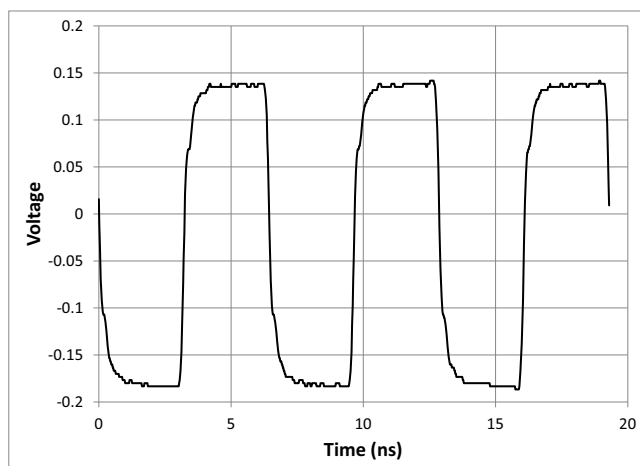
\*The values in this table were taken with an approximate input slew rate of 0.8 V/ns

### Additive jitter in the presence of power supply noise\*

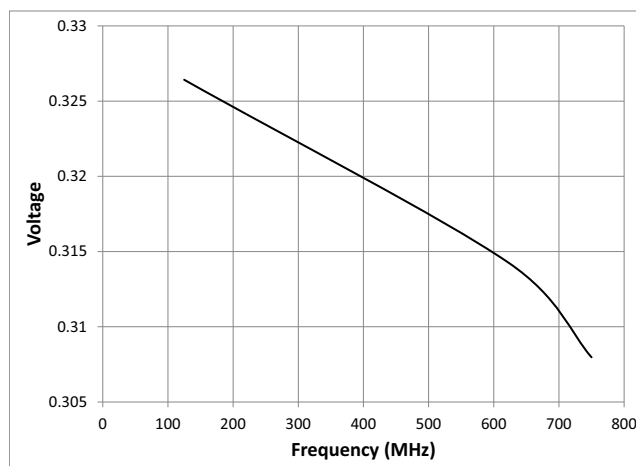
| Carrier frequency | Parameter        | Typical | Units  | Notes |
|-------------------|------------------|---------|--------|-------|
| 125               | 25 mV at 100 kHz | 48      | fs RMS |       |
| 750               | 25 mV at 100 kHz | 53      | fs RMS |       |

\* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for  $V_{DD} = 3.3$  V. The magnitude of the interfering tone is measured at the DUT.

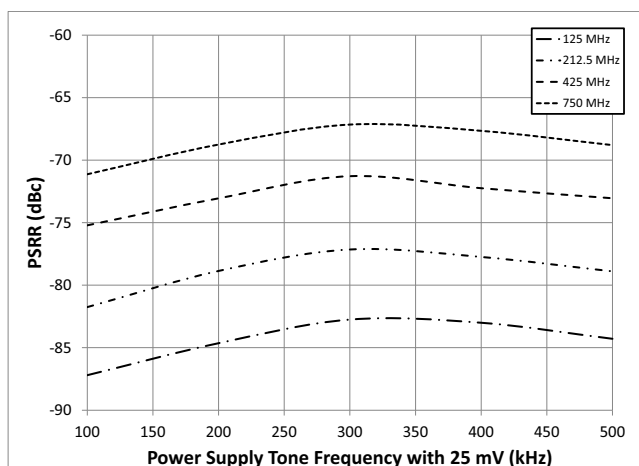
## 6.0 Typical Behavior



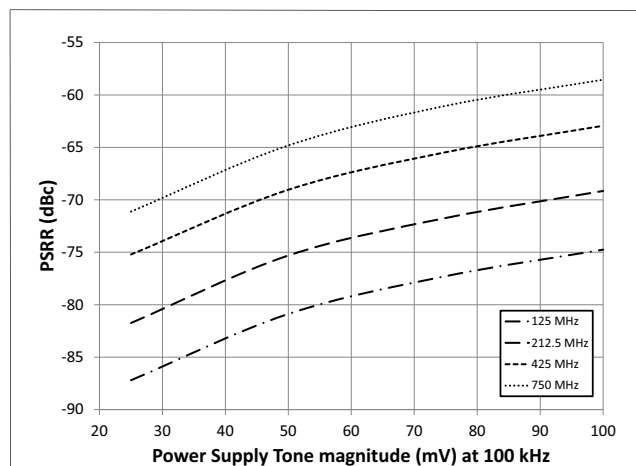
Typical Waveform at 155.52 MHz



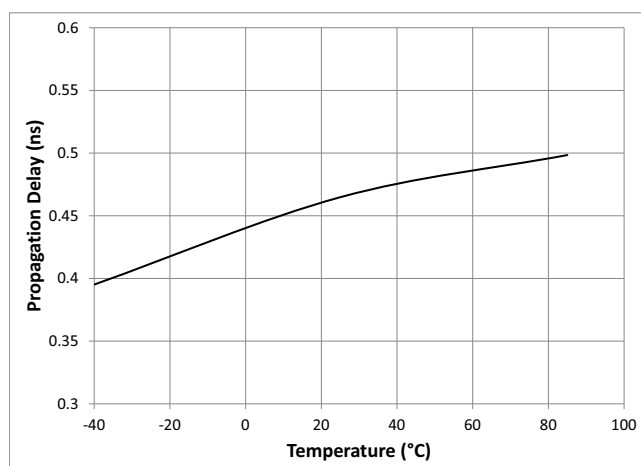
$V_{OD}$  versus Frequency



Power Supply Tone Frequency versus PSRR



Power Supply Tone Magnitude versus PSRR



Propagation Delay versus Temperature

Note: This is for a single device. For more details see the characterization section.

## 7.0 Package Thermal Characteristics

### Thermal Data

| Parameter                              | Symbol        | Test Condition              | Value                | Unit                 |
|----------------------------------------|---------------|-----------------------------|----------------------|----------------------|
| Junction to Ambient Thermal Resistance | $\Theta_{JA}$ | Still Air<br>1 m/s<br>2 m/s | 67.9<br>61.6<br>58.1 | $^{\circ}\text{C/W}$ |
| Junction to Case Thermal Resistance    | $\Theta_{JC}$ | Still Air                   | 44.1                 | $^{\circ}\text{C/W}$ |
| Junction to Board Thermal Resistance   | $\Theta_{JB}$ | Still Air                   | 23.2                 | $^{\circ}\text{C/W}$ |
| Maximum Junction Temperature*          | $T_{jmax}$    |                             | 125                  | $^{\circ}\text{C}$   |
| Maximum Ambient Temperature            | $T_A$         |                             | 85                   | $^{\circ}\text{C}$   |

\* Proper thermal management must be practiced to ensure that  $T_{jmax}$  is not exceeded.

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
2. DIMENSIONS ARE IN MILLIMETERS \* IN DEGREES
3. DIMENSION OF LEAD WIDTH APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Technical drawing of a Microsemi CMPG 16 QFN package outline. The drawing includes a top view, a side view, and a detail view of the terminal.

**Top View:** Shows the package footprint with dimensions. The lead width is specified as  $0.10$  to  $0.15$  mm. The terminal pitch is  $0.50$  mm. The package is labeled "PIN 1 AREA" and "DATUM A".

**Side View:** Shows the package height and lead length. The lead length is  $0.90 \pm 0.10$  mm. The package height is  $0.20$  mm. The package is labeled "SEATING PLANE" and "DATUM A".

**Detail A (Scale 3:1):** Shows the terminal profile with dimensions. The lead width is  $0.10$  to  $0.15$  mm. The terminal pitch is  $0.50$  mm. The terminal radius is  $0.025$  mm. The package is labeled "DETAIL A (SCALE 3:1)" and "DATUM A OR B".



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