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## TimeBuffer™ with up to 10 Inputs and 20 Outputs Product Brief

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### Features

#### Highlights

- Time signal fanout
- Time signal conversion between Ref-Sync pair and embedded Sync signals
- Time signal phase/frequency measurement
- Inputs: up to 10, differential or single-ended
- Outputs: up to 10 differential, up to 20 CMOS
- Core power consumption <0.9W

#### Input Clocks

- Accepts up to 10 differential or CMOS inputs
- Any input frequency from 1 kHz to 250 MHz
- Per-input activity and frequency monitoring
- Automatic or manual reference switching
- Revertive or nonrevertive switching
- Any input can be a 0.5 Hz to 8 kHz Sync input for Ref-Sync frequency/phase/time locking
- Any input can be a clock with embedded Sync
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution

#### 2 DPLLs

- One DPLL for buffer channel
- One for input phase/frequency measurement

#### Output Clocks

- Any frequency 0.5 Hz to 500 MHz
- Each OUTP/N pair can be LVDS, LVPECL, 2xC-MOS, Low- $V_{CM}$ , or programmable differential

- In 2xC-MOS mode, the P and N pins can be different frequencies (e.g. 125 MHz and 25 MHz)
- VDD per output pair, CMOS voltages 1.8V to 3.3V
- Per-synth phase adjustment, 1 ps resolution
- Per-output duty cycle adjustment
- Precise output alignment circuitry and per-output phase adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)

#### Local Oscillator

- Operates from a single oscillator 9.72 MHz to 400 MHz

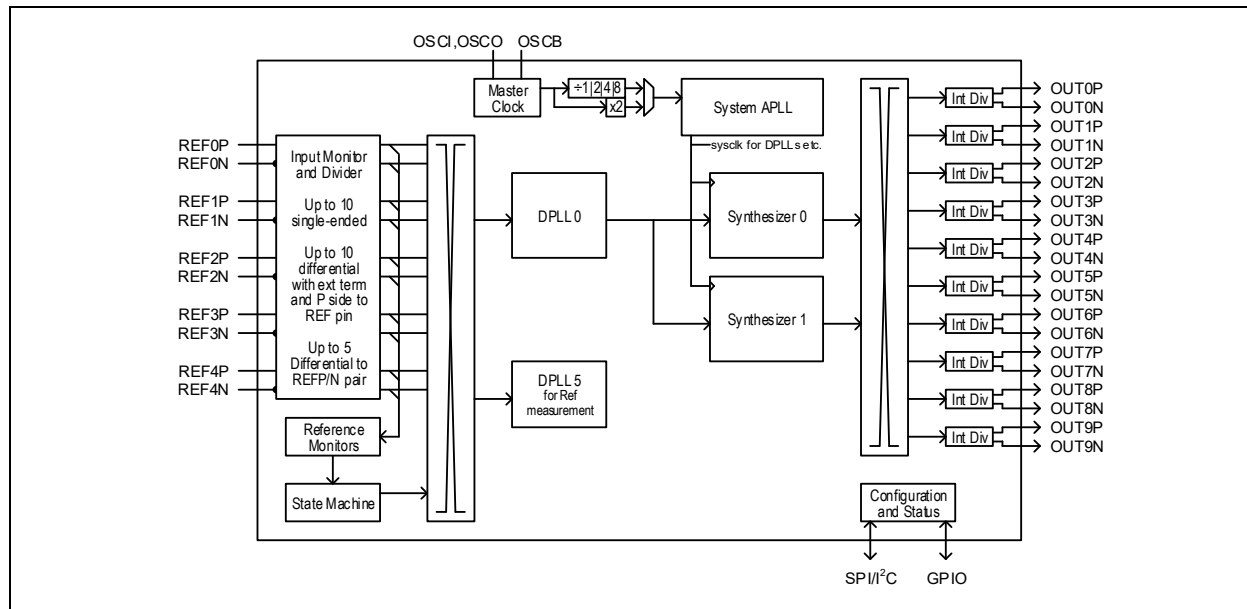
#### General Features

- Automatic self-configuration at power-up from internal Flash memory, 7 configurations
- Input-to-output alignment <100 ps
- Fast Ref-Sync locking for frequency and 1PPS phase alignment with lower-cost oscillator
- Easy-to-configure design requires no external VCXO or loop filter components
- 5 GPIO pins with many possible behaviors, each REF can be GPI, each OUT can be GPO
- SPI or I<sup>2</sup>C processor Interface
- 1.8V and 3.3V core VDD voltages
- Easy-to-use evaluation/programming software

#### Applications

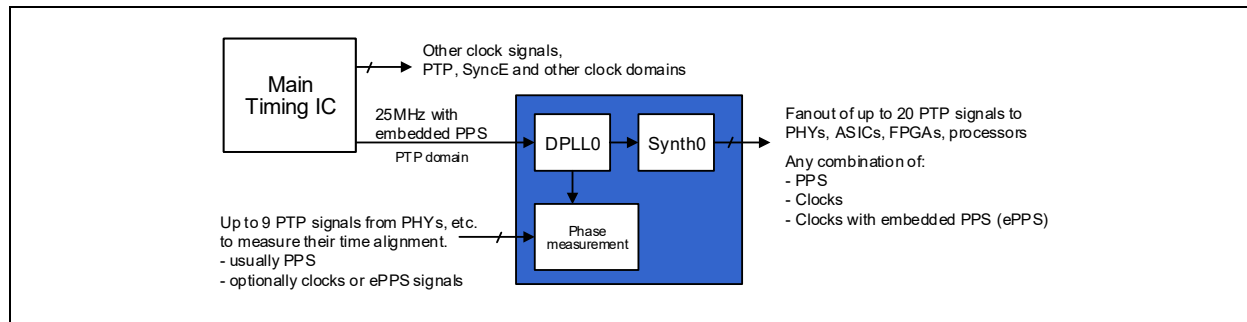
- Companion time-signal fanout device for timing card or line card timing ICs for telecom systems
- Companion phase/frequency measurement device for timing card or line card timing ICs

## 1.0 BLOCK DIAGRAM



**FIGURE 1-1:** Functional Block Diagram.

## 2.0 APPLICATION EXAMPLE



**FIGURE 2-1:** TimeBuffer Application Example.

## 3.0 DETAILED FEATURES

### 3.1 General

- Time signal fanout, up to 20 outputs
- Time signal conversion from Ref-Sync pair or embedded Sync signal to any combination of PPS, Ref-Sync pair and/or embedded Sync signals
- Operates from a single crystal resonator or clock oscillator
  - ≥48 MHz for lowest jitter
  - 9.72 MHz to 400 MHz total frequency range
- Configurable via SPI or I²C interface
- Internal nonvolatile memory
  - Factory-configurable power-on configuration
  - Multiple time writeable/re-writeable
- Default settings can be overridden using SPI/I²C

## 3.2 Input Block Features

- Ten input reference pins; each can accept a CMOS signal or the POS side of a differential pair; or two can be paired to accept both sides of a differential pair
- Any input can be a SYNC signal (0.5 Hz to 8 kHz) for Ref-Sync frequency/phase/time locking
- Any input can be a clock with embedded Sync signal (0.5 Hz to 1 kHz, duty cycle distortion for Sync)
- Input clocks can be any frequency from 1 kHz up to 250 MHz
- Inputs constantly monitored by programmable frequency and single-cycle monitors
- Single-cycle monitor can quickly disqualify a reference when measured period is incorrect
- Frequency measurement and monitoring (coarse, fine, and frequency-step monitors)
- Optional input clock invalidation on GPIO or GPI assertion to react to LOS signals from PHYs
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution
- Each REF pin can be a GPI (general-purpose input)

## 3.3 DPLL Features

- Two DPLLs: one for buffer channel and one for input phase and frequency measurement
- State machine automatically transitions among freerun, tracking, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 14 Hz to 470 Hz
- High-resolution frequency and phase measurement (4e-15 and 1 ps)
- Fast detection of input clock failure and transition to holdover mode

## 3.4 Synthesizer Features

- Two next-generation low-power, any-frequency synthesizers
- Two output frequency families
- Any-to-any frequency conversion with 0 ppm error
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components

## 3.5 Output Clock Features

- Up to 20 single-ended outputs, up to 10 differential outputs, from any synthesizer
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 0.5 Hz to 500 MHz (250 MHz max for CMOS)
- In CMOS mode, the OUTxN frequency can be an integer divisor of the OUTxP frequency (Example 1: OUT3P 125 MHz, OUT3N 25 MHz. Example 2: OUT2P 25 MHz, OUT2N 1 Hz)
- Outputs directly interface (DC-coupled) with LVDS, LVPECL, HCSL, and CMOS components
- Each output pair can have clock plus embedded Sync signal (0.5 Hz to clock div 4) indicated by wide or narrow high pulse
- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1 ps resolution
- Per-output phase adjustment to accommodate trace delays or compensate for system routing paths
- Per-output duty cycle/pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)
- Each OUT pin can be a GPO (general-purpose output)

## 3.6 Local Oscillator

- Operates from a single oscillator 9.72 MHz to 400 MHz. Best jitter:  $\geq 48$  MHz.

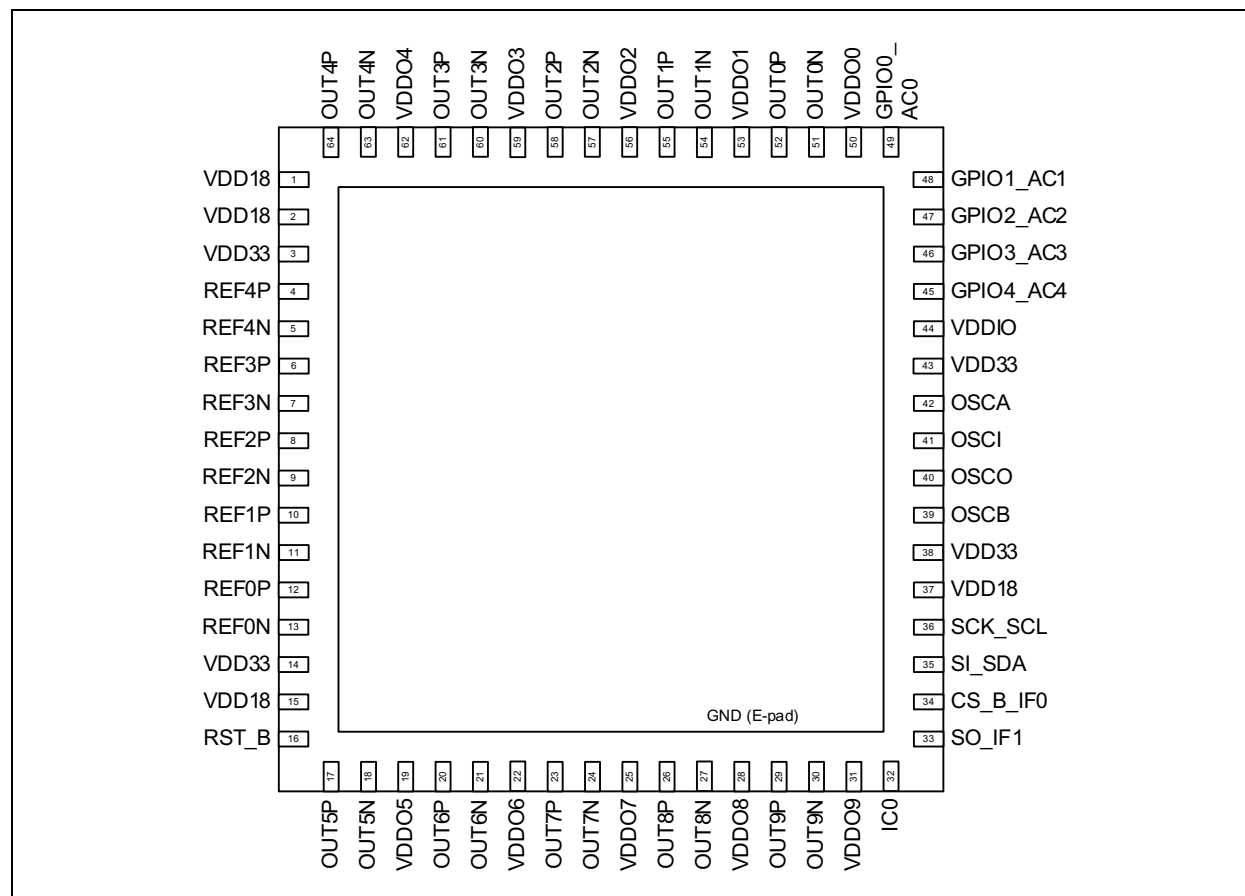
## 3.7 General Features

- Automatic self-configuration at power-up from internal Flash memory
- Input-to-output alignment <200 ps with external feedback
- Fast Ref-Sync locking for frequency and 1PPS phase alignment with lower-cost oscillator
- Generates output SYNC signals: 1PPS (IEEE 1588), 2 kHz or 8 kHz (SONET/SDH), or other frequency
- JESD204B clocking: clock and SYSREF signal generation with skew adjustment
- Five general-purpose I/O pins each with many possible status and control options
- SPI or I<sup>2</sup>C serial microprocessor interface

## 3.8 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts
- Works with or without an evaluation board

## 4.0 PIN DIAGRAM



**FIGURE 1:** 64-Lead 9 mm x 9 mm VQFN (0.5 mm pitch) for ZL30640.

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