Features

April 2010

- Supports Telcordia GR-1244-CORE Stratum 3
- Supports G.823 and G.824 for 2048 kbit/s and 1544 kbit/s interfaces
- Supports ANSI T1.403 and ETSI ETS 300 011 for ISDN primary rate interfaces
- Simple hardware control interface
- Accepts two input references and synchronizes to any combination of 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz inputs
- Provides a range of clock outputs: 1.544 MHz, 2.048 MHz, 16.384 MHz and either 4.096 MHz & 8.192 MHz or 32.768 MHz & 65.536 MHz
- Hitless reference switching between any combination of valid input reference frequencies
- Provides 5 styles of 8 kHz framing pulses
- Holdover frequency accuracy of 1 x 10^{-8}
- Lock, Holdover and Out of Range indication
- Selectable loop filter bandwidth of 1.8 Hz or 922 Hz
- Less than 0.6 ns_{pp} jitter on all output clocks

Ordering Information

ZL30101QDG1 64 Pin TQFP* Trays, Bake & Drypack
*Pb Free Matte Tin
-40°C to +85°C

- External master clock source: clock oscillator or crystal

Applications

- Synchronization and timing control for multi-trunk DS1/E1 systems such as DSLAMs, gateways and PBXs
- Clock and frame pulse source for ST-BUS, GCI and other time division multiplex (TDM) buses

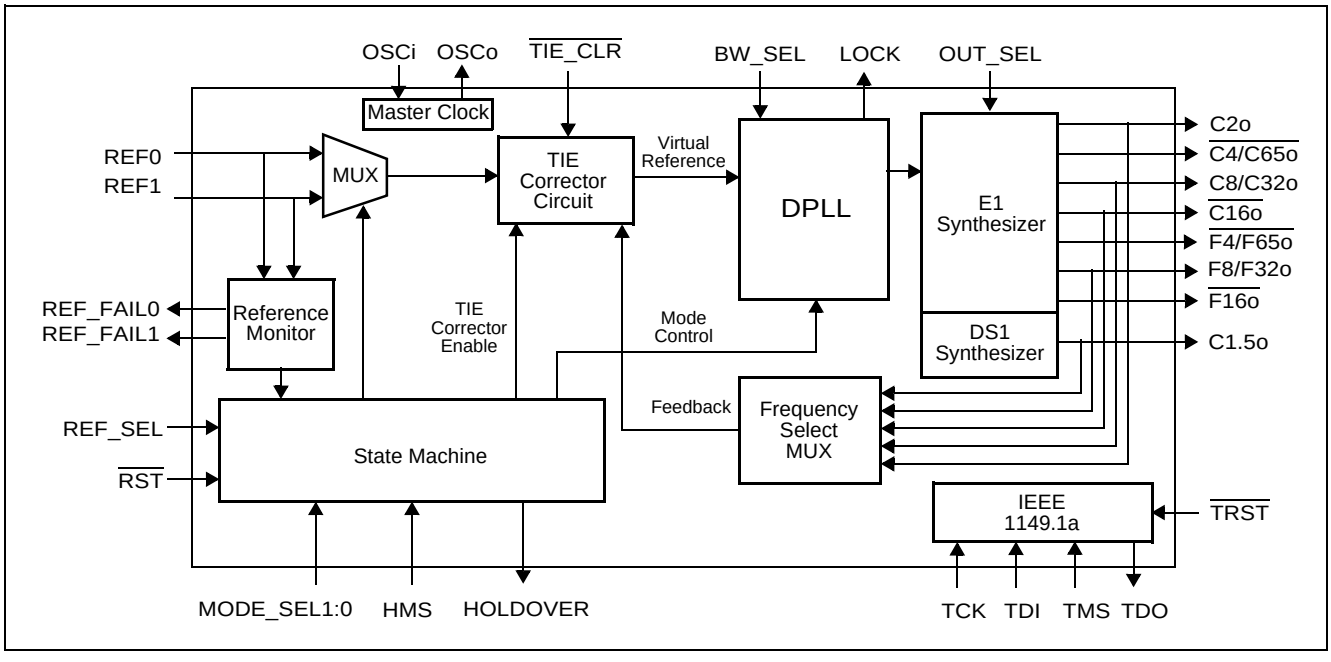


Figure 1 - Functional Block Diagram

Description

The ZL30101 Stratum 3 System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization for multi-trunk T1 and E1 transmission equipment.

The ZL30101 generates ST-BUS and other TDM clock and framing signals that are phase locked to one of two input references. It helps ensure system reliability by monitoring its references for accuracy and stability and by maintaining stable output clocks during reference switching operations and during short periods when a reference is unavailable.

The ZL30101 is intended to be the central timing and synchronization resource for network equipment that complies with Telcordia, ETSI, ITU-T and ANSI network specifications.

Table of Contents

List of Figures

1.0 Change Summary

Changes from February 2006 Issue to April 2010 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information Box	Leaded part number ZL30101QDC has been obsoleted and replaced by ZL30101QDG1.

Changes from November 2005 Issue to February 2006 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information Box	Updated Ordering Information

Changes from July 2005 Issue to November 2005 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Features	Added description for hitless reference switching.
23	Section 6.1	Removed power supply decoupling circuit and included reference to synchronizer power supply decoupling application note.

Changes from October 2004 Issue to July 2005 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
9	$\overline{\text{RST}}$ pin	Specified clock and frame pulse outputs forced to high impedance
28	Table “DC Electrical Characteristics*“	Corrected Schmitt trigger levels
32	Table “Performance Characteristics* - Functional“	Gave more detail on Lock Time conditions

Changes from June 2004 Issue to October 2004 Issue. Page, section, figure and table numbers refer to this issue.

Page	Item	Change
1	Text	Jitter changed to 0.6 ns from 0.5 ns
7	Figure 2	Added note specifying not e-Pad
8	Table “Pin Description“	Added information about Schmitt trigger feedback paths to C1.5o, C2o, C16o, and F8/F32o
11	Section 3.2	Added text about input pulse width restriction
16	Section 3.4	Added details on LOCK pin behaviour
20	Section 4.4	Added text and Figure 10 explaining LOCK pin behaviour
21	Section 5.0	Added Jitter definition
26	Section 6.4	Corrected time-constant of example reset circuit
27	Table “Absolute Maximum Ratings*“	Corrected package power rating
28	Table “DC Electrical Characteristics*“	Corrected current consumption Corrected input voltage characteristics to reflect Schmitt trigger Corrected input leakage current to reflect internal pull-ups Corrected output voltage note to reflect two pad strengths
29	Table “AC Electrical Characteristics* - Input Timing for REF0 and REF1 References (see Figure 15)“	Added explanatory note
33	Table “Performance Characteristics*: Output Jitter Generation - ANSI T1.403 Conformance“	Changed jitter numbers
33	Table “Performance Characteristics*: Output Jitter Generation - ITU-T G.812 Conformance“	Changed jitter number
33	Table “Performance Characteristics* - Unfiltered Intrinsic Jitter“	Changed jitter numbers, removed UI column

2.0 Physical Description

2.1 Pin Connections

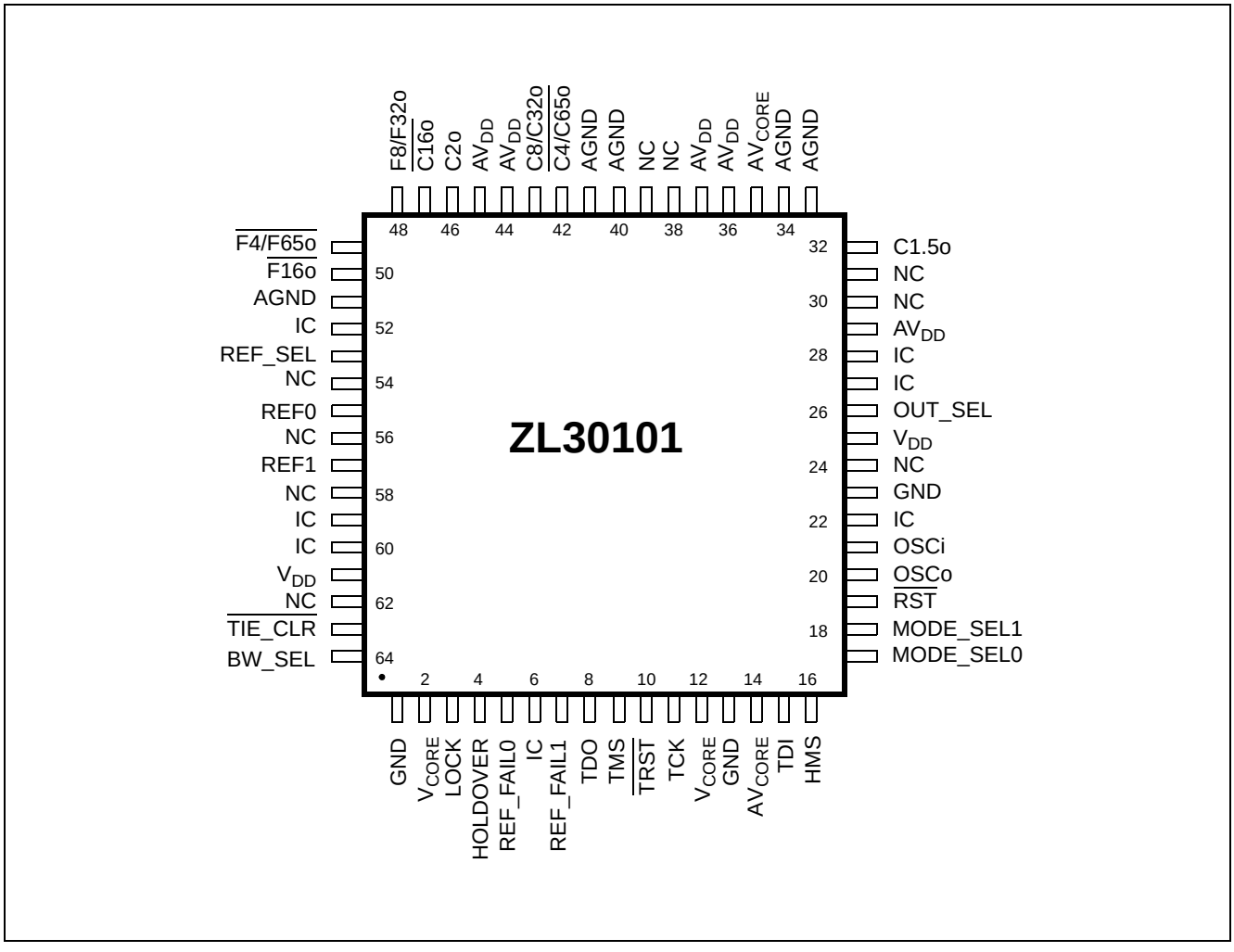


Figure 2 - Pin Connections (64 pin TQFP, please see Note 1)

Note 1: The ZL30101 uses the TQFP shown in the package outline designated with the suffix QD, the ZL30101 does not use the e-Pad TQFP.

2.2 Pin Description

Pin Description

Pin #	Name	Description
1	GND	**Ground.** 0 V.
2	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal.
3	LOCK	**Lock Indicator (Output).** This output goes to a logic high when the PLL is frequency locked to the selected input reference.
4	HOLDOVER	**Holdover (Output).** This output goes to a logic high whenever the PLL goes into holdover mode.
5	REF_FAIL0	**Reference 0 Failure Indicator (Output).** A logic high at this pin indicates that the REF0 reference frequency has exceeded the out-of-range limit or that it is exhibiting abrupt phase or frequency changes.
6	IC	**Internal bonding Connection.** Leave unconnected.
7	REF_FAIL1	**Reference 1 Failure Indicator (Output).** A logic high at this pin indicates that the REF1 reference frequency has exceeded the out-of-range limit or that it is exhibiting abrupt phase or frequency changes.
8	TDO	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
9	TMS	**Test Mode Select (Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
10	$\overline{TRST}$	**Test Reset (Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
11	TCK	**Test Clock (Input):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
12	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal.
13	GND	**Ground.** 0 V.
14	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
15	TDI	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
16	HMS	**Hitless Mode Switching (Input).** The HMS circuit controls phase accumulation during the transition from Holdover or Freerun mode to Normal mode on the same reference. A logic low at this pin will cause the ZL30101 to maintain the delay stored in the TIE Corrector Circuit when it transitions from Holdover or Freerun mode to Normal mode. A logic high on this pin will cause the ZL30101 to measure a new delay for its TIE Corrector Circuit thereby minimizing the output phase movement when it transitions from Holdover or Freerun mode to Normal mode.
17	MODE_SEL0	**Mode Select 0 (Input).** This input combined with MODE_SEL1 determines the mode (Normal, Holdover or Freerun) of operation, see Table 3 on page 18.
18	MODE_SEL1	**Mode Select 1 (Input).** See MODE_SEL0 pin description.

Pin Description (continued)

Pin #	Name	Description
19	$\overline{RST}$	**Reset (Input).** A logic low at this input resets the device. On power up, the $\overline{RST}$ pin must be held low for a minimum of 300 ns after the power supply pins have reached the minimum supply voltage. When the RST pin goes high, the device will transition into a Reset state for 3 ms. In the Reset state all clock and frame pulse outputs will be forced into high impedance.
20	OSCo	**Oscillator Master Clock (Output).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCi. This output is not suitable for driving other devices. For clock oscillator operation, this pin must be left unconnected.
21	OSCi	**Oscillator Master Clock (Input).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin must be connected to a clock source.
22	IC	**Internal Connection.** Leave unconnected.
23	GND	**Ground.** 0 V.
24	NC	**No internal bonding Connection.** Leave unconnected.
25	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal.
26	OUT_SEL	**Output Selection (Input).** This input selects the signals on the combined output clock and frame pulse pins, see Table 2 on page 18.
27	IC	**Internal Connection.** Connect this pin to ground.
28	IC	**Internal Connection.** Connect this pin to ground.
29	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
30	NC	**No internal bonding Connection.** Leave unconnected.
31	NC	**No internal bonding Connection.** Leave unconnected.
32	C1.5o	**Clock 1.544 MHz (Output).** This output is used in DS1 applications. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
33	AGND	**Analog Ground.** 0 V
34	AGND	**Analog Ground.** 0 V
35	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
36	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
37	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
38	NC	**No internal bonding Connection.** Leave unconnected.
39	NC	**No internal bonding Connection.** Leave unconnected.
40	AGND	**Analog Ground.** 0 V
41	AGND	**Analog Ground.** 0 V
42	$\overline{C4}/\overline{C65o}$	**Clock 4.096 MHz or 65.536 MHz (Output).** This output is used for ST-BUS operation at 2.048 Mbps, 4.096 Mbps or 65.536 MHz (ST-BUS 65.536 Mbps). The output frequency is selected via the OUT_SEL pin.

Pin Description (continued)

Pin #	Name	Description
43	C8/C32o	**Clock 8.192 MHz or 32.768 MHz (Output).** This output is used for ST-BUS and GCI operation at 8.192 Mbps or for operation with a 32.768 MHz clock. The output frequency is selected via the OUT_SEL pin.
44	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
45	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
46	C2o	**Clock 2.048 MHz (Output).** This output is used for standard E1 interface timing and for ST-BUS operation at 2.048 Mbps. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
47	$\overline{C16o}$	**Clock 16.384 MHz (Output).** This output is used for ST-BUS operation with a 16.384 MHz clock. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
48	F8/F32o	**Frame Pulse (Output).** This is an 8 kHz 122 ns active high framing pulse (OUT_SEL=0) or it is an 8 kHz 31 ns active high framing pulse (OUT_SEL=1), which marks the beginning of a frame. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
49	$\overline{F4}/\overline{F65o}$	**Frame Pulse ST-BUS 2.048 Mbps or ST-BUS at 65.536 MHz clock (Output).** This output is an 8 kHz 244 ns active low framing pulse (OUT_SEL=0), which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mbps and 4.096 Mbps. Or this output is an 8 kHz 15 ns active low framing pulse (OUT_SEL=1), typically used for ST-BUS operation with a clock rate of 65.536 MHz.
50	$\overline{F16o}$	**Frame Pulse ST-BUS 8.192 Mbps (Output).** This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mbps.
51	AGND	**Analog Ground.** 0 V
52	IC	**Internal Connection.** Connect this pin to ground.
53	REF_SEL	**Reference Select (Input)**. This input selects the input reference that is used for synchronization, see Table 4 on page 20. This pin is internally pulled down to GND.
54	NC	**No internal bonding Connection.** Leave unconnected.
55	REF0	**Reference (Input).** This is one of two (REF0, REF1) input reference sources used for synchronization. One of five possible frequencies may be used: 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz. This pin is internally pulled down to GND.
56	NC	**No internal bonding Connection.** Leave unconnected.
57	REF1	**Reference (Input).** See REF0 pin description.
58	NC	**No internal bonding Connection.** Leave unconnected.

Pin Description (continued)

Pin #	Name	Description
59	IC	**Internal Connection.** Connect this pin to ground.
60	IC	**Internal Connection.** Connect this pin to ground.
61	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal.
62	NC	**No internal bonding Connection.** Leave unconnected.
63	$\overline{\text{TIE\_CLR}}$	**TIE Corrector Circuit Reset (Input).** A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a realignment of the input phase with the output phase.
64	BW_SEL	**Filter Bandwidth Selection (Input).** This pin selects the bandwidth of the DPLL loop filter, see Table 1 on page 18. Set continuously high to track jitter on the input reference closely or temporarily high to allow the ZL30101 to quickly lock to the input reference.

3.0 Functional Description

The ZL30101 is a DS1/E1 Stratum 3 System Synchronizer providing timing (clock) and synchronization (frame) signals to interface circuits for DS1 and E1 Primary Rate Digital Transmission links. Figure 1 is a functional block diagram which is described in the following sections.

3.1 Reference Select Multiplexer (MUX)

The ZL30101 accepts two simultaneous reference input signals and operates on their rising edges. One of them, the primary reference (REF0) or the secondary reference (REF1) signal can be selected as input to the TIE corrector circuit based on the reference selection (REF_SEL) input.

3.2 Reference Monitor

The input references are monitored by two independent reference monitor blocks, one for each reference. The block diagram of a single reference monitor is shown in Figure 3. For each reference clock, the frequency is detected and the clock is continuously monitored for three independent criteria that indicate abnormal behavior of the reference signal, for example; long term drift from its nominal frequency or excessive jitter. To ensure proper operation of the reference monitor circuit, the minimum input pulse width restriction of 15 nsec must be observed.

- **Reference Frequency Detector (RFD)**: This detector determines whether the frequency of the reference clock is 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz and provides this information to the various monitor circuits and the phase detector circuit of the DPLL.
- **Precise Frequency Monitor (PFM)**: This circuit determines whether the frequency of the reference clock is within the applicable accuracy range of ±12 ppm, see Figure 5. It will take the precise frequency monitor up to 10 s to qualify or disqualify the input reference.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference frequency over intervals of approximately 30 µs to quickly detect large frequency changes.
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.

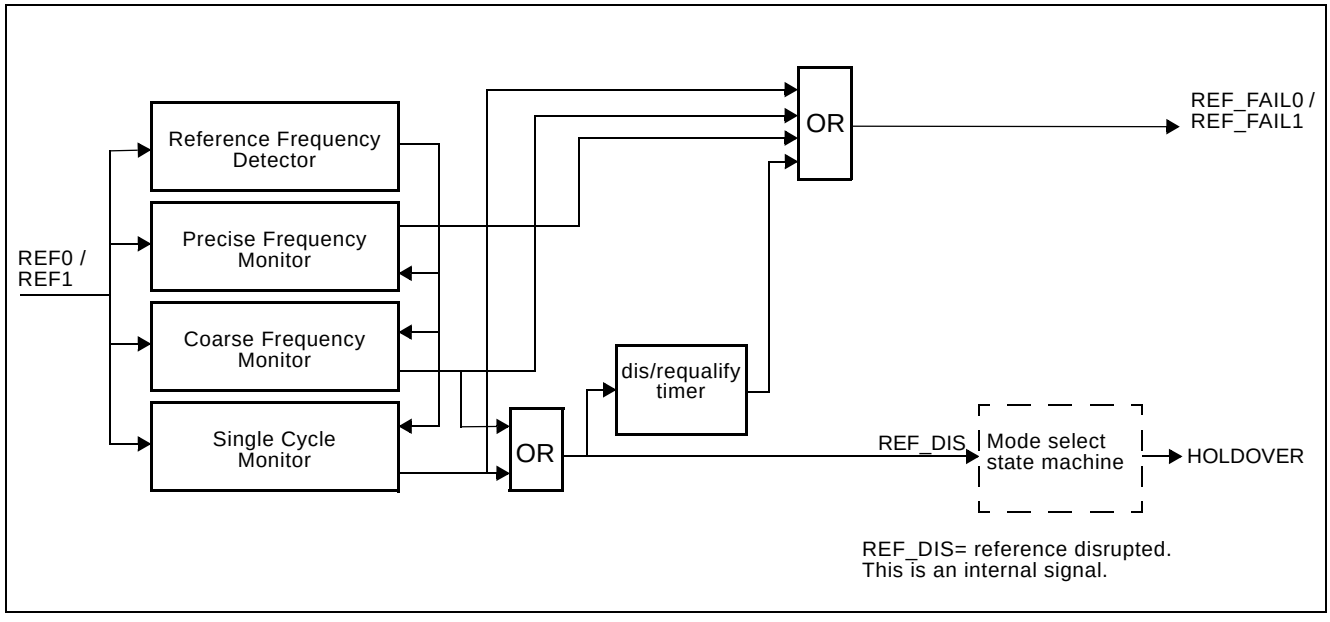


Figure 3 - Reference Monitor Circuit

Exceeding the thresholds of any of the monitors forces the corresponding REF_FAIL pin to go high. The single cycle and coarse frequency failure flags force the DPLL into Holdover mode and feed a timer that disqualifies the reference input signal when the failures are present for more than 2.5 s. The single cycle and coarse frequency failures must be absent for 10 s to let the timer requalify the input reference signal as valid. Multiple failures of less than 2.5 s each have an accumulative effect and will disqualify the reference eventually. This is illustrated in Figure 4.

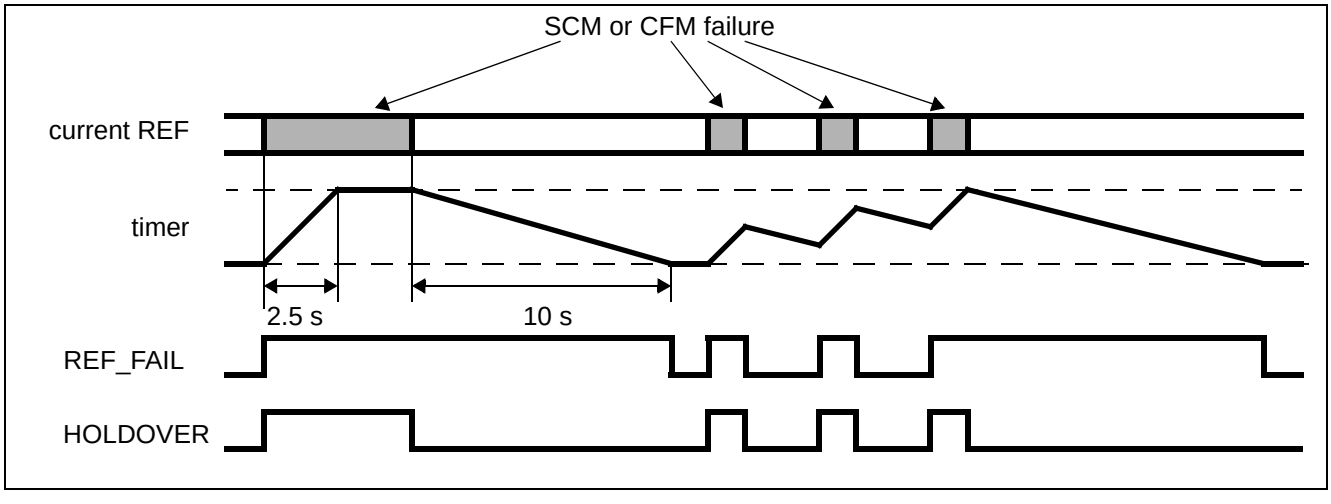


Figure 4 - Behaviour of the Dis/Requalify Timer

When the incoming signal returns to normal (REF_FAIL=0), the DPLL returns to Normal mode with the output signal locked to the input signal. Each of the monitors has a built-in hysteresis to prevent flickering of the REF_FAIL status pin at the threshold boundaries. The precise frequency monitor and the timer do not affect the mode (Holdover/Normal) of the DPLL.

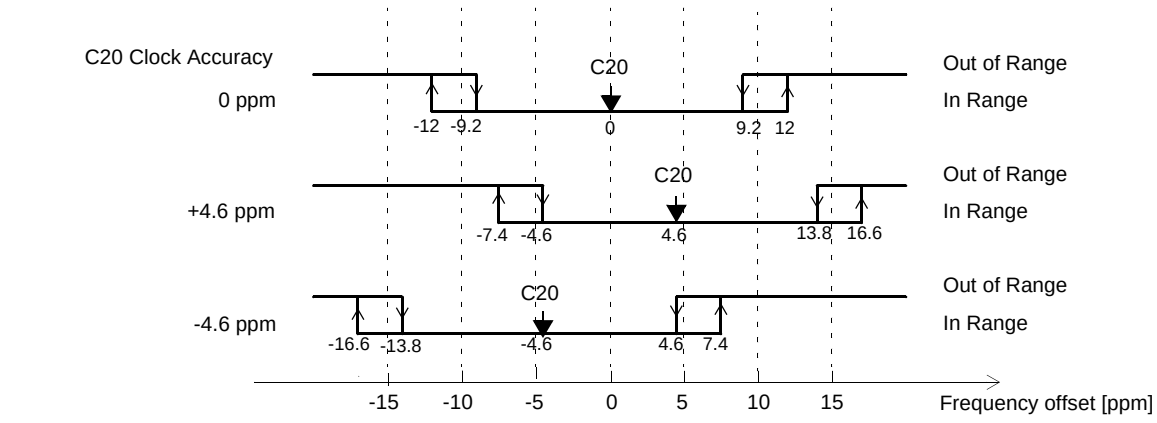


Figure 5 - Out-of-Range Thresholds

The precise frequency monitor's failure thresholds are compatible with Telcordia GR-1244-CORE Stratum 3 as shown in Figure 5. It will take the precise frequency monitor up to 10 s to qualify or disqualify the input reference.

3.3 Time Interval Error (TIE) Corrector Circuit

The TIE corrector circuit eliminates phase transients on the output clock that may occur during reference switching or the recovery from Holdover mode to Normal mode.

On recovery from Holdover mode (dependent on the HMS pin) or when switching to another reference input, the TIE corrector circuit measures the phase delay between the current phase (feedback signal) and the phase of the selected reference signal. This delay value is stored in the TIE corrector circuit. This circuit creates a new virtual reference signal that is at the same phase position as the feedback signal. By using the virtual reference, the PLL minimizes the phase transient it experiences when it switches to another reference input or recovers from Holdover mode.

The delay value can be reset by applying a logic low pulse to the TIE corrector circuit clear pin ($\overline{\text{TIE\_CLR}}$). A minimum reset pulse width is 20 ns. This results in a phase alignment between the input reference signal and the output clocks and frame pulses as shown in Figure 15 on page 29 and Figure 16 on page 31. The speed of the phase alignment correction is limited to 61 µs/s when BW_SEL=0. Convergence is always in the direction of least phase travel. In general the TIE correction should not be exercised when Holdover mode is entered for short time periods. $\overline{\text{TIE\_CLR}}$ can be kept low continuously. In that case the output clocks will always be aligned with the selected input reference. This is illustrated in Figure 6.

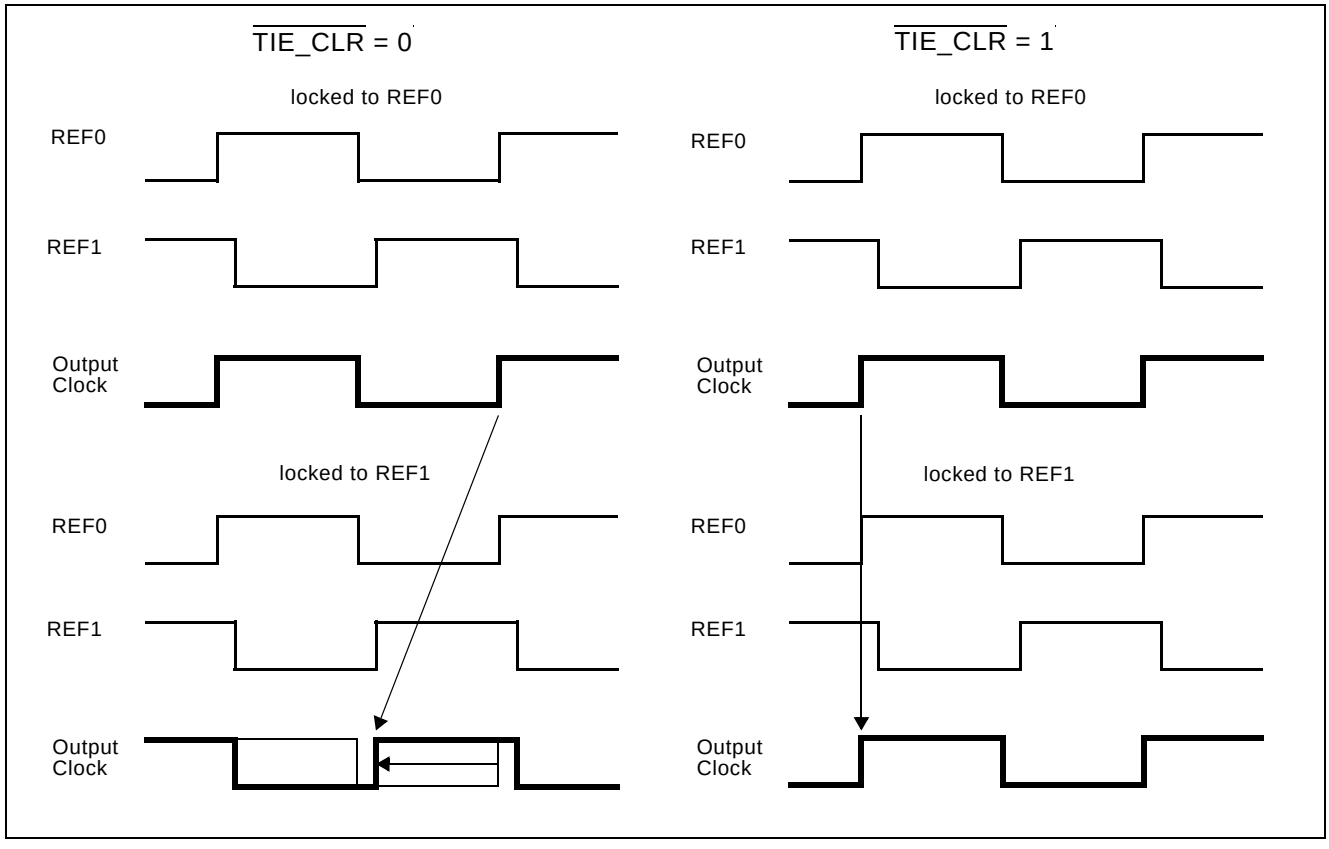


Figure 6 - Timing Diagram of Hitless Reference Switching

The Hitless Mode Switching (HMS) pin enables phase hitless returns from Freerun and Holdover modes to Normal mode in a single reference operation. A logic low at the HMS input disables the TIE corrector circuit updating the delay value thereby forcing the output of the PLL to gradually move back to the original point before it went into Holdover mode. (see Figure 7). This prevents accumulation of phase in network elements. A logic high (HMS=1) enables the TIE corrector circuit to update its delay value thereby preventing a large output phase movement after return to Normal mode. This causes accumulation of phase in network elements. In both cases the PLL's output can be aligned with the input reference by setting $\overline{\text{TIE\_CLR}}$ low. Regardless of the HMS pin state, reference switching in the ZL30101 is always hitless unless $\overline{\text{TIE\_CLR}}$ is kept low continuously.

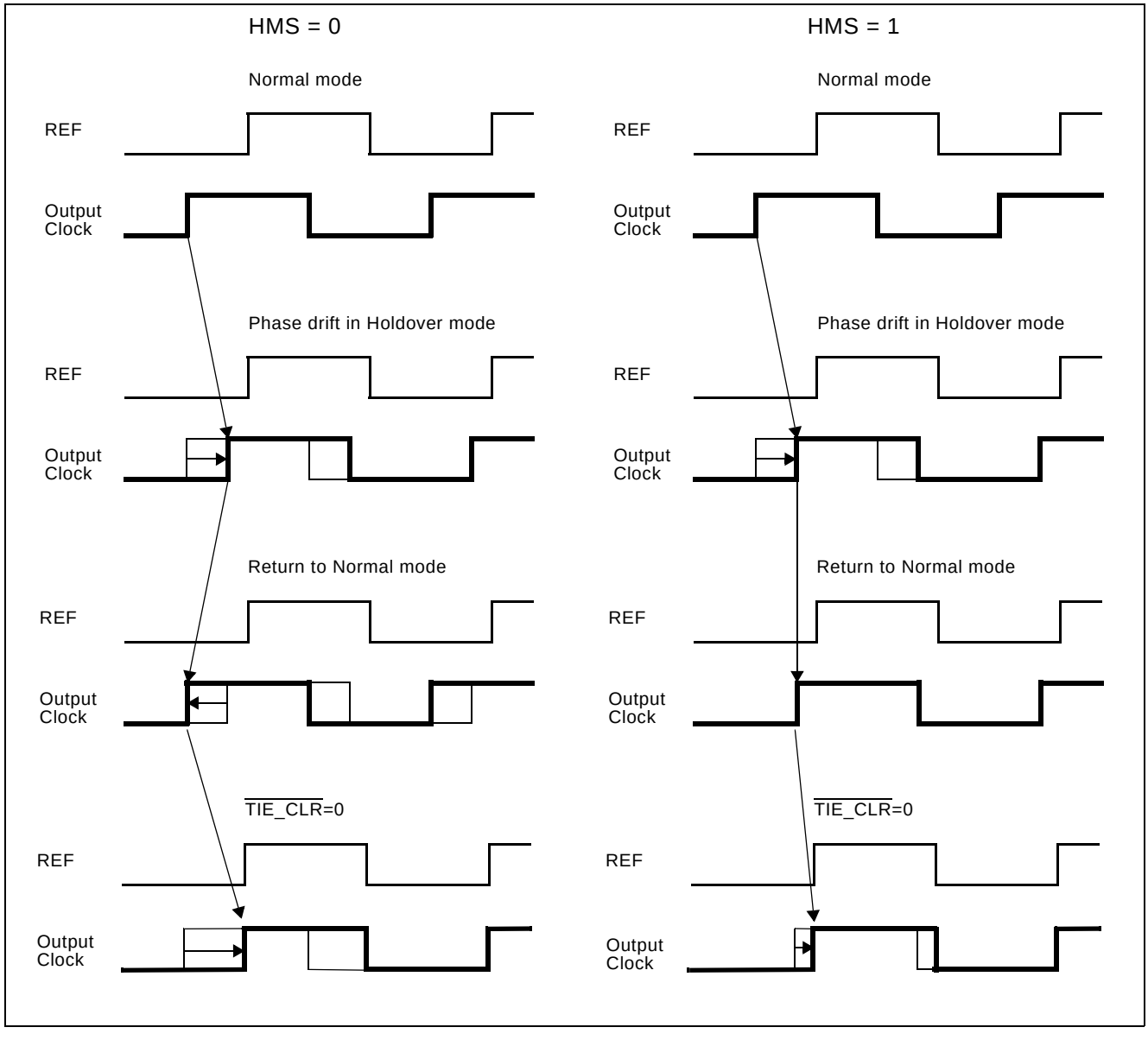


Figure 7 - Timing Diagram of Hitless Mode Switching

Examples:

HMS=1: When 10 Normal to Holdover to Normal mode transitions occur and in each case the Holdover mode was entered for 2 seconds, then the accumulated phase change (MTIE) could be as large as 330 ns.

- $Phase_{holdover\_drift}$ = 0.01 ppm x 2 s = 20 ns
- $Phase_{mode\_change}$ = 0 ns + 13 ns = 13 ns
- $Phase_{10\ changes}$ = 10 x (20 ns + 13 ns) = 330 ns

where:

- 0.01 ppm is the accuracy of the Holdover mode
- 0 ns is the maximum phase discontinuity in the transition from the Normal mode to the Holdover mode

- 13 ns is the maximum phase discontinuity in the transition from the Holdover mode to the Normal mode when a new TIE corrector value is calculated

HMS=0: When the same ten Normal to Holdover to Normal mode changes occur and in each case Holdover mode was entered for 2 seconds, then the overall MTIE would be 20 ns. As the delay value for the TIE corrector circuit is not updated, there is no 13 ns measurement error at this point. The phase can still drift for 20 ns when the PLL is in Holdover mode but when the PLL enters Normal mode again, the phase moves back to the original point so the phase is not accumulated.

3.4 Digital Phase Lock Loop (DPLL)

The DPLL of the ZL30101 consists of a phase detector, a limiter, a loop filter, a digitally controlled oscillator (DCO) and a lock indicator, as shown in Figure 8. The data path from the phase detector to the limiter is tapped and routed to the lock indicator that provides a lock indication which is output at the LOCK pin.

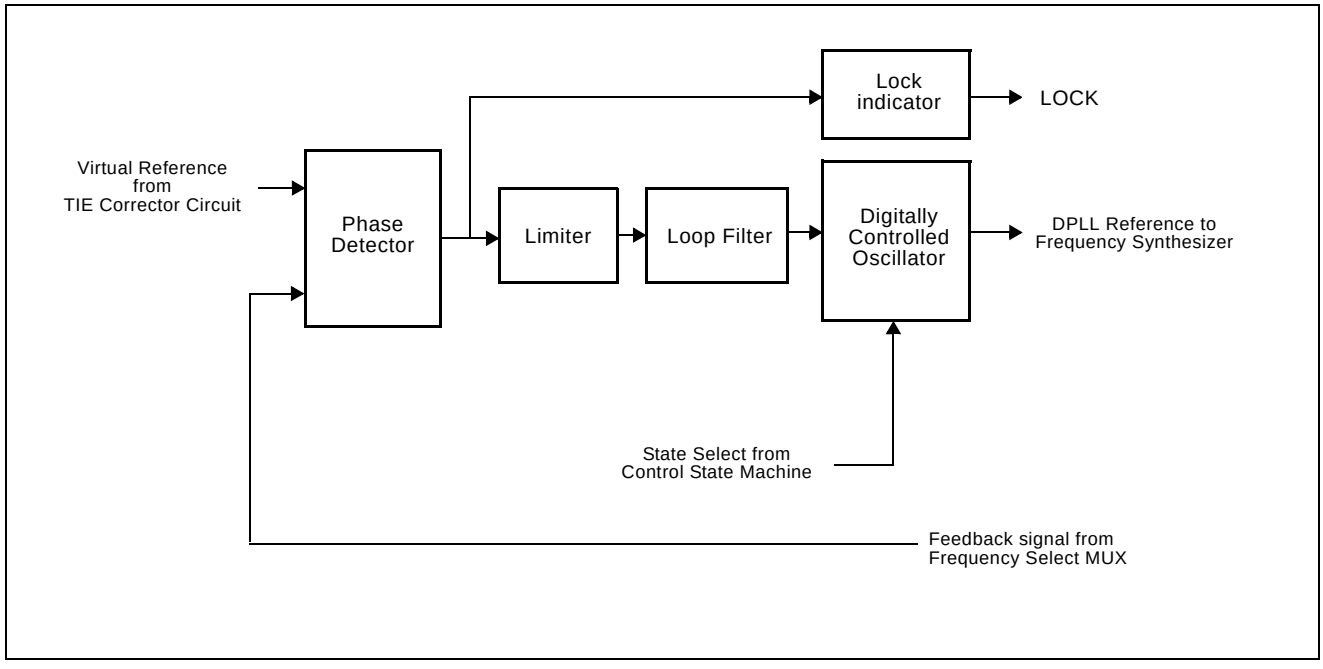


Figure 8 - DPLL Block Diagram

Phase Detector - the phase detector compares the virtual reference signal from the TIE corrector circuit with the feedback signal and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the limiter circuit.

Limiter - the limiter receives the error signal from the phase detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 61 μs/s or 9.5 ms/s, see Table 1.

Loop Filter - the loop filter is similar to a first order low pass filter with a narrow or wide bandwidth suitable to provide system synchronization or line card timing, see Table 1. The wide bandwidth can be used to closely track the input reference in the presence of jitter or it can be temporarily enabled for fast locking to a new reference (1 s lock time).

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the loop filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30101.

In Normal mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover mode, the DCO is free running at a frequency equal to the frequency that the DCO was generating in Normal mode. The frequency in Holdover mode is calculated from frequency samples stored 26 ms to 52 ms before the ZL30101 entered Holdover mode.

In Freerun mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20 MHz source.

Lock Indicator - the lock detector monitors if the output value of the phase detector is within the phase-lock-window for a certain time. The selected phase-lock-window guarantees the stable operation of the LOCK pin with maximum network jitter and wander on the reference input. If the DPLL is locked and then goes into Holdover mode (auto or manual), the LOCK pin will initially stay high for 1 s. If at that point the DPLL is still in holdover mode, the LOCK pin will go low; subsequently the LOCK pin will not return high for at least the full lock-time duration. In Freerun mode the LOCK pin will go low immediately.

3.5 Frequency Synthesizers

The output of the DCO is used by the frequency synthesizers to generate the C1.5o, C2o, $\overline{\text{C4o}}$, C8o, $\overline{\text{C16o}}$, C32o and C65o clocks and the F4o, F8o, F16o, F32o and F65o frame pulses which are synchronized to the selected reference input (REF0 or REF1). The frequency synthesizers use digital techniques to generate output clocks and advanced noise shaping techniques to minimize the output jitter. The clock and frame pulse outputs have limited driving capability and should be buffered when driving high capacitance loads.

3.6 State Machine

As shown in Figure 1, the control state machine controls the TIE Corrector Circuit and the DPLL. The control of the ZL30101 is based on the inputs MODE_SEL1:0, REF_SEL and HMS.

3.7 Master Clock

The ZL30101 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

4.0 Control and Modes of Operation

4.1 Loop Filter Selection

The loop filter settings can be selected through the BW_SEL pin, see Table 1. For the ZL30101 to be compliant with Telcordia GR-1244-CORE Stratum 3, BW_SEL must be set low.

BW_SEL	Detected REF Frequency	Loop Filter Bandwidth	Phase Slope Limiting
0	any	1.8 Hz	61 μs/s
1	8 kHz	58 Hz	9.5 ms /s
1	1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz	922 Hz	9.5 ms /s

Table 1 - Loop Filter Settings

4.2 Output Clock and Frame Pulse Selection

The output clock and frame pulses of the frequency synthesizers are available in two groups controlled by the OUT_SEL input. Table 2 lists the supported combinations of output clocks and frame pulses.

OUT_SEL	Generated Clocks	Generated Frame Pulses
0	C1.5o, C2o, $\overline{\text{C4o}}$, C8o, $\overline{\text{C16o}}$	$\overline{\text{F4o}}$, F8o, $\overline{\text{F16o}}$
1	C1.5o, C2o, $\overline{\text{C16o}}$, C32o, $\overline{\text{C65o}}$	$\overline{\text{F16o}}$, F32o, $\overline{\text{F65o}}$

Table 2 - Clock and Frame Pulse Selection

4.3 Modes of Operation

The ZL30101 has three possible manual modes of operation; Normal, Holdover and Freerun. These modes are selected with the mode select pins MODE_SEL1 and MODE_SEL0 as is shown in Table 3. Transitioning from one mode to the other is controlled by an external controller.

MODE_SEL1	MODE_SEL0	Mode
0	0	Normal (with automatic Holdover)
0	1	Holdover
1	0	Freerun
1	1	reserved (must not be used)

Table 3 - Operating Modes

4.3.1 Freerun Mode

Freerun mode is typically used when an independent clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun mode, the ZL30101 provides timing and synchronization signals which are based on the master clock frequency (supplied to OSCi pin) only, and are not synchronized to the reference input signals.

The Freerun accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±4.6 ppm output clock is required, the master clock must also be ±4.6 ppm. See Applications - Section 6.2, “Master Clock“.

4.3.2 Holdover Mode

Holdover mode is typically used for short durations while network synchronization is temporarily disrupted.

In Holdover mode, the ZL30101 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

When in Normal mode, and locked to the input reference signal, a numerical value corresponding to the ZL30101 output reference frequency is stored alternately in two memory locations every 26 ms. When the device is switched into Holdover mode, the value in memory from between 26 ms and 52 ms is used to set the output frequency of the device. The frequency accuracy of Holdover mode is 0.01 ppm.

Two factors affect the accuracy of Holdover mode. One is drift on the master clock while in Holdover mode, drift on the master clock directly affects the Holdover mode accuracy. Note that the absolute master clock (OSCi) accuracy does not affect Holdover accuracy, only the *change* in OSCi accuracy while in Holdover mode. For example, a ±4.6 ppm master clock may have a temperature coefficient of ±0.1 ppm per °C. So a ±10 °C change in temperature, while the ZL30101 is in Holdover mode may result in an additional offset (over the 0.01 ppm) in frequency accuracy of ±1 ppm. Which is much greater than the 0.01 ppm of the ZL30101. The other factor affecting the accuracy is large jitter on the reference input prior to the mode switch.

4.3.3 Normal Mode

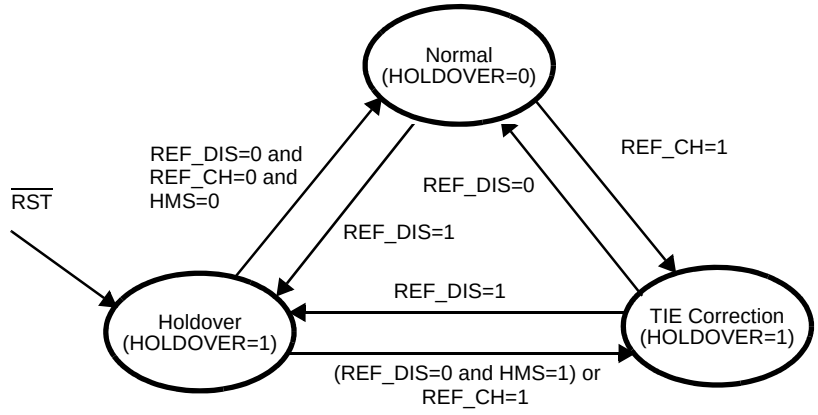
Normal mode is typically used when a system clock source, synchronized to the network is required. In Normal mode, the ZL30101 provides timing and frame synchronization signals, which are synchronized to one of two reference inputs (REF0 or REF1). The input reference signal may have a nominal frequency of 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz. The frequency of the reference inputs are automatically detected by the reference monitors.

When the ZL30101 comes out of RESET while Normal mode is selected by its MODE_SEL pins then it will initially go into Holdover mode and generate clocks with the accuracy of its free running local oscillator (see Figure 9). If the ZL30101 determines that its selected reference is disrupted (see Figure 3), it will remain in Holdover until the selected reference is no longer disrupted or the external controller selects another reference that is not disrupted. If the ZL30101 determines that its selected reference is not disrupted (see Figure 3) then the state machine will cause the DPLL to recover from Holdover via one of two paths depending on the logic level at the HMS pin. If HMS=0 then the ZL30101 will transition directly to Normal mode and it will align its output signals with its selected input reference (see Figure 7). If HMS=1 then the ZL30101 will transition to Normal mode via the TIE correction state and the phase difference between the output signals and the selected input reference will be maintained.

When the ZL30101 is operating in Normal mode, if it determines that its selected reference is disrupted (Figure 3) then its state machine will cause it to automatically go to Holdover mode. When the ZL30101 determines that its selected reference is not disrupted then the state machine will cause the DPLL to recover from Holdover via one of two paths depending on the logic level at the HMS pin (see Figure 9). If HMS=0 then the ZL30101 will transition directly to Normal mode and it will align its output signals with its input reference (see Figure 7). If HMS=1 then the ZL30101 will transition to Normal mode via the TIE correction state and the phase difference between the output signals and the input reference will be maintained.

If the reference selection changes because the value of the REF_SEL1:0 pins changes, the ZL30101 goes into Holdover mode and returns to Normal mode through the TIE correction state regardless of the logic value on HMS pin.

The ZL30101 provides a wide bandwidth loop filter setting (BW_SEL=1), which enables the PLL to lock to an incoming reference in approximately 1 s.



REF_DIS=1: Current selected reference disrupted (see Figure 3). This is an internal signal.

REF_CH= 1: Reference change, a change in the REF_SEL pin. This is an internal signal.

Figure 9 - Mode Switching in Normal Mode

4.4 Reference Selection

The active reference input (REF0, REF1) is selected by the REF_SEL pin as shown in Table 4. If the logic value of the REF_SEL pin is changed when the DPLL is in Normal mode, the ZL30101 will perform a hitless reference switch.

REF_SEL (input pin)	**Input Reference Selected**
0	REF0
1	REF1

Table 4 - Reference Selection

When the REF_SEL inputs are used to force a change from the currently selected reference to another reference, the action of the LOCK output will depend on the relative frequency and phase offset of the old and new references. Where the new reference has enough frequency offset and/or TIE-corrected phase offset to force the output outside the phase-lock-window, the LOCK output will de-assert, the lock-qualify timer is reset, and LOCK will stay de-asserted for the full lock-time duration. Where the new reference is close enough in frequency and TIE-corrected phase for the output to stay within the phase-lock-window, the LOCK output will remain asserted through the reference-switch process.

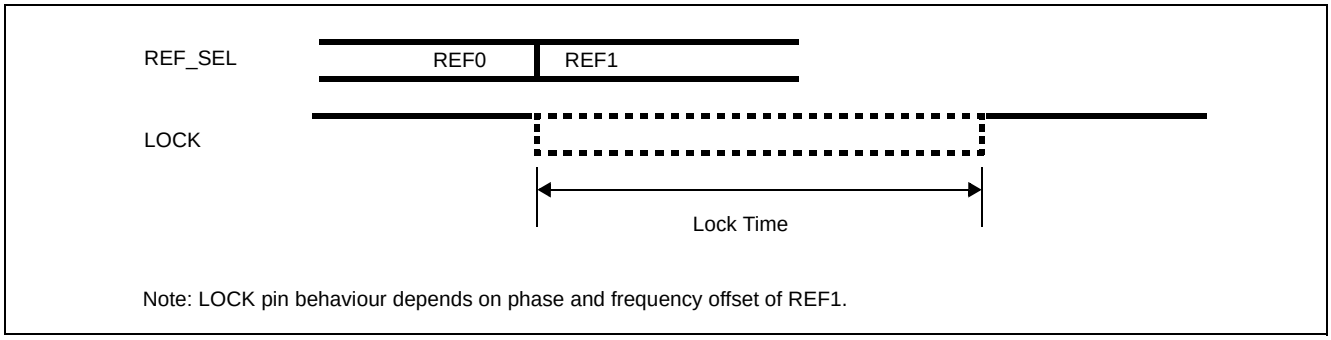


Figure 10 - Reference Switching in Normal Mode

5.0 Measures of Performance

The following are some PLL performance indicators and their corresponding definitions.

5.1 Jitter

Timing jitter is defined as the high frequency variation of the clock edges from their ideal positions in time. Wander is defined as the low-frequency variation of the clock edges from their ideal positions in time. High and low frequency variation imply phase oscillation frequencies relative to some demarcation frequency. (Often 10 Hz or 20 Hz for DS1 or E1, higher for SONET/SDH clocks.) Jitter parameters given in this data sheet are total timing jitter numbers, not cycle-to-cycle jitter.

5.2 Jitter Generation (Intrinsic Jitter)

Generated jitter is the jitter produced by the PLL and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Generated jitter may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Generated jitter is usually measured with various bandlimiting filters depending on the applicable standards.

5.3 Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

5.4 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the Zarlink digital PLLs two internal elements determine the jitter attenuation; the internal low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to, for example, 61 μs/s. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated).

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (for example 75% of the specified maximum tolerable input jitter).

5.5 Frequency Accuracy

Frequency accuracy is defined as the absolute accuracy of an output clock signal when it is not locked to an external reference, but is operating in a free running mode.

5.6 Holdover Accuracy

Holdover accuracy is defined as the absolute accuracy of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the ZL30101, the storage value is determined while the device is in Normal Mode and locked to an external reference signal.

5.7 Pull-in Range

Also referred to as capture range. This is the input frequency range over which the PLL must be able to pull into synchronization.

5.8 Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization.

5.9 Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal. Another way of specifying the phase slope is as the fractional change per time unit. For example; a phase slope of 61 μs/s can also be specified as 61 ppm.

5.10 Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

5.11 Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

5.12 Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the PLL after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

5.13 Lock Time

This is the time it takes the PLL to frequency lock to the input signal. Phase lock occurs when the input signal and output signal are aligned in phase with respect to each other within a certain phase distance (not including jitter). Lock time is affected by many factors which include:

- initial input to output phase difference,
- initial input to output frequency difference,
- PLL loop filter bandwidth,

- PLL phase slope limiter,
- in-lock phase distance.

The presence of input jitter makes it difficult to define when the PLL is locked as it may not be able to align its output to the input within the required phase distance, dependent on the PLL bandwidth and the input jitter amplitude and frequency.

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times.

6.0 Applications

This section contains ZL30101 application specific details for power supply decoupling, reset operation, clock and crystal operation.

6.1 Power Supply Decoupling

Jitter levels on the ZL30101 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30101 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Zarlink Application Note ZLAN-178.

6.2 Master Clock

The ZL30101 can use either a clock or crystal as the master timing source. Zarlink application note ZLAN-68 lists a number of applicable oscillators and crystals that can be used with the ZL30101.

6.2.1 Clock Oscillator

When selecting a clock oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, phase noise, output rise and fall times, output levels and duty cycle.

1	Frequency	20 MHz
2	Tolerance	4.6 ppm
3	Rise & fall time	< 10 ns
4	Duty cycle	40% to 60%

Table 5 - Typical Clock Oscillator Specification

The output clock should be connected directly (not AC coupled) to the OSCi input of the ZL30101, and the OSCo output should be left open as shown in Figure 11.

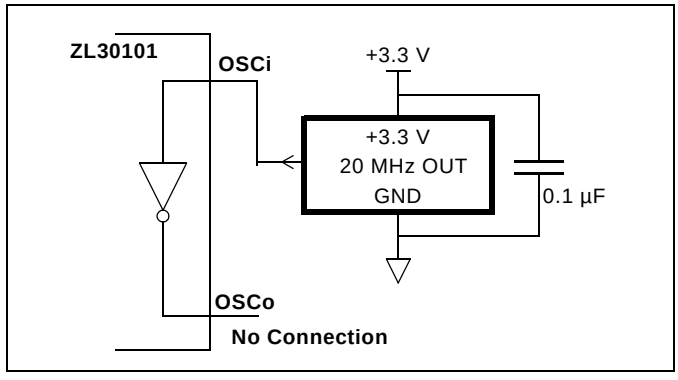


Figure 11 - Clock Oscillator Circuit

6.2.2 Crystal Oscillator

Alternatively, a crystal oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 12. The Telcordia GR1244-CORE Stratum 3 requirements for holdover stability and freerun accuracy may not be met with this crystal oscillator circuit.

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. A typical crystal oscillator specification and circuit is shown in Table 6 and Figure 12 respectively.

1	Frequency	20 MHz
2	Tolerance	as required
3	Oscillation mode	fundamental
4	Resonance mode	parallel
5	Load capacitance	as required
6	Maximum series resistance	50 Ω

Table 6 - Typical Crystal Oscillator Specification

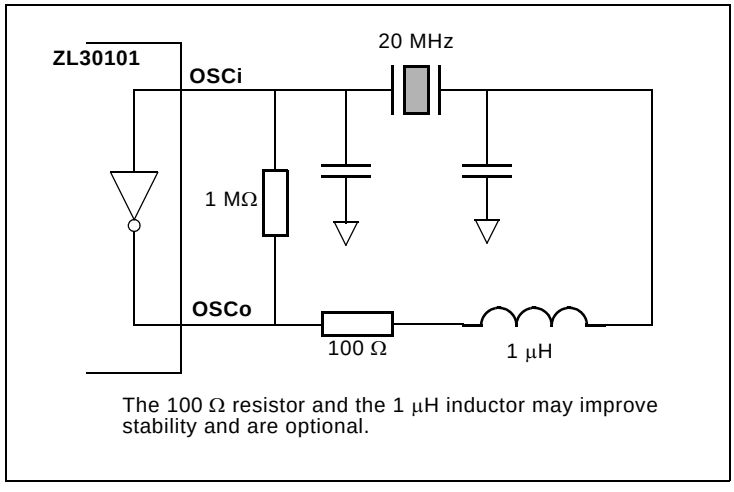


Figure 12 - Crystal Oscillator Circuit

6.3 Power Up Sequence

The ZL30101 requires that the 3.3 V rail is not powered-up later than the 1.8 V rail. This is to prevent the risk of latch-up due to the presence of parasitic diodes in the IO pads.

Two options are given:

1. Power up the 3.3 V rail fully first, then power up the 1.8 V rail

2. Power up the 3.3 V rail and 1.8 V rail simultaneously, ensuring that the 3.3 V rail voltage is never lower than the 1.8 V rail voltage minus a few hundred millivolts (e.g., by using a schottky diode or controlled slew rate)

6.4 Reset Circuit

A simple power up reset circuit with about a 60 μs reset low time is shown in Figure 13. Resistor R_P is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

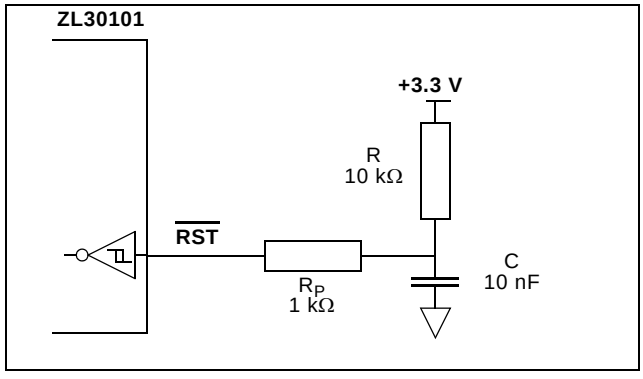


Figure 13 - Power-Up Reset Circuit

7.0 Characteristics

7.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on OSCi and OSCo pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Current on any pin	I_{PIN}		30	mA
6	Storage temperature	T_{ST}	-55	125	°C
7	TQFP 64 pin package power dissipation	P_{PD}		500	mW
8	ESD rating	V_{ESD}		2	kV

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated.

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	2.97	3.30	3.63	V
2	Core supply voltage	V_{CORE}	1.62	1.80	1.98	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	Supply current with: OSCi = 0 V	I_{DDS}	3.0	6.5	mA	outputs loaded with 30 pF
2	OSCi = Clock, OUT_SEL=0	I_{DD}	32	52	mA	
3	OSCi = Clock, OUT_SEL=1	I_{DD}	42	71	mA	
4	Core supply current with: OSCi = 0 V	I_{CORES}	0	22	µA	
5	OSCi = Clock	I_{CORE}	14	20	mA	
6	Schmitt trigger Low to High threshold point	V_{t+}	1.43	1.85	V	All device inputs are Schmitt trigger type.
7	Schmitt trigger High to Low threshold point	V_{t-}	0.80	1.10	V	
8	Input leakage current	I_{IL}	-105	105	µA	$V_I = V_{DD}$ or 0 V
9	High-level output voltage	V_{OH}	2.4		V	I_{OH} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs
10	Low-level output voltage	V_{OL}		0.4	V	I_{OL} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

AC Electrical Characteristics* - Timing Parameter Measurement Voltage Levels (see Figure 14)

	Characteristics	Sym.	CMOS	Units	Notes
1	Threshold voltage	V_T	1.5	V	
2	Rise and fall threshold voltage high	V_{HM}	2.0	V	
3	Rise and fall threshold voltage low	V_{LM}	0.8	V	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

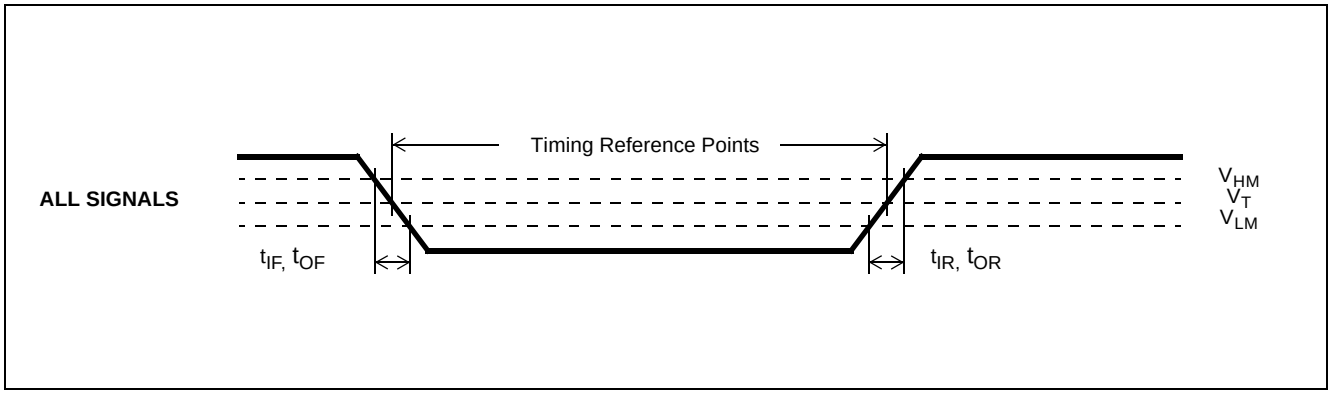


Figure 14 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics* - Input Timing for REF0 and REF1 References (see Figure 15)

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	8 kHz reference period	t_{REF8KP}	121	125	128	µs
2	1.544 MHz reference period	$t_{REF1.5P}$	338	648	950	ns
3	2.048 MHz reference period	t_{REF2P}	263	488	712	ns
4	8.192 MHz reference period	t_{REF8P}	63	122	175	ns
5	16.384 MHz reference period	t_{REF16P}	38	61	75	ns
6	reference pulse width high or low	t_{REFW}	15			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Period Min/Max values are the limits to avoid a single-cycle fault detection. Short-term and long-term average periods must be within Out-of-Range limits.

AC Electrical Characteristics* - Input to Output Timing for REF0 and REF1 References (see Figure 15)

	Characteristics	Symbol	Min.	Max.	Units
1	8 kHz reference input to F8/F32o delay	t_{REF8KD}	0.7	2.0	ns
2	1.544 MHz reference input to C1.5o delay	$t_{REF1.5D}$	2.4	3.0	ns
3	1.544 MHz reference input to F8/F32o delay	$t_{REF1.5\_F8D}$	2.5	3.3	ns
4	2.048 MHz reference input to C2o delay	t_{REF2D}	2.0	3.0	ns
5	2.048 MHz reference input to F8/F32o delay	t_{REF2_F8D}	2.2	3.3	ns
6	8.192 MHz reference input to C8o delay	t_{REF8D}	5.2	6.2	ns
7	8.192 MHz reference input to F8/F32o delay	t_{REF8_F8D}	5.5	6.3	ns
8	16.384 MHz reference input to $\overline{C16o}$ delay	t_{REF16D}	2.6	3.3	ns
9	16.384 MHz reference input to F8/F32o delay	t_{REF16_F8D}	-28.0	-27.2	ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

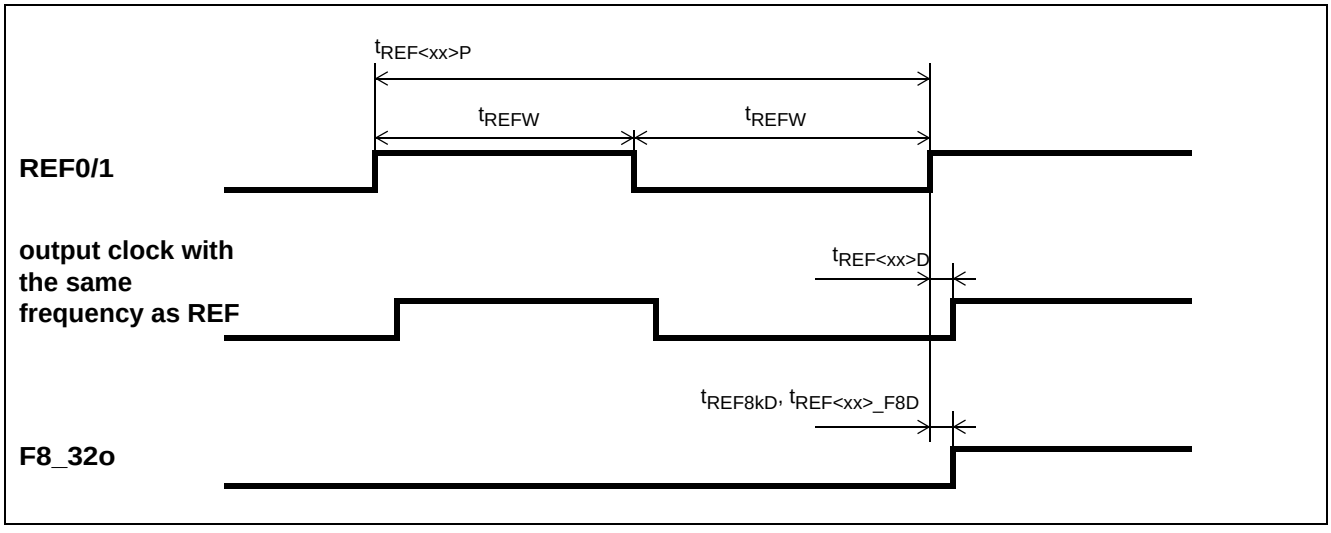
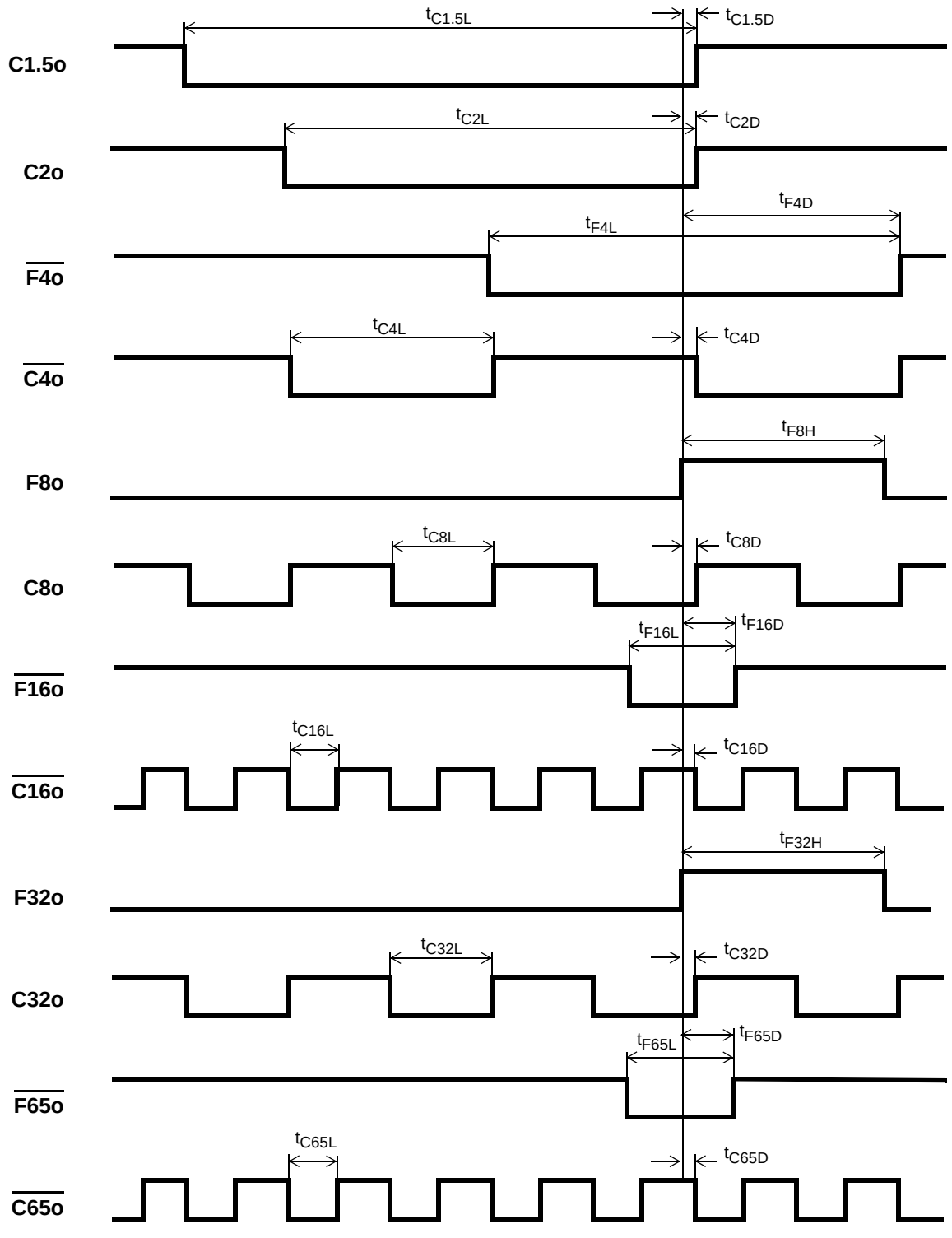


Figure 15 - Input to Output Timing

AC Electrical Characteristics* - Output Timing (see Figure 16)

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	C1.5o pulse width low	$t_{C1.5L}$	323.1	323.7	ns	outputs loaded with 30 pF
2	C1.5o delay	$t_{C1.5D}$	-0.6	0.6	ns	
3	C2o pulse width low	t_{C2L}	243.2	243.8	ns	
4	C2o delay	t_{C2D}	-0.4	0.3	ns	
5	$\overline{\text{F4o}}$ pulse width low	t_{F4L}	243.5	244.2	ns	
6	$\overline{\text{F4o}}$ delay	t_{F4D}	121.5	122.2	ns	
7	$\overline{\text{C4o}}$ pulse width low	t_{C4L}	121.2	122.3	ns	
8	$\overline{\text{C4o}}$ delay	t_{C4D}	-0.3	1.0	ns	
9	F8o pulse width high	t_{F8H}	121.6	123.2	ns	
10	C8o pulse width low	t_{C8L}	60.3	61.2	ns	
11	C8o delay	t_{C8D}	-0.4	0.2	ns	
12	$\overline{\text{F16o}}$ pulse with low	t_{F16L}	60.6	61.1	ns	
13	$\overline{\text{F16o}}$ delay	t_{F16D}	29.9	30.8	ns	
14	$\overline{\text{C16o}}$ pulse width low	t_{C16L}	28.7	30.8	ns	
15	$\overline{\text{C16o}}$ delay	t_{C16D}	-0.5	1.4	ns	
16	F32o pulse width high	t_{F32H}	30.0	31.8	ns	
17	C32o pulse width low	t_{C32L}	14.8	15.3	ns	
18	C32o delay	t_{C32D}	-0.5	0.1	ns	
19	$\overline{\text{F65o}}$ pulse with low	t_{F65L}	14.8	15.4	ns	
20	$\overline{\text{F65o}}$ delay	t_{F65D}	7.1	8.0	ns	
21	$\overline{\text{C65o}}$ pulse width low	t_{C65L}	7.2	8.1	ns	
22	$\overline{\text{C65o}}$ delay	t_{C65D}	-1.0	0.0	ns	
23	Output clock and frame pulse rise time	t_{OR}	1.0	2.0	ns	
24	Output clock and frame pulse fall time	t_{OF}	1.2	2.3	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.



F32o, C32o, F65o and C65o are drawn on a larger scale than the other waveforms in this diagram.

Figure 16 - Output Timing Referenced to F8/F32o

AC Electrical Characteristics* - OSCi 20 MHz Master Clock Input

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	Oscillator tolerance		-4.6	4.6	ppm	
2	Duty cycle		40	60	%	
3	Rise time			10	ns	
4	Fall time			10	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

7.2 Performance Characteristics

Performance Characteristics* - Functional

	Characteristics	Min.	Max.	Units	Notes
1	Holdover accuracy		0.01	ppm	
2	Holdover stability		0	ppm	Determined by stability of the 20 MHz master clock oscillator
3	Freerun accuracy		0	ppm	Determined by accuracy of the 20 MHz master clock oscillator
4	Capture range	-12	+12	ppm	The 20 MHz master clock oscillator set at 0 ppm
5	Reference Out of Range Threshold (including hysteresis)	-9.2 -12	+9.2 +12	ppm	The 20 MHz master clock oscillator set at 0 ppm
Lock Time					
7	1.8 Hz loop filter		40	s	±12 ppm frequency offset, HMS=1, TIE_CLR=1, BW_SEL=0
8	58 Hz and 922 Hz loop filter		1	s	±12 ppm frequency offset, HMS=1, TIE_CLR=1, BW_SEL=1
Output Phase Continuity (MTIE)					
9	Reference switching		13	ns	
10	Switching from Normal mode to Holdover mode		0	ns	
11	Switching from Holdover mode to Normal mode		13	ns	
Output Phase Slope					
12	1.8 Hz Filter		61	µs/s	BW_SEL=0
13	58 Hz and 922 Hz Filter		9.5	ms/s	BW_SEL=1

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics*: Output Jitter Generation - ANSI T1.403 Conformance

	Signal	ANSI T1.403 Jitter Generation Requirements			ZL30101 maximum jitter generation	Units
		Jitter measurement filter	Limit in UI	Equivalent limit in the time domain		
DS1 Interface						
1	C1.5o (1.544 MHz)	8 kHz to 40 kHz	0.07 UI_{pp}	45.3	0.30	ns_{pp}
2		10 Hz to 40 kHz	0.5 UI_{pp}	324	0.32	ns_{pp}

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics*: Output Jitter Generation - ITU-T G.812 Conformance

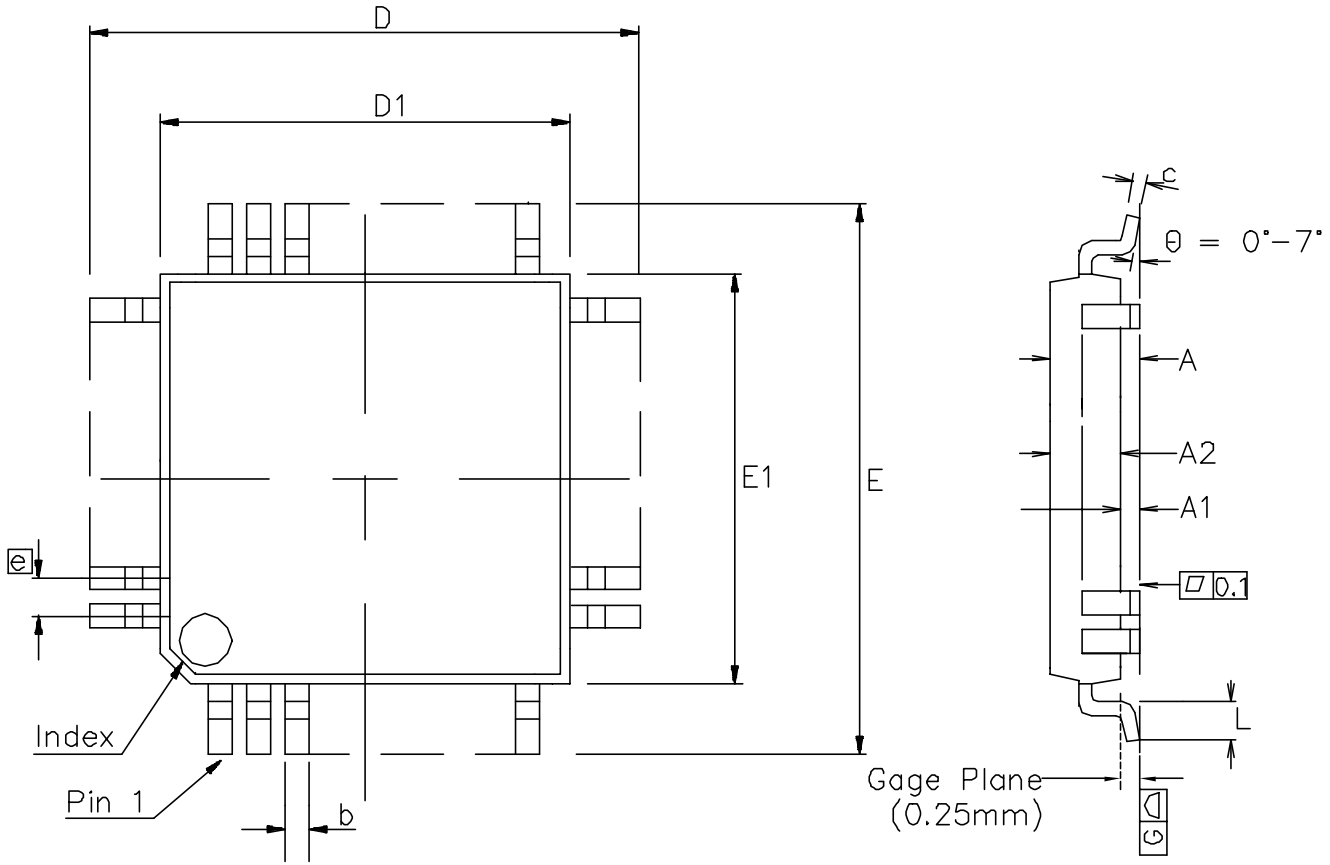
	Signal	ITU-T G.812 Jitter Generation Requirements			ZL30101 maximum jitter generation	Units
		Jitter measurement filter	Limit in UI	Equivalent limit in the time domain		
E1 Interface						
1	C2o (2.048 MHz)	20 Hz to 100 kHz	0.05 UI_{pp}	24.4	0.36	ns_{pp}

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics* - Unfiltered Intrinsic Jitter

	Characteristics	Max. [ns_{pp}]	Notes
1	C1.5o (1.544 MHz)	0.45	
2	C2o (2.048 MHz)	0.47	
3	$\overline{\text{C4o}}$ (4.096 MHz)	0.42	
4	C8o (8.192 MHz)	0.42	
5	$\overline{\text{C16o}}$ (16.384 MHz)	0.56	
6	C32o (32.768 MHz)	0.46	
7	$\overline{\text{C65o}}$ (65.536 MHz)	0.49	
8	$\overline{\text{F4o}}$ (8 kHz)	0.40	
9	F8o (8 kHz)	0.33	
10	$\overline{\text{F16o}}$ (8 kHz)	0.43	
11	F32o (8 kHz)	0.36	
12	$\overline{\text{F65o}}$ (8 kHz)	0.42	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	12.00 BSC			0.472 BSC	
D1	10.00 BSC			0.394 BSC	
E	12.00 BSC			0.472 BSC	
E1	10.00 BSC			0.394 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	64				
ND	16				
NE	16				
NOTE	SQUARE				

Conforms to JEDEC MS-026 ACD Iss. C

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protrusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

ISSUE	1	2	3	4
ACN	203170	207075	213856	CDCA
DATE	14Oct97	5Jul99	17Dec02	15Aug05
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

TP/TH

Package Code QD/QG

Package Outline for 64 Lead TQFP 10x10x1.0mm, +2.0mm (footprint)

GPD00450

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