VX-805

Voltage Controlled Crystal Oscillator

Description

The VX-805 is a Voltage Control Crystal Oscillator that operates at the fundamental frequency of the internal crystal. The crystal is a high-Q quartz device that enables the circuit to achieve low phase noise jitter performance over a wide operating temperature range. The VX-805 is housed in an industry standard hermetically sealed LCC package and is available in tape and reel.

Features

- CMOS output VCXO, 30-170MHz
- LVPECL output VCXO, 100 - 204.8 MHz
- LVDS output VCXO, 60 - 200 MHz
- 3.3 V Operation, 2.5 V LVDS
- Fundamental Crystal Design with Low Jitter Performance
- Output Disable Feature
- Excellent ±20 ppm Temperature Stability
- 0/70°C, -40/85°C or -40/105°C Operating Temperature
- Small Industry Standard 5.0x3.2 mm Package
- Product is free of lead and compliant to EC RoHS Directive

Applications

- 5G
- LTE
- SONET/SDH/DWDM
- Ethernet, SyncE, GE
- xDSL, PCMIA
- Digital Video
- Broadband Access
- Base Stations, Picocells

Block Diagram

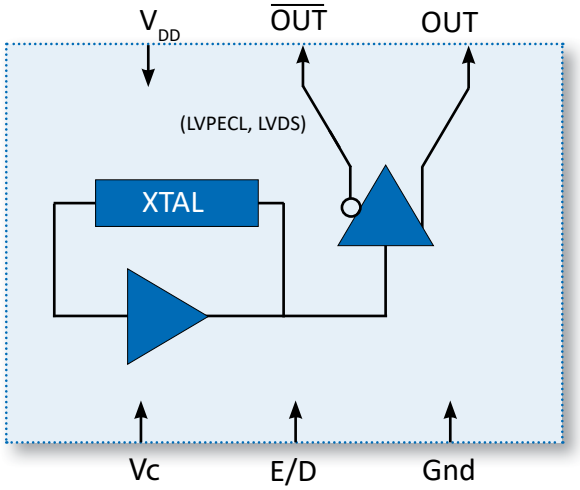

Figure 1. Block Diagram

Performance Specifications

Table 1. Electrical Performance - 3.3V CMOS

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	3.135	3.3	3.465	V
Current[2] , f_{out} < 100MHz f_{out} ≥ 100MHz	I_{DD}			15 25	mA mA
Frequency					
Nominal Frequency[3]	f_N	30		170	MHz
Absolute Pull Range [2,6], *ordering option*	APR		±30 or ±50		ppm
Linearity[2]	Lin		5		%
Gain Transfer[2,] 77.76MHz	K_V		+100		ppm/V
Temperature Stability	f_{STAB}		±20		ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-0.4		 0.4	 V V
Output Drive Levels I_{OH} I_{OL} I_{OH} f_{out} ≥ 100MHz I_{OL} f_{out} ≥ 100MHz	I_{OUT}	 4 8		 -4 -8	 mA mA mA mA
Load	t_R			15	pF
Rise/Fall Time[2,4] f_O > 100MHz	t_F			3 2.4	ns
Symmetry[2]	SYM	45	50	55	%
Phase Noise[8] (122.88 MHz) 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			 -66 -98 -124 -138 -151 -158 -161		dBc/Hz
Control Voltage					
Control Voltage Range for Pull Range	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	10			MΩ
Control Voltage Modulation BW	BW	20			kHz
Output Enable/Disable[9] Output Enabled Output Disabled	 V_{IH} V_{IL}	 0.7*V_{DD}		 0.3*V_{DD}	V
Start-Up and Enable Time[9] Disable Time	T_S			10 200	ms ns
Operating Temp, Ordering Option	T_{OP}		0/70, -20/70 or -40/85		°C
Package Size			5.0 x 3.2 x 1.2		mm

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01uF
2] Parameters are tested with production test circuit as shown in Figure 2.
3] See Standard Frequencies and Ordering Information tables for more specific information
4] Measured from 20% to 80% of a full output swing as shown in Figure 5.
5] Not tested in production, guaranteed by design, verified at qualification.
6] Tested with Vc = 0.3V to 3.0V unless otherwise stated in part description
7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
8] Phase Noise is measured with an Agilent E5052A.
9] The Output is Enabled if the Enable/Disable is left open. The output will be glitch-free upon start up and enable.

Performance Specifications

Table 2. Electrical Performance - 3.3V LVPECL

Parameter	Symbol	Min	Typical	Max	Units
Supply					
Voltage[1]	V_{DD}	3.135	3.3	3.465	V
Current[2]	I_{DD}		50	90	mA
Frequency					
Nominal Frequency	f_N	100		204.8	MHz
Absolute Pull Range [2,6], *ordering option*	APR		±30, ±50		ppm
Linearity[2]	Lin		5		%
Gain Transfer[2]	K_V		+80		ppm/V
Temperature Stability[3]	f_{STAB}		±20		ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-1.025 V_{DD}-1.810	 V_{DD}-0.950 V_{DD}-1.700	 V_{DD}-0.880 V_{DD}-1.620	 V V
Rise Time[2,4]	t_R		0.3	0.5	ns
Fall Time[2,4]	t_F		0.3	0.5	ns
Symmetry[2] Symmetry[2] (-40 °C to 105 °C)	SYM	45 40	50 50	55 60	% %
Jitter, RMS [5,7] (12kHz to 20 MHz)	ϕJ		0.2	0.5	ps
Phase Noise[7], 122.88MHz 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			 -68 -98 -125 -148 -157 -157 -157		dBc/Hz
Control Voltage					
Control Voltage Range for Pull Range	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	10			MΩ
Control Voltage Modulation BW	BW	20			kHz
Output Enable/Disable[8] Output Enabled, Option A Output Disabled, Option A	 V_{IH} V_{IL}	 0.9*V_{DD}		 0.1*V_{DD}	V
Start-Up Time	T_S			10	ms
Operating Temp, *Ordering Option*	T_{OP}		0/70 or -40/85 or -40/105		°C
Package Size			5.0 x 3.2 x 1.2		mm

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01uF
2] Parameters are tested with production test circuit below as shown in Figure 3.
3] ±20ppm temperature stability is not available for -40 °C to 105 °C temperature range
4] Measured from 20% to 80% of a full output swing as shown in Figure 5.
5] Not tested in production, guaranteed by design, verified at qualification.
6] Tested with Vc = 0V to 3.3V unless otherwise stated in part description
7] Phase Noise is measured with an Agilent E5052A Signal Source Analyzer.
8] The Output is Enabled if the Enable/Disable is left open.

Performance Specifications

Table 3. Electrical Performance - LVDS

Parameter	Symbol	Min	Typical	Max	Units
Supply					
Voltage[1], 3.3V, *ordering option* 2.5V	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current[2], 3.3V 2.5V	I_{DD}			30 23	mA mA
Frequency					
Nominal Frequency	f_N	60		200	MHz
Absolute Pull Range [2,6], *ordering option*	APR		±30, ±50		ppm
Linearity[2]	Lin		5		%
Gain Transfer[2]	K_V		+80		ppm/V
Temperature Stability[3]	f_{STAB}		±20		ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.90	 1.43 1.1	 1.60 	 V V
Diffferntial Output Voltage		247	350	454	V
DIfferential Output Voltage Error				50	mV
Offset Voltage		1.125	1.250	1.375	V
Offset Voltage Error				50	mV
Rise Time[2,4]	t_R		0.4	0.7	ns
Fall Time[2,4]	t_F		0.4	0.7	ns
Symmetry[2])	SYM	45	50	55	%
Jitter, RMS [5,7] (12kHz to 20 MHz)	ϕJ		0.2		ps
Phase Noise[7], 122.88MHz 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			 -68 -98 -124 -147 -153 -157 -161		dBc/Hz
Control Voltage					
Control Voltage Range for Pull Range	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	10			MΩ
Control Voltage Modulation BW	BW	20			kHz
Enable/Disable					
Output Enable/Disable[8] Output Enabled, Option A Output Disabled, Option A	 V_{IH} V_{IL}	 0.7*V_{DD} 	 	 0.3*V_{DD}	 V V
Start-Up Time	T_S			10	ms
Operating Temp, *Ordering Option*	T_{OP}		0/70 or -40/85 or -40/105		°C
Package Size			5.0 x 3.2 x 1.2		mm

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01uF
2] Parameters are tested with production test circuit as shown in Figure 4.
3] ±20ppm temperature stability is not available for -40 °C to 105 °C temperature range
4] Measured from 20% to 80% of a full output swing as shown in Figure 5.
5] Not tested in production, guaranteed by design, verified at qualification.
6] Tested with Vc = 0V to 3.0V for 3.3V an 0.3 to 2.2V for 2.5V.
7] Phase Noise is measured with an Agilent E5052A Signal Source Analyzer.
8] The Output is Enabled if the Enable/Disable is left open.

Outline Drawing & Pad Layout

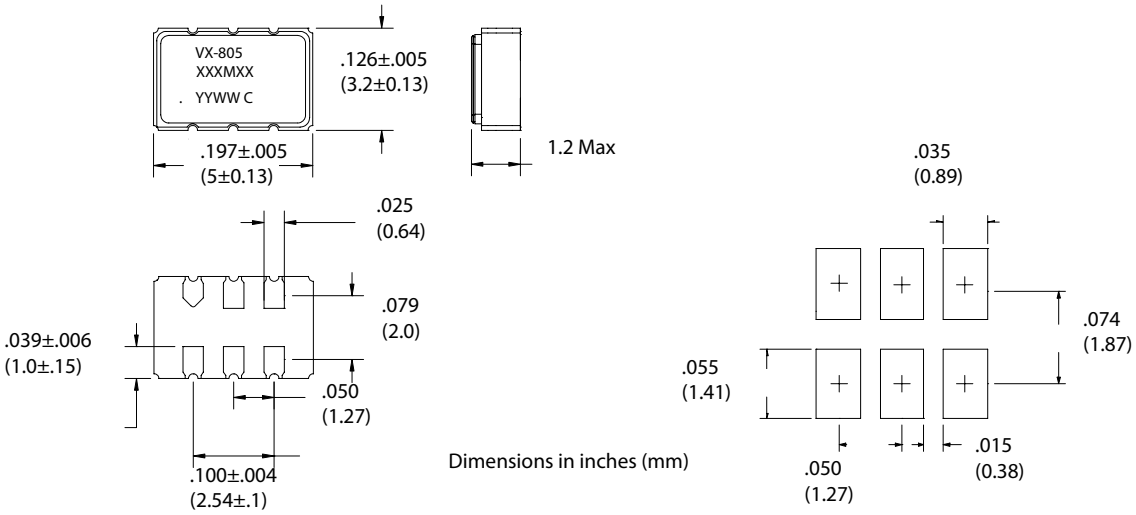

Figure 1. Outline Drawing and Pad Layout

Table 4. LVPECL, LVDS Pin Out

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	E/D	Enable Disable **See Ordering Options**
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{DD}	Power Supply Voltage

Table 5. CMOS Pin Out

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	E/D	Enable Disable **See Ordering Options**
3	GND	Case and Electrical Ground
4	Output	Output
5	NC	No Connect
6	V_{DD}	Power Supply Voltage

Test Circuit

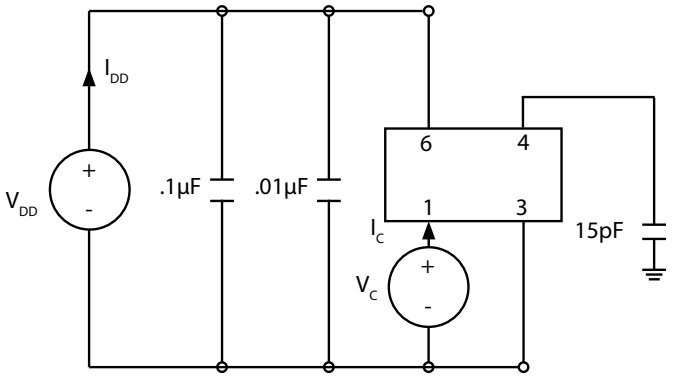

Figure 2. CMOS Test Circuit

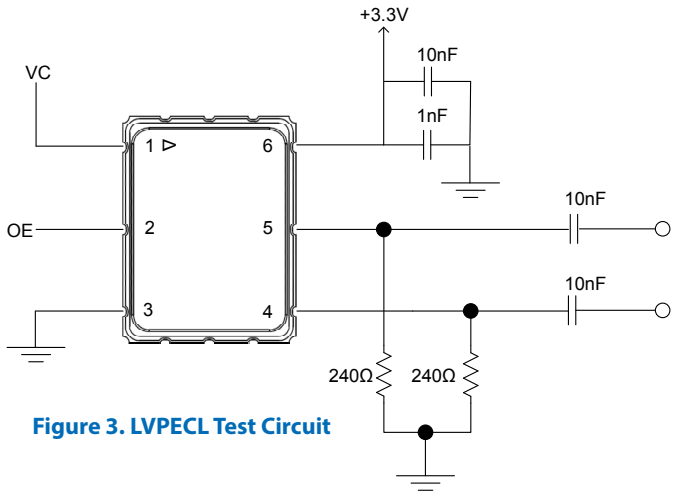

Figure 3. LVPECL Test Circuit

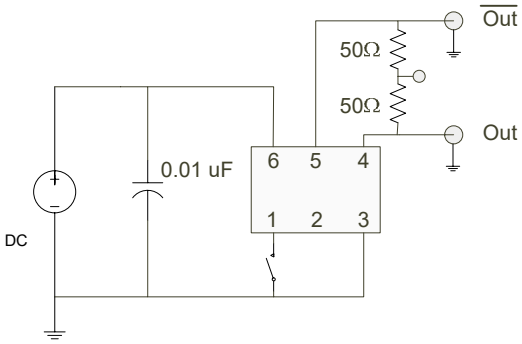

Figure 4. LVDS Test CIrcuit

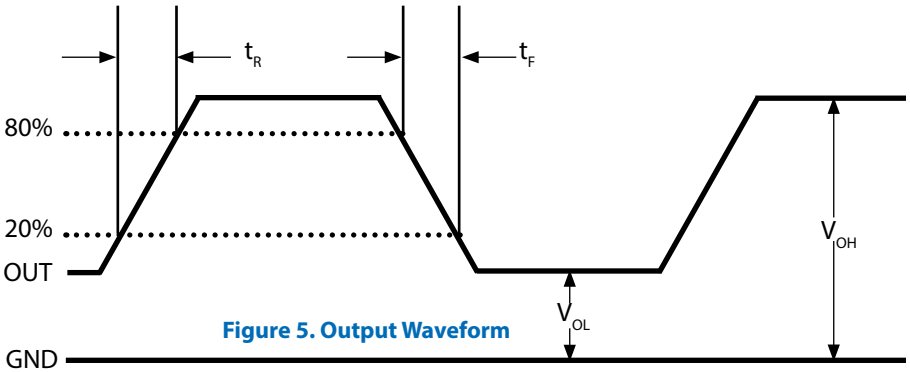

Figure 5. Output Waveform

Tape & Reel (EIA-481-2-A)

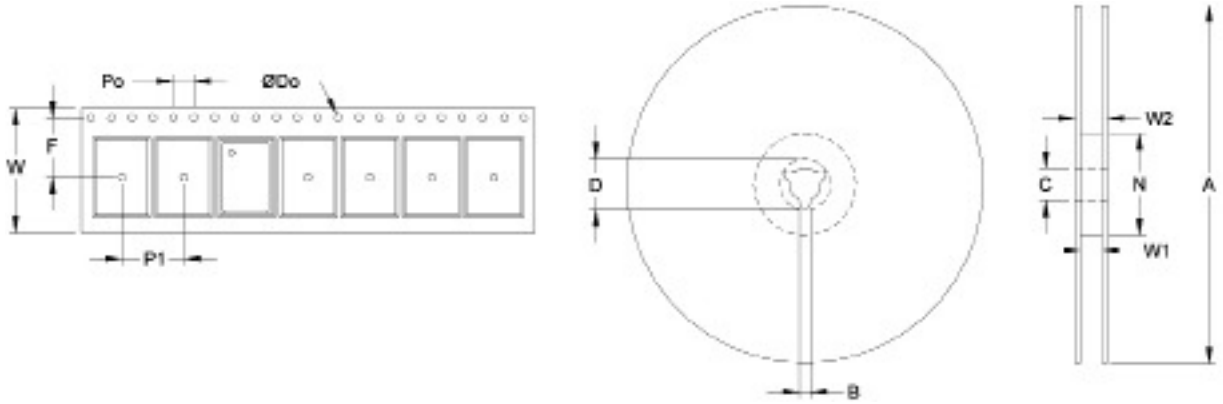

Figure 6. Tape and Reel Drawing

Table 6. Tape and Reel Information													
Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VX-805	12	5.5	1.5	4	8	178	1.78	13	20.6	55	12.4	22.4	1000

Table 7. Absolute Maximum Ratings			
Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	-0.3 to +5.0	V
Voltage Control Range	V_C	-0.3 to V_{DD}+0.3	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 20	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before V_{DD}.

Reliability

Vectron qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VX-805 family is capable of meeting the following qualification tests:

Table 8. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 um min to 1.0um max) over Nickel
Weight	57 mg

Handling Precautions

Although ESD protection circuitry has been designed into the VX-805 proper precautions should be taken when handling and mounting. Vectron employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 9. ESD Ratings

Model	Minimum	Conditions
Human Body Model	500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

Table 10. Reflow Profile

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 260 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_P	30 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VX-805 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating:
Electrolytic Gold Plate over Electrolytic Nickel Plate

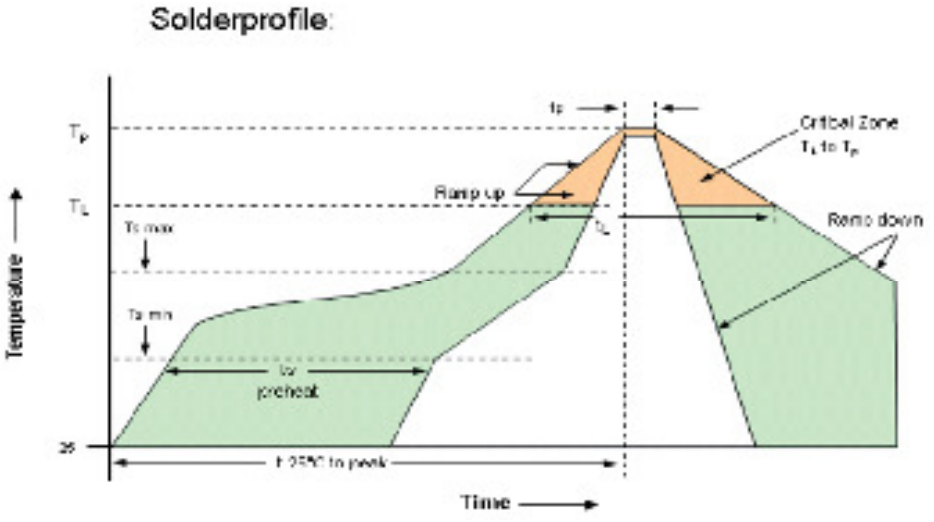

Figure 5. Recommended Reflow Profile

Ordering Information

VX-805- E C T - K A A N- xxxMxxxxxxXX

Product
VCXO, 5.0x3.2 Package

Voltage Options
E: +3.3 Vdc
H: +2.5V (LVDS only)

Output
A: CMOS
C: LVPECL
D: LVDS

Temp Range
T: 0/70°C
E: -40/85°C
F: -40/105°C

Absolute Pull Range
G: ±30 ppm
K: ±50 ppm

Stability
X: Standard
E: ±20 ppm Temperature Stability

Enable/Disable
A: Enable High, Pin 2
C: Enable Low, Pin 2 (LVPECL)
X: No Enable Disable Feature on Pin 2
(No Connect Internally)

Other (Future Use)
N: Standard

Frequency in MHz

Packaging
TR: Tape and Reel
blank: Cut Tape / non Tape and Reel quantities
_SNPB: Tin lead solder dipped

**Note: not all combination of options are available. Other specifications may be available upon request. Please consult with factory.*

Example:

VX-805-ECE-KAAN-122M880000TR	**Tape and Reel**
VX-805-ECE-KAAN-122M880000	**Cut Tape**
VX-805-ECE-KAAN-122M880000_SNPB	**Tin lead solder dipped**

Revision History

Revision Date	Approved	Description
January 21, 2015	VN	Included Extended temperature Range of -40/105°C. Added revision history table.
May 28, 2015	VN	Changed maximum nominal output frequency from 250MHz to 204.8MHz
February 3, 2016	RC	Update Figure 3
January 17, 2017	RC	Update Reflow Profile
August 10, 2018	FB	Updated logo and contactinformation, added "SNPBDIP" odering option
April 15, 2019	FB	Updated logo and contact information, change SNPBDIP to SNPB
April 30, 2020	FB	Add tape and reel, CMOS and LVDS ordering options, updates and corrections as needed

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