VC-830

LVPECL, LVDS Crystal Oscillator

Features

- 40 fs_{RMS} Phase Jitter Typical, 12 kHz to 20 MHz
- 3rd OT or Fundamental Crystal Design
- Extended Operating Temperature Range: –40°C to +105°C
- 100 MHz to 200 MHz Output Frequencies
- Excellent Power Supply Rejection Ratio
- Glitch Free Output upon Power-Up and Enable
- Hermetically Sealed 3.2 mm x 2.5 mm Ceramic Package
- Product is Compliant to RoHS Directive and Fully Compatible with Lead-Free Assembly

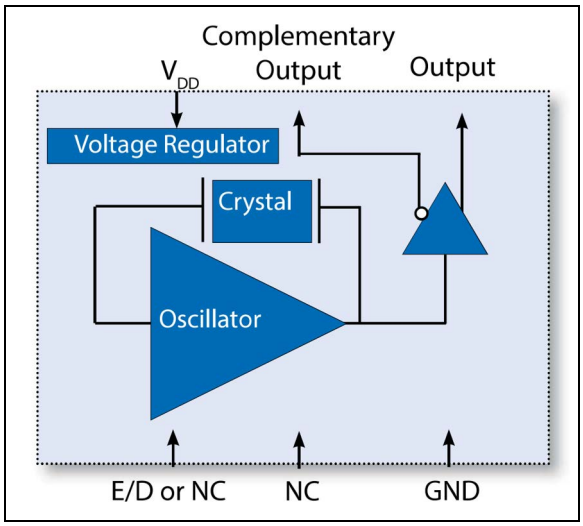
Applications

- Medical, Ultrasound
- Ethernet, GbE, SynchE
- Fibre Channel
- PON
- Clock Source for A/Ds, D/As, FPGAs
- Test and Measurement
- Storage Area Network

General Description

Microchip's VC-830 crystal oscillator is a quartz-stabilized, differential output oscillator that operates off a 2.5V or 3.3V power supply in a hermetically sealed 3.2 mm x 2.5 mm ceramic package.

Block Diagram



Phase Noise Plot

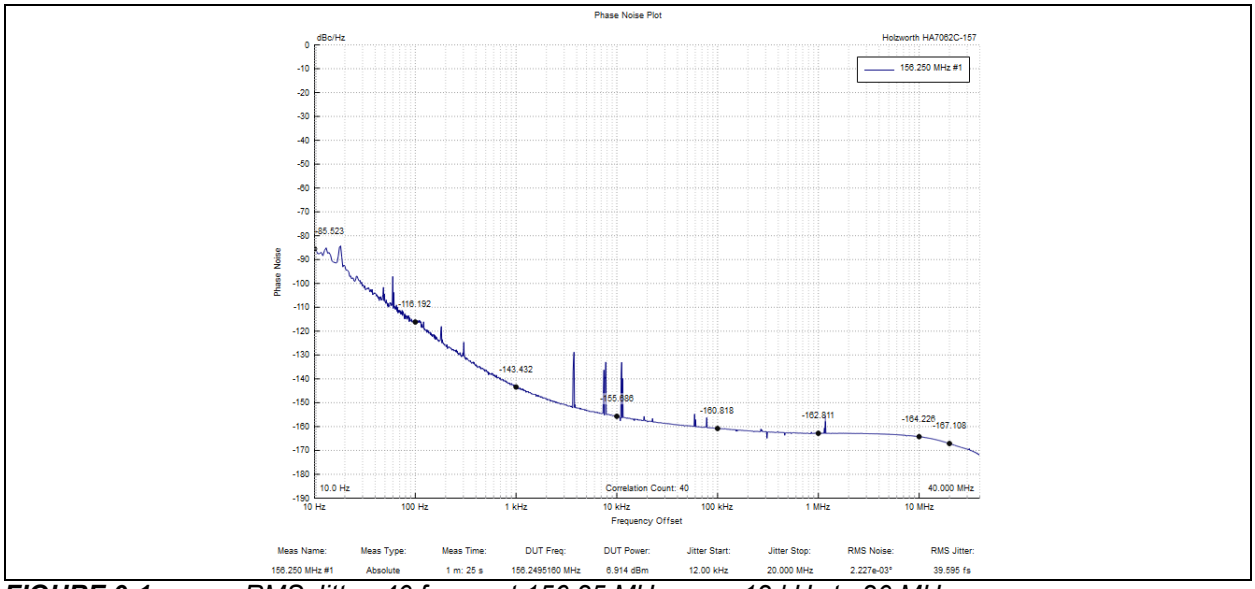


FIGURE 0-1: *RMS Jitter, 40 fs_{RMS} at 156.25 MHz, over 12 kHz to 20 MHz.*

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... –0.3V to +4.5V
Enable Disable Voltage ..... –0.3V to V_{DD} + 0.3V
ESD Rating, Human Body Model (Note 1) ..... 2 kV
ESD Rating, Charged Device Model (Note 1) 200V
Storage Temperature (T_S) ..... –40°C to +125°C
Junction Temperature (T_J) ..... +150°C

† Notice: Stresses in excess of the Absolute Maximum Ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods may adversely affect device reliability.

Note 1: Although ESD protection circuitry has been designed into the VC-830, proper precautions should be taken when handling and mounting. Microchip employs a Human Body Model (HBM) and a Charged Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM, a standard resistance of 1.5 kΩ and capacitance of 100 pF is widely used and therefore can be used for comparison purposes.

ELECTRICAL CHARACTERISTICS, LVPECL OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.375	2.5	2.625	V	Ordering Option
		3.135	3.3	3.465		
Current Consumption	I_{DD}	—	—	66	mA	—
Frequency						
Nominal Frequency	f_N	100	—	200	MHz	Ordering Option
Stability (Note 2)	—	—	—	±25	ppm	Ordering Option
		—	—	±30		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High (Note 3)	V_{OH}	V_{DD} – 1.085	—	V_{DD} – 0.880	V	V_{DD} = +2.5V
Output Logic Level Low (Note 3)	V_{OL}	V_{DD} – 1.810	—	V_{DD} – 1.620		
Output Logic Level High (Note 3)	V_{OH}	V_{DD} – 1.085	—	V_{DD} – 0.880	V	V_{DD} = +3.3V
Output Logic Level Low (Note 3)	V_{OL}	V_{DD} – 1.810	—	V_{DD} – 1.620		

Note 1: The VC-830 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.
2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
3: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.
4: Output rise and fall time will be 600 ps (max.) for –40°C to +105°C operating temperature range.
5: Duty Cycle is measured as On/Time Period.
6: Measured using an Agilent E5052 Signal Source Analyzer at 25°C.
7: Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.
8: In order to reduce current, the pull-up resistance is higher when V_{DD} is set to ground.

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ELECTRICAL CHARACTERISTICS, LVPECL OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Rise and Fall Time (Note 3)	t_r/t_f	—	—	400	ps	Note 4
Load	—	50Ω into V_{DD} – 2.0V			—	—
Duty Cycle (Note 5)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 6)	ϕ_N	—	–79	—	dBc/Hz	10 Hz
		—	–110	—		100 Hz
		—	–130	—		1 kHz
		—	–154	—		10 kHz
		—	–160	—		100 kHz
		—	–163	—		1 MHz
		—	–163	—		10 MHz
		—	–167	—		20 MHz
Phase Jitter, 156.25 MHz, 12 kHz to 20 MHz (Note 6)	ϕ_J	—	40	60	fs	—
Enable/Disable						
Outputs Enabled (Note 7)	V_{IH}	0.7 * V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3 * V_{DD}	V	—
Disable Time	t_D	—	—	200	ns	—
E/D Pull-Up Resistance (Note 8)	—	0.5	—	2	M	E/D = GND
E/D Pull-Up Resistance	—	30	—	150	kΩ	E/D = V_{DD}
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85		
		–40	—	105		

Note 1: The VC-830 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time will be 600 ps (max.) for –40°C to +105°C operating temperature range.

5: Duty Cycle is measured as On/Time Period.

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8: In order to reduce current, the pull-up resistance is higher when V_{DD} is set to ground.

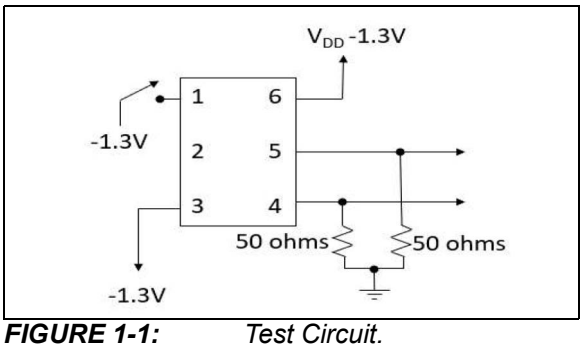

FIGURE 1-1: *Test Circuit.*

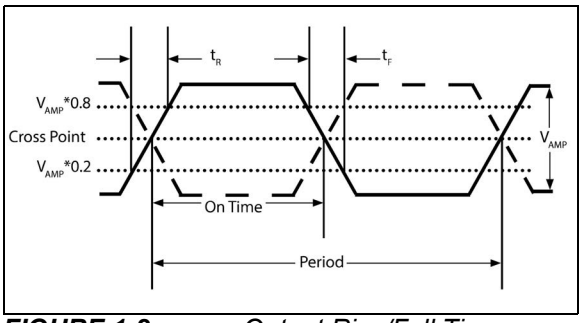

FIGURE 1-2: *Output Rise/Fall Time.*

ELECTRICAL CHARACTERISTICS, LVDS OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.375	2.5	2.625	V	Ordering Option
		3.135	3.3	3.465		
Current Consumption	I_{DD}			29	mA	2.5V
		—	—	30		3.3V
Frequency						
Nominal Frequency	f_N	100	—	200	MHz	Ordering Option
Stability (Note 2)	—	—	—	±25	ppm	Ordering Option
		—	—	±30		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High (Note 3)	V_{OH}	—	1.43	1.6	V	—
Output Logic Level Low (Note 3)	V_{OL}	0.9	1.10	—		
Output Amplitude	—	±247	±350	±454	mV	—
Differential Output Error	—	—	—	50	mV	—
Offset Voltage	—	1.125	1.25	1.375	V	—
Offset Voltage Error	—	—	—	50	mV	—
Output Leakage Current, Outputs Disabled	—	—	—	30	µA	—
Output Rise and Fall Time (Note 3)	t_r/t_f	—	—	300	ps	Note 4
Load	—	100Ω Differential			—	—
Duty Cycle (Note 5)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 6)	ϕ_N	—	–79	—	dBc/Hz	10 Hz
		—	–110	—		100 Hz
		—	–130	—		1 kHz
		—	–154	—		10 kHz
		—	–160	—		100 kHz
		—	–162	—		1 MHz
		—	–163	—		10 MHz
		—	–164	—		20 MHz
Phase Jitter, 156.25 MHz, 12 kHz to 20 MHz (Note 6)	ϕ_J	—	43	64	fs	—

Note 1: The VC-830 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time will be 600 ps (max.) for –40°C to +105°C operating temperature range.

5: Duty Cycle is measured as On/Time Period.

6: Measured using an Agilent E5052 Signal Source Analyzer at 25°C.

7: Outputs will be enabled if Enable/Disable is left open. There is an oscillation detection circuit that ensures glitch free output upon power-up or enable.

8: In order to reduce current, the pull-up resistance is higher when V_{DD} is set to ground.

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ELECTRICAL CHARACTERISTICS, LVDS OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Enable/Disable						
Outputs Enabled (Note 7)	V_{IH}	0.7 * V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3 * V_{DD}	V	—
Disable Time	t_D	—	—	200	ns	—
E/D Pull-Up Resistance (Note 8)	—	0.5	—	2	M	E/D = GND
E/D Pull-Up Resistance	—	30	—	150	kΩ	E/D = V_{DD}
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85		
		–40	—	105		

Note 1: The VC-830 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.

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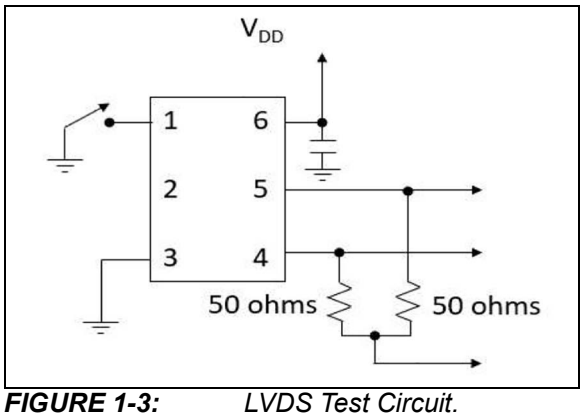

FIGURE 1-3: *LVDS Test Circuit.*

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	E/D	Enable/Disable.
2	NC	No internal connection is made.
3	GND	Electrical and lid ground.
4	f_O	Output frequency.
5	Cf_O	Complementary output frequency.
6	V_{DD}	Supply voltage.

TABLE 2-2: ENABLE/DISABLE FUNCTION

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

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3.0 APPLICATION DIAGRAMS

3.1 LVPECL Application Diagrams

The VC-830 incorporates a standard PECL output scheme, which are unterminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground (Figure 3-1) and a pull-up/pull-down scheme as shown in Figure 3-2. AC-coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated because if one of the two outputs is left open, it will result in excessive jitter on both. PCB layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

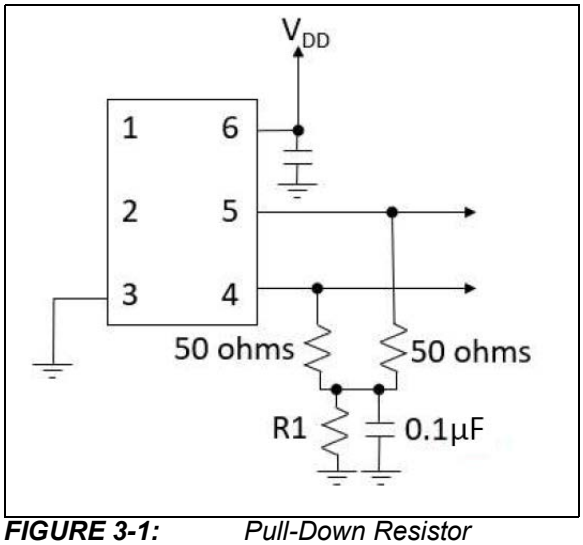

FIGURE 3-1: *Pull-Down Resistor Termination Scheme.*

Figure 3-1 shows one option to terminate LVPECL outputs and is optimized to reduce common mode noise. R1 is 50Ω for 3.3V supply voltage and 18Ω for 2.5V.

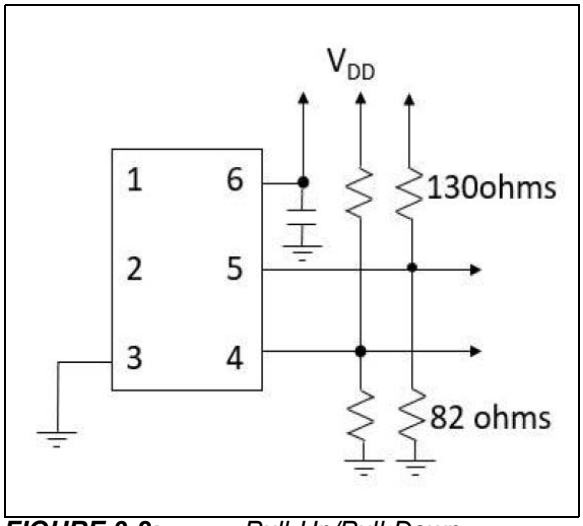

FIGURE 3-2: *Pull-Up/Pull-Down Termination.*

Resistor values shown are typical for 3.3V operation. For 2.5V operation, the resistor to ground is 62Ω and the resistor to supply is 250Ω.

3.2 LVDS Application Diagrams

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated because if one of the two outputs is left open, it will result in excessive jitter on both. PCB layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

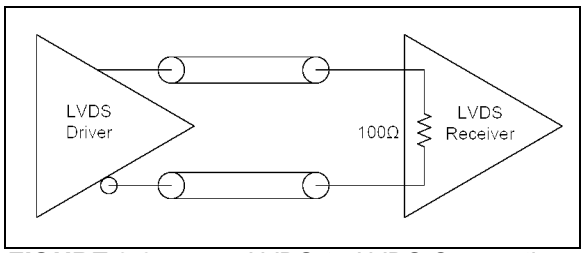

FIGURE 3-3: *LVDS-to-LVDS Connection, Internal 100Ω Resistor.*

Some LVDS structures have an internal 100Ω resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.

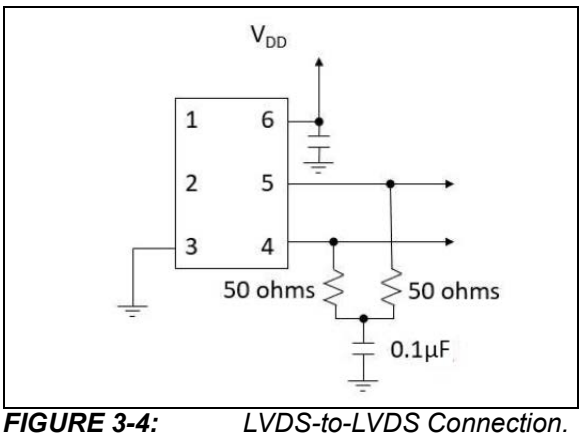

FIGURE 3-4: *LVDS-to-LVDS Connection.*

Some input structures may not have an internal 100Ω resistor on the input and will need an external 100Ω resistor located at the receiver for impedance matching. Figure 3-4 is optimized to reduce common mode noise. Additionally, the input may have an internal DC bias that may not be compatible with LVDS levels. AC blocking capacitors, such as 0.1 µF, should be used in this case.

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4.0 RELIABILITY

Microchip qualification will include aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-830 family is capable of meeting the following qualification tests.

TABLE 4-1: ENVIRONMENTAL COMPLIANCE

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 µm min., 1.0 µm max.) over Nickel
θ_{JC} (Bottom of Case)	28°C/W
Maximum Junction Temperature	150°C
Weight	23 mg

5.0 IR REFLOW

Devices are built using lead-free epoxy and can be subjected to standard lead-free IR reflow conditions shown in Table 5-1. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220°C.

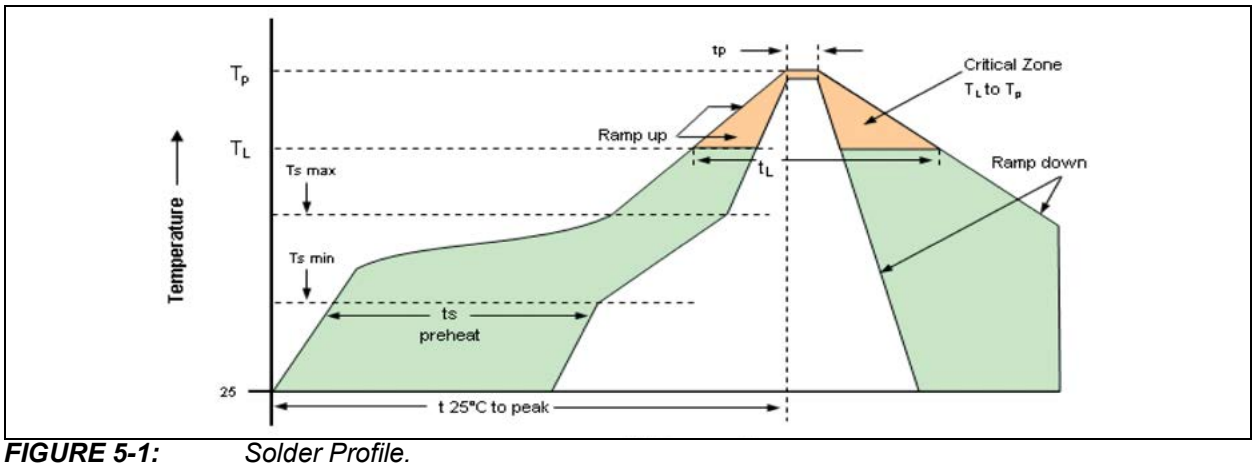

FIGURE 5-1: *Solder Profile.*

TABLE 5-1: REFLOW PROFILE

Parameter	Symbol	Value
Pre-Heat Time	t_S	200 seconds maximum
Ramp Up	R_{UP}	3°C/sec. maximum
Time above 217°C	t_L	150 seconds maximum
Time to Peak Temperature	T_{AMB-P}	480 seconds maximum
Time at 260°C	t_P	30 seconds maximum
Time at 240°C	t_{P2}	60 seconds maximum
Ramp Down	R_{DN}	6°C/sec. maximum

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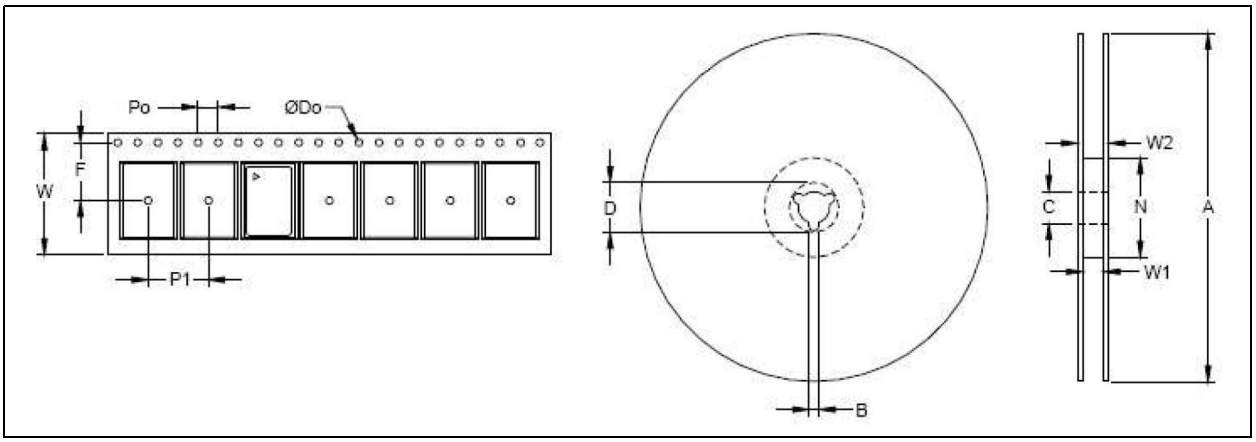
6.0 TAPE AND REEL

TABLE 6-1: TAPE AND REEL DIMENSIONS

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Max**	
VC-830	8	3.5	1.5	4	4	178	2	13	21	60	10	14	3000



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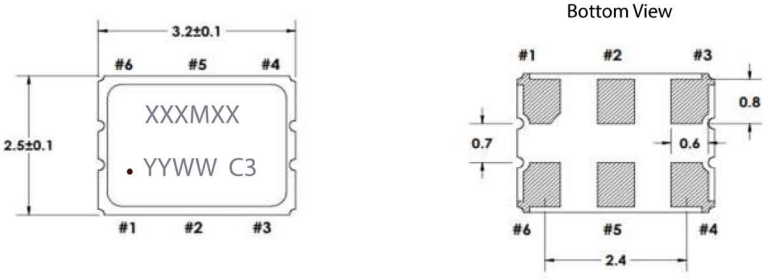
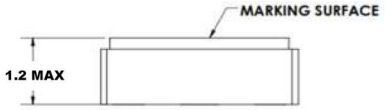
7.0 PACKAGING INFORMATION

6-Lead 3.2 mm x 2.5 mm VDFN Package Outline and Recommended Land Pattern

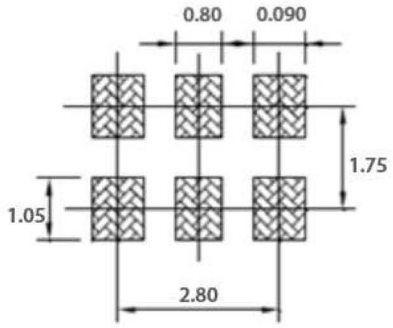
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Marking Information:
XXXMXX = Frequency (example: 100M00)
YY = Year of Manufacture
WW = Week of the Year
C3= Manufacturing Location
● = Pin 1 Indicator

Dimensions in mm



NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (May 2021)

- Converted Vectron document VC-830 to Microchip data sheet template DS20006510A.
- Minor grammatical text changes throughout.

Revision B (August 2021)

- Added a plus/minus (±) symbol to each value listed for Output Amplitude in the Electrical Characteristics, LVDS Option table.
- Updated maximum package height to 1.2 mm.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X	X	X	-X	X	X	X	-XXXXXXXXXX	XX
Part No.	Power Supply	Output	Temp. Range	Stability	E/D Logic	E/D Pin	Custom Options	Frequency	Packaging

Device:	VC-830:		LVPECL, LVDS Crystal Oscillator in 6-Lead 3.2 mm x 2.5 mm VDFN
Power Supply:	E H	= =	3.3VDC ±5% 2.5VDC ±5%
Output:	C D	= =	LVPECL LVDS
Temperature Range:	E F W	= = =	–40°C to +85°C –40°C to +105°C –10°C to +70°C
Stability:	F G K S	= = = =	±25 ppm ±30 ppm ±50 ppm ±100 ppm
Enable/Disable Logic:	A	=	Output Enabled with a Logic High or Open
Enable/Disable Pin:	A	=	Pin 1 (Pin 2 = No Connect)
Custom Options:	N	=	Standard option
Frequency:	xxxMxxxxxx=Frequency in MHz		
Packaging:	TR <blank>=	= 	3,000/Reel Cut Tape/ non-TR quantities

Examples:

a) VC-830-ECF-GAAN-156M250000TR:
VC-830, 3.3VDC, LVPECL Output, –40°C to +105°C Temp Range, ±30 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 156.25 MHz, 3000/Reel

b) VC-830-HDW-KAAN-125M000000TR:
VC-830, 2.5VDC, LVDS Output, –10°C to +70°C Temp Range, ±50 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 125 MHz, 3000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note: Not all combinations of options are available. Other specifications may be available upon request.

NOTES:

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