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## Description

Vectron's VC-827 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off a 1.8 (LVDS) 2.5 or 3.3 volt power supply in a hermetically sealed 3.2x2.5 mm ceramic package.

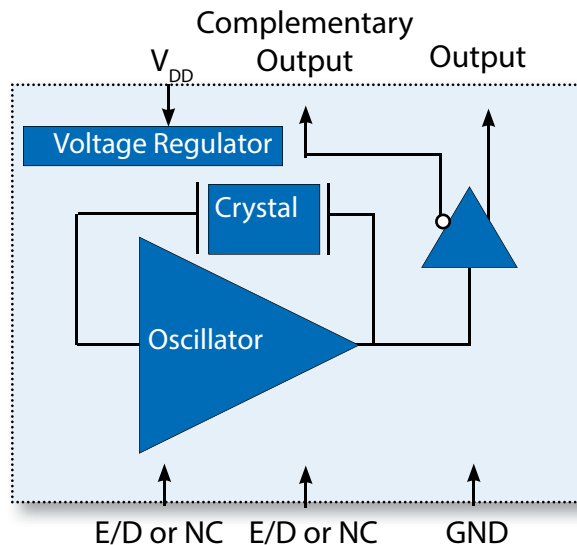
## Features

- Ultra Low Jitter Performance, 3rd OT or Fundamental Crystal Design
- Extended Operating Temperature Range, -40 to 105°C
- 20MHz -220MHz Output Frequencies
- Excellent Power Supply Rejection Ratio
- Enable/Disable
- 1.8 (LVDS), 2.5 or 3.3 V ordering operations
- Hermetically Sealed 3.2x2.5mm Ceramic Package
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

## Applications

- Ethernet, GbE, Synchronous Ethernet
- PCIe
- Fiber Channel
- Enterprise Servers and Storage
- Clock source for ADC's, DAC's
- Test and Measurement
- GPON
- Clock source for ADC's, DAC's, FPGA's

## Block Diagram

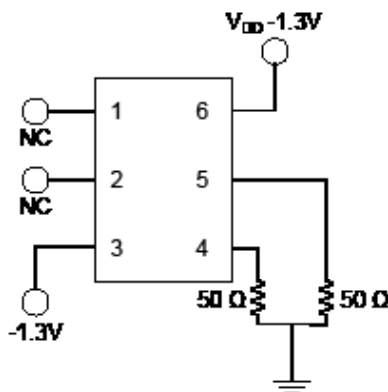


## Performance Specifications

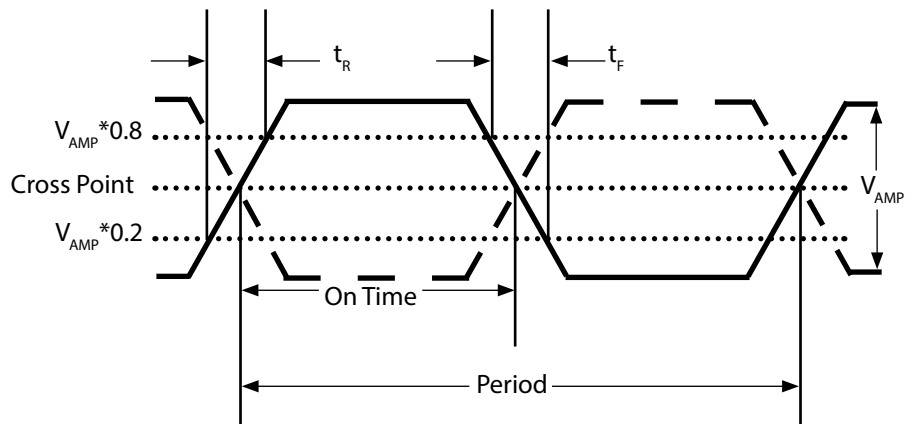
**Table 1. Electrical Performance, LVPECL Option**

Parameter	Symbol	Min	Typical	Maximum	Units
Supply Voltage <sup>1</sup> (Ordering Option)	V <sub>DD</sub>	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current Consumption, 3.3V 2.5V	I <sub>DD</sub>			69 61	mA mA
Frequency					
Nominal Frequency (Ordering Option)	f <sub>N</sub>	20		220	MHz
Stability <sup>2</sup> (Ordering Option)		±25, ±50 or ±100			ppm
Outputs					
Output Logic Levels <sup>3</sup> Output Logic High Output Logic Low	V <sub>OH</sub> V <sub>OL</sub>	V <sub>DD</sub> -1.025 V <sub>DD</sub> -1.810		V <sub>DD</sub> -0.880 V <sub>DD</sub> -1.620	V V
Output Rise and Fall Time <sup>3,4</sup>	t <sub>R</sub> /t <sub>F</sub>			500	ps
Load		50 ohms into V <sub>DD</sub> -2.0V			
Duty Cycle <sup>5</sup>	DC	45		55	%
Phase Noise, 3.3V, 156.25MHz <sup>6</sup> 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 20MHz 40MHz	ϕ <sub>N</sub>		-80 -111 -134 -147 -153 -155 -156 -156		dBc/Hz
Jitter <sup>6</sup> , 156.25MHz 12kHz -20MHz	ϕ <sub>J</sub>		95	130	fs
Enable/Disable					
Outputs Enabled <sup>7</sup> Outputs Disabled	V <sub>IH</sub> V <sub>IL</sub>	0.7*V <sub>DD</sub>		0.3*V <sub>DD</sub>	V V
Disable Time	t <sub>D</sub>			200	ns
Enable/Disable Leakage Current				±200	uA
Start-Up Time	t <sub>SU</sub>			10	ms
Operating Temp. (Ordering Option)	T <sub>OP</sub>	-10/70 or -40/85 or -40/105			°C

1. The VC-827 power supply pin should be filtered, eg, a 10uf, 0.1uf and 0.01uf capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 1 defines the test circuit and Figure 2 defines these parameters.
4. Output rise and fall time will be 600ps (max) for -40/105  $^{\circ}C$  operating temperature range.
5. Duty Cycle is defined as the On/Time Period.
6. Measured using an Agilent E5052 Signal Source Analyzer at 25  $^{\circ}C$ .
7. Outputs will be Enabled if Enable/Disable is left open.



**Figure 1.**



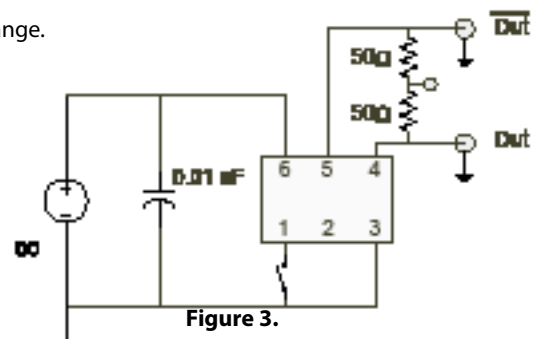
**Figure 2.**

## Performance Specifications

**Table 2. Electrical Performance, LVDS Option**

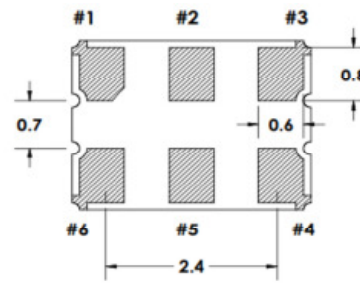
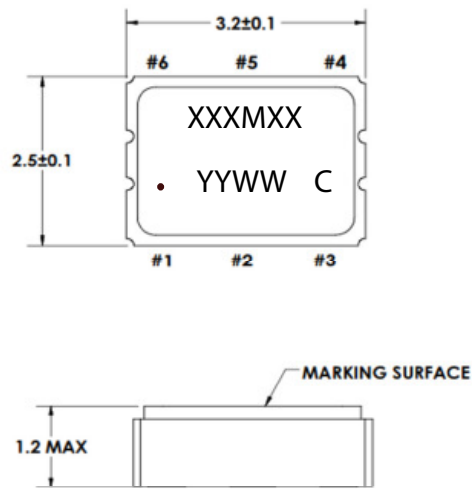
Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Supply Voltage <sup>1</sup> (Ordering Option)	V <sub>DD</sub>	3.135 2.375 1.71	3.3 2.5 1.8	3.465 2.625 1.89	V V V
Current Consumption, 3.3V 2.5V 1.8V	I <sub>DD</sub>			33 29 21	mA mA mA
Frequency					
Nominal Frequency (Ordering Option) 1.8V	f <sub>N</sub>	20 100		220 175	MHz MHz
Stability <sup>2</sup> (Ordering Option)		±25, ±50 or ±100			ppm
Outputs					
Output Logic Levels <sup>3</sup> Output Logic High Output Logic Low	V <sub>OH</sub> V <sub>OL</sub>	0.9	1.43 1.10	1.6	V V
Output Amplitude		247	350	454	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error				50	mV
Output Leakage Current, Outputs Disabled				10	uA
Output Rise and Fall Time <sup>3,4</sup>	t <sub>R</sub> /t <sub>F</sub>			500	ps
Load		100 ohms differential			
Duty Cycle <sup>5</sup>	DC	45		55	%
Phase Noise, 3.3V, 156.25MHz <sup>6</sup> 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 20MHz 40MHz	ϕ <sub>N</sub>		-77 -107 -134 -148 -154 -156 -157 -157		dBc/Hz
Jitter <sup>6</sup> , 156.25MHz 12kHz - 20MHz	ϕ <sub>J</sub>		90	125	fs
Enable/Disable					
Outputs Enabled <sup>7</sup> Outputs Disabled	V <sub>IH</sub> V <sub>IL</sub>	0.7*V <sub>DD</sub>		0.3*V <sub>DD</sub>	V V
Disable Time	t <sub>D</sub>			200	ns
Enable/Disable Leakage Current	I <sub>E/D</sub>			±200	uA
Start-Up Time	t <sub>SU</sub>			10	ms
Operating Temp. (Ordering Option)	T <sub>OP</sub>	-10/70 or -40/85 or -40/105			°C

1. The VC-827 power supply pin should be filtered, eg, a 10 $\mu f$ , 0.1 $\mu f$  and 0.01 $\mu f$  capacitor.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 2 defines these parameters and Figure 3 defines the test circuit.
4. Output rise and fall time will be 600ps (max) for -40/105  $^{\circ}C$  operating temperature range.
5. Duty Cycle is defined as the On/Time Period.
6. Measured using an Agilent E5052 Signal Source Analyzer at 25  $^{\circ}C$ .
7. Outputs will be Enabled if Enable/Disable is left open.



**Figure 3.**

## Package Outline Drawing



Dimensions in mm

### Marking Information:

XXXMXX = Frequency (example: 100M00)

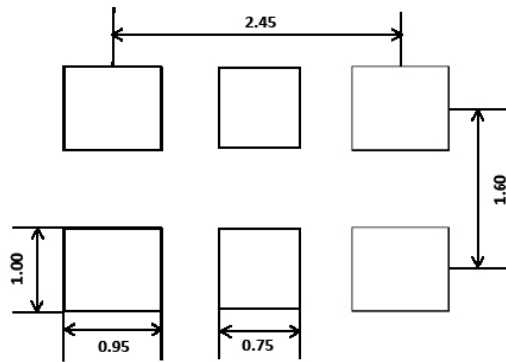
YY = Year of Manufacture

WW = Week of the Year

C = Manufacturing Location

• = Pin 1 Indicator

## Recommended Pad Layout



## Pin Diagram

Table 3. Pinout

Pin #	Symbol	Function
1	E/D or NC	Enable/Disable or No Connection
2	E/D or NC	Enable/Disable or No Connection
3	GND	Electrical and Lid Ground
4	$f_o$	Output Frequency
5	$Cf_o$	Complementary Output Frequency
6	$V_{DD}$	Supply Voltage

Table 4. Enable Disable Function (optional on pin 1 or pin2)

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

## LVPECL Application Diagrams

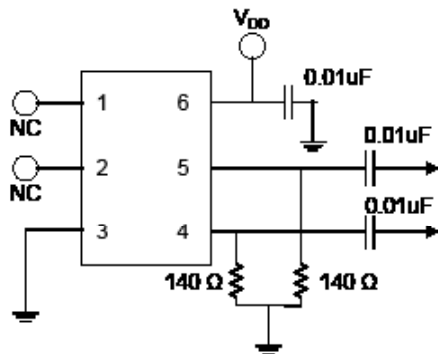


Figure 4. Single Resistor Termination Scheme

Resistor values are typically 140 ohms for 3.3V operation and 84 ohms for 2.5V operation.

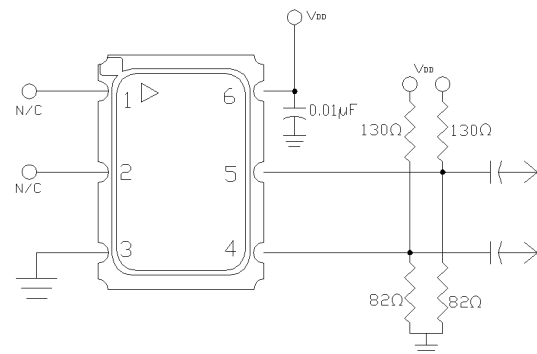


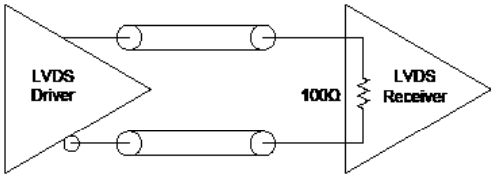
Figure 5. Pull-Up Pull Down Termination

Resistor values shown are typical for 3.3 V operation. For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 250 ohms

The VC-827 incorporates a standard PECL output scheme, which are un-terminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 4, or for best 50 ohm matching a pull-up/pull-down scheme as shown in Figure 5 should be used. AC coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

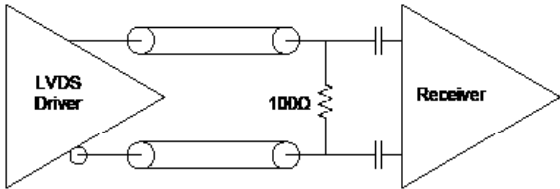
One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## LVDS Application Diagrams



**Figure 6. LVDS to LVDS Connection, Internal 100ohm Resistor**

Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.



**Figure 7. LVDS to LVDS Connection**

Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

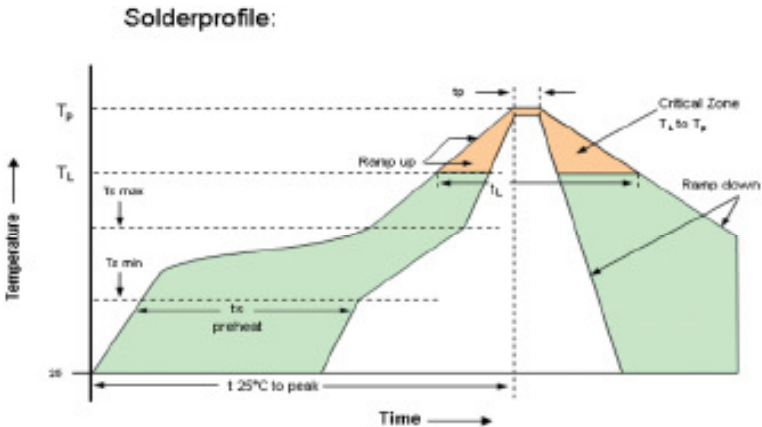
One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## IR Compliance

### Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 4. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 5. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	ts	200 sec Max
Ramp Up	R <sub>UP</sub>	3°C/sec Max
Time above 217°C	tL	150 sec Max
Time to Peak Temperature	tAMB-P	480 sec Max
Time at 260°C	tP	30 sec Max
Time at 240°C	tP2	60 sec Max
Ramp down	R <sub>DN</sub>	6°C/sec Max



## Environmental Compliance

Table 6. Environmental Compliance	
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-202 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (0.3-1.0um) over Nickel
ThetaJC (bottom of case), Maximum Junction Temperature	23 °C/W, 150°C
Weight	28 mg

## Maximum Ratings, Tape & Reel

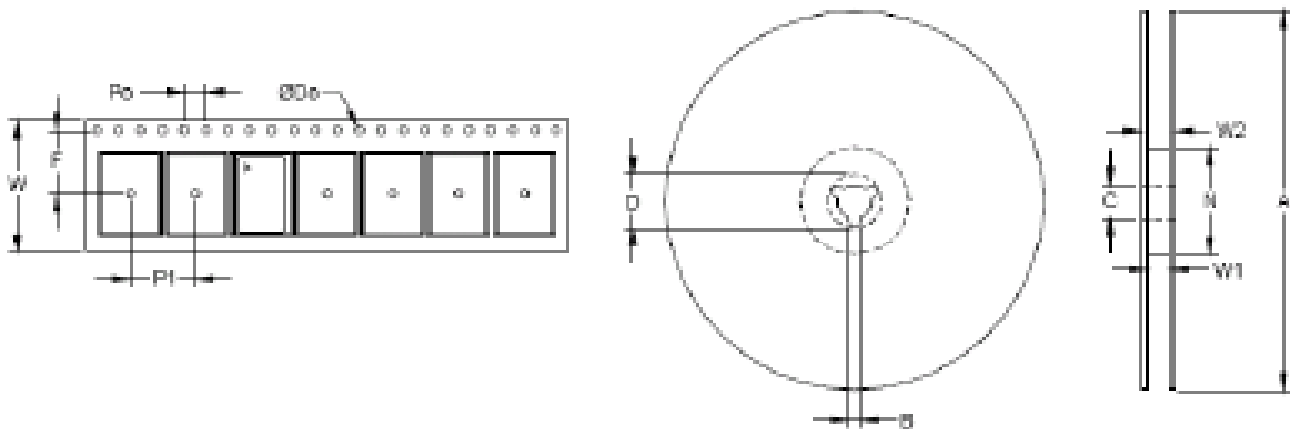
### Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Although ESD protection circuitry has been designed into the VC-827, proper precautions should be taken when handling and mounting, Vectron employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Table 7. Maximum Ratings		
Parameter		Unit
Storage Temperature	-55 to 125	°C
Junction Temperature	150	°C
Supply Voltage	-0.5 to 5.0	V
Enable Disable Voltage	-0.5 to $V_{DD}+0.5$	V
ESD, Human Body Model	1500	V
ESD, Charged Device Model	1500	V

**Table 8. Tape and Reel Information**

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
8	3.5	1.5	4	4	178	2	13	21	60	10	14	3000



## Ordering Information

**VC-827- E C E - K A A N - xxxMxxxxxxXX**

**Product**

XO

**Package**

3.2x2.5mm

**Voltage Options**

E: +3.3 Vdc  $\pm 5\%$

H: +2.5 Vdc  $\pm 5\%$

J: +1.8 Vdc  $\pm 5\%$  (LVDS only)

**Output**

C: LVPECL

D: LVDS

**Temp Range**

W: -10/70°C

E: -40/85°C

F: -40/105°C

**Packaging**

TR: Tape and Reel

blank: Cut Tape / non Tape and Reel quantities

\_SNPB: Tin lead solder dipped

**Frequency** in MHz

**Other (Future Use)**

N: Standard

**Enable/Disable Pin**

A: Pin 1 (Pin 2 = No Connection)

B: Pin 2 (Pin 1 = No Connection)

**Enable/Disable Logic**

A: Output is Enabled with a Logic High or open,  
Output is Disabled with a Logic Low

**Stability**

F:  $\pm 25$ ppm

K:  $\pm 50$ ppm

S:  $\pm 100$ ppm

**Notes:**

a) Only  $\pm 100$ ppm stability option is available for temperature range of -40/105 °C.  $\pm 50$ ppm is available in some cases.

b) Not all combinations of options are available. Other specifications may be available upon request. Consult with factory.

**Example:**

**VC-827-ECE-KAAN-125M000000TR**

**VC-827-ECE-KAAN-125M000000**

**VC-827-ECE-KAAN-125M000000\_SNPB**

**Tape and Reel**

**Cut Tape**

**Tin lead solder dipped**

## Revision History

Revision Date	Approved	Description
Dec 07, 2016	RC	Rev 0.0: VC-827 Preliminary datasheet for factory approval (Internal Revision)
May 31, 2017	VN	Rev 0.1: Internal Revision based on factory information
June 14, 2017	VN	Rev 0.2: Initial Product Release in Website
Sept 06, 2018	FB	Update logo and contact info, add thetaJC, add SNPB DIP ordering option
May 09, 2019	FB	Update logo and contact information, change to SNPB ordering option, increase frequency range to 220MHz
Dec 10, 2019	FB	Add 1.8V LVDS ordering option and maximum junction temperature
April 30, 2020	FB	Add tape and reel ordering option, updates and corrections as needed

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