

Helping Customers Innovate, Improve &amp; Grow


**VC-806**

## Description

Vectron's VC-806 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off either a 2.5 or 3.3 volt supply in a hermetically sealed 5.0x3.2 mm ceramic package.

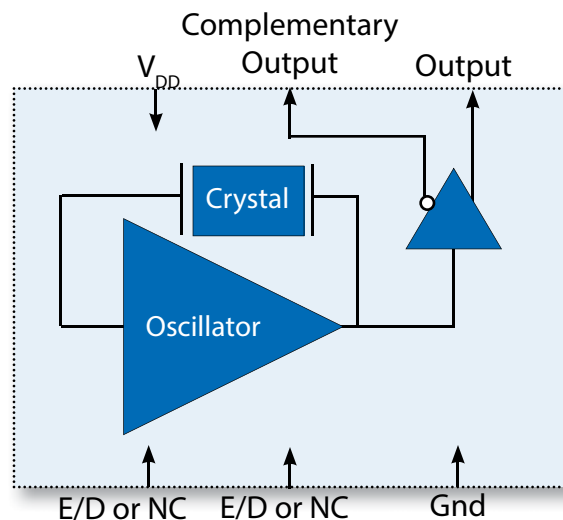
## Features

- Ultra Low Jitter Performance
- Fundamental or 3rd OT Crystal Design
- Output Frequencies to 250.000MHz
- <0.7 ps RMS jitter, 12kHz-20MHz
- Differential Output
- Enable/Disable
- -10/70°C, -40/85°C and -40/105°C Operating Temperature Range
- Hermetically Sealed 5.0x3.2 mm Ceramic Package
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

## Applications

- Storage Area Networking
- Telecom
- Ethernet, GE, SynchE
- Fiber Channel
- PON
- Driving A/D's, D/A's, FPGA's
- Test and Measurement
- Medical
- COTS

## Block Diagram



## Performance Specifications

**Table 1. Electrical Performance, LVPECL Option**

| Parameter                                                                             | Symbol                                         | Min                                              | Typ                          | Max                                              | Units                    |
|---------------------------------------------------------------------------------------|------------------------------------------------|--------------------------------------------------|------------------------------|--------------------------------------------------|--------------------------|
| Supply                                                                                |                                                |                                                  |                              |                                                  |                          |
| Supply Voltage <sup>1</sup> (Ordering Option)                                         | V <sub>DD</sub>                                | 3.135<br>2.375                                   | 3.3<br>2.5                   | 3.465<br>2.625                                   | V                        |
| Current (No Load)                                                                     | I <sub>DD</sub>                                |                                                  |                              | 75                                               | mA                       |
| Frequency                                                                             |                                                |                                                  |                              |                                                  |                          |
| Nominal Frequency <sup>2</sup>                                                        | f <sub>N</sub>                                 | 25                                               |                              | 250                                              | MHz                      |
| Stability <sup>3</sup> (Ordering Option)                                              |                                                | ±25, ±50, ±100                                   |                              |                                                  | ppm                      |
| Outputs                                                                               |                                                |                                                  |                              |                                                  |                          |
| Output Logic Levels <sup>4</sup> , -10/70°C<br>Output Logic High<br>Output Logic Low  | V <sub>OH</sub><br>V <sub>OL</sub>             | V <sub>DD</sub> -1.025<br>V <sub>DD</sub> -1.810 |                              | V <sub>DD</sub> -0.880<br>V <sub>DD</sub> -1.620 | V                        |
| Output Logic Levels <sup>4</sup> , -40/105°C<br>Output Logic High<br>Output Logic Low | V <sub>OH</sub><br>V <sub>OL</sub>             | V <sub>DD</sub> -1.085<br>V <sub>DD</sub> -1.830 |                              | V <sub>DD</sub> -0.880<br>V <sub>DD</sub> -1.555 | V                        |
| Output Rise and Fall Time <sup>4</sup>                                                | t <sub>R</sub> / t <sub>F</sub>                |                                                  |                              | 700                                              | ps                       |
| Load                                                                                  |                                                | 50 ohms into V <sub>DD</sub> -1.3V               |                              |                                                  |                          |
| Duty Cycle <sup>5</sup>                                                               |                                                | 45                                               | 50                           | 55                                               | %                        |
| Phase Jitter <sup>6</sup> , 156.25MHz<br>12kHz - 20MHz offset                         | ϕJ                                             |                                                  | 0.3                          | 0.7                                              | ps                       |
| Period Jitter <sup>7</sup><br>RMS<br>P/P<br>Random Jitter<br>Deterministic Jitter     | ϕJ<br><br><br>R <sub>J</sub><br>D <sub>J</sub> |                                                  | <br>2.6<br>23<br>2.6<br><0.2 |                                                  | <br>ps<br>ps<br>ps<br>ps |
| Enable/Disable                                                                        |                                                |                                                  |                              |                                                  |                          |
| Output Enabled <sup>8</sup><br>Output Disabled                                        | V <sub>IH</sub><br>V <sub>IL</sub>             | 0.7*V <sub>DD</sub>                              |                              | 0.3*V <sub>DD</sub>                              | V<br>V                   |
| Enable/Disable Time                                                                   | t <sub>D</sub>                                 |                                                  |                              | 200                                              | ns                       |
| Enable/Disable Leakage Current                                                        |                                                |                                                  |                              | ±200                                             | uA                       |
| Enable Pull-Up Resistor<br>Output Enabled<br>Output Disabled                          |                                                |                                                  | 33<br>1                      |                                                  | KOhm<br>MOhm             |
| Start-Up Time                                                                         | t <sub>SU</sub>                                |                                                  |                              | 10                                               | ms                       |
| Operating Temperature Range (Ordering Option) <sup>9</sup>                            | T <sub>OP</sub>                                | -10/70 or -40/85 or -40/105                      |                              |                                                  | °C                       |
| Package Size                                                                          |                                                | 5.0 x 3.2 x 1.3                                  |                              |                                                  | mm                       |

1. The VC-806 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. See Standard Frequencies and Ordering Information for more information.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Figure 1 shows the test circuit and Figure 2 defines these parameters.
5. Duty Cycle is defines as the On/Time Period.
6. Measured using an Agilent E5052 Signal Source Analyzer at 25 °C. Phase Jitter will be 1.0ps (max) for carrier frequencies between 25MHz and 100MHz. Above 100MHz carrier frequency, phase jitter will be 0.7ps (max).
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.
9. Only  $\pm 50$ ppm and  $\pm 100$ ppm stability options are available for -40 °C to 105 °C operating temperature range.

## Performance Specifications

**Table 2. Electrical Performance, LVDS Option**

| Parameter                                                                 | Symbol                             | Min                         | Typ          | Max                 | Units        |
|---------------------------------------------------------------------------|------------------------------------|-----------------------------|--------------|---------------------|--------------|
| Supply                                                                    |                                    |                             |              |                     |              |
| Supply Voltage <sup>1</sup> (Ordering Option)                             | V <sub>DD</sub>                    | 3.135<br>2.375              | 3.3<br>2.5   | 3.465<br>2.625      | V            |
| Current (No Load)                                                         | I <sub>DD</sub>                    |                             |              | 60                  | mA           |
| Frequency                                                                 |                                    |                             |              |                     |              |
| Nominal Frequency <sup>2</sup>                                            | f <sub>N</sub>                     | 25                          |              | 250                 | MHz          |
| Stability <sup>3</sup> (Ordering Option)                                  |                                    | ±25, ±50, ±100              |              |                     | ppm          |
| Outputs                                                                   |                                    |                             |              |                     |              |
| Output Logic Levels <sup>4</sup><br>Output Logic High<br>Output Logic Low | V <sub>OH</sub><br>V <sub>OL</sub> | 0.9                         | 1.43<br>1.10 | 1.6                 | V            |
| Output Swing                                                              |                                    | 247                         | 330          | 454                 | mV           |
| Differential Output Error                                                 |                                    |                             |              | 50                  | mV           |
| Offset Voltage                                                            |                                    | 1.125                       | 1.25         | 1.375               | V            |
| Offset Voltage Error                                                      |                                    |                             |              | 50                  | mV           |
| Output Leakage Current                                                    |                                    |                             |              | 10                  | uA           |
| Output Rise and Fall Time <sup>4</sup>                                    | t <sub>R</sub> / t <sub>F</sub>    |                             |              | 700                 | ps           |
| Load                                                                      |                                    | 100 ohms differential       |              |                     |              |
| Duty Cycle <sup>5</sup>                                                   |                                    | 45                          | 50           | 55                  | %            |
| Phase Jitter <sup>6</sup> , 156.25MHz<br>12kHz - 20MHz offset             | ϕJ                                 |                             | 0.35         | 0.8                 | ps           |
| Period Jitter <sup>7</sup><br>RMS<br>P/P                                  | ϕJ                                 |                             | 2.9<br>25.1  |                     | ps<br>ps     |
| Random Jitter                                                             | R <sub>J</sub>                     |                             | 2.9          |                     | ps           |
| Deterministic Jitter                                                      | D <sub>J</sub>                     |                             | <0.2         |                     | ps           |
| Enable/Disable                                                            |                                    |                             |              |                     |              |
| Output Enabled <sup>8</sup><br>Output Disabled                            | V <sub>IH</sub><br>V <sub>IL</sub> | 0.7*V <sub>DD</sub>         |              | 0.3*V <sub>DD</sub> | V<br>V       |
| Enable/Disable Time                                                       | t <sub>D</sub>                     |                             |              | 200                 | ns           |
| Enable/Disable Leakage Current                                            |                                    |                             |              | ±200                | uA           |
| Enable Pull-Up Resistor<br>Output Enabled<br>Output Disabled              |                                    |                             | 33<br>1      |                     | KOhm<br>MOhm |
| Start-Up Time                                                             | t <sub>SU</sub>                    |                             |              | 10                  | ms           |
| Operating Temperature Range (Ordering Option) <sup>9</sup>                | T <sub>OP</sub>                    | -10/70 or -40/85 or -40/105 |              |                     | °C           |
| Package Size                                                              |                                    | 5.0 x 3.2 x 1.3             |              |                     | mm           |

1. The VC-806 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.

2. See Standard Frequencies and Ordering Information for more information.

3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.

4. Figure 3 shows the test circuit and Figure 2 defines these parameters.

5. Duty Cycle is defines as the On/Time Period.

6. Measured using an Agilent E5052 Signal Source Analyzer at 25 °C. Phase Jitter will be 1.0ps (max) for carrier frequencies between 25MHz and 100MHz. Above 100MHz carrier frequency, phase jitter will be 0.8ps (max).

7. Measured using a Wavcrest SIA3300C, 90K samples.

8. Outputs will be Enabled if Enable/Disable is left open.

9. Only  $\pm 50$ ppm and  $\pm 100$ ppm stability options are available for -40 °C to 105 °C operating temperature range.

## Test Diagrams

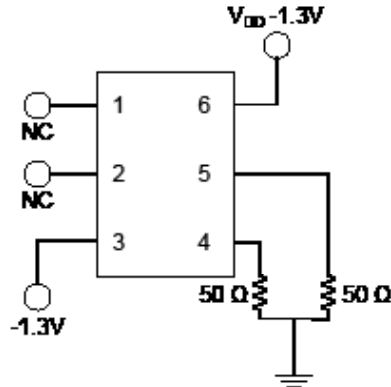


Figure 1 - LV-PECL test circuit

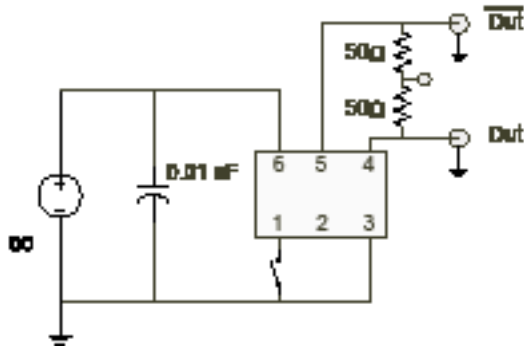


Figure 3 - LVDS test circuit

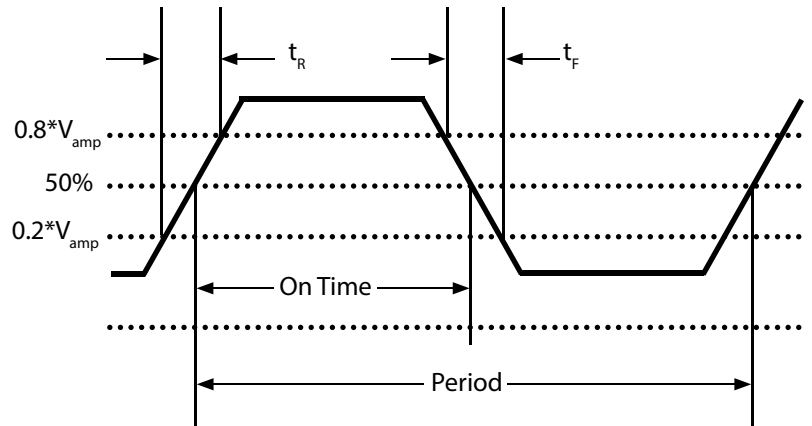


Figure 2 - Waveform

## Package and Pinout

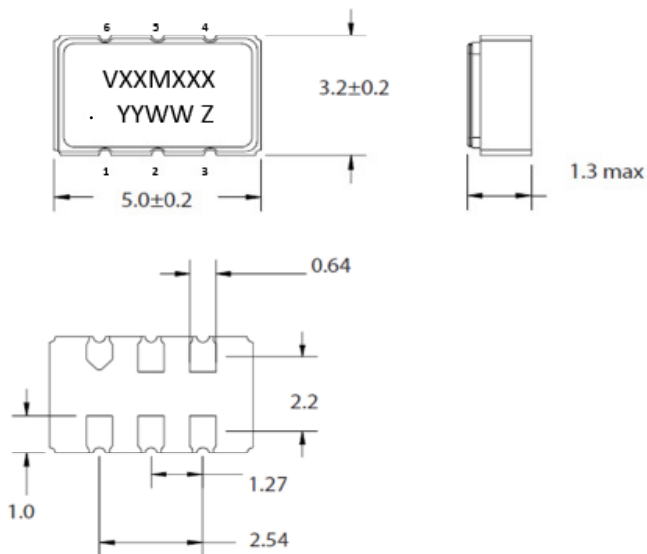


Figure 4 - Package (Dimensions in mm)

### Marking Information:

V: Vectron

XXMXXX: Frequency in MHz (Example: 25M000 or 125M00)

YYWW: Year and Week (1642: Year 2016 and Week 42)

Z: Manufacturing Location

Table 3. Pinout

| Pin # | Symbol    | Function                        |
|-------|-----------|---------------------------------|
| 1     | E/D or NC | Enable Disable or No Connection |
| 2     | E/D or NC | Enable Disable or No Connection |
| 3     | GND       | Electrical and Lid Ground       |
| 4     | $f_o$     | Output Frequency                |
| 5     | $Cf_o$    | Complementary Output Frequency  |
| 6     | $V_{DD}$  | Supply Voltage                  |

The Enable/Disable function is set at the factory on either pin 1 or pin 2 and is an ordering option.

Table 4. Enable Disable Function

| E/D Pin | Output         |
|---------|----------------|
| High    | Clock Output   |
| Open    | Clock Output   |
| Low     | High Impedance |

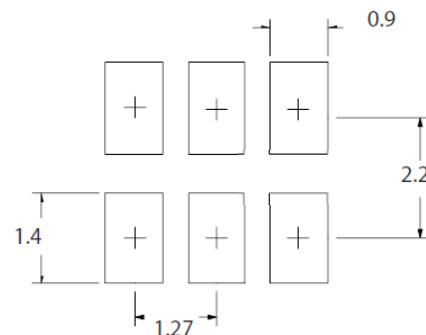
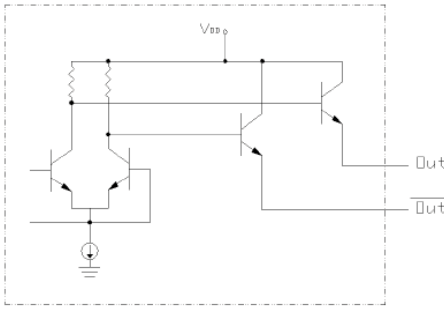
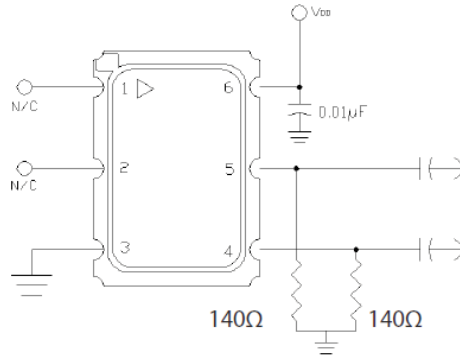


Figure 5 - Pad Layout (Dimensions in mm)

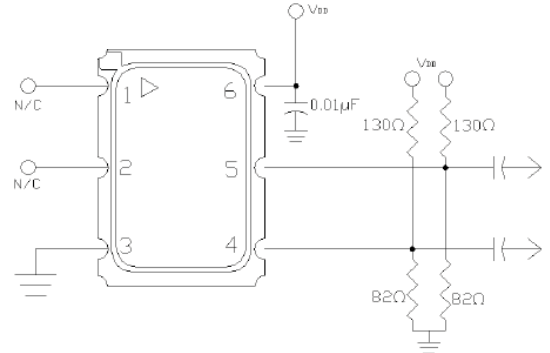
## LVPECL Application Diagrams



**Figure 6 - Standard PECL Output Configuration**



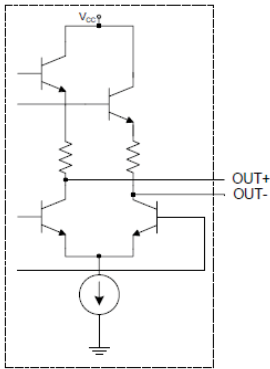
**Figure 7 - Single Resistor Termination Scheme**  
Resistor values are typically 140 ohms for 3.3V operation. Resistor values are typically 84 for 2.5V operation.



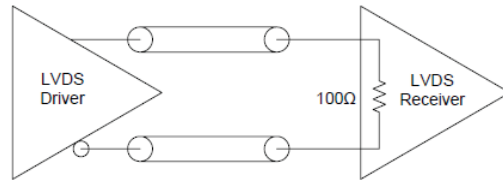
**Figure 8 - Pull-Up Pull Down Termination**  
Resistor values are typically for 3.3V operation. For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 240 ohms

The VC-806 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 6. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 7, and a pull-up/pull-down scheme as shown in Figure 8. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

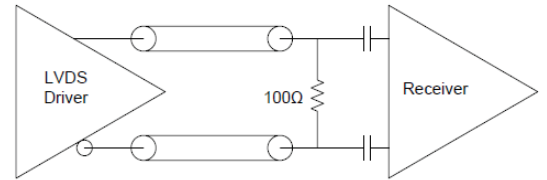
## LVDS Application Diagrams



**Figure 9 - Standard LVDS Output Configuration**



**Figure 10 - LVDS to LVDS Connection, Internal 100ohm**  
Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.



**Figure 11 - LVDS to LVDS Connection External 100ohm and AC blocking caps**  
Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## Environmental and IR Compliance

| Table 5. Environmental Compliance |                                                                                                  |
|-----------------------------------|--------------------------------------------------------------------------------------------------|
| Parameter                         | Condition                                                                                        |
| Mechanical Shock                  | MIL-STD-883 Method 2002                                                                          |
| Mechanical Vibration              | MIL-STD-883 Method 2007                                                                          |
| Temperature Cycle                 | MIL-STD-883 Method 1010                                                                          |
| Solderability                     | MIL-STD-883 Method 2003                                                                          |
| Fine and Gross Leak               | MIL-STD-883 Method 1014                                                                          |
| Resistance to Solvents            | MIL-STD-883 Method 2015                                                                          |
| Moisture Sensitivity Level        | MSL1                                                                                             |
| Contact Pads                      | Gold over Nickel<br>Thickness of Gold: ~0.3µm to 1.0µm<br>Thickness of Nickel: ~1.27µm to 8.89µm |
| Weight                            | 57 mg                                                                                            |

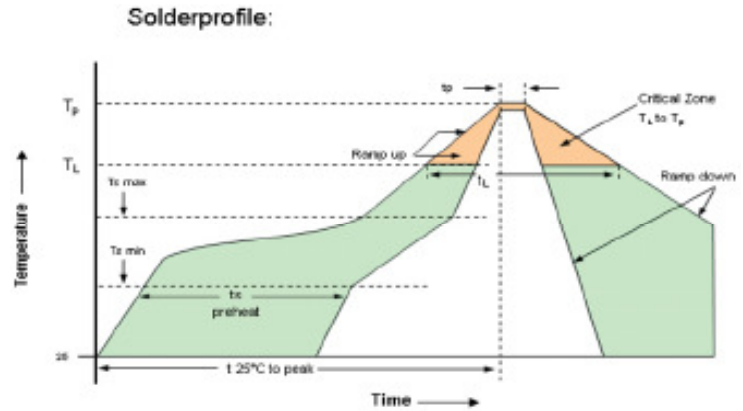
# IR Compliance

## Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 6. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

**Table 6. Reflow Profile**

| Parameter                | Symbol      | Value       |
|--------------------------|-------------|-------------|
| PreHeat Time             | $t_s$       | 200 sec Max |
| Ramp Up                  | $R_{UP}$    | 3°C/sec Max |
| Time above 217°C         | $t_L$       | 150 sec Max |
| Time to Peak Temperature | $t_{AMB-P}$ | 480 sec Max |
| Time at 260°C            | $t_p$       | 30 sec Max  |
| Time at 240°C            | $t_{P2}$    | 60 sec Max  |
| Ramp down                | $R_{DN}$    | 6°C/sec Max |



## Maximum Ratings, Tape & Reel

### Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

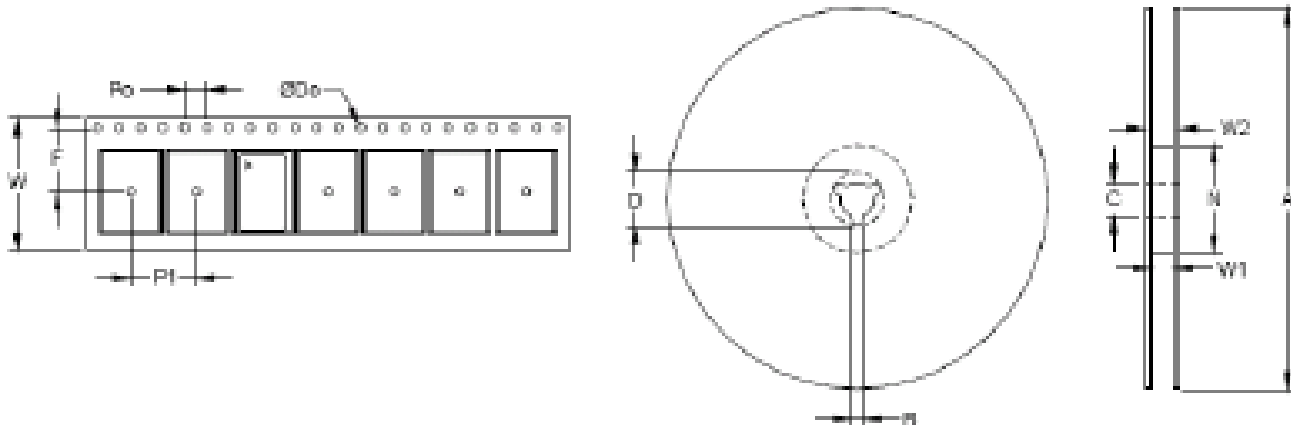
Although ESD protection circuitry has been designed into the VC-806, proper precautions should be taken when handling and mounting, Vectron employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

**Table 7 Maximum Ratings**

| Parameter                 | Symbol      | Rating               | Unit |
|---------------------------|-------------|----------------------|------|
| Storage Temperature       | $T_{STORE}$ | -55/125              | °C   |
| Supply Voltage            | $V_{DD}$    | -0.5 to 5.0          | V    |
| Enable Disable Voltage    | E/D         | -0.5 to $V_{DD}+0.5$ | V    |
| ESD, Human Body Model     | HBM         | 1500                 | V    |
| ESD, Charged Device Model | CDM         | 1000                 | V    |

**Table 8. Tape and Reel Information**

| Tape Dimensions (mm) |     |     |    |    | Reel Dimensions (mm) |   |    |    |    |    |      |        |
|----------------------|-----|-----|----|----|----------------------|---|----|----|----|----|------|--------|
| W                    | F   | Do  | Po | P1 | A                    | B | C  | D  | N  | W1 | W2   | #/Reel |
| 12                   | 5.5 | 1.5 | 4  | 8  | 180                  | 2 | 13 | 21 | 60 | 13 | 15.4 | 250    |



**Table 9. Standard Frequencies (MHz)**

|         |          |            |         |         |         |          |          |         |         |         |          |
|---------|----------|------------|---------|---------|---------|----------|----------|---------|---------|---------|----------|
| 25.000  | 25.00125 | 27.000     | 32.000  | 33.000  | 38.880  | 40.000   | 50.000   | 53.125  | 56.000  | 56.250  | 60.000   |
| 61.440  | 62.500   | 66.000     | 66.667  | 67.500  | 75.000  | 77.760   | 80.000   | 83.333  | 98.304  | 100.000 | 103.000  |
| 106.250 | 108.000  | 114.285    | 122.280 | 124.512 | 125.000 | 133.000  | 143.000  | 148.351 | 148.500 | 150.000 | 153.600  |
| 155.520 | 156.250  | 156.253906 | 160.000 | 161.130 | 164.355 | 166.6286 | 166.6667 | 167.000 | 167.330 | 168.750 | 173.3707 |
| 180.000 | 186.667  | 187.500    | 190.000 | 200.000 | 212.500 | 218.750  | 250.000  |         |         |         |          |

## Ordering Information

### VC-806- E C E - K A A N - xxxMxxxxxxXX

**Product**

XO

**Package**

5.0x3.2 mm Ceramic

**Voltage Options**E: +3.3 Vdc  $\pm 5\%$ H: +2.5 Vdc  $\pm 5\%$ **Output**

C: LVPECL

D: LVDS

**Temp Range**

W: -10/70°C

E: -40/85°C

F: -40/105°C

**Packaging**

TR: Tape and Reel

blank: Cut Tape / non Tape and Reel quantities

\_SNPB: Tin lead solder dipped

**Frequency in MHz****Other (Future Use)**

N: Standard

**Enable/Disable Pin**

A: Pin 1

B: Pin 2

**Enable/Disable Logic**

A: Enable High

**Stability**F:  $\pm 25$ ppmK:  $\pm 50$ ppmS:  $\pm 100$ ppm**Notes:**

- Only  $\pm 50$ ppm and  $\pm 100$ ppm stability options are available over -40/105°C operating temperature range.
- Stability option of  $\pm 20$ ppm is available. But it does not include aging and reflow.
- Not all combinations of ordering options are available. Other specifications may be available upon request. Please consult with Vectron Applications Team.
- Ordering information for frequency is xxxMxxxxxx or xxMxxxxxx depending on the oscillator frequency

**Example:****VC-806-EDE-KAAN-125M000000TR****Tape and Reel****VC-806-EDE-KAAN-125M000000****Cut Tape****VC-806-EDE-KAAN-125M000000\_SNPB****Tin lead solder dipped**

## Revision History

| Revision Date  | Approved | Description                                                                                                                                                                |
|----------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2009 - 2011    | FB, TG   | Initial Datasheet, Minor modifications                                                                                                                                     |
| Oct 21, 2013   | TG       | Updated Vectron Asia contact information                                                                                                                                   |
| Feb 07, 2014   | TG       | Vectron Knowles Logo                                                                                                                                                       |
| May 13, 2015   | VN       | Modified Marking Information in Package Drawing                                                                                                                            |
| Mar 18, 2016   | VN       | Updated Standard Frequencies Table (Table 8) - Added 3 new frequencies                                                                                                     |
| Aug 24, 2016   | VN       | Changed Maximum Frequency to 250MHz. Removed 312.5MHz from Frequency Table 8.                                                                                              |
| Jan 17, 2017   | RC       | Changed reflow profile to indicate 30s (max.) for time at 260 °C. However, Incorrect version of VC-806 design file used to create datasheet which was loaded in website.   |
| Sep 22, 2017   | VN       | Added extended temperature option, termination finish information, added notes for phase jitter and stability, added notes under ordering options, updated T&R dimensions. |
| May 10, 2019   | FB       | Update logo and contact information, add _SNPB ordering details                                                                                                            |
| April 30, 2020 | FB       | Add tape and reel ordering option                                                                                                                                          |

## Contact Information

### **USA:**

100 Watts Street  
Mt Holly Springs, PA 17065  
Tel: 1.717.486.3411  
Fax: 1.717.486.5920

### **Europe:**

Landstrasse  
74924 Neckarbischofsheim  
Germany  
Tel: +49 (0) 7268.801.0  
Fax: +49 (0) 7268.801.281



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