UPD301A

Stand-alone USB Type-C™ Power Delivery 3.0 Controller

Highlights

- Single-chip USB Type-C™ (1) Power Delivery Solution for Stand-alone Source-only
- Preprogrammed Power Delivery Firmware
- Supports Standard Power Delivery Power Profiles (15/27/45/60W)
- USB Power Delivery 3.0 Compliant MAC
- USB Type-C™ Connector Support with Connection Detection and Control
- Integrated Analog Discrete Components Reduce Bill of Materials and Design Footprint
- Easily Supports 2nd Port via UPD350 Add-on
- Commercial, Industrial, and Automotive Temperature Support

Target Applications

- Point-of-Sale Terminals
- Charging Lockers
- IoT Products and Sensors
- Smart Speakers and Monitors
- Conference Systems
- Power Tools
- Multi-port Charging Docks
- Automotive Rear Seat Charging Ports

Key Benefits

- Preprogrammed Power Delivery Firmware
  - Supports Standard Power Delivery Power Profiles (15/27/45/60W)
  - No Custom Firmware Development Required
- Multiple Stand-alone Configurations via Pin Straps
  - Power Delivery Power Profile Selection
- Optional Two Port Solution via External UPD350
  - SPI for External UPD350 Communication
  - Power Delivery Firmware Controls Both Ports
- Integrated Analog Discrete Components
  - VCONN FETs with Rp/Rd Switching
  - Programmable Current Sense for Overcurrent Conditions
  - Voltage Sense for Overvoltage Conditions
- USB Power Delivery MAC
  - Compliant with USB Power Delivery Specification Revision 3.0
  - Power Delivery Packet Framing
  - CRC Checking/Generation
  - 4B/5B Encoding/Decoding
  - BMC Encoding/Decoding
  - EOP/SOP Generation for PD Frames
  - SOP Detection and SOP Header Processing
  - Separate RX/TX FIFOs
  - Automatic GoodCRC Message Generation
  - Automatic Retry Generation
  - Error Handling
  - Low Standby Power Support
- USB Type-C Cable Detect Logic
  - Auto Cable Attach & Orientation Detection
  - Routes Baseband Communication to Respective CC Pin per Detected Orientation
  - VCONN Supply Control for Active Cable
  - Strappable Downstream Facing Port (DFP) Modes
  - Charging Current Capability Detection
- Package
  - 40-VQFN (6.0mm x 6.0mm)
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial / AEC-Q100 Automotive Grade 3 Temperature Range (-40°C to +85°C)

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1.0 PREFACE

1.1 Glossary of Terms

TABLE 1-1: GLOSSARY OF TERMS

Term	Definition
ADC	Analog to Digital Converter
AFE	Analog Front End
BCI	Baseband CC Interface
Billboard	USB Billboard Device. A required USB device class for UFPs which support Alternate Modes in order to provide product information to the USB Host.
BIST	Built-In Self Test
BMC	Bi-phase Mark Coding
Byte	8-bits
CC	Generic reference to USB Type-C™ Cable / Connector CC1/CC2 pins
CSR	Control and Status Register
DFP	Downstream Facing Port (USB Type-C™ Specification definition)
DP	DisplayPort (a VESA standard interface)
DPM	Device Policy Manager (PD Specification definition)
DWORD	32-bits
EC	Embedded Controller
EP	USB Endpoint
ESD	Electro-Static Discharge
FIFO	First In First Out buffer
FW	Firmware
FS	Full-Speed
GPIO	General Purpose Input/Output
Host	External system (Includes processor, application software, etc.)
HBM	Human Body Model (Simulates ESD from humans)
HPD	Hot-Plug Detect functionality as defined by DisplayPort and DisplayPort Alternate Mode specifications
HS	High-Speed
HW	Hardware (Refers to function implemented by the device)
IC	Integrated Circuit
IFC	InterFrame Gap
LDO	Linear Drop-Out regulator
MAC	Media Access Controller
Microchip	Microchip Technology Incorporated
N/A	Not Applicable
NC	No Connect (pin)
OCS	Over-Current Sense
PCS	Physical Coding Sublayer
PD / UPD	USB Power Delivery
PDO	Power Delivery Object (USB PD Specification definition) PDOs enable the port to indicate its Port Partner supported combinations of Voltage/Current or Power as well as the type of supply (Fixed, Variable, Battery) in Source Role or Sink Role.
PDP	Power Delivery Power (USB PD Specification definition) A wattage value which corresponds to a set of voltages with corresponding current values.

TABLE 1-1: GLOSSARY OF TERMS (CONTINUED)

Term	Definition
PIO	General Purpose I/O
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
Port Partner	Remote port which is connected to the UPD301A's local port
PRBS	Pseudo Random Binary Sequence
QWORD	64-bits
SA	Source Address
SBU	SideBand Use
SCSR	System Control and Status Register
Source Role	USB Type-C port is sinking power from its Port Partner
Source-only Operation	Operation exclusively in USB Type-C / Power Delivery Source Role as defined in the USB Type-C and Power-Delivery specifications. In this mode of operation, USB Type-C Dual-Role Power Operation is not supported and there is no support for USB Power Role Swap.
SPI	Serial Peripheral Interface
SPM	System Policy Manager (USB PD Specification definition)
SS	SuperSpeed
Stand-alone Mode	Chip operation without the control or configuration by an external MCU. Policy is defined locally by the UPD301A firmware. Configuration is achieved by use of configuration straps.
SVDM	Standard/Vendor Defined Message (USB PD Specification definition)
SVID	Standard/Vendor IDentity (USB PD Specification definition)
TCPC	USB Type-C™ Port Controller
UFP	Upstream Facing Port (USB Type-C™ Specification definition)
USB	Universal Serial Bus
USB Power Delivery Operation	Port is operating using USB Power Delivery protocols in conformance to the USB PD Specification.
USB Power Role Swap	Message sequence as defined in the USB PD Specification, enabling a transition between Source Role and Sink Role during USB Power Delivery Operation
USB Type-C™	USB Type-C™ Cable / Connector
VDO	Vendor-Defined Object (USB PD Specification definition)
VSM	Vendor Specific Messaging
WORD	16-bits
ZLP	Zero Length USB Packet

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
I	Input
IS	Schmitt-triggered input
O2	Output with 2 mA sink and 2 mA source
OD2	Open-drain output with 2 mA sink and 2 mA source
O8	Output with 8 mA sink and 8 mA source
PD	200kΩ (typical) internal pull-down. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AO	Analog output
AIO	Analog bidirectional
P	Power pin

Note: Refer to Section 5.5, "DC Characteristics," on page 28 for the electrical characteristics of the various buffers.

1.3 References

- USB Power Delivery: https://www.usb.org/document-library/usb-power-delivery.
- USB Type-C™ Specification: ihttps://www.usb.org/document-library/usb-type-cr-cable-and-connector-specification-revision-14-march-29-2019

2.0 INTRODUCTION

2.1 General Description

The UPD301A is a stand-alone, small form factor USB Type-C™ Power Delivery (PD) Port Controller designed to adhere to the *USB Type-C™ Cable and Connector Specification* and *USB Power Delivery 3.0 Specification*. The UPD301A provides stand-alone operation for source PD applications, enabling cable plug orientation and detection for a USB Type-C receptacle, and implementing baseband communication with a partner USB Type-C device via the integrated USB Power Delivery 3.0 MAC.

The embedded 32-bit ARM Cortex-M0+ implements a full Power Delivery firmware stack, providing a turn-key solution for USB-C™ power-only applications, and requiring minimal customer development. Configuration is supported via pin straps to select source functionality and PD power profiles. Optionally, a second PD port is supported via SPI connection of an external Microchip UPD350.

Additionally, the UPD301A integrates many of the analog discrete components required for USB Type-C PD applications, including two VCONN FETs with Rp/Rd switching and current/voltage sense circuitry for over-voltage/current detection. By integrating the PD firmware and many of the analog discrete components required for USB Type-C PD applications, the UPD301A provides a low cost, stand-alone, fast time-to-market solution for consumer, industrial, and automotive applications.

The UPD301A is available in commercial (0°C to +70°C) and industrial/automotive grade 3 (-40°C to +85°C) temperature ranges. For ordering information, refer to the Product Identification System on page 38.

2.2 Example Applications

The UPD301A has been designed for multiple applications, including:

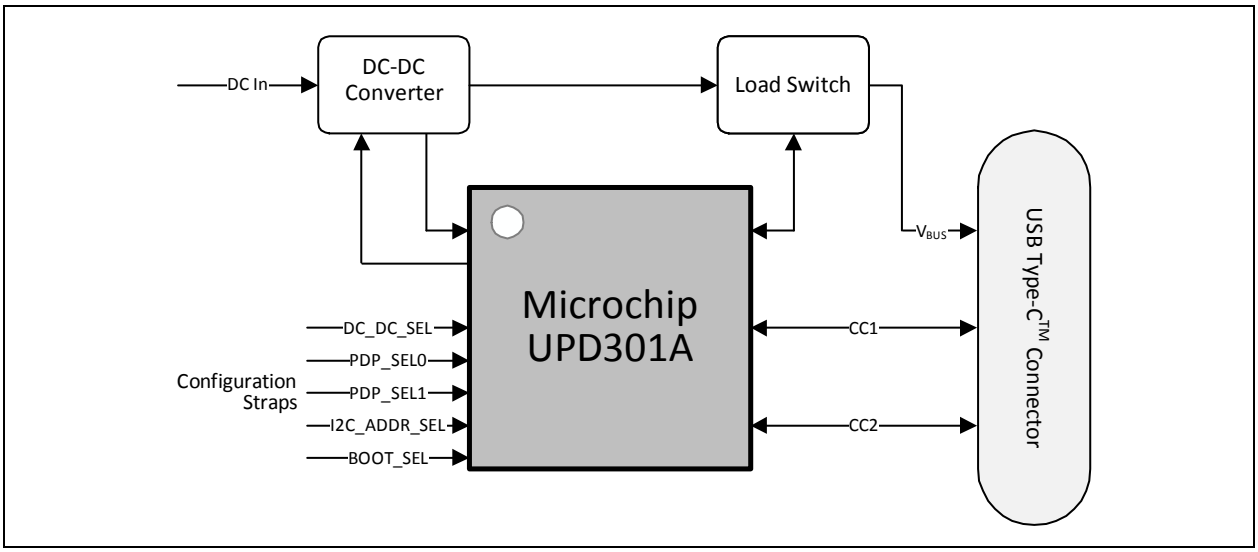
- Source-Only Applications (E.G., Charging Ports)
- Two-Port Applications (E.G., Automotive Rear Seat Charging)

Note:	Single-Port Source and Dual-Port Source modes are the only supported modes of operation.

2.2.1 SOURCE-ONLY APPLICATIONS (E.G., CHARGING PORTS)

The simplest UPD301A application is a power source (Source-Only), as shown in Figure 2-1. Using the device configuration straps, various PD parameters/options can be configured. The integrated DAC configures the DC-DC converter, selecting the output voltage, and controls the load switch to regulate and protect the output voltage. The load switch can also be replaced by discrete FETs and over-current / over-voltage protection circuits.

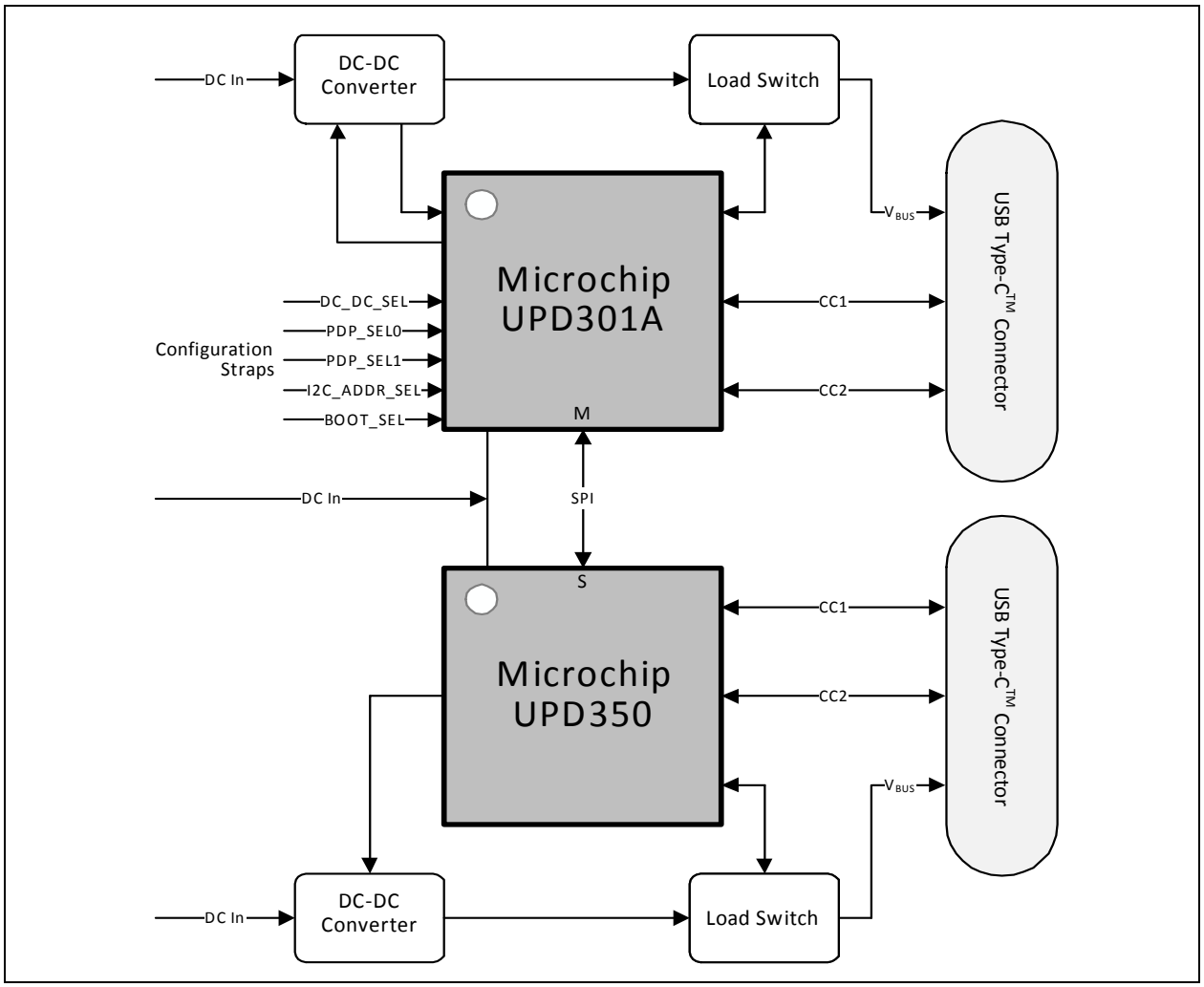
FIGURE 2-1: SYSTEM BLOCK DIAGRAM - SOURCE-ONLY APPLICATION



2.2.2 TWO-PORT APPLICATIONS (E.G., AUTOMOTIVE REAR SEAT CHARGING)

Some applications, such as a automotive rear seat charging port, may need up to two USB Type-C™ power delivery ports. These ports can be implemented by connecting a UPD301A and a UPD350 via the SPI interface, as shown in Figure 2-2. The UPD301A will execute the stack for the UPD350. The two-port implementation supports dynamic power allocation (e.g., go-to power min based on an external input). The integrated DAC from the UPD301A and additional GPIOs from the UPD350 control the DC-DC converter, selecting the voltages, and control the load switch to regulate and protect the output voltage. The load switch can also be replaced by discrete FETs and over-current / over-voltage protection circuits.

FIGURE 2-2: SYSTEM BLOCK DIAGRAM - TWO-PORT APPLICATION

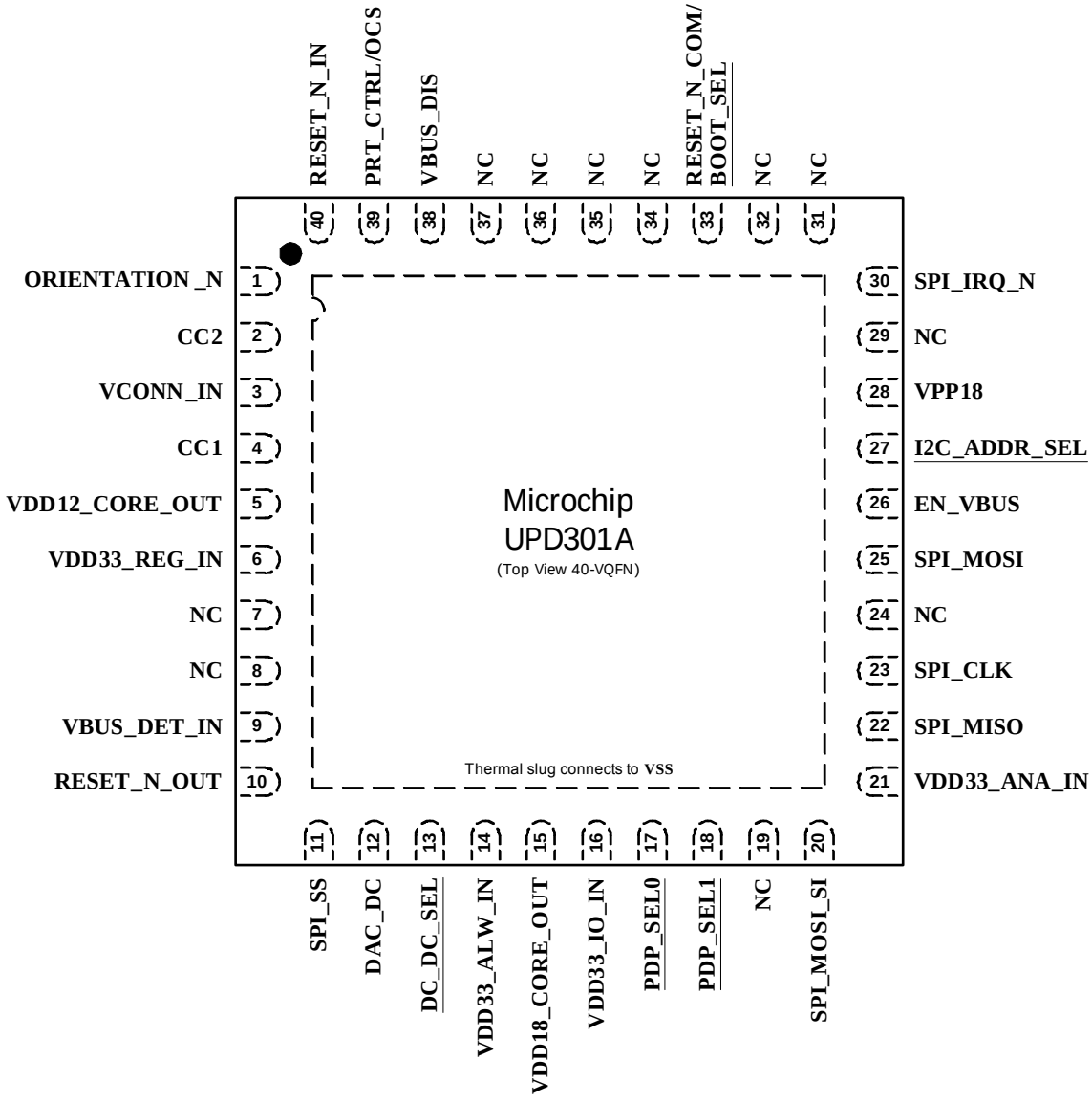


3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

The device pin diagram for the UPD301A can be seen in Figure 3-1. Table 3-1 provides a UPD301A pin assignment table. Pin descriptions are provided in Section 3.2, "Pin Descriptions".

FIGURE 3-1: UPD301A PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (VSS) on bottom of package must be connected to ground .

TABLE 3-1: UPD301A PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name
1	ORIENTATION_N	21	VDD33_ANA_IN
2	CC2	22	SPI_MISO
3	VCONN_IN	23	SPI_CLK
4	CC1	24	NC
5	VDD12_CORE_OUT	25	SPI_MOSI
6	VDD33_REG_IN	26	EN_VBUS
7	NC	27	I2C_ADDR_SEL
8	NC	28	VPP18
9	VBUS_DET_IN	29	NC
10	RESET_N_OUT	30	SPI_IRQ_N
11	SPI_SS	31	NC
12	DAC_DC	32	NC
13	DC_DC_SEL	33	RESET_N_CO M/BOOT_SEL
14	VDD33_ALW_IN	34	NC
15	VDD18_CORE_OUT	35	NC
16	VDD33_IO_IN	36	NC
17	PDP_SEL0	37	NC
18	PDP_SEL1	38	VBUS_DIS
19	NC	39	PRT_CTRL/OCS
20	SPI_MOSI_SI	40	RESET_N_IN
Exposed Pad (VSS) must be connected to ground.			

3.2 Pin Descriptions

This sections details the functions of the various device signals.

TABLE 3-2: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB Type-C™			
Configuration Channel 1	**CC1**	AIO	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Configuration Channel 2	**CC2**	AIO	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
VBUS Detection	**VBUS_DET_IN**	AIO	Scaled down version of VBUS input used for VBUS detection. Tie this signal to VBUS via a resistor divider.
SPI Interface			
SPI Clock	**SPI_CLK**	IS	SPI clock. The maximum supported SPI clock frequency is 8 MHz.
SPI Data Master In / Slave Out	**SPI_MISO**	I/O8	SPI data master in, slave out.
SPI Data Master Out / Slave In	**SPI_MOSI**	O2	SPI data master out / slave in. This pin must be connected to **SPI_MOSI_SI** for proper operation.
SPI Data Slave In	**SPI_MOSI_SI**	IS	SPI data slave in. This pin must be connected to **SPI_MOSI** for proper operation.
SPI Chip Enable	**SPI_SS**	O2	Active low SPI chip enable input for optional external UPD350.
SPI Interrupt	**SPI_IRQ_N**	I	SPI interrupt indicating request for service from optional external UPD350.
DC/DC Control			
DAC Output (Source)	**DAC_DC**	AO	In the Source Role, this DAC output is used to control the DC/DC converter output voltage.
Miscellaneous			
VBUS Load Switch Enable	**EN_VBUS**	O8	When asserted, closes the VBUS load switch. Only valid in the Attach.SRC state.
VBUS Discharge	**VBUS_DIS**	O8	When asserted, enables external current sink in order to discharge VBUS.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port Control	**PRT_CTRL/OCS**	I/O2/OD2	When the UPD301A is in the Source Role, any external VBUS/VCONN/temperature faults may be wire-ORed on **OCS** to indicate a default has occurred, prompting the device's firmware to make VBUS safe (open load switches, discharge VBUS, and enter error recovery). When the UPD301A is in the Source Role, this pin is a bi-directional signal indicating various faults to a load switch, DC/DC converter, DFP or hub. This pin is nominally configured as an output, sending faults to a load switch or DC/DC converter. However, if a different fault condition (e.g. over-voltage) is detected internally by the UPD301A, this pin is reconfigured as an open-drain output with an internal pull-down enabled and asserted low for a duration to allow detection by the hub's PRT_ENx/OCSx_N input, and is then reconfigured back to an input. **Note:** For proper operation, a 100kOhm pull-up to +3.3V should be applied to this pin externally.
Type-C Orientation	**ORIENTATION_N**	O2	This signal is used to indicate which CC pin is terminated by the attached device. When asserted CC = CC1, otherwise CC=CC2. **Note:** For proper operation, a 200kOhm pull-up to +3.3V should be applied to this pin externally.
System Reset Input	**RESET_N_IN**	I	Active low system reset input. This reset is used for reset of the UPD301A by a companion MCU.
System Reset Output	**RESET_N_OUT**	O2	Active low system reset output. This pin must be connected to **RESET_N_COM** for proper operation.
System Reset Common	**RESET_N_COM**	IS	This pin must be connected to **RESET_N_OUT** for proper operation.
No Connect	**NC**	-	For proper operation, this pin must be left unconnected.
Configuration Straps			
Power Delivery Power Select 0 Configuration Strap	**PDP_SEL0**	I/O2	This multi-level configuration strap is sampled after system reset to specify a Power Delivery Power (PDP) which defines the voltages and currents to be used by the UPD301A Power Delivery Objects (PDOs). Refer to Section 3.3, "Configuration Straps" for additional information.
Power Delivery Power Select 1 Configuration Strap	**PDP_SEL1**	I/O2	For a two port system, this multi-level configuration strap is sampled after a system reset to specify a Power Delivery Power (PDP) which defines the voltages and currents to be used by the optional external UPD350 Power Delivery Objects (PDOs). Refer to Section 3.3, "Configuration Straps" for additional information.
I^2C Address Select Configuration Strap	**I2C_ADDR_SEL**	AIO	This multi-level configuration signal is sampled after a system reset to select the device's default I^2C slave address. Refer to Section 3.3, "Configuration Straps" for additional information.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Boot Select Configuration Strap	**BOOT_SEL**	IS	This configuration strap is sampled after a system reset to select between a normal boot or a boot ROM boot using a 200KΩ pull-down/up resistor. 0 = Boot from boot ROM 1 = Normal operation Refer to Section 3.3, "Configuration Straps" for additional information.
DC/DC Converter Configuration Strap	**DC_DC_SEL**	I/O2	This configuration strap is sampled after a system reset to select which DC/DC converter the DAC output is configured for. Refer to Section 3.3, "Configuration Straps" for additional information.
Power/Ground			
+5V Port Power Switch Input	**VCONN_IN**	P	+5V VCONN FET power source.
+3.3V I/O Power Supply Input	**VDD33_IO_IN**	P	+3.3V I/O power supply input.
+3.3V Analog Power Supply Input	**VDD33_ANA_IN**	P	+3.3V analog power supply input.
+3.3V Always Supply Input	**VDD33_ALW_IN**	P	+3.3V always supply input. **Note:** This pin must be connect to a 2.2 uF capacitor to ground.
+3.3V Regulator Power Supply Input	**VDD33_REG_IN**	P	+3.3V regulator power supply input.
+1.8V Core Voltage Power Supply Input	**VPP18**	P	+1.8V core voltage power supply input.
+1.8V Digital Core Power Supply Output	**VDD18_CORE_OUT**	P	+1.8V digital core power supply output. This signal must be connected to a 1uF capacitor to ground for proper operation.
+1.2V Core Power Supply Output	**VDD12_CORE_OUT**	P	+1.2V core power supply output. This signal must be connected to a 1uF capacitor to ground for proper operation.
Ground	**VSS**	P	Ground pins.

3.3 Configuration Straps

Configuration straps are used during Power-On Reset (POR) or external chip reset (RESET_N) to determine the default configuration of a particular feature. The state of the signal is latched following deassertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated functions.

3.3.1 PDP_SEL0/PDP_SEL1 CONFIGURATION STRAPS

The **PDP_SEL0** and **PDP_SEL1** configuration straps are used to define the normative Power Delivery Object (PDO) support in the Source Role, as defined in Chapter 10 of the USB Power Delivery Specification.

In the Source Role, the Power Delivery Power (PDP) defines all of the normative PDOs returned in the USB PD Source_Capabilities Message. These correspond to the fixed voltages and currents the Source supports.

The **PDP_SEL0** input configuration strap is used to define the PDP value used to configure the UPD301A.

The **PDP_SEL1** input configuration strap is used to define the PDP value used to configure the external UPD350 for the optional UPD301A two port solution.

The **PDP_SEL0** and **PDP_SEL1** configuration straps are each encoded to one of five possible values determined by external resistors. Table 3-3 indicates the PDP that each configuration corresponds to and the PDO values that should be returned in the USB Power Delivery Source capabilities.

TABLE 3-3: PDP_SEL RESISTOR ENCODING

PDP_SEL*x* Resistor Value	PDP	PDO 1	PDO 2	PDO 3	PDO 4
200 kΩ Pull-Down	7.5 W	5 V@1.5 A	-	-	-
200 kΩ Pull-Up	15 W	5 V@3 A	-	-	-
4.7 kΩ Pull-Down	27 W	5 V@3 A	9 V@3 A	-	-
4.7 kΩ Pull-Up	45 W	5 V@3 A	9 V@3 A	15 V@3 A	-
10 Ω Pull-Down	60 W	5 V@3 A	9 V@3 A	15 V@3 A	20 V@3 A

3.3.2 I2C_ADDR_SEL CONFIGURATION STRAP

The **I2C_ADDR_SEL** configuration strap is used to define the default I^2C address that the UPD301A will respond to when operating as a companion MCU. The **I2C_ADDR_SEL** configuration strap is encoded to one of six possible values determined by external resistors, as detailed in Table 3-4.

TABLE 3-4: I2C_ADDR_SEL RESISTOR ENCODING

I2C_ADDR_SEL Resistor Value	I^2C Slave Address
200 kΩ Pull-Down	1111_000
200 kΩ Pull-Up	1101_000
20 kΩ Pull-Down	1101_001
20 kΩ Pull-Up	1101_010
10 Ω Pull-Down	1101_011
10 Ω Pull-Up	1101_100

3.3.3 BOOT_SEL CONFIGURATION STRAP

The **BOOT_SEL** configuration strap is used to select the UPD301A boot mode between a normal boot or a boot ROM boot, and is implemented using a weak pull-up/pull-down of 200 kΩ, as shown in Table 3-5.

TABLE 3-5: BOOT_SEL RESISTOR ENCODING

BOOT_SEL Resistor Value	Setting
200 kΩ Pull-Down	Boot from boot ROM
200 kΩ Pull-Up	Normal operation

3.3.4 DC_DC_SEL CONFIGURATION STRAP

The **DC_DC_SEL** configuration strap is used to specify which DC/DC converter the DAC output is configured for.

The **DC_DC_SEL** configuration strap is encoded to one of three possible values determined by external resistors, as detailed in Table 3-6.

TABLE 3-6: DC_DC_SEL RESISTOR ENCODING

DC_DC_SEL Resistor Value	DAC Output
200 kΩ Pull-Down	General linear DAC operation. The DAC output range is defined as: • 0V - 0V on VBUS • 2.5V = 20V on VBUS This output is linear for the range in between.
200 kΩ Pull-Up	Reserved for future use.
4.7 kΩ Pull-Down	Reserved for future use.

4.0 FUNCTIONAL DESCRIPTIONS

This section provides functional descriptions of the following:

- Serial Peripheral Interface (SPI)
- Power States
- Cable Plug Orientation and Detection
- Baseband CC Interface (BCI)
- Power Delivery MAC
- Supported Power Delivery (PD) Functionality

4.1 Serial Peripheral Interface (SPI)

The UPD301A integrates a SPI master/slave controller which includes the following features:

- • Full-duplex, four-wire interface (**SPI_MISO**, **SPI_MOSI**, **SPI_SCK**, **SPI_SS**)
- • Single-buffered transmitter, double-buffered receiver
- • Master operation:
  - – Serial clock speed, $f_{SCK}=1/t_{SCK}$(Note 4-1)
  - – 8-bit clock generator
- • Slave operation:
  - – Serial clock speed, $f_{SCK}=1/t_{SSCK}$(Note 4-1)
  - – Optional 8-bit address match operation

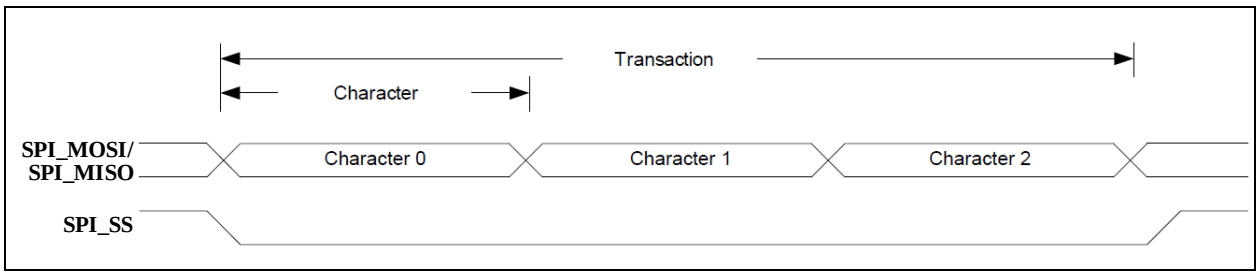
Note 4-1 For t_{SCK} and t_{SSCK} values, refer to Section 5.6.2, "SPI Timing"

The SPI is a high-speed synchronous data transfer interface which allows high-speed communication between the device and peripheral devices. The SPI can operate as a master or slave. As a master, the SPI initiates and controls all data transactions. The SPI is single buffered for transmitting and double buffered for receiving.

When transmitting data, a Data register is loaded with the next character to be transmitted during the current transmission. When receiving, the data is transferred to the two-level receive buffer, and the receiver is ready for a new character.

The SPI transaction format is shown in Figure 4-1. Each transaction can contain one or more characters. The character size is configurable, and can be either 8 or 9 bits.

FIGURE 4-1: SPI TRANSACTION FORMAT



The SPI master pulls the slave select line (**SPI_SS**) of the desired slave low to initiate a transaction. The master and slave prepare data to send via their respective shift registers, and the master generates the serial clock on the **SPI_SCK** line.

Data is always shifted from master to slave on the Master Output Slave Input line (**SPI_MOSI**); data is shifted from slave to master on the Master Input Slave Output line (**SPI_MISO**).

Each time character is shifted out from the master, a character will be shifted out from the slave simultaneously. To signal the end of a transaction, the master will pull the **SPI_SS** line high.

4.2 Power States

The device supports the following power states, as defined in their respective sub-sections:

- STANDBY
- ATTACHED IDLE
- ACTIVE

4.2.1 STANDBY

STANDBY is the lowest power functional state of the device. The majority of the device is powered off in this state. The internal CC comparator and 20 KHz oscillator are enabled in this state as well as requisite analog components (1.8V LDO, PORs, Biases, etc).

The CC lines are constantly monitored for an attach condition which shall result in an interrupt assertion to the host. If an attachment has been made, this state can detect a change in the partner's advertisement as well as a detach.

STANDBY is the power state that the UPD301A device will be in when in USB Type-C™ Unattached.SRC.

4.2.2 ATTACHED IDLE

In this state, a USB Type-C™ device is connected and the USB PD bus is idle (no USB packets in transit). The CC signals are constantly being monitored for packet transmission.

4.2.3 ACTIVE

This state defines the condition of the device after an attachment occurred. In this state, Power Delivery communication is supported. This state is also used for any condition in which the 48 MHz Relaxation Oscillator must be enabled, such as when it is desired to debounce a GPIO within the micro-second range.

When transmitting a Power Delivery packet, an additional 5 mA may be consumed. Additional power consumption results from enabling the OCS comparator, VBUS comparator and other modules. When VCONN FETs are enabled, there is an additional 70 mW of power consumption.

This section details the functions that control and monitor the CC pins, monitor the **VBUS_DET** pin, control the VCONN FETs, and sample the **CFG_SEL** pin.

4.3 Cable Plug Orientation and Detection

4.3.1 CC COMPARATOR

The device integrates a comparator and DAC circuit to implement Type-C attach and detach functions. It supports up to eight programmable thresholds for attach detection between UFP and DFP. When operating as a UFP, the device supports detecting changes in the DFP's advertised thresholds to determine current sourcing capability. The default nominal values for the thresholds detected by the CC comparators are:

- 0.20 V
- 0.40 V
- 0.66 V
- 0.80 V
- 1.23 V
- 1.60 V
- 2.60 V
- 3.0 V Proprietary Mode

TABLE 4-1: CABLE DETECT SUMMARY

Parameter	Threshold CSR	Description	Min	Typ	Max
DFP_ACT_DEF	CC_THR0	Detecting an active cable when configured as DFP and advertising default USB current.		0.20 V	
UFP_DFP_DEF	CC_THR0	Detecting DFP attach when configured as UFP and DFP is advertising default USB current.		0.20 V	
DFP_ACT_1A5	CC_THR1	Detecting an active cable when configured as DFP and advertising 1.5A.		0.40 V	
UFP_DFP_1A5	CC_THR2	Detecting DFP attach when configured as UFP and DFP is advertising 1.5A.		0.66 V	
DFP_ACT_3A0	CC_THR3	Detecting an active cable when configured as DFP and advertising 3.0A.		0.80 V	
UFP_DFP_3A0	CC_THR4	Detecting DFP attach when configured as UFP and DFP is advertising 3.0A.		1.23 V	
DFP_UFP_DEF	CC_THR5	Detecting UFP attach when configured as DFP advertising default USB current.		1.60 V	
DFP_UFP_1A5	CC_THR5	Detecting UFP attach when configured as DFP advertising 1.5A.		1.60 V	
DFP_UFP_3A0	CC_THR6	Detecting UFP attach when configured as DFP advertising 3.0A.		2.60 V	

The following table summarizes the expected thresholds to be matched for various configurations.

TABLE 4-2: DFP CC MATCH SUMMARY

CC State	CC THR0	CC THR1	CC THR2	CC THR3	CC THR4	CC THR5	CC THR6	CC THR7
Advertise Default USB Current and connected to powered cable	0	0	0	0	0	0	0	0
Advertise 1.5 A and connected to powered cable	0	0	0	0	0	0	0	0
Advertise 3.0 A and connected to powered cable	0	0	0	0	0	0	0	0
Advertise Default USB Current and connected to UFP	1	0	0	0	0	0	0	0
Advertise 1.5 A and connected to UFP	0	1	0	0	0	0	0	0
Advertise 3.0 A and connected to UFP	0	0	0	1	0	0	0	0
Advertise Default USB Current and no connect (vOpen)	1	0	0	0	0	1	0	0
Advertise 1.5 A and no connect (vOpen)	0	1	0	0	0	1	0	0
Advertise 3.0 A and no connect (vOpen)	0	0	0	1	0	0	1	0
Proprietary Mode and no connect (vOpen)	0	0	0	0	0	0	0	1

4.3.2 DFP OPERATION

The device implements current sources to advertise current charging capabilities on both CC pins when operating as a DFP.

When a UFP connection is established, the current driven across the CC pins creates a voltage across the UFP's Rd pull-down that can be detected by the integrated CC comparator. The voltages monitored are summarized in Table 4-3. When connected to an active cable, an alternative pull-down (Ra) appears on the CC pin.

The DFP also integrates two 5V FETs for implementing the VCONN function. This is further discussed in Section 4.3.5, "VCONN Operation".

TABLE 4-3: SOURCE DETECTION

CC1	CC2	Connection State	CC Comparator State	VBUS	VCONN
Open	Open	Nothing Attached	Monitor both CC pins for attach	Off	Off
Rd	Open	UFP Attached	Monitor **CC1** for detach	On	Off
Open	Rd	UFP Attached	Monitor **CC2** for detach	On	Off
Ra	Open	Powered Cable, No UFP attached	Monitor **CC2** for UFP attach. Monitor **CC1** for cable detach.	Off	Off
Open	Ra	Powered Cable, No UFP attached	Monitor **CC1** for UFP attach. Monitor **CC2** for cable detach.	Off	Off
Ra	Rd	Powered Cable, UFP attached	Monitor **CC2** for UFP detach. **CC1** is not monitored for detach.	On	On
Rd	Ra	Powered Cable, UFP attached	Monitor **CC1** for UFP detach. **CC2** is not monitored for detach.	On	On
Rd	Rd	Debug accessory mode attached	Monitor both CC pins for detach	Off	Off
Ra	Ra	Audio accessory mode attached.	Monitor both CC pins for detach	Off	Off

4.3.3 RP CURRENT SOURCES

In order to advertise the current charging capabilities of the device via the integrated port power controller or external power circuit, Rp current sources are used. The current source can be selected by software. Table 4-4 summarizes the values supported by the current sources in regards to the programmed value.

TABLE 4-4: RP CURRENT SOURCES

DFP Advertisement	Current source (1.7V to 5.5V)	RPx Value
Disabled		00b
Default USB Power	80 uA +/-20%	01b
1.5A @ 5V	180 uA +/-8%	10b
3.0A @ 5V	330 uA +/-8%	11b

4.3.4 COLLISION AVOIDANCE

An alternative mode of operation is required to enable the CC detection circuit to facilitate software implementation of collision detection which was incorporated into version 3.0 of the USB PD Specification.

In order to avoid message collisions due to asynchronous Messaging (AMS) sent from the Sink, the Source sets Rp to SinkTxOk (3A@5V) to indicate to the Sink that it is OK to initiate an AMS. When the Source wishes to initiate an AMS it sets Rp to SinkTxNG (1.5A@5V). When the Sink detects that Rp is set to SinkTxOk it may initiate an AMS. When the Sink detects that Rp is set to SinkTxNG it shall not initiate an AMS and shall only send Messages that are part of an AMS the Source has initiated.

4.3.5 VCONN OPERATION

VCONN is a 5V supply that is used to power circuitry in the USB Type-C™ plug, which is required to implement Electronically Marked Cables. By default, the DFP always sources VCONN when connected to an active cable. However, this may be changed by software.

APPLICATION NOTE: It is not envisioned to ever enable both FETs simultaneously.

VCONN is monitored for an over current condition via an internal monitoring circuit. A VCONN over current condition is recognized when the event persists for a time longer than specified.When an over-current VCONN event is detected, an interrupt asserts. The device may be configured to automatically disable the VCONN FET upon detection of a CC1/CC2 Back-Drive Error or VCONN Discharge Error. In the event of the detection of a debounced over-current VCONN event, the enabled VCONN FET will be disabled.

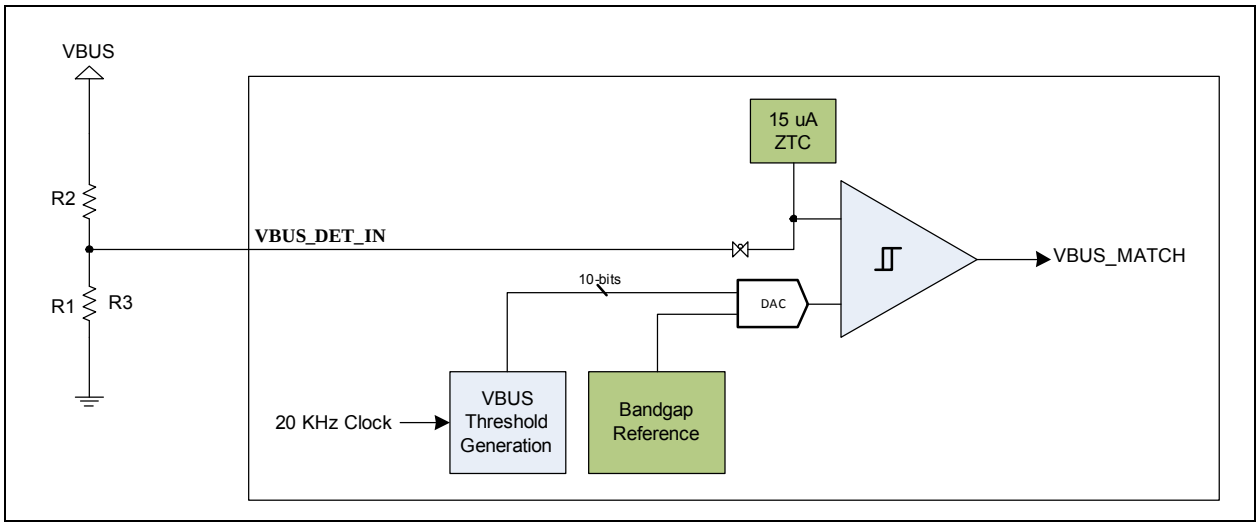
4.3.6 VBUS DETECTION

The device implements a comparator for determining when VBUS is within a programmed range, vSafe5V, or vSafe0v. VBUS is divided down externally via a 1:9 resistor divider to generate **VBUS_DET_IN**. **VBUS_DET_IN** is compared with an 8-bit threshold generated by an integrated DAC.

Figure 4-2 illustrates the **VBUS_DET_IN** circuit. In a typical use case, **VBUS_DET_IN** thresholds are programmed to track the following voltage ranges as defined in Table 4-5.

Note:	Table 4-5 illustrates the values of **VBUS_DET_IN** utilizing +/-1% accurate resistors where R1 is 10K Ohms and R2 is 90 kOhms.

FIGURE 4-2: VBUS_DET_IN COMPARATOR



For a DFP, the VBUS comparator is useful to detect when VBUS is within the desired range per PD negotiations. This is the case when VBUS is generated by a source external to the device.

For a UFP, the VBUS comparator is required to determine when a DFP is attached or detached. It may also use the comparator to determine when VBUS is within a new voltage range negotiated via PD.

TABLE 4-5: VBUS DETECTION THRESHOLDS

VBUS	Range	VBUS_DET_IN	Comments
20	21.5	2.11	
	18.5	1.82	
12	13.1	1.29	
	10.9	1.07	
8	8.9	0.88	
	7.1	0.69	
5	5.5	0.51	vSafe5V
	3.67	0.33	
0.68	0.68	0.068	vSafe0V

If supported, the ranges 8V, 12V and 20V may be programmed in VBUS Threshold 2 and VBUS Threshold 3 registers. Likewise 5V range, vSafe5v, can be programmed in VBUS Threshold 0 and VBUS Threshold 1 registers.

The threshold for vSafe0V is programmable.

VBUS_DET_IN monitoring logic operates off of the 20 KHz oscillator which cycles through each threshold. Including vSafe0v, a total of five values are compared.

4.4 Baseband CC Interface (BCI)

The device integrates a Baseband CC Interface (BCI) to facilitate USB Power Delivery communication. This module bridges between the PD MAC/BMC and the analog front end. Baseband communication is initiated by the PD MAC, which interfaces to the BCI. The BCI implements the digital functions required to control TX baseband components.

4.4.1 BASEBAND TX DATA-FLOW

The key responsibility of the BCI is to generate the wave form required for baseband communication. To this end, the BMC has a group of eight registers that define the Lo-Hi and Hi-Lo transitions for the generated BMC signal.

When instructed to transition from Lo-Hi, the BCI steps through all BB TX Rise Registers. Likewise when instructed to transition from Hi-Lo, the BCI steps through all BB TX Fall Registers

APPLICATION NOTE: The user may replicate values if it is desired to use less than twelve unique values for this purpose.

4.4.2 BASEBAND RX DATA-FLOW

Baseband RX data is received by the BCI from the RX analog front end where it is compared to a threshold programmed by software. The CC RX DAC Value defines the trip point used for reception of baseband data. The field shall be programmed to be 175 mV below the RX Eye center, as defined in the PD Specification for the mode in which the device is operating (Sourcing Power, Sinking Power, Power Neutral).

4.5 Power Delivery MAC

The PD MAC implements certain features of the protocol layer and physical layer of the Universal Serial Bus Power Delivery Specification. On one end the PD MAC interfaces to the software implementing the bulk of protocol and higher level layers and on the other end it interfaces to a BMC encoder / decoder module.

In addition to the normal TX and RX functions, the PD MAC implements the test mode logic defined in the USB PD specification (BIST).

The PD MAC supports the following features:

- Automatic TX Mode for packet framing and CRC32 insertion.
- Raw TX Mode for bit level packet control.
- Automatic GoodCRC response to received messages.
- Automatic BIST Error Count Message in BIST RX Mode.
- GoodCRCTimer implementation.
- Automatic retries with programmable retry count.
- Redundant receive packets automatically dropped in auto response mode.
- 74 byte TX queue.
- 128 byte RX queue.
- Programmable TX Bit-time. Allows for changing operating frequency.
- Programmable preamble length.
- BIST TX and RX logic.
- Programmable TX and RX queue modes - buffer mode and FIFO mode.
- CRC32 generator for TX.
- CRC32 calculator and comparator for RX.

4.5.1 PD MAC TRANSMITTER

The PD MAC transmitter is comprised of three major blocks:

- **TX Queue:**
  The TX Queue is where software loads the message to be transmitted.
- **TX Control:**
  The TX Control implements the necessary control logic. It is responsible for reading the data from the TX queue and based on the data processing mode (automatic or raw), processing the data to make it suitable (nibbles with control information) for use by the TX Comm. It is also responsible for generating packet framing and terminating the packet in automatic mode, and generating messages for automatic response (GoodCRC and BIST Error Count). TX Control also handles the selection of the SOP type that is to be transmitted.
- **TX Comm:**
  The TX Comm is comprised of a TX CRC generator, a 4b5b encoder, serializer, preamble generator, and TX bit timer. It takes the nibble data, computes and inserts the CRC, 5b encodes, and generates the baseband serial data. Preamble insertion is also performed by this logic.

4.5.2 PD MAC RECEIVER

The PD MAC receiver is comprised of three major blocks:

- **RX Queue:**
  The RX Queue is where software reads the received messages.
- **RX Control:**
  The RX Control implements the necessary control logic. It is responsible for validating the received packet, updating the RX Queue status, and triggering automatic responses, if required.
- **RX Comm:**
  The RX Comm is comprised of the Clock and Data Recovery (CDR), RX DES (de-serializer) (serial-to-parallel converter, 4b5b decoder, and framing detector), RX CRC32 (CRC calculator, receive timer), and other logic to detect valid packet reception.

4.5.3 PD MAC BIST

The PD MAC incorporates BIST functions as defined in the USB PD Specification. It is comprised of a TX and RX block.

The BIST TX block contains a PRBS (Pseudo Random Binary Sequence) generator, BIST pattern generation logic, and its own bit-timing logic. The SOP type used by TX BIST Test Frames is a 20-bit static vector which is created by multiplexing between the five SOP ordered sets based on a register setting. The resultant 20-bit vector is simply bit selected when the packet is transmitted.

The BIST RX block contains a PRBS generator and bit error detection logic. BIST RX is used only during the BIST Receiver Test.

4.6 Supported Power Delivery (PD) Functionality

This section details the UPD301A PD support in firmware. The UPD301A PD functionality operates according to the *USB Power Delivery Specification*. Table 4-6 details the PD parameter values used.

TABLE 4-6: USB PD VALUES

Parameter	Value
VendorID	0x0424
ProductID	0x301A
HWVersion	0x01
SiVersion	0x01
FWVersion1...4	Will vary based on latest major and minor revision. For example. c1.10 is represented by 0x0110 and will be returned as: • FWVersion1 = 0x0000 • FWVersion2 = 0x0000 • FWVersion3 = 0x0000 • FWVersion4 = 0x0110

4.6.1 SUPPORTED PD MESSAGES

The following USB PD Control messages are supported:

- GoodCRC
- Accept
- Reject
- Ping
- PS_RDY
- Get_Sink_Cap
- VCONN_Swap
- Wait
- Soft_Reset

The following USB PD Data messages are supported:

- Source_Capabilities
- Request
- BIST

The following USB PD Extended messages are supported:

- Firmware_Update_Request
- Firmware_Update_Response

4.6.2 UNSUPPORTED PD MESSAGES

The following USB PD Control messages are not supported:

- GotoMin
- DR_Swap
- PR_Swap
- Get_Source_Cap_Extended
- Get_Status
- FR_Swap
- Get_PPS_Status
- Get_Country_Codes

The following USB PD Data messages are not supported:

- Battery_Status
- Alert
- Get_Country_Info
- Vendor_Defined

The following USB PD Extended messages are not supported:

- Source_Capabilities_Extended
- Status
- Get_Battery_Cap
- Get_Battery_Status
- Battery_Capabilities
- Manufacturer_Info
- Security_Request
- Security_Response
- PPS_Status
- Country_Info
- Country_Codes

4.6.3 SOURCE POWER DELIVERY OBJECTS (PDOS)

The PDOs defined in the *USB PD Specification* Section 10.2.2 are used when in Source Role based on the selected value of the **PDP_SEL0** configuration strap and for the external UPD350 when in Source Role based on the selected value of the **PDP_SEL1**. These are the PDOs returned in the PD Source_Capabilities message and correspond to the capabilities of the Source power supply.

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage (**VCONN_IN**) (Note 5-1) . . . . . -0.3 V to +6.0 V

Supply Voltage (**VDD33_ALW_IN**, **VDD33_IO_IN**) (Note 5-1) . . . . . 0 V to +6.0 V

Supply Voltage (**VDD33_REG_IN**, **VDD33_ANA_IN**) (Note 5-1) . . . . . 0 V to +3.8 V

Supply Voltage (**VPP18**) (Note 5-1) . . . . . 0 V to +7.75 V

Pin voltage with respect to ground (Note 5-2) . . . . . **VSS**-0.6 V to **VDD33_REG_IN**+0.6 V

Pin voltage with respect to ground (**VBUS_DET_IN**) . . . . . -0.5 V to +3.96 V

Pin voltage with respect to ground (**CC1**, **CC2**, **SPI_MOSI_SI**, **EN_VBUS**, **RESET_N_COM**, **VBUS_DIS**, **I2C_ADDR_SEL**) . . . . . -0.5 V to +6.0 V

Storage Temperature . . . . . -55°C to +150°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . +/-2 kV

Note 5-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

Note 5-2 This rating does not apply to the following pins: **VBUS_DET_IN**, **CC1**, **CC2**, **SPI_MOSI_SI**, **EN_VBUS**, **RESET_N_IN**, **VBUS_DIS**

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 5.2, "Operating Conditions**", Section 5.5, "DC Characteristics", or any other applicable section of this specification is not implied.

5.2 Operating Conditions**

Supply Voltage (**VCONN_IN**) . . . . . +4.75 V to +5.25 V

Supply Voltage (**VDD33_ALW_IN**, **VDD33_IO_IN**) . . . . . +2.97 V to +3.63 V

Supply Voltage (**VDD33_REG_IN**, **VDD33_ANA_IN**) . . . . . +2.97 V to +3.63 V

Supply Voltage (**VPP18**) . . . . . +1.62 V to +1.98 V

Pin voltage with respect to ground (Note 5-3) . . . . . 0 V to +2.00 V

Positive pin voltage with respect to ground (**VBUS_DET_IN**) . . . . . **VDD33_IO_IN**-0.3 V to **VDD33_IO_IN**+0.3 V

Negative pin voltage with respect to ground (**VBUS_DET_IN**) . . . . . -0.33 V to -0.27 V

Positive pin voltage with respect to ground (**CC1**, **CC2**, **SPI_MOSI_SI**, **EN_VBUS**, **RESET_N_COM**, **VBUS_DIS**, **I2C_ADDR_SEL**) . . . . . +2.97 V to +3.63 V

Negative pin voltage with respect to ground (**CC1**, **CC2**, **SPI_MOSI_SI**, **EN_VBUS**, **RESET_N_COM**, **VBUS_DIS**, **I2C_ADDR_SEL**) . . . . . -0.33 V to -0.27 V

Power Supply Rise Time Max (T_{RT}) (**VDD33_IO_IN**) (Figure 5-1) 100ms

Power Supply Rise Rate Max (**VDD33_ANA_IN**, **VDD33_REG_IN**) . . . . . 0.1 V/µs

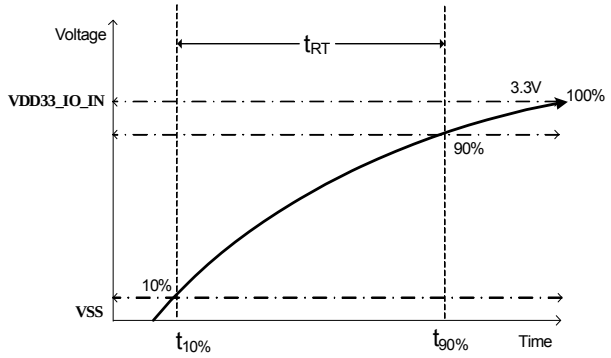
Ambient Operating Temperature in Still Air (T_A) . . . . . Note 5-4

Note 5-3 This rating does not apply to the following pins: **VBUS_DET_IN**, **CC1**, **CC2**, **SPI_MOSI_SI**, **EN_VBUS**, **RESET_N_COM**, **VBUS_DIS**

Note 5-4 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is assured only within the ranges specified in this section.

FIGURE 5-1: SUPPLY RISE TIME MODEL



5.3 Package Thermal Specifications

TABLE 5-1: PACKAGE THERMAL PARAMETERS

Parameter	Symbol	°C/W
Thermal Resistance Junction to Ambient (@ 0 air flow)	Θ_{JA}	36.6
Thermal Resistance Junction to Top of Case	Θ_{JC}	9.2
Thermal Resistance Junction to Board	Θ_{JB}	15.7
Thermal Resistance Junction to Bottom of Case (@ 0 air flow)	Ψ_{JT}	0.2

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

TABLE 5-2: POWER DISSIPATION

Parameter	Symbol	Max	Units
Power Dissipation	P_{dis}	214	mW

Note: This is the worst-case power dissipation as a consequence of maximum loading (before current-limiting protections take effect) upon the VCONN power switch, 3.3V power-ORing switch, analog blocks, and core digital logic.

5.4 Current Consumption

TABLE 5-3: DEVICE CURRENT CONSUMPTION

Power State	3.3V Supply Current		
	Typical	Max	Units
RESET	1.27	-	mA
STANDBY (source)	7.49	-	mA
ATTACHED IDLE (source)	11.40	-	mA
ACTIVE (with PD packet transmitting)	-	23.84	mA

Note 1: This table details the power consumption of the UPD301A device as measured during various modes of operation. Refer to Section 4.2, "Power States" for additional information. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements. Maximum values represent very short bursts of activity over a small amount of time. Typical values represent averaged current consumption over time.

2: **STANDBY** is equivalent to USB Type-C™ specification's Unattached.SRC

3: Currents measured with all 3.3V rails tied together.

5.5 DC Characteristics

TABLE 5-4: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
I Type Input Buffer						
Low Input Level	V_{IL}			0.3*VDD33_REG_IN	V	
High Input Level	V_{IH}	0.55*VDD33_REG_IN			V	
Input Leakage	I_{LEAK}	-1	±0.015	1	µA	
IS_1 Type Input Buffer						
Low Input Level	V_{IL}			0.3*VDD33_REG_IN	V	
High Input Level	V_{IH}	0.55*VDD33_REG_IN			V	
Input Leakage	I_{IH}	-1	±0.015	1	µA	
IS_2 Type Input Buffer						
Low Input Level	V_{ILI}	-0.3		0.8	V	
High Input Level	V_{IHI}	2.0		3.6	V	
Negative-Going Threshold	V_{ILT}	1.21	1.33	1.8	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.31	1.58	1.8	V	Schmitt trigger
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	100	133	0	mV	
Input Leakage (V_{IN} = VSS or VDD33_IO_IN)	I_{IH}	-10		10	µA	Note 5-5
Input Capacitance	C_{IN}			3	pF	
O2 Type Output Buffer						
Low Output Level	V_{OL}		0.1*VDD33_REG_IN	0.2*VDD33_REG_IN	V	I_{OL} = -2 mA
High Output Level	V_{OH}	0.8*VDD33_REG_IN	0.9*VDD33_REG_IN		V	I_{OH} = 2 mA
OD2 Type Output Buffer						
Low Output Level	V_{OL}		0.1*VDD33_REG_IN	0.2*VDD33_REG_IN	V	I_{OL} = -2 mA
O8_1 Type Output Buffer						
Low Output Level	V_{OL}		0.1*VDD33_REG_IN	0.2*VDD33_REG_IN	V	I_{OL} = -8 mA
High Output Level	V_{OH}	0.8*VDD33_REG_IN	0.9*VDD33_REG_IN		V	I_{OH} = 8 mA
O8_2 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = -8 mA
High Output Level	V_{OH}	VDD33_IO_IN - 0.4			V	I_{OH} = 8 mA

Note 5-5 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50 µA per-pin (typical).

TABLE 5-5: VOLTAGE REGULATOR OPERATING RANGES

Pin Name	Parameter	Min	Typ	Max	Units
VDD18_CORE_OUT	DC uncalibrated output voltage	1.62	1.80	1.91	V
VDD12_CORE_OUT	DC calibrated output voltage	1.10	1.23	1.30	V

TABLE 5-6: VCONN SOURCE DC PARAMETERS

Parameter	Symbol	Min	Typ	Max	Units	Notes
ILIM	I_{LIM_VCONN}		600		mA	**VCONN_IN**=5V
On Resistance	R_{ON_VCONN}		270		mΩ	

TABLE 5-7: POWER SWITCH DC PARAMETERS

Parameter	Symbol	Min	Typ	Max	Units	Notes
VSW Load	VSW_Load			100	mA	**VDD33_ALW_IN** = 3.3V
VSW Resistance	R_VSW		500		Ω	

5.6 AC Characteristics and Timing

This section details the various AC timing specifications of the device.

5.6.1 RESET_N TIMING

Figure 5-2 illustrates the **RESET_N** timing requirements. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified

FIGURE 5-2: RESET_N TIMING

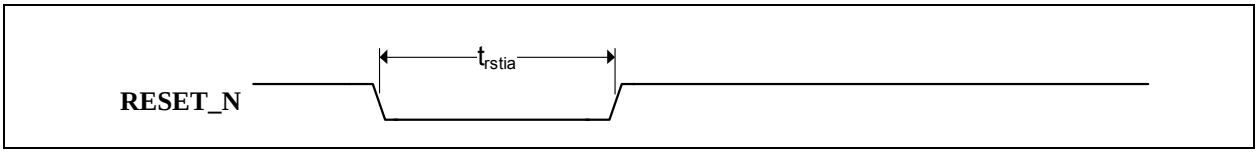


TABLE 5-8: RESET_N TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	1			µs

5.6.2 SPI TIMING

Figure 5-3 and Figure 5-4 illustrate the SPI master and slave timing requirements, respectively. Refer to Section 4.1, "Serial Peripheral Interface (SPI)" for additional information.

FIGURE 5-3: SPI MASTER TIMING

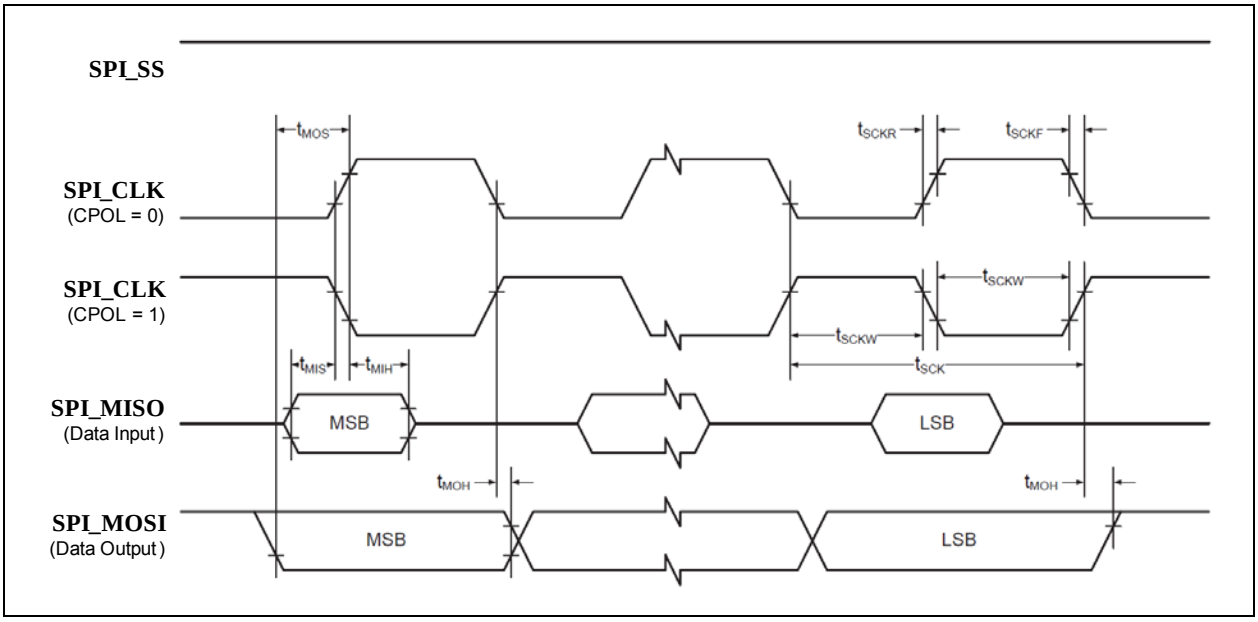


FIGURE 5-4: SPI SLAVE TIMING

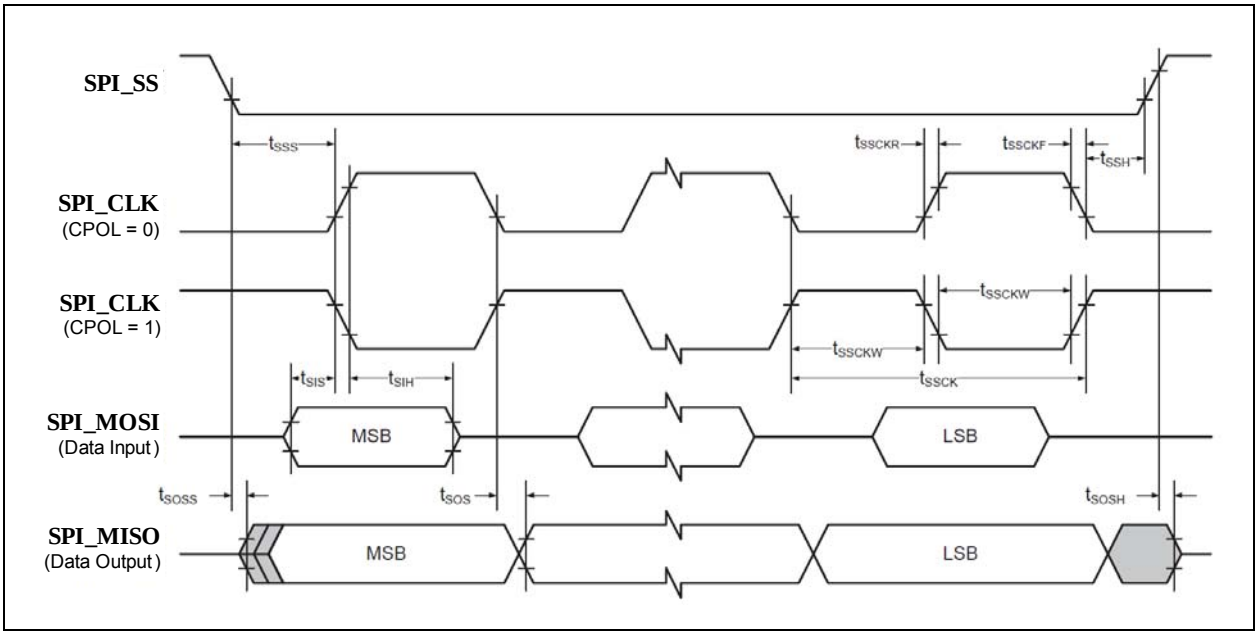


TABLE 5-9: SPI TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{SCK}	**SPI_CLK** period (Master)		84		
t_{SCKW}	**SPI_CLK** high/low width (Master)		$0.5*t_{SCK}$		
t_{SCKR}	**SPI_CLK** rise time (Master)		7		ns
t_{SCKF}	**SPI_CLK** fall time (Master)		9.5		ns
t_{MIS}	**SPI_MISO** setup to **SPI_CLK** (Master)		29		ns
t_{MIH}	**SPI_MISO** hold after **SPI_CLK** (Master)		8		ns
t_{MOS}	**SPI_MOSI** setup to **SPI_CLK** (Master)		$t_{SCK}/2 - 16$		ns
t_{MOH}	**SPI_MOSI** hold after **SPI_CLK** (Master)		16		ns
t_{SSCK}	**SPI_CLK** period (Slave)	$1*t_{CLK\_APB}$			ns
t_{SSCKW}	**SPI_CLK** high/low width (Slave)	$0.5*t_{SSCK}$			ns
t_{SSCKR}	**SPI_CLK** rise time (Slave)		7		ns
t_{SSCKF}	**SPI_CLK** fall time (Slave)		9.5		ns
t_{SIS}	**SPI_MOSI** setup to **SPI_CLK** (Slave)	$t_{SSCK}/2-19$			ns
t_{SIH}	**SPI_MOSI** hold after **SPI_CLK** (Slave)	$t_{SSCK}/2-5$			ns
t_{SSS}	**SPI_SS** setup to **SPI_CLK** (Slave, PRELOADEN=1)	$2*t_{CLK\_APB} + t_{SOS}$			ns
	SPI_SS setup to **SPI_CLK** (Slave, PRELOADEN=0)	$t_{SOS}+7$			ns
t_{SSH}	**SPI_SS** hold after **SPI_CLK** (Slave)	$t_{SIH}-4$			ns
t_{SOS}	**SPI_MISO** setup to **SPI_CLK** (Slave)		$t_{SSCK}/2-20$		ns
t_{SOH}	**SPI_MISO** hold after **SPI_CLK** (Slave)		20		ns
t_{SOSS}	**SPI_MISO** setup after **SPI_SS** low (Slave)		16		ns
t_{SOSH}	**SPI_MISO** setup after **SPI_SS** high (Slave)		11		ns

6.0 PACKAGE INFORMATION

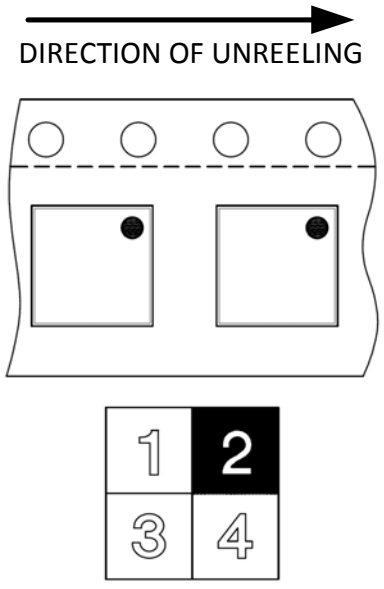
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 6-1: PACKAGE MARKING INFORMATION

40-VQFN

Legend:	*i*	Temperature range designator (Blank = commercial, *i* = industrial/automotive)
	V	Automotive (blank for non-automotive versions)
	R	Functional revision
	nnn	Internal code
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

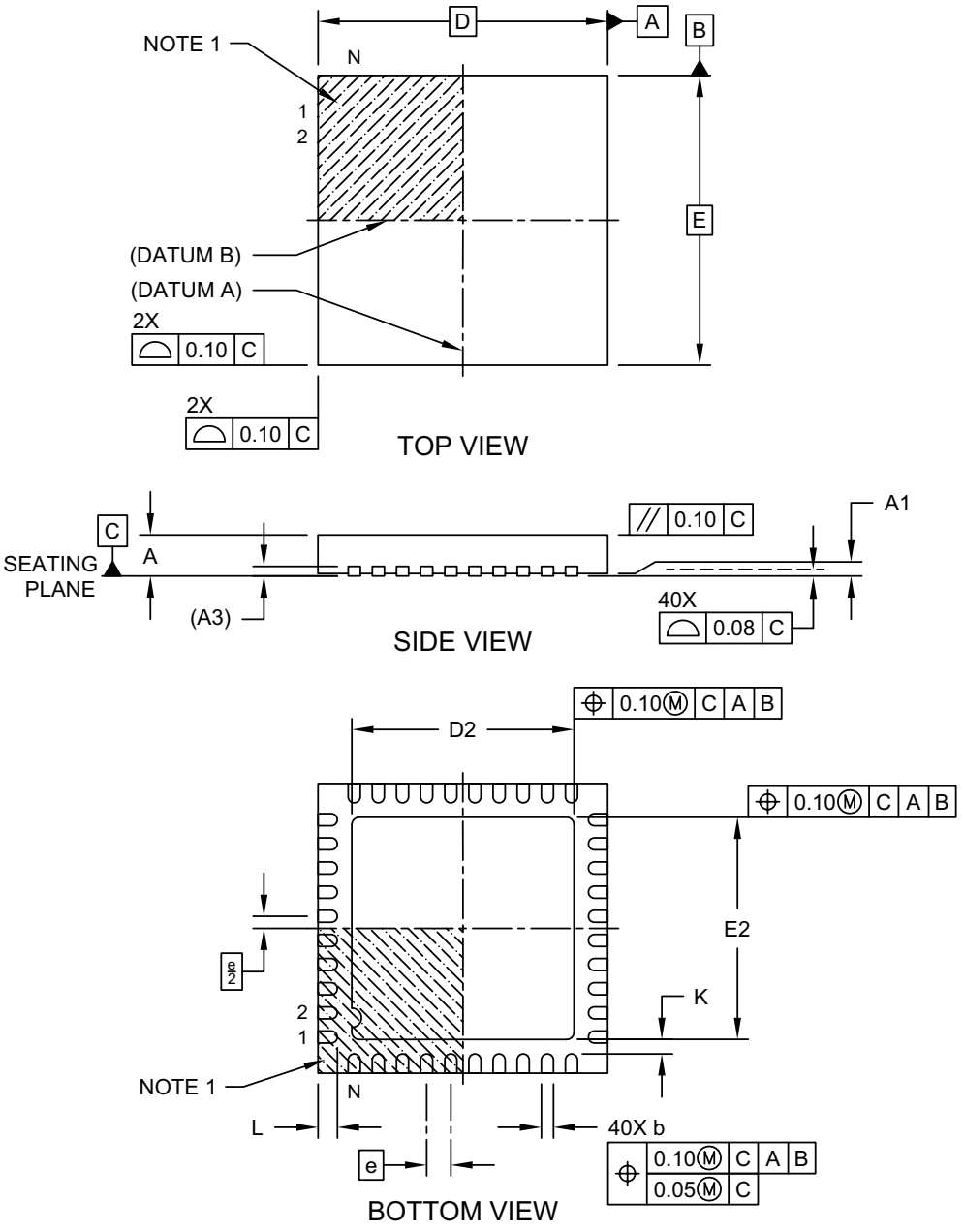
FIGURE 6-2: TAPE & REEL DEVICE ORIENTATION



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 6-3: 40-VQFN PACKAGE (DRAWING)

40-Lead Very Thin Plastic Quad Flat, No Lead Package (KYX) - 6x6 mm Body [VQFN] With 4.6x4.6 mm Exposed Pad

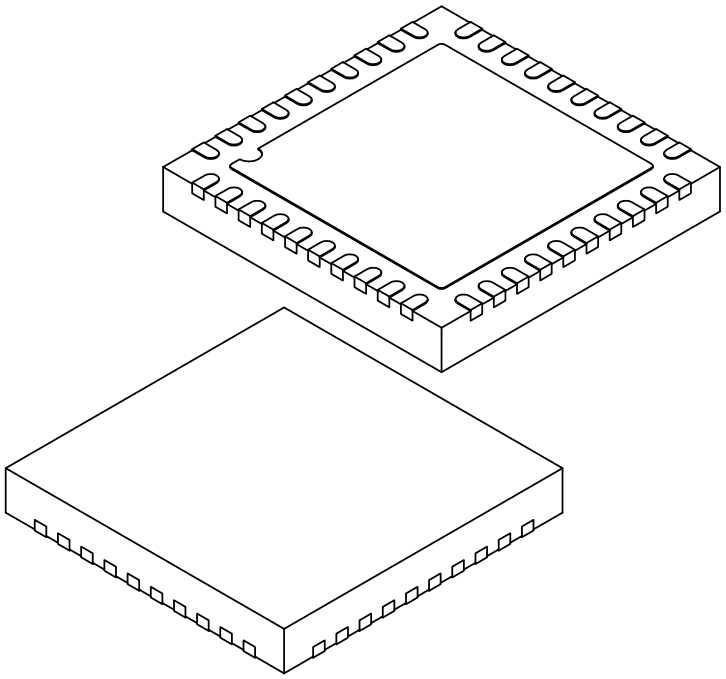


Microchip Technology Drawing C04-473 Rev. A Sheet 1 of 2

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 6-4: 40-VQFN PACKAGE (DIMENSIONS)

40-Lead Very Thin Plastic Quad Flat, No Lead Package (KYX) - 6x6 mm Body [VQFN] With 4.6x4.6 mm Exposed Pad



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		40	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.07
Terminal Thickness	A3		0.20 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.50	4.60	4.70
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.50	4.60	4.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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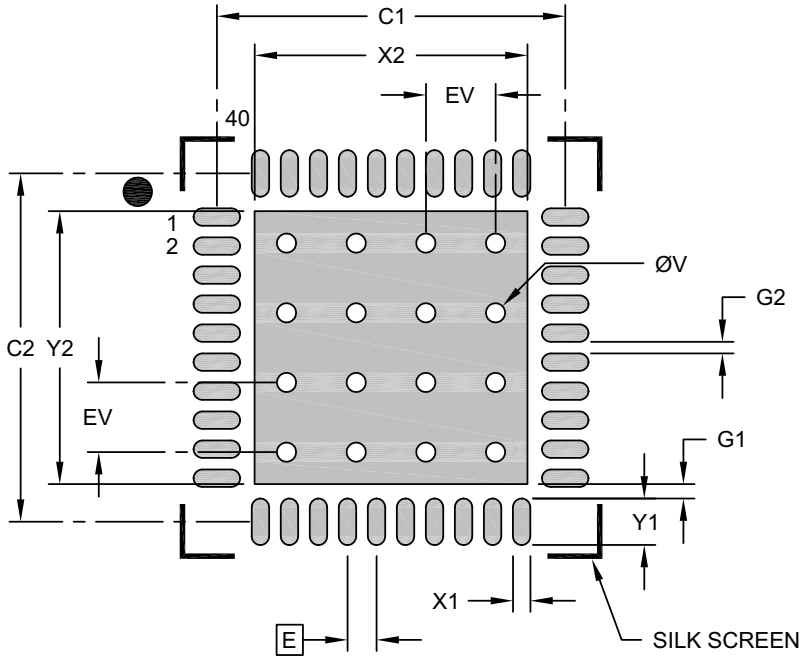
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 6-5: 40-VQFN PACKAGE (LAND PATTERN)

40-Lead Very Thin Plastic Quad Flat, No Lead Package (KYX) - 6x6 mm Body [VQFN] With 4.6x4.6 mm Exposed Pad



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			4.70
Optional Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X40)	X1			0.30
Contact Pad Length (X40)	Y1			0.80
Contact Pad to Center Pad (X40)	G1	0.20		
Contact Pad to Contact Pad (X36)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2473 Rev. A

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002838B (08-27-19)	Public Release	
DS00002838A (11-29-18)	Initial Document Release	

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PART NO.	[X](1)	[X]	/XX	[XXX]
Device	Tape & Reel Option	Temp. Range	Package	Automotive Code

Device:	UPD301A	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	Blank I	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial/Automotive Grade 3)
Package:	KYX	= 40-pin VQFN
Automotive Code:	Vxx	= 3 character code with “V” prefix, specifying automotive grade 3 product.

Examples:

a) UPD301A/KYX
Standard packaging,
0°C to +70°C,
40-pin VQFN package

b) UPD301AT/KYX
Tape and Reel,
0°C to +70°C,
40-pin VQFN package

c) UPD301A-I/KYX
Standard packaging,
-40°C to +85°C,
40-pin VQFN package

d) UPD301A-I/KYX
Tape and Reel,
-40°C to +85°C,
40-pin VQFN package

e) UPD301A-I/KYXVAO
Standard packaging,
-40°C to +85°C,
40-pin VQFN package,
Automotive Grade 3

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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