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MICROCHIP

ATTPM20P

Trusted Platform Module (TPM) 2.0 - SPI Interface Summary Data Sheet

Introduction

The Microchip ATTPM20P is a fully integrated security cryptoprocessor designed to be integrated into personal computers, embedded systems and IoT platforms. It implements version 2.0 of the Trusted Computing Group® (TCG) specification for Trusted Platform Modules (TPM).

Features

- Compliant to the Trusted Computing Group (TCG) Trusted Platform Module (TPM) Version 2.0, r116 Trusted Platform Module Library
- Single-Chip Turnkey Solution
- Hardware Asymmetric Crypto Engine
- Microchip ARM® M0+Microprocessor
- Internal FLASH Storage for Keys
- Serial Peripheral Interface (SPI) Protocol up to 36 MHz
- Secure Hardware and Firmware Design and Device Layout
- FIPS-140-2 Module Compliant Including the High-Quality Random Number Generator (RNG), HMAC, AES, SHA, ECC, and RSA Engines
- 8-pad UDFN Package for the Industry Smallest TPM 2.0 Device
- Offered in both Commercial (0°C to + 70°C) and Industrial (-40°C to +85°C) Temperature Range for both the 1.8V and 3.3V Supply Voltage ranges
- Cryptographic Support for:
  - HMAC
  - AES-128
  - SHA-1
  - SHA-256
  - ECC BN_P256, ECCNIST_P256
  - RSA 1024-2048 bit keys
- 16 KB of User-Accessible Nonvolatile Memory
- X.509 EK Certificates (*Optional*)
- Pre-Generated Endorsement Keys

Table of Contents

1. Pin Configurations and Pinouts

Table 1-1. Pin Configuration

Pin Name	Function
V_{CC}	Supply Voltage
GND	Ground
MISO	SPI Client Data Output
MOSI	SPI Client Data Input
PIRQ#	SPI Interrupt Requests
SPI_CLK	SPI Clock Input
SPI_CS#	SPI Chip Select
SPI_RST#	SPI Reset Pin

Figure 1-1. 8-Pad UDFN Pinout Diagram

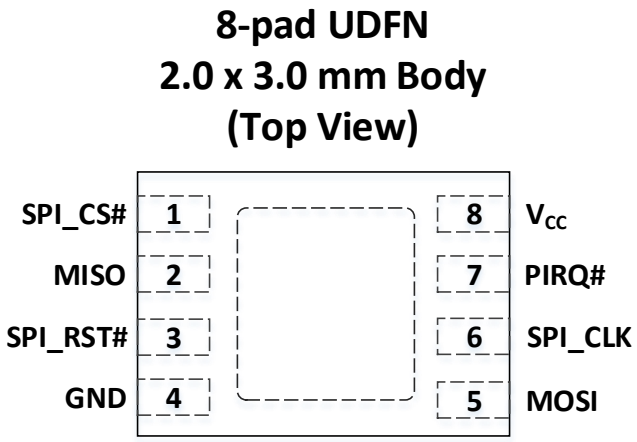


Table 1-2. Pin Descriptions

Pin	Pin Type	Description
V_{CC}	Power	Power Supply. Proper decoupling is required.
GND	Power	System Ground.
MISO	Output	Host In Client Out. This pin serves as the SPI Data Output from the TPM.
MOSI	Input	Host Out Client In. This pin serves as the SPI Data Input to the TPM.
PIRQ#	Open Drain Output	SPI Interrupt Pin, active-low. This pin is used by the TPM to assert interrupts. If unused, it is recommended to tie this pin to ground directly or through a 4.7 kΩ resistor.
SPI_CLK	Clock Input	Input Clock to drive the SPI bus. It is recommended to assert this pin high for power savings when the TPM is not in use.

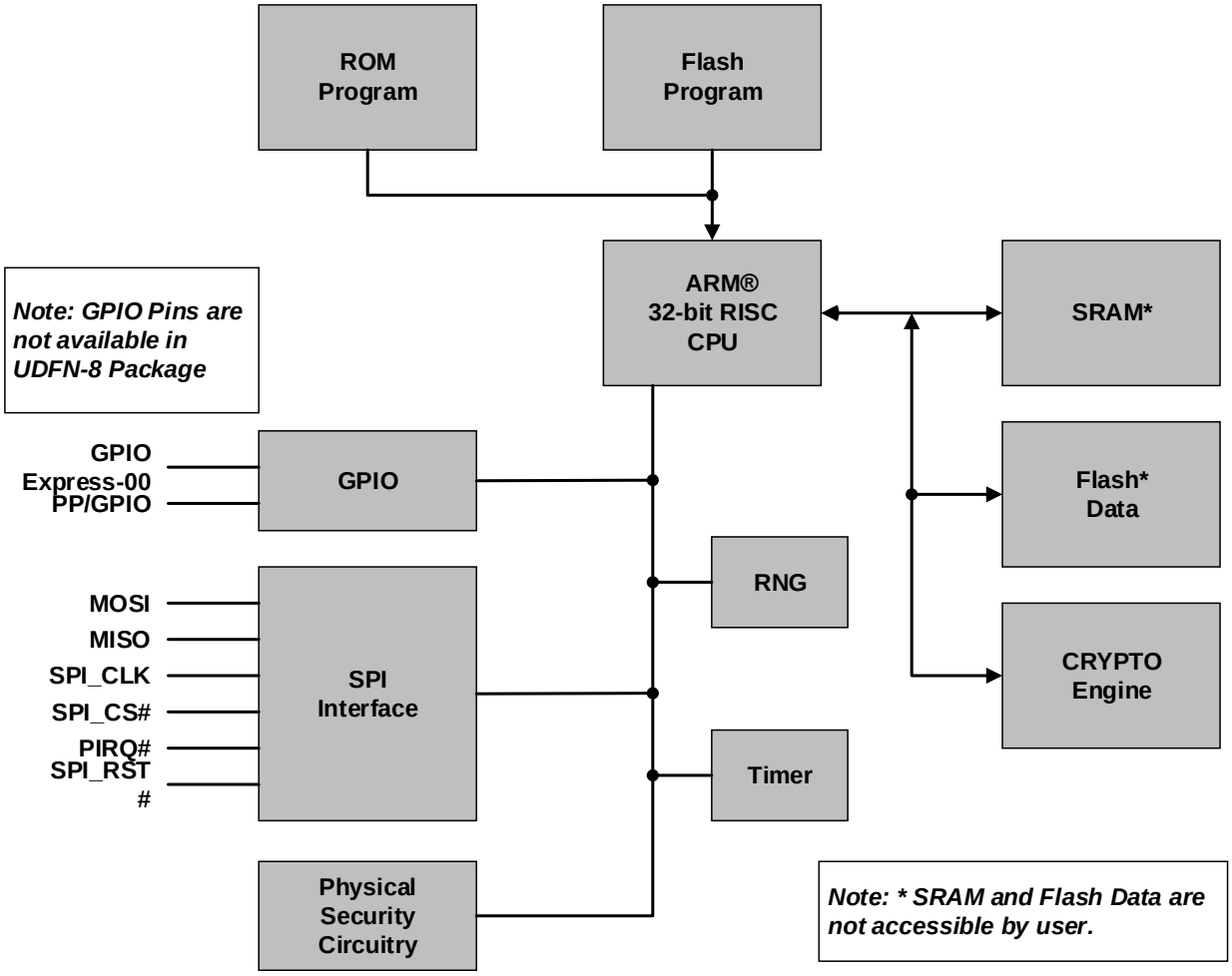
.....continued

Pin	Pin Type	Description
SPI_CS#	Input	SPI_CS# Chip Select, active-low. The TPM device will be selected when the chip select is asserted LOW.
SPI_RST#	Input	SPI Reset Pin, active-low. Pulsing this signal low resets the internal state of the TPM, and is equivalent to the removal/restoration of power to the device. The required minimum reset pulse width is 2 µs. On power-up, it is critical that the reset be kept active-low until the V_{CC} and SPI_CLK stabilize. To be compliant with TCG requirements, this pin needs to be tied to the system reset. TPM_Init is indicated by asserting this pin.

Notice: The SPI standard uses the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

2. Block Diagram

Figure 2-1. Block Diagram



Random Number Generator

The ATTPM20P includes a hardware Random Number Generator (RNG), configured as a FIPS Deterministic Random Bit Generator (DRBG) that is used for key generation and TCG protocol functions. The RNG is also available to the system to generate random numbers that may be needed during normal operation.

Physical Security

The ATTPM20P has voltage and temperature tampers, an active shield and other physical security measures built into the device.

TCG Documentation

The ATTPM20P has been designed to be compliant with the Trusted Computing Group TPM 2.0 specification. Full documentation for TCG primitives can be found in the TCG Trusted Platform Module Library, parts 1 to 3, on the TCG website: https://www.trustedcomputinggroup.org. TPM features specific to PC client platforms are specified in TCG PC Client Platform TPM Profile (PTP) specification, also available on the TCG website.

Turnkey Solution

The ATTPM20P is offered to OEM and ODM manufacturers as a turnkey solution, including the firmware integrated on the chip. If custom firmware requirements are needed, please contact Microchip Sales for more information.

3. Design Considerations

The following sections provide considerations when implementing the ATTPM20P into a given system.

3.1 SPI Design Considerations

1. The TPM SPI Interface is always configured to be in client mode.
2. The bit order on the SPI Interface is Most Significant bit (MSb) first.

Notice: The SPI standard uses the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

3.2 Wait State

The TPM may insert Wait states per the TCG PC Client specification.

3.3 Available Key Storage

The ATTPM20P provides support for the loading of up to ten 2048-bit RSA or ECC keys. These key slots are in addition to the root keys allocated for the Platform, Storage and Endorsement Hierarchies (i.e., PPK, SRK and EK).

3.4 Standard Mode Self-Test

Following a power-up event or a reset, the TPM will execute a series of self-tests of the TPM capabilities. ATTPM20P splits the TPM power-on self-tests into two groups as defined by the PTP. The initial group is executed immediately upon TPM power-up. The initial ATTPM20P self-test includes verification of the RNG and the SHA capabilities for secure boot operations.

The remaining tests of critical internal resources are performed at a later time, either:

- After the TPM2_SelfTest command is issued
- Upon receipt of the TPM2_IncrementalSelftest command
- Upon receipt of a command that requires TPM resources that were not tested

In the event that a TPM command calls an untested resource, the TPM may return TPM_RC_TESTING and automatically complete internal self-test operations. The requesting software will then be required to resend the original command.

4. TCG PC Client Platform TPM Profile (PTP) Specification Summary

The Microchip TPM SPI communications protocol is implemented in accordance with the TCG PC Client Platform TPM Profile (PTP) Specification 1.3. A complete description of the protocol is contained in the specification available at www.trustedcomputinggroup.org. It is recommended that application development and platform system design be based on the TCG PTP specification.

TPM_DID_VID_x Register
The TPM_DID_VID_x register contains Device ID (DID) and Vendor ID (VID) information. The VID register contents are assigned by the TCG Administration and contain the hex string `0x01 0x01 0x01 0x04`.

DID Register
The ATTPM20P DID register contains the device ID information and this is set to `0x03 0x02 0x00 0x05`.

TPM_RID_x register
The ATTPM20P Revision ID (RID) register is a single byte register containing revision information. Current value is set to `0x01`.

Firmware Revision Information
The current firmware revision can be found by executing the TCG TPM2_GetCapability command.

Important: Per the TCG specification, the TPM2_Startup command must be issued to the TPM device before any other command can be executed successfully. This includes the TPM2_GetCapability command.

Table 4-1. TCG formatted input command structure:

Raw input: `80 01 00 00 00 16 00 00 01 7A 00 00 00 06 00 00 01 0B 00 00 00 01`

Name	Value
tag	`0x80 0x01`
commandSize	`0x00 0x00 0x00 0x16`
commandCode	`0x00 0x00 0x01 0x7A`
capability	`0x00 0x00 0x00 0x06` (TPM_CAP_TPM_PROPERTIES)
property	`0x00 0x00 0x01 0x0B` (TPM_PT_FIRMWARE_VERSION_1)
propertyCount	`0x00 0x00 0x00 0x01`

Table 4-2. TCG formatted Output Command Structure:

Expected Output: `80 01 00 00 00 1B 00 00 00 00 01 00 00 00 06 00 00 00 01 00 00 01 0B` **`02 00 50 XX`**

Name	Value
tag	`0x80 0x01`
responseSize	`0x00 0x00 0x00 0x1B`
responseCode	`0x00 0x00 0x00 0x00`
moreData	`0x01`
capability	`0x00 0x00 0x00 0x06` (TPM_CAP_TPM_PROPERTIES)

.....continued

Name	Value
propertyCount	0x00 0x00 0x00 0x01
property	0x00 0x00 0x01 0x0B (TPM_PT_FIRMWARE_VERSION_1)
Firmware Version	0x02 0x00 0x50 0xXX

5. TCG TPM Command Data Bytes Transfer Format

5.1 TCG TPM Command Protocol

The TPM command protocol, as defined by the TCG TPM specification, specifies an initial predefined sequence of 10 data bytes for all commands transmitted to the TPM and also for all responses returned by the TPM. A required component of this 10-byte sequence is commandSize, which specifies the total number of data bytes in the command input or the response output.

The TPM uses a combination of commandSize and the host deasserting SPI_CS# inactive high to define the termination point of all input and output sequences. After the input or output sequence has completed, the TPM automatically enters an Idle (Wait) state until the next communication is received from the host. A new input or output sequence is initiated by the host asserting SPI_CS# active-low.

5.2 TCG Command - Incoming Operands and Sizes

Every TCG command begins with 10 initial bytes that contain information common to all commands:

- tag (two bytes) — Specifies the authorization session type for the command
- commandSize (four bytes) — Total number of input bytes including tag and commandSize
- commandCode (four bytes) — Command code as defined in TCG TPM specification

Following the 10-byte preamble, the SPI host continues to transmit the remaining command data bytes as specified by the TCG TPM specification until the total number of bytes reaches commandSize.

Table 5-1. Command Data Written to the TPM

tag[0]	tag[1]		
commandSize[0]	commandSize[1]	commandSize[2]	commandSize[3]
commandCode[0]	commandCode[1]	commandCode[2]	commandCode[3]

5.3 TCG Command - Outgoing Operands and Sizes

The TPM will respond to every TCG command with 10 initial bytes that contain information common to all commands:

- tag (two bytes) — Specifies the authorization session type for the command
- responseSize (four bytes) — Total number of output bytes including tag and responseSize
- responseCode (four bytes) — The return code of the operation

Following the 10-byte preamble, the TPM continues to output data until the total number of data bytes reaches responseSize. Depending on the command, zero bytes of data are possible. After output of the final data byte and the host writing Command_Ready to a one, the TPM enters an Idle state until the next valid SPI command sequence is initiated by the host.

Table 5-2. Response Data Read from the TPM

tag[0]	tag[1]		
responseSize[0]	responseSize[1]	responseSize[2]	responseSize[3]

responseCode[0]	responseCode[1]	responseCode[2]	responseCode[3]
data[0]	data[1]	...	...
data[responseSize-3]	data[responseSize-2]	data[responseSize-1]	data[responseSize]

6. Background Operations

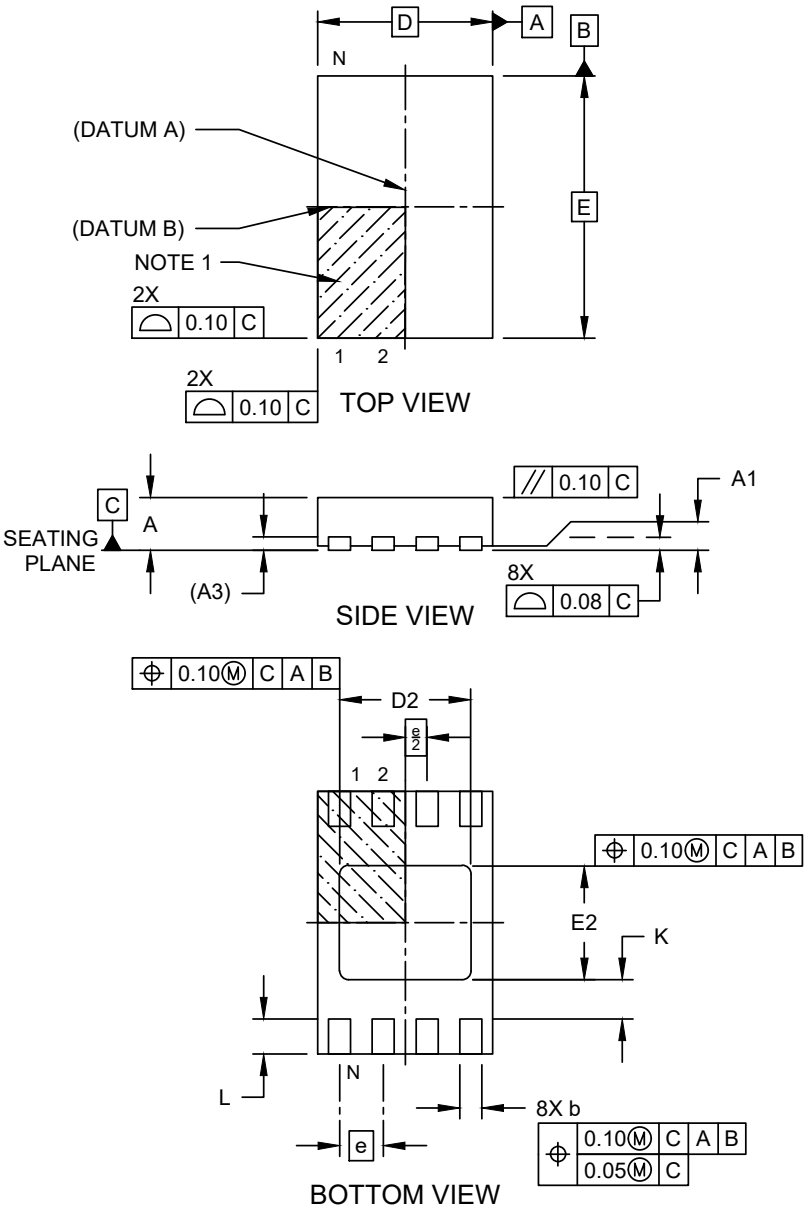
The ATTPM20P enters the Idle mode between the end of execution of an initial TCG command and preparation to receive the next command. During Idle mode, the TPM may automatically begin execution of background operations in order to reduce execution time when those capabilities are required in the future. Background operations are aborted if activity is detected on the data bus.

7. Package Drawings

7.1 8 Pin UDFN Package Drawing

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21355-Q4B Rev B Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

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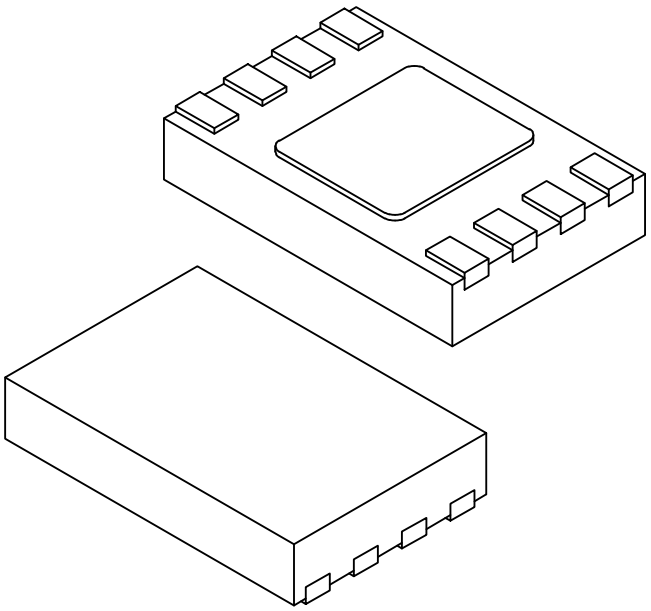

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev B Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

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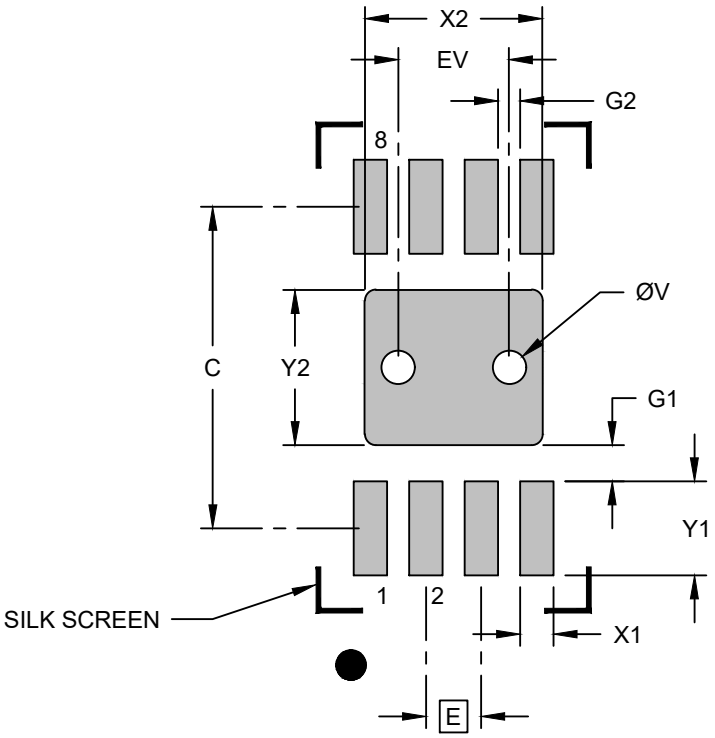

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev B

7.2 TPM 2.0 Standard Packages

The TCG TPM 2.0 working group has defined an industry standard 32 QFN pinout. For more information on obtaining this product in a TCG standard package format please contact Microchip Sales.

7.3 Package Marking

As part of Microchip's overall security features, the part mark for all TPM Security devices is intentionally vague. The marking on the top of the package does not provide any information as to the actual device type or the manufacturer of the device. The alphanumeric code on the package provides manufacturing information and varies with assembly lot. The packaging mark is not recommended to be used as part of the incoming inspection procedure.

8. Revision History

Revision C (December 2020)

- Added 1.8V operation back to the feature list for both Industrial and Commercial Temperature ranges.
- Modified wording in Package Marking Disclaimer to indicate TPM security devices instead of CryptoAuthentication Devices.
- Updated Portion of ordering code to G6 and H6 from G3 and H3 to reflect newest silicon revision. 1.8V supply range is now supported for industrial grade products. G3/H3 silicon is no longer available for sale.
- Updated Revision information in TCG PC Client Platform TPM Profile (PTP) Specification Summary section.
- Updated SPI Terminology.
- Updated UDFN Package Outline Drawings to latest version.

Revision B (September 2019)

- Removed 1.8V operation from the Features list.

Revision A (December 2018)

- Original release of this document. Generated from the full version of the Trusted Platform Module (TPM) 2.0 - SPI Interface data sheet. Microchip Doc#: DS40002064.

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PART NO.	-XX	XXX	-XX	(-X)
Device	Temp Range	Package Code	Mfg ID	Shipping Option

Device:	ATTPM20P: TPM 2.0 Cryptographic processor with SPI Interface	
Temperature Range	G6	Commercial Range 0°C to +70°C
	H6	Industrial Range -40°C to +85°C
Package Options	MA1	8-Pad 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat NoLead Package (UDFN)
MFG Code	-10	Pre-generated Endorsement Key
Tape and Reel Options		Tape and Reel in 3K quantity

PIS Examples:

ATTPM20P-G6MA1-10	ATTPM20P SPI Device, Commercial Temp Range, UDFN Package, Pre-generated Endorsement Key, 3K Tape and Reel
ATTPM20P-H6MA1-10	ATTPM20P SPI Device, Industrial Temp Range, UDFN Package, Pre-generated Endorsement Key, 3K Tape and Reel

PIS Notes:

1. No Special code for 3K Tape and Reel.

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