TP2435

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- Low Threshold
- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Linear Amplifiers
- Analog Switches
- Power Management
- Telecommunication Switches

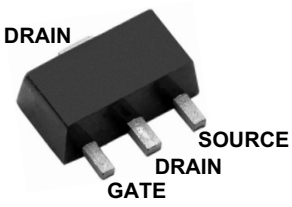
General Description

The TP2435 low-threshold Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type

3-lead SOT-89
(Top view)



See Table 3-1 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Gate-to-Source Voltage ..... ±20V
Operating Ambient Temperature, T_A ..... -55°C to +150°C
Storage Temperature, T_S ..... -55°C to +150°C

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	-350	—	—	V	V_{GS} = 0V, I_D = -250 µA
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	-2.4	V	V_{GS} = V_{DS}, I_D = -1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1 mA (**Note 1**)
Gate Body Leakage Current	I_{GSS}	—	—	-100	nA	V_{GS} = ± 20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	-10	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	-1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 1**)
On-State Drain Current	$I_{D(ON)}$	-0.3	—	—	A	V_{GS} = -4.5V, V_{DS} = -25V
		-0.8	—	—	A	V_{GS} = -10V, V_{DS} = -25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	15	Ω	V_{GS} = -3V, I_D = -20 mA
		—	—	15	Ω	V_{GS} = -4.5V, I_D = -150 mA
		—	—	15	Ω	V_{GS} = -10V, I_D = -500 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.7	%/°C	V_{GS} = -10V, I_D = -150 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	125	—	—	mmho	V_{DS} = -25V, I_D = -350 mA
Input Capacitance	C_{ISS}	—	—	200	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	—	70	pF	
Reverse Transfer Capacitance	C_{RSS}	—	—	25	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	—	15	ns	V_{DD} = -25V, I_D = -250 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	—	20	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	25	ns	
Fall Time	t_f	—	—	50	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	-1.5	V	V_{GS} = 0V, I_{SD} = -750 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = -750 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 µs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	°C	
Storage Temperature	T_S	-55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-89	θ_{JA}	—	78.4	—	°C/W	**Note 1**

Note 1: Mounted on an FR5 board, 25 mm x 25 mm x 1.57 mm

THERMAL CHARACTERISTICS

Package	I_D (**Note 1**) (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at T_A = 25°C (**Note 2**) (W)	I_{DR} (**Note 1**) (mA)	I_{DRM} (A)
3-lead SOT-89	-231	-1.1	1.6	-231	-1.1

Note 1: I_D (continuous) is limited by maximum rated T_J.

2: Mounted on an FR5 board, 25 mm x 25 mm x 1.57 mm

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

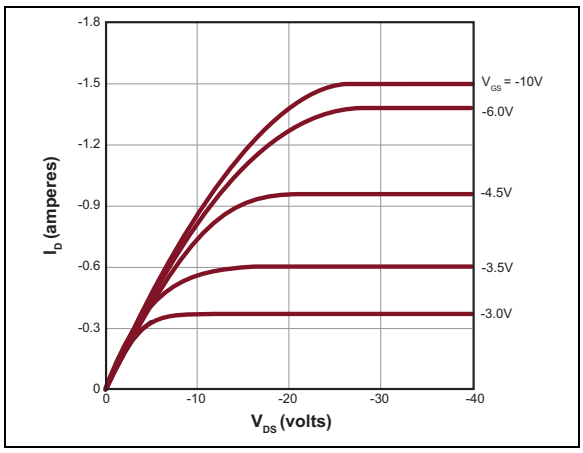

FIGURE 2-1: *Output Characteristics.*

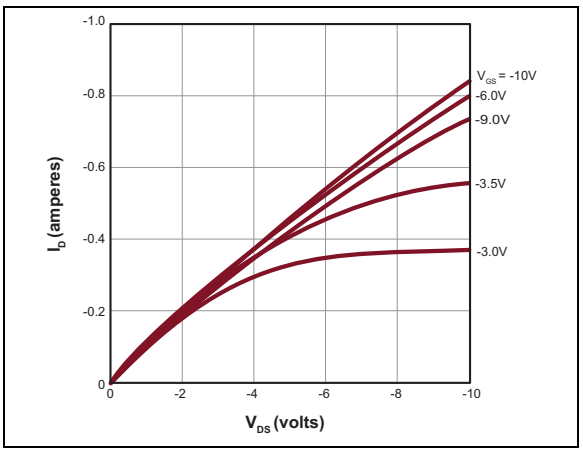

FIGURE 2-4: *Saturation Characteristics.*

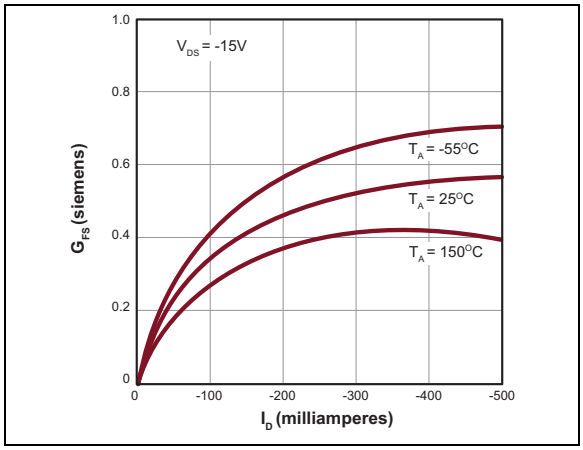

FIGURE 2-2: *Transconductance vs. Drain Current.*

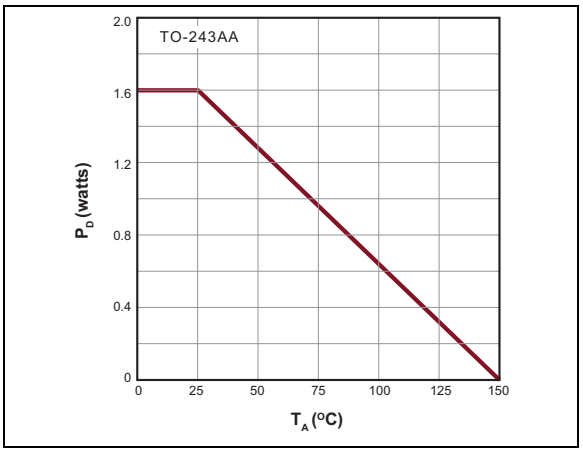

FIGURE 2-5: *Power Dissipation vs. Ambient Temperature.*

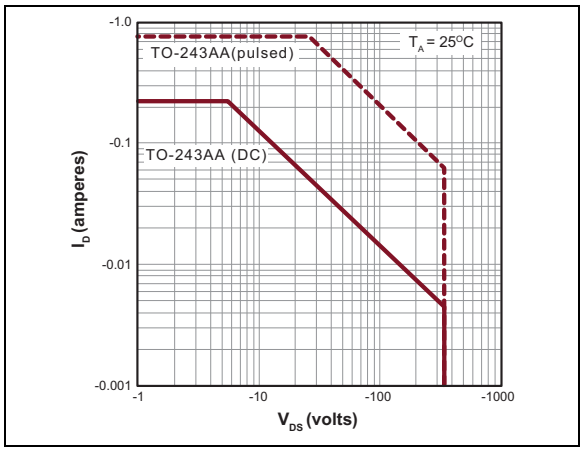

FIGURE 2-3: *Maximum Rated Safe Operating Area.*

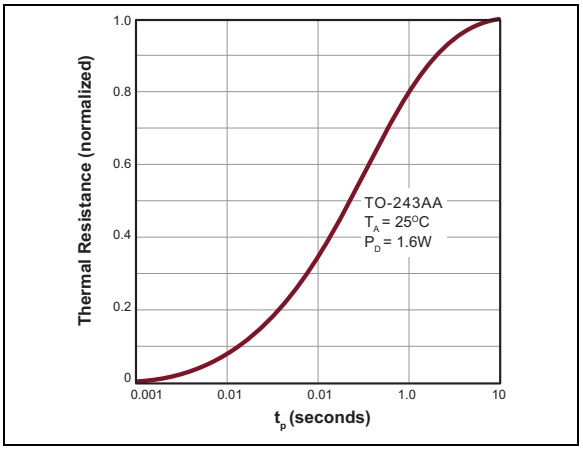

FIGURE 2-6: *Thermal Response Characteristics.*

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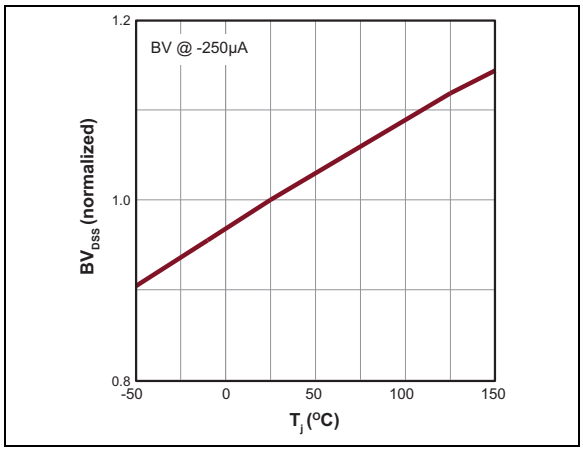

FIGURE 2-7: *BV_{DSS} Variation with Temperature.*

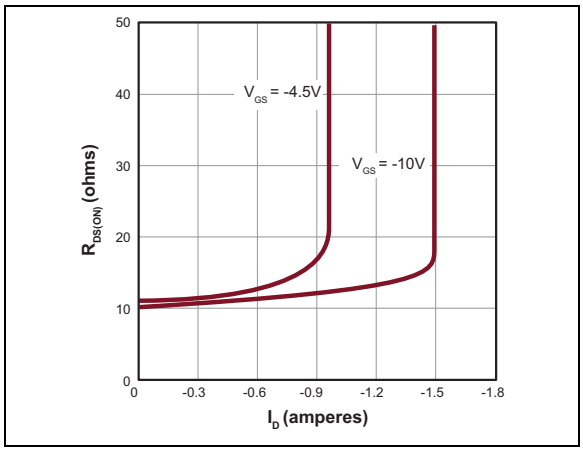

FIGURE 2-10: *On-Resistance vs. Drain Current.*

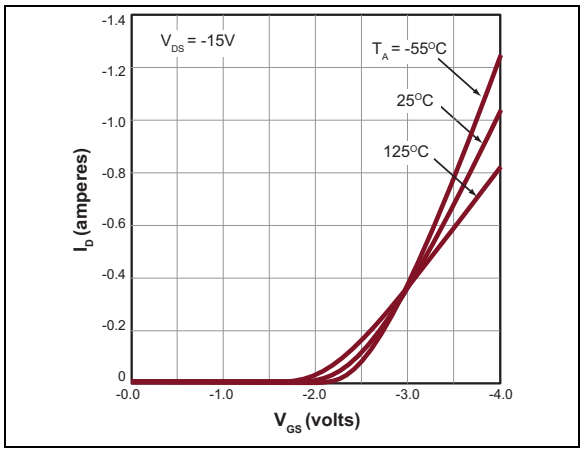

FIGURE 2-8: *Transfer Characteristics.*

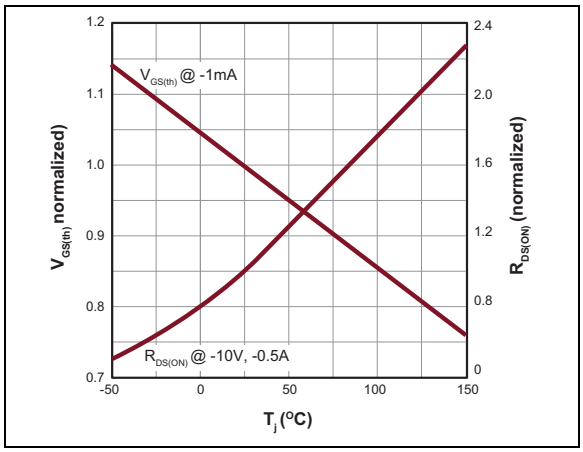

FIGURE 2-11: *$V_{GS(th)}$ and R_{DS} Variation with Temperature.*

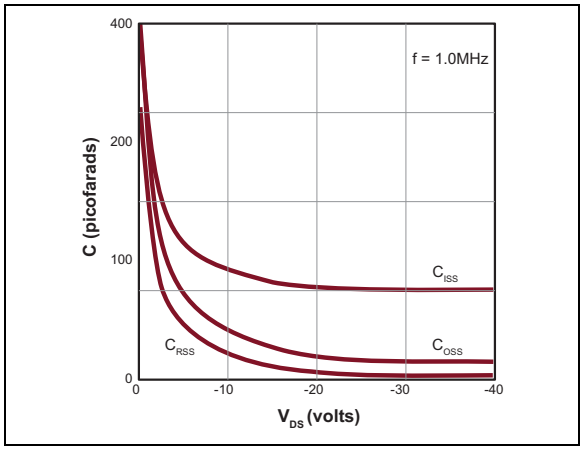

FIGURE 2-9: *Capacitance vs. Drain-to-Source Voltage.*

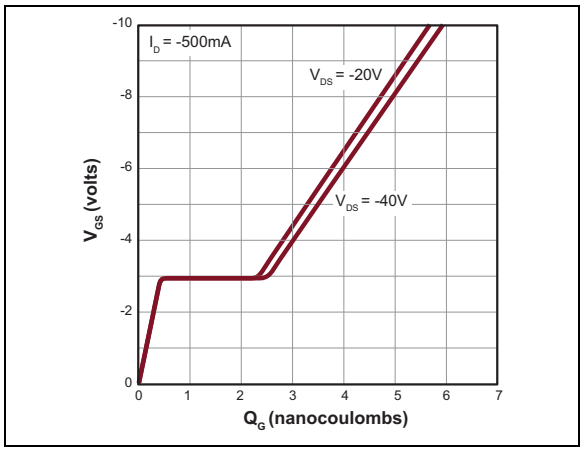

FIGURE 2-12: *Gate Drive Dynamic Characteristics.*

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3.0 PIN DESCRIPTION

The details on the pins of TP2435 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2, 4	Drain	Drain
3	Source	Source

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4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TP2435.

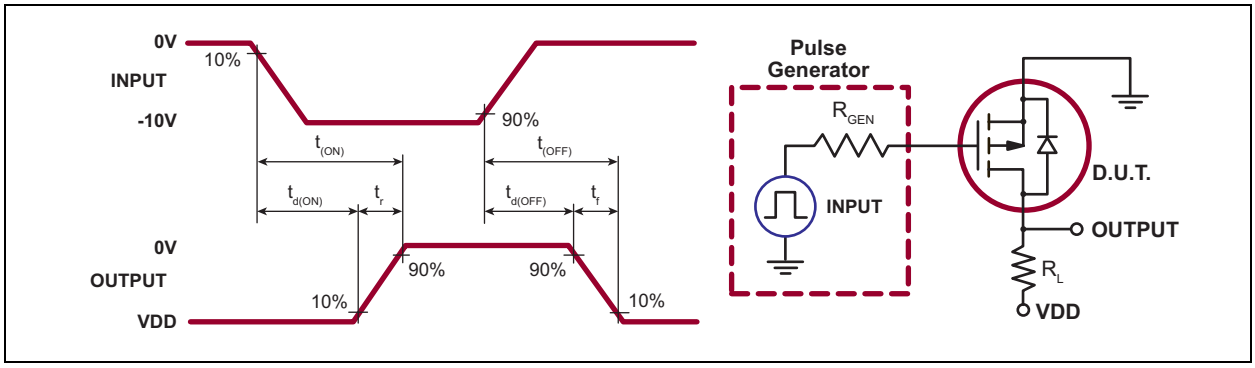

FIGURE 4-1: *Switching Waveforms and Test Circuit.*

TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(TH)}$ (Maximum) (V)	$I_{D(ON)}$ (Minimum) (mA)
-350	15	-2.4	-800

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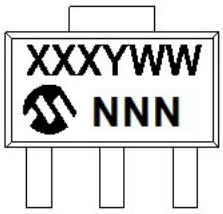
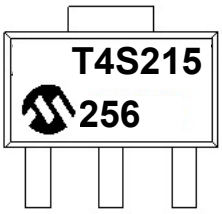
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

3-Lead SOT-89



Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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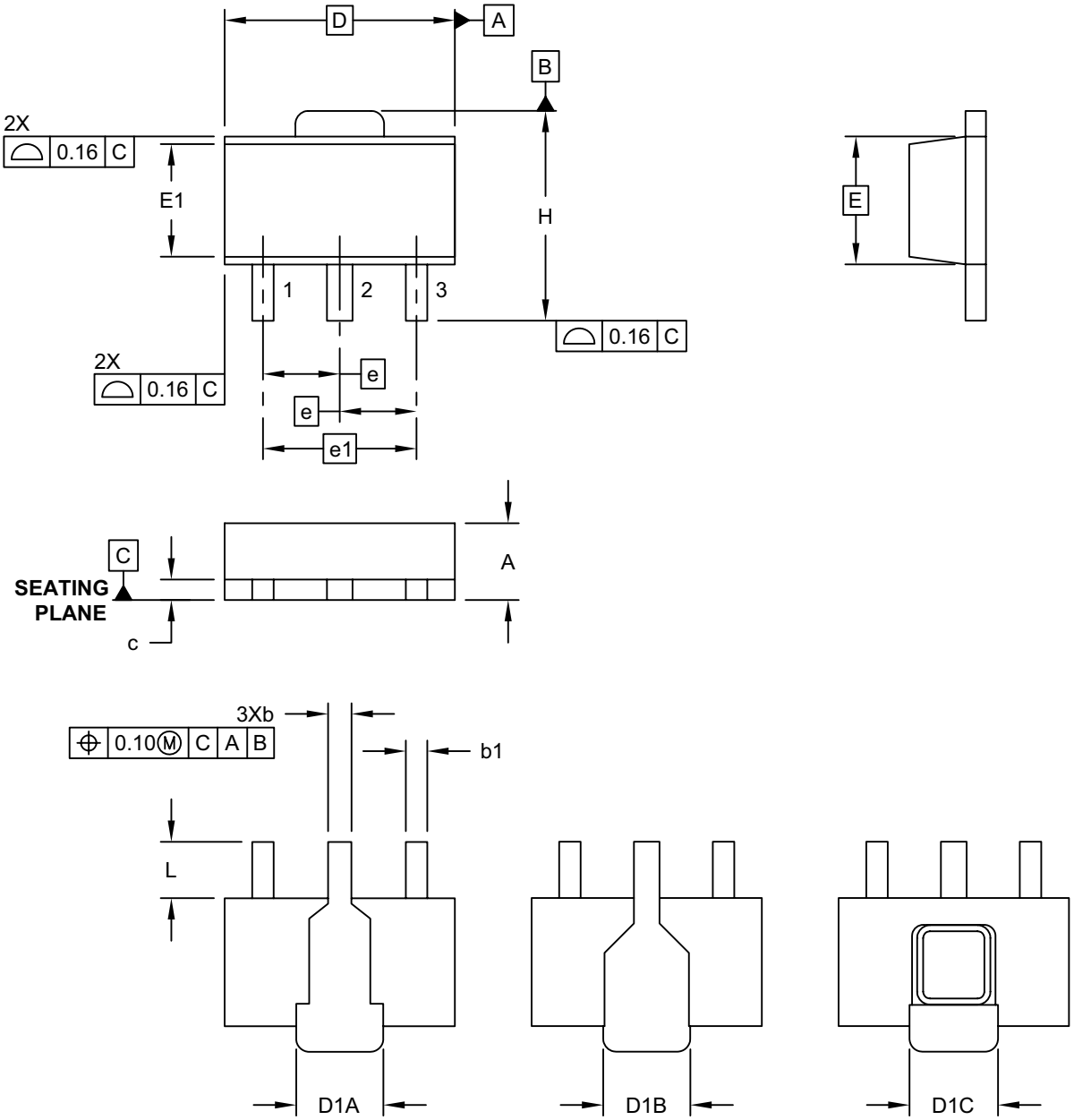
3-Lead Plastic Small Outline Transistor (MB) - [SOT-89]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



OPTIONAL BACKSIDE PATTERNS — PARTS MAY BE SUPPLIED WITH ANY PATTERN SHOWN

Microchip Technology Drawing C04-029C Sheet 1 of 2

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3-Lead Plastic Small Outline Transistor (MB) - [SOT-89]

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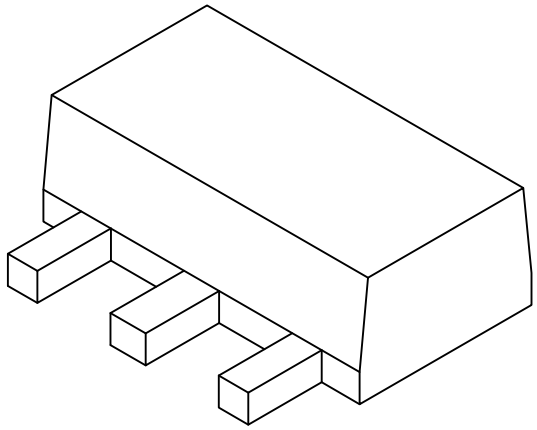

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		3	
Pitch	e		1.50 BSC	
Outside Lead Pitch	e1		3.00 BSC	
Overall Height	A	1.40	1.50	1.60
Overall Width	H	3.94	4.10	4.25
Molded Package Width at Base	E		2.50 BSC	
Molded Package Width at Top	E1	2.13	2.20	2.29
Overall Length	D		4.50 BSC	
Tab Length (Option A)	D1A	1.63	1.73	1.83
Tab Length (Option B)	D1B	1.40	1.60	1.75
Tab Length (Option C)	D1C	1.62	1.73	1.83
Foot Length	L	0.79	1.10	1.20
Lead Thickness	c	0.35	0.40	0.44
Lead 2 Width	b	0.41	0.50	0.56
Leads 1 & 3 Width	b1	0.36	0.42	0.48

Notes:

1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-029C Sheet 2 of 2

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3-Lead Plastic Small Outline Transistor (MB) - [SOT-89]

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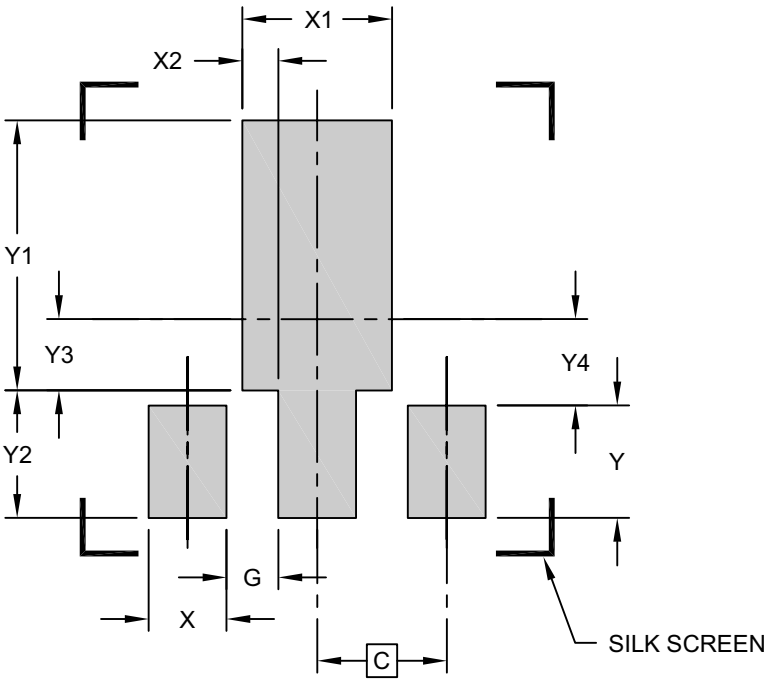

RECOMMENDED LAND PATTERN

Units	MILLIMETERS		
Dimension Limits	MIN	NOM	MAX
C		1.50 (BSC)	
X (3 PLACES)		0.900	
X1		1.733	
X2 (2 PLACES)		0.416	
G (2 PLACES)		0.600	
Y (2 PLACES)		1.300	
Y1		3.125	
Y2		1.475	
Y3		0.825	
Y4		1.000	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2029C

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision B (October 2022)

- Updated typical value in **Section "Package Thermal Resistance"**.
- Updated package markings and drawings in **Section 5.0 "Packaging Information"**.
- Minor text and format changes throughout.

Revision A (October 2019)

- Converted Supertex Doc# DSFP-TP2435 to Microchip DS20005961A.
- Added a pin function table.
- Changed the package marking format.
- Made minor text changes throughout the document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-X	-X
Device	Package Options	Environmental	Media Type

Device:	TP2435	=	P-Channel Enhancement-Mode Vertical DMOS FET
Package:	N8	=	3-Lead SOT-89
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	2000/Reel for an N8 Package

Example:

a) TP2435N8-G: P-Channel Enhancement-Mode, Vertical DMOS FET, 3-Lead SOT-89, 2000/Reel

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